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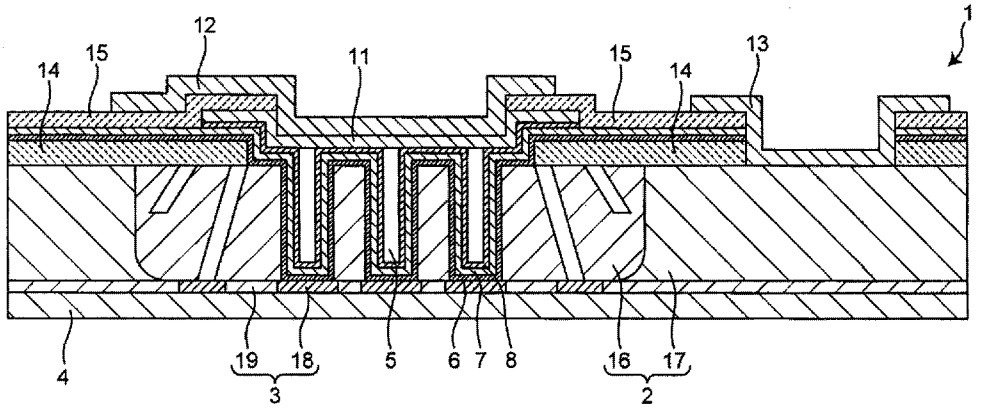
(54) Title: CAPACITOR

Fig. 1



(57) Abstract: The present invention provides a capacitor including: a base material including a pore structure part; a metal layer provided on one main surface of the base material; an extended layer provided on the metal layer; a lower electrode layer provided on surfaces of pores in the pore structure part; a dielectric layer provided on the lower electrode layer; and an upper electrode layer provided on the dielectric layer, where at least some of the pores penetrate the base material, the metal layer has a sealing part that seals one opening of a pore that penetrates, and the sealing part is conductive, and the lower electrode layer is electrically connected to the extended layer through the sealing part of the metal layer.

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Description

Title of Invention: CAPACITOR

Technical Field

[0001] The present invention relates to a capacitor.

Background Art

[0002] In recent years, there is a growing demand for reduction in size and increase in capacitance for capacitors. In response to such a demand, capacitors have been proposed which have a metal-dielectric-metal (hereinafter also referred to as an "MIM") structure formed on a base material that has a surface area increased by a fine structure such as a porous structure. For example, Patent Document 1 discloses a capacitor that has an MIM structure provided in a nanotube formed in an aluminum base material. The nanotube structure in Patent Document 1, which can be obtained by anodically oxidizing an aluminum base material, has very fine and high-density pores. The capacitor in Patent Document 1 has a capacitance increased by providing the MIM structure in such fine and high-density pores.

Citation List

Patent Literature

[0003] [Patent Literature 1] US Pat. No. 8,912,522

Summary of Invention

Technical Problem

[0004] As described in Patent Document 1, high capacitance can be ensured by providing a porous structure in the base material and forming a capacitor structure in the pores. In the case of providing a capacitor structure in the pores, however, there is the problem of equivalent series resistance (hereinafter also referred to as "ESR") increased, because of the thin capacitor electrodes, in particular, because the lower electrode has a relatively long distance to an external electrode.

[0005] In order to reduce the ESR of a capacitor with a nanotube structure as in Patent Document 1, it is conceivable to extend the lower electrode from the bottom of the pore, and connect the extended electrode to the external electrode through a conductive layer which is larger in cross-sectional area and is disposed below the base material. In a case where such a structure is to be applied, it is necessary to provide a conductive layer on one main surface of the aluminum base material and perform anodic oxidation from the other main surface, and it is necessary to provide a barrier layer between the aluminum base material and the conductive layer such that the conductive layer is not eroded by the anodic oxidation. It is conceivable to use a tungsten layer as such a barrier layer, but in this case, when a pore is formed by the anodic oxidation to

penetrate the aluminum, the tungsten layer exposed to the bottom of the pore can also be oxidized. Since such tungsten oxide has low conductivity, the lower electrode in the pore and the conductive layer are electrically cut off. Accordingly, it becomes necessary to remove the barrier layer at the pore bottom, and the manufacturing process will be complicated. In addition, the barrier layer at the pore bottom can be removed by etching, but in order to remove only this tungsten oxide, it is necessary to select the etching solution and set other conditions.

[0006] An object of the present disclosure is to provide a capacitor including a fine pore structure, without requiring the above-mentioned barrier layer removal step.

Solution to Problems

[0007] The present disclosure includes the following aspects:

[1] A capacitor including:

a base material including a pore structure part;

a metal layer provided on one main surface of the base material;

an extended layer provided on the metal layer;

a lower electrode layer provided on surfaces of pores in the pore structure part;

a dielectric layer provided on the lower electrode layer; and

an upper electrode layer provided on the dielectric layer,

where

at least some of the pores penetrate the base material,

the metal layer has a sealing part that seals one opening of a pore that penetrates, and the sealing part is conductive, and

the lower electrode layer is electrically connected to the extended layer through the sealing part of the metal layer.

[2] The capacitor according to the foregoing [1], where the base material is an aluminum base material, and is oxidized in the pore structure part.

[3] The capacitor according to the foregoing [1] or [2], where the metal layer is a layer of Ru, Re, Sn, Ti, V, Fe, a Li-Ti alloy, a Li-V alloy, or a Na-W alloy, and is oxidized in the sealing part.

[4] The capacitor according to any of the foregoing [1] to [3], where the metal layer is 10 nm or more and 1.0 μm or less in thickness.

Advantageous Effects of Invention

[0008] According to the present disclosure, a capacitor can be provided which is low in equivalent series resistance and easy to manufacture.

Brief Description of Drawings

[0009] [fig.1]Fig. 1 is a schematic cross-sectional view of a capacitor 1 according to an embodiment of the present disclosure.

[fig.2]Fig. 2 is a cross-sectional view for explaining a method for manufacturing the capacitor 1 according to the present disclosure.

[fig.3]Fig. 3 is a cross-sectional view for explaining the method for manufacturing the capacitor 1 according to the present disclosure.

[fig.4]Fig. 4 is a cross-sectional view for explaining the method for manufacturing the capacitor 1 according to the present disclosure.

[fig.5]Fig. 5 is a cross-sectional view for explaining the method for manufacturing the capacitor 1 according to the present disclosure.

[fig.6]Fig. 6 is a cross-sectional view for explaining the method for manufacturing the capacitor 1 according to the present disclosure.

[fig.7]Fig. 7 is a cross-sectional view for explaining the method for manufacturing the capacitor 1 according to the present disclosure.

[fig.8]Fig. 8 is a cross-sectional view for explaining the method for manufacturing the capacitor 1 according to the present disclosure.

[fig.9]Fig. 9 is a cross-sectional view for explaining the method for manufacturing the capacitor 1 according to the present disclosure.

Description of Embodiments

[0010] A capacitor according to the present disclosure will be described in detail below with reference to the drawings. However, the capacitor according to the present embodiment, and the shapes and arrangement of respective constructional elements are not limited to the examples shown in the figures.

[0011] A cross-sectional view of a capacitor 1 according to the present embodiment is schematically shown in FIG. 1.

[0012] As shown in FIG. 1, the capacitor 1 according to the present embodiment schematically includes a base material 2, a metal layer 3 provided on one main surface of the base material 2, and an extended layer 4 provided on the metal layer 3, a lower electrode layer 6 provided on the surfaces of pores 5 of the base material 2, a dielectric layer 7 provided on the lower electrode layer 6, and an upper electrode layer 8 provided on the dielectric layer 7. Furthermore, the capacitor 1 according to the present embodiment includes: an upper extended electrode 11 provided on the upper electrode layer 8 and a first external electrode 12 provided on the upper extended electrode 11; and a second external electrode 13 electrically insulated from the upper extended electrode 11 and the first external electrode 12 and electrically connected to the base material 2. The base material 2 has a pore structure part 16 and a non-pore structure part 17. The pore structure part 16 is not conductive, and the non-pore structure part 17 is conductive. The pore structure part 16 has a plurality of pores 5 formed, and at least some of the pores 5 penetrate the base material 2. One opening of the through-pore is

sealed with the metal layer 3. The metal layer 3 has a sealing part 18 that seals the opening of the pore 5. The sealing part 18 has an oxidized state, but has conductivity. The lower electrode layer 6-dielectric layer 7-upper electrode layer 8 constitute an MIM capacitor structure, and charge can be accumulated in the dielectric layer 7 by applying a voltage between the lower electrode layer 6 and the upper electrode layer 8. The lower electrode layer 6 is electrically connected to the extended layer 4 through the sealing part 18 of the metal layer 3. The extended layer 4 is electrically connected to a non-pore structure part 17 of the base material 2 through the metal layer 3. The non-pore structure part 17 of the base material 2 is electrically connected to the second external electrode 13. The upper electrode layer 8 is electrically connected to the upper extended electrode 11, and the upper extended electrode 11 is electrically connected to the external electrode 12. More specifically, in the capacitor 1 according to the present embodiment, the current on the side with the lower electrode layer 6 flows through in the order of lower electrode layer 6 - metal layer 3 (specifically sealing part 18) - extended layer 4 - metal layer 3 - non-pore structure part 17 of base material 2 - second external electrode 13 (or vice versa). Further, the current may partially flow through in the order of lower electrode layer 6 - metal layer 3 - non-pore structure part 17 of base material 2 - second external electrode 13, without passing through the extended layer 4. On the other hand, the current on the side with the upper electrode layer 8 flows through in the order of upper electrode layer 8 - upper extended electrode 11 - external electrode 12 (or vice versa).

[0013] The capacitor 1 as mentioned above is manufactured, for example, as follows.

[0014] (Layer Formation Step)

On a substrate 30, a layer 34 corresponding to the extended layer 4 is formed , a barrier layer 33 corresponding to the metal layer 3 is formed thereon, and a base layer 32 corresponding to the base material 2 is further formed thereon (FIG. 2).

[0015] The substrate 30 supports the base layer 32, the barrier layer 33, and the extended layer 34. After the capacitor is manufactured, the substrate 30 supports the base material 2, the metal layer 3, and the extended layer 4. The substrate 30 may be removed after manufacturing the capacitor.

[0016] The substrate 30 is not particularly limited, but a silicon wafer is preferably used.

[0017] The material constituting the extended layer 34 is not particularly limited as long as the material is conductive, and examples thereof include Al, Cu, Ag, Ti, Ta, or alloys thereof such as AlCu, or nitrides TiN and TaN.

[0018] The extended layer 34 may be a single layer, or may be multi-layer, for example, two-layer or three-layer.

[0019] According to one aspect, the extended layer 34 is a single layer.

[0020] According to another embodiment, the extended layer 34 is multi-layer, and can be

preferably a three-layer structure of TiN-AlCu-TiN.

[0021] The thickness of the extended layer 34 (the total in the case of a multi-layer) can be, for example, 0.5 μm or more and 20 μm or less, preferably 1 μm or more and 10 μm or less, more preferably 2 μm or more and 5 μm or less. The thickness of the layer is adjusted to 0.5 μm or more, thereby allowing the equivalent series resistance to be reduced. The thickness of the layer is increased, thereby allowing the equivalent series resistance to be further reduced. On the other hand, the thickness of the layer is adjusted to 20 μm or less, thereby allowing the capacitor to be further reduced in height.

[0022] The method for forming the extended layer 34 is not particularly limited, and physical vapor deposition (PVD), chemical vapor deposition (CVD), sputtering, plating, and the like can be used. Preferably, PVD or CVD is used.

[0023] The barrier layer 33 prevents etching from proceeding to the extended layer 4 in a subsequent step, i.e., a step of etching the base layer 32 by anodic oxidation. In this regard, the barrier layer 33 exposed to an etching solution at the bottoms of the through pores is oxidized to serve as the sealing part 18.

[0024] Examples of the material constituting the barrier layer 33 corresponding to the metal layer 3 include Ru, Re, Sn, Ti, V, Fe, Li-Ti alloys, Li-V alloys, or Na-W alloys.

[0025] The thickness of the barrier layer 33 can be, for example, 100 nm or more and 2.0 μm or less, preferably 150 nm or more and 1.0 μm or less, more preferably 200 nm or more and 500 nm or less. The thickness of the layer is adjusted to 100 nm or more, thereby making it possible to achieve the effect of preventing the etching from proceeding. The effect mentioned above can be further enhanced by increasing the thickness of the layer. On the other hand, when the thickness of the layer is adjusted to 2.0 μm or less, the thickness of the sealing part 18 after the capacitor formation is also 2.0 μm or less, thereby allowing the resistance between the lower electrode layer 6 and the extended layer 4 to be reduced. Reducing the thickness of the layer also reduces the thickness of the sealing part 18 after the capacitor formation, thereby allowing the resistance between the lower electrode layer 6 and the extended layer 4 to be further reduced.

[0026] The method for forming the barrier layer 33 is not particularly limited, and physical vapor deposition (PVD), chemical vapor deposition (CVD), sputtering, plating, and the like can be used. Preferably, PVD or CVD is used.

[0027] Examples of the material constituting the layer 32 corresponding to the base material 2 include Al, Ti, Nb, Mg, Zn, Fe, W, Zr, or Ta. Preferably, the material is Al.

[0028] The thickness of the base layer 32 can be, for example, 1 μm or more and 100 μm or less, preferably 5 μm or more and 50 μm or less, more preferably 8 μm or more and 30 μm or less. The thickness of the layer is adjusted to 1 μm or more, thereby increasing

the depth of pores to be formed later, and then increasing the capacitance of the capacitor obtained. The increased thickness of the layer can further increase the capacitance of the capacitor. On the other hand, the thickness of the layer is adjusted to 100 μm or less, thereby allowing the capacitor to be reduced in thickness, and makes it easier to form pores.

[0029] The method for forming the base layer 32 is not particularly limited, and physical vapor deposition (PVD), chemical vapor deposition (CVD), sputtering, plating, and the like can be used. Preferably, PVD or CVD is used.

[0030] (Etching Step)

First, a mask 44 corresponding to a part an insulating part 14 is formed on the base layer 32, except for a part where the pore structure part 16 is formed (FIG. 3).

[0031] The material constituting the mask 44 corresponding to a part of the insulating part 14 is not particularly limited as long as the material is resistant to an etching agent for use in the subsequent etching step, and examples of the material include SiO_2, SiN, or SiON. Preferably, the material is SiO_2.

[0032] The thickness of the mask 44 can be, for example, 0.1 μm or more and 10 μm or less, preferably 0.5 μm or more and 5 μm or less, for example, 1 μm or more and 3 μm or less. The thickness of the layer is adjusted to 0.1 μm or more, thereby allowing the base layer 32 in the mask part to be prevented from being etched. In addition, it is possible to improve the insulation property between the non-pore structure part 17 of the base material 2 and the lower electrode layer 6 on the insulating part 14 after the capacitor formation. The thickness of the mask 44 is further increased, thereby allowing the etching to be prevented more reliably from proceeding, and allowing the insulation property to be further improved. On the other hand, the thickness of the mask 44 is adjusted to 10 μm or less, thereby allowing the capacitor to be further reduced in thickness.

[0033] The method for forming the mask 44 is not particularly limited, and examples of the method include a vacuum vapor deposition method, a chemical vapor deposition method, a sputtering method, an atomic layer deposition (ALD), and a pulsed laser deposition method (PLD). For example, the mask can be obtained by forming a mask layer on the entire base layer 32 and then removing, by etching or the like, the mask layer on the part where the pore structure part 16 is to be formed. As an alternative method, the mask 44 may be formed selectively at a site to be protected.

[0034] Next, the base layer 32 is etched by anodic oxidation to form the pore structure part 16 in the base layer 32 (FIG. 4).

[0035] The conditions for the anodic oxidation treatment, such as the etching solution, the temperature, the time, the current density, and the voltage, for example, can be selected depending on the material of the base layer 32, the desired pore structure, and the like.

[0036] The etching solution is an etching solution that is capable of etching the base layer 32, but does not etch the barrier layer 33. As such an etching solution, for example, an oxalic acid, a phosphoric acid, a sulfuric acid, a chromic acid, or the like can be used. The etching solution is preferably an oxalic acid.

[0037] A preferred combination of the etching solution, the material constituting the base layer 32, and the material constituting the barrier layer 33 is that: the etching solution is an oxalic acid; the material constituting the base layer 32 is Al; and the material constituting the barrier layer 33 is Ru.

[0038] The etching step anodically oxidizes a part of the base layer 32 to form the pore structure part 16. The part which is not anodically oxidized because of the masking serves as the non-pore structure part 17.

[0039] According to one aspect, the base layer 32 is an aluminum layer, and after the etching step, the treated part becomes anodized aluminum and constitutes the pore structure part 16. The untreated part remains aluminum and constitutes the non-pore structure part 17. More specifically, the base layer 32 serves as the base material 2 composed of the pore structure part 16 and the non-pore structure part 17 after the etching step.

[0040] The pore structure part 16 formed by the etching step has a large number of pores formed. At least some of the pores penetrate the base layer 32 and reach the barrier layer 33. According to a preferred aspect, 80% or more, preferably 90% or more, more preferably 98% or more of the pores penetrate through the base layer 32. According to a preferred embodiment, when the pore structure part 16 is planarly viewed from the main surface where the base layer 32 is started to be etched, in a region of 10 μm or more inside, preferably 5 μm or more inside, more preferably 1 μm or more inside from the boundary between the pore structure part 16 and the non-pore structure part 17, 90% or more, preferably substantially all of the pores penetrate the base layer 32. In this regard, the boundary between the pore structure part 16 and the non-pore structure part 17 refers to the boundary between the region oxidized by the anodic oxidation and the region which is not oxidized.

[0041] The shape of the pore 5 is not particularly limited. According to a preferred embodiment, the pore 5 has a cylindrical shape with an axis in the thickness direction of the base material 2.

[0042] The width of the pore 5 (the diameter in the case of a cylindrical shape) is preferably 5 nm or more and 300 nm or less, more preferably 20 nm or more and 200 nm or less.

[0043] The density of the pores 5 is not particularly limited, but is preferably 1×10^8 pores/cm^2 or more and 1×10^{12} pores/cm^2 or less, more preferably 1×10^9 pores/cm^2 or more and 1×10^{11} pores/cm^2 or less.

[0044] The barrier layer 33 is not etched even in a case where the layer is exposed to the

etching solution in the etching step. More specifically, the barrier layer 33 has the function of keeping the etching from proceeding, and seals one opening of the pore 5 to form the sealing part 18. A part of the barrier layer 33 exposed to the etching solution, that is, the sealing part 18 can be oxidized. In a case where the sealing part 18 is not sufficiently oxidized, and is preferably further oxidized, the sealing part 18 may be further oxidized by heating or the like.

[0045] The barrier layer 33 in the capacitor according to the present disclosure is made of a metal with conductivity, even in a case where the layer is oxidized in the etching step. More specifically, both the sealing part 18 and the other part 19 of the barrier layer 33 have conductivity after the etching step. As mentioned above, examples of the metal constituting the barrier layer 33 include Ru, Re, Sn, Ti, V, Fe, Li-Ti alloys, Li-V alloys, or Na-W alloys, and preferably, examples of respective oxides of the metals includes RuO_2, ReO_3, SnO_2, TiO_2, V_2O_3, Fe_3O_4, $LiTi_2O_4$, LiV_2O_4, and $NaWO_3$.

[0046] The use of the metal mentioned above as the metal constituting the barrier layer 33 ensure, even if the sealing part 18 is present between the lower electrode layer 6 of the capacitor structure to be subsequently formed in the pores 5 and the extended layer 4, the electrical connection between the lower electrode layer 6 and the extended layer 4. On the other hand, in a case where a material that conducts no electricity when the material is oxidized, such as tungsten, is used for the barrier layer 33, it is necessary to remove the sealing part 18 present between the lower electrode layer 6 and the extended layer 4 in order to ensure the electrical connection between the lower electrode layer 6 and the extended layer 4. In this case, the sealing part 18 has to be removed without affecting the base material 2, and an extremely difficult treatment is required. On the other hand, in the capacitor according to the present disclosure, the sealing part 18 has conductivity, and the electrical connection between the lower electrode layer 6 and the extended layer 4 can be thus ensured without removing the sealing part 18. More specifically, the capacitor according to the present disclosure is easy to manufacture.

[0047] (Capacitor Structure Formation Step)

Next, the MIM capacitor structure of lower electrode layer 6 - dielectric layer 7 - upper electrode layer 8 is formed.

[0048] First, a mask 45 is formed which covers a region of the pore structure part 16 where there are pores that do not penetrate the base layer 32 and pores that penetrate the base layer 32 but have pore axes greatly inclined with respect to the thickness direction of the base layer 32 (FIG. 5). In this regard, the pores with the axes greatly inclined preferably refer to pores which are preferably 30° or more, more preferably 20° or more, even more preferably 10° or more inclined with respect to the thickness direction of the base layer 32, preferably . Since the pores that do not penetrate and the pores

with the axes inclined have variations in pore depth (length), there is a possibility that the surface area may vary, and thus, the electrical characteristics of the capacitor may vary. Covering such pores with the mask 45 makes it possible to obtain a capacitor with small variations in electrical characteristics.

[0049] The material constituting the mask 45 is not limited as long as the material is resistant to the subsequent layer formation step, typically an atomic layer deposition step, and examples of the material include SiO_2, SiN, or SiON. Preferably, the material is SiO_2.

[0050] According to one embodiment, the mask 45 is made of the same material as the mask 44. The mask 44 and the mask 45 are made of the same material, thereby improving the adhesion between both the layers, and allowing the generation of stress between both the layers to be suppressed. According to a preferred aspect, since SiO_2 has resistance to both the etching step and the ALD step, the mask 44 and the mask 45 are both SiO_2.

[0051] The thickness of the mask 45 can be, for example, 0.1 μm or more and 10 μm or less, preferably 0.5 μm or more and 5 μm or less, for example, 1 μm or more and 3 μm or less. The thickness of the layer is adjusted to 0.1 μm or more, thereby allowing the base layer 32 in the mask part to be prevented from being etched. In addition, it is possible to improve the insulation property between the non-pore structure part 17 of the base material 2 and the lower electrode layer 6 on the insulating part 14 after the capacitor formation. The thickness of the mask 44 is further increased, thereby allowing the etching to be prevented more reliably from proceeding, and allowing the insulation property to be further improved. On the other hand, the thickness of the mask 44 is adjusted to 10 μm or less, thereby allowing the capacitor to be further reduced in thickness.

[0052] The method for forming the mask 45 is not particularly limited, and examples of the method include a vacuum vapor deposition method, a chemical vapor deposition method, a sputtering method, ALD, and PLD.

[0053] Next, an MIM structure is formed on the base layer 32 (base material 2) including the inside of the pores 5 (FIG. 6).

[0054] First, the lower electrode layer 6 is formed.

[0055] The material that forms the lower electrode layer 6 mentioned above is not particularly limited as long as the material is conductive, and examples of the material include Ni, Cu, Al, W, Ti, Ag, Au, Pt, Zn, Sn, Pb, Fe, Cr, Mo, Ru, Pd, and Ta and alloys thereof, e.g., CuNi, AuNi, AuSn, and metal oxides and metal oxynitrides such as TiN, TiAlN, TiON, TiAlON, and TaN.

[0056] The thickness of the lower electrode layer 6 is not particularly limited, but is preferably 10 to 50 nm, for example. The thickness of the lower electrode layer is

increased, for example, to 10 nm or more, allowing the ESR to be further reduced. In addition, the thickness of the lower electrode layer is decreased, for example, to 50 nm or less, thereby making it possible to form a MIM structure without filling the pores, that is, without reducing the surface area of the base material 2, and allowing high capacitance to be achieved.

[0057] The method for forming the lower electrode layer 6 is not particularly limited, and examples of the method include a vacuum vapor deposition method, a chemical vapor deposition method, a sputtering method, ALD, and PLD. The ALD is preferred, because the ALD can form a more homogeneous and denser film even in microscopic regions of the pores.

[0058] Next, the dielectric layer 7 is formed on the lower electrode layer 6.

[0059] The material that forms the dielectric layer 7 mentioned above is not particularly limited as long as the material has an insulating property, but examples thereof preferably include metal oxides such as AlO_x (e.g., Al_2O_3), SiO_x (e.g., SiO_2), $AlTiO_x$, $SiTiO_x$, HfO_x, TaO_x, ZrO_x, $HfSiO_x$, $ZrSiO_x$, $TiZrO_x$, $TiZrWO_x$, TiO_x, $SrTiO_x$, $PbTiO_x$, $BaTiO_x$, $BaSrTiO_x$, $BaCaTiO_x$, and $SiAlO_x$; metal nitrides such as AlN_x, SiN_x, and $AlScN_x$; or metal oxynitrides such as AlO_xN_y, SiO_xN_y, $HfSiO_xN_y$, and SiC_xO_yNz, and AlO_x, SiO_x, SiO_xN_y, and $HfSiO_x$ are preferred. It is to be noted that the formulas mentioned above are merely intended to represent the constitutions of the materials, but not intended to limit the compositions. More specifically, the x, y, and z attached to O and N may have any value larger than 0, and the respective elements including the metal elements may have any presence proportion.

[0060] The thickness of the dielectric layer 7 mentioned above is not particularly limited, but for example, preferably 5 nm or more and 100 nm or less, more preferably 10 nm or more and 50 nm or less. The dielectric layer of 5 nm or more in thickness can increase the insulating property, and thus allows leakage current to be reduced. In addition, the dielectric layer of 100 nm or less in thickness makes it possible to achieve higher electrostatic capacitance.

[0061] The method for forming the dielectric layer 7 is not particularly limited, and examples of the method include a vacuum vapor deposition method, a chemical vapor deposition method, a sputtering method, ALD, and PLD. The ALD is preferred, because the ALD can form a more homogeneous and denser film even in microscopic regions of the pores.

[0062] Next, the upper electrode layer 8 is formed on the dielectric layer 7.

[0063] The material constituting the upper electrode layer 8 mentioned above is not particularly limited as long as the material is conductive, and examples of the material include Ni, Cu, Al, W, Ti, Ag, Au, Pt, Zn, Sn, Pb, Fe, Cr, Mo, Ru, Pd, and Ta and alloys thereof, e.g., CuNi, AuNi, AuSn, and metal oxides and metal oxynitrides such as

TiN, TiAlN, TiON, TiAlON, and TaN.

[0064] The thickness of the upper electrode layer 8 is not particularly limited, but is preferably 10 to 50 nm, for example. The thickness of the lower electrode layer is increased, for example, to 10 nm or more, allowing the ESR to be further reduced.

[0065] The method for forming the lower electrode layer 6 is not particularly limited, and examples of the method include a vacuum vapor deposition method, a chemical vapor deposition method, a sputtering method, ALD, and PLD. The ALD is preferred, because the ALD can form a more homogeneous and denser film even in microscopic regions of the pores.

[0066] (External Electrode Formation Step)

Next, the external electrodes 12 and 13 are formed.

[0067] First, the upper extended electrode 11 is formed on the upper electrode layer 8 (FIG. 7).

[0068] The material constituting the upper extended electrode 11 mentioned above is not particularly limited as long as the material has a conductive property, but examples of the material include Ni, Cu, Al, W, Ti, Ag, Au, Pt, Zn, Sn, Pb, Fe, Cr, Mo, Ru, Pd, and Ta and alloys thereof, e.g., CuNi, AuNi, AuSn, metal oxides and metal oxynitrides such as TiN, TiAlN, TiON, TiAlON, TaN, and electrically conductive polymers (for example, PEDOT (poly(3,4-ethylenedioxythiophene)), polypyrrole, polyaniline).

[0069] The thickness of the upper extended electrode 11 is not particularly limited, but for example, preferably 3 nm or more, more preferably 10 nm or more. The upper extended electrode of 3 nm or more in thickness can reduce the resistance of the upper extended electrode itself. In addition, the upper extended electrode 11 may be formed so as to fill the inside of the pores 5. The ESR is further reduced by filling the inside of the pores with the upper extended electrode.

[0070] The upper extended electrode 11 may be formed by a method such as a chemical vapor deposition method, a plating method, a bias sputtering method, a Sol-Gel method, conductive polymer filling, or ALD. Moreover, multiple methods may be combined for the formation.

[0071] Then, the surface a part of the base layer 32 electrically connected to the lower electrode layer 6 is partially exposed (FIG. 8), and the second external electrode 13 and first external electrode 12 are formed respectively on the exposed part 46 and the upper extended electrode 11 (FIG. 9).

[0072] The materials constituting the first external electrode 12 and second external electrode 13 are not particularly limited, but examples of the materials include metals such as Au, Pb, Ag, Sn, Ni, and Cu, and alloys thereof, and electrically conductive polymers.

[0073] The method for forming the first external electrode 12 and the second external

electrode 13 is not particularly limited, but for example, CVD, electrolytic plating, electroless plating, vapor deposition, sputtering, conductive paste baking, and the like can be used, and electrolytic plating, electroless plating, vapor deposition, sputtering, and the like are preferred.

[0074] While the capacitor 1 according to the present embodiment has been described above, various modifications can be made to the capacitor according to the present disclosure.

Industrial Applicability

[0075] The capacitor according to the present disclosure is small in size, high in capacitance, and further low in equivalent series resistance, and thus can be used for various applications.

Reference Signs List

[0076] 1 capacitor
2 base material
3 metal layer
4 extended layer
5 pore
6 lower electrode layer
7 dielectric layer
8 upper electrode layer
11 upper extended electrode
12 first external electrode
13 second external electrode
16 pore structure part
17 non-pore structure part
18 sealing part
19 other part
30 substrate
32 base layer
33 barrier layer
34 extended layer
44 mask
45 mask

Claims

[Claim 1] A capacitor comprising:
a base material comprising a pore structure part;
a metal layer provided on one main surface of the base material;
an extended layer provided on the metal layer;
a lower electrode layer provided on surfaces of pores in the pore structure part;
a dielectric layer provided on the lower electrode layer; and
an upper electrode layer provided on the dielectric layer,
wherein
at least some of the pores penetrate the base material,
the metal layer has a sealing part that seals one opening of a pore that penetrates, and the sealing part is conductive, and
the lower electrode layer is electrically connected to the extended layer through the sealing part of the metal layer.

[Claim 2] The capacitor according to claim 1, wherein the base material is an aluminum base material, and is oxidized in the pore structure part.

[Claim 3] The capacitor according to claim 1 or 2, wherein the metal layer is a layer of Ru, Re, Sn, Ti, V, Fe, a Li-Ti alloy, a Li-V alloy, or a Na-W alloy, and is oxidized in the sealing part.

[Claim 4] The capacitor according to any one of claims 1 to 3, wherein the metal layer is 10 nm or more and 1.0 μm or less in thickness.

[Fig. 1]

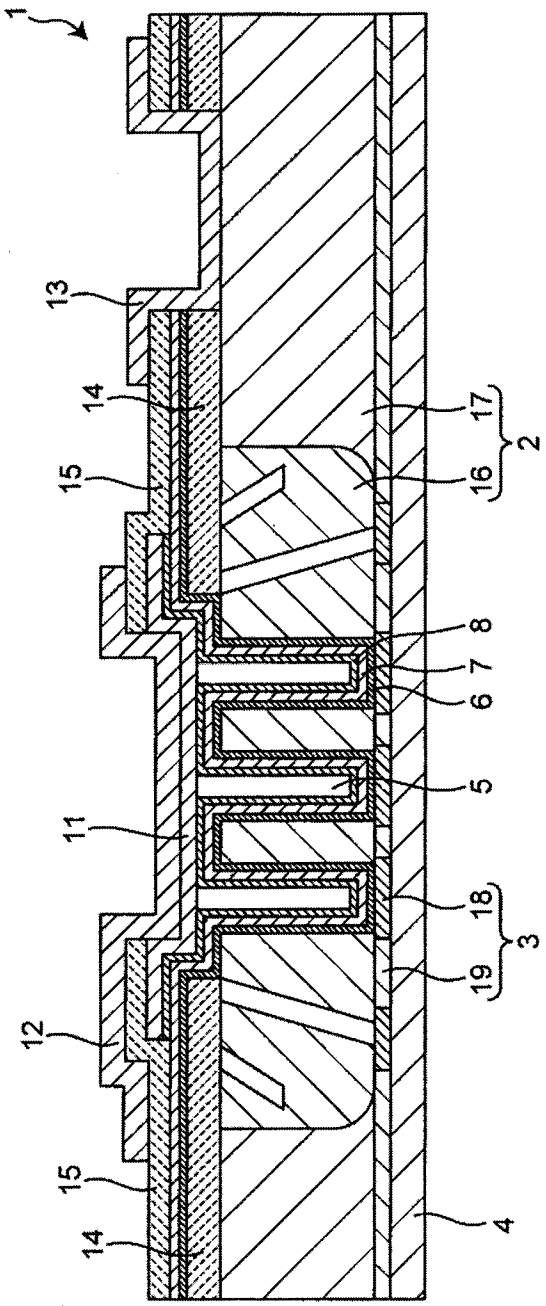

Fig. 1

[Fig. 2]

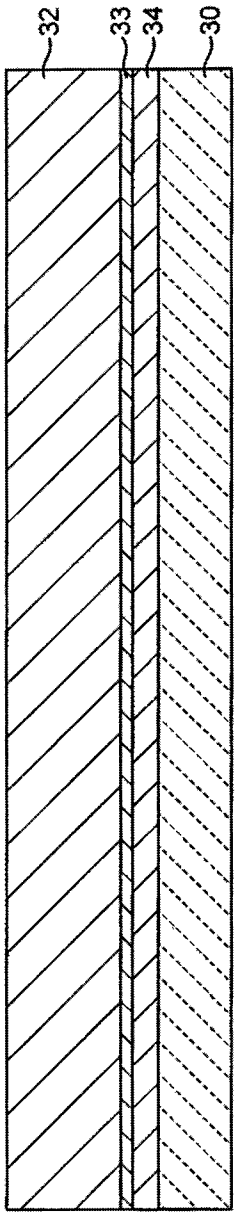

Fig. 2

[Fig. 3]

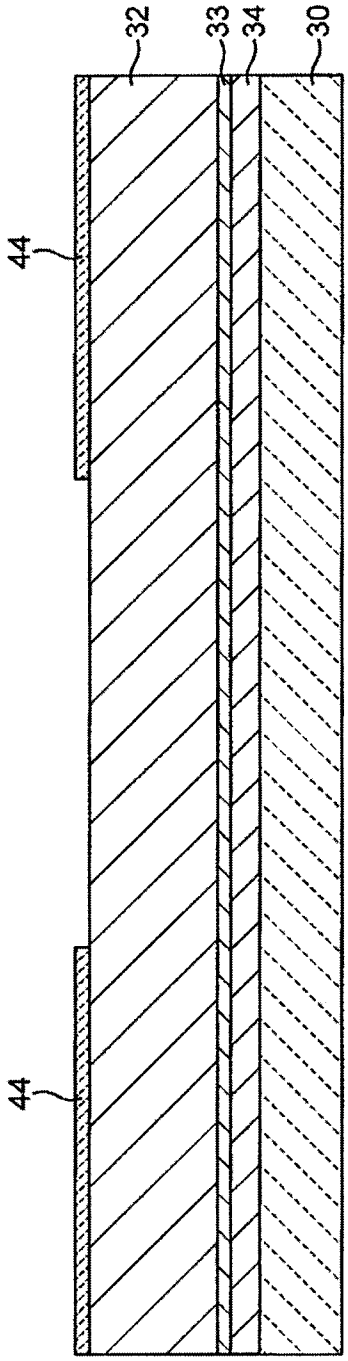

Fig. 3

[Fig. 4]

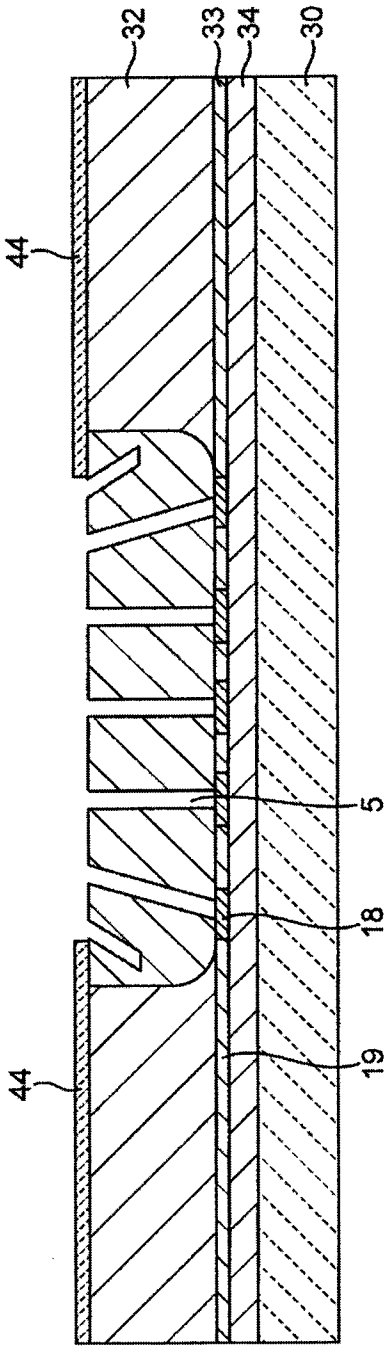

Fig. 4

[Fig. 5]

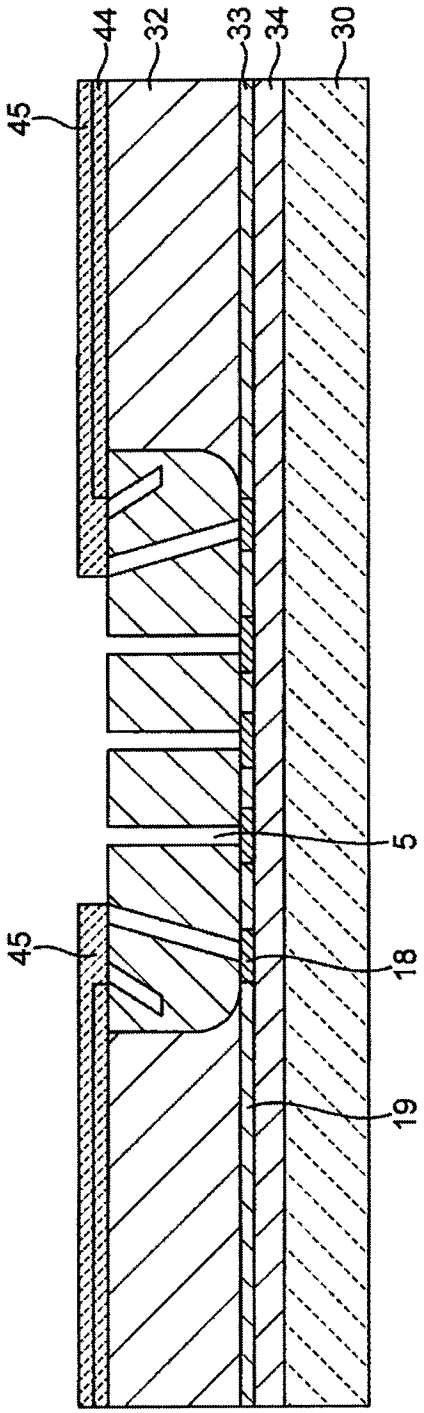

Fig. 5

[Fig. 6]

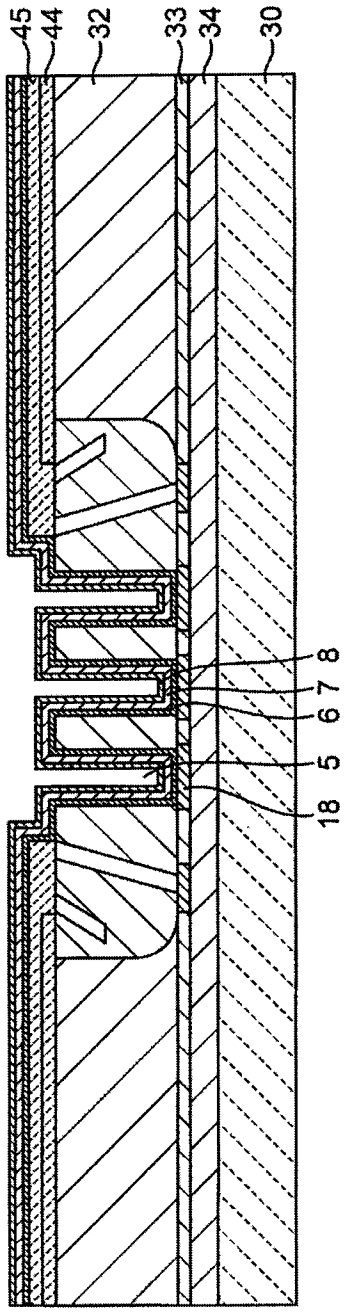

Fig. 6

[Fig. 7]

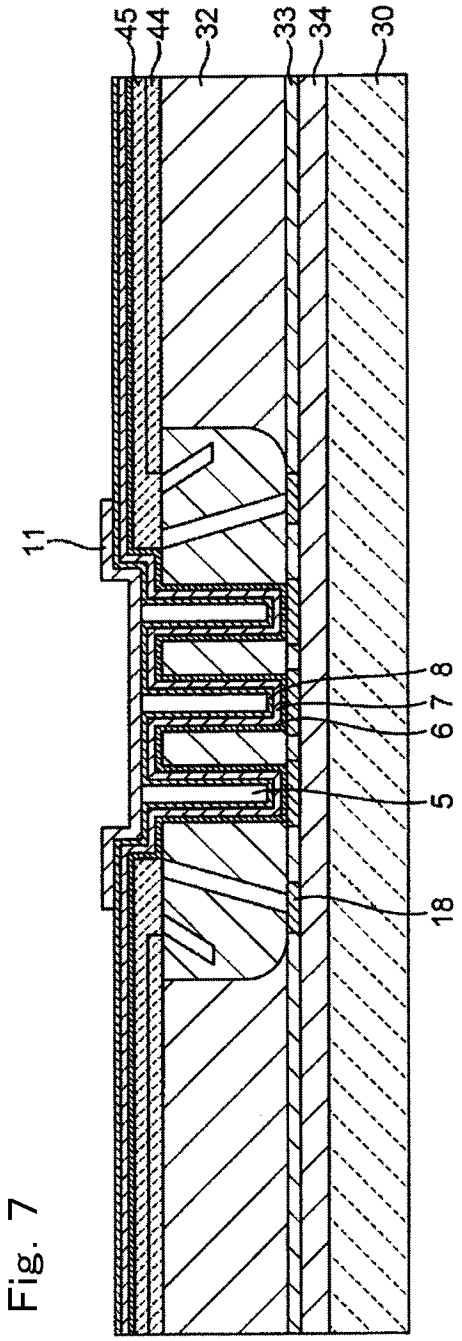

Fig. 7

[Fig. 8]

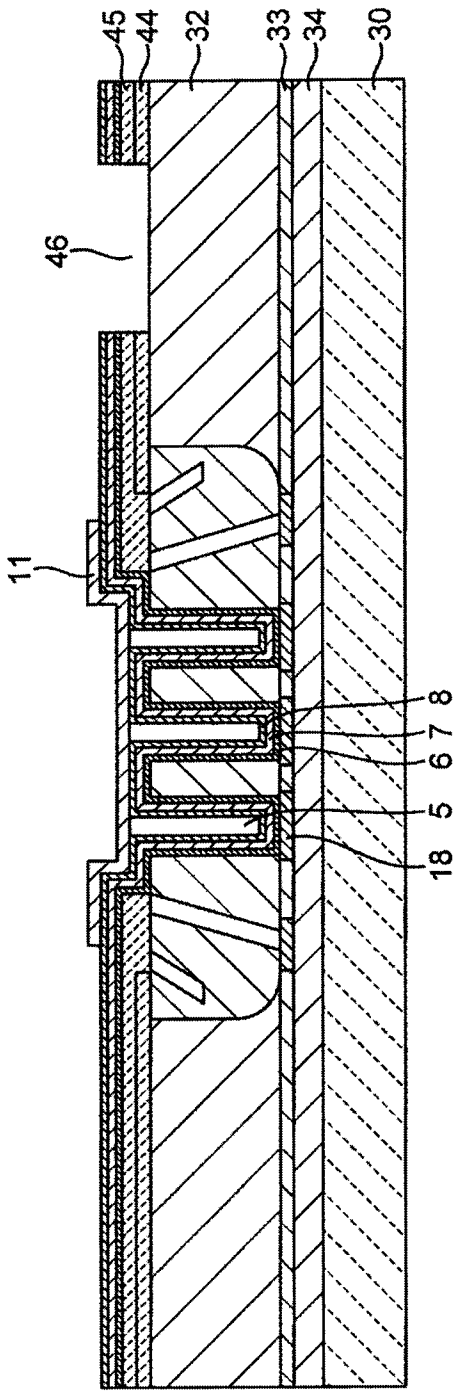

Fig. 8

[Fig. 9]

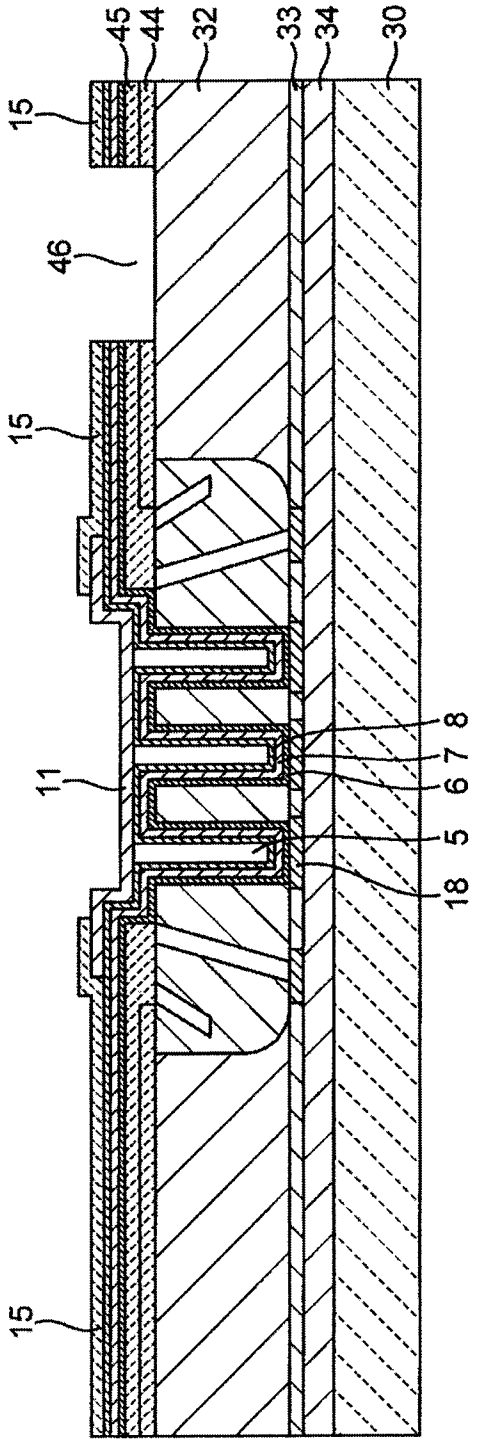

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2020/004147

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01G4/012 H01G11/26 H01G9/04 H01L49/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01G H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/268144 A1 (VOIRON FRÉDÉRIC [FR] ET AL) 15 September 2016 (2016-09-15) paragraphs [0057] - [0060]; figure 1	1-4
A	HOURDAKIS E ET AL: "High-Density MIM Capacitors With Porous Anodic Alumina Dielectric", IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 30, no. 10, 1 October 2010 (2010-10-01), pages 2679-2683, XP011316023, ISSN: 0018-9383 II. Sample Fabrication; figure 1	1

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 April 2020	07/05/2020

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CHI-TSUNG HONG ET AL: "Nanotexture Electrode on Nanoporous AAO Dielectric for Micro Tactile Sensing Devices", MICRO ELECTRO MECHANICAL SYSTEMS, 2009. MEMS 2009. IEEE 22ND INTERNATIONAL CONFERENCE ON, IEEE, PISCATAWAY, NJ, USA, 25 January 2009 (2009-01-25), pages 100-103, XP031444240, ISBN: 978-1-4244-2977-6 2. DESIGN CONCEPT 3. FABRICATION PROCESS AND RESULTS; figure 2	1
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1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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