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(54) METHODS FOR PREPARING A BONDING SURFACE OF A SEMICONDUCTOR WAFER

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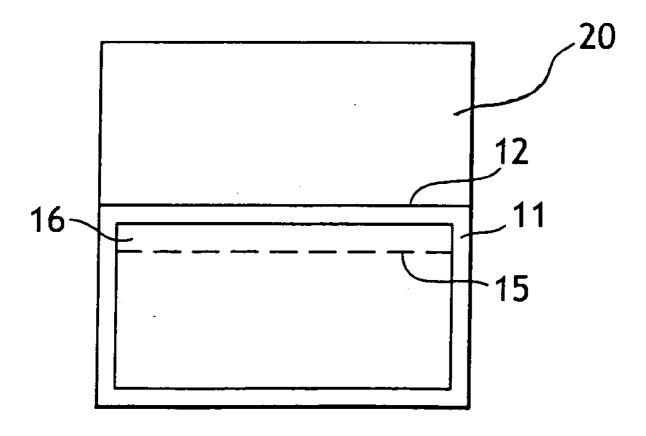
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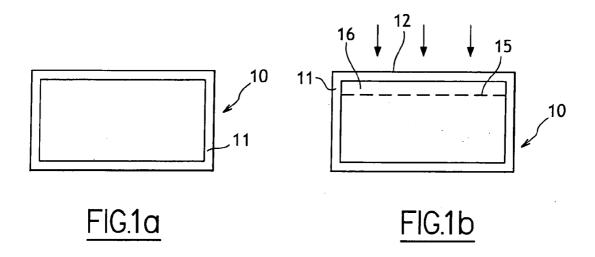
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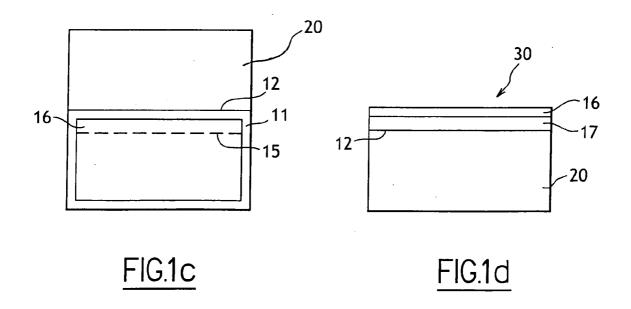
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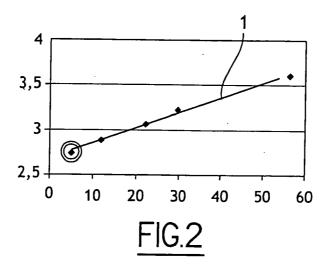
(57)**ABSTRACT**

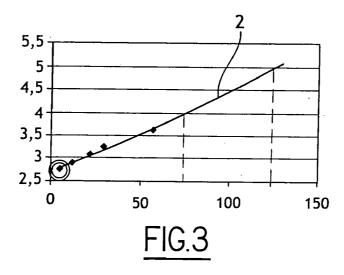
A method for preparing an oxidized surface of a first wafer for bonding with a second wafer. The method includes treating the oxidized surface using a mix of NH₄OH/H₂O₂ to increase the bonding energy between the first and second wafers. The treatment parameters are chosen such that etching occurs that is sufficient to remove isolated particles from the oxidized surface, but that is sufficiently weak to smooth the surface without creating rough patches thereon. Also described is a thin layer removal process, which may advantageously be used to fabricate a semiconductor on insulator structure.

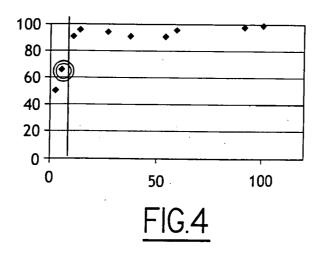












METHODS FOR PREPARING A BONDING SURFACE OF A SEMICONDUCTOR WAFER

BACKGROUND ART

[0001] The present invention generally relates to the bonding of two semiconductor wafers suitable for us in microelectronics, optics, or optronics applications. In particular, the invention relates to preparing an oxidized bonding surface of at least one of the wafers, wherein treatment parameters are chosen to provide etching that is sufficient to remove isolated particles from the oxidized surface but that is sufficiently weak to smooth the surface without creating rough patches thereon.

[0002] Atomic species may be implanted through an oxidized surface of a wafer to form a weakened area therein at a pre-set depth beneath the oxidized surface (thus creating a film on the wafer surface). It is then possible to detach the surface film from the implanted wafer after it has been bonded to another substrate. An example of such a detachment process is the SMART-CUT® process, which is known to skilled person in the art (see "Silicon-on-Insulator Technology, Materials to VLSI", 2nd edition, by Jean-Pierre Colinge, published by Kluwer Academic Publishers, pages 50 and 51), and which allows a film to be removed from a wafer for transfer to another wafer. A semiconductor-on-insulator structure such as an SOI (Silicon On insulator) structure can be made in this manner by transferring a thin silicon film from a donor wafer to a receiver wafer.

[0003] With the increase of miniaturization of electronic components formed in semiconductor layers, manufacturers of semiconductor-on-insulator substrates are increasingly asked to make semiconductor-on-insulator structures that include thinner and thinner semiconductor films. Thus,, it is vitally important to improve the quality of a transferred layer and therefore to improve removal techniques.

[0004] Consequently, the quality of the bond between the layer to be transferred and the receiver substrate is essential in order to ensure good removal, wherein the quality of the bond is mainly measured by the bonding energy between the two wafers. To ensure that the contact area of the two wafers to be joined is of good quality, it is necessary to implement a cleaning operation to clean at least one of the two bonding surfaces.

[0005] A trend in the prior art is to chemically treat the wafers in stages prior to bonding. To clean the surface of a wafer of oxidized or non-oxidized semi-conductor material, the known technique is to use a treatment called RCA. The RCA treatment includes a first bath of SC1(Standard Clean 1) solution that includes ammonium hydroxide (NH₄OH), hydrogen peroxide (H₂O₂) and deionised water, and then a second bath of SC2(Standard Clean 2)solution, which contains hydrochloric acid (HCl), and hydrogen peroxide (H₂O₂), and deionised water. The first bath is intended mainly for removing isolated particles on the wafer surface and for removing particles buried in the vicinity of the surface and to prevent them from resettling. The SC2 solution mainly removes any metallic contamination that has settled on the wafer surface that may, in particular, form chlorides. However, after implementing such chemical treatments the resulting surfaces have rough patches, which can, in some cases, be more significant than that existing prior to treatment. Such rough patches on the surface of the wafers alter the bonding energy of the wafers all the more because they have a high RMS (Root Mean Square) value in angstroms. The presence of isolated particles or contaminants on the surface of the wafers can also be detrimental to good bonding of the wafers when they are found at its interface. After bonding, these particles which are enclosed at the bonding interface, may cause surface blisters to form in the structure obtained after using a SMART-CUT® detachment technique, and/or cause surface blisters in areas not transferred between the area at the level of which the species were implanted and the surface of the structure. These blisters increase in size and/or grow during any subsequent heat treatment, for example, a heat treatment used after bonding to strengthen the bond.

[0006] A known solution for increasing separation of the isolated particles is to conduct the chemical treatment while applying megasonic waves. The megasonic waves cause the isolated particles to vibrate and therefore to separate off. It is preferable, however, to avoid implementing an additional process when cleaning the wafers to avoid complicating the cleaning stage. Furthermore, additional equipment would be required in order to generate the megasounds.

SUMMARY OF THE INVENTION

[0007] Presented is a method for preparing an oxidized surface of a first wafer for bonding with a second wafer. The method includes treating the oxidized surface using a solution of NH₄OH/H₂O₂ to increase the bonding energy between the subsequently bonded first and second wafers. The treatment parameters are advantageously chosen to provide etching that is sufficient to remove isolated particles from the oxidized surface but that is sufficiently weak to smooth the surface without creating rough patches thereon to enable an increased bonding energy between the first and second wafers when those surfaces are bonded together compared to bonding without treating the oxidized surface of the first wafer.

[0008] Advantageously, the treating is conducted after atomic species are implanted through the oxidized surface.

[0009] In an embodiment, the treatment parameters of the method include at least one of a predetermined dose of chemical elements, a predetermined temperature, or a predetermined duration for applying the treatment. These treatment parameters are advantageously chosen such that treating removes isolated surface particles having an average diameter of more than about 0.1 micrometers. In a beneficial implementation, the treatment parameters are chosen such that after treatment any rough patches that appear are less than about 5 ÅRMS. In a variation, the treatment parameters are chosen such that after treatment any rough patches that appear are less than about 4 ÅRMS.

[0010] Advantageously, the method limits the etching that occurs to a depth of about 10 angstroms to about 120 angstroms, or to a depth of about 10 angstroms to about 60 angstroms. The dose per unit mass of NH_4OH/H_2O_2 may beneficially be in the range from about 1/2 to about 1/1, and treating may occur at a temperature in a range of between about 30° C. and about 90° C. and for a cleaning duration of between 1 and 6 minutes. In an implementation, the treatment parameters comprise a dose per unit mass of NH_4OH/H_2O_2 of about 1/2, a temperature of about 50° C., and a cleaning duration of about 3 minutes. In a variation, the

treatment parameters comprise a dose per unit mass of NH₄OH/H₂O₂ of about 1/2, a temperature of about 70° C., and a cleaning duration of about 3 minutes. In yet another beneficial implementation, the treatment parameters comprise a dose per unit mass of NH₄OH/H₂O₂ of about 3/4, a temperature of about 80° C., and a cleaning duration of about 3 minutes.

[0011] In another aspect of the invention, the first wafer is a donor wafer and the second wafer is a receiving wafer. The method includes the step of removing a thin layer from the donor wafer and transferring it to the receiving wafer. The atomic species are implanted through the oxidized surface of the donor wafer to form a weakened zone at a predetermined depth to define the thin layer, and then the donor wafer surface is treated with the NH₄OH/H₂O₂ solution. The method also includes bonding the donor wafer to the receiver wafer, and supplying energy to detach the thin layer from the donor wafer at the level of the weakened zone to transfer it to the receiving wafer.

[0012] In an advantageous embodiment, the implanted atomic species comprise at least one of hydrogen and helium ions. The process also beneficially includes conducting a thermal oxidation step prior to treating the donor wafer. The structure that includes the thin layer and donor wafer resulting from use of the process according to the invention is advantageously a semiconductor-on-insulator structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Other aspects, purposes and advantages of the invention will become clear after reading the following detailed description with reference to the attached drawings, in which:

[0014] FIGS. 1a to 1d show the different stages in a SMART-CUT® removal process.

[0015] FIG. 2 is a graph showing a plot of measurements of the depths of etch in angstroms to the values of rough patches in RMS angstroms on wafers after different cleaning operations.

[0016] FIG. 3 is a graph showing a plot of the same measurements as those shown in FIG. 2, but used here to predict the resultant rough patches due to more substantial cleaning operations.

[0017] FIG. 4 is a graph showing a plot of measurements of the effectiveness of surface particle removal from a wafer as a function of the depths of etch caused by the cleaning.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] The wafer cleaning process according to the invention may be used with the thin layer removal method according to the SMART-CUT® process. Referring to FIG. 1a, a first stage includes oxidizing a semi-conductor wafer to create a donor wafer 10 having an oxide layer 11 on its surface. This oxidation process may be native, or may be conducted under a heat treatment (i.e. thermal oxidation), or by deposit of aggregates of SiO₂.

[0019] With reference to FIG. 1b, the oxidized donor wafer 10 is subjected to an implantation of atomic species through one of the oxidized surfaces. The atomic species may be hydrogen and/or helium ions. The atomic species

used during implantation are dosed and are implanted with a predetermined energy to form a weakened zone 15 at a pre-set depth under the surface of the donor wafer 10. The weakened zone 15 has a particular weakness relative to the rest of the donor wafer 10. A film 16 is thus formed that is delimited by the weakened zone 15 and the oxidized surface 12.

[0020] Referring to FIG. 1c, a receiver wafer 20 is brought into contact with the oxidized surface 12 through which implantation has taken place. Bonding by molecular adhesion takes place between the surfaces that are brought into contact. An annealing stage may be applied to reinforce the bonding interface. Next, sufficient energy, such as heat and/or mechanical energy, is supplied to break the weak bonds of the weakened zone 15. This causes detachment of the thin film 16 from the donor wafer 10, thus forming the semiconductor-on-insulator structure 30 shown in FIG. 1d. The thin film 16 removed from the donor wafer 10 forms the semiconductor part, and the subjacent oxide layer 17 forms the electrically insulating part of the structure 30.

[0021] A finishing stage, using for example mechanical chemical polishing, may then be implemented to minimize any defects and rough patches that appeared when detaching the thin film. The final structure may then be used in applications for micro-electronics, optics or optronics. For example, it would be possible to form components in the detached layer.

[0022] It is thus possible to make semiconductor-on-insulator structures such as SOI, SGOI (Silicon Germanium on Insulator), SOQ (Silicon on Quartz), GeOI (Germanium On Insulator) structures, an alloy made of components belonging to the Group Ill-V on insulator family; each having an insulating layer including the cleaned oxide layer according to the invention introduced between the detached layer and another wafer.

[0023] As shown above, the SMART-CUT® process may be used to bond the donor wafer 10 to the receiver wafer 20, and the present invention improves upon the overall process. One goal is to improve the bonding between the two wafers 10 and 20, which can be achieved by satisfying the following three objectives. First, remove isolated particles from the bonding surface of at least one of the wafers to reduce the appearance of post-bonding defects. Second; reduce the size and the number of the rough patches on the wafer surface to increase the contact areas of the bonding surfaces which results in improving the bonding energy. Third, make the surfaces hydrophilic. The three objectives can be achieved by utilizing a simple, fast and cost-effective technique according to the invention. Another goal is to create a semiconductor-on-insulator structure 30 by using the SMART-CUT® process and incorporating a stage according to the invention.

[0024] Another purpose is to control the preparation of an oxidized surface 12 that has been subject to implantation for subsequent bonding. It has been observed that such a surface is about 5 times more sensitive to such preparation than if it had not been subject to implantation. Consequently, it is important to accurately calibrate and to correctly set preparation parameters.

[0025] The wafer to be cleaned may be made of any type of semiconductor material. However, with regard to the

following discussions, the wafer material is silicon, which material has been studied as described below. In an implementation, a wafer was oxidized naturally (or has a native oxide) or artificially (for example, the case of a thermally formed oxide). The invention proposes a process for preparing a surface of the wafer for bonding with another wafer, implementing at least one chemical treatment stage that employs ammoniated chemical species mixed with molecules of H_2O_2 . In a preferred embodiment, such chemical species are supplied in a moist medium. The chemical species are, for example, diluted in de-ionized water. An ammoniated solution of this kind is also called an SC1 solution.

[0026] Cleaning by means of an SC1 solution results in the following effects (obtained by the chemical action of this solution). The surface is etched, making it possible to dig under the particles and thus to "strip" them (otherwise known as a "lift-off" effect). An opposite electric potential between the surface and the particles is created, linked directly to the high pH of the solution which causes detachment of isolated particles. The opposite electrical potential prevents migration of particles from the bath to the plate. This cleaning is therefore linked particularly to the high pH of the ammoniated solution, including as a result a significant concentration of OH- ions in solution. During the etching of the oxide by the ammonia, these ions react with the pendant bonds generated on the surface and saturate them in SiOH termination. This layer of SiOH formed on the surface then creates the repelling opposite potential, which detaches particles bonded to the surface (in other words the isolated particles) and prevents them from resettling. These surface SiOH bonds will also be the point of insertion of water molecules on the surface of the wafer, thus causing a hydrophilic condition. This hydrophilic condition improves the bonding with another wafer.

[0027] With reference to FIG. 2, the results are shown of a study conducted to find the relationship between the thickness of etched materials (etch depth) by different SC1 solutions, to the rough patches that are present and measured on the wafer surface. The etch depths were measured by reflectometry, and the rough patches were measured using an AFM (Atomic Force Microscope), on oxidized silicon wafers that are and have been subject to ion implantation.

[0028] The level of particle removal is determined by measurements taken prior to and following each SC1 treatment. Measurements were taken by reflectometry, typically by using a laser adjusted to a pre-set light spectrum, to about 0.13 microns. This value is constitutes the average diameter of the smallest particles detectable by reflectometry. The x-coordinate of the graph in FIG. 2 shows the etch depths obtained with different SC1 solutions, expressed in angstroms. The y-coordinates of the graph in FIG. 2 show the values of rough patches measured on the wafer for the different etches carried out on the wafers, and these rough patches are expressed in RMS angstroms. The rough patches are presented as a function of the etches implemented on the wafer surface, and are shown on the graph by black dots.

[0029] A first result of the measurement is that the average roughness increases with the etch depth. A second result is that a roughly linear relationship was obtained between the etch depth and the roughness values.

[0030] Referring to FIG. 3, a linear extension of the curve 1 of FIG. 2 is shown that takes the substantially linear relationship between the etch depth and the roughness values noted above into account. The result is the curve 2 shown in FIG. 3. Using this linear extension of the curve 1, and knowing that a maximum pre-set roughness value beyond which the bonding energy becomes insufficient exists, it is then possible to deduce and predict the maximum depth of etch that is associated with it, beyond which the bonding energy becomes insufficient. In an implementation, the maximum roughness value was set at about 5 RMS angstroms, in compliance, for example, with the results of measurements disclosed in "Detailed characterization of wafer bonding mechanisms", C. Malleville et al., published by Electromechanical Society Proceedings, volume 97-36, page 50, section 3. It has been shown that for a roughness value above about 5 RMS angstroms the bonding energy may be drastically reduced. Consequently, with reference to FIG. 3, it may be deduced that the maximum etch depth is around 120 angstroms.

[0031] Wafer bonding, when applied to making an SOI structure by using the SMART-CUT® technique, requires a bond strength that is sufficient, and in particular much greater, than the implantation force of the buried (having been implanted) atomic species. This is achieved experimentally with regard to rough patches of less than about 4 RMS angstroms, thus reducing (again with reference to FIG. 3) the maximum depth etch to around 60 to 70 angstroms. These measurements underscore the need to restrict as far as possible the etching action on the wafer surface, with a maximum limit on the etch depth that must not be exceeded.

[0032] FIG. 4 depicts another study undertaken to find relationships between the efficiency of surface particle removal from the wafer, and the etch depth of the wafer when using different SC1 solutions. When these measurements were taken, the wafers were deliberately contaminated by depositing a pre-set number of isolated particles, which represented the particles to be removed. The efficiency of removal of these particles was measured by taking LPD (Light Point Defect) measurements on the surfaces of different wafers that had been deliberately contaminated in a similar manner. An LPD is a defect that is detectable by laser light scattering optical measurements. An LPD defect is also known as a "highlight".

[0033] An LPD measurement is made by illuminating the wafer surface using an incident optical wave emitted by the laser source. The light scattered by the LPD defects present on the surface is detected by means of an optical detector. The light scattering on the wafer surface can be correlated with the number of residual particles on the wafer surface, and thus light scattering measurements provide information on the number of residual particles. Other residual particle measurement techniques may be implemented, alone or in combination with the LPD measurements.

[0034] Etch depth is typically measured by using reflectometry, in substantially the same way as that used to measure the rough patches as explained above with reference to FIG. 2. The x-coordinate of FIG. 4, in the same way as that for FIGS. 2 and 3, shows the different etch depths effected by means of different SC1 solutions, expressed in angstroms. The y-coordinate shows isolated particle

removal efficiencies, expressed as a percentage relative to the estimated total number of present isolated particles on the wafer surface. Particle removal efficiency measurements as a function of the etch depths are shown on the graph as black dots.

[0035] FIG. 4 illustrates that beyond an etch depth of about 10 angstroms, particle removal efficiency is close to 100%. In contrast, below the value of about 10 angstroms, particle removal is much less impressive, having an efficiency of around 50% to 60%. Thus, for etches of less than about 10 angstroms, particle removal is insufficient for allowing good bonding conditions. This means that if the etched thickness is too small, the particles are no longer separated from the surface and their removal efficiency falls very quickly.

[0036] Optionally, it is possible to simultaneous use an SC1 bath and to apply megasounds to help separate the particles from the surface.

[0037] It is noted again, that an oxidized surface that has been subject to implantation is particularly sensitive to chemical treatments. This sensitivity is about 5 times greater than that of the same type of surface that has not been subject to implantation. Thus, the implementation and the calibration of the chemical treatment must be carefully conducted.

[0038] The measurements discussed above with reference to FIGS. 2 and 4 make it possible to evaluate the desired etch depth when the wafer to be cleaned will be brought into the presence of an SC1 solution. The etch depth is bound to be located in the range between about 10 angstroms and about 120 angstroms, or between about 10 angstroms and about 60 angstroms in an embodiment using an SOI structure formed by using the SMART-CUT® technique. Within this authorized range of etch depths, a considerable number of experiments were conducted to attempt to optimize etch conditions using SC1 solutions, with a view to further increasing the post-cleaning bonding energy. These etch results typically employed a dosing per unit mass of NH₄OH/H₂O₂ in the range from about 1/2 to about 4/4 or 1/1, temperatures in a range of from about 30° C. to about 80° C., and etch durations of from about a few seconds to several hours. Generally, the parameters are chosen so that the cleaning duration is relatively short, on the order of between about 1 and 6 minutes.

[0039] The following Table 1 lists some conditions wherein cleaning by using SC1 proved to be particularly impressive:

TABLE 1

SC1	% per unit mass NH ₄ OH/H ₂ O ₂	T(C)	Cleaning time	
	1/2 2/4 (or 1/2) 3/4	50 70 80	3 min 3 min 3 min	

[0040] In particular, if a % per unit mass NH_4OH/H_2O_2 equal to approximately ½ is used at a temperature of about 70° C., and with a cleaning time of about 3 minutes, then an etch of about 20 angstroms was obtained. This resulted in a roughness value of about 3 RMS angstroms, and a level of particle removal of more than about 90%, thus attaining an optimum bonding energy.

[0041] Optionally, one or more cleaning stages may precede or follow the previous cleaning stage. In this manner, an SC2 treatment is advantageously implemented subsequent to the SC1 treatment. The SC2 treatment may be conducted with a solution comprising a mix of HCl and of H₂O₂. This treatment is typically applied at temperatures of between about 70° C. and about 80° C. The action of the SC2 solution makes it possible to remove mainly metal contaminants from the wafer surface.

[0042] After cleaning at least one of the two oxidized bonding surfaces of the two wafers that are to be bonded, the wafers are brought into close contact with each other. Oxidized wafer cleaning thus makes it possible to restrict a sizeable number of large-size particles and to avoid defects that would result in a downgrade of the wafers. Wafers are downgraded when the bonding energy is not sufficient to obtain non-defective final structures. The two wafers 10 and 20 (see FIG. 1c) are advantageously brought into contact just after cleaning, without any intermediate treatment stage. The two wafers can be bonded by adhesion of the molecules present on their bonding surfaces. This adhesive property is explained mainly by the hydrophilic properties present on the wafer surface. In particular, water molecules are present on the wafer surface which give rise to Si-OH bonds and to water diffusion in the vicinity of the wafer surfaces. The Si-OH bonds of a wafer bonding surface are linked via hydrogen bonds to the surface of the other wafer, thus forming a bond strength between the two wafers 10 and 20 that is sufficiently significant to create a sufficient binding adhesion. It is then advantageous to apply a heat treatment to increase the bonds between the two wafers 10 and 20. This heat treatment may be applied at one or more pre-set temperatures and for a pre-set period of time to optimize the bonding efficiency and to avoid creating structural defects on the wafer surface. The heat treatment causes the disappearance of a large part of the Si-OH bonds to the benefit of the covalent Si-O-Si (stronger) bonds.

[0043] With reference to the FIGS. 1c and 1d, after bonding of two wafers, a thin film 16 is detached at the level of a weakened zone 15 to form the structure 30. The detachment step may be imperfect if, for example, nontransferred areas appear that result from the presence of intervening particles at the bonding interface that were imprisoned during bonding. These apparent defects may be accentuated or created during a subsequent heat treatment such as a heat treatment to solidify the bonding interface. Such defects are reduced as much as possible by the cleaning stage according to the invention, which is implemented prior to the bonding step. The SC1 chemical treatment is carried out under conditions and in accordance with treatment parameters chosen to maximally reduce the number of isolated particles at the bonding interface, while reducing interfacial rough patches as much as possible. The SC1 treatment also takes into account the particular etching sensitivity of an oxidized surface that has been subject to implantation.

[0044] The present invention relates to preparing the surface of oxidized wafers of any kind of material relating to the field of semi-conductors. Thus, any material belonging to atomic Group IV family such as silicon or a Silicon-Germanium alloy, and extending also to other types of alloys of the Group IV-IV, Group III-V or Group II-VI family. It

should also be understood that these alloys may be binary, ternary, quaternary or of higher degree.

What is claimed is:

- 1. A method for preparing an oxidized surface of a first wafer for bonding with a second wafer, which comprises treating the oxidized surface of the surface with a solution of NH₄OH/H₂O₂, wherein treatment parameters are chosen to provide etching that is sufficient to remove isolated particles from the oxidized surface but that is sufficiently weak to smooth the surface without creating rough patches thereon to enable an increased bonding energy between the first and second wafers when those surfaces are bonded together compared to bonding without treating the oxidized surface of the first wafer.
- 2. The method of claim 1, which further comprises implanting atomic species through the oxidized surface of the first wafer prior to the treating.
- 3. The method of claim 1, wherein the treatment parameters include at least one of a predetermined dose of chemical elements, a predetermined temperature, or a predetermined duration for applying the treatment.
- 4. The method of claim 1, wherein the treatment parameters are chosen such that treating removes isolated surface particles having an average diameter of more than about 0.1 micrometers
- 5. The method of claim 1, wherein the treatment parameters are chosen such that after treatment any rough patches that appear are less than about 5 ÅRMS.
- 6. The method of claim 1, wherein the treatment parameters are chosen such that after treatment any rough patches that appear are less than about 4 ÅRMS.
- 7. The method of claim 1, wherein the etching occurs to a depth of about 10 angstroms to about 120 angstroms.
- **8**. The method of claim 1, wherein the etching occurs to a depth of about 10 angstroms to about 60 angstroms.
- 9. The method of claim 1, wherein the solution provides a dose per unit mass of NH_4OH/H_2O_2 in the range from about 1/2 to about 1/1.

- 10. The method of claim 1, wherein the treating occurs at a temperature in a range of between about 30° C. and about 90° C. and a cleaning duration of between about 1 and 6 minutes.
- 11. The method of claim 1, wherein the treatment parameters comprise a dose per unit mass of NH₄OH/H₂O₂ of about 1/2, a temperature of about 50° C., and a cleaning duration of about 3 minutes.
- 12. The method of claim 1, wherein the treatment parameters comprise a dose per unit mass of NH₄OH/H₂O₂ of about 1/2, a temperature of about 70° C., and a cleaning duration of about 3 minutes.
- 13. The method of claim 1, wherein the treatment parameters comprise a dose per unit mass of NH_4OH/H_2O_2 of about 3/4, a temperature of about 80° C., and a cleaning duration of about 3 minutes.
- 14. The method of claim 2, wherein the first wafer is a donor wafer, the second wafer is a receiving wafer, and the atomic species are implanted through the oxidized surface of the first wafer to form a weakened zone at a predetermined depth to define a thin layer for subsequent transfer; and the method further comprises bonding the donor wafer to the receiver wafer; and supplying energy to detach the thin layer from the donor wafer at the weakened zone.
- 15. The method of claim 14, wherein the implanted atomic species comprise at least one of hydrogen and helium ions.
- **16**. The method of claim 14, further comprising conducting a thermal oxidation step prior to treating the donor wafer.
- 17. The method of claim 14, wherein the thin layer and donor wafer comprise a semiconductor-on-insulator structure.

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