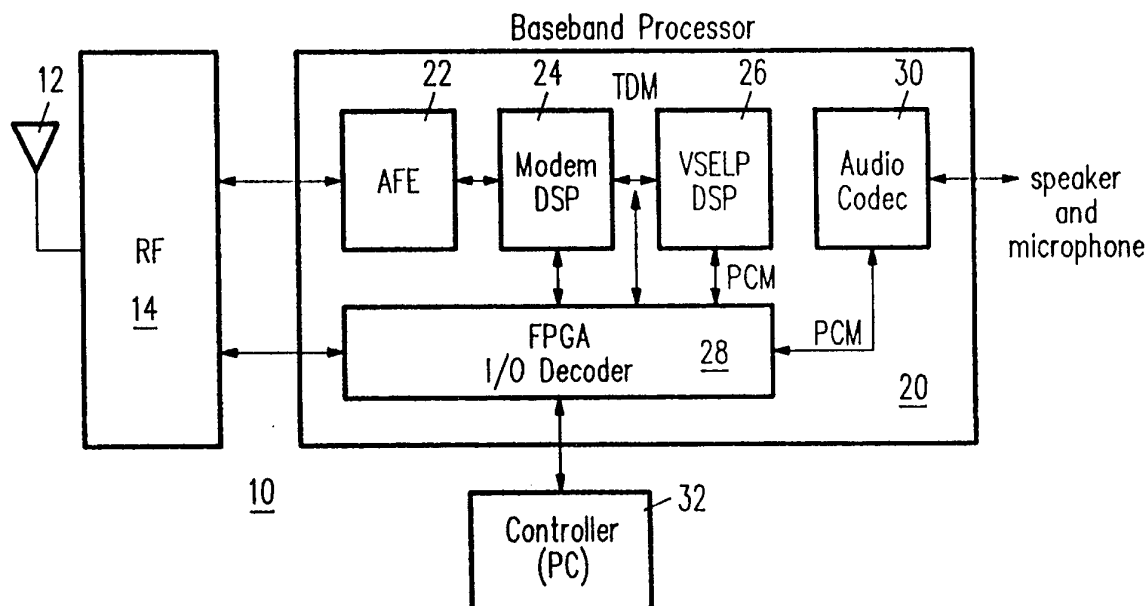




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁵ : H03D 1/00, H04L 7/00, 27/06	A1	(11) International Publication Number: WO 95/05705 (43) International Publication Date: 23 February 1995 (23.02.95)
(21) International Application Number: PCT/US94/09175 (22) International Filing Date: 12 August 1994 (12.08.94) (30) Priority Data: 08/108,061 17 August 1993 (17.08.93) US 08/107,451 17 August 1993 (17.08.93) US 08/108,113 17 August 1993 (17.08.93) US 08/107,938 17 August 1993 (17.08.93) US 08/108,084 17 August 1993 (17.08.93) US (71) Applicant: TEKNEKRON COMMUNICATIONS SYSTEMS, INC. [US/US]; 2121 Allston Way, Berkeley, CA 94704-1301 (US). (72) Inventors: CHENG, Jong-Keung; 4055 Westminster Place, Danville, CA 94506 (US). SUBRAMANIAN, Ravi; 218 Cranbury Circle, East Brunswick, NJ 08816 (US). TOURIGUIAN, Mihran, H.; 2 Moonstone Court, Hercules, CA 94547 (US). LIN, Nan-Sheng; 4611 Kelso Street, Union City, CA 94587 (US). GHOSH, Biswa; Apartment 416, 880 E. Fremont Avenue, Sunnyvale, CA 94087 (US). KAVALER, Robert; 1305 Walnut Street, Berkeley, CA 94709 (US). HAOUL, Amine; 98 Northhampton, Berkeley, CA 94707 (US). SUZUKI, Kenkichi; Fuji Heights #203, 2-3-17, Onigoe, Ichikawa-city, Chiba 272 (JP).		(74) Agents: YIN, Ronald, L. et al.; Limbach & Limbach, 2001 Ferry Building, San Francisco, CA 94111 (US). (81) Designated States: CA, JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: DIGITAL WIRELESS COMMUNICATION SYSTEM AND METHOD OF OPERATION THEREFOR



(57) Abstract

In a digital wireless communication system (fig. 1), the apparatuses can estimate the speed of the mobile unit in relationship to the stationary unit (fig. 12). In addition, the apparatus can adjust the sampling phase of a digitally encoded signal in such a system (figs. 6 and 9). In addition, the apparatus can adaptably control the frequency of reception and to determine the frequency and time slot position in a digital wireless communication session (fig. 4 and 6). Finally, the system can operate to equalize (fig. 6) digitally encoded signals transmitted in a plurality of non-contiguous time slots (fig. 11).

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DIGITAL WIRELESS COMMUNICATION SYSTEM AND
METHOD OF OPERATION THEREFOR

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Technical Field

The present invention is a digital wireless communication system and a method of operation therefor.

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Background of the Invention

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Wireless communication is well known in the art. Heretofore, one type of wireless communication is known as a "cellular" communication wherein each stationary unit receives and transmits signals to mobile units within its allocated geographical region, called a cell. As mobile units move from one cell to another, communication is transferred from one stationary unit in one cell to another stationary unit in another cell.

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Heretofore, cellular communication is analog based and has risen in popularity. However, as a result, the airways have become increasingly crowded and the capacity of the communication system to take on new subscribers is becoming increasingly of a problem. Digital cellular communication offers an opportunity to increase the number of subscribers to operate within the cellular system. However, to bridge the gap between the current analog cellular system and the digital cellular system, a standard has been proposed. The standard proposed by EIA/TIA

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(Electronic Industry Association/Telecommunications Industry Association), known as the IS-54 standard, specifies that communication between a mobile unit and a base unit should be capable of operating in both the analog and the digital mode. More particularly, when operating in the digital wireless communication mode, the IS-54 standard specifies that communication between a base unit and a mobile unit occur in a Time Division Multiplex Access (TDMA) mode. In a TDMA mode, the digitally encoded signal is transmitted in a plurality of non-contiguous time slots. Communication between a base unit and a mobile unit occurs in an assigned time slot, within each frame. In each time slot, digitally encoded synchronization signal must first be transmitted followed by the digitally encoded data signal. Furthermore, within the digitally encoded data signal, at a predetermined time period, a digitally encoded marker signal is transmitted. These are all well known standards in the IS-54 specification.

One of the problems of a digital wireless communication system is the problem of equalizing the digitally encoded signals. As the digitally encoded signal is transmitted from one unit to another, through a multiplicity of data paths, the various signals arriving at the other unit can cause delay spread between the digitally encoded signals. This is known as inter-symbol interference. An equalizer is a digital hardware/software apparatus which corrects inter-symbol interference between the digitally encoded signals arriving from a plurality of signal paths.

In the prior art, a number of equalization strategies is disclosed. See, for example, "BER Performances Of Mobile Radio Equalizer Using RLS

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Algorithm In Selective Fading Environment" by Akihiro Higashi, Hiroshi Suzuki; "Bi-Directional Equalization Technique For TDMA Communication Systems Over Land Mobile Radio Channels" by Yow-Jong, Liu, page 1458-1462, Globecom '91; and "Development Of Japanese Adaptive Equalization Technology Toward High Bit Rate Data Transmission In Land Mobile Communications" by Seiichi Sampei, page 1512-1521 IEICE Transactions, Volume E, 74, No. 6, June, 1991.

Although the present invention, in the preferred embodiment, discloses a wireless communication systems using the IS-54 standard capable of operating in both analog and digital mode, it should be apparent that the invention, as set forth herein, can be used in any digital, wireless, communication system.

Summary of the Invention

The present invention is a digital wireless communication system and a method of operation therefor. More particularly, the present invention relates to a method of estimating the speed of a mobile unit moving relative to a stationary unit in the digital wireless communication system. In addition, the digital wireless communication system can adjust the sampling phase of the digitally encoded signal transmitted between the mobile unit and the stationary unit. The invention also relates to an apparatus to control the frequency of reception in the digital wireless communication system, and a method for adjusting the carrier frequency of reception in such a system. Further, the invention relates to a technique to correct deviation in the frequency in the transmission from one unit to another in the digital wireless communication system.

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Finally, the invention relates to a method and apparatus for equalizing the signals transmitted in such a digital wireless communication system.

Brief Description of the Drawings

5 Figure 1 is a block level diagram of a wireless communication unit which is a remote unit or is a portion of a stationary unit of a digital wireless communication system.

10 Figure 2 is a block level diagram of the signal flow path when the wireless communication unit shown in Figure 1 is operating in the analog mode.

 Figure 3 is a block level diagram of the signal flow path when the wireless communication unit shown in Figure 1 is operating in a digital mode.

15 Figure 4 is a detailed block level diagram of the RF unit portion of the communication unit shown in Figure 1.

20 Figure 5 is a detailed block level diagram of the AFE portion of the communication unit shown in Figure 1.

25 Figure 6 is a flow chart showing the operation of the software used in the Modem DSP of the communication unit shown in Figure 1, when the Modem DSP is operating in the receive mode and having two modes of operation : sync acquisition mode and steady state mode.

 Figure 7 is a functional block diagram of the Modem DSP with its software, operating in the sync acquisition mode.

30 Figure 8 is a functional block diagram of the Modem DSP with its software, operating in the steady state mode

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Figure 9 is a detailed functional block diagram of the timing recovery function during the steady state mode shown in Figure 8.

5 Figure 10 is a detailed functional block diagram of the DQPSK receiver function during the steady state mode shown in Figure 8.

Figure 11 is a timing diagram of the protocol of communication between like units of Figure 1, when operating in a digital mode.

10 Figure 12 is a diagram showing the difference in energy of a signal received by a mobile unit when moving.

Figure 13 is a block level diagram showing the measurement of energy in a time slot to estimate the speed of a mobile unit.

Figure 14(a-c) are diagrams showing the methods of training an equalizer.

Detailed Description of Drawings

Referring to Figure 1 there is shown a schematic
20 block level diagram of a communication unit 10. In a wireless communication system between a mobile unit and a stationary unit, the communication unit 10 is that of the mobile unit. In addition, the schematic block level diagram shown in Figure 1 represents a
25 portion of the stationary unit. More particularly, as will be appreciated by those having ordinary skilled in the art, the stationary unit would comprise additional units to accomplish function such as hand off and the ability to process many remote
30 units at the same time.

The communication unit 10 comprises an antenna 12 which receives the RF (radio frequency) wireless signal. The RF signal is then processed by an RF processing unit 14. From the RF processing unit 14,

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the signal is then passed to a base band processor 20. The base band processor 20 comprises in AFE (analog front end) 22, which receives the RF signal from the RF processing unit 14. The signal from the AFE unit 22 is then received by a Modem DSP 24. The signal from the Modem DSP 24 is received by a VSELP DSP 26. A FPGA (Field Programmable Gate Array) 28 communicates with the Modem DSP 24 and the VSELP DSP 26. The FPGA 28 also communicates with an audio codec 30. In addition, the FPGA 28 is connected to a controller 32. Finally, the audio codec 30 is connected to a conventional speaker and microphone.

As previously discussed, the communication unit 10 in the preferred embodiment implements the IS-54 standard. Thus, the communication unit 10 can process both analog wireless signals as well as digital by encoded wireless signals. In general, the above-identified components operate in the following manner:

RF processing unit 14 receives the analog or the digitally encoded RF signal and converts them into an baseband signal for further processing by the based band processor 20. When operating in the digital mode, the RF processing unit 14 also demodulates the received IF signal to produce the analog I,Q signals.

The AFE unit 22 implements analog to digital and digital to analog conversions with associated filtering functions for the I/Q signals. In addition, it provides for four (one not used) channel D/A for RF control. It also has one A/D for RSSI (Receive Signal Strength Indicator) measurement.

The Modem DSP 24 in the preferred embodiment is a digital signal processor which is ROM coded (TMS 320c51) which implements analog mode processing, modem functions in the digital mode, as well as FACCH

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(Fast Access Control Channel)/SACCH (Slow Access Control Channel) error control functions.

FACCH/SACCH are defined by the IS-54 standard and is well known in the art. The modem processor 24
5 interfaces with the FPGA I/O decoder 28 through its serial port. Through the FPGA 28, the FPGA 28 then communicates with the controller 32. The Modem DSP 24 also maintains the time division multiplex (TDM) bus for communication with the VSELP DSP processor 26
10 and the audio codec 30 when operating in the analog mode. The Modem DSP 24 communicates with the RF processor 14 through the AFE 22.

The VSELP DSP 26 is also a ROM coded DSP (TMS 320c51) which implements the VSELP codec functions,
15 which is a speech compression algorithm. In addition, it performs error control functions associated with the speech frame and echo cancellation. Finally, it communicates with the Modem DSP 24 via the TDM port and is powered down
20 during the analog mode operation.

The audio codec 30 implements the speech A to D and D to A conversion and associated filtering. It interfaces directly to the speaker and to the microphone (not shown). The speech samples are
25 exchanged with the Modem DSP 24 through the TDM port and TDM to pulse code modulation (PCM) conversion circuit in the FPGA I/O decoder 28 during the analog mode operation. In addition, during the digital mode operation, the audio codec 30 interfaces with the
30 VSELP DSP 26 through the PCM bus.

The FPGA I/O decoder 28 consist of a first FPGA1 28a, a second FPGA2 28d, and a PAL (Programmable Array Logic - not shown), for I/O address decoding. The first FPGA1 28a includes timing generation
35 circuitry, wideband data demodulator, sync control

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interface, and baseband test interface. The second
FPGA2 28b includes an interface (UPIF) to interface
with the controller 32. In addition, it communicates
with the audio codec 30 and the VSELP DSP 26 through
the PCM port and has TDM/PCM conversion circuitry.
Finally, the second FPGA2 28b has a sampling clock
(interrupt control).

Referring to Figure 2, there is shown the signal
flow for the communication unit 10 when operating in
the analog mode. As can be seen, when operating in
the analog mode, the VSELP DSP 26 is completely
"turned off". The analog wireless signal is received
by the RF unit 14 and is supplied to the AFE unit 22.
From the AFE unit 22, the signal is supplied to the
Modem DSP 24. The Modem DSP 24 through its TDM port
communicates with the second FPGA2 28b. From the PCM
port of the second FPGA2 28b, the second FPGA2 28b
communicates with the codec 30.

Referring to Figure 3, there is shown a block
level diagram of the signal flow when the
communication unit 10 operates in the digital mode.
In this mode, the VSELP DSP 26 is actively involved
in the processing of the received digitally encoded
signal.

Referring to Figure 11, there is shown a timing
diagram of a digitally encoded signal when the
communication unit 10 operates in the digital mode,
implementing in particular, the IS-54 standard. The
communication between a base unit and a mobile unit
is divided into a plurality of frames, designated as
F1, F2, etc., with each frame lasting 20 msec. In
the digital mode of operation, each 20 msec. frame is
further divided into a plurality of time slots, shown
as T1, T2 and T3. Using the capability of voice
compression as performed by VSELP processor 26, at

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full rate, 8 kbits/sec., for the same frame at the same frequency, in the digital mode, the base unit can serve to communicate with three different mobile units. Further, when the VSELP DSP 26 is operating at half rate compression i.e., 4 kbits per second, communication between the base unit and a plurality of mobile units can occur using a 40 msec. frame with each frame divided into six different time slots or serving six users.

Each time slot T_n can accommodate the transmission of 162 symbols or 324 bits. The base unit and the mobile unit communicate over separate frequency channels thereby accomplishing full duplex transmission. The protocol of transmission from the base unit to the mobile unit is shown and designated as f (for forward). The protocol of transmission from the mobile unit to the base unit is shown and is designated as r (for reverse). In the forward protocol, the IS-54 standard dictates that the digitally encoded signal begins with 14 symbols of synchronization signal followed by 148 symbols of data signal, with 6 symbols of DVCC (a marker signal) located in the middle of the data field between symbols 85-91. Thus, within each forward time slot, transmission of 162 symbols include sync and data.

Referring to Figure 4, there is shown a detailed block level diagram of the RF processing unit 14. The RF processing unit 14 receives the signal from the antenna 12 through a duplexer. The received signal is supplied to an RF + IF stage 72. The RF + IF stage 72, as is well known in the art, has an RF filter, low noise amplifier which serves to filter and amplify the received signal, and an RF to IF converter to convert the received RF signal into an intermediate frequency signal. The conversion is

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based upon a difference frequency signal generated by an RX frequency synthesizer 74. The frequency selected by the RX frequency synthesizer 74 is based upon a signal supplied from a temperature compensated crystal oscillator 70, passing through an appropriate multiplier 78.

The output of the RF + IF stage 72 is then supplied to an amp and I/Q demodulator 76 whose gain is selected by an automatic gain control signal AGC. The outputs of the amp + I/Q demodulator 76 are the analog I and analog Q signals.

In the transmit mode, the RF processing unit 14 comprises similar components as the above. The analog I and analog Q signals are supplied to an I/Q modulator 86, which modulates the analog I,Q signals on an IF carrier signal. The output of the I/Q modulator 86 is then supplied to an RF + IF stage 82. The RF + IF stage 82 converts up the output of the I/Q modulator 86 into an RF signal for transmission by the antenna 12. The frequency to convert from the intermediate frequency to the RF frequency is controlled by the TX frequency synthesizer 84. The TX frequency synthesizer 84 also receives the output of the temperature compensated crystal oscillator 70 multiplied by an appropriate multiplier 88.

Referring to Figure 5, there is shown a detailed block level diagram of the AFE unit 22. The AFE unit 22 comprises a first LPF (low pass filter) 91. The first LPF 91 receives the received analog I/Q signals from the RF unit 14. The output of the LPF 91 is then supplied to an A-to-D converter 90 from which the digital RxI and the digital RxQ signals are produced. The A-to-D converter 90 also receives a clock signal from a clock 92. The clock 92 is adjusted by a sampling phase adjustment signal (which

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will be described hereinafter). The AFE unit 22 also comprises a D-to-A converter 118. The D-to-A converter 118 receives the transmit digital I and Q (Tx I/Q) signals and converts them into analog Tx I/Q signals. The D-to-A converter 118 also receives the clock signal from the clock 92. The analog Tx I/Q signals are then supplied to a second LPF 117. The output of the second LPF 117 is then supplied as the Tx analog I/Q signals and are provided to the RF unit 14.

The AFE unit 22 also comprises a WBDD (wide band data demodulator) 119. From the WBDD 119, the signal wide band data is produced. The wide band data demodulator signal is an analog control channel. It is disclosed herein only because the IS-54 standard requires that the communication unit 10 can handle both analog and digital communication. It is not used during digital communication. The AFE unit 22 also comprises a D-to-A converter 93 which receives the control signals of Tx_Power, AFC, and AGC. These digital signals are converted into an analog signal and are supplied to the RF unit 14 to control the RF unit 14. Finally, the AFE unit 22 receives the RSSI (receive signal strength indicator) signal and digitizes it by the A-to-D converter 95.

Referring to Figure 6, there is shown a flowchart of the operation of the software used in the Modem DSP 24 when the Modem DSP 24 is operating in the received mode. When operating in the received mode, the Modem DSP 24 has two modes of operation: a sync acquisition mode, and a steady state mode. In the sync acquisition mode, the operation occurs at the start of each communication session. Once communication has been established, the software proceeds into the steady state mode. There, the

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operation occurs once every frame or once every 20
millisec. Further, during the steady state, the
Modem DSP 24 initially performs a timing recovery
operation 42 which is shown in Figure 9 and which
5 will be explained in greater detail. After the
timing recovery operation 42, the Modem DSP 24
operates on the signal shown in block level diagram
form in Figure 10 and will be discussed in greater
detail hereinafter.

10 Referring to Figure 7, there is shown a detailed
functional block diagram of the sync acquisition mode
of operation for the Modem DSP 24. The digital I/Q
received signals from the AFE unit 22 are supplied to
a normalizing circuit 96. The normalizing circuit 96
15 serves to normalize the magnitude or the amplitude of
the digitized I,Q signals from the A to D converter
90.

From the normalizing circuit 96, the digitally
encoded signal is then stored in a storage unit 98,
20 which is just a buffer. As will be explained
hereinafter, the storage 98 stores at least 15
symbols (or 30 samples) which is the length of the
synchronization signal portion of the digitized
signal. The stored signals are then supplied to a
25 first bank of match filters 100. Each of the filters
in the first bank 100 is adapted to receive the
digital signal from the storage 98 and to filter this
digital signal through a frequency range different
from one another. Thus, the output of the first bank
30 of match filters 100 is a plurality of filtered
digital signals. The plurality of filtered digital
signals are supplied to a plurality of first
magnitude circuits 102. Each of the plurality of
first magnitude circuits 102 determines the magnitude
35 of the filtered digital signal from the first bank of

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match filters 100. The output of the first magnitude circuits 102 is yet another plurality of digital signals which are supplied to a first maximum and threshold circuit detector 106.

5 The output of the first maximum and threshold circuit detector 106 serves to detect the filtered digital signal having the maximum magnitude. In addition, the first maximum and threshold circuit 106 selects the match filter from the first bank of
10 matched filters 100 that generated the signal having the maximum output.

 The output of the first maximum and threshold circuit 106 is supplied to a second bank of match filters 108. Each of the filters in the second bank
15 of match filters 108 has a fine frequency offset from one another and having a different filter coefficients from one another. The output of the second bank of match filters 108 is a plurality of fine filtered digital signals which are supplied to a
20 second magnitude circuit 110.

 The second magnitude circuit 110, similar to the first magnitude circuit 102, comprises a plurality of circuits each of which receives a fine filtered digital signal and determines the amplitude or the
25 magnitude thereof. The output of the second magnitude circuit 110 is a plurality of signals which are supplied to a second maximum and threshold circuit detector 112. The second maximum and threshold detector 112 selects the digital signal
30 having the maximum amplitude as the output thereof. In addition, the second maximum and threshold circuit 112 selects the filter from the second bank of match filters 102, producing that output. Finally, the output of the second maximum and threshold circuit
35 112 is an initial carrier frequency offset signal to

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correct the carrier frequency to the AFC (automatic frequency control), and a time slot position signal. The time slot position signal is used internally to control the start and stop of each subsequent frame.

5 Referring to Figure 8, there is shown a block level functional diagram of the operation of the Modem DSP 24 with the software therein when operating in the steady state mode. In the steady state mode, the Modem DSP 24 performs SQRC filtering function 42 and 50 (for receive and transmit) and timing recovery 10 42 (for receive), DQPSK modulation 44 and 52 (again receive and transmit respectively) and frame interleaving/De-interleaving 46 and 54 (receive and transmit respectfully), and FACCH decode and encode 15 48 and 56 (receive and transmit respective). In addition, the VSELP DSP 26 performs channel decode and encoding 62 and 66 (receive and transmit, respectively) and speech decode and encode 64 and 68 (receive and transmit respectively).

20 Referring to Figure 9, there is shown a detailed block level functional diagram of the timing recovery function 42 performed by the Modem DSP 24 when operating in the steady state mode.

The Rx I/Q signals from the second maximum and 25 threshold circuit detector 112 are supplied to a 1:4 interpolator 114. The output of the interpolator 114 is then supplied to a third match filter 116. The match filter 116 also receives the stored sync signal from a storage location 104. The match filter 116 is 30 a single filter and it matches each input sample symbol with the stored sync signal from the storage location 104. After each match, the input signal is shifted by $T/8$, or by one input sample and then is matched again with the sync signal from the storage 35 location 104. Thus, the output of the match filter

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116 is a signal operating at the $T/8$ rate. The outputs of the match filter 116 are then supplied to a peak detector 118. The peak detector 118 receives the plurality of outputs from the match filter 116, being supplied thereto at the $T/8$ rate, and determines the output having the highest peak value. The output of the peak detector 118 is the value $imax$, the use of which will be discussed hereinafter. The output from the peak detector 118 is then supplied to a second order phase lock loop 119. The second order phase lock loop 119 has an internal variable AVG-POS, the use of which will be described hereinafter in greater detail. The output of the second order phase lock loop 119 is the sampling phase adjustment signal which is supplied to the clock 92 of the AFE 22 shown in Figure 5. The received digital Rx I/Q signals at the $T/2$ rate are also supplied to a bank of SQRC filters 117. The output of the second order PLL 119 is used to select the appropriate SQRC filter from the bank of SQRC filters 117. The output of the bank of SQRC filters 117 is then supplied to the DQPSK receiver 44.

The output of the second order PLL 119 is the signal $Avg-pos(n+1)$. It is supplied to the AFE unit 22 and is adjusted once every frame during the idle period. the coefficient filter of each of the bank of SQRC filters 117 is tuned to a different sampling phase adjustment. Thus, the output of the second order PLL 117 selects one of the coefficient filters from the bank of SQRC filters 117.

Referring to Figure 10 there is shown a detailed block level diagram of a portion of the DQPSK receiver 44. The DQPSK receiver 44 receives each symbol as the output of the timing recovery function 42. The digital Rx I/Q symbols are supplied to a

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pre-processing unit 121 which generates the control signals: speed estimation, energy calculation, and CTRL. The CTRL signal controls the DQPSK receiver 44 in its two modes of operation. In one mode, each
5 symbol from the output of the timing recovery 42 is supplied to a fine all pass filter 120. From the fine all pass filter 120, each symbol signal is supplied to a differential detector 122. From the differential detector 122, the symbol signal is then
10 supplied to a phase slicer 126 and an arc tangent processor 128.

In another mode of operation, each symbol from the timing recovery function 42 is supplied to an equalizer 124. The equalizer 124 operates on all the
15 symbols received during the assigned time slot. After the equalizer 124 has performed its operation (to be discussed hereinafter), each symbol is outputted from the equalizer 124, one at a time. Each symbol signal from the equalizer 124 is also
20 supplied to the phase slicer 126 and at the same time to the arc tangent processor 128.

Each of the symbol signal from the equalizer 124 or the differential detector 122 is received simultaneously by the phase slicer 126 and the arc
25 tangent processor 128. The phase slicer 126 operates upon the symbol signal by quantizing the input phase into one of a plurality of pre-determined constellation points (i.e. 45° , 135° , 225° , 315°) and generates the phase signal $\tilde{e}$. The arc tangent
30 processor 128 receives the same symbol signal and serves to operate on the symbol signal received to determine the arc tangent of its phase. The output of the arc tangent processor 128 is the phase signal e . The phase signal $\tilde{e}$ and the phase signal e are
35 supplied to a first subtractor (or adder with a

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negative input) 130 which generates the phase error signal $(e - \tilde{e})$. The phase error signal $(e - \tilde{e})$ is then supplied to a first multiplier 132 to which a constant g_1 is multiplied. Thereafter, the output of the first multiplier 132 is supplied to a second adder 134 to which the frequency signal output from a prior operation on a prior symbol was stored in the storage 136. From the second adder 134, the adjustment to the frequency to the next symbol or the frequency error signal, is then generated. Thus, the frequency error signal which is generated is in accordance with:

$$\Delta f(n+1) = \Delta f(n) + g_1 (e(n) - \tilde{e}(n));$$

The output of the first adder 130 is also supplied to a second multiplier 138 to which the constant g_2 is supplied. The output of the second multiplier 138 is then supplied to a third adder 140 to which the frequency error signal $\Delta f(n)$ from a prior symbol is also supplied. The output of the third adder 140 is supplied to a fourth adder 142 to which the carrier phase ϕ signal from a prior bit has been supplied and stored in storage 144. The output of the fourth adder 142 is a carrier phase error signal and is calculated in accordance with:

$$\phi(n+1) = \phi(n) + g_2 (e(n) - \tilde{e}(n)) + \Delta f(n)$$

Operation

I. Initial Determination of Frequency and Time Slot Position

As previously discussed, the digital wireless communication unit 10 is particularly adapted for digital cellular communication wherein errors such as rayleigh fading, intersymbol interference and carrier frequency offset present problems. At the commencement of each communication session, the

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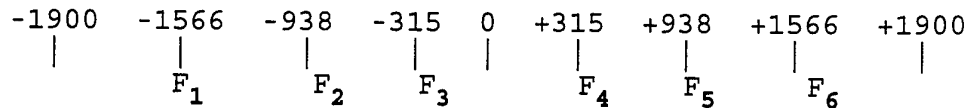
remote unit and the base unit must necessarily establish initial frequency and time slot position.

Referring to Figure 7, after the IQ signals are digitized by the analog to digital converter 90, they are normalized by the normalizing unit 96 to retain only the phase information. The digitized I,Q samples are then stored in a storage unit 98 or a delay line of size of 30 complex. The size is chosen because the storage unit 98 or the delay line must contain 14 phase changes for the sync word, which is 15 symbols or 30 samples at T/2 sampling rate.

The output of the storage unit 98 is supplied to a first bank 100 of 6 matched filters consisting of six 15-TAP FIR complex filters. Each one is matched to the same sync word but with a different carrier frequency offset. The range of offset is designed to cover the plus or minus 2.5 ppm offset of an 850 MHz carrier or an offset of about 1900 Hz. Even though each of the filters has 15 symbols spaced taps, odd and even samples from the delay line 98 are alternately entered into each of the match filters so that T/2 resolution is maintained. Thus, the output of each match filter is an output also at the T/2 rate.

Each of the match filters of the first bank 100 is matched to the carrier phase shifted versions of the sync word symbols-not the phase changes from symbol to symbol. By not using the phase changes from symbol to symbol, this would obviate the requirement that the delay line 98 or the storage 98 contain phase changes themselves. In the preferred embodiment, each of the match filters from the first bank 100 has a center of frequency offset covering the 2.5 ppm 1900 Hz range of possible frequency offsets as shown below.

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with F₁-F₆ being the center frequency of six 15-TAP
 5 FIR filters.

Each of the match filters from the first bank
 100 simultaneously provides frequency offset
 estimate, start of frame, and time slot and symbol
 timing to within T/2 accuracy. If a particular match
 10 filter of the first bank 100 matches a particular
 sync word, then there will be a high output when the
 contents of the storage 98 are exactly aligned with
 the sync word and low output for any other alignment.
 Thus, the match filters from the first bank 100
 15 provide a good indication of frame, slot and symbol
 timing to within one T/2 sample.

When there is some frequency offset, because
 there is a plurality or a bank 100 of match filters,
 the detection range of a particular offset can be
 20 found empirically to be about ± 11 degree, i.e., each
 match filter has high output only when the match
 filter's offset matches the signal's offset within
 this range. By using the first bank match filters
 100, both sync and frequency offset estimation can be
 25 performed simultaneously.

Once the match filter producing the largest
 amplitude is detected and is chosen, i.e., that match
 filter from the first bank 100 has the exact or the
 closest offset to the frequency, then it is supplied
 30 to a second bank 108 of match filters. The second
 bank 108 of match filters is a bank of 4 fine match
 filters each spaced 126 Hz apart. The output of the
 first maximum and threshold circuit detector 106 or
 the coarse frequency estimate is used to find the

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center frequency. The received sync word samples are then digitally rotated by this estimate to bring them down to near the baseband. The rotated sync samples are then run through the second bank 108 comprising
5 of 4 fine match filters. The filter with the highest output from the five filters (including the one which gave the coarse estimate) determines the final fine frequency offset estimate. The final frequency offset estimate should be accurate to within 0.9
10 degrees or 63 Hz.

In a preferred embodiment, the centers of the match filters for the second bank 108 are offset to the plus and minus of the center frequency from the coarse estimate. In addition, the time slot position
15 is precise up to $T/2$ because the filters from the first bank 100 are precise up to $T/2$.

The use of two banks 100 and 108 of match filters to initially set the coarse center frequency and then to adjust the fine frequency permits rapid
20 frequency acquisition without using expensive processing capability.

II. Adaptive Frequency Control

Once the initial frequency has been set, due to the mobility of the remote unit, frequency offset,
25 such as drift, can occur during the communication session. Thus, the communication unit 10 must adaptively control the frequency during the communication session.

Referring to Figure 10 there is shown a portion
30 of the DQPSK receiver 44. As previously discussed, the symbol signal from the output of the differential detector 122 or from the output of the equalizer 124 is supplied to both the phase slicer 126 and the arc tangent processor 128. The phase slicer 126

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generates the phase signal $\theta(n)$. The arc tangent processor 128 generates the phase signal $\theta(n)$. The output of the phase slicer processor 126 and the arc tangent processor 128 are supplied to a first adder 130 which computes the phase error signal as previously discussed.

The frequency error signal $\Delta f(n)$ is computed as previously discussed.

The constant g_1 is 2^{-11} during sync acquisition and is 2^{-13} in a steady state mode.

In addition, the carrier phase error signal $\phi(n+1)$ is calculated as follows:

$$\phi(n+1) = \phi(n) + g_2 (\theta(n) - \tilde{\theta}(n)) + \Delta f(n)$$

The constant g_2 is 2^{-7} during the sync acquisition and 2^{-8} in a steady state mode.

Both equations are updated every symbol. Thus, (n) is the symbol index. The frequency error signal $\Delta f(n)$ is supplied to the digital to analog converter 118 and is used to control the temperature compensator crystal oscillator 70. The adjustment based upon frequency error signal is performed once after the assigned time slot in question i.e., during the idle slot and does not affect the received sample until the beginning of the next frame. During the interrupt, the higher order 10 bits of Δf are used for AFE correction and this number is subtracted from Δf so that Δf keeps a running total of only the residual frequency offset.

The carrier phase error signal is also calculated as shown above. The carrier phase error signal (different from sampling phase error signal) is used to adjust the carrier phase of the frequency. It is corrected in the following manner:

$$e^{-j\phi}$$

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and is applied to the I/Q signals from the demodulator 76 shown in Figure 4. In the preferred embodiment, it is calculated only in the beginning of the communication session. However, as can be seen, this calculation, like the calculation for the frequency error signal Δf , can be adjusted every frame, or even every symbol.

III. Adaptive Sampling Phase Control

Similar to the adaptive frequency control, sampling phase during the operation of the communication session must also be adaptively controlled. Referring to Figure 9, the received I/Q samples around the sync word are passed to an interpolator 114. The interpolator 114 generates $8xT$ samples (the input to the interpolator 114 is already at $2T$ rate). The output of the interpolator 114 is match filtered by the filter 116 with an ideal sync word stored from the storage 104 at T sampling rate. Although the acquisition mode has already determined timing to within $T/2$ sampling phase, by interpolating at $4x$ the input rate, in theory, the match filter 116 must only determine within a plus or minus four sample range. Four samples at $8XT$ sampling rate means the search window is $T/2$. However, due to delay spread, the detected peak may belong to the delayed path, hence its timing may be the delayed version of ideal timing. In fact, it is possible that the main signal may not be the largest. Thus, in order to determine the largest, i.e., maximum amplitude peak, the search is extended over minus 1 and plus 2 symbols of the expected symbol or minus 8 to plus 16 sample range.

The sampling phase adjustment of the phase adjuster 94 is computed in a second order timing

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recovery loop. The sampling phase is adjusted after the completion of the assigned time slot and prior to the commencement of the next frame. Thus, the sampling phase adjustment occurs during the idle time slot. The purpose of using a second order rather than first is to minimize jitter of the correction. Instant sampling phase correction or first order timing correction can cause a jitter. In addition, the first order timing phase error is corrected by choosing the best matched filters from the bank of match filters 108 for each frame. The frequency offset from frame to frame is adjusted as previously discussed.

The timing recovery update equations are

$$\text{drift}(n+1) = \text{drift}(n) + \beta [\text{imax}(n) - \text{avg-pos}(n)]$$

$$\text{avg-pos}(n+1) = \text{avg-pos}(n) + [\text{imax}(n) - \text{avg-pos}(n)] + \text{drift}(n+1)$$

where n is the frame count, $\text{imax}(n)$ is the peak position of matched filter output for frame n , $\beta=2^{-6}$ for the first 100 frames, $\beta=2^{-7}$ for the next 100 frames, and $\beta=2^{-8}$ after 200 frames.

The adjustment to the sampling phase adjuster 94 depends upon whether the argument inside $[\cdot]$ is negative argument (in which case the unit 10 should advance timing, sample should be sooner) or is positive argument (in which case the unit 10 should retard timing, the samples being later). For negative argument, i.e. $\text{avg-pos}(n) > \text{imax}(n)$, the timing adjustment in the preferred embodiment should be limited by:

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$$a. \quad -3 \times \frac{T}{8} \text{ for } n < 100$$

$$5 \quad b. \quad -1.25 \times \frac{T}{8} \text{ for } 100 \leq n < 200$$

$$c. \quad -.5 \times \frac{T}{8} \text{ for } n \geq 200$$

10 For positive argument, i.e. $\text{avg-pos}(n) < \text{imax}(n)$, the timing adjustment in the preferred embodiment should be limited by

$$15 \quad a. \quad .5 \times \frac{T}{8} \text{ for } n < 100$$

$$b. \quad .15 \times \frac{T}{8} \text{ for } 100 \leq n < 200$$

$$20 \quad c. \quad .0667 \times \frac{T}{8} \text{ for } n \geq 200$$

As can be seen from the above, the advance magnitude is larger than the retard magnitude so that the equations are biased towards moving to the first ray, which implies earlier sampling. There is more bias in the advance magnitude because that is more likely the source of the no-delay signal path, whereas the retard direction is more likely the source of the delay path.

30 The sampling time for the current frame is determined by picking the SQRC filter closest to avg-pos . The sampling clock 92 is corrected by the amount $\text{avg-pos}(n+1)$ but is limited by $T/8$. In practice, because the base station's clock accuracy is 5 ppm and the remote unit is 100 ppm, the correction is never even as large as $T/8$.

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In the case where the signals are passed through another bank of fine pass filters 120 in Figure 10, where another digital fine timing correction is performed. Each of the fine all pass filters is a
5 complex $T/2$ spaced 4 tap FIR filter. The bank of the coarse filters from the maximum and threshold detector 112 along with the timing recovery equations determine timing for the current frame to an accuracy of $T/8$. Finer accuracy $T/32$ is obtained by using one
10 of five fine all pass filter 120 spaced 11.25 degrees apart. The correct filter is determined by the residual value of avg-pos after choosing the coarse all pass filter. The fine filter centers are:

-22.5 -11.25 0 +11.25 +22.5

15 IV. Estimation of Speed for Equalization

To determine the optimum parameter values for equalization using RLS adaptation techniques, vehicles speed estimation is necessary. Vehicle speed can be roughly estimated from the slope of the
20 received signal amplitude.

Referring to Figure 12 there is shown a graph of the amplitude of transmission by a moving vehicle (or reception by the moving vehicle) of a signal generated by the other. As can be seen, the slope of
25 the amplitude is indicative of the speed of the mobile unit. In general, the information required is very coarse, e.g., slow, medium or fast. Thus, accuracy is not critical. At higher speeds fades occur more rapidly so the slopes are greater.

30 The slope is estimated by measuring the difference between short term energies of a plurality of contiguous symbols. The short term energy $E(k)$ is averaged over 8 contiguous samples. Since there are 162 symbols in a time slot plus 14 symbols of the

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sync field of an adjacent time slot, there are a total of 176 symbols. The 176 symbols are processed at T/2 rate. Thus there are 352 (T/2) samples. With eight samples per short term average, there are 44 short term average samples. The slope estimation updated equation is

$$\text{diff} = \frac{1}{150} \sum_{k=0}^{29} \left| \sum_{n=0}^4 E(n+k) - \sum_{n=0}^4 E(n+k+10) \right|$$

$$\text{where } E(k) = \frac{1}{8} \sum_{n=0}^7 \text{Mag}(8K + n)$$

As can be seen in Figure 13, the average energy of groups of five contiguous short term energy E(k) is taken. A second group is separated from a first group by five short term energy points. The magnitude of the difference between the first group and the second group is computed. This process is repeated 30 times by shifting the groups by one short term energy point each time.

Further smoothing can be achieved by the equation

$$\text{Diff}_{\text{Ave}} = \alpha \times \text{Diff}_{\text{Ave}} + (1-\alpha) \times \text{Diff}$$

where α is a smoothing constant.

As a result of the calculation of Diff or slope, an estimation of the speed of the mobile unit can be made.

V. Equalization

As previously discussed, when inter symbol interference occurs, equalization must be performed. In this method, all of the digital signals from the assigned time slot, including the sync digital signals, the data signals, and the sync signals of an immediately succeeding time slot (not assigned to the

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communication unit 10) are stored (162 symbols of the assigned time slot + 14 symbols of sync of adjacent time slot). Thus, there are a total of 176 symbols stored. Further, as previously discussed, the sync symbols comprise the first 14 symbols of each time slot with the DVCC marker signal being 6 in number and being located at symbols 85-91.

The performance of equalization can be improved significantly by doing equalization bi-directionally. First, one minimum energy point is located in the assigned time slot (as shown in Figure 14(a)), then the RLS equalizer is trained by progressing forward from the commencement of the sync signal of the assigned time slot until the minimum energy point and progressing backward from the end of the sync signal of the succeeding, non-assigned time slot, until the minimum energy point is reached.

The performance of equalization can be further improved by making use of the DVCC signal as a training sequence. In so doing, two minimum energy points (one in data1 field and one in data2 field) are detected, as shown in Figure 14(b). Then the RLS equalizer is trained by progressing forward from the commencement of the sync signal of the assigned time slot until the first minimum energy point is reached. The RLS equalizer is trained by progressing backwards from the DVCC marker signal until the first minimum energy point is reached. The RLS equalizer is then trained by progressing forward from the DVCC marker into the data2 field, until the second minimum energy point is reached. Finally, the RLS equalizer is trained by progressing backward from the end of the sync signal of the succeeding, non-assigned time slot backward to the second minimum energy point.

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Finally, if it is desired to decode the DVCC marker signals, the RLS equalizer can be trained by first progressing forward from the sync signal until the DVCC marker is encountered. There, the DVCC marker signal is decoded and the RLS equalizer is trained by progressing backwards from the DVCC marker into the first data field, data1, until the first minimum energy point is reached. This is shown in Figure 14(c).

As a further refinement on the above method, the minimum energy point detected can be compared to a threshold level. If the minimum energy point is above the threshold level, then the RLS equalizer proceeds as if there is no minimum energy point. In that event, the RLS equalizer is trained starting with sync of the assigned time slot proceeding through the data1 field, through the DVCC marker signal, and through the data2 field.

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WHAT IS CLAIMED IS:

1. A method of estimating the speed of a second unit moving relative to a first unit, in a digital wireless communication system communicating between said first and second units, wherein said first unit transmits a digitally encoded signal, at a substantially constant power, said method comprising:
- receiving said digitally encoded signal by said second unit;
- sampling said digitally encoded signal to produce a first sampled digital signal having a plurality of symbols;
- measuring the short term energy over a plurality of contiguous symbols;
- measuring the average of short term energy (hereinafter: first short term energy average) over a first plurality of contiguous short term energy points;
- measuring the average of short term energy (hereinafter: second short term energy average) over a second plurality of contiguous short term energy points, said second plurality of contiguous short term energy points spaced apart from said first plurality of contiguous short term energy points; and
- determining the difference between said first short term energy average and said second short term energy average to derive an estimate of the speed of said first unit moving relative to said second unit.
2. The method of Claim 1 wherein said number of said plurality of contiguous symbol is 8 and said measuring step is calculating

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$$E(k) = \frac{1}{8} \sum_{n=0}^7 \text{Mag } (8K + n)$$

K is an index, i.e. first plurality or second plurality;

Mag (8K + n) is the magnitude of the energy of the (8K + n)th symbol.

3. The method of Claim 1 wherein said first and second plurality of contiguous short term energy points are separated by about 5 short term energy points.

4. The method of Claim 1 wherein said determining step is calculated in accordance with:

$$\text{Diff} = \frac{1}{150} \sum_{k=0}^{29} \left| \sum_{n=0}^4 E(n+k) - \sum_{n=0}^4 E(n+k+10) \right|$$

5. The method of Claim 4 wherein said determining step further comprises:

$$\text{Diff}_{\text{Ave}} = \alpha \times \text{Diff}_{\text{Ave}} + (1-\alpha) \times \text{Diff}$$

where α is a smoothing constant.

6. The method of Claim 1 wherein said digitally encoded signal is transmitted in a plurality of non-contiguous time slots.

7. The method of Claim 1 wherein said steps of measuring the energy averaged over a plurality of contiguous symbols and the determining step are performed during each time slot.

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8. An apparatus for adjusting the sampling phase of a digitally encoded signal transmitted between a first unit and a second unit in a digital wireless communication system, wherein said digitally encoded signal is transmitted in a plurality of non-contiguous time slots and within each time slot said digitally encoded signal has a synchronization signal portion followed by a data signal portion, said second unit comprising:

antenna means for receiving said synchronization signal portion of said digitally encoded signal;

clocking means for generating a clock signal at a first rate having a sampling phase;

analog to digital converting means for receiving said clock signal and said synchronization signal and for sampling said synchronization signal at said first rate, to generate a first plurality of symbols;

interpolating means for receiving said first plurality of symbols and for interpolating said first plurality of symbols to generate a second plurality of symbols at a second rate, wherein said second rate is a multiple of said first rate;

match filter means for receiving said second plurality of symbols and for comparing said second plurality of symbols to a stored plurality of symbols to generate an error signal; and

means for altering the sampling phase of said clock signal in response to said error signal.

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9. The apparatus of Claim 8 wherein said sampling phase of said clock signal is altered prior to the receipt of said synchronization signal from a subsequent time slot.

5 10. The apparatus of Claim 9 wherein said error signal can be positive or negative.

11. The apparatus of Claim 10 wherein said error signal is weighted to the positive.

10 12. A method of adjusting the sampling phase of a digitally encoded signal transmitted between a first unit and a second unit in a digital wireless communication system wherein said digitally encoded signal is transmitted in a plurality of non-contiguous time slots and within each time slot said
15 digitally encoded signal has a synchronization signal portion followed by a data signal portion, said method comprising;

 receiving said synchronization signal portion of said digitally encoded signal;

20 generating a clock signal having a sampling phase, operating at a first rate;

 sampling said synchronization signal by said clock signal to generate a first plurality of symbols;

25 interpolating said first plurality of symbols to generate a second plurality of symbols at a second rate wherein said second rate is a multiple of said first rate;

30 filtering said second plurality of symbols and comparing said second plurality of symbols to a stored plurality of symbols to generate an error signal; and

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altering the sampling phase of the clock signal in response to said error signal.

13. The method of Claim 12 wherein said sampling phase is altered prior to receiving the synchronization signal from a subsequent time slot.

14. The method of Claim 13 wherein said error signal can be positive or negative.

15. The method of Claim 14 wherein said error signal is weighted to the positive.

16. An apparatus to control the frequency of reception in a digital wireless communication system between a first unit and a second unit, wherein said first unit transmits a digitally encoded signal at a first frequency in a plurality of non-contiguous time slots to said second unit, said second unit comprising:

antenna means for receiving said digitally encoded signal;

converting means, coupled to said antenna means, for converting said received digitally encoded signal, to a lower frequency;

sampling means for receiving said filtered received digitally encoded signal at said lower frequency and for generating a plurality of discrete binary symbols during one of said plurality of non-contiguous time slots;

determining means for receiving each one of said plurality of discrete binary symbols (n) and for determining the phase error signal thereof ($e - \tilde{e}$);

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means for generating a frequency error signal for the subsequent symbol (n+1) in accordance with

$$\Delta f(n+1) = \Delta f(n) + g_1 (e(n) - \tilde{e}(n))$$

5 where g_1 is a constant; and

means for controlling said converting means in response to said frequency error signal after said one time slot but prior to the commencement of a subsequent one of said plurality of non-contiguous time slots.

10

17. The apparatus of Claim 16 wherein said digitally encoded signal in each of said time slot comprises synchronization signal followed by data signal.

15 18. The apparatus of Claim 16 wherein said $g_1 = 2^{-11}$ during the receipt of said synchronization signal, and $g_1 = 2^{-13}$ during the receipt of said data signal.

19. The apparatus of Claim 16 further comprising digital to analog converting means for receiving said frequency error signal and for converting it into an analog signal, supplied to said controlling means.

20

20. The apparatus of Claim 16 wherein said determining means further comprises:

25

first means for processing said plurality of discrete binary symbols;

second means for processing said plurality of discrete binary symbols by equalization; and

30 means for activating either said first or said second processing means.

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21. The apparatus of Claim 20 wherein said first processing means further comprises:

fine pass filter means for receiving said plurality of symbols and for filtering each symbol; and

differential detector means for receiving each filtered symbol and for generating an output symbol.

22. The apparatus of Claim 21 wherein said second processing means further comprises:

equalizer means for correcting inter-symbol interference, and for generating an output symbol one at a time.

23. The apparatus of Claim 22 wherein said determining means further comprises:

phase slicer means for receiving the output symbol and for generating a first phase signal $\tilde{e}$;

arc tangent means for receiving the output symbol and for generating a second phase signal e ; and

means for receiving the first phase signal $\tilde{e}$ and the second phase signal e and for generating the phase error signal $(e - \tilde{e})$.

24. A method of adjusting the carrier frequency of reception in a wireless digital communication system operating between a first unit and a second unit wherein said first unit transmits a digitally encoded signal at a first frequency in a plurality of non-contiguous time slots to said second unit said method comprising:

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receiving said digitally encoded signal by
said second unit;

converting said received digitally encoded
signal to a lower frequency;

5 sampling said lower frequency received
digitally encoded signal, during one of said
plurality of non-contiguous time slots, to
produce a plurality of discrete binary symbols;

10 determining the phase error signal
($e(n) - \tilde{e}(n)$) associated with each symbol (n);

generating a frequency error signal for the
subsequent symbol (n+1) in accordance with

$$\Delta f(n+1) = \Delta f(n) + g_1 (e(n) - \tilde{e}(n))$$

where g_1 is a constant; and

15 adjusting said lower frequency in response
to said frequency error signal after said one
time slot but prior to a succeeding time slot.

25. The method of Claim 24 wherein said
digitally encoded signal in each of said time slot
20 comprises synchronization signal followed by data
signal.

26. The method of Claim 25 wherein said
 $g_1 = 2^{-11}$ during the receipt of said synchronization
signal, and $g_1 = 2^{-13}$ during the receipt of said data
25 signal.

27. The method of Claim 24 further comprising:
converting the frequency error signal into
an analog frequency error signal; and
30 adjusting said filter frequency in response
to said analog frequency error signal.

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28. The method of Claim 24 wherein determining step further comprises:

processing said binary symbols in accordance with either of the following processes:

- I. filtering each symbol;
differentially detecting each filtered symbol;
determining a first phase e of a symbol (n) by a phase slicer means;
determining a second phase $\tilde{e}$ of a symbol (n) by an arc tangent processor means; and
determining the phase error signal $e(n) - \tilde{e}(n)$ by summing $e(n)$ and $-\tilde{e}(n)$; or
- II. correcting the inter-symbol interference for all symbols stored;
outputting each corrected symbol, one at a time;
determining a first phase e of a symbol (n) by a phase slicer means;
determining a second phase $\tilde{e}$ of a symbol (n) by an arc tangent processor means; and
determining the phase error signal $e(n) - \tilde{e}(n)$ by summing $e(n)$ and $-\tilde{e}(n)$.

29. A digital wireless communication system for communicating between a first unit and a second unit, wherein said first unit transmits a digitally encoded signal at a first frequency, and wherein said transmission is subject to deviation in said first frequency upon arrival at said second unit, said second unit comprising:

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antenna means for receiving said digitally encoded signal;

means for sampling said digitally encoded signal to produce a first sampled digital signal;

5

a plurality of first digital filter means for receiving said first sampled digital signal simultaneously, each of said first digital filter means for passing said first sampled digital signal therethrough in a frequency range different from one another to produce a plurality of second sampled digital signals with each having an amplitude;

10

means for receiving said plurality of second sampled digital signals and for selecting the second sampled digital signal with the largest amplitude, and for selecting the first digital filter means producing said selected second sampled digital signal;

15

a plurality of second digital filter means for receiving said selected second sampled digital signal, each of said second digital filter means for passing said selected second sampled digital signal therethrough in a frequency different from one another to produce a plurality of third sampled digital signals with each having an amplitude; and

20

means for receiving said plurality of third sampled digital signals and for selecting the third sampled digital signal with the largest amplitude and for selecting the second digital filter means producing said selected third sampled digital signal.

25

30

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30. The system of Claim 29 wherein said first unit is a stationary base station.

31. The system of Claim 30 wherein said second unit is a mobile unit.

5 32. The system of Claim 29 wherein said first unit transmits said digitally encoded signal in a TDMA mode.

10 33. The system of Claim 29 wherein said digitally encoded signal is subject to sampling phase error upon arrival at said second unit.

34. The system of Claim 33 wherein said digitally encoded signal encodes digital signals at a first rate.

15 35. The system of Claim 34 wherein said sampling means samples said digitally encoded signal at a rate faster than said first rate.

20 36. A digital wireless communication method between a first unit and a second unit, wherein said first unit transmits a digitally encoded signal at a first frequency, and wherein said transmission is subject to deviation in said first frequency upon arrival at said second unit, said method comprising:

 receiving said digitally encoded signal by said second unit;

25 sampling said digitally encoded signal by said second unit to produce a first sampled digital signal;

 passing said first sampled digital signal through a plurality of first digital filter

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means simultaneously, with each of said first digital filter means having a digital filter frequency range different from one another, to produce a plurality of second sampled digital signals with each having an amplitude;

5 selecting the second sampled digital signal having the largest amplitude and selecting the first digital filter means producing the selected second sampled digital signal;

10 passing said selected second sampled digital signal through a plurality of second digital filter means simultaneously, with each of said second digital filter means having a digital filter frequency different from one another, to produce a plurality of third sampled digital signals with each having an amplitude; and

15 selecting the third sampled digital signal having the largest amplitude and selecting the second digital filter means producing the selected third sampled digital signal.

37. The method of Claim 36 further comprising transmitting said digitally encoded signal in a TDMA mode.

25 38. The method of Claim 37 further comprising transmitting said digitally encoded signal in a TDMA mode.

30 39. A digital cellular communication system for communicating between a mobile unit and a first base station unit with each transmitting a digitally encoded signal at a frequency to the other, each of said units comprising:

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antenna means for receiving the digitally encoded signal transmitted by the other unit;

means for sampling said digitally encoded signal to produce a first sampled digital signal;

a plurality of first digital filter means for receiving said first sampled digital signal simultaneously, each of said first digital filter means for passing said first sampled digital signal therethrough in a frequency range different from one another to produce a plurality of second sampled digital signals with each having an amplitude;

means for receiving said plurality of second sampled digital signals and for selecting the second sampled digital signal with the largest amplitude, and for selecting the first digital filter means producing said selected second sampled digital signal;

a plurality of second digital filter means for receiving said selected second sampled digital signal, each of said second digital filter means for passing said selected second sampled digital signal therethrough in a frequency different from one another to produce a plurality of third sampled digital signals with each having an amplitude; and

means for receiving said plurality of third sampled digital signals and for selecting the third sampled digital signal with the largest amplitude and for selecting the second digital filter means producing said selected third sampled digital signal.

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40. The system of Claim 39 wherein each unit transmits digitally encoded signal to the other in non-contiguous slots of time.

5 41. The system of Claim 39 wherein each unit initially transmits synchronization data signal followed by data signal.

10 42. The system of Claim 41 wherein said first and second digital filter means are selected during the receipt of the synchronization data signal and are maintained for the data signal following said synchronization data signal.

43. The system of Claim 41 wherein said digitally encoded signal is subject to sampling phase error upon arrival at said second unit.

15 44. The system of Claim 43 wherein said digitally encoded signal encodes digital signals at a first rate.

20 45. The system of Claim 44 wherein said sampling means samples said digitally encoded signal at a rate faster than said first rate.

25 46. A method of equalizing a digitally encoded signal transmitted in a plurality of non-contiguous time slots with a digitally encoded synchronization signal commencing during each time slot followed by a digitally encoded data signal, having a digitally encoded marker signal at a predetermined time period in each slot, said method comprising:

storing the digitally encoded
synchronization signal (hereinafter: "first

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synchronization signal") and the digitally encoded data signal of a time slot, and the digitally encoded synchronization signal of the immediately succeeding time slot (hereinafter:
5 "second synchronization signal");

determining the location of the minimum energy point of the stored digitally encoded signals;

10 performing an equalization of said stored digitally encoded signals starting from said first synchronization signal to said minimum energy point; and

15 performing an equalization of said stored digitally encoded signals starting from said second synchronization signal to said minimum energy point.

47. The method of Claim 46 further comprising the steps of:

20 comparing the energy level of the minimum energy point detected to a threshold level; and

performing an equalization of said stored digitally encoded signals starting from said first synchronization signal to said second synchronization signal, in the event said energy
25 level of the minimum energy point is below said threshold level.

48. A method of equalizing a digitally encoded signal transmitted in a plurality of non-contiguous time slots with a digitally encoded synchronization
30 signal commencing during each time slot followed by a digitally encoded data signal, having a digitally encoded marker signal at a predetermined time period in each slot, said method comprising:

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storing the digitally encoded
synchronization signal (hereinafter: "first
synchronization signal") and the digitally
encoded data signal of a time slot, and the
5 digitally encoded synchronization signal of the
immediately succeeding time slot (hereinafter:
"second synchronization signal");

determining the location of a plurality of
minimum energy points of the stored digitally
10 encoded signals;

performing an equalization of said stored
digitally encoded signals starting from said
first synchronization signal to a first minimum
energy point;

15 performing an equalization of said stored
digitally encoded signals starting from said
marker signal to said first minimum energy
point;

performing an equalization of said stored
20 digitally encoded signals starting from said
marker signal to a second minimum energy point;
and

performing an equalization of said stored
digitally encoded signals starting from said
25 second synchronization signal to said second
minimum energy point.

49. The method of Claim 48 further comprising
the steps of:

30 comparing the energy level of each of said
plurality of minimum energy points to a
threshold level; and

performing an equalization of said stored
digitally encoded signals starting from said
first synchronization signal to said second

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synchronization signal, in the event said energy level of each of the minimum energy points is below said threshold level.

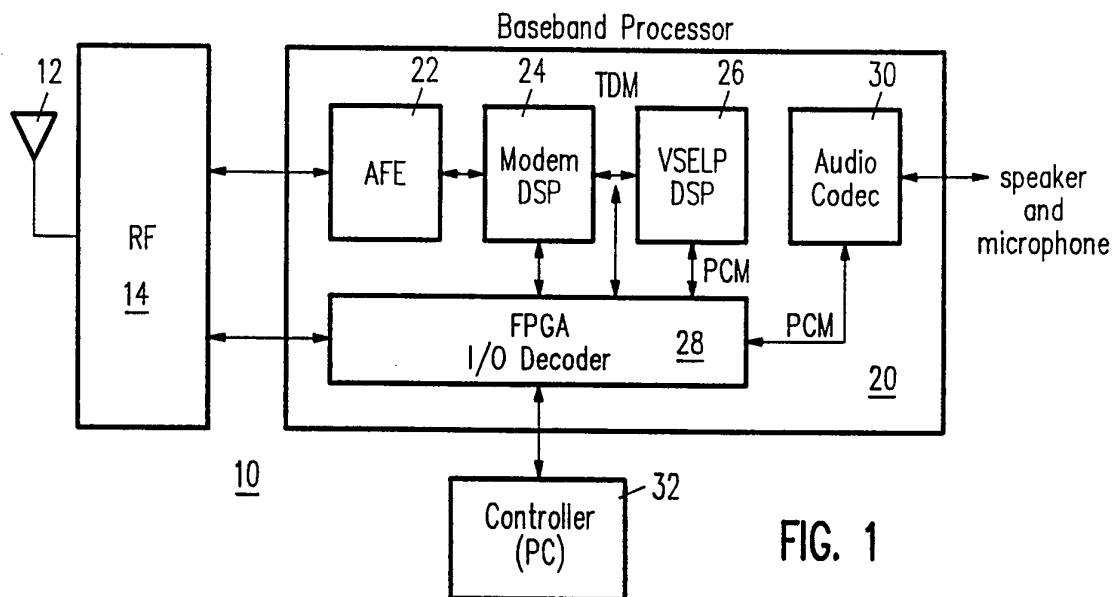


FIG. 1

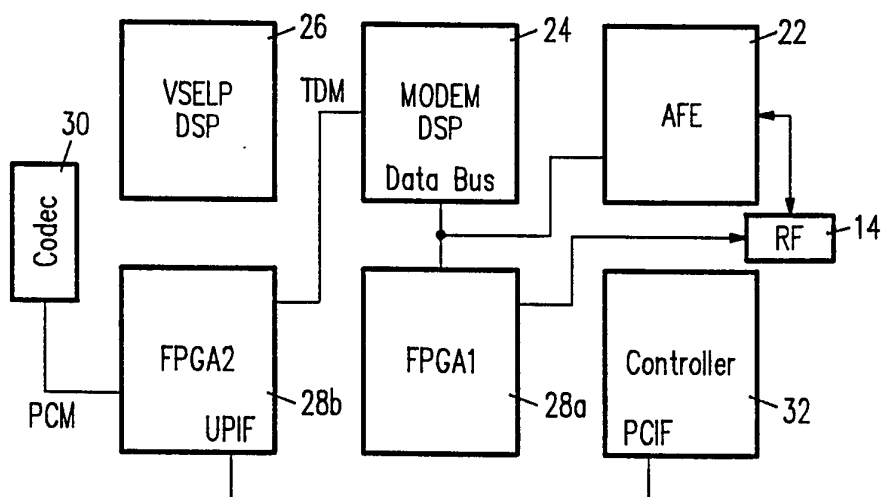


FIG. 2

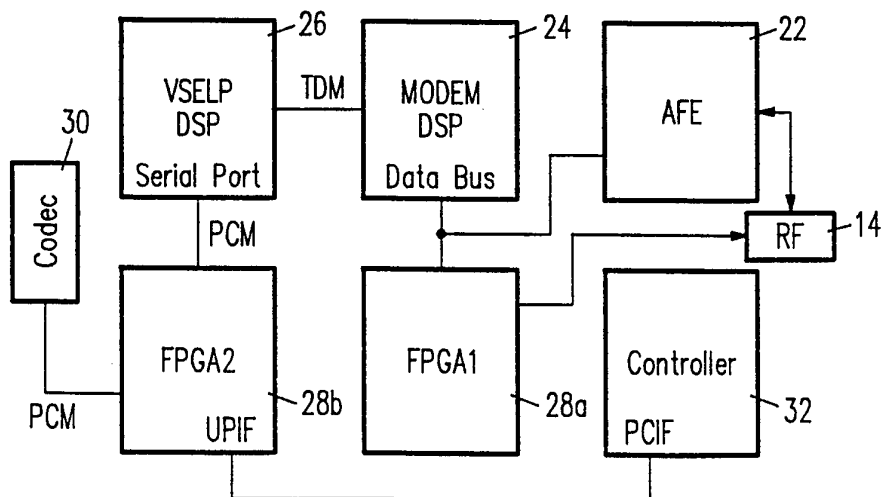


FIG. 3

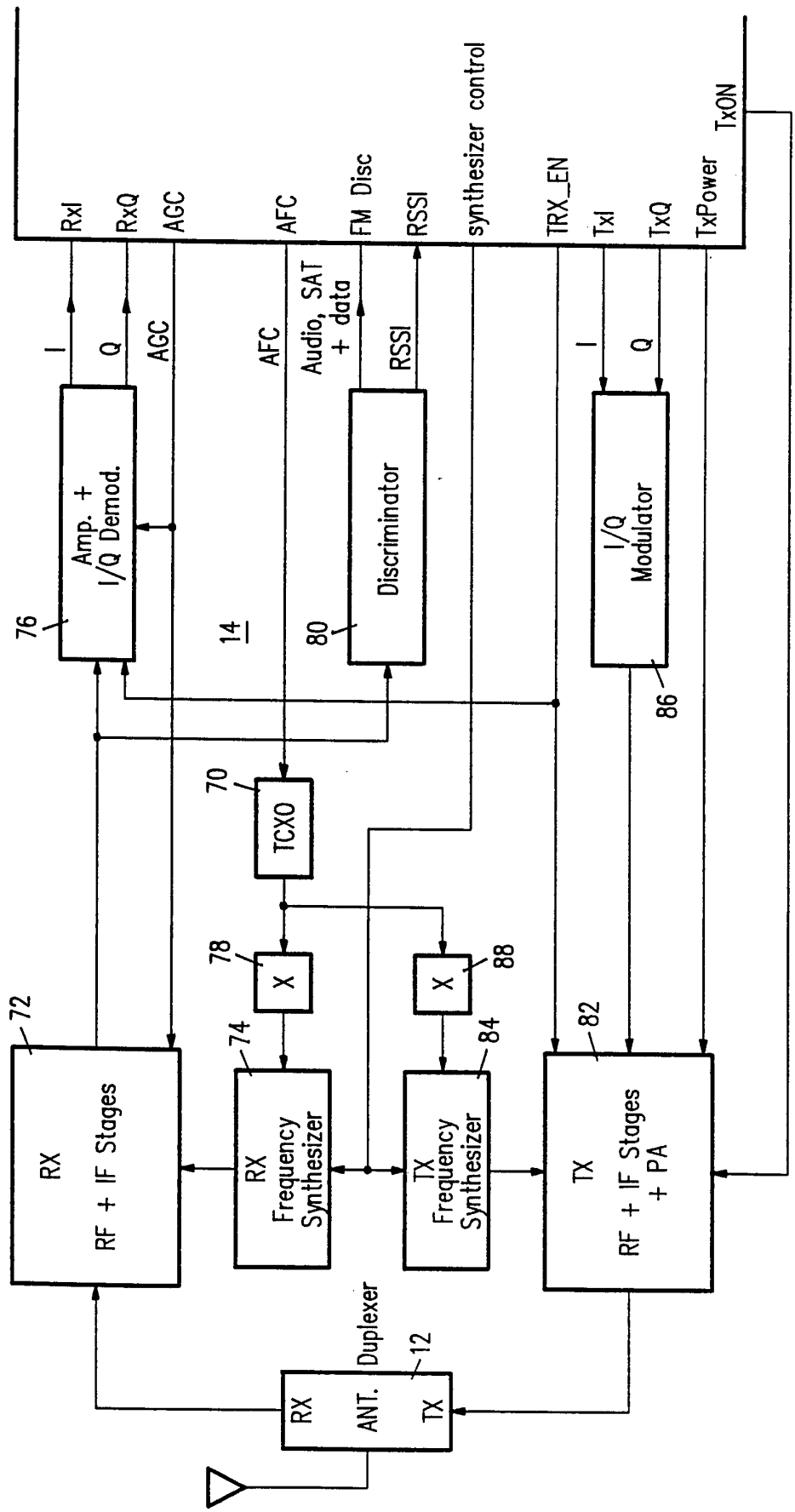


FIG. 4

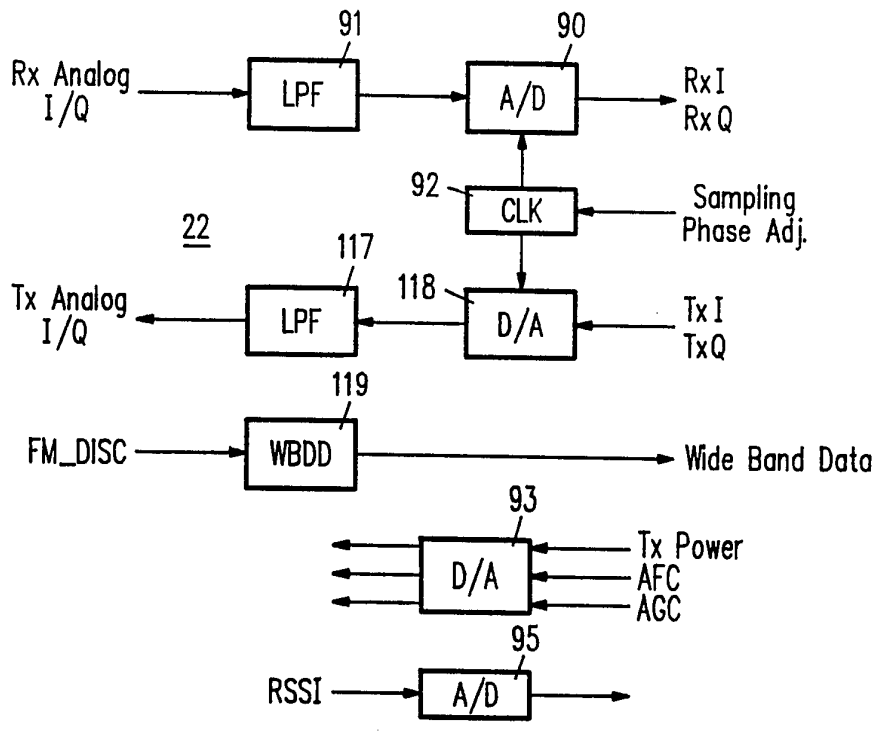


FIG. 5

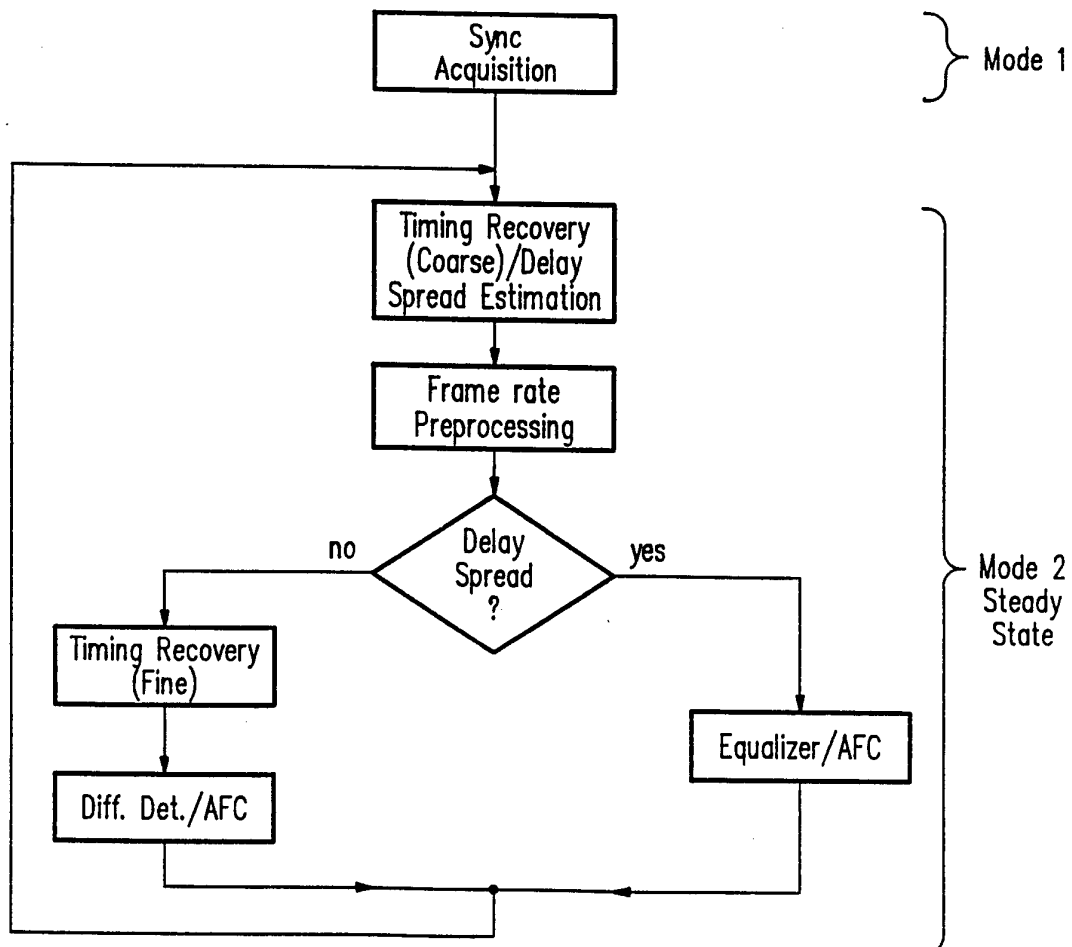


FIG. 6

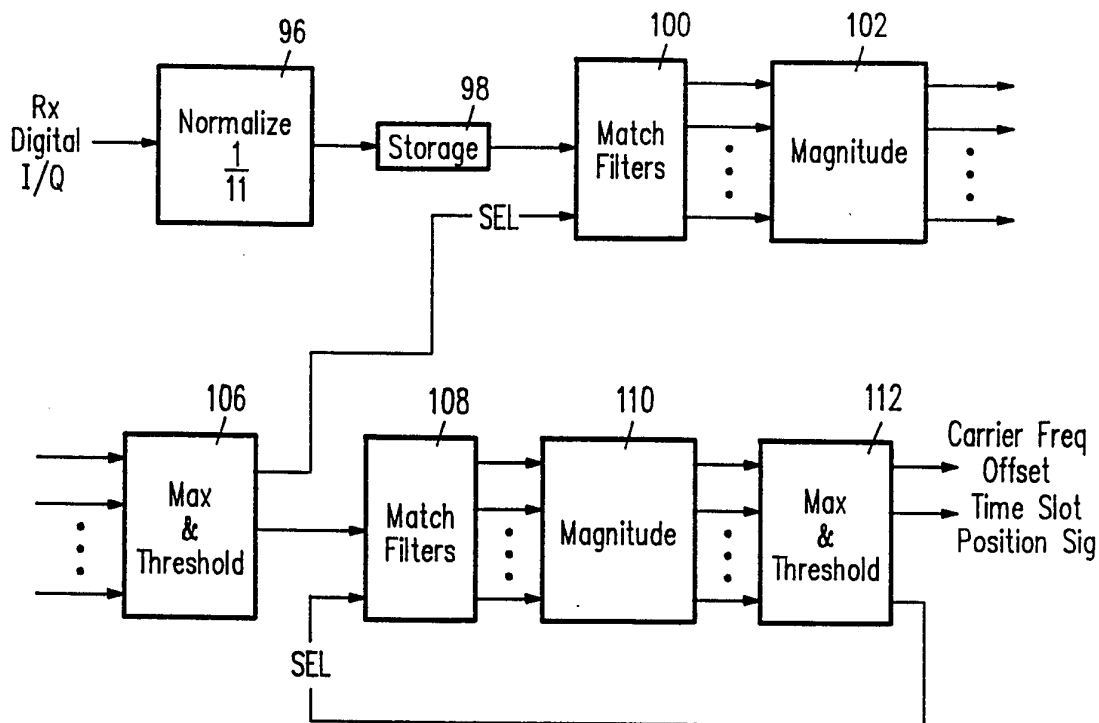


FIG. 7

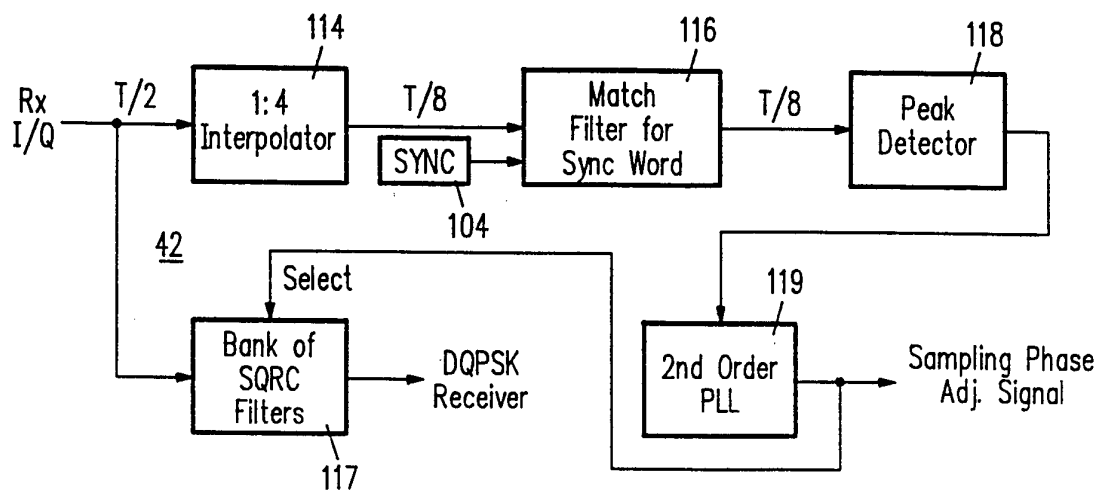


FIG. 9

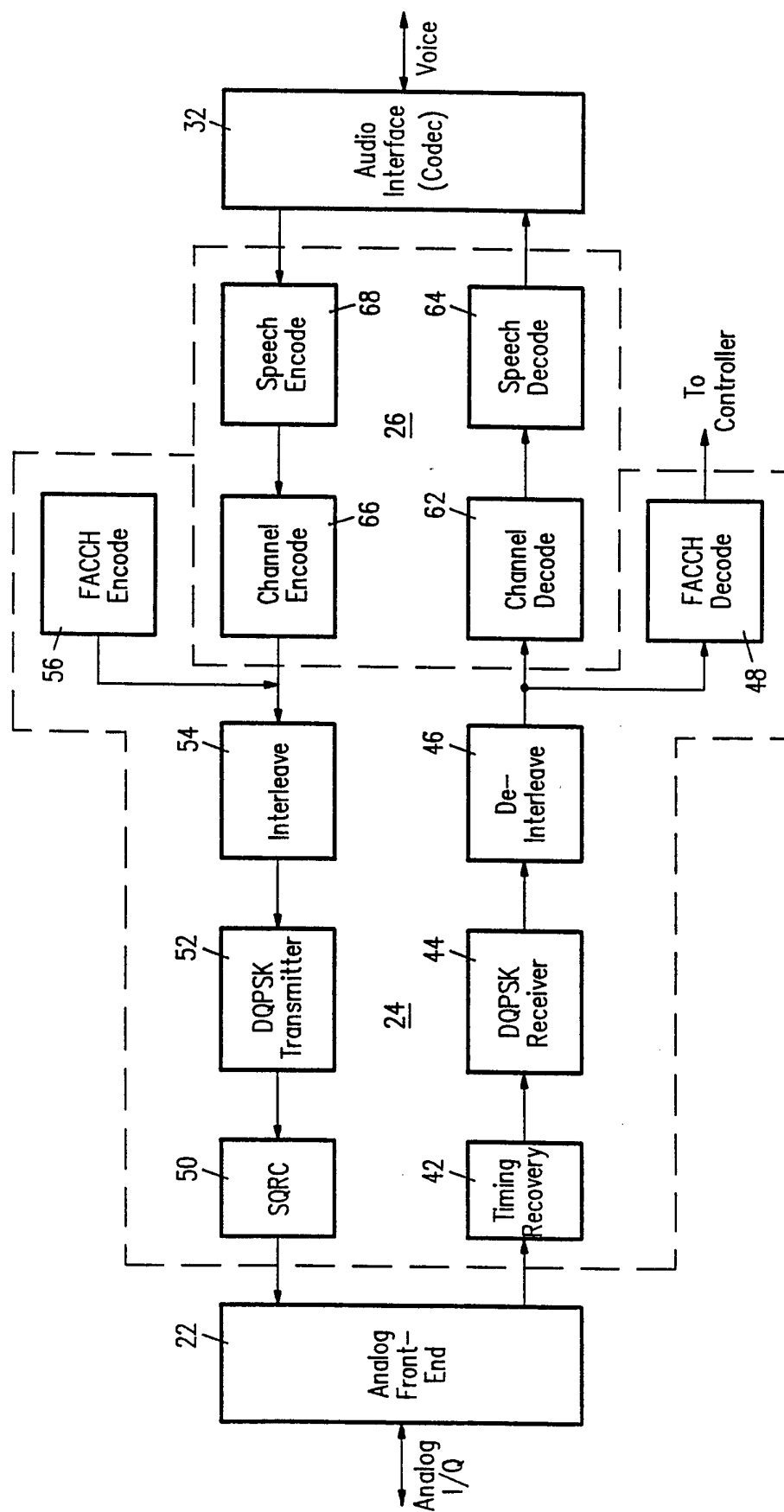


FIG. 8

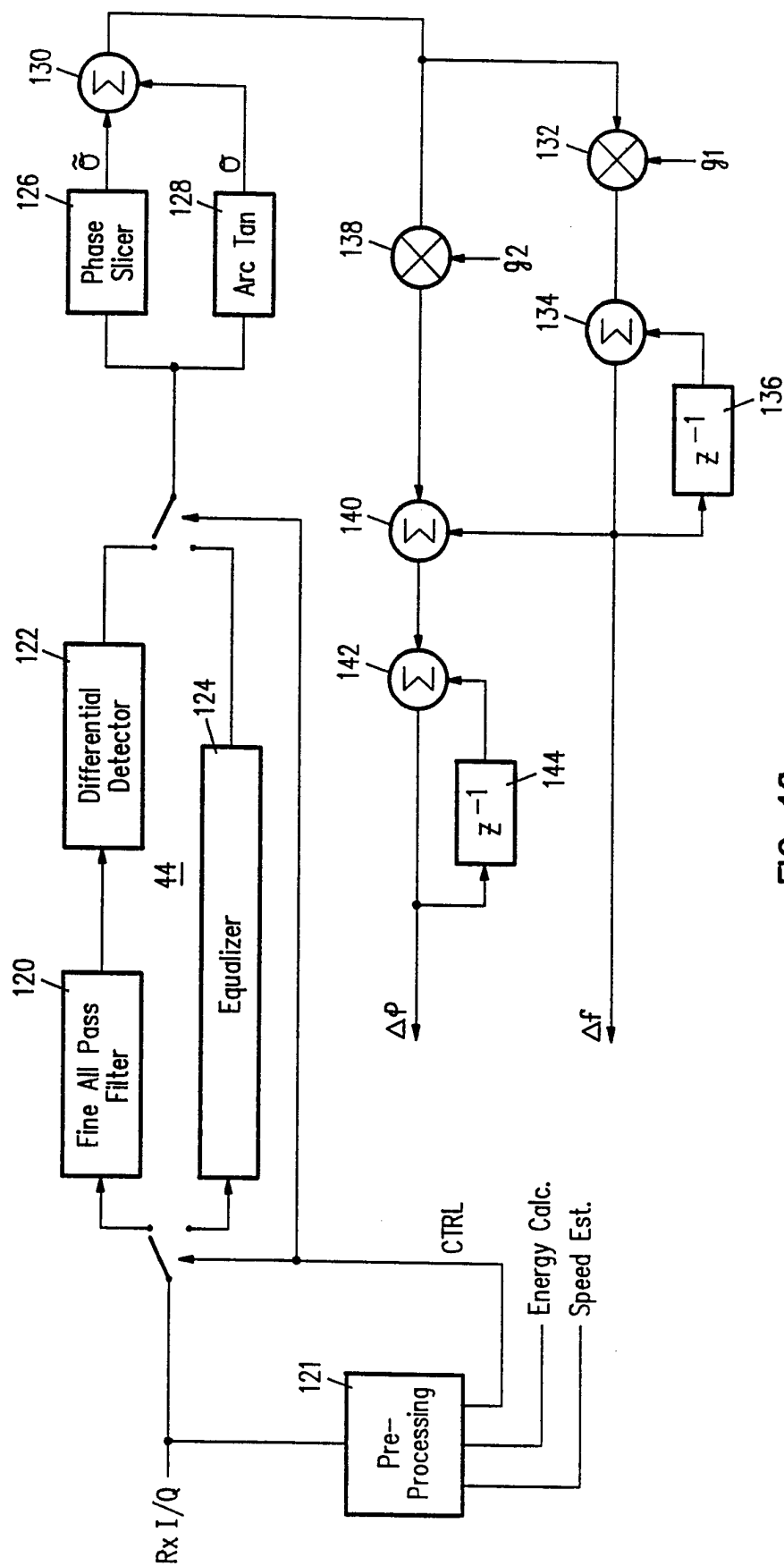


FIG. 10

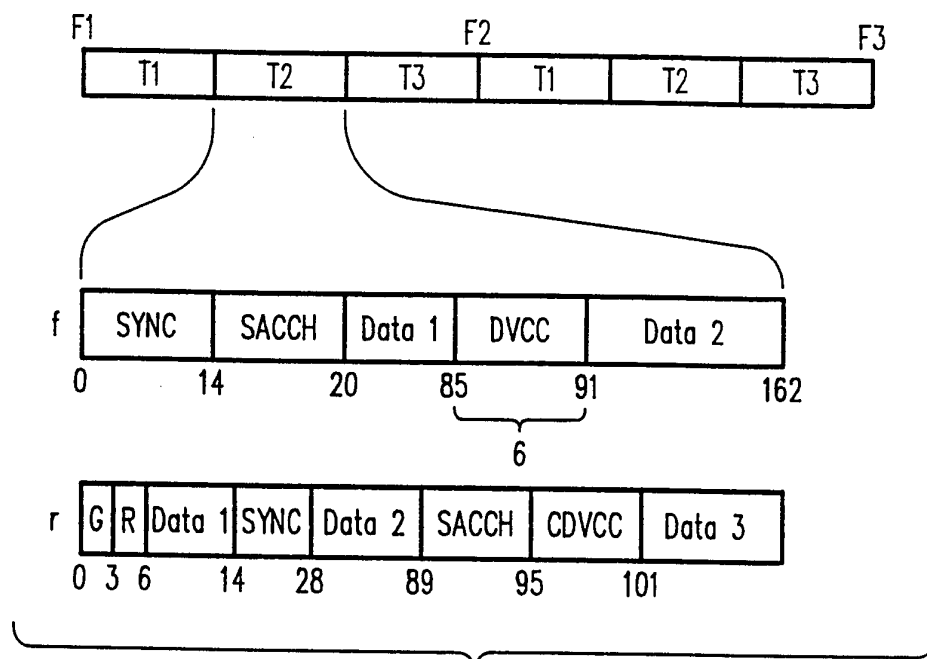


FIG. 11

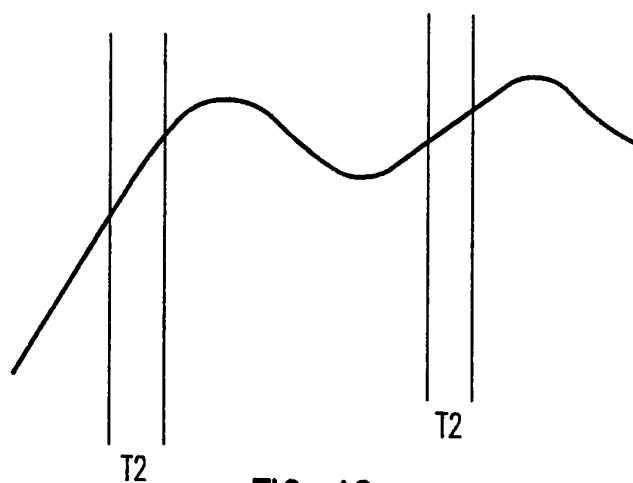


FIG. 12

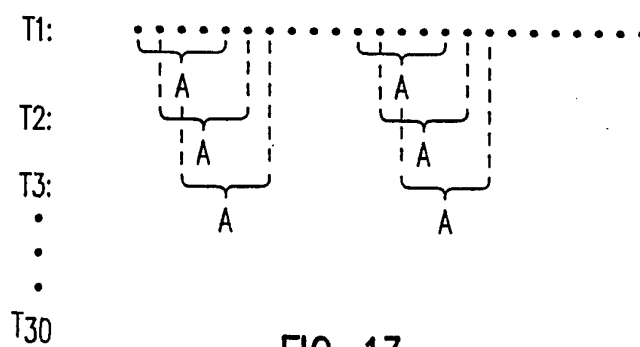


FIG. 13

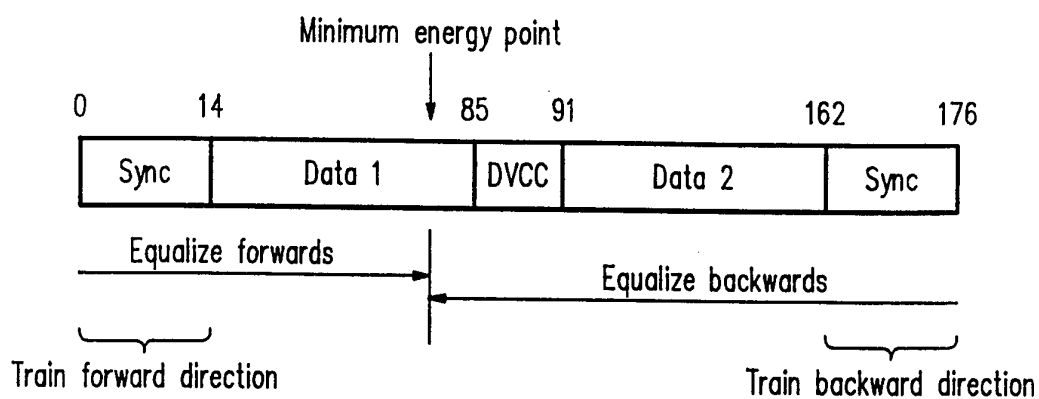


FIG. 14a

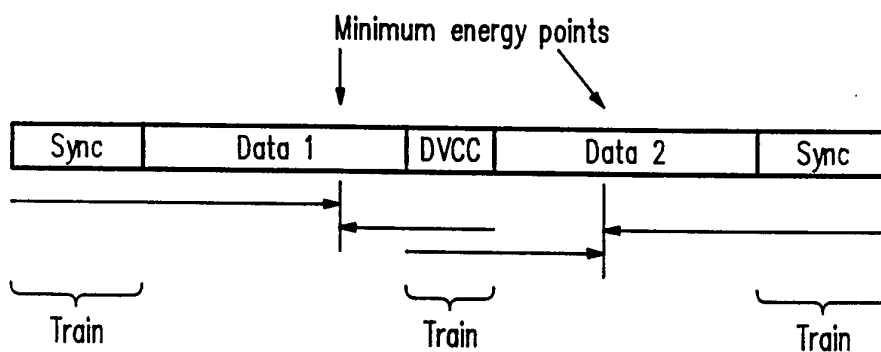


FIG. 14b

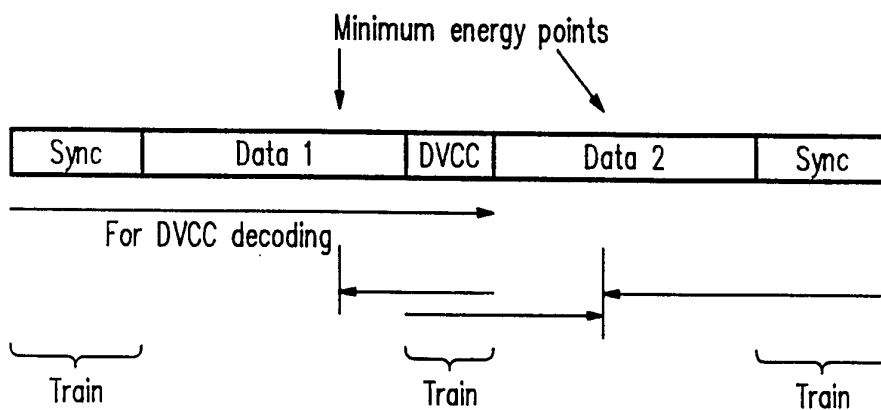


FIG. 14c

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/09175

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :IPC (5): H03D 1/00; H04L 7/00; H04L 27/06
US CL :375/11, 94, 95, 96, 97

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y, P	US, A, 5,263,026 (PARR et al) 16 November 1993, see fig. 1, column 2, lines 21-56 and columns 6-7.	46 and 48 47 and 49
A	US, A, 4,558,460 (TANAKA et al) 10 December 1985, see fig. 1.	1
A	US, A, 5,027,432 (SKALA et al) 25 JUNE 1991, see fig. 1.	1
A, P	WO, A, WO94197704 (TAKENAKA) 09 January 1994, see fig. 1.	1
A	US, A, 5,012,491 (IWASAKI) 30 April 1991, see fig. 1.	8-15

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
*A document defining the general state of the art which is not considered to be part of particular relevance	*X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
*E earlier document published on or after the international filing date	*Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
*L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*& document member of the same patent family
*O document referring to an oral disclosure, use, exhibition or other means	
*P document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

23 NOVEMBER 1994

Date of mailing of the international search report

13 DEC 1994

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
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Telephone No. (703) 305-4735

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/09175

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5,018,166 (TJAHJADI et al) 21 May 1991, see fig. 1.	8-15
A	US, A, 5,040,192 (TJAHJADI) 13 August 1991, see figs 1-2.	8-15
A,P	US, A, 5,276,706 (CRITCHLOW) 04 January 1994, see fig. 1.	8-15 and 29-45
Y	US, A, 4,466,108 (RHODES) 14 August 1984, see figs. 1 and 3.	16,17,19, 24,25 and 27
Y	US, A, 4,879,728 (TARALLO) 07 November 1989, see figs 1 and 3-5.	16,17,19, 24,25 and 27
A,P	US, A 5,272,446 (CHALMERS et al) 21 December 1993, see fig. 2.	29-45
A,P	US, A, 5,274,670 (SEIZAWA et al) 28 December 1993, see fig. 5.	46-49
A,P	US, A, 4,947,409 (RAITH et al) 07 August 1990, see figs 1 and 3.	16-28

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/09175

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US94/09175

B. FIELDS SEARCHED

Minimum documentation searched

Classification System: U.S.

375/11,13,14,58,94,95, 96, 97, 39; 455/257,283.1,33.1,33.2,52.3,54.1; 364/724.19; 370/93; 307/353; 328/63,72; 381/86;342/461;324/161,166,175

B. FIELDS SEARCHED

Electronic data bases consulted (Name of data base and where practicable terms used):

USPTO APS measuring(1a)speed and mobile units, average(1w)energy, Timing(1a)recover? and interpolat? filter, match?(1w)filter automatic frequency control and time slots, stor? synch? signal# and equaliz?

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING

This ISA found multiple inventions as follows:

Group I. Claims 1-7, drawn to estimating the relative speed of mobile digital communication systems based on the received energy level classified in class 375 subclass 94.

Group II. Claims 8-15, drawn to adjusting the sampling phase (timing recovery) of the received encoded signals classified in class 375, subclass 106.

Group III. Claims 16-28, drawn to controlling the frequency of the received digital signal classified in class 375, subclass 97.

Group IV. Claims 29-45 drawn to selecting a received signal among a plurality of sampled signals using a digital signal filters (matched filters) classified in class 375, subclass 96.

Group V. Claims 46-49, drawn to equalizing the digitally encoded signal classified in class 375, subclass 11.

Noting in particular that the method for estimating of relative speed of mobile units in group I does not include the apparatus and method for timing recovery in group II, the method and apparatus for controlling the frequency of the digitally encoded received signal in group III, method and apparatus for selecting among the plurality of sampled signal from a received digital signal using a matched filter in group IV, and method and apparatus for equalizing the digitally encoded received signal in V.

Noting the method and apparatus for timing recovery in group II does not include the method and apparatus for controlling the frequency of the digitally encoded received signal in group III, method and apparatus for selecting among the plurality of sampled signal from a received digital signal using a matched filter in group IV, and method and apparatus for equalizing the digitally encoded received signal in V.

Noting the method and apparatus for controlling the frequency of the digitally encoded received signal in group III does not include method and apparatus for selecting among the plurality of sampled signal from a received digital signal using a matched filter in group IV, and method and apparatus for equalizing the digitally encoded received signal in V. Noting the method and apparatus for selecting among the plurality of sampled signal from a received digital signal using a matched filter in group IV does not include, method and apparatus for equalizing the digitally encoded received signal in V.

Since the claims of the different groups, groups I-V, do not share or have in common the same special technical feature as indicated above, there is no unity between the groups.