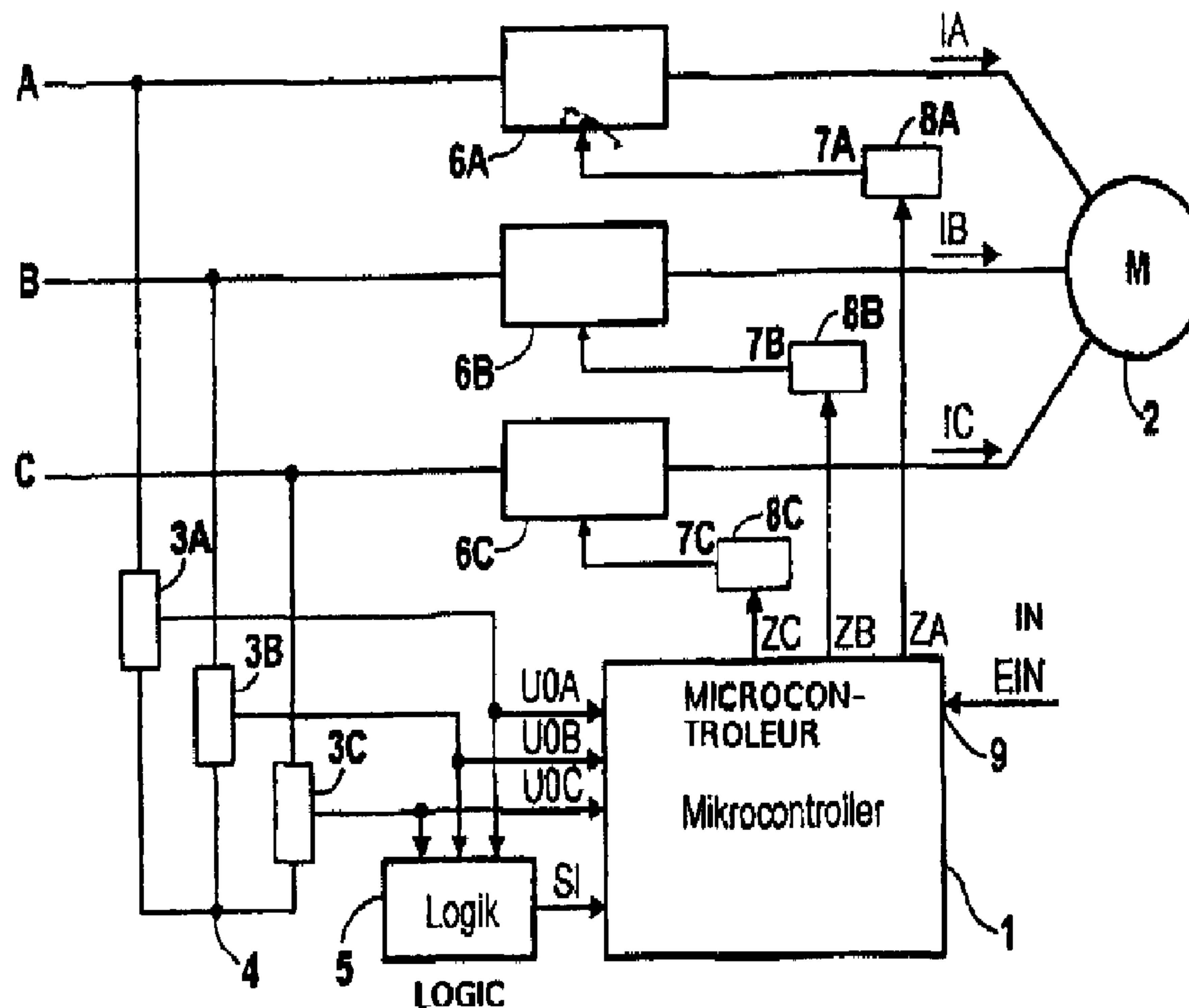




(86) Date de dépôt PCT/PCT Filing Date: 1997/10/07
(87) Date publication PCT/PCT Publication Date: 1998/04/16
(45) Date de délivrance/Issue Date: 2001/09/04
(85) Entrée phase nationale/National Entry: 1999/04/08
(86) N° demande PCT/PCT Application No.: DE 97/02298
(87) N° publication PCT/PCT Publication No.: WO 98/16004
(30) Priorité/Priority: 1996/10/10 (196 41 832.1) DE

(51) Cl.Int.⁶/Int.Cl.⁶ H02P 7/622
(72) Inventeurs/Inventors:
SEITZ, Johann, DE;
FRITSCH, Andreas, DE
(73) Propriétaire/Owner:
SIEMENS AKTIENGESELLSCHAFT, DE
(74) Agent: FETHERSTONHAUGH & CO.

(54) Titre : REGULATEUR DE COURANT TRIPHASE AVEC COMMANDE DE PHASE REALISEE PAR INTERRUPTION
(54) Title: THREE-PHASE POWER CONTROLLER WITH INTERRUPT-CONTROLLED PHASE-GATING CONTROL



(57) Abrégé/Abstract:

This invention concerns a three-phase current regulator with interrupt-performed phase control characterized by a simple, cost-effective design, particularly by the use of a simple microcontroller (1) with only one or two interrupt inputs. This is made possible by forming zero crossover signals (U0A, U0B, U0C) the edges of which can be used for interrupt control. Interrupt routines in the program of the microcontroller (1) control the times for output of firing signals (ZA, ZB, ZC) starting exclusively from the zero crossovers as data about the three-phase network.



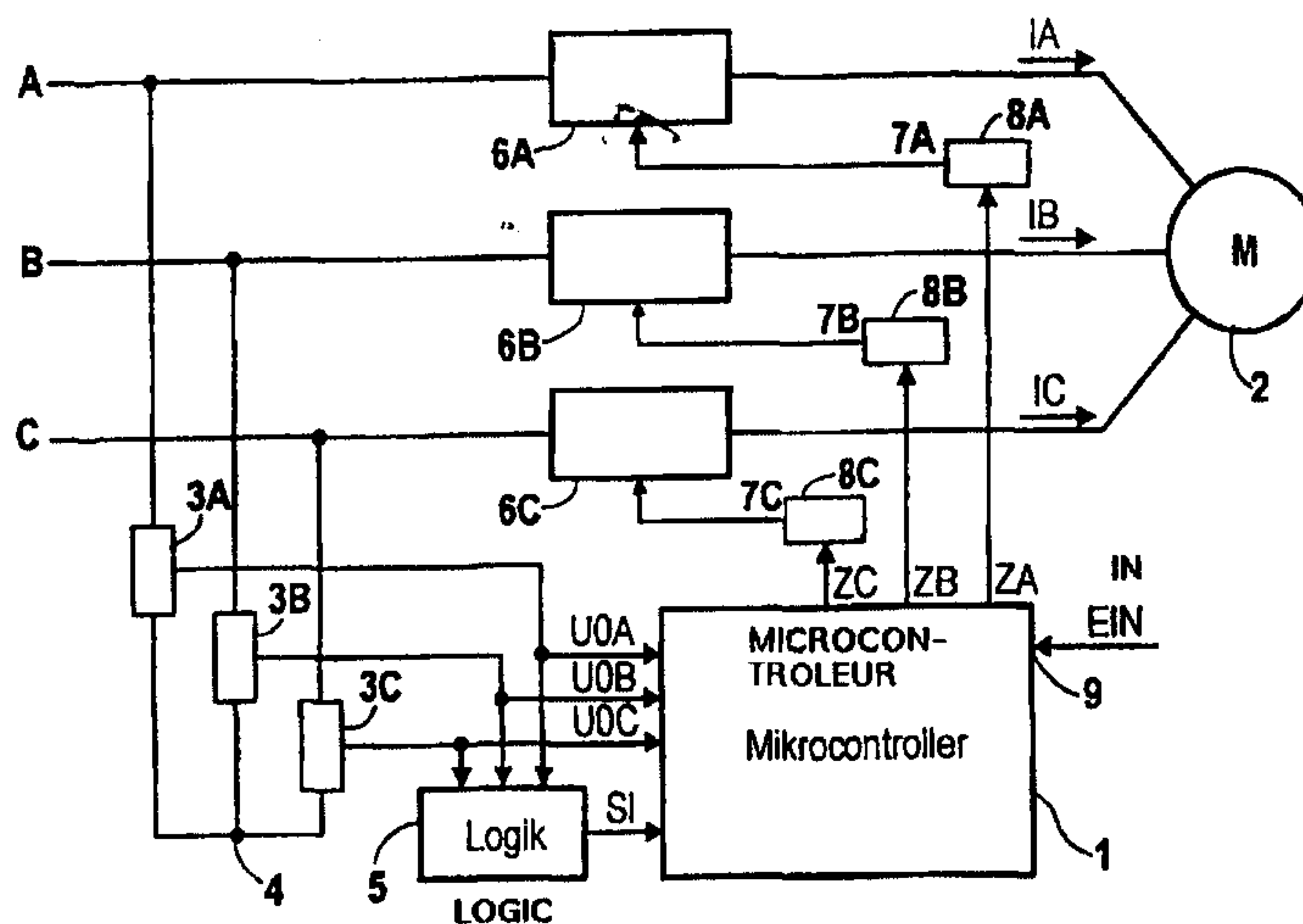


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WELTORGANISATION FÜR GEISTIGES EIGENTUM
Internationales Büro
INTERNATIONALE ANMELDUNG VERÖFFENTLICHT NACH DEM VERTRAG ÜBER DIE
INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT)

(51) Internationale Patentklassifikation ⁶ : H02P 7/622	A1	(11) Internationale Veröffentlichungsnummer: WO 98/16004 (43) Internationales Veröffentlichungsdatum: 16. April 1998 (16.04.98)
(21) Internationales Aktenzeichen: PCT/DE97/02298 (22) Internationales Anmeldedatum: 7. Oktober 1997 (07.10.97) (30) Prioritätsdaten: 196 41 832.1 10. Oktober 1996 (10.10.96) DE (71) Anmelder (für alle Bestimmungsstaaten ausser US): SIEMENS AKTIENGESELLSCHAFT [DE/DE]; Wittelsbacherplatz 2, D-80333 München (DE). (72) Erfinder; und (75) Erfinder/Anmelder (nur für US): FRITSCH, Andreas [DE/DE]; Ganghoferweg 2, D-92245 Kümmersbruck (DE). SEITZ, Johann [DE/DE]; Im Drillingsfeld 14, D-92224 Amberg (DE).		(81) Bestimmungsstaaten: AU, BR, CA, US, europäisches Patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Veröffentlicht <i>Mit internationalem Recherchenbericht.</i>

(54) Title: THREE-PHASE CURRENT REGULATOR WITH INTERRUPT-PERFORMED PHASE CONTROL

(54) Bezeichnung: DREHSTROMSTELLER MIT INTERRUPTGESTEUERTER PHASENANSCHNITTSTEUERUNG



(57) Abstract

This invention concerns a three-phase current regulator with interrupt-performed phase control characterized by a simple, cost-effective design, particularly by the use of a simple microcontroller (1) with only one or two interrupt inputs. This is made possible by forming zero crossover signals (U0A, U0B, U0C) the edges of which can be used for interrupt control. Interrupt routines in the program of the microcontroller (1) control the times for output of firing signals (ZA, ZB, ZC) starting exclusively from the zero crossovers as data about the three-phase network.

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Description

Three-phase power controller with interrupt-controlled
5 phase-gating control

The invention relates to a three-phase power controller for controlling a load which is connected to a three-phase mains system, having a microcontroller,
10 having voltage detection devices which produce voltage zero signals which are associated with the voltage zeroes in the individual mains-system phases, from which signals the microcontroller derives trigger signals for driving phase-related semiconductor valves.
15 The invention furthermore relates to a method for phase-gating control of a three-phase power controller.

A three-phase power controller of this generic type is disclosed in EP 0 435 038 B1. In this case, the time at which the semiconductor valves are triggered in
20 order to carry out phase-gating control is derived from the time difference between the voltage zero of one phase of the three-phase mains system and the switching-off of the semiconductor valve associated with this phase.

25 British Patent Specification 2 084 359 discloses an apparatus for controlling a three-phase asynchronous motor. To this end, controllable semiconductor valves, in particular a triac or back-to-back connected thyristors are assigned to each supply
30 phase in the motor and allow power to be supplied to the motor in a controlled manner via phase-gating control. The time of the current zero is used as the time reference for determining the triggering times for the semiconductor valves in the known apparatus, this
35 time being determined by measuring the voltage drop across the semiconductor valve. This voltage is supplied to a comparator whose output states correspond to the switching states of the semiconductor valve. The current zero then

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corresponds to one flank of the output signal of the comparator, from which a monoflop is used to produce a sampling pulse for a ramp voltage which is synchronized to the supply voltage zero. The sampled value of the ramp voltage is subtracted from a reference voltage, which is entered externally via a potentiometer, and is passed to the inverting input of a differential amplifier. Its output voltage is supplied together with the ramp voltage in a further comparator, which uses a downstream trigger pulse generator to produce a primary trigger signal when the ramp voltage exceeds the output voltage of the differential amplifier.

Most known solutions use the current zeroes or a combination of voltage and current zeroes in the individual phases to derive the trigger time for the semiconductor valves in three-phase power controllers. When determining the current zero, the voltage across the semiconductor valve is generally evaluated, and an ON or OFF signal is derived. In this case, the use of the voltage across the semiconductor valve may be regarded as being problematic, since this voltage is the difference between the mains-system voltages and the induced motor voltage. In the event of any voltage drops in the mains-system voltage, this difference can, for example tend to zero, which then results in the current zero not being detected.

The invention is based on the object of providing a three-phase power controller of the type mentioned above which is particularly simple, that is to say it can be constructed using cost-effective components. Another object is to specify a method for phase-gating control of a three-phase power controller of the type mentioned above, which allows a hardware design with low costs.

The first object is achieved in that the voltage zero signals are square-wave signals whose flanks are used for interrupt control of an executive program in the microcontroller, the interrupt routines which are associated
5 with the interrupt control in the executive program controlling the switch-on times of the trigger signals exclusively on the basis of the voltage zeroes as information about the three-phase mains system.

A particularly simple development of the invention
10 consists in that only two voltage detection devices are provided which produce, as voltage zero signals of two mains-system phases, square-wave signals whose flanks are used for interrupt control by the microcontroller. The microcontroller required for this purpose is of an even simpler design since it
15 requires only two interrupt inputs, three port lines and two timers.

If a common interrupt signal, which is formed from the square-wave signals in a logic device, is supplied to the microcontroller for interrupt control, then a microcontroller
20 with only one interrupt input is sufficient to achieve this.

In accordance with the present invention there is provided a three-phase power controller for controlling a load which is connected to a three-phase mains system, having a microcontroller, having voltage detection devices which produce
25 voltage zero signals which are associated with the voltage zeroes in the individual mains-system phases, from which signals the microcontroller derives trigger signals for driving phase-related semiconductor valves, characterized in that the voltage zero signals are square-wave signals whose flanks are
30 used for interrupt control of an executive program in the microcontroller, the interrupt routines which are associated

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with the interrupt control in the executive program controlling the switch-on times of the trigger signals exclusively on the basis of the voltage zeroes as information about the three-phase mains system, and the trigger signals always being
5 switched off directly after each voltage zero.

In accordance with the present invention there is provided a method for phase-gating the control of a three-phase power controller for controlling a three-phase load which is connected to a three-phase mains system, having a
10 microcontroller, having voltage detection devices which produce voltage zero signals which are associated with the voltage zeroes in the individual mains-system phases, from which signals the microcontroller derives trigger signals for driving phase-related semiconductor valves, characterized in that the
15 voltage zero detection devices produce square-wave voltage zero signals, which are combined via a logic device to form a common interrupt signal in that a jump is made to an interrupt routine either on each negative flank or on each positive flank in the common interrupt signal, in which interrupt routine the
20 triggering voltage zero is first of all assigned one of the mains-system phases, and a timer-interrupt-controlled sequence is then initiated for the associated mains-system phase, in order to produce a trigger signal for the semiconductor valve for the relevant mains-system phase.

25 Further advantageous embodiments of the three-phase power controller according to the invention can be found in the dependent claims 4 to 7.

The method according to claim 8 is proposed in order to achieve the other object.

30 An exemplary embodiment of the invention is explained in the following text with reference to the drawing, in which:

3b

FIG 1

shows a simplified circuit diagram of a three-phase power controller for controlling, for example, a three-phase asynchronous motor,

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- FIG 2 shows the time waveforms of mains system variables and signals relating to the three-phase power controller according to FIG 1,
- 5 FIG 3 shows the initialization routine with an endless loop in the interrupt-controlled method for controlling the three-phase power controller, applied to the three-phase power controller according to FIG 1,
- 10 FIG 4 shows the voltage zero interrupt routine in the interrupt-controlled method for controlling the three-phase power controller,
- 15 FIGS 5,6 and 7 show timer interrupt routines for the interrupt-controlled method for controlling the three-phase power controller,
- 20 FIG 8 shows a simplified illustration of a circuit of a three-phase power controller with two voltage zero detection devices,
- 25 FIG 9 shows mains system variables as well as signals relating to the operation of the three-phase power controller according to FIG 8,
- 30 FIG 10 shows the initialization routine with an endless loop for the interrupt-controlled method for controlling the three-phase power controller according to FIG 8,
- 35 FIGS 11 and 12 show the voltage zero interrupt routines for the interrupt-controlled method for controlling the three-phase power controller according to FIG 8,
- FIG 13 shows the triggering routine for the interrupt-controlled method for controlling the three-phase power controller according to FIG 8, and

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FIGs 14 and 15 show timer-interrupt routines for the interrupt-controlled method for controlling the three-phase power controller according to FIG 8.

5

FIG 1 shows a simplified circuit diagram of a three-phase power controller according to the invention, by means of which a load which is connected to three mains-system phases A, B and C of a three-phase mains system, for example a three-phase asynchronous motor 2, can be controlled. In this case, a semiconductor valve 6A, 6B or 6C, respectively, for example a triac or a thyristor circuit comprising two back-to-back connected thyristors, is connected in each of the supply leads of the three mains-system phases A, B and C to the load 2. The semiconductor valves 6A, 6B and 6C are connected via control lines 7A, 7B and 7C to trigger devices 8A, 8B and 8C. A microcontroller 1 is connected via signal lines to the trigger devices 8A, 8b and 8C. The microcontroller 1 emits trigger signals ZA, ZB and ZC via the signal lines to the trigger devices 8A, 8B and 8C so that the semiconductor valves 6A, 6B and 6C can be driven, that is to say they can be switched on and off directly. In the present exemplary embodiment, although the trigger signals ZA, ZB and ZC are low-active, that is to say the low level 0 on the signal lines corresponds to the ON state and the high level 1 corresponds to the OFF state, an embodiment with high-active trigger signals ZA, ZB and ZC is likewise also feasible. The microcontroller 1 has at least one interrupt input, seven port lines and three timers. The three timers (which are not illustrated in the drawing) for the microcontroller 1 are required to achieve separate and independent phase gating in the mains-system phases A, B and C, one timer being permanently allocated to each of the three mains-system phases A, B and C. The term phase gating in this case means a defined time delay between the voltage zero in one mains-system phase A, B or C of the connected

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three-phase mains system and the switching-on of the semiconductor valve 6A, 6B or 6C in the relevant

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mains-system phase, as is illustrated in FIG 2, which is explained in the following text. Voltage zero detection devices 3A, 3B and 3C, which are connected to the mains-system phases A, B and C, are used to detect the voltage zeroes of the voltages UA, UB, UC of the individual mains-system phases A, B and C with respect to a synthetic star point 4, at which the voltage zero detection devices 3A, 3B and 3C are connected to one another. The voltage zero detection devices 3A, 3B and 3C are in this case designed such that they supply a high signal in response to voltage values above a positive voltage reference or below a negative voltage reference, and supply a low signal at the voltage zero in the individual mains-system phases A, B or C, that is to say when the voltage is less than the positive reference value or greater than the negative reference value. The voltage zero detection devices 3A, 3B and 3C form voltage zero signals U0A, U0B and U0C. These signals are supplied on the one hand to the microcontroller 1 and on the other hand to a logic device 5, which combines these three voltage zero signals U0A, U0B and U0C to form a common interrupt signal SI, which is passed to the interrupt input of the microcontroller 1. The interrupt input of the microcontroller 1 is in this case designed to be negative-flank triggered so that each negative flank in the common interrupt signal SI triggers within the executive program in the microcontroller 1 an interrupt which is called a "voltage zero interrupt". However, in principle, positive flank triggering is also possible.

FIG 2 shows the time waveforms of mains system variables and signals which are of interest for understanding the interrupt-controlled method for controlling a three-phase power controller according to the invention. The three upper waveforms indicate the voltages UA, UB and UC, which are applied to the voltage zero detection devices 3A, 3B and 3C,

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of the individual mains-system phases A, B and C. The corresponding square-wave voltage zero signals U0A, U0B and U0C which are produced by the voltage zero detection devices 3A, 3B and 3C are shown underneath these first three waveforms. SI denotes the common interrupt signal formed in the logic device 5. On the basis of the negative flanks 11 of the common interrupt signal SI after assignment to the respective mains-system phase A, B or C having the voltage zero, that is to say the voltage zero signal U0A, U0B or U0C and once a predetermined time value 13A, 13B or 13C, respectively, has elapsed, a trigger signal is emitted in the relevant phases at the times 14A, 14B, 14C as can be seen from the waveforms denoted by ZA, ZB and ZC. This results in the current wave forms denoted by IA, IB and IC.

The executive program contained in the microcontroller 1 of the three-phase power controller operates using an interrupt-controlled method. This starts with an initialization routine according to FIG 3, which shows the sequence in the microcontroller 1 from the switching on of the supply voltage for the microcontroller 1, denoted as the start 30 in the diagram, until an endless loop 36 is called. After the start, all the system initialization actions required for the method are carried out first of all, as stated in the block 31. Following this, all three trigger signals ZA, ZB and ZC are sent to the defined output state OFF, as shown by the blocks 32, 33 and 34. Once this has been done the interrupts used by the microcontroller 1 for the method are enabled in the block 35. Interrupt enabling is followed directly by the endless loop 36, in which the interrupt-controlled method is embedded and which runs until the supply voltage for the microcontroller 1 is switched off.

The sequence of the interrupt-controlled method for phase-gating control is described in the following text, by way of example, for the mains-system

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phase A. The phase-gating control actions in the mains-system phases B and C are carried out in a corresponding manner.

The interrupt-controlled method is initiated by
5 the negative flank (denoted 11 in FIG 2) in the common
interrupt signal SI, with the voltage zero interrupt
routine according to FIG 4, in the microcontroller 1.
In the voltage zero interrupt routine in block 41, the
first step is to evaluate the state of the control
10 input signal ON denoted by 9 in FIG 1. If a control
input signal is activated, that is to say $ON = 0$, the
time value corresponding to a predetermined phase-
gating value is calculated in the block 42. This value
is then checked in the block 43 against a minimum
15 value, which defines the time for ending the phase-
gating control. The jump to end the phase-gating
control is explained at the end of the description.
Assuming that the minimum-value check gives a positive
result, the next step of the voltage zero interrupt
20 routine in the block 44 produces, via the condition
 $U0A = 0$, the association between the initiating
interrupt event, namely the negative flank in the
common interrupt signal SI denoted by 11, and the
voltage zero, denoted by 10A, in the mains-system
25 voltage UA. After confirming this association, the
trigger signal ZA for the mains-system phase A is
switched off in the block 46. It is admittedly not
absolutely essential to switch off the trigger signal
ZA at this time, which is denoted by 12A in FIG 2, when
30 the first phase-gating action takes place after the
activation of the method by the control input ON
denoted by the reference number 9, since the trigger
signal ZA is already in the switched-off state by
virtue of the assignment in the initialization routine
35 before the first phase-gating action but, in order to
simplify the software control structure,

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the trigger signal ZA or ZB and ZC is also switched off during the first phase-gating action.

Once the trigger signal ZA has been switched off, the timer associated with the mains-system phase A is loaded, in the block 49, with the previously calculated time value, is activated in the subsequent block 52 and the voltage zero interrupt routine is then left once again via the questions $U0B = 0$ and $U0C = 0$, which cannot be satisfied at the same time.

Once the time value loaded into the timer for the mains-system phase A has elapsed, denoted by 13A in FIG 2, this initiates an interrupt, and the microcontroller 1 makes a jump to a time interrupt routine for the mains-system phase A according to FIG 5. In this routine, trigger signal ZA is switched on in the block 61, as a result of which the semiconductor valve 5A in the mains-system phase A is triggered via the trigger device 8A and the connecting line 7A. This time when the trigger signal ZA is switched on is denoted by 14a in the time waveform in FIG 2. Before leaving this timer interrupt routine, the timer is deactivated again in the block 62.

The trigger signal ZA for the mains-system phase A remains switched on until the next voltage zero of the voltage UA, which is denoted by 22 here in FIG 2. The associated switching-off of the trigger signal ZA at the time 15A is carried out in the voltage zero interrupt routine, which is initiated by this voltage zero, immediately before the associated timer is, according to block 49, loaded with the next phase-gating value or the corresponding time value. The time waveform illustrated in FIG 2 for the trigger signal ZA of the semiconductor valve 6A is produced by the repetition of the described sequence.

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The interrupt-controlled phase-gating control sequence described for the mains-system phase A is carried out in the same way for the mains-system phases B and C. This results in the corresponding time waveforms for the trigger signals ZB and ZC for the semiconductor valves 6B and 6C according to FIG 2.

In a three-phase system without a neutral conductor, at least two phases must be switched on at the same time for any current to flow, that is to say a corresponding time overlap of two trigger signals ZA, ZB, ZC is required. Based on the three-phase mains-system phase sequence illustrated in FIG 2, current first flows once the semiconductor valve 6B in the mains-system phase B has been switched on by the trigger signal ZB at the time 14B. Between the time 14B in the ZB waveform and the time 15A in the ZA waveform there is a time overlap when the trigger signals ZA and ZB are switched on, and this result in the current wave forms IA and IB with the current peaks 16 and 17 in the mains-system phases A and B.

The next time overlap of two switched-on trigger signals occurs from the time 14C in the ZC waveform to the time 15B in the ZB waveform, which results in the right-hand half of the current flow denoted by 17 in the mains-system phase B and the left-hand half of the current flow denoted by 18 in the IC waveform in the mains-system phase C. The splitting of the current waveforms into two sections is a result of the current flow being commutated, as a function of the phase-gating, from one pair of phases to another phases. In the case of the current flow denoted by 17, the current in the three-phase system commutates, for example as a result of the trigger signal ZC for the mains-system phase C being switched on at the time 14C, from the pair of phases AB to the pair of phases BC.

In order to achieve a time overlap of two switched-on trigger signals, the trigger signal of the

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second mains-system phase involved must always be switched on, for example at the time 14B, before the trigger signal for the first mains-system phase to be switched on is switched off, for example at the time 15A. In order to satisfy this condition, the phase-gating value must always be less than 120° electrical. This is obvious from the fact that, for example in the case of a balanced three-phase mains system, the loading of the timer with the time value 13B for phase gating of the second mains-system phase involved, at the time 12B always takes place 60° after the loading of the time value 13A for the phase-gating value of the first mains phase involved, at the time 12A, and as a result of the fact that the trigger signal ZA of the mains-system phase A that is the first to be switched on is switched off at the time 15A, always 180° after the time 12A.

Owing to the inductive elements when motor windings are connected, the end of the current flow within a mains-system phase, denoted by 19, 20 and 21, for example, in FIG 2, never takes place at the same time as or at a time before the trigger signal in this mains-system phase is switched off, for example at the times 15A, 15B or 15C, but always with a time delay with respect to the time at which the trigger signal is switched off. Owing to this characteristic of the current waveforms and the switching-off of the trigger signal for the semiconductor valve whenever a voltage zero occurs in a mains-system phase, double or multiple triggering within one half-cycle of a mains-system phase, which is denoted for example by the start time 10A and the end time 22 in the waveform of the phase voltage UA, can be virtually precluded. The duration of the time delay between the end of the current flow and the switching-off of the trigger signal is in this case dependent on the inductive element of the motor winding, which varies dynamically while the connected motor is accelerating from rest to the rated speed.

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The described sequence of interrupt-controlled phase-gating control repeats itself with a

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phase-gating value which is in each case reduced by a predetermined step width, until the time value which corresponds to the phase-gating value falls below a permanently specified minimum value, which is checked
5 in the voltage zero interrupt routine according to block 43 in FIG 4. At the same time, for example, a connected motor 2 as the load accelerates smoothly from rest to the rated speed, in which case it is possible to vary the soft starting time of the motor 2 by
10 selecting the step width for the reduction in the phase-gating value. Once the permanently specified minimum value for phase gating has been reached, which minimum value is chosen such that the connecting motor 2 has undoubtedly accelerated by the time this minimum
15 value is reached, the three semiconductor valves 6A, 6B and 6C are driven without any phase gating by the trigger signals ZA, ZB and ZC being switched on directly in the blocks 47, 50 and 53.

By applying the value 1 to the control input ON
20 of the microcontroller 1, denoted by the reference number 9 in FIG 1, the motor can be switched off at any time during the soft-starting process or during direct drive without phase-gating. In this case, all three trigger signals ZA, ZB and ZC are switched off directly
25 in blocks 45, 48 and 51 and, in the block 54, the phase-gating value of the next soft-starting process is reset to the predetermined start value for phase gating.

Since, owing to the fact that they are derived
30 directly from the voltage zeroes 10A, 10B and 10C of the phase voltages UA, UB and UC, the trigger signals ZA, ZB and ZC for the individual mains-system phases A, B and C always automatically have to follow the phase sequence dictated by the three-phase system, the
35 interrupt-controlled method proposed here for phase-gating control is independent of the rotation direction.

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A second exemplary embodiment of the invention is explained in the following text with reference to the other Figures 8, 9, 10, 11, 12, 13, 14 and 15. The phase-gating control is carried out here using two semiconductor valves 6B and 6C in the mains-system phases B and C. The three-phase power controller in this case operates with two voltage zero detection devices 3B and 3C, which are connected between the mains-system phases B and C on one side and the synthetic star point 4 on the other side, the star point 4 being linked to the mains-system phase A. The voltage zero signals U0B and U0C formed by the voltage zero detection devices 3B and 3C are in this case passed directly to interrupt inputs of the microcontroller 1. In this embodiment, the microcontroller 1 has to have at least two interrupt inputs, three port lines and two timers. The circuit for two-phase control systems for a three-phase power controller according to FIG 8 is otherwise in principle of identical design to that for the three-phase control system according to FIG 1. The two timers are required for carrying out the phase gating separately and independently in the two controlled mains-system phases B and C. In this case, a timer is permanently allocated to each of the two controlled mains-system phases B and C. The term phase-gating in this context means a defined time delay between the voltage zero of a mains-system phase B or C in the three-phase mains system and the switching-on of the semiconductor valve 6B or 6C as is denoted, for example, by 13A and 13B in the signal waveforms ZB and ZC in FIG 9.

FIG 9 shows the time waveforms of the voltages UB and UC applied to the voltage zero detection devices 3B and 3C. Of these, the voltage zero signals formed by the voltage zero detection devices 3B and 3C are denoted by U0B and U0C. Their negative flanks are denoted by 11B and 11C. This is followed by the ON signal by means of which the two-phase

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interrupt-controlled method for phase-gating control can be activated or deactivated at any time via the low-active control input 9 of the microcontroller 1. The two next wave forms show the trigger signals ZB and ZC. IA, IB and IC represent the current waveforms in the mains-system phases A, B and C.

FIG 10 shows the initialization routine of the microcontroller 1. This initialization routine covers the sequence from switching on the supply voltage for the microcontroller 1, denoted by the block 30, until an endless loop 36 is called, in which the two-phase interrupt-controlled control method proposed here is embedded. This initialization routine corresponds to that already shown in FIG 3, with the exception that, in this case, only the two trigger signals ZB and ZC that are used are set to the defined output state OFF before the interrupts which are used for the method in the microcontroller 1 are enabled.

The following description of the interrupt-controlled method for phase-gating control relates, by way of example, to the mains-system phase B. The voltage zero interrupt U0B according to FIG 11 is initiated in the microcontroller 1 by the negative flank (which is denoted by 11B in FIG 9) in the signal waveform in the voltage zero signal U0B. The flank 11B is in this case caused by the voltage zero 10B of the mains-system voltage UB. After jumping to the voltage zero interrupt routine, the "triggering" routine is called up and processed in block 37 in this routine, before the interrupt routine jumps back, via the return instruction, to the endless loop of the microcontroller 1. In the "triggering" routine according to FIG 13, once the routine has started in the block 40, the state of the control input signal ON is first of all evaluated in the block 41. If a control signal $ON = 0$ has been activated, the

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time value corresponding to a predetermined phase-gating value is first of all calculated, in the block 42, for the mains-system phase B. This time value is checked in block 43 against a minimum value, which
5 determines the time for ending the phase-gating control process, as will be explained at a later point.

In the next step in the routine, the condition $U0B = 0$ is used in the block 44 to associate the mains-system phase B with the initiating interrupt event,
10 denoted by the negative flank 11B in the voltage zero signal U0B and the voltage zero denoted by 10B in the mains-system phase B. Once this association has been made, the trigger signal ZB for the mains-system phase B is then first of all switched off in the block 46.
15 Admittedly, it is not absolutely essential to switch the trigger signal ZB at the time 12 during the first phase-gating action after activation of the method by the control input ON, since, as a result of the association in block 33, the trigger signal is in the
20 switched-off state before the first phase-gating action but, in order to simplify the software control structure, the trigger signal ZB or ZC is also switched off during the first phase-gating action.

Once the trigger signal ZB has been switched
25 off, the timer associated with the mains-system phase B is loaded, in 49, with the time value calculated in block 42 and, in the block 52, the timer is activated and the routine is then left again via the question $U0C = 0$, which cannot be satisfied at the same time.
30 Once the time value 13B, which is loaded in the timer according to FIG 9 has elapsed, this initiates an interrupt, at which point a jump is made to the timer interrupt routine illustrated in FIG 14. In this timer interrupt routine, the trigger signal ZB is switched on
35 in the block 61, as a result of which [lacuna] is triggered via the trigger device 8B and connecting line 7B of the semiconductor valve 6B in the mains-system

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phase B. This time when the trigger signal ZB is switched on is denoted by 14B in the time waveform of ZB in FIG 9. Before

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leaving the timer interrupt routine, the timer for the relevant mains-system phase is inactivated again, in the block 62.

5 The trigger signal ZB then remains switched on all the time until the next voltage zero 22 according to FIG 9. The associated switching-off of the trigger signal ZB at the time 15B in this case takes place in the "triggering" routine, which is called by the voltage zero interrupt routine U0B, immediately before
10 the relevant timer is loaded, in the block 49, with the next phase-gating value. The repetition of the described sequence results in the time waveform illustrated in FIG 9 for the trigger signal ZB of the semiconductor valve 6B.

15 This interrupt-control sequence, which has been described for the mains-system phase B, for producing phase-gating control is carried out in the same way in the mains-system phase C, with the sole difference that the voltage zero interrupt is in this case initiated by
20 a negative flank 11C in the voltage zero signal U0C, and a jump is made to the voltage zero interrupt routine U0C illustrated in FIG 12. The "triggering" routine is once again called there, in the block 37, and the already described sequence is carried out for
25 the mains-system phase C. This results in the time waveform ZC which is illustrated in FIG 9 for the trigger signal of the semiconductor valve 6C.

In the case of a phase-gating control system designed for two phases, one phase of the three-phase
30 mains system that is connected to the load is not controlled and is thus always switched on. The condition that at least two mains-system phases must be switched on at the same time for any current to flow in the main-system phases in a three-phase system without
35 a neutral conductor is thus satisfied at all times by the phase-gating control system designed for two phases.

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In contrast to the phase-gating control system designed for three phases, the problem of initial triggering thus does not arise in the case of a phase-gating control system designed for two phases, which
5 problem means that control-engineering measures always have to be adopted to ensure that two phases are always switched on at the same time in order that a current flow in the phases is possible.

In the case of the exemplary embodiment of a
10 two-phase phase-gating control system described here, the mains-system phase A of the three-phase mains system connected to the load is always switched on. Based on the sequence of mains-system phases B and C and the three-phase mains system illustrated in FIG 9,
15 the first current flow thus takes place once the semiconductor valve 6B has been switched on by the trigger signal ZB at the time 14B. This first triggering at the time 14B results in the current flow denoted by 16 in the waveform of IB in the mains-system phase B. The second triggering at the time 14C in the
20 mains-system phase C causes the current flow denoted by 17 in the waveform of IC in phase C. The resultant current flow in the uncontrolled mains-system phase A, which is denoted by 18 in the waveform of IA, is in
25 this case respectively composed of the current flow elements in the controlled mains-system phases B and C.

Owing to the inductive element of the connected motor windings, the end of the current flow in a controlled mains-system phase, for example denoted by
30 20 and 21, never takes place at the same time or at a time before the switching-off of the trigger signal for this mains-system phase, for example at the times 15B or 15C, but always with a time delay with respect to the switching-off of the trigger signal. As a result of
35 this characteristic of the current waveforms and the switching-off of the trigger signal for a semiconductor valve, whenever a voltage zero occurs in a mains-system phase, double or multiple triggering within one phase

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half-cycle, which is denoted for example by the start time 10B and the end time 22 in the waveform of the phase voltage UB,

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can virtually be precluded. The duration of the time delay of the current flow end with respect to the switching-off of the trigger signal is in this case dependent on the inductive element of the motor winding, which varies dynamically while the connected motor is accelerating from rest to the rated speed.

By calculating the phase-gating values in the two controlled mains-system phases using functions with different profiles, it is possible to influence the imbalance in the current waveforms of the three mains-system phases caused by the two-phase phase-gating control system.

The described sequence of two-phase interrupt-controlled phase-gating control is in each case repeated, as in the case of three-phase control, with phase-gating values in each case reduced by predetermined step widths, until one of the two time values which correspond to the phase-gating values falls below a permanently predetermined minimum value. The motor 2, two phases of which are driven via the semiconductor valves 6A and 6B, in this case accelerates softly from rest to the rated speed, in which case it is possible to vary the soft starting time of the motor via the choice of the step widths for the reduction of the phase-gating values. After reaching the permanently predetermined minimum value for phase gating, which is chosen such that the connected motor 2 has undoubtedly accelerated by the time this minimum value is reached, the two semiconductor valves 6A and 6B are driven without phase gating, by directly switching on the trigger signals ZB and ZC in the blocks 50 and 53.

By applying the value 1 to the control input ON of the microcontroller 1, the motor 2 can be switched off at any time during the soft starting or during direct drive without phase gating. The two trigger signals ZB and ZC

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are in this case switched off directly by the blocks 48 and 51 and, in the block 54, the phase-gating values for the next soft starting process are reset to the predetermined start values for phase gating.

Since, owing to the fact that the trigger signals are derived directly from the voltage zeroes 10B and 10C of the two controlled mains-system phases of the three-phase mains system, the trigger signals of the two controlled mains-system phases always automatically have to follow the predetermined phase sequence, the interrupt-controlled method proposed here for two-phase phase-gating control of a three-phase power controller operates independently of the rotation direction.

Although the present invention has been explained with reference to the embodiments illustrated in the attached FIGs 1 to 15, it should be remembered that this is not intended to limit the invention just to the illustrated embodiments, but to include all possible changes, modifications and equivalent arrangements to the extent that they are covered by the content of the patent claims.

Patent Claims

1. A three-phase power controller for controlling a load (2) which is connected to a three-phase mains system, having a microcontroller (1), having voltage detection devices (3A, 3B, 3C) which produce voltage zero signals (U0A, U0B, U0C) which are associated with the voltage zeroes (10A, 10B, 10C) in the individual mains-system phases (A, B, C), from which signals the microcontroller (1) derives trigger signals (ZA, ZB, ZC) for driving phase-related semiconductor valves (6A, 6B, 6C), characterized in that the voltage zero signals (U0A, U0B, U0C) are square-wave signals whose flanks (11, 11B, 11C) are used for interrupt control of an executive program in the microcontroller (1), the interrupt routines which are associated with the interrupt control in the executive program controlling the switch-on times of the trigger signals (ZA, ZB, ZC) exclusively on the basis of the voltage zeroes (10A, 10B, 10C) as information about the three-phase mains system, and the trigger signals (ZA, ZB, ZC) always being switched off directly after each voltage zero (10A, 10B or 10C).
2. The three-phase power controller as claimed in claim 1, characterized in that only two voltage detection devices (3B, 3C) are provided which produce, as voltage zero signals of two mains-system phases (B, C), square-wave signals (U0B, U0C) whose flanks (11B, 11C) are used for interrupt control by the microcontroller (1).
3. The three-phase power controller as claimed in claim 1, characterized in that a common interrupt signal (SI), which is formed from the square-wave signals (U0A, U0B, U0C) in a logic device (5), is supplied to the microcontroller (1) for interrupt control.

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4. The three-phase power controller as claimed in one of the preceding claims, characterized in that the interrupt control includes a "voltage zero interrupt" interrupt routine, in which a timer is loaded with a time value and is activated, and in that once the time value in a relevant timer interrupt routine has elapsed, the associated semiconductor valve is triggered (61).
5. The three-phase power controller as claimed in one of the preceding claims, characterized in that the trigger signal (ZA, ZB or ZC) is switched off in the voltage zero interrupt routine before the loading of the timer.
6. The three-phase power controller as claimed in one of the preceding claims, characterized in that the timer is deactivated (62) in the time interrupt routine.
7. The three-phase power controller as claimed in one of the preceding claims, characterized in that the voltage zero interrupt routine produces an association between one flank (11) of the common interrupt signal (SI) and one of the voltage zero signals (U0A, U0B, U0C).
8. A method for phase-gating the control of a three-phase power controller for controlling a three-phase load (2) which is connected to a three-phase mains system, having a microcontroller (1), having voltage detection devices (3A, 3B, 3C) which produce voltage zero signals (U0A, U0B, U0C) which are associated with the voltage zeroes (10A, 10B, 10C) in the individual mains-system phases (A, B, C), from which signals the microcontroller (1) derives trigger signals (ZA, ZB, ZC) for driving phase-related semiconductor valves (6A, 6B, 6C), characterized in that the voltage zero detection devices (3A, 3B, 3C) produce square-wave

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voltage zero signals (U0A, U0B, U0C), which are combined via a logic device (5) to form a common interrupt signal (SI) in that a jump is made to an interrupt routine either on each negative flank or on each positive flank in the common interrupt signal (SI), in which interrupt routine the triggering voltage zero (10A, 10B or 10C) is first of all assigned one of the mains-system phases (A, B or C), and a timer-interrupt-controlled sequence is then initiated for the associated mains-system phase, in order to produce a trigger signal (ZA, ZB, ZC) for the semiconductor valve (6A, 6B, 6C) for the relevant mains-system phase.

Herstonhaugh & Co
Ottawa, Canada
Patent Agents

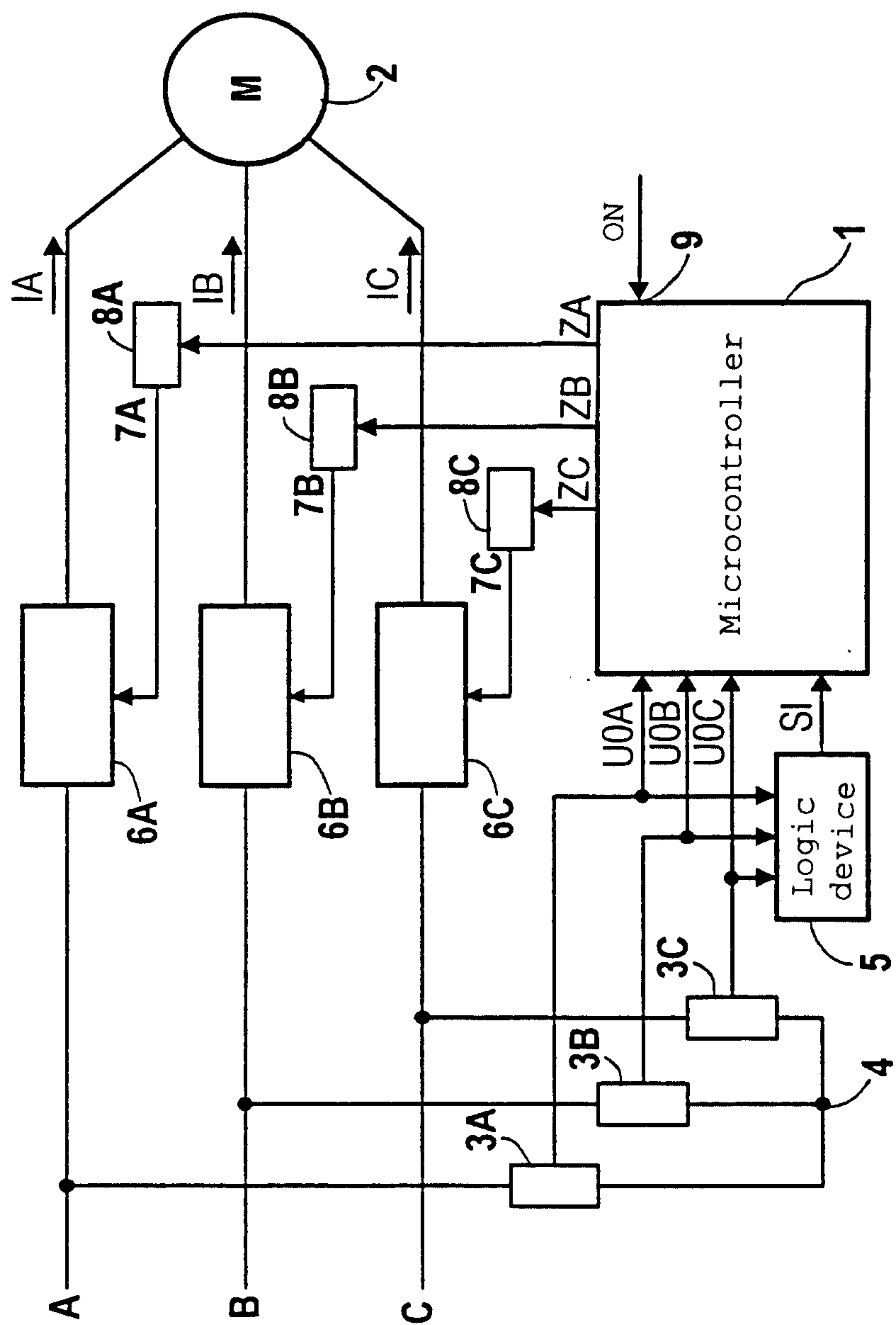


FIG 1

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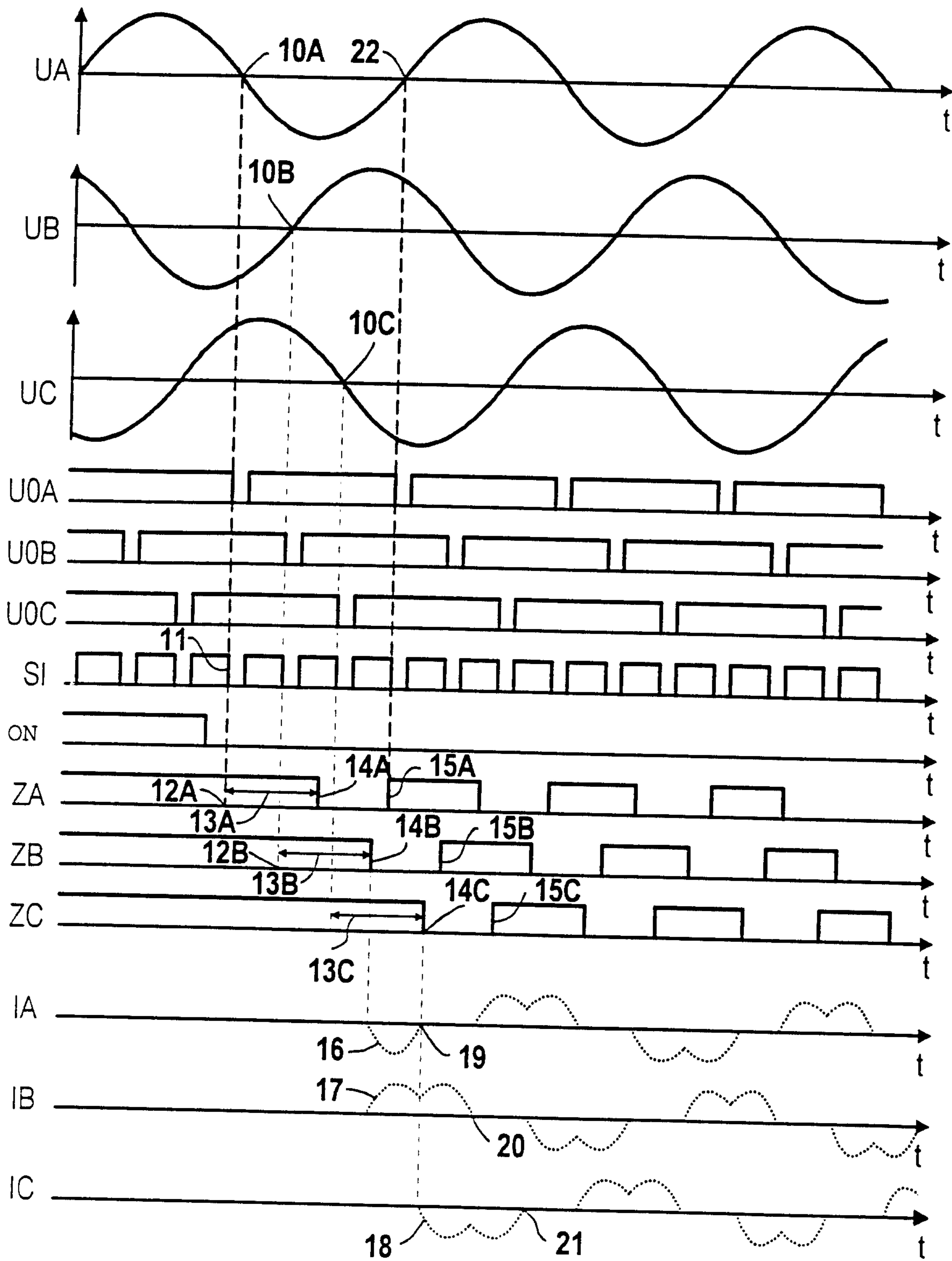


FIG 2

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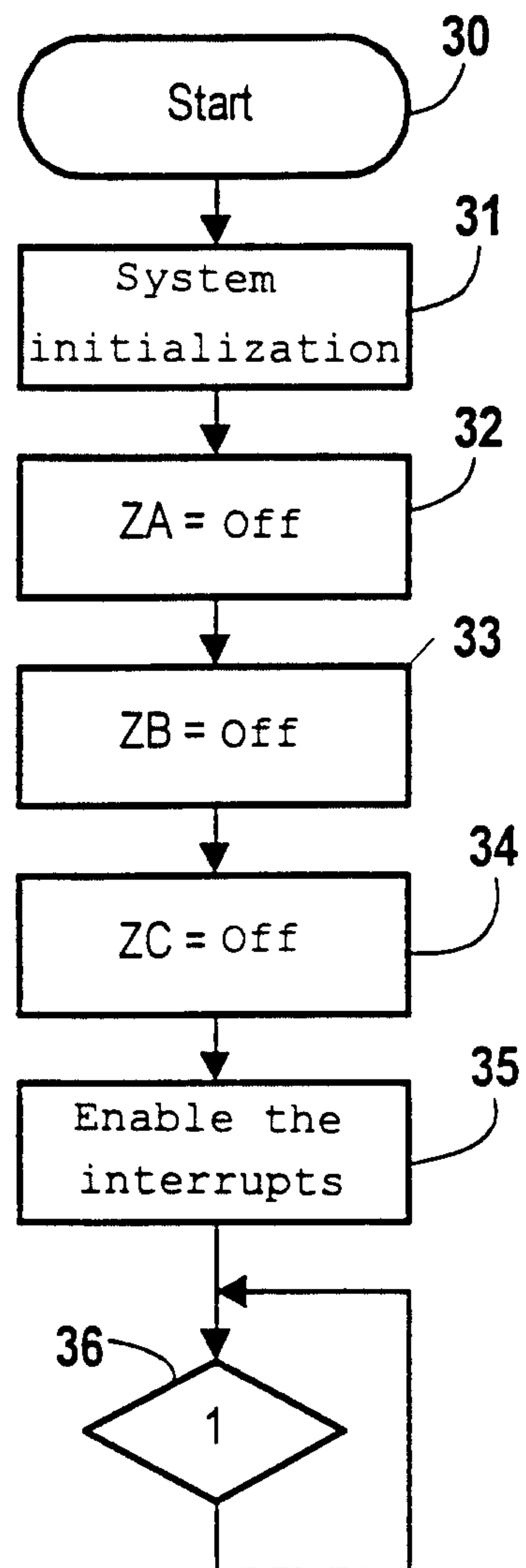


FIG 3

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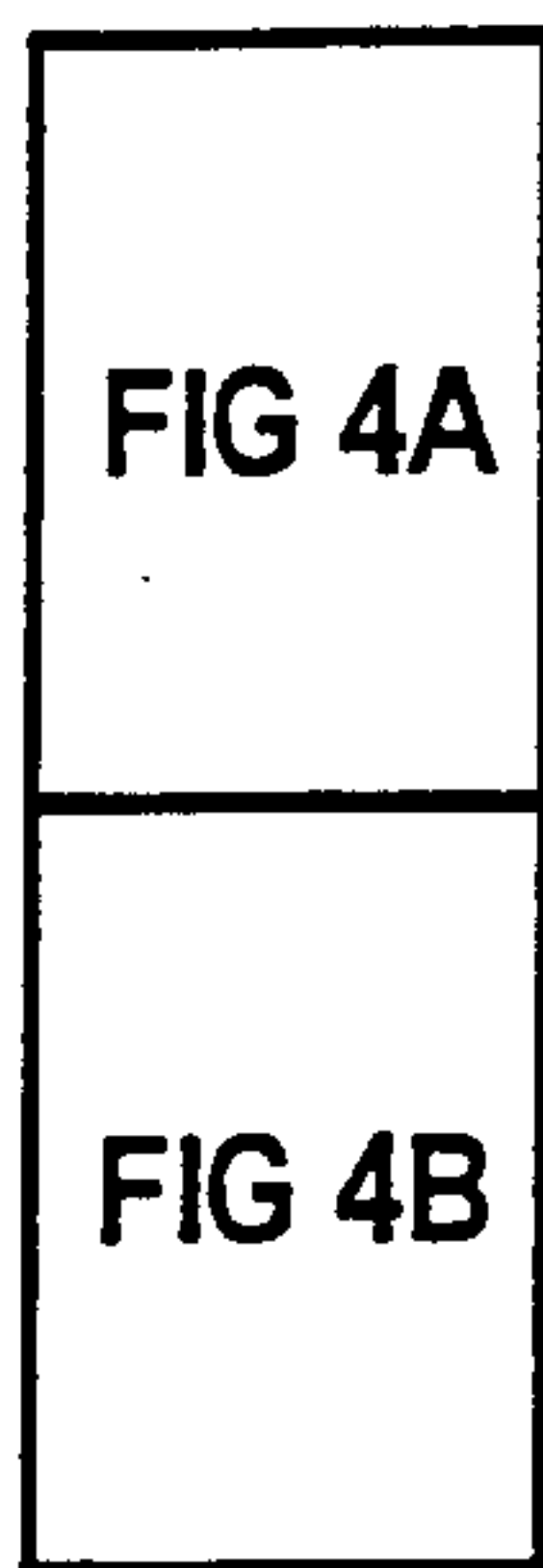


FIG 4

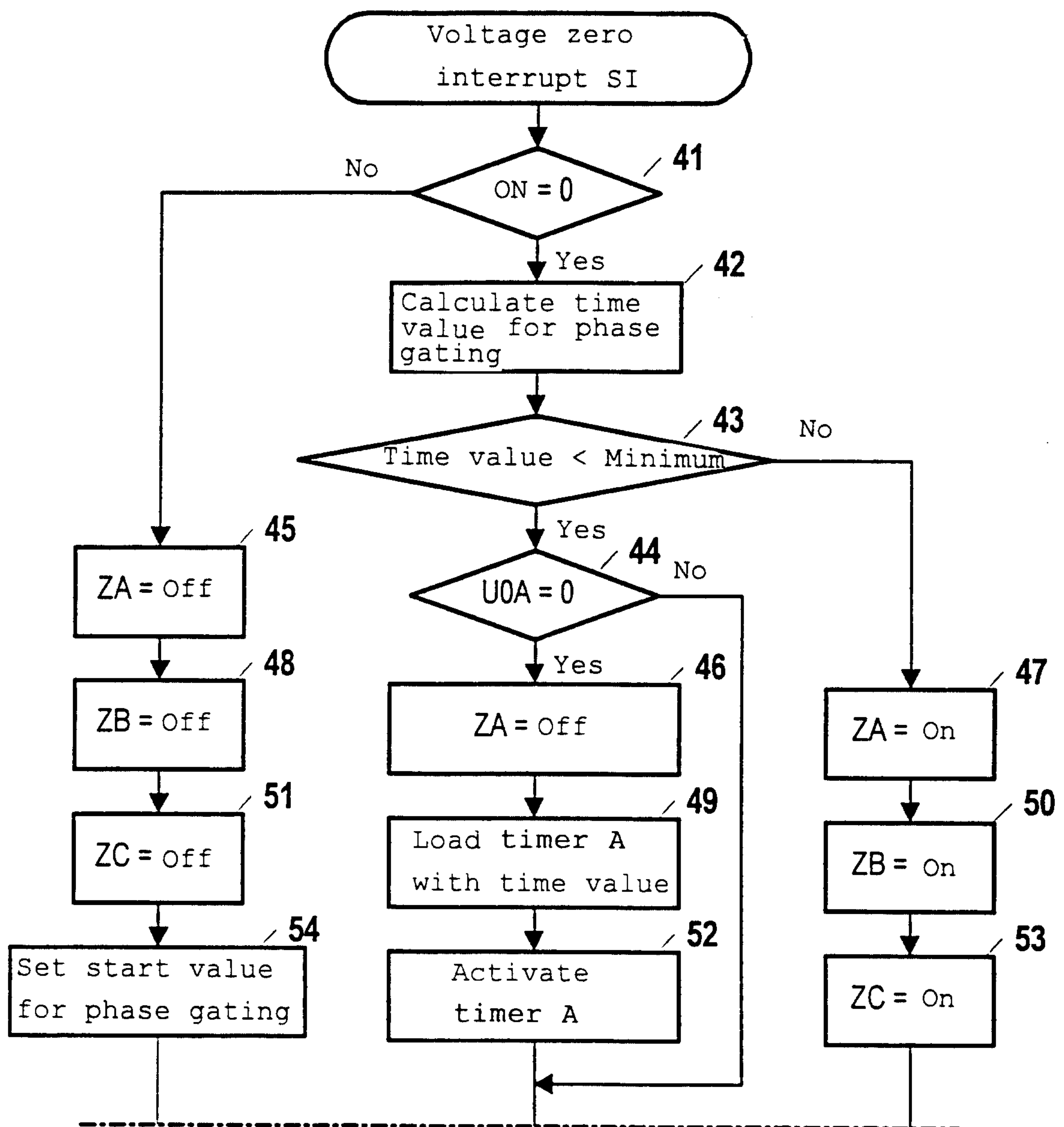


FIG 4A

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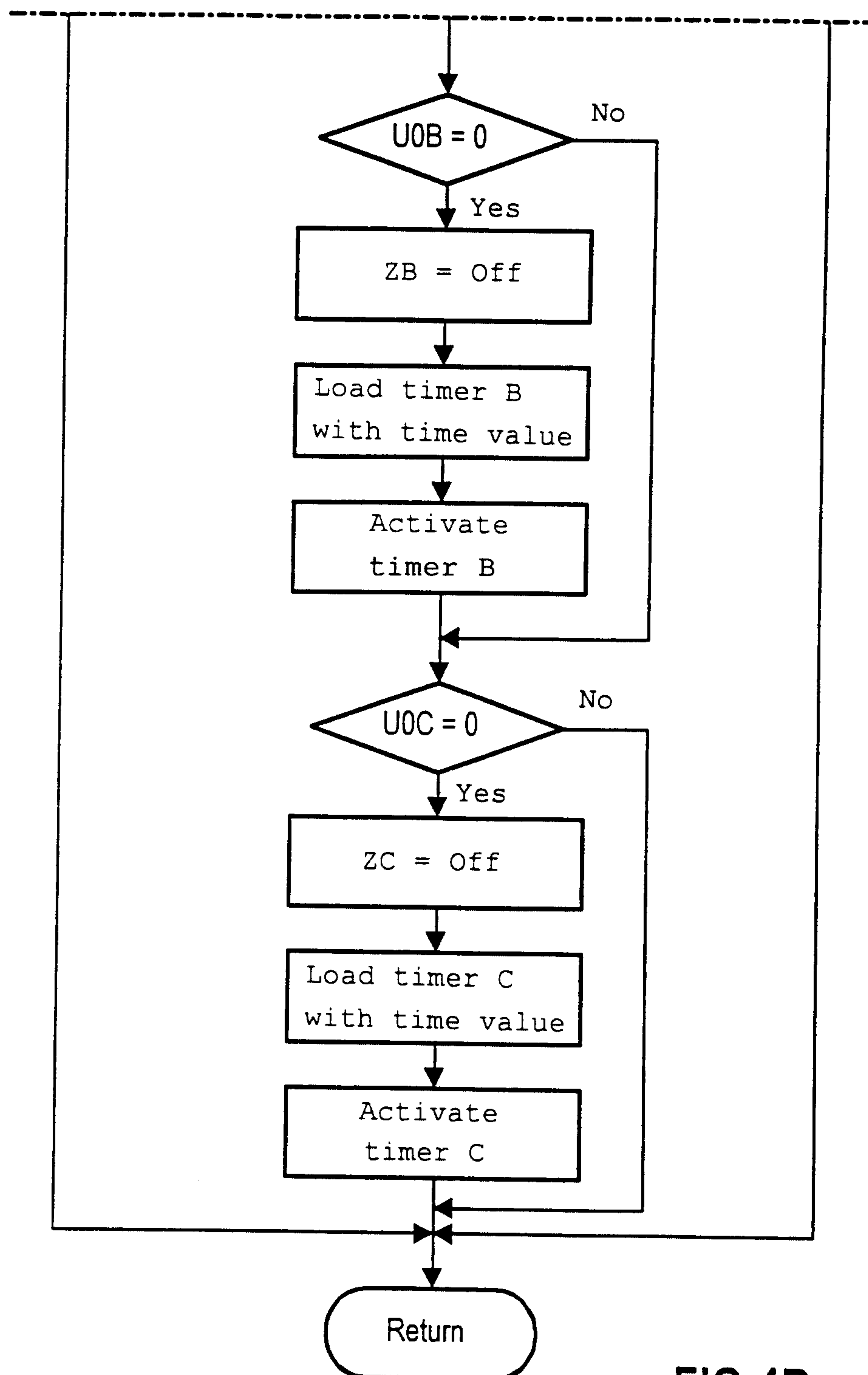


FIG 4B

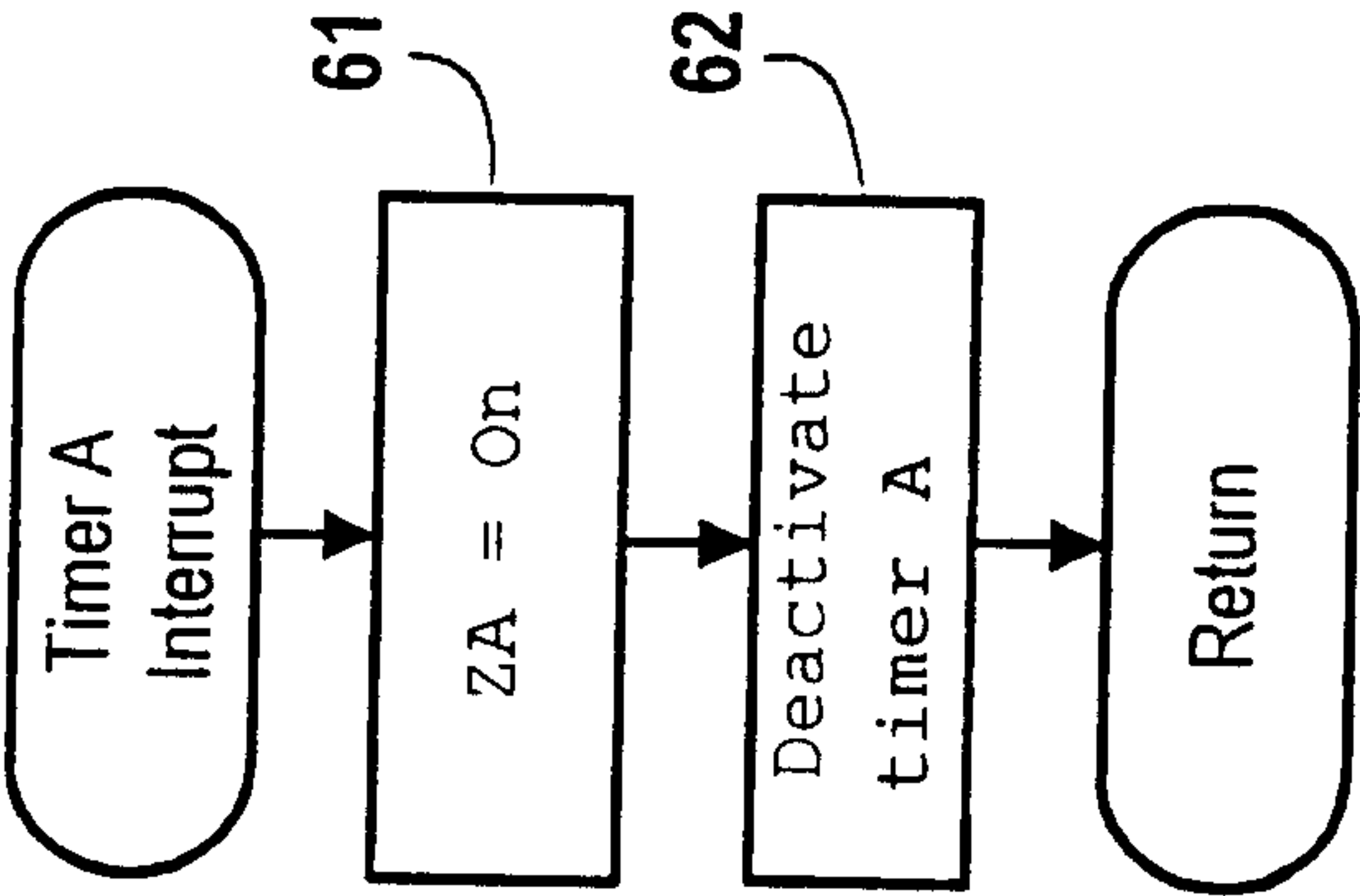


FIG 5

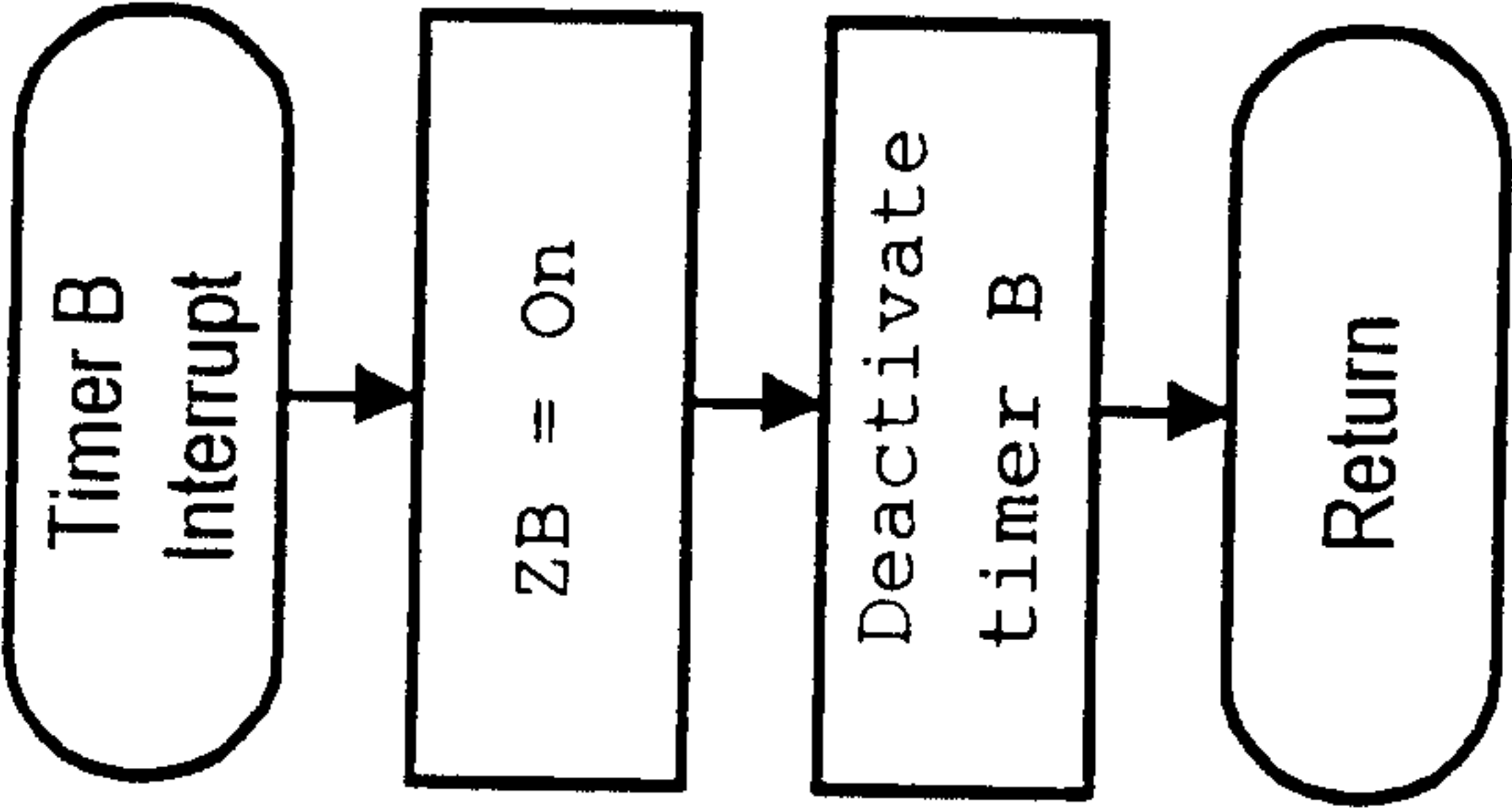


FIG 6

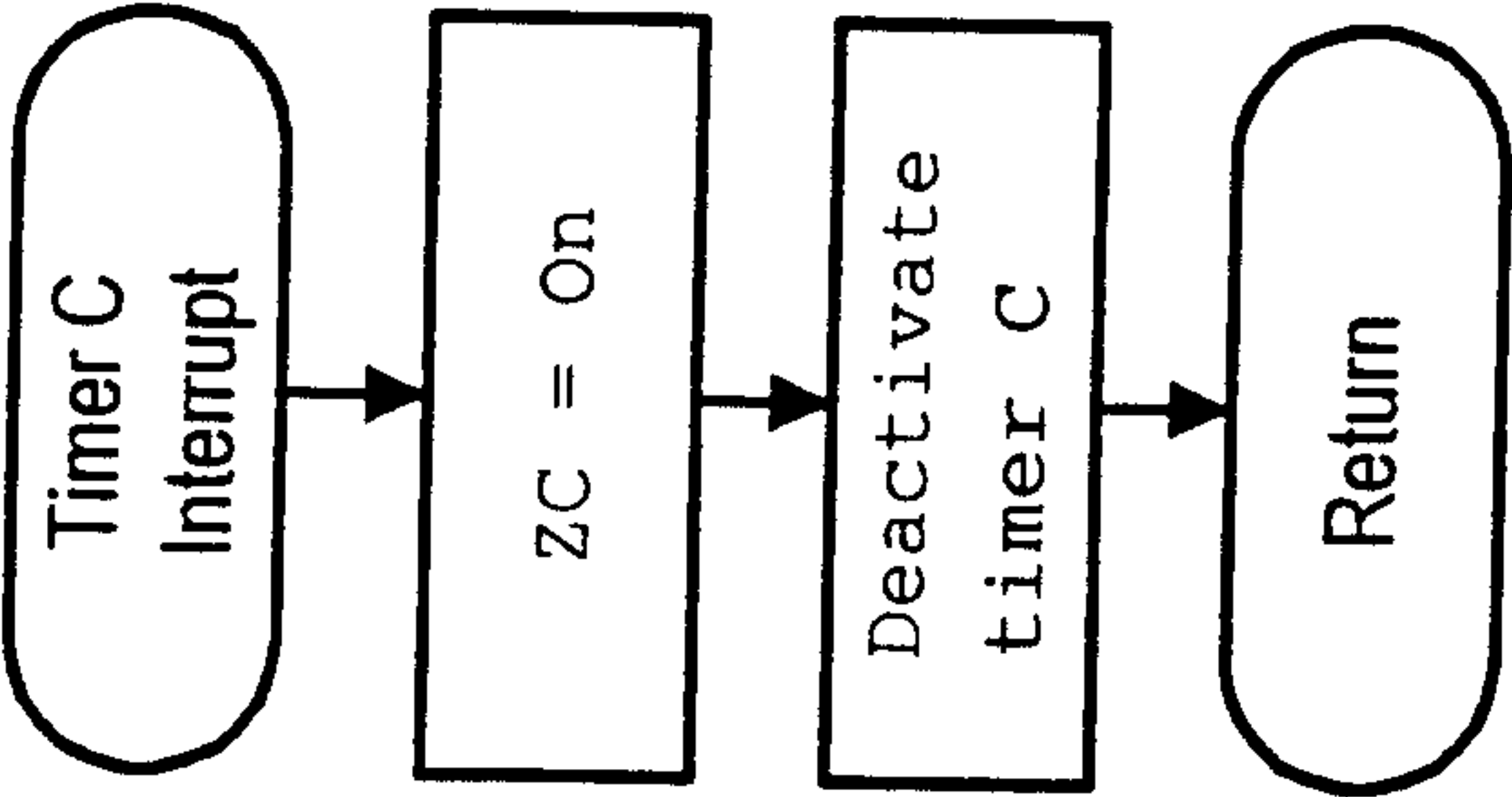


FIG 7

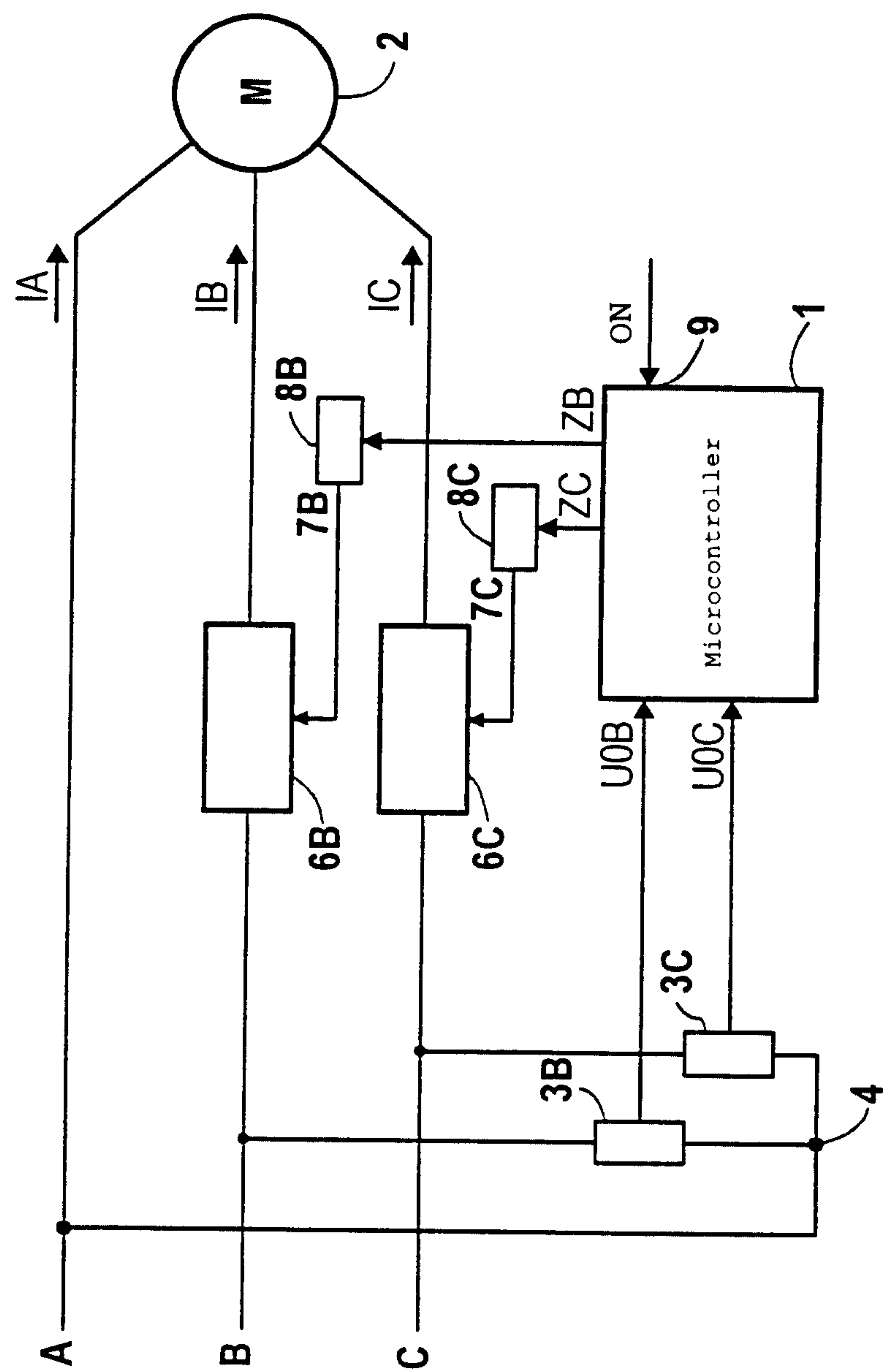


FIG 8

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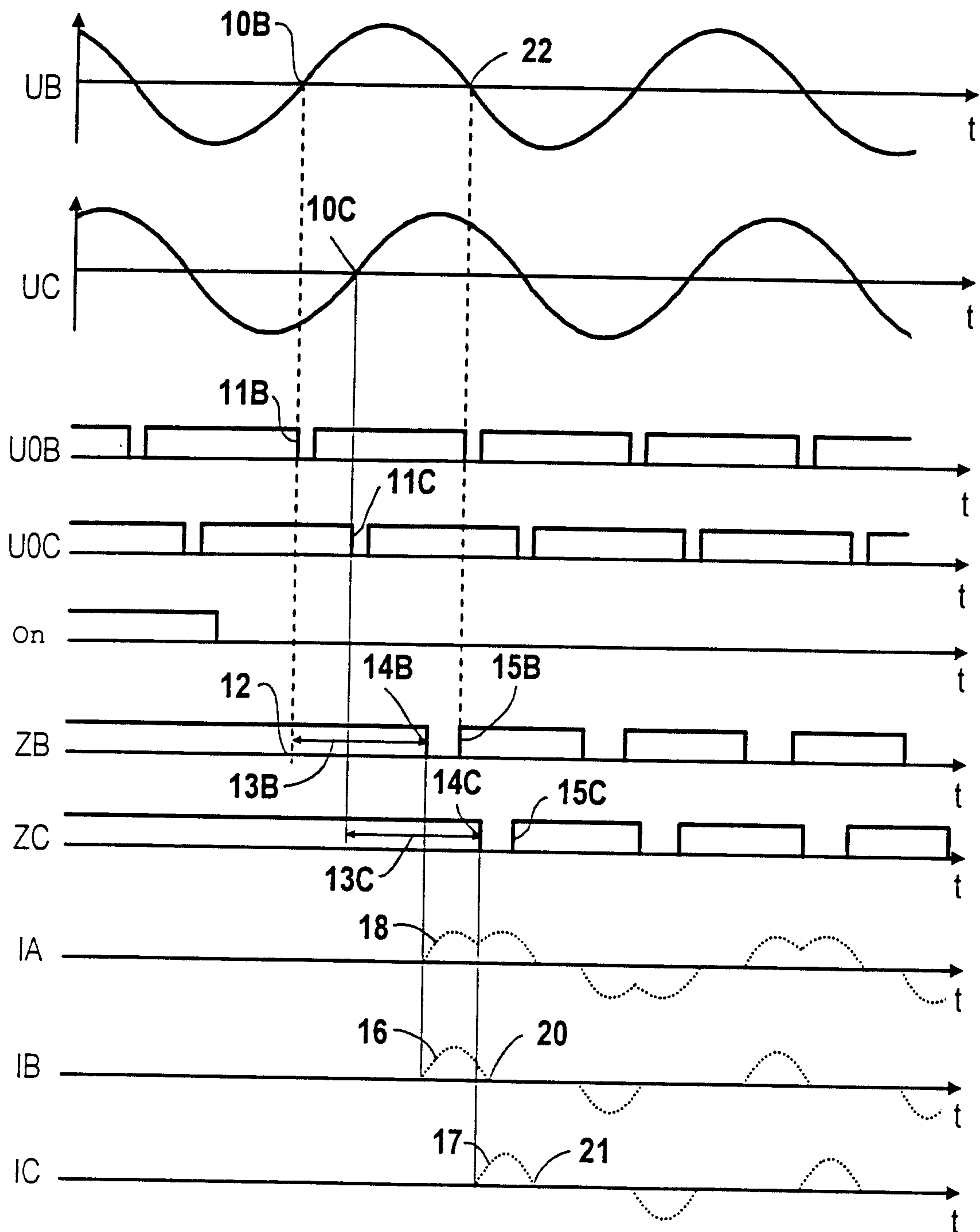


FIG 9

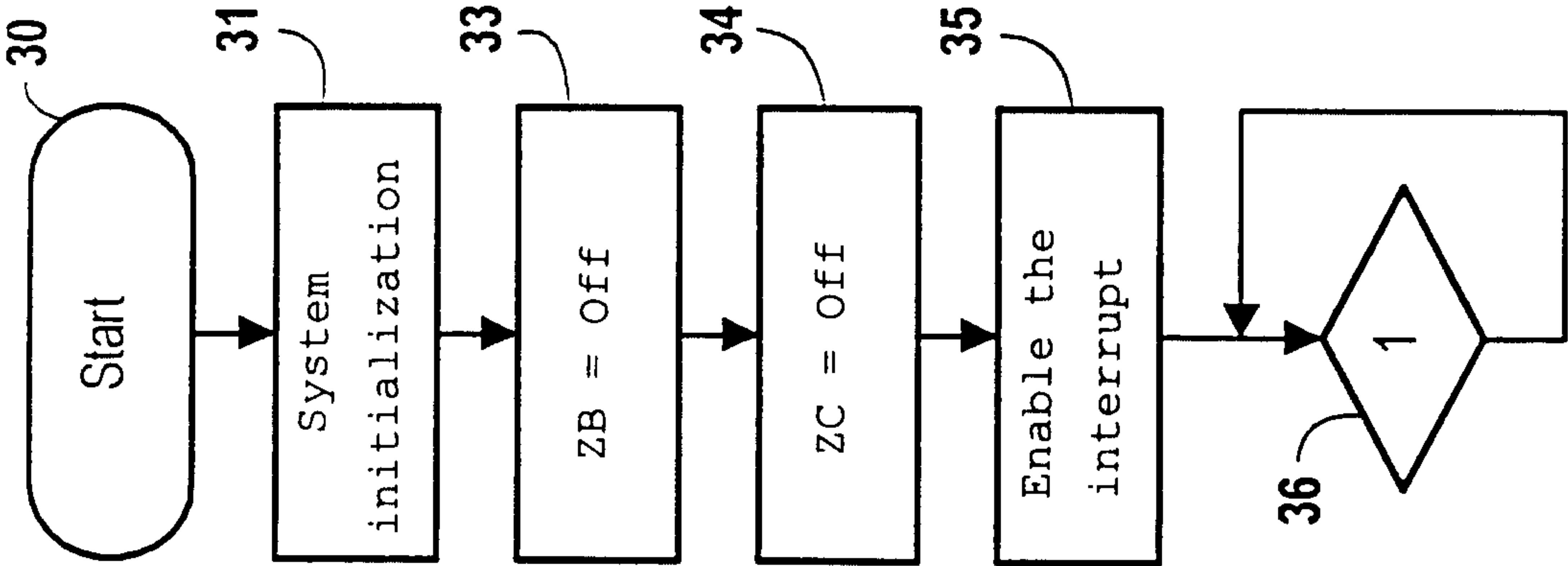


FIG 10

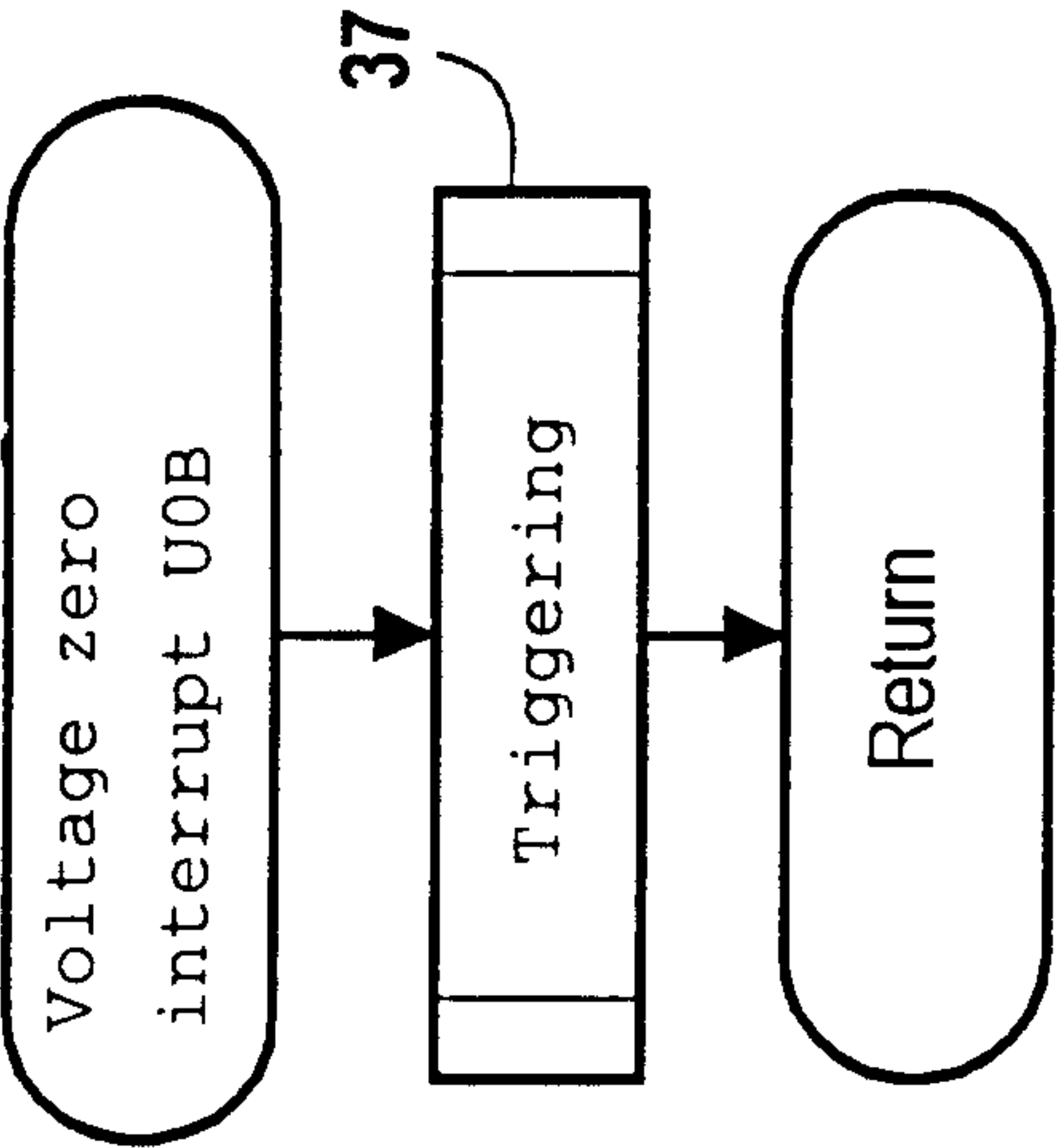


FIG 11

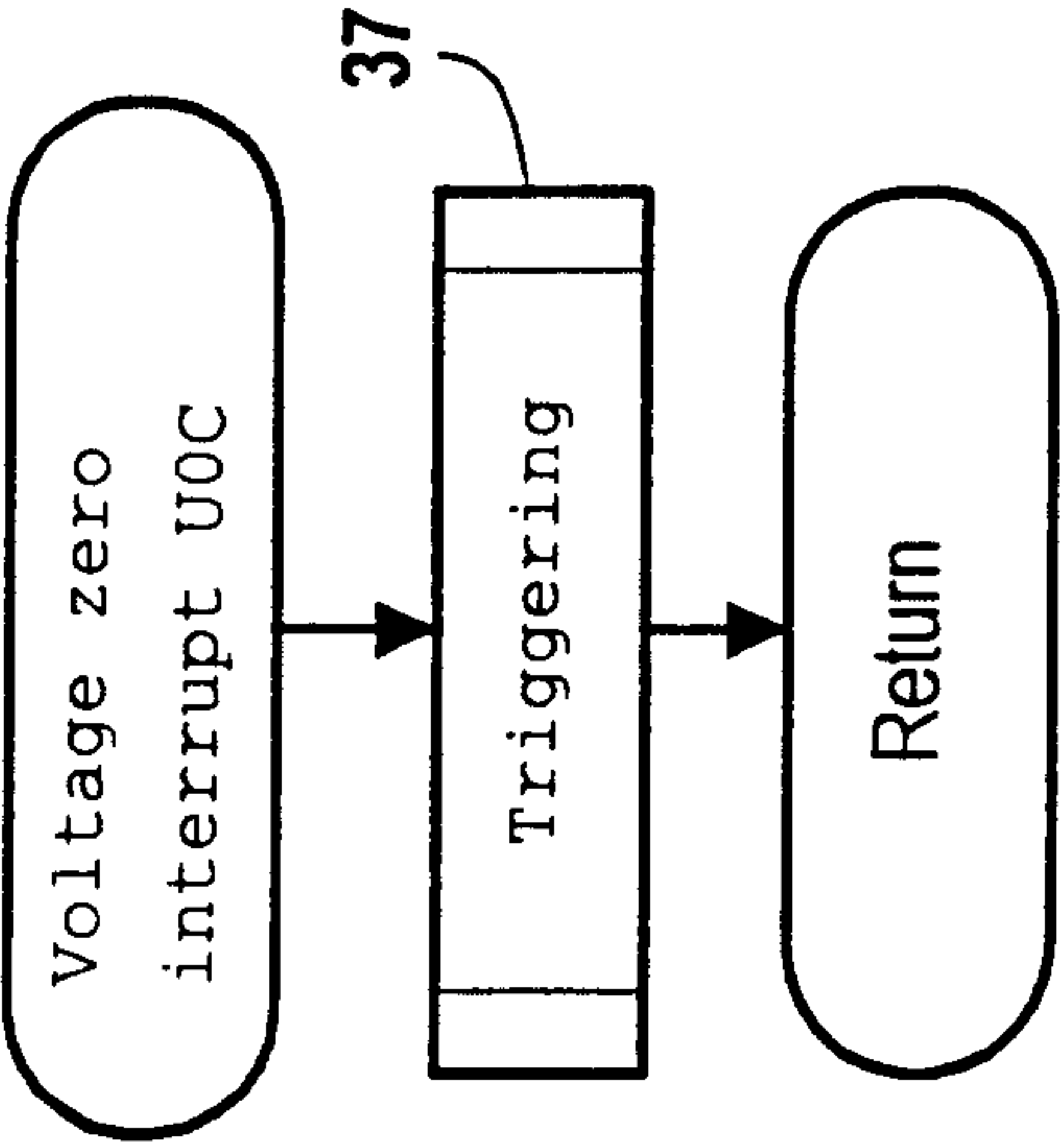


FIG 12

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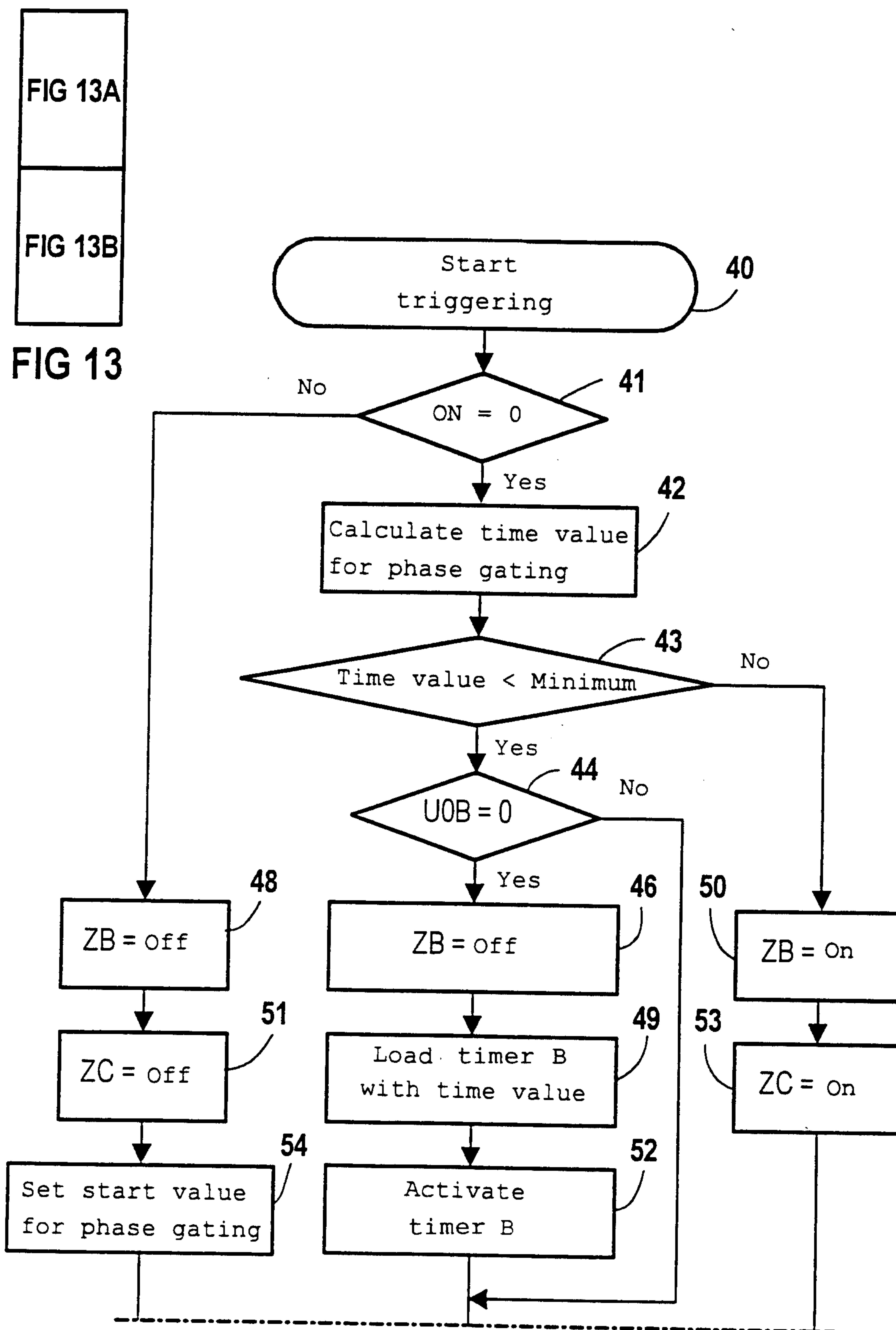


FIG 13A

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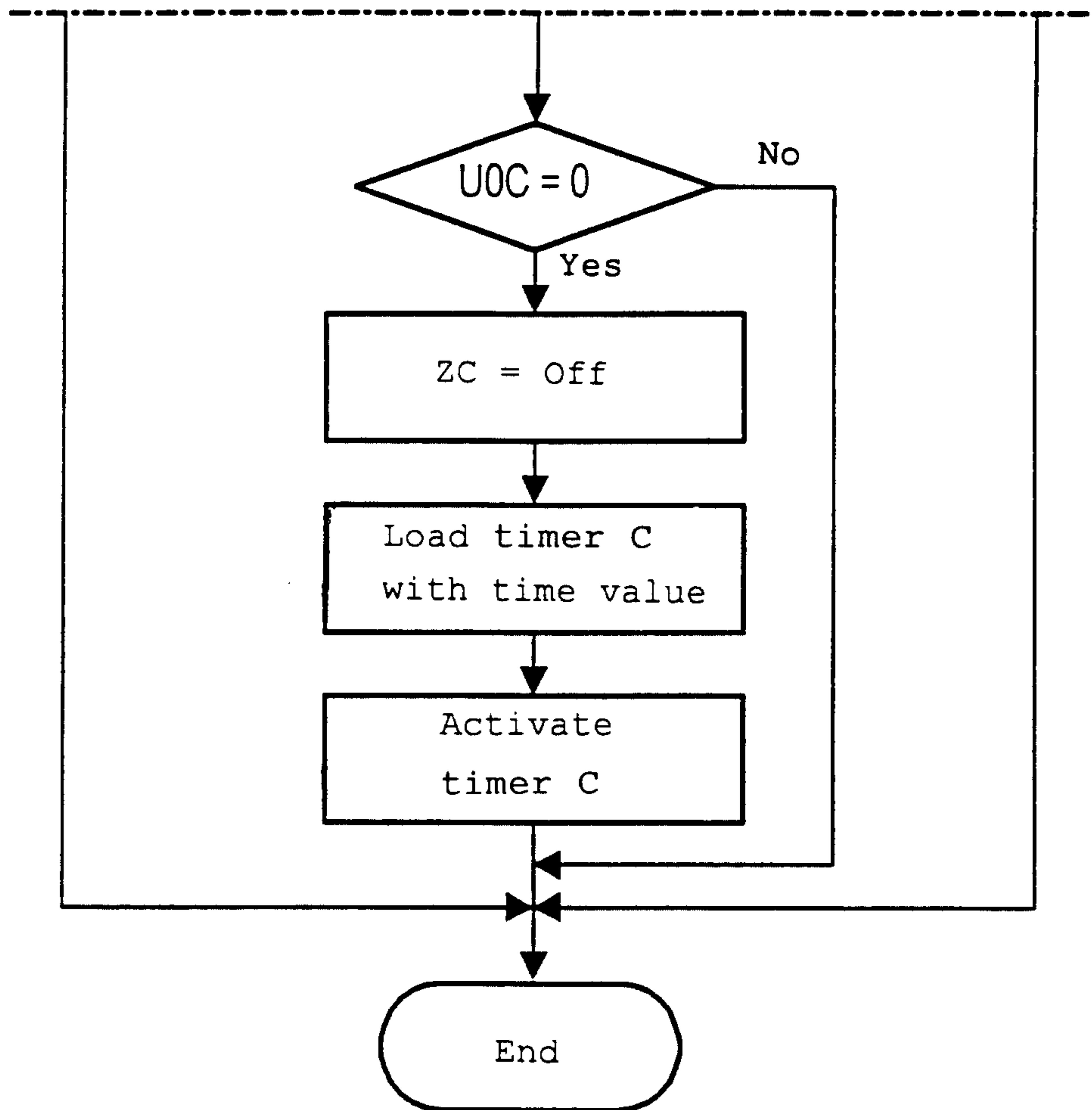


FIG 13B

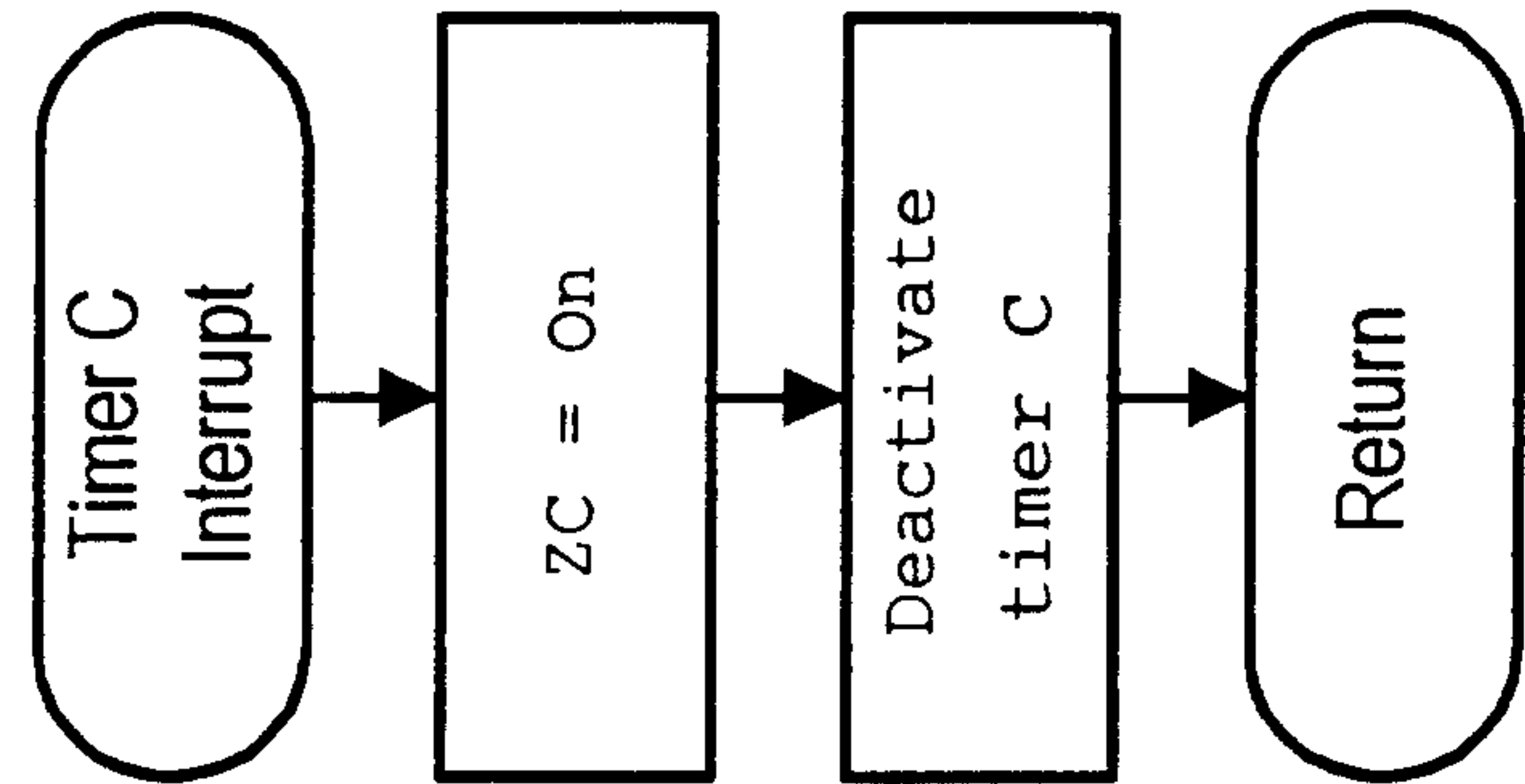


FIG 15

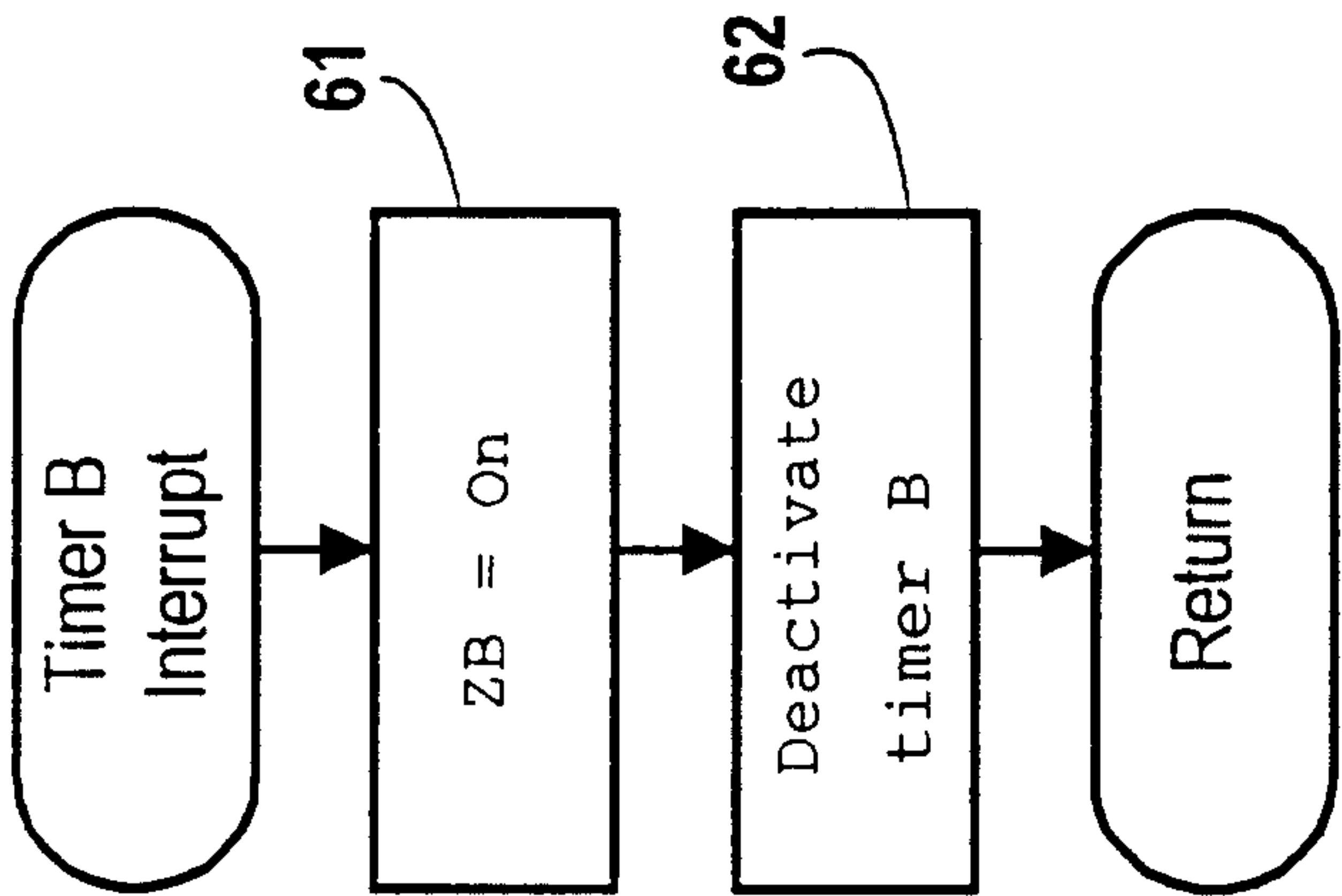


FIG 14

