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(54) Title: ECCENTRIC INCIDENT LUMINANCE PUPIL TRACKING

(57) Abstract: In one embodiment, an electronic assembly includes a flexible circuit board formed into a curved shape that is configured to be substantially concentric with a viewer's eye. The electronic assembly further includes a plurality of facets coupled to a side of curved shape of the flexible circuit board that is configured to face the viewer's eye. Each facet has a planar face, one or more emitters configured to emit light towards the viewer's eye, and one or more receptors configured to detect the emitted light after it has been reflected back towards the electronic assembly from a retina of the viewer's eye. Each face is normal to a line pointing towards a center area of the viewer's eye when the curved shape is substantially concentric with the viewer's eye. Each facet is individually addressable such that the plurality of facets are configurable to detect a center of gaze of the viewer.

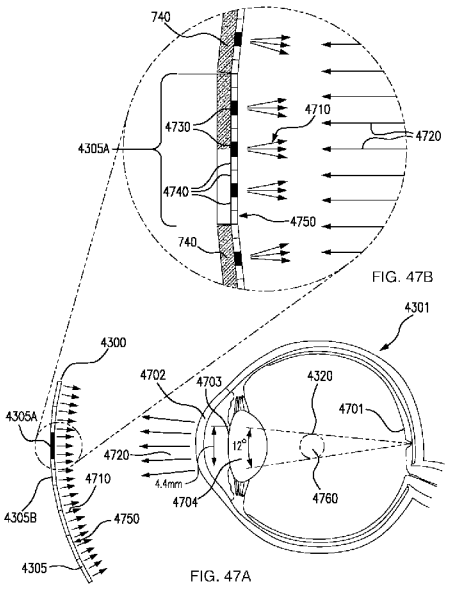

FIG. 47B

FIG. 47A

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ECCENTRIC INCIDENT LUMINANCE PUPIL TRACKING

TECHNICAL FIELD

[1] This disclosure relates generally to light field displays and cameras, and more particularly to eccentric incident luminance pupil tracking systems and methods.

BACKGROUND

[2] Electronic displays are utilized in a variety of applications. For example, displays are used in smartphones, laptop computers, and digital cameras. Some devices, such as smartphones and digital cameras, may include an image sensor in addition to an electronic display. While some cameras and electronic displays separately capture and reproduce light fields, light field displays and light field cameras are generally not integrated with one another.

SUMMARY OF PARTICULAR EMBODIMENTS

[3] In one embodiment, an electronic assembly includes a flexible circuit board formed into a curved shape that is configured to be substantially concentric with a viewer's eye. The electronic assembly further includes a plurality of facets coupled to a side of curved shape of the flexible circuit board that is configured to face the viewer's eye. Each facet has a planar face, one or more emitters configured to emit light towards the viewer's eye, and one or more receptors configured to detect the emitted light after it has been reflected back towards the electronic assembly from a retina of the viewer's eye. Each face is normal to a line pointing towards a center area of the viewer's eye when the curved shape is substantially concentric with the viewer's eye. Each facet is individually addressable such that the plurality of facets are configurable to detect a center of gaze of the viewer.

[4] The present disclosure presents several technical advantages. Some embodiments provide a complete and accurate recreation of a target light field while remaining lightweight and comfortable to wear for a user. Some embodiments provide a thin electronic system which offers both opacity and controllable unidirectional emulated transparency, as well as digital display capabilities such as virtual reality (VR), augmented reality (AR), and mixed reality (MR). Some embodiments provide a direct sensor-to-display system that utilizes a direct association of input pixels to corollary output pixels to circumvent the need for image transformation. This reduces the complexity, cost, and power requirements for some systems. Some embodiments provide in-layer signal processing configurations that provide for local, distributed processing of large quantities of data (e.g., 160k of image data

or more), thereby circumventing bottlenecks as well as performance, power, and transmission line issues associated with existing solutions. Some embodiments utilize microlens layers with arrays of plenoptic cells to accurately capture and display a volume of light to a viewer. The plenoptic cells include opaque cell walls to eliminate optical cross-talk between cells, thereby improving the accuracy of the replicated light field.

[5] Some embodiments provide three-dimensional electronics by geodesic faceting. In such embodiments, a flexible circuit board with an array of small, rigid surfaces (e.g., display and/or sensor facets) may be formed into any 3D shape, which is especially useful to accommodate the narrow radii of curvature (e.g., 30-60 mm) necessary for head-mounted near-eye wrapped displays. Some embodiments provide distributed multi-screen arrays for high density displays. In such embodiments, an array of small, high-resolution micro displays (e.g., display facets) of custom sizes and shapes are formed and then assembled on a larger, flexible circuit board that may then be formed into a 3D shape (e.g., a semispherical surface). Each micro display may act independently of any other display, thereby providing a large array of many high-resolution displays with unique content on each, such that the whole assembly together forms essentially a single extremely high-resolution display. Some embodiments provide a distributed multi-aperture camera array. Such embodiments provide an array of small image sensors (e.g., sensor facets) of custom sizes and shapes, all of which are assembled on a larger, flexible circuit board that is then formed to a 3D (e.g., semi-spherical) shape. Each discrete image sensor may act independently of any other image sensor in order to provide a large array of many apertures capturing unique content on each, such that the whole assembly

essentially becomes a seamless, very high resolution, multi-node camera.

[6] Some embodiments utilize tracking surfaces to track a viewer's eye and to determine a center of gaze of the user. In some embodiments, the tracking surfaces are ocular-centric (i.e., have curved shapes that are substantially concentric with an eye of the viewer). In other embodiments, the tracking surfaces are not ocular-centric. The tracking surfaces may include IR emitters to emit IR light into the viewer's eye and IR detectors to detect a cone of retro-reflected IR light from the viewer's eye (e.g.. from the retina or other portion of the eye). In some embodiments, the IR emitters and detectors are embedded within display pixels of display facets of a near-eye wrapped display.

[7] Other technical advantages will be readily apparent to one skilled in the art from FIGURES 1A through 42, their descriptions, and the claims. Moreover, while specific advantages have been enumerated above, various embodiments may include all, some, or none of the enumerated advantages.

BRIEF DESCRIPTION OF THE DRAWINGS

[8] For a more complete understanding of the present disclosure and its advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

[9] FIGURES 1A-1C illustrate a reference scene with various three-dimensional (3D) objects and various viewing positions, according to certain embodiments;

[10] FIGURES 2A-2C illustrate viewing the 3D objects of FIGURES 1A-1C through a transparent panel, according to certain embodiments;

[11] FIGURES 3A-3C illustrate viewing the 3D objects of FIGURES 1A-1C through a camera image panel, according to certain embodiments;

[12] FIGURES 4A-4C illustrate viewing the 3D objects of FIGURES 1A-1C through an emulated-transparency electronic panel, according to certain embodiments;

[13] FIGURES 5A-5C illustrate viewing the 3D objects of FIGURES 1A-1C through the camera image panel of FIGURES 3A-3C from an alternate angle, according to certain embodiments;

[14] FIGURES 6A-6C illustrate viewing the 3D objects of FIGURES 1A-1C through the emulated-transparency electronic panel of FIGURES 4A-4C from an alternate angle, according to certain embodiments;

[15] FIGURE 7 illustrates a cut-away view of an emulated transparency assembly, according to certain embodiments;

[16] FIGURE 8 illustrates an exploded view of the emulated transparency assembly of FIGURE 7, according to certain embodiments;

[17] FIGURE 9 illustrates a method of manufacturing the emulated transparency assembly of FIGURE 7, according to certain embodiments;

[18] FIGURE 10 illustrates a direct sensor-to-display system that may be used by the emulated transparency assembly of FIGURE 7, according to certain embodiments;

[19] FIGURE 11 illustrates a method of manufacturing the direct sensor-to-display system of FIGURE 10, according to certain embodiments;

[20] FIGURES 12-13 illustrate various in-layer signal processing configurations that may be used by the emulated transparency assembly of FIGURE 7, according to certain embodiments;

[21] FIGURE 14 illustrates a method of manufacturing the in-layer signal processing systems of FIGURES 12-13, according to certain embodiments;

[22] FIGURE 15 illustrates a plenoptic cell assembly that may be used by the emulated transparency assembly of FIGURE 7, according to certain embodiments;

[23] FIGURE 16 illustrates a cross section of a portion of the plenoptic cell assembly of FIGURE 15, according to certain embodiments;

[24] FIGURES 17A-17C illustrate cross sections of a portion of the plenoptic cell assembly of FIGURE 15 with various incoming fields of light, according to certain embodiments;

[25] FIGURES 18A-18B illustrate a method of manufacturing the plenoptic cell assembly of FIGURE 15, according to certain embodiments;

[26] FIGURES 19A-19B illustrate another method of manufacturing the plenoptic cell assembly of FIGURE 15, according to certain embodiments;

[27] FIGURES 20-21 illustrate a plenoptic cell assembly that may be manufactured by the methods of FIGURES 18A-19B, according to certain embodiments;

[28] FIGURE 22 illustrates a flexible circuit board that may be used by the emulated transparency assembly of FIGURE 7, according to certain embodiments;

[29] FIGURE 23 illustrates additional details of the flexible circuit board of FIGURE 22, according to certain embodiments;

[30] FIGURE 24 illustrates a data flow through the flexible circuit board of FIGURE 22, according to certain embodiments;

[31] FIGURE 25 illustrates a method of manufacturing an electronic assembly using the flexible circuit board of FIGURE 22, according to certain embodiments;

[32] FIGURE 26 illustrates a cut-away view of a curved multi-display array, according to certain embodiments;

[33] FIGURE 27 illustrates an exploded view of the curved multi-display array of FIGURE 26, according to certain embodiments;

[34] FIGURES 28-29 illustrate logic facets and display facets of the curved multi-display array of FIGURE 26, according to certain embodiments;

[35] FIGURE 30 illustrates a back side of the flexible circuit board of FIGURE 22, according to certain embodiments;

[36] FIGURE 31 illustrates a data flow through the flexible circuit board of FIGURE 30, according to certain embodiments;

[37] FIGURE 32 illustrates the flexible circuit board of FIGURE 30 that has been formed into a semispherical shape, according to certain embodiments;

[38] FIGURE 33 illustrates a data flow through the flexible circuit board of FIGURE 32, according to certain embodiments;

[39] FIGURE 34 illustrates an array of logic facets that have been formed into a semispherical shape, according to certain embodiments;

[40] FIGURE 35 illustrates communications between the logic facets of FIGURE 34, according to certain embodiments;

[41] FIGURE 36 illustrates a method of manufacturing the curved multi-display array of FIGURE 26, according to certain embodiments;

[42] FIGURE 37 illustrates a cut-away view of a curved multi-camera array, according to certain embodiments;

[43] FIGURES 38-39 illustrate exploded views of the curved multi-camera array of FIGURE 37, according to certain embodiments;

[44] FIGURE 40 illustrates a back view of the flexible circuit board of FIGURE 32, according to certain embodiments;

[45] FIGURE 41 illustrates a data flow through the flexible circuit board of FIGURE 40, according to certain embodiments;

[46] FIGURE 42 illustrates a method of manufacturing the curved multi-camera array of FIGURE 37, according to certain embodiments;

[47] FIGURES 43-46 illustrate perspective views of a near-eye pupil-tracking surface, according to certain embodiments;

[48] FIGURES 47A-47B illustrate cross-sectional views of the near-eye pupil-tracking surface of FIGURES 43-46, according to certain embodiments;

[49] FIGURES 48A-48B illustrate cones of retinal retro-reflected light as detected by an ocular-concentric tracking surface, according to certain embodiments;

[50] FIGURES 49A-49B illustrate cones of retinal retro-reflected light as detected by a non-ocular-concentric tracking surface, according to certain embodiments;

[51] FIGURES 50A-50B illustrate cones of retinal retro-reflected light as detected by a flat tracking surface, according to certain embodiments; and

[52] FIGURE 51 illustrates a method of manufacturing the near-eye pupil-tracking surface of FIGURE 43, according to certain embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[53] Electronic displays are utilized in a variety of applications. For example, displays are used in smartphones, laptop computers, and digital cameras. Some devices, such as smartphones and digital cameras, may include an image sensor in addition to an electronic display. Devices with displays and image sensors, however, are generally limited in their ability to accurately capture and display the full photonic environment.

[54] To address problems and limitations associated with existing electronic displays, embodiments of the disclosure provide various electronic assemblies for capturing and displaying light fields. FIGURES 1A-9 are directed to display assemblies with electronically emulated transparency, FIGURES 10-11 are directed to direct camera-to-display systems, FIGURES 12-14 are directed to in-layer signal processing, FIGURES 15-21 are directed to plenoptic cellular imaging systems, FIGURES 22-25 are directed to three-dimensional (3D) electronics distribution by geodesic faceting, FIGURES 26-36 are directed to distributed multi-screen arrays for high density displays, FIGURES 37-42 are directed to distributed multi-aperture camera arrays, and FIGURES 43-51 are directed to tracking surfaces that utilize IR emitters and IR detectors to detect a cone of retinal retro-reflected IR light from the viewer's eye.

[55] To facilitate a better understanding of the present disclosure, the following examples of certain embodiments are given. The following examples are not to be read to limit or define the scope of the disclosure. Embodiments of the present disclosure and its advantages are best understood by referring to FIGURES 1A-42, where like numbers are used to indicate like and corresponding parts.

[56] FIGURES 1A-9 illustrate various aspects of an assembly with electronically emulated transparency, according to certain embodiments. In general, the electronic assembly illustrated in detail in FIGURES 7-8 may be used in different applications to provide features such as virtual reality (VR), augmented reality (AR), and mixed reality (MR). For VR applications, a digital display is required which can completely replace a view of the real world, similar to how a standard computer monitor blocks the view of the scene behind it. However, for AR applications, a digital display is required which can overlay data on top of that view of the real world, such as a pilot's heads-up display in a modern cockpit. MR applications require a combination of both. Typical systems used to provide some or all of these features are not desirable for a number of reasons. For example, typical solutions do not provide an accurate or complete recreation of a target light field. As another example, existing solutions are typically bulky and not comfortable for users.

[57] To address problems and limitations with existing electronic displays, embodiments of the disclosure provide a thin electronic system which offers both opacity and controllable unidirectional emulated transparency, as well as digital display capabilities. From one side the surface appears opaque, but from the opposite side the surface can appear fully transparent, appear fully opaque, act as a digital display, or any combination of these. In some embodiments, simultaneous plenoptic sensing and display technologies are combined within a single layered structure to form what appears to be a unidirectional visually transparent surface. The system may include multiple layers of electronics and optics for the purpose of artificially recreating transparency that may be

augmented and/or digitally controlled. Individual image sensor pixels on one side may be arranged spatially to match the positions of display pixels on the opposite side of the assembly. In some embodiments, all electronic driving circuitry as well as some display logic circuitry may be sandwiched between the sensor layer and display layer, and each sensor pixel's output signal may be channeled through the circuitry to the corresponding display pixel on the opposite side. In some embodiments, this centrally-processed signal is aggregated with the incoming signal from the plenoptic imaging sensor array on the opposite side, and is handled according to the following modes of operation. In VR mode, the external video feed overrides the camera data, completely replacing the user's view of the outside world with the incoming view from the video. In AR mode, the external video feed is overlaid on the camera data, resulting in a combined view of both the external world and the view from the video (e.g., the video data is simply added to the scene). In MR mode, the external video feed is mixed with the camera data, allowing virtual objects to appear to interact with actual objects in the real world, altering the virtual content to make it appear integrated with the actual environment through object occlusion, lighting, etc.

[58] Some embodiments combine stacked transparent high dynamic range (HDR) sensor and display pixels into a single structure, with sensor pixels on one side of the assembly and display pixels on the other, and with pixel-for-pixel alignment between camera and display. Both the sensor and display pixel arrays may be focused by groups of micro lenses to capture and display four-dimensional light fields. This means that the complete view of the real world is captured on one side of the assembly and electronically reproduced on the other, allowing

for partial or complete alteration of the incoming image while maintaining image clarity, luminance, and enough angular resolution for the display side to appear transparent, even when viewed at oblique angles.

[59] FIGURES 1A-6C are provided to illustrate the differences between electronically emulated transparency provided by embodiments of the disclosure and typical camera images (such as through a camera viewfinder or using a smartphone to display its current camera image). FIGURES 1A-1C illustrate a reference scene with various 3D objects 110 (i.e., 110A-C) and a frontal viewing position, according to certain embodiments. FIGURE 1A is a top view of an arrangement of 3D objects 110 and a frontal viewing direction of 3D objects 110. FIGURE 1B is a perspective view of the same arrangement of 3D objects 110 and frontal viewing direction as FIGURE 1A. FIGURE 1C is the resulting front view of 3D objects 110 from the position illustrated in FIGURES 1A and 1B. As can be seen, the view in FIGURE 1C of 3D objects 110 is a normal, expected view of 3D objects 110 (i.e., the view of 3D objects 110 is not altered at all because there is nothing between the viewer and 3D objects 110).

[60] FIGURES 2A-2C illustrate viewing the 3D objects 110 of FIGURES 1A-1C through a transparent panel 210, according to certain embodiments. Transparent panel 210 may be, for example, a piece of transparent glass. FIGURE 2A is a top view of a frontal viewing direction of 3D objects 110 through transparent panel 210, and FIGURE 2B is a perspective view of the same arrangement of 3D objects 110 and frontal viewing direction as FIGURE 2A. FIGURE 2C is the resulting front view of 3D objects 110 through transparent panel 210 from the position illustrated in FIGURES 2A and 2B. As can be seen, the view in FIGURE 2C of

3D objects 110 through transparent panel 210 is a normal, expected view of 3D objects 110 (i.e., the view of 3D objects 110 is not altered at all because the viewer is looking through a transparent panel 210). In other words, the view of 3D objects 110 through transparent panel 210 in FIGURE 2C is the same as the view in FIGURE 1C where no object is between the viewer and 3D objects 110 (i.e., "perceived" transparency). Stated another way, the edges of the projected imagery on transparent panel 210 line up with the view of the actual 3D objects 110 behind transparent panel 210 to create a view-aligned image 220A of 3D object 110A, a view-aligned image 220B of 3D object 110B, and a view-aligned image 220C of 3D object 110C.

[61] FIGURES 3A-3C illustrate viewing the 3D objects 110 of FIGURES 1A-1C through a camera image panel 310, according to certain embodiments. Camera image panel 310 may be, for example, a camera viewfinder or a display of a smartphone that is displaying its current camera image. In these images, camera image panel 310 is at an angle (e.g., 30 degrees) to the viewer to illustrate how such systems do not provide true emulated transparency. FIGURE 3A is a top view of a frontal viewing direction of 3D objects 110 through camera image panel 310, and FIGURE 3B is a perspective view of the same arrangement of 3D objects 110 and frontal viewing direction as FIGURE 3A. FIGURE 3C is the resulting front view of 3D objects 110 through camera image panel 310 from the position illustrated in FIGURES 3A and 3B. As can be seen, the view in FIGURE 3C of 3D objects 110 through camera image panel 310 is different from a view of 3D objects 110 through transparent panel 210. Here, camera image panel 310 redirects the lines of sight that are normal to camera image panel 310, thereby showing no perceived transparency (i.e., the image on camera image panel 310 is not aligned with

the view but instead depicts the image acquired by the redirected lines of sight). Stated another way, the edges of the projected imagery on camera image panel 310 do not line up with the view of the actual 3D objects 110 behind camera image panel 310. This is illustrated by an unaligned image 320A of 3D object 110A and an unaligned image 320B of 3D object 110B on camera image panel 310 in FIGURE 3C.

[62] FIGURES 4A-4C illustrate viewing the 3D objects 110 of FIGURES 1A-1C through an emulated-transparency electronic panel 410, according to certain embodiments. In these images, emulated transparency panel 410 is at an angle (e.g., 30 degrees) to the viewer to illustrate how emulated transparency panel 410 provides true emulated transparency unlike camera image panels 310. FIGURE 4A is a top view of a frontal viewing direction of 3D objects 110 through emulated transparency panel 410, and FIGURE 4B is a perspective view of the same arrangement of 3D objects 110 and frontal viewing direction as FIGURE 4A. FIGURE 4C is the resulting front view of 3D objects 110 through emulated transparency panel 410 from the position illustrated in FIGURES 4A and 4B. As can be seen, the view in FIGURE 4C of 3D objects 110 through emulated transparency panel 410 is different from a view of 3D objects 110 through camera image panel 310 but is similar to a view of 3D objects 110 through transparent panel 210. Here, emulated transparency panel 410 does not redirect the lines of sight from the viewer through emulated transparency panel 410, but allows them to remain virtually unchanged and thereby providing emulated transparency (i.e., the image on emulated transparency panel 410 is aligned with the view as in transparent panel 210). Like transparent panel 210, the edges of the projected imagery on emulated transparency panel 410 lines up with the view of the actual 3D objects 110 behind

emulated transparency panel 410 to create view-aligned image 220A of 3D object 110A, view-aligned image 220B of 3D object 110B, and view-aligned image 220C of 3D object 110C.

[63] FIGURES 5A-5C illustrate viewing the 3D objects 110 of FIGURES 1A-1C through the camera image panel 310 of FIGURES 3A-3C, but from an alternate angle. In these images, camera image panel 310 is at a different 30 degree angle to the viewer to further illustrate how such systems do not provide true emulated transparency. Like in FIGURES 3A-3C, the edges of the projected imagery on camera image panel 310 do not line up with the view of the actual 3D objects 110 behind camera image panel 310. This is illustrated by an unaligned image 320C of 3D object 110C and an unaligned image 320B of 3D object 110B on camera image panel 310 in FIGURE 5C.

[64] FIGURES 6A-6C illustrate viewing the 3D objects 110 of FIGURES 1A-1C through the emulated-transparency electronic panel 410 of FIGURES 4A-4C, but from an alternate angle. Like in FIGURES 4A-4C, the edges of the projected imagery on emulated transparency panel 410 in FIGURE 6C line up with the view of the actual 3D objects 110 behind emulated transparency panel 410 to create view-aligned image 220B of 3D object 110B and view-aligned image 220C of 3D object 110C.

[65] As illustrated above in FIGURES 4A-4C and 6A-6C, emulated transparency panel 410 provides view-aligned images 220 of 3D objects 110 behind emulated transparency panel 410, thereby providing electronically-emulated transparency. FIGURES 7-8 illustrate an example embodiment of emulated transparency panel 410. FIGURE 7 illustrates a cut-away view of an emulated transparency assembly 710 which may be emulated transparency panel 410, and FIGURE 8 illustrates an exploded

view of the emulated transparency assembly 710 of FIGURE 7, according to certain embodiments.

[66] In some embodiments, emulated transparency assembly 710 includes two microlens arrays 720 (i.e., a sensor side microlens array 720A and a display side microlens array 720B), an image sensor layer 730, a circuit board 740, and an electronic display layer 760. In general, incoming light field 701 enters sensor side microlens array 720A where it is detected by image sensor layer 730. Electronically-replicated outgoing light field 702 is then generated by electronic display layer 760 and projected through display side microlens array 720B. As explained in more detail below, the unique arrangement and features of emulated transparency assembly 710 permits it to provide electronically-emulated transparency via electronically-replicated outgoing light field 702, as well as other features described below. While a specific shape of emulated transparency assembly 710 is illustrated in FIGURES 7-8, emulated transparency assembly 710 may have any appropriate shape including any polygonal or non-polygonal shape, and both flat and non-flat configurations.

[67] Microlens arrays 720 (i.e., sensor side microlens array 720A and display side microlens array 720B) are generally layers of microlenses. In some embodiments, each microlens of microlens arrays 720 is a plenoptic cell 1510 as described in more detail below in reference to FIGURE 15. In general, each microlens of sensor side microlens array 720A is configured to capture a portion of incoming light field 701 and direct it to pixels within image sensor layer 730. Similarly, each microlens of display side microlens array 720B is configured to emit a portion of electronically-replicated outgoing light field 702 that is generated by pixels of electronic display layer 760. In

some embodiments, each microlens of sensor side microlens array 720A and display side microlens array 720B is in a 3D shape with a collimating lens on one end of the 3D shape. The 3D shape may be, for example, a triangular polyhedron, a rectangular cuboid, a pentagonal polyhedron, a hexagonal polyhedron, a heptagonal polyhedron, or an octagonal polyhedron. In some embodiments, each microlens of sensor side microlens array 720A and display side microlens array 720B includes opaque walls such as cell walls 1514 (discussed below in reference to FIGURE 15) that are configured to prevent light from bleeding into adjacent microlenses. In some embodiments, each microlens of sensor side microlens array 720A and display side microlens array 720B additionally or alternatively includes a light incidence angle rejection coating such as filter layer 1640 described below to prevent light from bleeding into adjacent microlenses.

[68] In some embodiments, the microlenses of sensor side microlens array 720A are oriented towards a first direction, and the microlenses of display side microlens array 720B are oriented towards a second direction that is 180 degrees from the first direction. In other words, some embodiments of emulated transparency assembly 710 include a sensor side microlens array 720A that is oriented exactly opposite from display side microlens array 720B. In other embodiments, any other orientation of sensor side microlens array 720A and display side microlens array 720B is possible.

[69] In general, image sensor layer 730 includes a plurality of sensor pixels that are configured to detect incoming light field 701 after it passes through sensor side microlens array 720A. In some embodiments, image sensor layer 730 includes an array of sensor units 735 (e.g., sensor units 735A-C as illustrated in FIGURE 8). Each sensor unit 735 may

be a defined portion of image sensor layer 730 (e.g., a specific area such as a portion of a rectangular grid) or a specific number or pattern of sensor pixels within image sensor layer 730. In some embodiments, each sensor unit 735 corresponds to a specific logic unit 755 of logic unit layer 750 as described below. In some embodiments, image sensor layer 730 is coupled to or otherwise immediately adjacent to sensor side microlens array 720A. In some embodiments, image sensor layer 730 is between sensor side microlens array 720A and circuit board 740. In other embodiments, image sensor layer 730 is between sensor side microlens array 720A and logic unit layer 750. In some embodiments, other appropriate layers may be included in emulated transparency assembly 710 on either side of image sensor layer 730. Furthermore, while a specific number and pattern of sensor units 735 are illustrated, any appropriate number (including only one) and pattern of sensor units 735 may be used.

[70] Circuit board 740 is any appropriate rigid or flexible circuit board. In general, circuit board 740 includes various pads and traces that provide electrical connections between various layers of emulated transparency assembly 710. As one example, in embodiments that include circuit board 740, circuit board 740 may be located between image sensor layer 730 and logic unit layer 750 as illustrated in FIGURES 7-8 in order to provide electrical connections between image sensor layer 730 and logic unit layer 750. In other embodiments, circuit board 740 may be located between logic unit layer 750 and electronic display layer 760 in order to provide electrical connections between logic unit layer 750 and electronic display layer 760. In some embodiments, circuit board 740 includes an array of unit attachment locations 745 (e.g., unit attachment locations 745A-

C as illustrated in FIGURE 8). Each unit attachment location 745 may be a defined portion of circuit board 740 (e.g., a specific area such as a portion of a rectangular grid) and may include a plurality of pads (e.g., ball grid array (BGA) pad) and/or vias. In some embodiments, each unit attachment location 745 corresponds to a specific sensor unit 735 of image sensor layer 730 and a specific display unit 765 of electronic display layer 760 (e.g., unit attachment location 745A corresponds to sensor unit 735A and display unit 765A) and is configured to permit electrical communication between the corresponding specific sensor unit 735 and the specific display unit 765.

[71] Logic unit layer 750 provides optional/additional logic and/or processing for emulated transparency assembly 710. In general, logic unit layer 750 emulates transparency by directing signals from the plurality of sensor pixels of image sensor layer 730 to the plurality of display pixels of electronic display layer 760, thereby emitting electronically-replicated outgoing light field 702 from display side microlens array 720B at angles that correspond to angles of the incoming light field 701 detected through sensor side microlens array 720A. By emitting electronically-replicated outgoing light field 702 from display side microlens array 720B at angles that correspond to angles of the incoming light field 701 detected through sensor side microlens array 720A, an image is displayed that matches what would be seen if emulated transparency assembly 710 was not present (i.e., emulated transparency). In some embodiments, logic unit layer 750 includes an array of logic units 755 (e.g., logic units 755A-C as illustrated in FIGURE 8). Each logic units 755 may be a defined portion of logic unit layer 750 (e.g., a specific area such as a portion of a rectangular grid). In some embodiments, each logic unit 755 is a separate physical,

rigid unit that is later joined to or coupled to other logic units 755 in order to form logic unit layer 750. In some embodiments, each logic unit 755 corresponds to a specific sensor unit 735 of image sensor layer 730 and a specific display unit 765 of electronic display layer 760 (e.g., logic unit 755A corresponds to (and is electrically coupled to) sensor unit 735A and display unit 765A). In some embodiments, logic unit layer 750 is located between circuit board 740 and electronic display layer 760. In other embodiments, logic unit layer 750 is between image sensor layer 730 and circuit board 740. In some embodiments, other appropriate layers may be included in emulated transparency assembly 710 on either side of logic unit layer 750. Furthermore, while a specific number and pattern of logic units 755 is illustrated, any appropriate number (including none or only one) and pattern of logic units 755 may be used.

[72] In general, electronic display layer 760 includes a plurality of display pixels that are configured to generate and project electronically-replicated outgoing light field 702 through display side microlens array 720B. In some embodiments, electronic display layer 760 includes an array of display units 765 (e.g., display units 765A-C as illustrated in FIGURE 8). Each display unit 765 may be a defined portion of electronic display layer 760 (e.g., a specific area such as a portion of a rectangular grid) or a specific number or pattern of display pixels within electronic display layer 760. In some embodiments, each display unit 765 corresponds to a specific logic unit 755 of logic unit layer 750. In some embodiments, electronic display layer 760 is coupled to or otherwise immediately adjacent to display side microlens array 720B. In some embodiments, electronic display layer 760 is between

display side microlens array 720B and circuit board 740. In other embodiments, electronic display layer 760 is between display side microlens array 720B and logic unit layer 750. In some embodiments, other appropriate layers may be included in emulated transparency assembly 710 on either side of electronic display layer 760. Furthermore, while a specific number and pattern of display units 765 are illustrated, any appropriate number (including only one) and pattern of display units 765 may be used.

[73] In some embodiments, the sensor pixels of image sensor layer 730 may be sensor pixels 1800 as described in FIGURES 18-20 and their associated descriptions in U.S. Patent Application No. 15/724,027 entitled "Stacked Transparent Pixel Structures for Image Sensors," which is incorporated herein by reference in its entirety. In some embodiments, the display pixels of electronic display layer 760 are display pixels 100 as described in FIGURES 1-4 and their associated descriptions in U.S. Patent Application No. 15/724,004 entitled "Stacked Transparent Pixel Structures for Electronic Displays," which is incorporated herein by reference in its entirety.

[74] While FIGURES 7-8 depict emulated transparency assembly 710 as having arrays of sensors, displays, and electronics, other embodiments may have single-unit setups. Furthermore, while the illustrated embodiments of emulated transparency assembly 710 depict unidirectional emulated transparency (i.e. allowing the capture of incoming light field 701 from a single direction and displaying a corresponding electronically-replicated outgoing light field 702 in the opposite direction), other embodiments may include arrangements and combinations of emulated transparency assembly 710 that permit bidirectional transparency.

[75] FIGURE 9 illustrates a method 900 of manufacturing the emulated transparency assembly 710 of FIGURE 7, according to certain embodiments. Method 900 may begin in step 910 where a plurality of unit attachment locations are formed on a circuit board. In some embodiments, the circuit board is circuit board 740 and the unit attachment locations are unit attachment locations 145. In some embodiments, each unit attachment location corresponds to one of a plurality of display units such as display units 765 and one of a plurality of sensor units such as sensor units 735.

[76] At step 920, a plurality of sensor units are coupled to a first side of the circuit board. In some embodiments, the sensor units are sensor units 735. In some embodiments, each sensor unit is coupled in step 920 to a respective one of the unit attachment locations of step 910. In some embodiments, the sensor units are first formed into an image sensor layer such as image sensor layer 730, and the image sensor layer is coupled to the first side of the circuit board in this step.

[77] At step 930, a plurality of display units are coupled to a second side of the circuit board that is opposite the first side. In some embodiments, the display units are display units 765. In some embodiments, each display unit is coupled to a respective one of the unit attachment locations. In some embodiments, the display units are first formed into a display layer such as electronic display layer 760, and the display layer is coupled to the second side of the circuit board in this step.

[78] At step 940, a first plurality of microlenses are coupled to the plurality of sensor units of step 920. In some embodiments, the microlenses are plenoptic cells 1510. In some embodiments, the microlenses are first formed into an microlens

array layer such as sensor side microlens array 720A, and the microlens array layer is coupled to the sensor units.

[79] At step 950, a second plurality of microlenses are coupled to the plurality of display units of step 930. In some embodiments, the microlenses are plenoptic cells 1510. In some embodiments, the microlenses are first formed into an microlens array layer such as display side microlens array 720B, and the microlens array layer is coupled to the display units. After step 950, method 900 may end.

[80] In some embodiments, method 900 may additionally include coupling a plurality of logic units between the circuit board of step 910 and the plurality of display units of step 930. In some embodiments, the logic units are logic units 755. In some embodiments, the plurality of logic units are coupled between the circuit board and the plurality of sensor units of step 920.

[81] Particular embodiments may repeat one or more steps of method 900, where appropriate. Although this disclosure describes and illustrates particular steps of method 900 as occurring in a particular order, this disclosure contemplates any suitable steps of method 900 occurring in any suitable order (e.g., any temporal order). Moreover, although this disclosure describes and illustrates an example emulated transparency assembly manufacturing method including the particular steps of method 900, this disclosure contemplates any suitable emulated transparency assembly manufacturing method including any suitable steps, which may include all, some, or none of the steps of method 900, where appropriate. Furthermore, although this disclosure describes and illustrates particular components, devices, or systems carrying out particular steps of method 900, this disclosure contemplates any suitable combination of any

suitable components, devices, or systems carrying out any suitable steps of method 900.

[82] FIGURE 10 illustrates a direct sensor-to-display system 1000 that may be implemented by the emulated transparency assembly of FIGURE 7, according to certain embodiments. In general, FIGURE 10 illustrates how embodiments of emulated transparency assembly 710 utilize a direct association of input pixels to corollary output pixels. In some embodiments, this is accomplished by using a layered approach such that the image sensor layer 730 and electronic display layer 760 are in close proximity to one another, mounted on opposite sides of a shared substrate (e.g., circuit board 740) as illustrated in FIGURES 7-8. Signals from image sensor layer 730 may be propagated directly to electronic display layer 760 through circuit board 740 (and logic unit layer 750 in some embodiments). Logic unit layer 750 provides simple processing with optional input for any necessary control or augmentation. Typical electronic sensor/display pairs (e.g., a digital camera) do not express a one-to-one relationship in that the display is not coupled directly with the input sensor and thus requires some degree of image transformation. Certain embodiments of the disclosure, however, implement a one-to-one mapping between input and output pixels (i.e., the sensor pixel and display pixel layouts are identical), thereby circumventing the need for any image transformation. This reduces the complexity and power requirements of emulated transparency assembly 710.

[83] As illustrated in FIGURE 10, each sensor unit 735 is directly coupled to a corresponding display unit 765. For example, sensor unit 735A may be directly coupled to display unit 765A, sensor unit 735B may be directly coupled to display unit 765B, and so on. In some embodiments, the signaling between

sensor units 735 and display units 765 may be any appropriate differential signaling such as low-voltage differential signaling (LVDS). More specifically, each sensor unit 735 may output first signals in a specific format (e.g., LVDS) that corresponds to incoming light field 701. In some embodiments, the first signals are sent via a corresponding logic unit 755, which in turn sends second signals to display unit 765 in the same format as the first signals (e.g., LVDS). In other embodiments, the first signals are sent directly to display units 765 from sensor units 735 (e.g., sensor units 735 and display units 765 are coupled directly to opposite sides of circuit board 740). Display unit 765 receives the second signals from the logic unit 755 (or the first signals directly from the sensor unit 735 via circuit board 740) and uses them to generate outgoing light field 702.

[84] Because no conversion is needed in the signaling between sensor units 735 and display units 765, emulated transparency assembly 710 may provide many benefits from typical display/sensor combinations. First, no signal processors are needed to convert the signals from sensor units 735 to display units 765. For example, no off-board signal processors are needed to perform image transformation between sensor units 735 and display units 765. This reduces the space, complexity, weight, and cost requirements for emulated transparency assembly 710. Second, emulated transparency assembly 710 may provide greater resolutions than would typically be possible for display/sensor combinations. By directly coupling sensor units 735 with display units 765 and not requiring any processing or transformation of data between the units, the resolution of sensor units 735 and display units 765 may be far greater than would typically be possible. Furthermore, emulated transparency

assembly 710 may provide heterogeneous resolutions across sensor units 735 and display units 765 at any particular time. That is, a particular sensor unit 735 and corresponding display unit 765 may have a particular resolution that is different from other sensor units 735 and display units 765 at a particular time, and the resolutions of each sensor unit 735 and display unit 765 may be changed at any time.

[85] In some embodiments, each particular sensor pixel of a sensor unit 735 is mapped to a single display pixel of a corresponding display unit 765, and the display pixel displays light corresponding to light captured by its mapped sensor pixel. This is illustrated best in FIGURES 17A-17B. As one example, each center sensing pixel 1725 of a particular plenoptic cell 1510 of sensor side microlens array 720A (e.g., the bottom plenoptic cell 1510 of sensor side microlens array 720A in FIGURE 17A) is mapped to a center display pixel 1735 of a corresponding plenoptic cell 1510 of display side microlens array 720B (e.g., the bottom plenoptic cell 1510 of display side microlens array 720B in FIGURE 17A). As another example, each top sensing pixel 1725 of a particular plenoptic cell 1510 of sensor side microlens array 720A (e.g., the top plenoptic cell 1510 of sensor side microlens array 720A in FIGURE 17B) is mapped to a bottom display pixel 1735 of a corresponding plenoptic cell 1510 of display side microlens array 720B (e.g., the top plenoptic cell 1510 of display side microlens array 720B in FIGURE 17B).

[86] In some embodiments, sensor units 735 are coupled directly to circuit board 740 while display units 765 are coupled to logic units 755 (which are in turn coupled to circuit board 740) as illustrated in FIGURE 8. In other embodiments, display units 765 are coupled directly to circuit board 740 while sensor

units 735 are coupled to logic units 755 (which are in turn coupled to circuit board 740). In other embodiments, both sensor units 735 and display units 765 are coupled directly to circuit board 740 (i.e., without any intervening logic units 755). In such embodiments, sensor units 735 and display units 765 are coupled to opposite sides of circuit board 740 at unit attachment locations 745 (e.g., sensor unit 735A and display unit 765A are coupled to opposite sides of circuit board 740 at unit attachment location 745A).

[87] FIGURE 11 illustrates a method 1100 of manufacturing the direct sensor-to-display system 1000 of FIGURE 10, according to certain embodiments. Method 1100 may begin at step 1110 where a plurality of unit attachment locations are formed on a circuit board. In some embodiments, the circuit board is circuit board 740 and the unit attachment locations are unit attachment locations 745. In some embodiments, each unit attachment location corresponds to one of a plurality of display units and one of a plurality of sensor units. The display units may be display units 765 and the sensor units may be sensor units 735. In some embodiments, each particular unit attachment location includes BGA pads that are configured to couple to one of the plurality of sensor units and/or one of the plurality of logic units. In some embodiments, each particular unit attachment location includes a plurality of interconnection pads configured to electrically couple the particular unit attachment location to one or more adjacent unit attachment locations. In some embodiments, the unit attachment locations are arranged into a plurality of columns and plurality of rows as illustrated in FIGURE 8.

[88] At step 1120, a plurality of sensor units are coupled to a first side of the circuit board. In some

embodiments, each sensor unit is coupled to a respective one of the unit attachment locations of step 1110. At step 1130, a plurality of display units are coupled to a second side of the circuit board that is opposite to the first side. In some embodiments, each display unit is coupled to a respective one of the unit attachment locations of step 1110 such that each particular one of the plurality of sensor pixel units is mapped to a corresponding one of the plurality of display pixel units. By mapping each particular sensor pixel unit to one of the display pixel units, the display pixels of each particular one of the plurality of display pixel units are configured to display light corresponding to light captured by sensor pixels of its mapped sensor pixel unit. After step 1130, method 1100 may end.

[89] Particular embodiments may repeat one or more steps of method 1100, where appropriate. Although this disclosure describes and illustrates particular steps of method 1100 as occurring in a particular order, this disclosure contemplates any suitable steps of method 1100 occurring in any suitable order (e.g., any temporal order). Moreover, although this disclosure describes and illustrates an example direct sensor-to-display system manufacturing method including the particular steps of method 1100, this disclosure contemplates any suitable direct sensor-to-display system manufacturing method including any suitable steps, which may include all, some, or none of the steps of method 1100, where appropriate. Furthermore, although this disclosure describes and illustrates particular components, devices, or systems carrying out particular steps of method 1100, this disclosure contemplates any suitable combination of any suitable components, devices, or systems carrying out any suitable steps of method 1100.

[90] FIGURES 12-13 illustrate various in-layer signal processing configurations that may be used by emulated transparency assembly 710 of FIGURE 7, according to certain embodiments. In general, the configurations of FIGURES 12-13 utilize a layer of digital logic (e.g., logic unit layer 750) that is sandwiched between the camera and display (i.e., between image sensor layer 730 and electronic display layer 760). These configurations allow for local, distributed processing of large quantities of data (e.g., 160k of image data or more), thereby circumventing bottlenecks as well as performance, power, and transmission line issues associated with typical configurations. Human visual acuity represents a tremendous amount of data which must be processed in real-time. Typical imaging systems propagate a single data stream to/from a high-powered processor (e.g., a CPU or GPU), which may or may not serialize the data for manipulation. The bandwidth required for this approach at human 20/20 visual acuity far exceeds that of any known transmission protocols. Typical systems also use a master controller which is responsible for either processing all incoming/outgoing data or managing distribution to smaller processing nodes. Regardless, all data must be transported off-system/off-chip, manipulated, and then returned to the display device(s). However, this typical approach is unable to handle the enormous amount of data required by human visual acuity. Embodiments of the disclosure, however, harness the faceted nature of a sensor/display combination as described herein to decentralize and localize signal processing. This enables previously unachievable real-time digital image processing.

[91] As illustrated in FIGURES 12-13, certain embodiments of emulated transparency assembly 710 include logic unit layer 750 that contains the necessary logic to manipulate input

signals from image sensor layer 730 and provide output signals to electronic display layer 760. In some embodiments, logic unit layer 750 is located between image sensor layer 730 and circuit board 740 as illustrated in FIGURE 12. In other embodiments, logic unit layer 750 is located between circuit board 740 and electronic display layer 760 as illustrated in FIGURE 13. In general, logic unit layer 750 is a specialized image processing layer that is capable of mixing an input signal directly from image sensor layer 730 and performing one or more mathematical operations (e.g., matrix transforms) on the input signal before outputting a resulting signal directly to electronic display layer 760. Since each logic unit 755 of logic unit layer 750 is responsible only for it's associated facet (i.e., sensor unit 735 or display unit 765), the data of the particular logic unit 755 can be manipulated with no appreciable impact to the system-level I/O. This effectively circumvents the need to parallelize any incoming sensor data for centralized processing. The distributed approach enables emulated transparency assembly 710 to provide multiple features such as magnification/zoom (each facet applies a scaling transform to its input), vision correction (each facet applies a simulated optical transformation compensating for common vision issues such as near-sightedness, far-sightedness, astigmatism, etc.), color blindness correction (each facet applies a color transformation compensating for common color blindness issues), polarization (each facet applies a transformation simulating wave polarization allowing for glare reduction), and dynamic range reduction (each facet applies a transformation that darkens high-intensity regions (e.g. Sun) and lightens low-intensity regions (e.g. shadows)). Furthermore, since any data transformations remain localized to logic unit layer 750 of each

facet, there may be no need for long transmission lines. This circumvents issues of cross talk, signal integrity, etc. Additionally, since the disclosed embodiments do not require optical transparency (but instead harness emulated transparency), there is no functional impact to placing an opaque processing layer between the sensor and display facets.

[92] In some embodiments, logic unit layer 750 contains discrete logic units (e.g., transistors) that are formed directly on circuit board 740. For example, standard photo lithography techniques may be used to form logic unit layer 750 directly on circuit board 740. In other embodiments, each logic unit 755 is a separate integrated circuit (IC) that is coupled to either a sensor facet or a display facet, or directly to circuit board 740. As used herein, "facet" refers to a discrete unit that is separately manufactured and then coupled to circuit board 740. For example, a "display facet" may refer to a unit that includes a combination of an electronic display layer 760 and a display side microlens array 720B, and a "sensor facet" may refer to a unit that includes a combination of an image sensor layer 730 and a sensor side microlens array 720A. In some embodiments, a display facet may include a single display unit 765, or it may include multiple display units 765. Similarly, a sensor facet may include a single sensor unit 735, or it may include multiple sensor units 735. In some embodiments, a logic unit 755 may be included in either a sensor facet or a display facet. In embodiments where a logic unit 755 is a separate IC that is coupled directly to either a display or sensor facet (as opposed to being formed directly on circuit board 740), any appropriate technique such as 3D IC design with through-silicon vias may be used to couple the IC of logic unit 755 to a wafer of the facet.

[93] In some embodiments, logic unit layer 750 is an application-specific integrated circuit (ASIC) or an arithmetic logic unit (ALU), but not a general purpose processor. This allows logic unit layer 750 to be power efficient. Furthermore, this allows logic unit layer 750 to operate without cooling, further reducing cost and power requirements of emulated transparency assembly 710.

[94] In some embodiments, logic units 755 are configured to communicate using the same protocol as sensor units 735 and display units 765. For example, in embodiments where logic units 755 are discrete ICs, the ICs may be configured to communicate in a same protocol as the sensor and display facets (e.g., LVDS or Inter-Integrated Circuit (I^2C)). This eliminates the problem of having to translate between the sensor and display facet, thereby reducing power and cost.

[95] In some embodiments, logic unit layer 750 performs one or more operations on signals received from image sensor layer 730 before transmitting output signals to electronic display layer 760. For example, logic unit layer 750 may transform received signals from image sensor layer 730 to include augmented information for display on electronic display layer 760. This may be used, for example, to provide AR to a viewer. In some embodiments, logic unit layer 750 may completely replace received signals from image sensor layer 730 with alternate information for display on electronic display layer 760. This may be used, for example, to provide VR to a viewer.

[96] FIGURE 14 illustrates a method 1400 of manufacturing the in-layer signal processing systems of FIGURES 12-13, according to certain embodiments. Method 1400 may begin in step 1410 where a plurality of sensor units are coupled to a first side of a circuit board. In some embodiments, the sensor units

are sensor units 735, and the circuit board is circuit board 740. In some embodiments, each sensor unit is coupled to one of a plurality of unit attachment locations such as unit attachment locations 745. Each sensor unit includes a plurality of sensor pixels.

[97] At step 1420, a plurality of display units are formed. In some embodiments, the display units are a combination of display units 765 and logic units 755. Each display unit may be formed by combining an electronic display and a logic unit into a single 3D integrated circuit using through-silicon vias. Each display unit includes a plurality of display pixels.

[98] At step 1430, the plurality of display units of step 1420 are coupled to a second side of the circuit board that is opposite the first side. In some embodiments, each logic unit is coupled to a respective one of the unit attachment locations. After step 1430, method 1400 may end.

[99] Particular embodiments may repeat one or more steps of method 1400, where appropriate. Although this disclosure describes and illustrates particular steps of method 1400 as occurring in a particular order, this disclosure contemplates any suitable steps of method 1400 occurring in any suitable order (e.g., any temporal order). Moreover, although this disclosure describes and illustrates an example in-layer signal processing system manufacturing method including the particular steps of method 1400, this disclosure contemplates any suitable in-layer signal processing system manufacturing method including any suitable steps, which may include all, some, or none of the steps of method 1400, where appropriate. Furthermore, although this disclosure describes and illustrates particular components, devices, or systems carrying out particular steps of method 1400, this disclosure contemplates any suitable combination of

any suitable components, devices, or systems carrying out any suitable steps of method 1400.

[100] FIGURES 15-17C illustrate various views of an array 1500 of plenoptic cells 1510 that may be used within microlens arrays 720A-B of emulated transparency assembly 710. FIGURE 15 illustrates a plenoptic cell assembly 1500, FIGURE 16 illustrates a cross section of a portion of the plenoptic cell assembly 1500 of FIGURE 15, and FIGURES 17A-17C illustrate cross sections of a portion of the plenoptic cell assembly 1500 of FIGURE 15 with various incoming and outgoing fields of light.

[101] Standard electronic displays typically include planar arrangements of pixels which form a two-dimensional rasterized image, conveying inherently two-dimensional data. One limitation is that the planar image cannot be rotated in order to perceive a different perspective within the scene being conveyed. In order to clearly view this image, regardless of what is portrayed within the image itself, either a viewer's eyes or the lens of a camera must focus on the screen. By contrast, a volume of light entering the eyes from the real world allows the eyes to naturally focus on any point within that volume of light. This plenoptic "field" of light contains rays of light from the scene as they naturally enter the eye, as opposed to a virtual image focused by an external lens at a single focal plane. While existing light field displays may be able to replicate this phenomenon, they present substantial tradeoffs between spatial and angular resolutions, resulting in the perceived volume of light looking fuzzy or scant in detail.

[102] To overcome problems and limitation with existing light field displays, embodiments of the disclosure provide a coupled light field capture and display system that is capable of recording and then electronically recreating the incoming

plenoptic volume of light. Both the capture and the display process are accomplished by an arrangement of plenoptic cells 1510 responsible for recording or displaying smaller views of a larger compound image. Each plenoptic cell 1510 of the sensor is itself comprised of a dense cluster of image sensor pixels, and each plenoptic cell of the display is itself comprised of a dense cluster of display pixels. In both cases, light rays entering the sensor cells or exiting the display cells are focused by one or more transparent lenslets 1512 to produce a precisely tuned distribution of near-collimated rays. This essentially records an incoming light field and reproduces it on the opposite side of the assembly. More specifically, for the sensor, the volume of light entering the lens (or series of lenses) of this cell is focused onto the image pixels such that each pixel gathers light from only one direction, as determined by its position within the cell and the profile of the lens. This allows rasterized encoding of the various angular rays within the light field, with the number of pixels in the cell determining the angular resolution recorded. For the display, the light emitted from the pixels is focused by an identical lens (or series of lenses) to create a volume of light that matches what was recorded by the sensor, plus any electronic augmentation or alterations (e.g., from logic unit layer 750 described above). The cone of emitted light from this cell contains a subset of rays at enough interval angles to enable the formation of a light field for the viewer, where each output ray direction is determined by the position of its originating pixel within the cell and the profile of the lens.

[103] Plenoptic cells 1510 may be utilized by both sensor side microlens array 720A and display side microlens array 720B. For example, multiple plenoptic cells 1510A may be included in

sensor side microlens array 720A, and each plenoptic cell 1510A may be coupled to or otherwise adjacent to an image sensor 1520. Image sensor 1520 may be a portion of image sensor layer 730 and may include a sensor pixel array 1525 that includes sensing pixels 1725. Similarly, multiple plenoptic cells 1510B may be included in display side microlens array 720B, and each plenoptic cell 1510B may be coupled to or otherwise adjacent to a display 1530. Display 1530 may be a portion of electronic display layer 760 and may include a display pixel array 1625 that includes display pixels 1735. Sensing pixels 1725 may be sensor pixels 1800 as described in FIGURES 18-20 and their associated descriptions in U.S. Patent Application No. 15/724,027 entitled "Stacked Transparent Pixel Structures for Image Sensors," which is incorporated herein by reference in its entirety. Display pixels 1735 may be display pixels 100 as described in FIGURES 1-4 and their associated descriptions in U.S. Patent Application No. 15/724,004 entitled "Stacked Transparent Pixel Structures for Electronic Displays," which is incorporated herein by reference in its entirety.

[104] In some embodiments, plenoptic cell 1510 includes a transparent lenslet 1512 and cell walls 1514. Specifically, plenoptic cell 1510A includes transparent lenslet 1512A and cell walls 1514A, and plenoptic cell 1510B includes transparent lenslet 1512B and cell walls 1514B. In some embodiments, transparent lenslet 1512 contains a 3D shape with a collimating lens on one end of the 3D shape. For example, as illustrated in FIGURE 15, transparent lenslet 1512 may be a rectangular cuboid with a collimating lens on one end of the rectangular cuboid. In other embodiments, the 3D shape of transparent lenslet 1512 may be a triangular polyhedron, a pentagonal polyhedron, a hexagonal polyhedron, a heptagonal polyhedron, an

octagonal polyhedron, a cylinder, or any other appropriate shape. Each plenoptic cell 1510A includes an input field of view (FOV) 1610 (e.g., 30 degrees), and each plenoptic cell 1510B includes an output FOV 1620 (e.g., 30 degrees). In some embodiments, input FOV 1610 matches output FOV 1620 for corresponding plenoptic cells 1510.

[105] Transparent lenslet 1512 may be formed from any appropriate transparent optical material. For example, transparent lenslet 1512 may be formed from a polymer, silica glass, or sapphire. In some embodiments, transparent lenslet 1512 may be formed from a polymer such as polycarbonate or acrylic. In some embodiments, transparent lenslets 1512 may be replaced with waveguides and/or photonic crystals in order to capture and/or produce a light field.

[106] In general, cell walls 1514 are barriers to prevent optical crosstalk between adjacent plenoptic cells 1510. Cell walls 1514 may be formed from any appropriate material that is opaque to visible light when hardened. In some embodiments, cell walls 1514 are formed from a polymer. Preventing optical cross talk using cell walls 1514 is described in more detail below in reference to FIGURES 17A and 17C.

[107] In some embodiments, image sensor 1520 includes or is coupled to backplane circuitry 1630A, and display 1530 includes or is coupled to backplane circuitry 1630B. In general, backplane circuitry 1630A-B provides electrical connections to permit image data to flow from image sensor 1520 to display 1530. In some embodiments, backplane circuitry 1630A and backplane circuitry 1630B are the opposite sides of a single backplane. In some embodiments, backplane circuitry 1630A and backplane circuitry 1630B are circuit board 740.

[108] In some embodiments, a filter layer 1640 may be included on one or both ends of transparent lenslet 1512 in order to restrict the entry or exit of light to a specific incidence angle. For example, a first filter layer 1640A may be included on the convex end of transparent lenslet 1512, and/or a second filter layer 1640B may be included on the opposite end of transparent lenslet 1512. Similar to cell walls 1514, such a coating or film may also limit image bleed between adjacent transparent lenslets 1512 to an acceptable amount. Filter layer 1640 may be used in addition to or in place of cell walls 1514.

[109] FIGURES 17A-17C each illustrate a cross-sectional view of seven adjacent plenoptic cells 1510 for a sensor side microlens array 720A and a corresponding display side microlens array 720B. These figures show how incoming light fields 701 are captured by image sensors 1520 and electronically replicated on display 1530 to emit a virtually identical field of light. In FIGURE 17A, an incoming light field 1710 from objects directly in front of the sensor plenoptic cells 1510 are focused by the transparent lenslets 1512 of the sensor plenoptic cells 1510 onto center sensing pixels 1725. Corresponding light is then transmitted by corresponding center display pixels 1735 of corresponding display plenoptic cells 1510. The transmitted light is focused and emitted as emitted light field 1711 by the transparent lenslets 1512 of display plenoptic cells 1510. Emitted light field 1711 precisely matches the zero degree source light field (i.e., incoming light field 1710). In addition, emitted light rays striking cell walls 1514 at location 1740 that would otherwise penetrate adjacent display plenoptic cells 1510 are blocked by the opaque cell walls 1514, thereby preventing optical cross-talk.

[110] In FIGURE 17B, an incoming light field 1720 from objects fourteen degrees off the axis of sensor plenoptic cells 1510 are focused by the transparent lenslets 1512 of the sensor plenoptic cells 1510 onto top sensing pixels 1725. Corresponding light is then transmitted by corresponding opposite (i.e., bottom) display pixels 1735 of corresponding display plenoptic cells 1510. The transmitted light is focused and emitted as emitted light field 1721 by the transparent lenslets 1512 of display plenoptic cells 1510. Emitted light field 1721 precisely matches the 14 degree source light field (i.e., incoming light field 1720).

[111] In FIGURE 17C, an incoming light field 1730 from objects 25 degrees off the axis of sensor plenoptic cells 1510 are focused by the transparent lenslets 1512 of the sensor plenoptic cells 1510 entirely onto cell walls 1514. Because incoming light field 1730 is focused entirely onto cell walls 1514 of sensor plenoptic cells 1510 instead of sensing pixels 1725, no corresponding light is transmitted by corresponding display plenoptic cells 1510. In addition, incoming light rays striking cell walls 1514 at location 1750 that would otherwise penetrate adjacent sensor plenoptic cells 1510 are blocked by the opaque cell walls 1514, thereby preventing optical cross-talk.

[112] FIGURES 18A-18B illustrate a method of manufacturing the plenoptic cell assembly of FIGURE 15, according to certain embodiments. In FIGURE 18A, a microlens array (MLA) sheet 1810 is formed or obtained. MLA sheet 1810 includes a plurality of lenslets as illustrated. In FIGURE 18B, a plurality of grooves 1820 are cut around each of the plurality of lenslets of MLA sheet 1810 to a predetermined depth. In some embodiments, grooves 1820 may be cut using multiple passes to achieve the

desired depth. In some embodiments, grooves 1820 may be cut using laser ablation, etching, lithographic processes, or any other appropriate method. After grooves 1820 are cut to the desired depth, they are filled with a material configured to prevent light from bleeding through grooves 1820. In some embodiments, the material is any light absorbing (e.g., carbon nanotubes) or opaque material (e.g., a non-reflective opaque material or a tinted polymer) when hardened. The resulting plenoptic cell assembly after grooves 1820 are filled and allowed to harden is illustrated in FIGURES 20-21.

[113] FIGURES 19A-19B illustrate another method of manufacturing the plenoptic cell assembly of FIGURE 15, according to certain embodiments. In FIGURE 19A, a pre-formed lattice 1830 having voids 1840 is obtained or formed. Lattice 1830 is made of any suitable material as described above for cell walls 1514. Lattice 1830 may be formed from any suitable method including, but not limited to, additive manufacturing and ablation of cell matter.

[114] In FIGURE 19B, voids 1840 are filled with an optical polymer 1850. Optical polymer 1850 may be any suitable material as described above for transparent lenslet 1512. After voids 1840 are filled with optical polymer 1850, the final lens profile is created using molding or ablation. An example of the resulting plenoptic cell assembly after the lenses are formed is illustrated in FIGURES 20-21.

[115] FIGURE 22-23 illustrates a flexible circuit board 2210 that may be used as circuit board 740 by the emulated transparency assembly 710 of FIGURE 7, according to certain embodiments. Generally, wrapping electronics around a 3D shape such as spherical or semispherical surface is a non-trivial task. Though various examples of flexible and even stretchable

circuitry are currently available, there are several hurdles to overcome when positioning such electronics on a small radius (e.g., 30 - 60 mm) spherical or semispherical surface. For example, bending of flexible electronics substrates in one direction does not inherently indicate adaptability to compound curvature, as the torsional forces required for such curvature can be damaging to the thin films involved. As another example, questions remain about the degree of stretchability and lifetime of stretchable electronics currently available.

[116] To address the problems and limitations of current solutions, embodiments of the disclosure present a 3D (e.g., spherical or semispherical) electronics manufacturing method using a geodesic faceted approach consisting of an array of small, rigid surfaces built on a single flexible circuit. In some embodiments, the flexible circuit is cut to a specific net shape and then wrapped to a 3D shape (e.g., a spherical or semispherical shape) and locked into place to prevent wear and tear from repeated flexing. The method is especially useful to accommodate the narrow radii of curvature (e.g., 30-60 mm) necessary for head-mounted near-eye wrapped displays. In some embodiments, the assembly includes a single, foundational flexible printed circuitry layer, with rigid sensor and display arrays layered on opposite sides of the flexible circuit. The entire assembly including sensor and display layers may be manufactured by standard planar semiconductor processes (e.g., spin coatings, photolithography, etc.). The rigid electronics layers may be etched to form individual sensor and display units (i.e., "facets") and then connected to the flexible circuitry by connection pads and adhered through patterned conductive and non-conductive adhesives. This permits the flexible circuitry to fold slightly at the edges between the rigid facets. In some

embodiments, following planar manufacturing, the fully cured and functional electronic stack is formed to the desired final 3D shape using one side of a final rigid polymer casing as a mold. In this way, the arrays of rigid electronics facets are not deformed but simply fall into place in their mold, with the flexible circuitry bending at defined creases/gaps to match the faceted interior of the casing. The assembly may be finally capped and sealed using an opposite matching side of the rigid casing.

[117] Embodiments of the disclosure are not limited to only spherical or semispherical shapes, although such shapes are certainly contemplated. The disclosed embodiments may be formed into any compound curvature or any other revolved shape. Furthermore, the disclosed embodiments may be formed into any non-uniform curvature, as well as non-curved (i.e., flat) surfaces.

[118] FIGURE 22 illustrates flexible circuit board 2210 in two different states: a flat flexible circuit board 2210A and a 3D-shaped flexible circuit board 2210B. Flexible circuit board 2210 includes facet locations 2220, which in general are locations in which facets (e.g., sensor facets 3735, display facets 2665, or logic facets 2655 discussed below) may be installed on flexible circuit board 2210. In some embodiments, flexible circuit board 2210 includes gaps 2215. As illustrated in the bottom portion of FIGURE 22, when flexible circuit board 2210 is flat, at least some of facet location 2220 are separated from one or more adjacent facet locations 2220 by one or more gaps 2215. As illustrated in the top portion of FIGURE 22, when flexible circuit board 2210 is formed into a 3D shape, gaps 2215 may be substantially eliminated, thereby forming a continuous surface across at least some of the facets that are coupled at

facet locations 2220 (e.g., a continuous sensing surface across multiple sensor facets 3735 or a continuous display surface across multiple display facets 2665).

[119] In general, facet locations 2220 may have any shape. In some embodiments, facet locations 2220 are in the shape of a polygon (e.g., a triangle, square, rectangle, pentagon, hexagon, heptagon, or octagon). In some embodiments, facet locations 2220 are all identical. In other embodiments, however, facet locations 2220 all share the same polygon shape (e.g., all are hexagonal), but have different dimensions. In some embodiments, facet locations 2220 have heterogeneous shapes (e.g., some are rectangular and some are hexagonal). Any appropriate shape of facet locations 2220 may be used.

[120] In some embodiments, facet locations 2220 are arranged in columns 2201. In some embodiments, facet locations 2220 are additionally or alternatively arranged in rows 2202. While a specific pattern of facet locations 2220 is illustrated, any appropriate pattern of facet locations 2220 may be used.

[121] FIGURE 23 illustrates additional details of flexible circuit board 2210, according to certain embodiments. In some embodiments, each facet location 2220 includes pads and/or vias for coupling sensor or display facets to flexible circuit board 2210. As an example, some embodiments of flexible circuit board 2210 include BGA pads 2240 at each facet location 2220. Any appropriate pattern and number of pads/vias may be included at each facet location 2220.

[122] In general, each particular facet location 2220 is configured to transmit signals between a particular sensor facet coupled to the particular facet location and a particular display facet coupled to an opposite side of the particular facet location. For example, a particular facet location 2220

may have a sensor facet 3735 coupled to one side, and a display facet 2665 coupled to its opposite side. The particular facet location 2220 provides the necessary electrical connections to permit signals from the sensor facet 3735 to travel directly to the display facet 2665, thereby enabling the display facet 2665 to display light that corresponds to light captured by the sensor facet 3735.

[123] In some embodiments, wire traces 2230 are included on flexible circuit board 2210 to electrically connect facet locations 2220. For example, wire traces 2230 may connect to interconnection pads 2250 of each facet location 2220 in order to electrically connect adjacent facet locations 2220. In some embodiments, facet locations 2220 are serially connected via wire traces 2230. For example, FIGURE 24 illustrates a serial data flow through flexible circuit board 2210, according to certain embodiments. In this example, each facet location 2220 is assigned a unique identifier (e.g., "1," "2," and so on), and data flows serially through facet locations 2220 via wire traces 2230 as illustrated. In this manner, each facet location 2220 may be addressed by a single processor or logic unit using its unique identifier. Any appropriate addressing scheme and data flow pattern may be used.

[124] FIGURE 25 illustrates a method 2500 of manufacturing an electronic assembly using flexible circuit board 2210 of FIGURE 22, according to certain embodiments. At step 2510, a plurality of facet locations are formed on a flexible circuit board. In some embodiments, the facet locations are facet locations 2220, and the flexible circuit board is flexible circuit board 2210. Each facet location corresponds to one of a plurality of sensor facets and one of a plurality of display facets. The sensor facets may be sensor facets 3735, and the display facets may be display facets 2665. In some embodiments, the plurality of facet locations are arranged into a plurality of facet columns such as columns 2201. In some embodiments, the plurality of facet locations are additionally or alternatively arranged into a plurality of facet rows such as rows 2202.

[125] At step 2520, the flexible circuit board of step 2510 is cut or otherwise shaped into a pattern that permits the flexible circuit board to be later formed into a 3D shape such as a spherical or semispherical shape. When the flexible circuit board is flat, at least some of the facet locations are separated from one or more adjacent facet locations by a plurality of gaps such as gaps 2215. When the flexible circuit board is formed into the 3D shape, the plurality of gaps are substantially eliminated.

[126] At step 2530, the electronic assembly is assembled by coupling a first plurality of rigid facets to a first side of the flexible circuit board. The first plurality of rigid facets may be sensor facets 3735 or display facets 2665. Each rigid facet is coupled to a respective one of the facet locations. In some embodiments, the first plurality of rigid facets are coupled to connection pads on the first side of the

flexible circuit board using patterned conductive and non-conductive adhesives.

[127] In some embodiments, the first plurality of rigid facets of step 2530 are rigid sensor facets such as sensor facet 3735, and method 2500 further includes coupling a plurality of rigid display facets such as display facet 2665 to a second side of the flexible circuit board that is opposite the first side. In this case, each particular facet location is configured to transmit signals between a particular rigid sensor facet electrically coupled to the particular facet location and a particular rigid display facet electrically coupled to the same particular facet location. This permits light to be displayed from the particular rigid display facet that corresponds to light captured by the corresponding rigid sensor facet.

[128] At step 2540, the assembled electronic assembly is formed into the desired 3D shape. In some embodiments, this step involves placing the flexible circuit board with its coupled rigid facets into one side of a rigid casing that is in the desired shape. This allows the rigid facets to fall into defined spaces in the casing and the flexible circuit board to bend at defined creases/gaps between the rigid facets. After placing the flexible circuit board with its coupled rigid facets into one side of the rigid casing, an opposite matching side of the rigid casing may be attached to the first side, thereby sealing the assembly into the desired shape.

[129] Particular embodiments may repeat one or more steps of method 2500, where appropriate. Although this disclosure describes and illustrates particular steps of method 2500 as occurring in a particular order, this disclosure contemplates any suitable steps of method 2500 occurring in any suitable order (e.g., any temporal order). Moreover, although this

disclosure describes and illustrates an example method of manufacturing an electronic assembly using flexible circuit board, this disclosure contemplates any suitable method of manufacturing an electronic assembly using flexible circuit board, which may include all, some, or none of the steps of method 2500, where appropriate. Furthermore, although this disclosure describes and illustrates particular components, devices, or systems carrying out particular steps of method 2500, this disclosure contemplates any suitable combination of any suitable components, devices, or systems carrying out any suitable steps of method 2500.

[130] FIGURES 26-36 illustrate distributed multi-screen arrays for high density displays, according to certain embodiments. In general, to provide a near-eye display capable of emulating the entire visual field of a single human eye, a high dynamic range image display with a resolution orders of magnitude greater than current common display screens is required. Such displays should be able to provide a light field display with enough angular and spatial resolution to accommodate 20/20 human visual acuity. This is an enormous amount of information, equating to a total horizontal pixel count of 100K to 200K. These displays should also wrap around the entire field of vision of one human eye (approximately 160° horizontally and 130° vertically). For rendering binocular vision, a pair of such displays spanning the entirety of a curved surface around each eye would be necessary. Typical displays available today, however, are unable to meet these requirements.

[131] To address these and other limitations of current displays, embodiments of the disclosure provide an array of small, high-resolution micro displays (e.g., display facets 2665) of custom sizes and shapes, all of which are formed and

then assembled on a larger, flexible circuit board 2210 that may be formed into a 3D shape (e.g., a semispherical surface). The micro displays may be mounted to the interior side of semispherical circuitry, where another layer containing an array of TFT logic units (e.g., logic units 755) may be included to handle all the power and signal management. Typically, one logic unit 755 may be included for each micro display. Each micro display operates as a discreet unit, displaying data from the logic unit behind it. Any additional information (e.g., such as external video for AR, VR, or MR applications) may be passed to the entire array via a central control processor. In some embodiments, the external data signal progresses serially from one micro display to the next as a packed multiplex stream, while the TFT logic unit for each display determines the source and section of the signal to read. This allows each unit to act independently of any other display, providing a large array of many high-resolution displays with unique content on each, such that the whole assembly together forms essentially a single extremely high-resolution display.

[132] To fulfill the requirements of resolution, color clarity, and luminance output, each micro display may have a unique, high performance pixel architecture. For example, each micro display screen may include arrays of display pixels 100 as described in FIGURES 1-4 and their associated descriptions in U.S. Patent Application No. 15/724,004 entitled "Stacked Transparent Pixel Structures for Electronic Displays," which is incorporated herein by reference in its entirety. The micro display screens may be assembled on the same substrate using any appropriate method. Such simultaneous manufacturing using standard semiconductor layering and photolithographic processes virtually eliminates the overhead and costs associated with

production and packaging of many individual screens, greatly improving affordability.

[133] FIGURE 26 illustrates a cut-away view of a curved multi-display array 2600, according to certain embodiments. FIGURE 26 is essentially the back side of flexible circuit board 2210B of FIGURE 22 with the addition of logic facets 2655 and display facets 2665 coupled to flexible circuit board 2210B at facet locations 2220. In general, each logic facet 2655 is an individual logic unit 755 from logic unit layer 750. Similarly, each display facet 2665 is an individual display unit 765 from display layer 760 coupled with a portion of microlens array 720.

[134] In some embodiments, each individual logic facet 2655 is coupled to flexible circuit board 2210, and each individual display facet 2665 is then coupled to one of the logic facets 2655. In other embodiments, each logic facet 2655 is first coupled one of the display facets 2665, and the combined facet is then coupled to flexible circuit board 2210. In such embodiments, the combined logic facet 2655 and display facet 2665 may be referred to as a display facet 2665 for simplicity. As used herein, "display facet" may refer to both embodiments (i.e., an individual display facet 2665 or a combination of a display facet 2665 with a logic facet 2655).

[135] In general, each display facet 2665 can be individually addressed (e.g., by a central control processor not pictured), and a collection of display facets 2665 may represent a dynamic, heterogeneous collection forming a singular collective. In other words, multi-display array 2600 provides a tiled electronic display system showing imagery through individual display facets 2665 that together form a complete whole. Each individual display facet 2665 is capable of providing multiple different display resolutions and can be

customized on the fly to run a different resolution, color range, frame rate, etc. For example, one display facet 2665 may have a 512x512 display resolution while an adjacent display facet 2665 (of equal size) has a 128x128 display resolution, wherein the former represents a higher concentration of imagery data. In this example, these two displays are heterogeneous, but are individually controllable and work in unison to form a singular display image.

[136] The overall collection of display facets 2665 can follow any curved or flat surface structure. For example, display facets 2665 may be formed into a semispherical surface, a cylindrical surface, an oblong spherical surface, or any other shaped surface.

[137] Logic facets 2655 and display facet 2665 may be in any appropriate shape. In some embodiments, the shapes of logic facets 2655 and display facets 2665 match each other and the shape of facet locations 2220. In some embodiments, logic facets 2655 and display facets 2665 are in the shape of a polygon such as a triangle, a quadrilateral, a pentagon, a hexagon, a heptagon, or an octagon. In some embodiments, some or all of logic facets 2655 and display facets 2665 have non-polygonal shapes. For example, display facets 2665 on the edges of flexible circuit board 2210 may not be polygonal as they may have curved cutoffs so as to enhance the aesthetic of the overall assembly.

[138] In addition to having a selectable/controllable display resolution, each display facet 2665 may in some embodiments also have a selectable color range from a plurality of color ranges and/or a selectable frame rate from a plurality of frame rates. In such embodiments, the display facets 2665 of a particular flexible circuit board 2210 are configurable to

provide heterogeneous frame rates and heterogeneous color range. For example, one display facet 2665 may have a particular color range while another display facet 2665 has a different color range. Similarly, one display facet 2665 may have a particular frame rate while another display facet 2665 has a different frame rate.

[139] FIGURE 27 illustrates an exploded view of the curved multi-display array 2600 of FIGURE 26, and FIGURES 28-29 illustrate additional details of logic facet 2655 and display facet 2665, according to certain embodiments. As illustrated in these figures, each logic facet 2655 may include interconnections pads 2850 that may be electrically coupled to interconnection pads 2250 of adjacent logic facets 2655. This may enable display facets 2665 to be serially coupled via wire traces 2230. In addition, each logic facet 2655 may include pads 2840 in a pattern that matches pads 2940 on the back side of display facet 2665. This permits logic facet 2655 and display facet 2665 to be coupled together using any appropriate technique in the art. In some embodiments, pads 2840 and pads 2940 are BGA pads or any other appropriate surface-mounting pads.

[140] FIGURES 30 and 32 illustrate a back side of flexible circuit board 2210 of FIGURE 22, and show similar details as described in reference to FIGURE 23. FIGURES 31 and 33 illustrate a serial data flow through flexible circuit board 2210, and show similar details as described in reference to FIGURE 24. FIGURE 34 illustrates an array of logic facets 2655 that have been formed into a semispherical shape, according to certain embodiments. In this figure, flexible circuit board 2210 and display facet 2665 have been removed for clarity. FIGURE 35 illustrates communications between the logic facets

2655 of FIGURE 34, according to certain embodiments. As illustrated in this figure, each logic facet 2655 may communicate with adjacent logic facets 2655 using interconnections pads 2850. In addition, each logic facet 2655 may have a unique identification as illustrated in FIGURE 35. This permits each logic facet 2655 to be uniquely addressed by, for example, a central processing unit.

[141] FIGURE 36 illustrates a method 3600 of manufacturing the curved multi-display array of FIGURE 26, according to certain embodiments. Method 3600 may begin in step 3610 where a plurality of facet locations are formed on a circuit board. In some embodiments, the facet locations are facet locations 2220 and the circuit board is flexible circuit board 2210. In some embodiments, each facet location corresponds to one of a plurality of display facets such as display facets 2665.

[142] At step 3620, the flexible circuit board is cut or otherwise formed into a pattern that permits the flexible circuit board to be later formed into a 3D shape. When the flexible circuit board is flat, at least some of the facet locations are separated from one or more adjacent facet locations by a plurality of gaps such as gaps 2215. When the flexible circuit board is formed into the 3D shape, the plurality of gaps are substantially eliminated.

[143] At step 3630, a plurality of logic facets are coupled to a first side of the flexible circuit board. Each logic facet is coupled to a respective one of the facet locations of step 3610. At step 3640, a plurality of display facets are coupled to a respective one of the plurality of logic facets of step 3630. In alternate embodiments, the display facets may be mounted to the logic facets of step 3630 at the wafer level prior to coupling the logic facets to the first side of the

flexible circuit board. At step 3650, the assembled electronic display assembly is formed into the 3D shape. In some embodiments, this step may be similar to step 2540 of method 2500 described above. After step 3650, method 3600 may end.

[144] Particular embodiments may repeat one or more steps of method 3600, where appropriate. Although this disclosure describes and illustrates particular steps of method 3600 as occurring in a particular order, this disclosure contemplates any suitable steps of method 3600 occurring in any suitable order (e.g., any temporal order). Moreover, although this disclosure describes and illustrates an example method of manufacturing a curved multi-display array, this disclosure contemplates any suitable method of manufacturing a curved multi-display array, which may include all, some, or none of the steps of method 3600, where appropriate. Furthermore, although this disclosure describes and illustrates particular components, devices, or systems carrying out particular steps of method 3600, this disclosure contemplates any suitable combination of any suitable components, devices, or systems carrying out any suitable steps of method 3600.

[145] FIGURES 37-42 illustrate a distributed multi-aperture camera array 3700, according to certain embodiments. In general, to capture the full light field of the entire visual field of a single human eye, a large, high dynamic range image sensor with a resolution much higher than currently available is needed. Such an image sensor would enable a light field camera with enough angular and spatial resolution to accommodate 20/20 human visual acuity. This is an enormous amount of information, equating to a total horizontal pixel count of 100K to 200K. This multi-aperture image sensor must also wrap around the entire field of vision of one human eye (approximately 160°

horizontally and 130° vertically). For imaging binocular vision, a pair of such cameras spanning the entirety of a curved surface around each eye are necessary. Typical image sensor assemblies available today are unable to meet these requirements.

[146] To overcome these and other limitations of typical image sensors, embodiments of the disclosure provide an array of small image sensors of custom sizes and shapes, all of which are assembled on a larger, flexible circuit board 2210 that is formed to a 3D (e.g., semi-spherical) shape. The image sensors (e.g., sensor facets 3735) are mounted to the exterior side of flexible circuit board 2210, where another layer containing an array of TFT logic units (e.g., logic units 755) may be provided to handle all the power and signal management – one logic unit for each display. Each image sensor operates as a discrete unit passing readout data to the logic unit behind it (in embodiments that include logic units), where it is handled and routed accordingly (e.g., to a corresponding display facet 2665 in some embodiments). This allows each sensor facet 3735 to act independently of any other sensor facet 3735, providing a large array of many apertures capturing unique content on each, such that the whole assembly essentially becomes a seamless, very high resolution, multi-node camera. It should be noted that while image sensors may pass data to their paired logic units in some embodiments, the functionality of the image sensors themselves do not necessarily require logic unit coupling.

[147] To fulfill the requirements of resolution, color clarity, and luminance output, each micro sensor may have a unique, high performance pixel architecture. For example, each micro sensor may include arrays of sensor pixels 1800 as described in FIGURES 18-20 and their associated descriptions in U.S. Patent Application No. 15/724,027 entitled "Stacked

Transparent Pixel Structures for Image Sensors," which is incorporated herein by reference in its entirety. The micro sensor may be assembled on the same substrate using any appropriate method. Such simultaneous manufacturing using standard semiconductor layering and photolithographic processes virtually eliminates the overhead and costs associated with production and packaging of many individual screens, greatly improving affordability.

[148] Another characteristic of certain embodiments of distributed multi-aperture camera array 3700 is built-in depth perception based on parallax between different plenoptic cells. Imagery produced by cells on opposite sides of a given sensor may be used to calculate the offset of image detail, where offset distance directly correlates with proximity of the detail to the sensor surface. This scene information may be used by a central processor when overlaying any augmented video signal, resulting in AR/MR content placed in front of the viewer at the appropriate depth. The information can also be used for a variety of artificial focus blurring and depth-sensing tasks, including simulated depth of field, spatial edge detection, and other visual effects.

[149] FIGURE 37 illustrates a cut-away view of distributed multi-aperture camera array 3700, according to certain embodiments. FIGURE 37 is essentially the flexible circuit board 2210B of FIGURE 22 with the addition of sensor facet 3735 coupled to flexible circuit board 2210B at facet locations 2220. In some embodiments, each sensor facet 3735 is an individual sensor unit 735 from image sensor layer 730.

[150] In some embodiments, each individual sensor facet 3735 is coupled to flexible circuit board 2210. In other embodiments, each individual sensor facet 3735 is coupled to one

of the logic facets 2655 that has been coupled to flexible circuit board 2210. In other embodiments, each logic facet 2655 is first coupled one of the sensor facets 3735, and the combined facet is then coupled to flexible circuit board 2210. In such embodiments, the combined logic facet 2655 and sensor facet 3735 may be referred to as a sensor facet 3735 for simplicity. As used herein, "sensor facet" may refer to both embodiments (i.e., an individual sensor facet 3735 or a combination of a sensor facet 3735 with a logic facet 2655).

[151] In general, each sensor facet 3735 can be individually addressed (e.g., by a central control processor not pictured), and a collection of sensor facets 3735 may represent a dynamic, heterogeneous collection forming a singular collective. In other words, distributed multi-aperture camera array 3700 provides a tiled electronic sensor system providing imagery captured through individual sensor facets 3735 that together form a complete whole. Each individual sensor facets 3735 is capable of capturing images at multiple different resolutions and can be customized on the fly to capture a different resolution, color range, frame rate, etc. For example, one sensor facet 3735 may have a 512x512 capture resolution while an adjacent sensor facet 3735 (of equal size) has a 128x128 capture resolution, wherein the former represents a higher concentration of imagery data. In this example, these two sensors are heterogeneous, but are individually controllable and work in unison to capture a singular light field.

[152] The overall collection of sensor facets 3735 can follow any curved or flat surface structure. For example, sensor facets 3735 may be formed into a semispherical surface, a cylindrical surface, an oblong spherical surface, or any other shaped surface.

[153] Sensor facets 3735 may be in any appropriate shape. In some embodiments, the shapes of sensor facets 3735 match the shapes of display facets 2665 and the shape of facet locations 2220. In some embodiments, sensor facets 3735 are in the shape of a polygon such as a triangle, a quadrilateral, a pentagon, a hexagon, a heptagon, or an octagon. In some embodiments, some or all of sensor facets 3735 have non-polygonal shapes. For example, sensor facets 3735 on the edges of flexible circuit board 2210 may not be polygonal as they may have curved cutoffs so as to enhance the aesthetic of the overall assembly.

[154] In addition to having a selectable/controllable resolution, each sensor facets 3735 may in some embodiments also have a selectable color range from a plurality of color ranges and/or a selectable frame rate from a plurality of frame rates. In such embodiments, the sensor facets 3735 of a particular flexible circuit board 2210 are configurable to provide heterogeneous frame rates and heterogeneous color range. For example, one sensor facet 3735 may have a particular color range while another sensor facet 3735 has a different color range. Similarly, one sensor facet 3735 may have a particular frame rate while another sensor facet 3735 has a different frame rate.

[155] FIGURES 38-39 illustrate exploded views of the distributed multi-aperture camera array 3700 of FIGURE 37, according to certain embodiments. As illustrated in these figures, each sensor facet 3735 may include pads 3940 in a pattern that matches pads 2240 on flexible circuit board 2210 or pads 2940 on logic facet 2655. This permits sensor facet 3735 to be coupled to logic facet 2655 or flexible circuit board 2210 using any appropriate technique in the art. In some embodiments, pads 3940 are BGA pads or any other appropriate surface-mounting pads. FIGURES 40-40 illustrate similar views

of flexible circuit board 2210 as shown in FIGURES 23-24, except that flexible circuit board 2210 has been formed into a 3D shape.

[156] FIGURE 42 illustrates a method 4200 of manufacturing distributed multi-aperture camera array 3700, according to certain embodiments. Method 4200 may begin in step 4210 where a plurality of facet locations are formed on a circuit board. In some embodiments, the facet locations are facet locations 2220 and the circuit board is flexible circuit board 2210. In some embodiments, each facet location corresponds to one of a plurality of sensor facets such as sensor facets 3735.

[157] At step 4220, the flexible circuit board is cut or otherwise formed into a pattern that permits the flexible circuit board to be later formed into a 3D shape. When the flexible circuit board is flat, at least some of the facet locations are separated from one or more adjacent facet locations by a plurality of gaps such as gaps 2215. When the flexible circuit board is formed into the 3D shape, the plurality of gaps are substantially eliminated.

[158] At step 4230, a plurality of sensor facets are coupled to a first side of the flexible circuit board. Each sensor facet is coupled to a respective one of the facet locations of step 4210. At step 4240, the assembled electronic camera assembly is formed into the 3D shape. In some embodiments, this step may be similar to step 2540 of method 2500 described above. After step 4240, method 4200 may end.

[159] Particular embodiments may repeat one or more steps of method 4200, where appropriate. Although this disclosure describes and illustrates particular steps of method 4200 as occurring in a particular order, this disclosure contemplates any suitable steps of method 4200 occurring in any suitable order (e.g., any temporal order). Moreover, although this

disclosure describes and illustrates an example method of manufacturing a distributed multi-aperture camera array, this disclosure contemplates any suitable method of manufacturing a distributed multi-aperture camera array, which may include all, some, or none of the steps of method 4200, where appropriate. Furthermore, although this disclosure describes and illustrates particular components, devices, or systems carrying out particular steps of method 4200, this disclosure contemplates any suitable combination of any suitable components, devices, or systems carrying out any suitable steps of method 4200.

[160] FIGURES 43-46 illustrates perspective views of a near-eye pupil-tracking surface 4300 worn by a viewer, according to certain embodiments. In general, near-eye pupil-tracking surface 4300 includes an array of facets 4305 that may be arranged in any appropriate pattern (e.g., a plurality of facet columns and a plurality of facet rows as illustrated). In some embodiments, facets 4305 are arranged in a grid pattern as illustrated. Facets 4305 are coupled to a side of near-eye pupil-tracking surface 4300 that faces an eye 4301 of the viewer (e.g., eye 4301A or 4301B). Facets 4305 transmit light towards an eye 4301 as the viewer focuses on a target object 4310. As the viewer looks toward target object 4310 along a view axis 4330 (e.g., view axis 4330A or 4330B), the light transmitted by facets 4305 towards eye 4301 will be reflected back towards near-eye pupil-tracking surface 4300 by eye 4301 as a cone of retro-reflected light 4320 (e.g., cones 4320A or 4320B). Cone of retro-reflected light 4320 will be centered upon view axis 4330 and will strike the inside surface of near-eye pupil-tracking surface 4300 and be detected by facets 4305. As illustrated in FIGURE 43, cone of retro-reflected light 4320 will intersect near-eye pupil-tracking surface 4300 at a cone

intersection 4340 (e.g., cone intersection 4340A or 4340B). In some embodiments, any facets 4305 that detect any portion of cone of retro-reflected light 4320 (i.e., facets 4305 that intersect with any portion of cone intersection 4340) will correspond to a direction of gaze of eye 4301. In some embodiments, different portions of cone of retro-reflected light 4320 are used to determine a direction of gaze of eye 4301. For example, the direction of gaze of eye 4301 may be based on an intensity of the reflection and the overall coverage area (i.e., the total combination of which facets - or which portions of which facets - are receiving reflection is used to determine the center of the gaze). As illustrated in FIGURE 44, the highlighted facets 4305 correspond to a direction of gaze of each eye 4301 and include a center-of-gaze facet 4305A and adjacent facets 4305B. As a result, near-eye pupil-tracking surface 4300 may accurately detect where a viewer is currently looking without causing any obstructions to the viewer's vision and without requiring expensive and bulky eye-tracking cameras.

[161] FIGURES 43-44 illustrate a viewer focusing on a target object 4310 that is directly in front of the viewer. As a result, the center-of-gaze facet 4305A for each near-eye pupil-tracking surface 4300 is in approximately the same location on near-eye pupil-tracking surface 4300 as illustrated in FIGURE 44. FIGURES 45-46 are similar to FIGURES 43-44 except that the viewer is focusing on a target object 4310 that is not directly in front of the viewer. In these examples, the center-of-gaze facet 4305A for each near-eye pupil-tracking surface 4300 is not in the same location on both near-eye pupil-tracking surfaces 4300. For example, as illustrated in FIGURE 45, the center-of-gaze facet 4305A for each near-eye pupil-tracking surface 4300 has been shifted to the right on both near-eye

pupil-tracking surfaces 4300 since target object 4310 has shifted to the right. Similarly, as illustrated in FIGURE 46, the center-of-gaze facet 4305A for each near-eye pupil-tracking surface 4300 has been shifted to the left on both near-eye pupil-tracking surfaces 4300 since target object 4310 has shifted to the left.

[162] FIGURES 47A-47B illustrate cross-sectional views of near-eye pupil-tracking surface 4300, according to certain embodiments. As illustrated in these figures, facets 4305 each include one or more emitters 4730 and one or more receptors 4740. Emitters 4730 and receptors 4740 may be interleaved or layered. Each emitter 4730 is capable of emitting light 4710 (e.g., visible, non-visible, IR, or near-IR), and each receptor 4740 is capable of detecting any reflected light 4720 that is reflected back towards near-eye pupil-tracking surface 4300 by eye 4301. While a specific number and pattern of emitters 4730 and receptors 4740 are illustrated, any appropriate number and pattern of emitters 4730 and receptors 4740 may be used.

[163] In general, facets 4305 are individual rigid or flexible electronic components that are capable of transmitting and detecting light. In some embodiments, facets 4305 are display facets 2665 (or are similar in design/shape/etc. to display facets 2665) described above. In some embodiments, each facet 4305 includes a planar face 4750. In embodiments where near-eye pupil-tracking surface 4300 has a curved shape that is concentric with eye 4301 (i.e., the curved shape of near-eye pupil-tracking surface 4300 is roughly centered on a center of eye 4760 when near-eye pupil-tracking surface 4300 is being worn by the viewer), each planar face 4750 may be normal to a line pointing towards center of eye 4760. In general, center of eye 4760 is a geometric area about which eye 4301 rotates. When

near-eye pupil-tracking surface 4300 has a shape that is designed to be centered on center of eye 4760, the planar faces 4750 of facets 4305 remain normal to lines pointing towards center of eye 4760 regardless of where eye 4301 is pointed.

[164] In some embodiments, each facet 4305 is coupled to a circuit board such as circuit board 740 described above. In some embodiments, circuit board 740 is a flexible circuit board that is formed into a curved shape that is configured to be substantially concentric with eye 4301. In other embodiments, circuit board 740 (and the overall near-eye pupil-tracking surface 4300) is curved but is not concentric with eye 4301. Such embodiments are described below in reference to FIGURES 49A-49B. In still other embodiments, circuit board 740 (and the overall near-eye pupil-tracking surface 4300) is flat. Such embodiments are described below in reference to FIGURES 50A-50B.

[165] In some embodiments, facets 4305 are not coupled directly to circuit board 740. Instead, each facet 4305 may be coupled to a respective logic facet such as logic facets 2655 described above. This may allow each facet 4305 to be individually addressable as described above with respect to display facets 2665. This may allow the detection of a center of gaze of the viewer (i.e., center-of-gaze facet 4305A).

[166] In some embodiments, each emitter 4730 and each receptor 4740 is an individual pixel or stand-alone component coupled to facet 4305. In other embodiments, facets 4305 may be display facets 2665, and the emitters 4730 and receptors 4740 may be individual layers or subpixels within display pixels 1735 of the display facets 2665. For example, the pixels may be display pixels 100, emitters 4730 may be IR emitter subpixels 2210, and receptors 4740 may be IR detector subpixels 2610 as described in FIGURES 1-4 and 22-29 and their associated

descriptions in U.S. Patent Application No. 15/808,368 entitled "Display-Integrated Infrared Emitter and Sensor Structures," which is incorporated herein by reference in its entirety.

[167] In general, a human eye 4301 includes a retina 4701, a cornea 4702, a pupil opening 4703, and a crystalline lens 4704. While the individual dimensions of these components of eye 4301 may vary from human to human, the variance is generally small and within a known range. For example, a typical eye 4301 will have a pupil opening 4703 that is approximately 4.4mm in diameter, but this may vary by ambient light intensity and not just biological distinctions. This results in a cone of retro-reflected light 4320 from retina 4701 that is typically around 12 degrees.

[168] Facets 4305 may be in any appropriate shape. In some embodiments, facets 4305 are coupled to facet locations 2220 on circuit board 740, and the shapes of facets 4305 match the shapes of facet locations 2220. In some embodiments, facets 4305 are in the shape of a polygon such as a triangle, a quadrilateral, a pentagon, a hexagon, a heptagon, or an octagon. In some embodiments, some or all of facets 4305 have non-polygonal shapes. For example, facets 4305 on the edges of near-eye pupil-tracking surface 4300 may not be polygonal as they may have curved cutoffs so as to enhance the aesthetics of the overall assembly.

[169] FIGURES 48A-50B illustrate cones of retinal retro-reflected light 4320 as detected by various embodiments of near-eye pupil-tracking surface 4300. FIGURES 48A-48B illustrate cones of retinal retro-reflected light 4320 as detected by an ocular-concentric tracking surface 4300, FIGURES 49A-49B illustrate cones of retinal retro-reflected light 4320 as detected by a curved, non-ocular-concentric tracking surface

4900, and FIGURES 50A-50B illustrate cones of retinal retro-reflected light 4320 as detected by a flat tracking surface 5000, according to certain embodiments. In reference to FIGURES 48A-50B, suppose a light-sensitive surface S (representing a possibly curved near-eye pupil-tracking surface 4300), which is finite and does not pass through the origin. Now suppose that there is some vector $\vec{D}$ of unit length (representing the central direction of light emission from the origin). Finally, suppose that light is emitted as a one-sided cone centered on the origin, pointing in the direction $\vec{D}$, and having an intensity value at unit distance of:

$$I\ (\cos\ \theta)$$

pointing in a direction which forms an angle θ with $\vec{D}$. That is, there is an eye at the origin of the system and a detector that is outside of the eye. The retroreflected light from the eye **also may have some arbitrary falloff rate given by I(cos θ).** Given some parameterization $\vec{r}(s, t)$ of S for some region in (s, t)-space, let $\vec{n}\ (s, t)$ denote the unit length normal vector to the surface. Using the shorthand $r = |\vec{r}|$, take $\vec{u} = \frac{\vec{r}}{r}$. Since the percieved intensity of incoming light to a surface is $|I\vec{u} \cdot \vec{n}|$ where $I\vec{u}$ represents the direction and intensity of the incoming light and $\vec{n}$ represents the normal vector to the surface, the detected intensity of light at a point $\vec{r}$ on S is $I_d = I\ (\vec{u} \cdot \vec{D})\ \vec{u} \cdot \vec{n}\ / r^2$. But the sensors which detect this light are distributed at (potentially) varying densities throughout S. Thus, $\rho\ (s, t)$ will be defined to be the number of sensors per square unit of S picking up light around $\vec{r}$. Now, assuming that S does not cast a shadow onto itself, the total light detected by the sensors is

$$\iint_S I_d \rho dS.$$

where I_d is the theoretical amount of light that is detected by any given sensor on the surface, $\vec{r}$ is the point at which it is detected and $\vec{n}$ is the normal of the detection surface (not necessarily pointing toward the center of the eye).

[170] Next, it is desirable to assign a vector $\vec{v}$ (s, t) to each sensor such that

$$\vec{V} \coloneqq \iint_S I_d \rho \vec{v} dS = c\vec{D}$$

for some positive value c. This equation reveals that simply by multiplying the detected value of light by a hardcoded vector in each sensor and then adding all of those products together across the entire sensor array (e.g., the sensor surface), the resultant vector has the same direction as the original direction of view. Taking $\vec{v} = \frac{\vec{u}}{\rho}$ and assuming that all of the light actually hits the surface S, $\vec{V}$ can be simplified as follows:

$$\vec{V} \coloneqq \iint_S I_d \rho \vec{v} dS$$

$$= \iint_S \frac{\left(I(\vec{u} \cdot \vec{D})\vec{u} \cdot \vec{n}\right)}{r^2} \rho \frac{\vec{u}}{\rho} dS$$

$$= \iint_S I(\vec{u} \cdot \vec{D}) \frac{\vec{u} \cdot \vec{n}}{r^2} \vec{u} dS$$

[171] Some perpendicular unit vector to $\vec{D}$ can be found and called $\vec{D}^{\perp}$, then θ and $\emptyset$ can be defined to parameterize the

unit sphere so that $\vec{u} = \vec{D}\cos\theta + (\sin\theta)\left(\vec{D}^{\perp}\cos\emptyset + \left(\vec{D} \times \vec{D}^{\perp}\right)\sin\emptyset\right)$. Observe that $\vec{r} = |\vec{r}|\,\vec{u}$. This leads to the following computations:

$$\vec{r}_\theta \times \vec{r}_\emptyset = (r\vec{u}_\theta + r_\theta\vec{u}) \times (r\vec{u}_\emptyset + r_\emptyset\vec{u})$$
$$= r\vec{u}_\theta \times r\vec{u}_\emptyset + r\vec{u}_\theta \times r_\emptyset\vec{u} + r_\theta\vec{u} \times r\vec{u}_\emptyset + r_\theta\vec{u} \times r_\emptyset\vec{u}$$
$$= r^2(\vec{u}_\theta \times \vec{u}_\emptyset) + r\vec{u}_\theta \times r_\emptyset\vec{u} - r\vec{u}_\emptyset \times r_\theta\vec{u} + 0$$
$$= r^2(\vec{u}_\theta \times \vec{u}_\emptyset) + r(r_\emptyset\vec{u}_\theta - r_\theta\vec{u}_\emptyset) \times \vec{u}$$

Here, a system of coordinates in terms of the retroreflected cone is established: θ represents the angle away from the cone axis and $\emptyset$ represents the angle around the cone's axis. Observe that since $\vec{n}$ is the unit normal to S, $\vec{n} = \frac{\vec{r}_\theta \times \vec{r}_\emptyset}{|\vec{r}_\theta \times \vec{r}_\emptyset|}$. Therefore,

$$\frac{\vec{u}\cdot\vec{n}}{r^2} = \frac{\vec{u}\cdot(\vec{r}_\theta \times \vec{r}_\emptyset)}{r^2|\vec{r}_\theta \times \vec{r}_\emptyset|}$$
$$= \frac{\vec{u}\cdot(r^2(\vec{u}_\theta \times \vec{u}_\emptyset) + r(r_\emptyset\vec{u}_\theta - r_\theta\vec{u}_\emptyset)\times\vec{u})}{r^2|\vec{r}_\theta \times \vec{r}_\emptyset|}$$
$$= \frac{\vec{u}\cdot r^2(\vec{u}_\theta \times \vec{u}_\emptyset) + 0}{r^2|\vec{r}_\theta \times \vec{r}_\emptyset|}$$
$$= \frac{\vec{u}\cdot\vec{u}_\theta \times \vec{u}_\emptyset}{|\vec{r}_\theta \times \vec{r}_\emptyset|}$$
$$= \frac{1}{|\vec{r}_\theta \times \vec{r}_\emptyset|}\begin{vmatrix} \cos\theta & \sin\theta\cos\emptyset & \sin\theta\sin\emptyset \\ -\sin\theta & \cos\theta\cos\emptyset & \cos\theta\sin\emptyset \\ 0 & -\sin\theta\sin\emptyset & \sin\theta\cos\emptyset \end{vmatrix}$$
$$= \frac{\sin\theta}{|\vec{r}_\theta \times \vec{r}_\emptyset|}$$

[172] Finally, it can be shown that $\vec{V}$ is in fact a scalar multiple of $\vec{D}$:

$$\vec{V} = \iint_S I(\vec{u} \cdot \vec{D}) \frac{\vec{u} \cdot \vec{n}}{r^2} \vec{u} dS$$

$$= \int_0^{\pi/2} \int_0^{2\pi} I(\vec{u} \cdot \vec{D}) \frac{\vec{u} \cdot \vec{n}}{r^2} \vec{u} |\vec{r_\theta} \times \vec{r_\emptyset}| d\emptyset d\theta$$

$$= \int_0^{\pi/2} \int_0^{2\pi} I(cos\theta) \frac{sin\theta}{|\vec{r_\theta} \times \vec{r_\emptyset}|} \vec{u} |\vec{r_\theta} \times \vec{r_\emptyset}| d\emptyset d\theta$$

$$= \int_0^{\pi/2} \int_0^{2\pi} I(cos\theta) \vec{u} \sin\theta d\emptyset d\theta$$

$$= \int_0^{\pi/2} I(cos\theta) sin\,\theta \int_0^{2\pi} \vec{u} d\emptyset d\theta$$

$$= \int_0^{\pi/2} I(cos\theta) sin\,\theta \int_0^{2\pi} \vec{D} \cos\theta + (\sin\theta)\left(\vec{D}^{\perp} \cos\emptyset + \left(\vec{D} \times \vec{D}^{\perp}\right) \sin\emptyset\right) d\emptyset d\theta$$

$$= \int_0^{\pi/2} I(cos\theta) sin\,\theta \left(2\pi\vec{D} \cos\theta + \sin\theta \int_0^{2\pi} \vec{D}^{\perp} \cos\emptyset + \left(\vec{D} \times \vec{D}^{\perp}\right) sin\,\emptyset d\emptyset \right) d\theta$$

$$= \int_0^{\pi/2} I(cos\theta) sin\,\theta \left(2\pi\vec{D} \cos\theta + \sin\theta \cdot 0\right) d\theta$$

$$= \int_0^{\pi/2} I(cos\theta)\, 2\pi\vec{D}\, \sin\theta\, cos\,\theta d\theta$$

$$= 2\pi\vec{D} \int_0^{\pi/2} I(cos\theta) \sin\theta\, cos\,\theta d\theta$$

$$= c\vec{D} \text{ for } c = 2\pi \int_0^{\pi/2} I\,(cos\theta) \sin\theta\, cos\,\theta d\theta$$

[173] To program and initially setup near-eye pupil-tracking surface 4300, a fixed point *O* representing the average apex of the light cone may first be chosen. Next, for each sensor at a point *X*, let $\vec{r} := X - O$, and let ρ be the sensor density at that location. Next, for each sensor, assign $r := |\vec{r}|$, $\vec{u} := \frac{\vec{r}}{r}$ and $\vec{v} := \frac{\vec{u}}{\rho}$. Next, store at each sensor the value of $\vec{v}$. Next, experimentally determine the control vector $\vec{W}$ by taking the value of $\sum I\vec{v}$ when there is no retroreflector present (such as when the device is being worn, but the eye is closed). Finally, store the value of $\vec{W}$.

[174] At runtime, the follow procedure may be followed. First, record at each sensor the intensity of light *I* hitting that sensor. Next, compute $\sum I\vec{v}$ over all sensors. Next, let $\vec{V} := (\sum I\vec{v}) - \vec{W}$. Finally, output the vector $\vec{D} := \frac{\vec{v}}{|\vec{v}|}$.

[175] FIGURE 51 illustrates a method 5100 of manufacturing an electronic assembly using flexible circuit such as flexible circuit board 2210, according to certain embodiments. At step 5110, a plurality of facet locations are formed on a flexible circuit board. In some embodiments, the facet locations are facet locations 2220, and the flexible circuit board is flexible circuit board 2210. Each facet location corresponds to one of a plurality of facets. The facets may be facets 4305 or display facets 2665. In some embodiments, the plurality of facet locations are arranged into a plurality of facet columns such as columns 2201. In some embodiments, the plurality of facet locations are additionally or alternatively arranged into a plurality of facet rows such as rows 2202.

[176] At step 5120, the flexible circuit board of step 5110 is cut or otherwise shaped into a pattern. In some embodiments, the pattern permits the flexible circuit board to be later formed into a curved shape that is configured to be substantially concentric with a viewer's eye. In some embodiments, the pattern permits the flexible circuit board to be later formed into a curved shape that will not be substantially concentric with a viewer's eye.

[177] At step 5130, the electronic assembly is assembled by coupling a plurality of facets to a first side of the flexible circuit board that is configured to face the viewer's eye. The plurality of facets may be facets 4305 or display facets 2665. Each facet may be coupled to a respective one of the facet locations. In some embodiments, the plurality of facets are coupled to connection pads on the first side of the flexible circuit board using any appropriate mounting technique such as patterned conductive and non-conductive adhesives. Each facet includes a planar face such as planar face 4750, one or more

emitters such as emitters 4730 that are configured to emit light towards the viewer's eye, and one or more receptors such as receptors 4740 that are configured to detect the emitted light after it has been reflected back towards the electronic assembly from a retina of the viewer's eye. Each planar face is normal to a line pointing towards a center area of the viewer's eye when the curved shape is substantially concentric with the viewer's eye.

[178] At step 5140, the assembled electronic assembly is formed into the desired curved shape. In some embodiments, this step involves placing the flexible circuit board with its coupled rigid facets into one side of a rigid casing that is in the desired shape. This allows the rigid facets to fall into defined spaces in the casing and the flexible circuit board to bend at defined creases/gaps between the rigid facets. After placing the flexible circuit board with its coupled rigid facets into one side of the rigid casing, an opposite matching side of the rigid casing may be attached to the first side, thereby sealing the assembly into the desired shape.

[179] Particular embodiments may repeat one or more steps of method 5100, where appropriate. Although this disclosure describes and illustrates particular steps of method 5100 as occurring in a particular order, this disclosure contemplates any suitable steps of method 5100 occurring in any suitable order (e.g., any temporal order). Moreover, although this disclosure describes and illustrates an example method of manufacturing an electronic assembly using flexible circuit board, this disclosure contemplates any suitable method of manufacturing an electronic assembly using flexible circuit board, which may include all, some, or none of the steps of method 5100, where appropriate. Furthermore, although this

disclosure describes and illustrates particular components, devices, or systems carrying out particular steps of method 5100, this disclosure contemplates any suitable combination of any suitable components, devices, or systems carrying out any suitable steps of method 5100.

[180] Herein, "or" is inclusive and not exclusive, unless expressly indicated otherwise or indicated otherwise by context. Therefore, herein, "A or B" means "A, B, or both," unless expressly indicated otherwise or indicated otherwise by context. Moreover, "and" is both joint and several, unless expressly indicated otherwise or indicated otherwise by context. Therefore, herein, "A and B" means "A and B, jointly or severally," unless expressly indicated otherwise or indicated otherwise by context.

[181] The scope of this disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the example embodiments described or illustrated herein that a person having ordinary skill in the art would comprehend. The scope of this disclosure is not limited to the example embodiments described or illustrated herein. Moreover, although this disclosure describes and illustrates respective embodiments herein as including particular components, elements, functions, operations, or steps, any of these embodiments may include any combination or permutation of any of the components, elements, functions, operations, or steps described or illustrated anywhere herein that a person having ordinary skill in the art would comprehend. Furthermore, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that

apparatus, system, component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative.

[182] Although this disclosure describes and illustrates respective embodiments herein as including particular components, elements, functions, operations, or steps, any of these embodiments may include any combination or permutation of any of the components, elements, functions, operations, or steps described or illustrated anywhere herein that a person having ordinary skill in the art would comprehend.

[183] Furthermore, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative.

WHAT IS CLAIMED IS:

1. An electronic assembly comprising:

a flexible circuit board formed into a curved shape that is configured to be substantially concentric with a viewer's eye; and

a plurality of facets coupled to a side of curved shape of the flexible circuit board that is configured to face the viewer's eye, each facet comprising:

a planar face, each face being normal to a line pointing towards a center area of the viewer's eye when the curved shape is substantially concentric with the viewer's eye;

one or more emitters configured to emit light from the face of the facet towards the viewer's eye; and

one or more receptors configured to detect the emitted light after it has been reflected back towards the face of the facet from a retina of the viewer's eye;

wherein each facet is individually addressable such that the plurality of facets are configurable to detect a center of gaze of the viewer.

2. The electronic assembly of Claim 1, wherein each of the plurality of facets are in a shape of a polygon comprising a triangle, a quadrilateral, a pentagon, a hexagon, a heptagon, or an octagon.

3. The electronic assembly of Claim 1, wherein the plurality of facets are arranged into a plurality of facet columns and a plurality of facet rows.

4. The electronic assembly of Claim 1, wherein:

the plurality of facets are display facets comprising a plurality of display pixels;

the one or more emitters each comprise an IR emitter layer within a respective one of the display pixels; and

and the one or more receptors each comprise an IR detector layer within a respective one of the display pixels.

5. The electronic assembly of Claim 4, wherein each display facet is coupled to a respective one of a plurality of logic facets.

6. The electronic assembly of Claim 1, wherein the light emitted by the one or more emitters comprises IR light.

7. The electronic assembly of Claim 1, wherein the center of gaze of the viewer comprises a central facet within a plurality of facets that detect any of the emitted light after it has been reflected back towards the electronic assembly from the retina of the viewer's eye.

8. An electronic assembly comprising:

a circuit board; and

a plurality of facets coupled to a side of the circuit board that is configured to face a viewer's eye, each facet comprising:

a planar face;

one or more emitters configured to emit light towards the viewer's eye; and

one or more receptors configured to detect the emitted light after it has been reflected back towards the electronic assembly from a portion of the viewer's eye;

wherein each facet is individually addressable such that the plurality of facets are configurable to detect a center of gaze of the viewer.

9. The electronic assembly of Claim 8, wherein each of the plurality of facets are in a shape of a polygon comprising a triangle, a quadrilateral, a pentagon, a hexagon, a heptagon, or an octagon.

10. The electronic assembly of Claim 8, wherein the plurality of facets are arranged into a plurality of facet columns and a plurality of facet rows.

11. The electronic assembly of Claim 8, wherein:

the plurality of facets are display facets comprising a plurality of display pixels;

the one or more emitters each comprise an IR emitter layer within a respective one of the display pixels; and

and the one or more receptors each comprise an IR detector layer within a respective one of the display pixels.

12. The electronic assembly of Claim 11, wherein each display facet is coupled to a respective one of a plurality of logic facets.

13. The electronic assembly of Claim 8, wherein the light emitted by the one or more emitters comprises IR light.

14. The electronic assembly of Claim 8, wherein the center of gaze of the viewer comprises a central facet within a plurality of facets that detect any of the emitted light after it has been reflected back towards the electronic assembly from the portion of the viewer's eye.

15. A method of manufacturing an electronic assembly, the method comprising:

forming a plurality of facet locations on a flexible circuit board, each facet location corresponding to one of a plurality of facets;

cutting the flexible circuit board into a pattern that permits the flexible circuit board to be later formed into a curved shape that is configured to be substantially concentric with a viewer's eye;

assembling the electronic assembly by coupling a plurality of facets to a side of the flexible circuit board that is configured to face the viewer's eye, each facet being coupled to a respective one of the facet locations, each facet comprising:

a planar face, each face being normal to a line pointing towards a center area of the viewer's eye when the curved shape is substantially concentric with the viewer's eye;

one or more emitters configured to emit light towards the viewer's eye; and

one or more receptors configured to detect the emitted light after it has been reflected back towards the electronic assembly from a portion of the viewer's eye; and

forming the assembled electronic assembly into the curved shape.

16. The method of manufacturing the electronic assembly of Claim 15, further comprising coupling each of a plurality of display facets to a respective one of the plurality of facets.

17. The method of manufacturing the electronic assembly of Claim 15, wherein the plurality of facets are in the shape of a polygon.

18. The method of manufacturing the electronic assembly of Claim 17, wherein the polygon comprises a triangle, a quadrilateral, a pentagon, a hexagon, a heptagon, or an octagon.

19. The method of manufacturing the electronic assembly of Claim 17, wherein the plurality of facet locations are arranged into a plurality of facet columns and a plurality of facet rows.

20. The method of manufacturing the electronic assembly of Claim 17, wherein each particular facet location comprises:

a ball grid array configured to couple to one of the plurality of facets; and

a plurality of interconnection pads configured to electrically couple the particular facet to one or more adjacent facets.

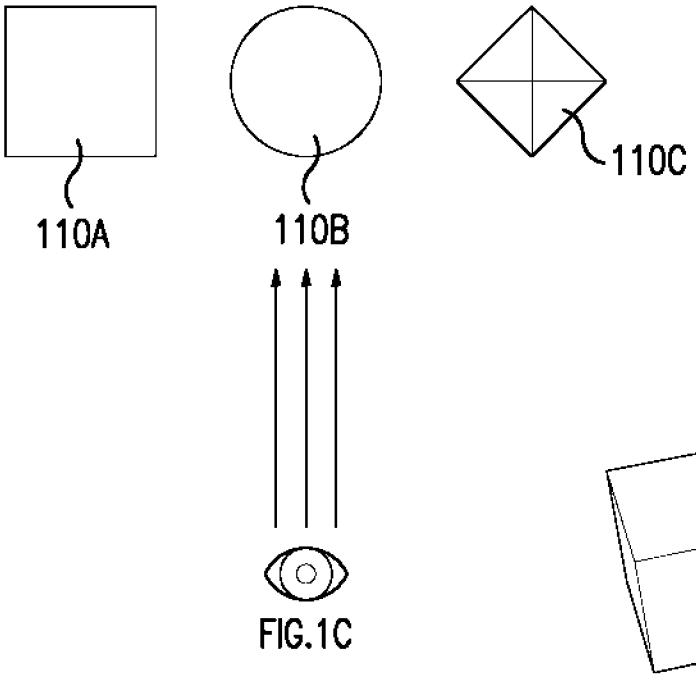

FIG. 1A

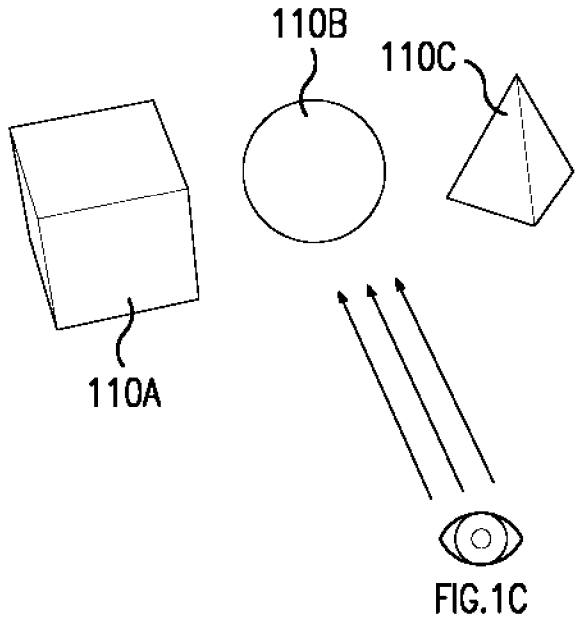

FIG. 1B

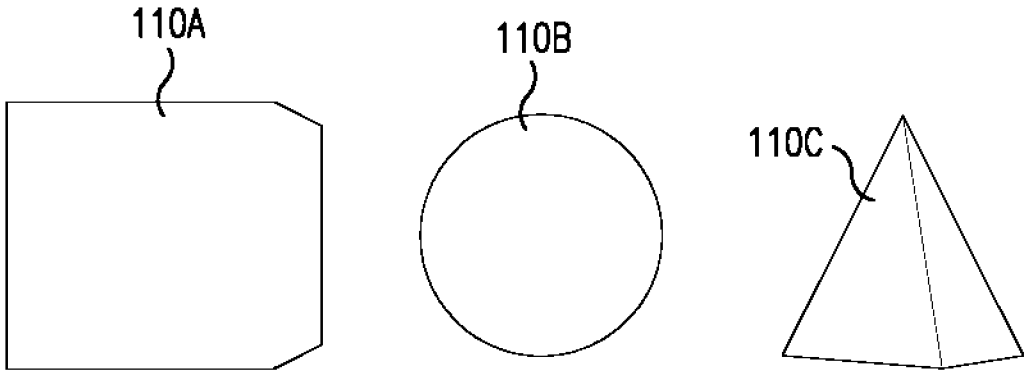

FIG. 1C

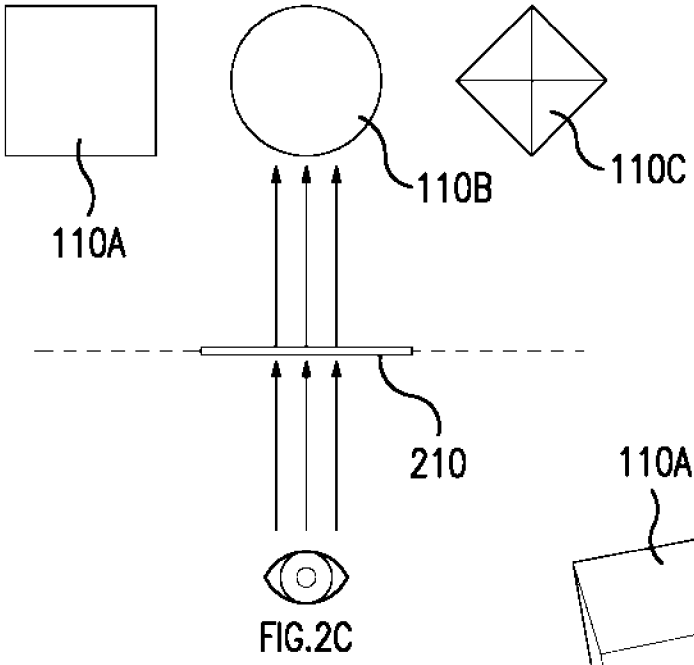

FIG. 2A

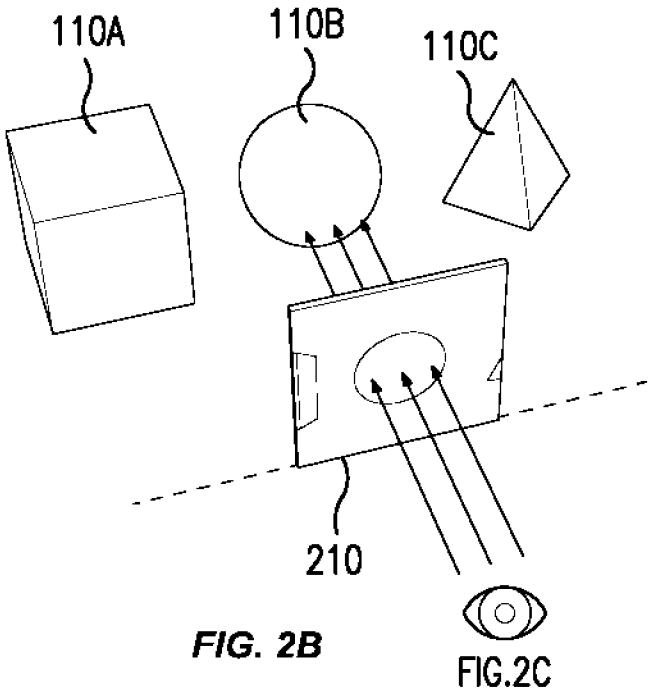

FIG. 2B

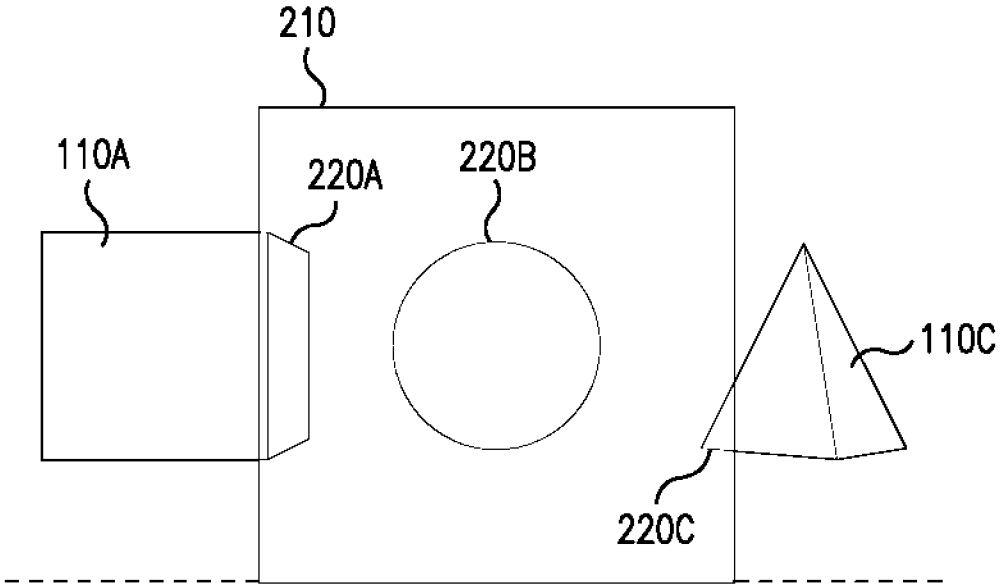

FIG. 2C

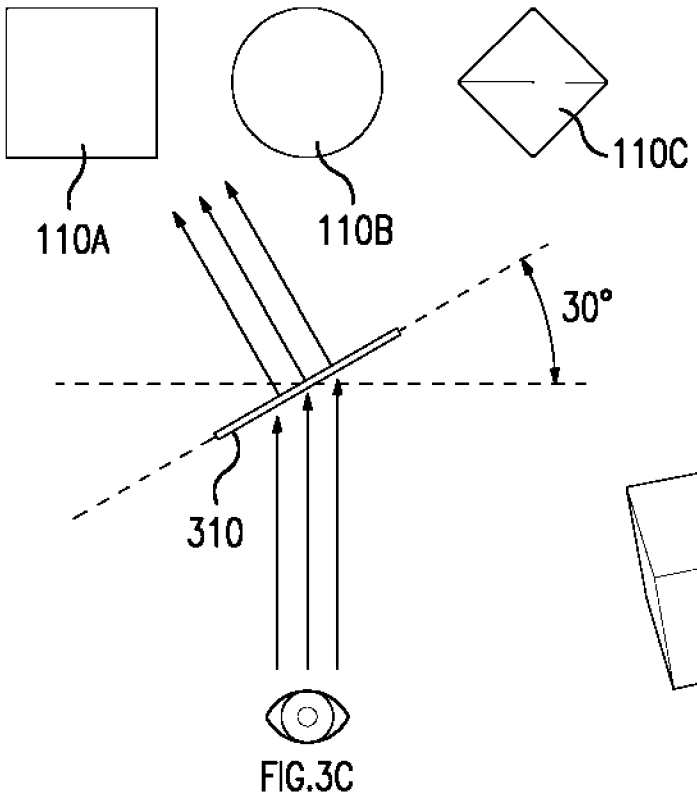

FIG. 3A

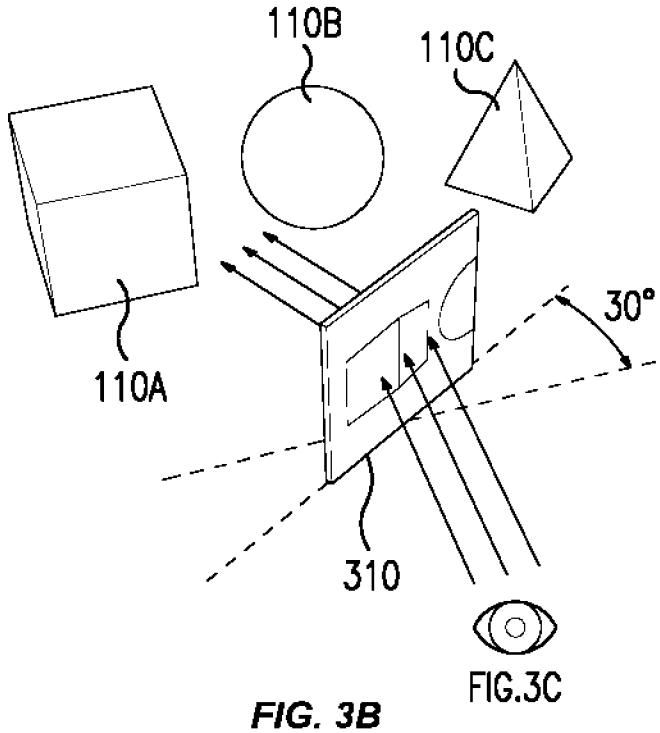

FIG. 3B

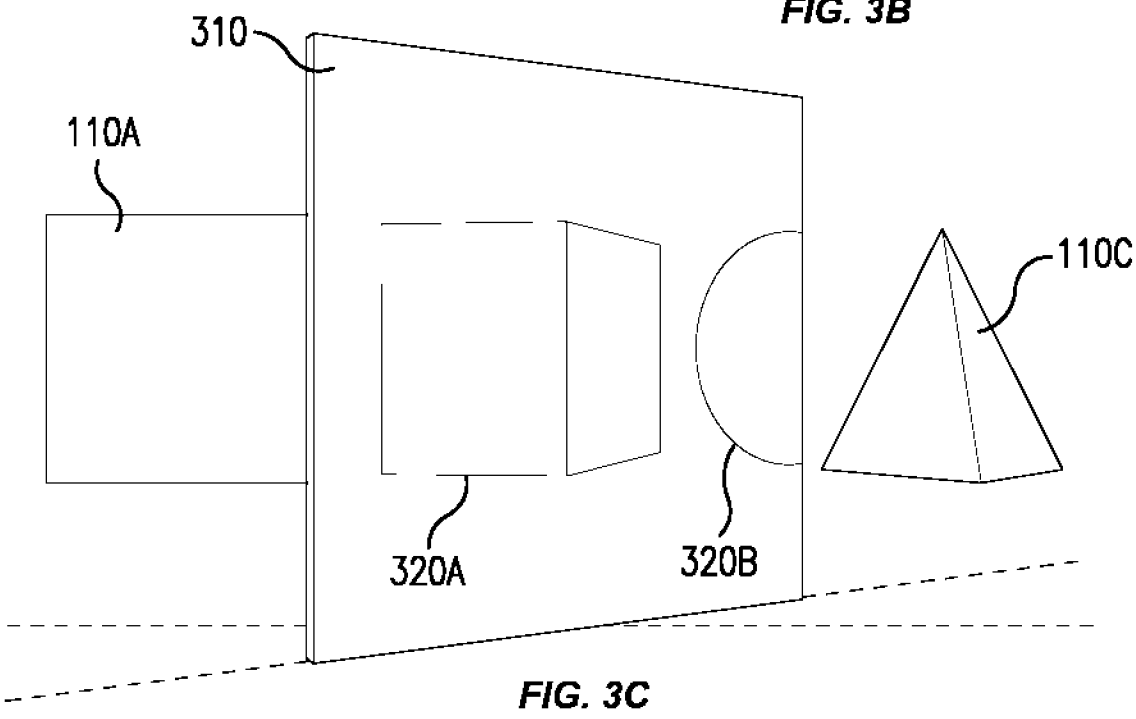

FIG. 3C

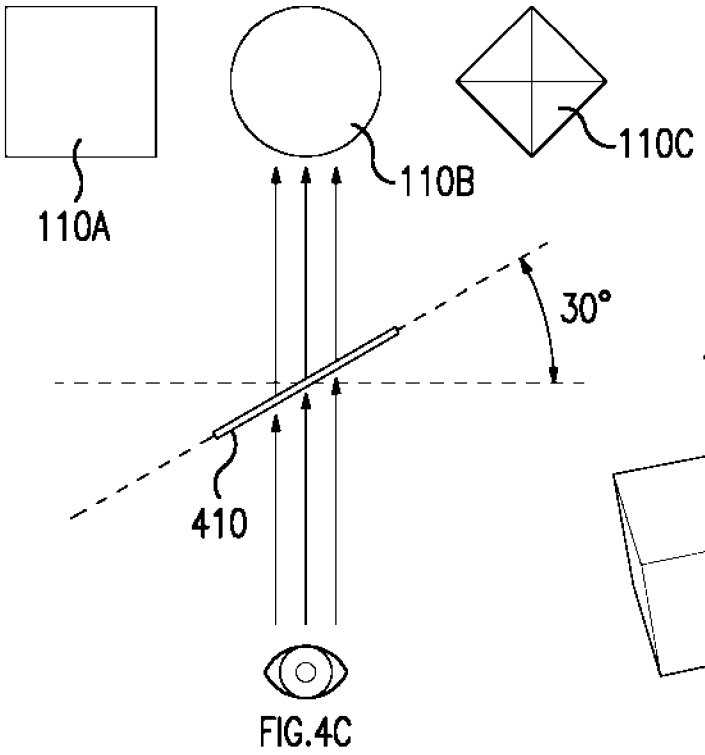

FIG. 4A

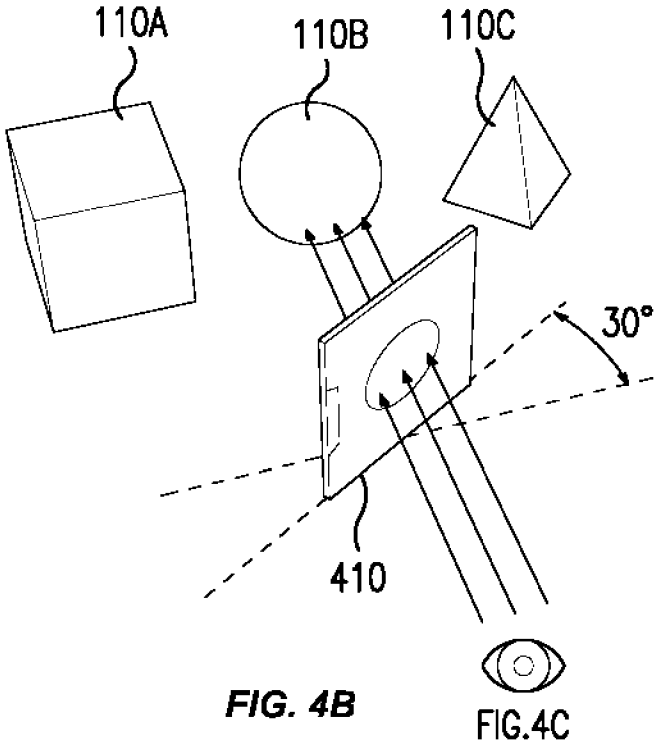

FIG. 4B

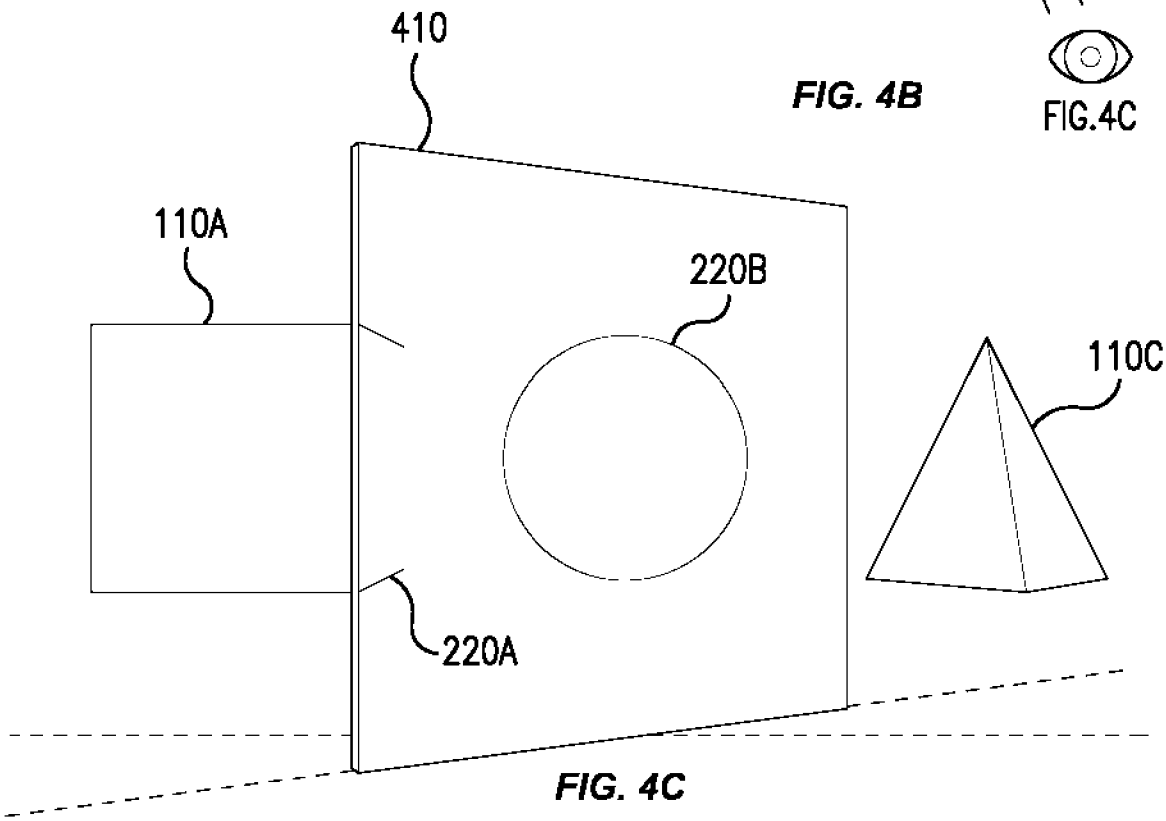

FIG. 4C

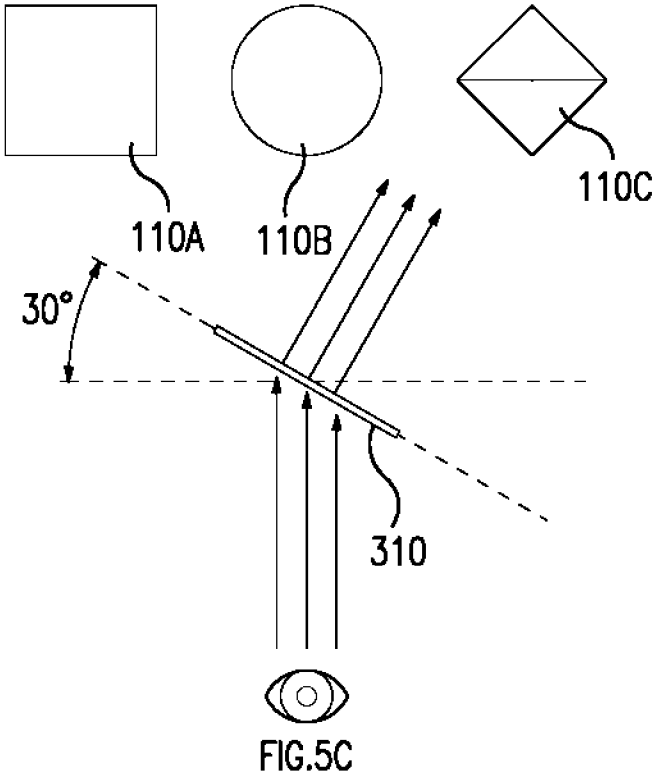

FIG. 5A

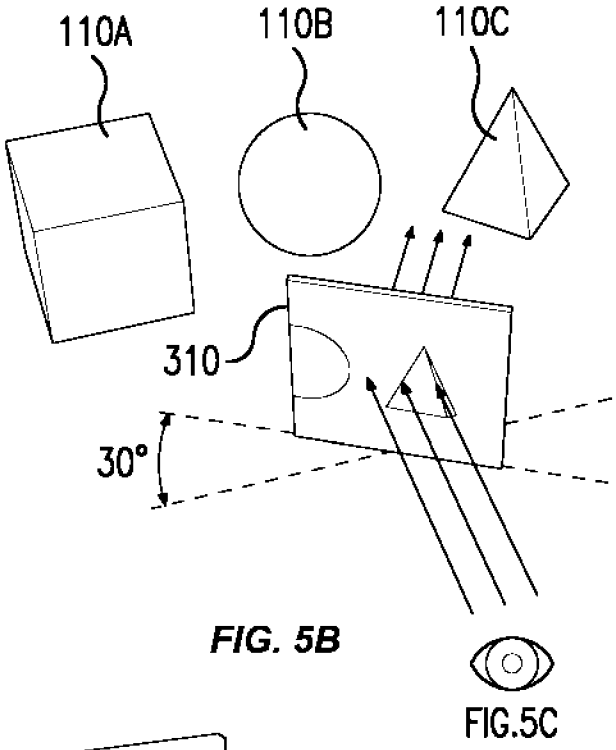

FIG. 5B

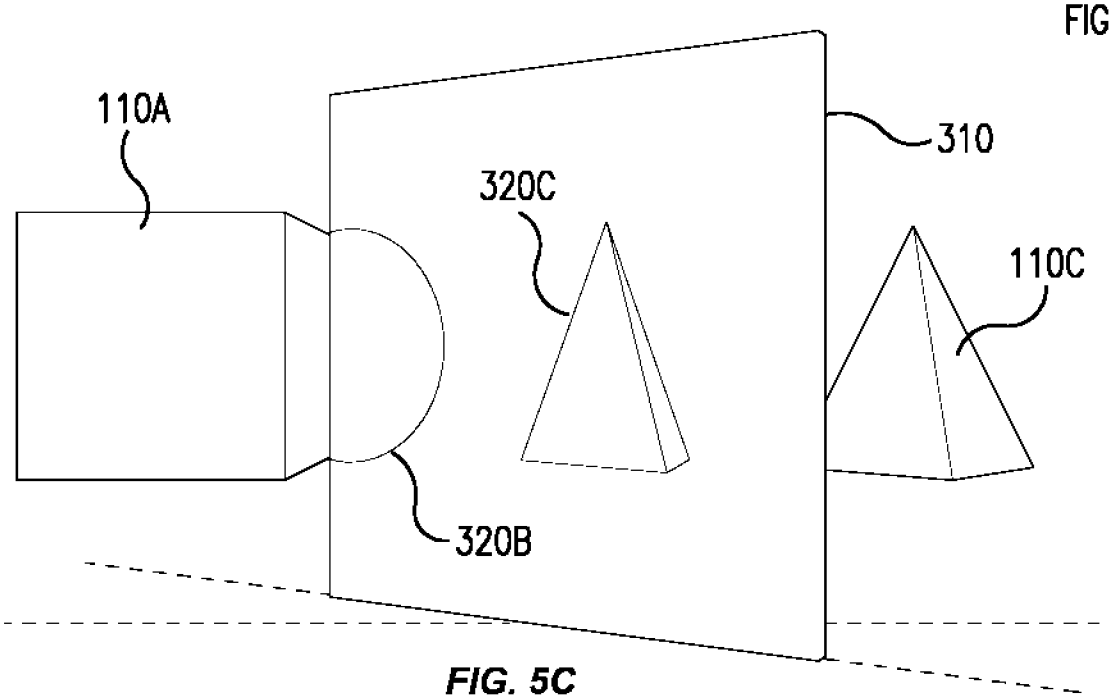

FIG. 5C

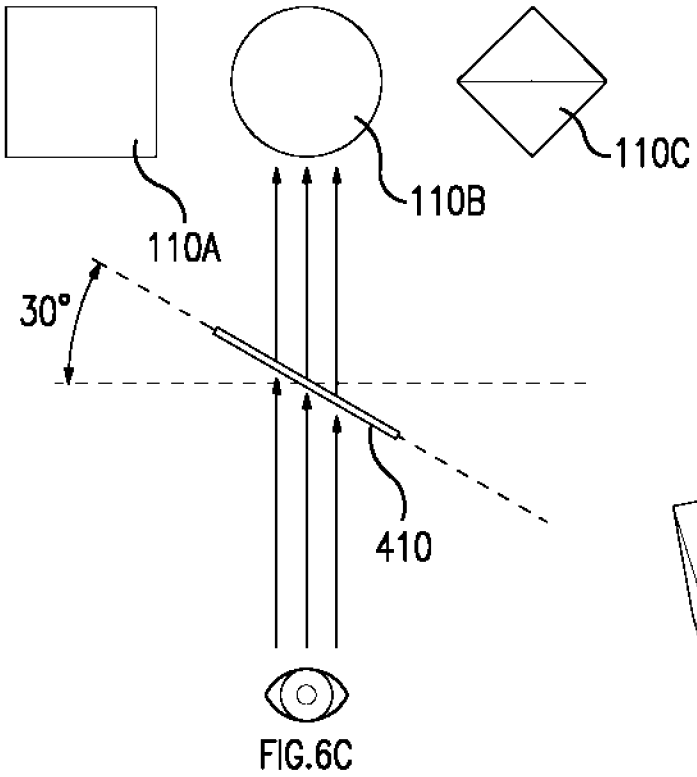

FIG. 6A

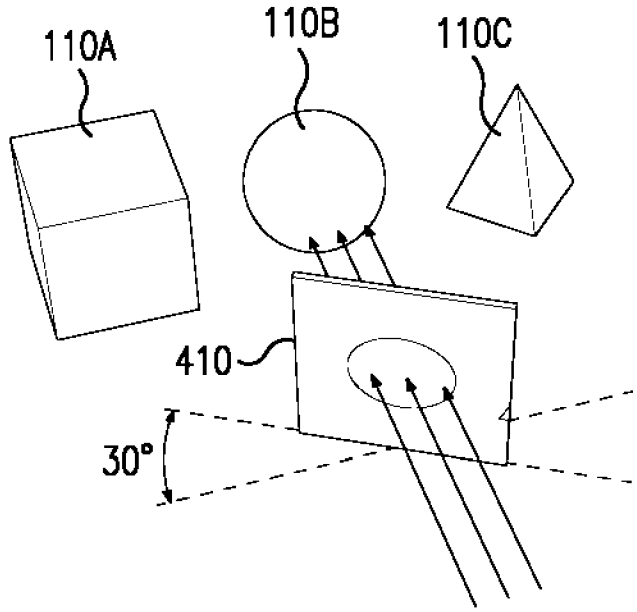

FIG. 6B

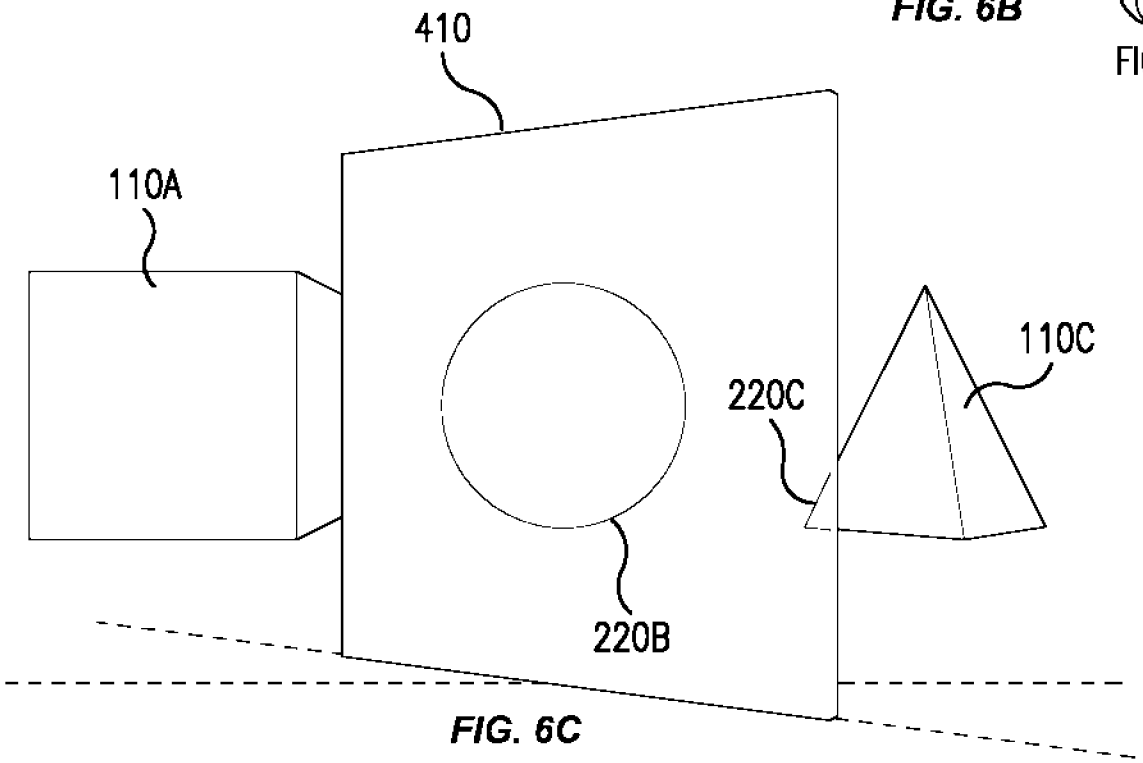

FIG. 6C

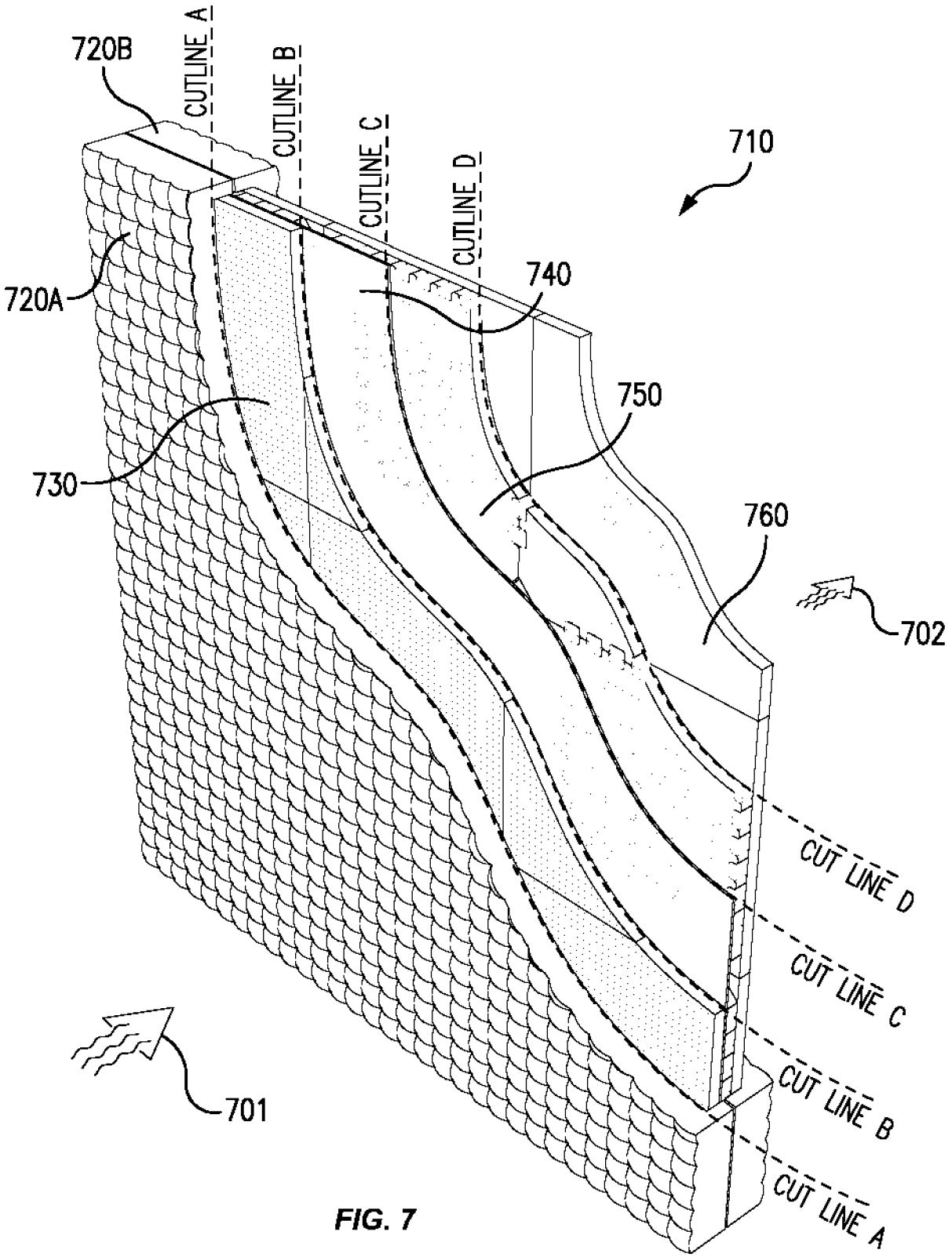
720B
CUTLINE_A
CUTLINE_B
CUTLINE_C
CUTLINE_D
710
720A
740
750
730
760
702
CUT LINE D
CUT LINE C
CUT LINE B
CUT LINE A
701

FIG. 7

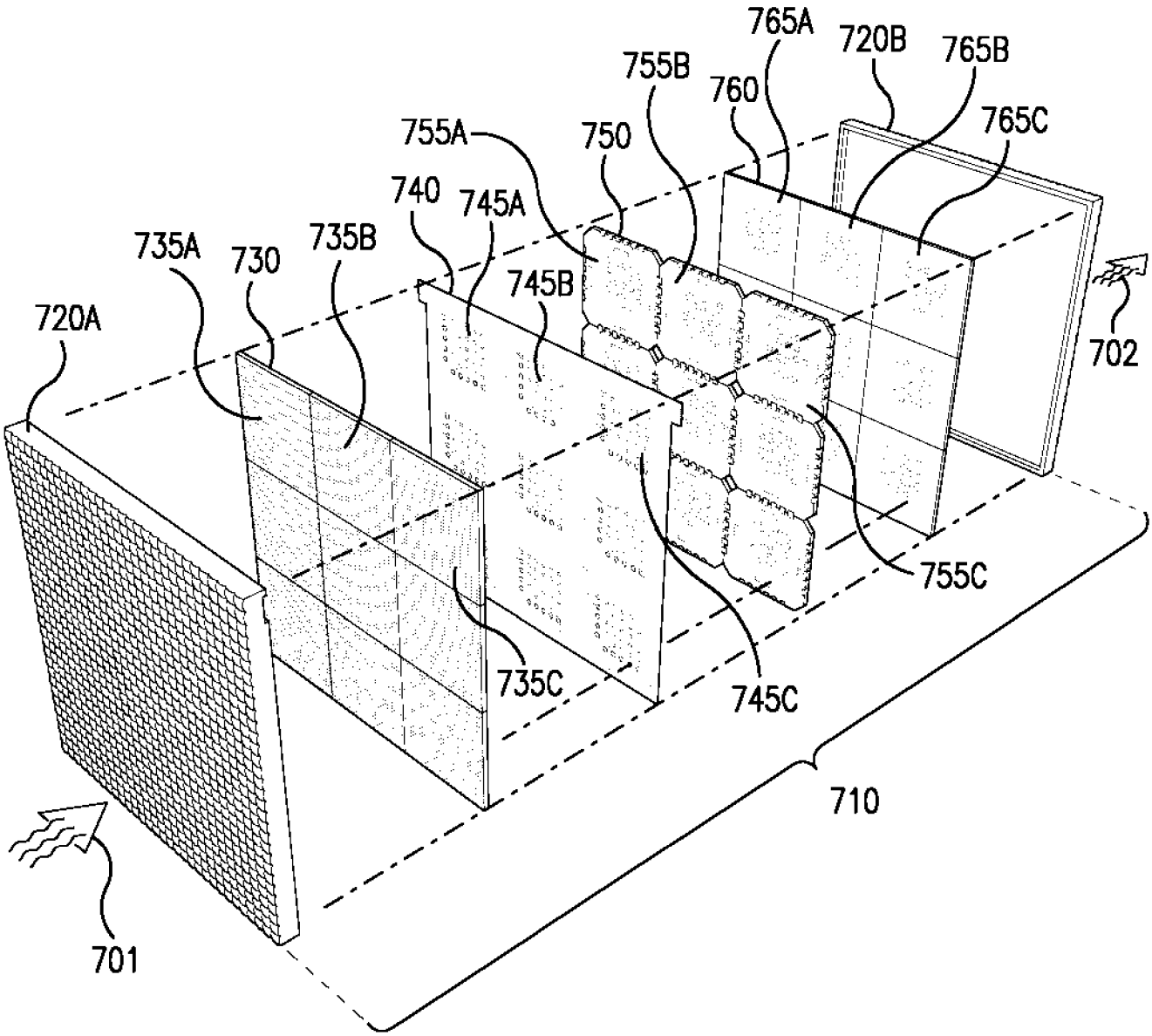
765A
720B
765B
755B
760
765C
755A
750
740
745A
735A
730
735B
745B
720A
702
755C
735C
745C
710
701

FIG. 8

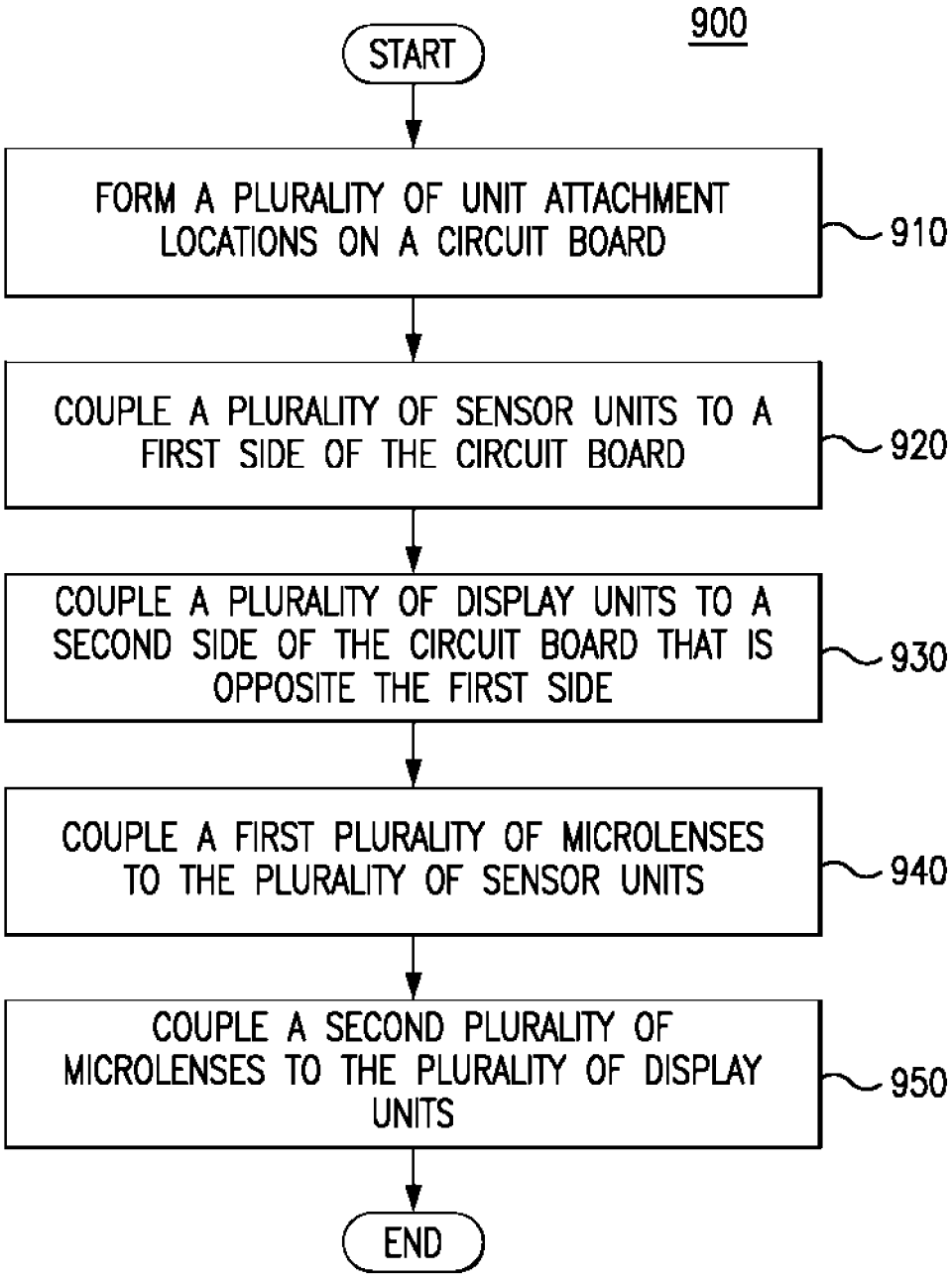
900
START
FORM A PLURALITY OF UNIT ATTACHMENT LOCATIONS ON A CIRCUIT BOARD
910
COUPLE A PLURALITY OF SENSOR UNITS TO A FIRST SIDE OF THE CIRCUIT BOARD
920
COUPLE A PLURALITY OF DISPLAY UNITS TO A SECOND SIDE OF THE CIRCUIT BOARD THAT IS OPPOSITE THE FIRST SIDE
930
COUPLE A FIRST PLURALITY OF MICROLENSES TO THE PLURALITY OF SENSOR UNITS
940
COUPLE A SECOND PLURALITY OF MICROLENSES TO THE PLURALITY OF DISPLAY UNITS
950
END

FIG. 9

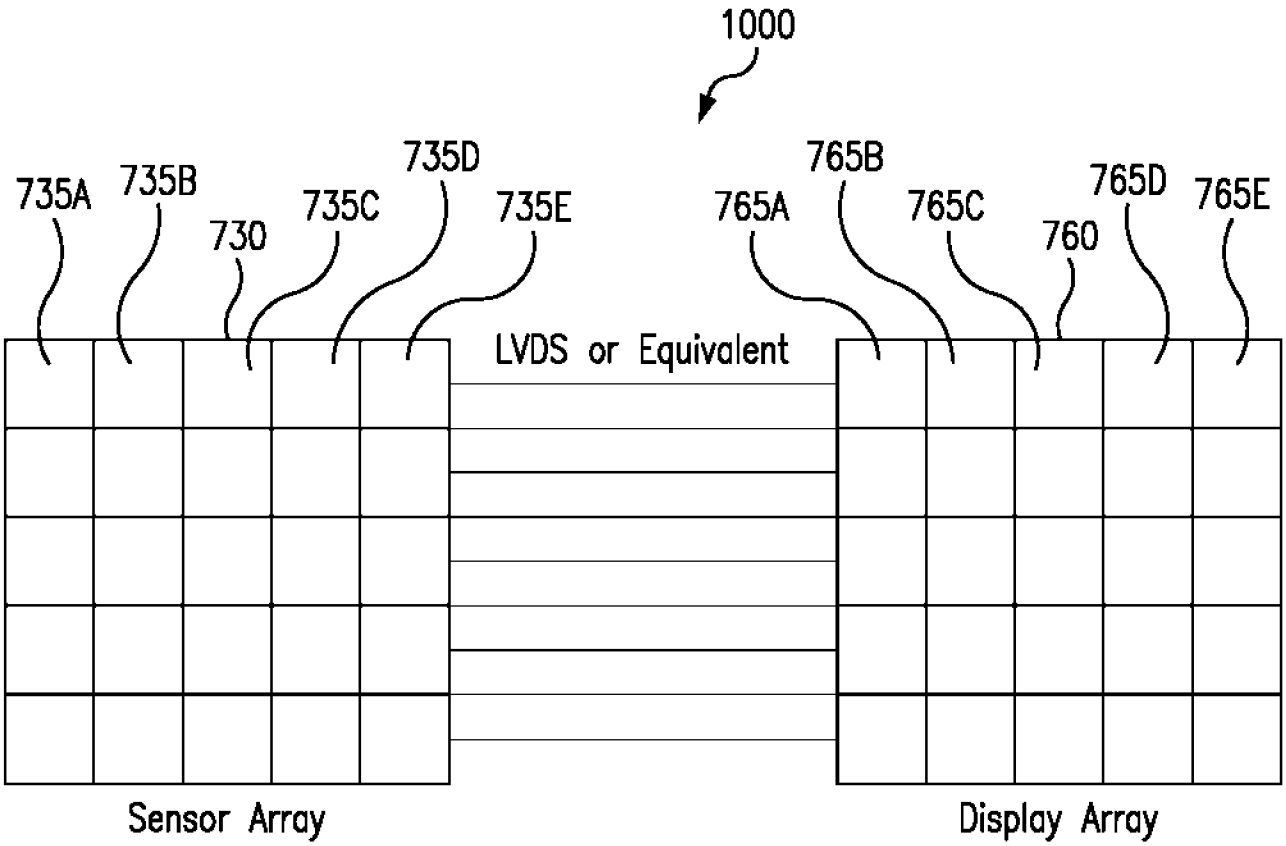
1000
735A
735B
730
735C
735D
735E
765A
765B
765C
760
765D
765E
LVDS or Equivalent
Sensor Array
Display Array

FIG. 10

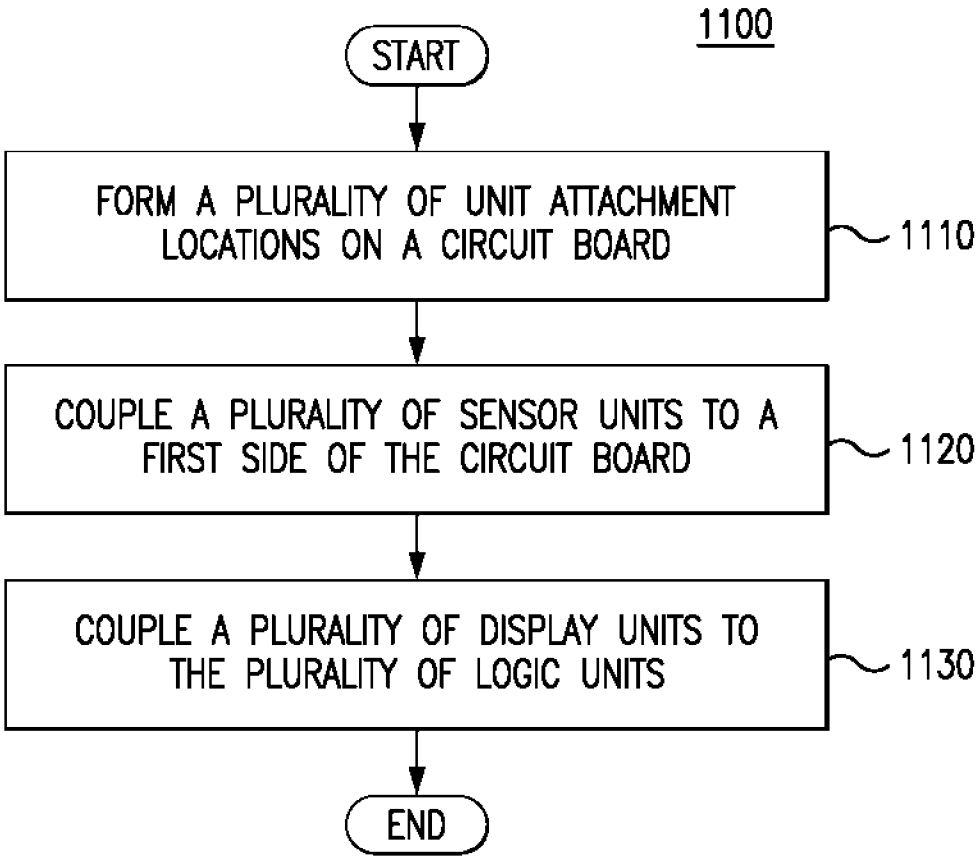
1100
START
FORM A PLURALITY OF UNIT ATTACHMENT LOCATIONS ON A CIRCUIT BOARD
1110
COUPLE A PLURALITY OF SENSOR UNITS TO A FIRST SIDE OF THE CIRCUIT BOARD
1120
COUPLE A PLURALITY OF DISPLAY UNITS TO THE PLURALITY OF LOGIC UNITS
1130
END

FIG. 11

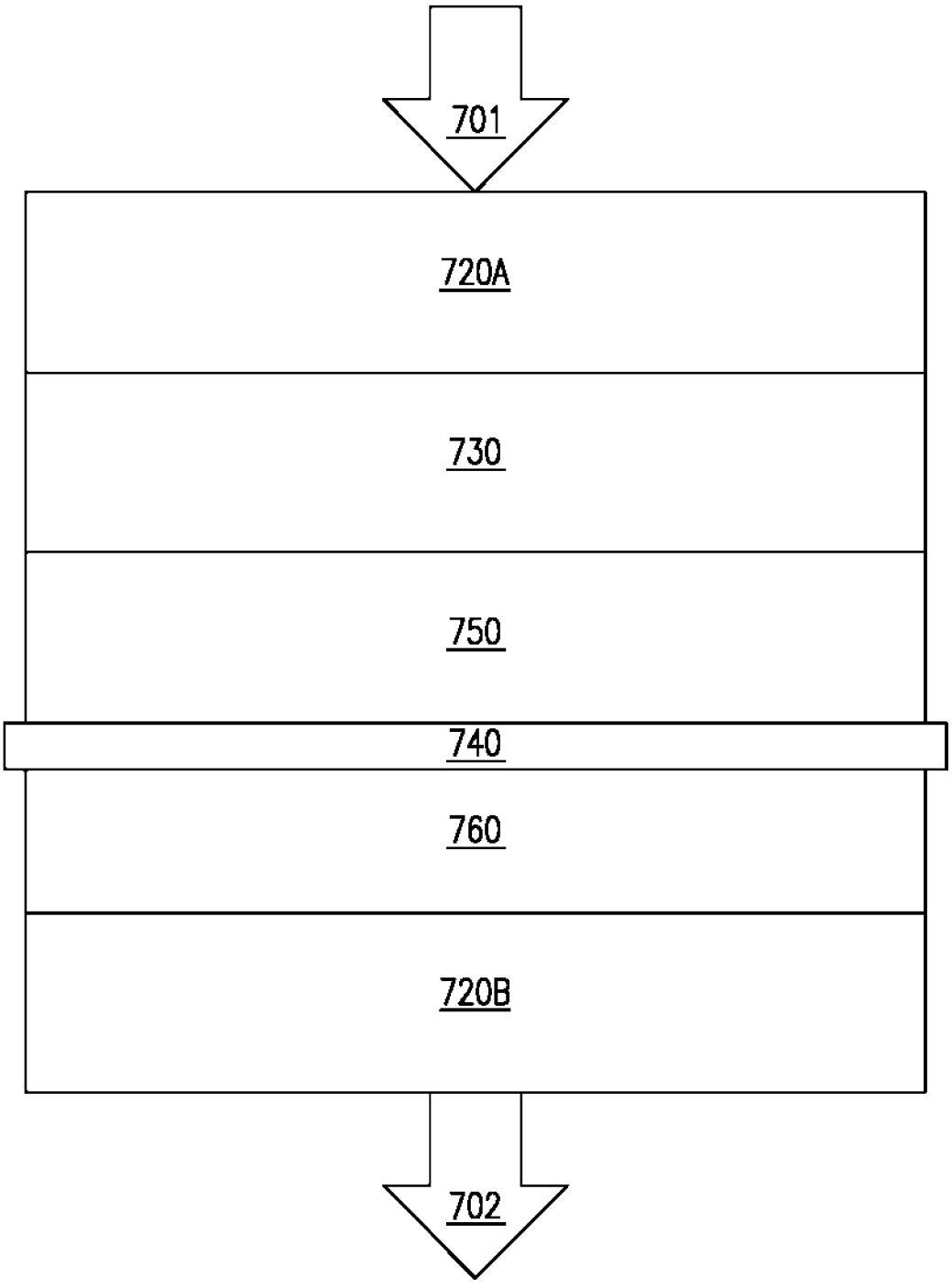

FIG. 12

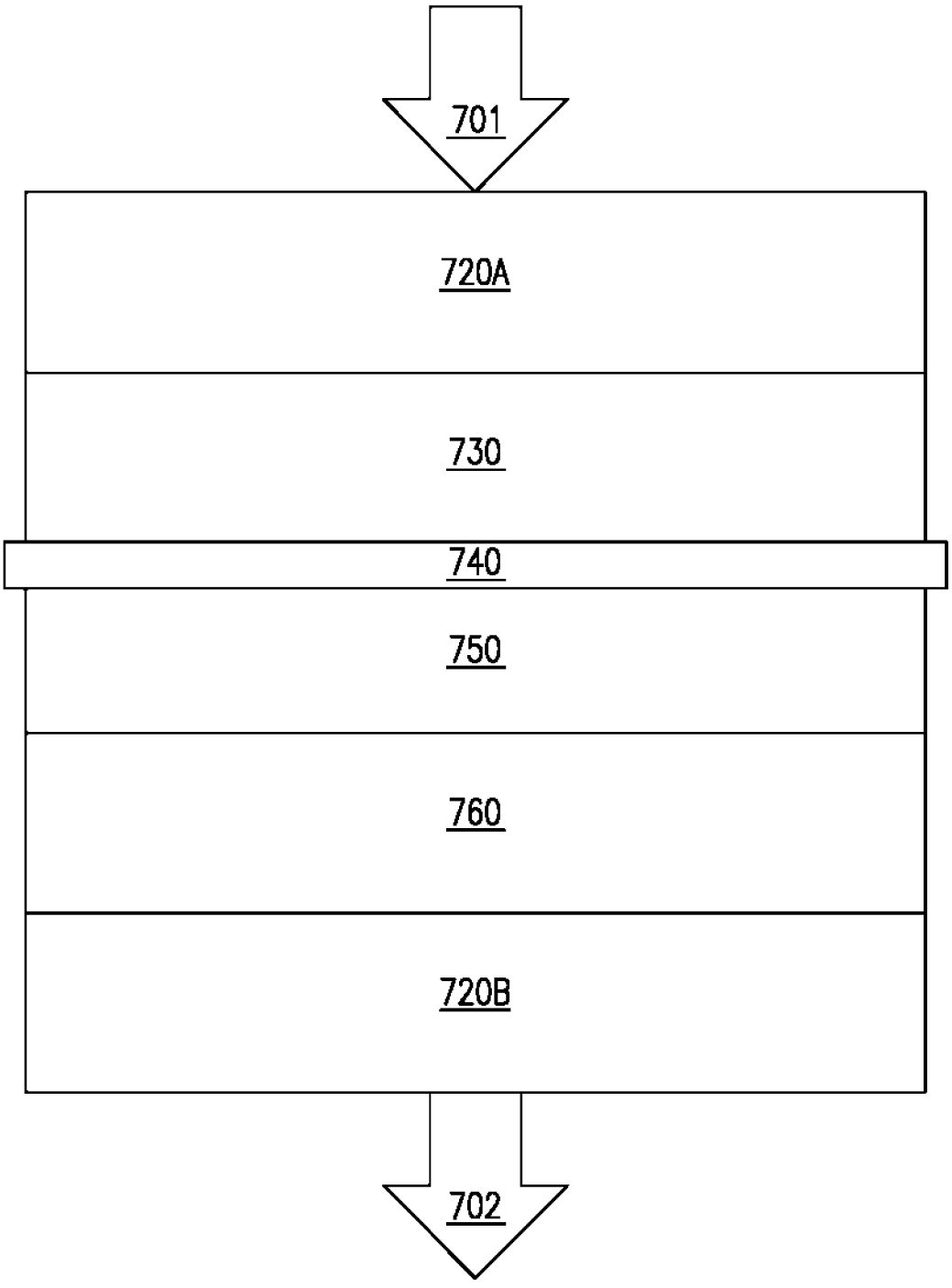

FIG. 13

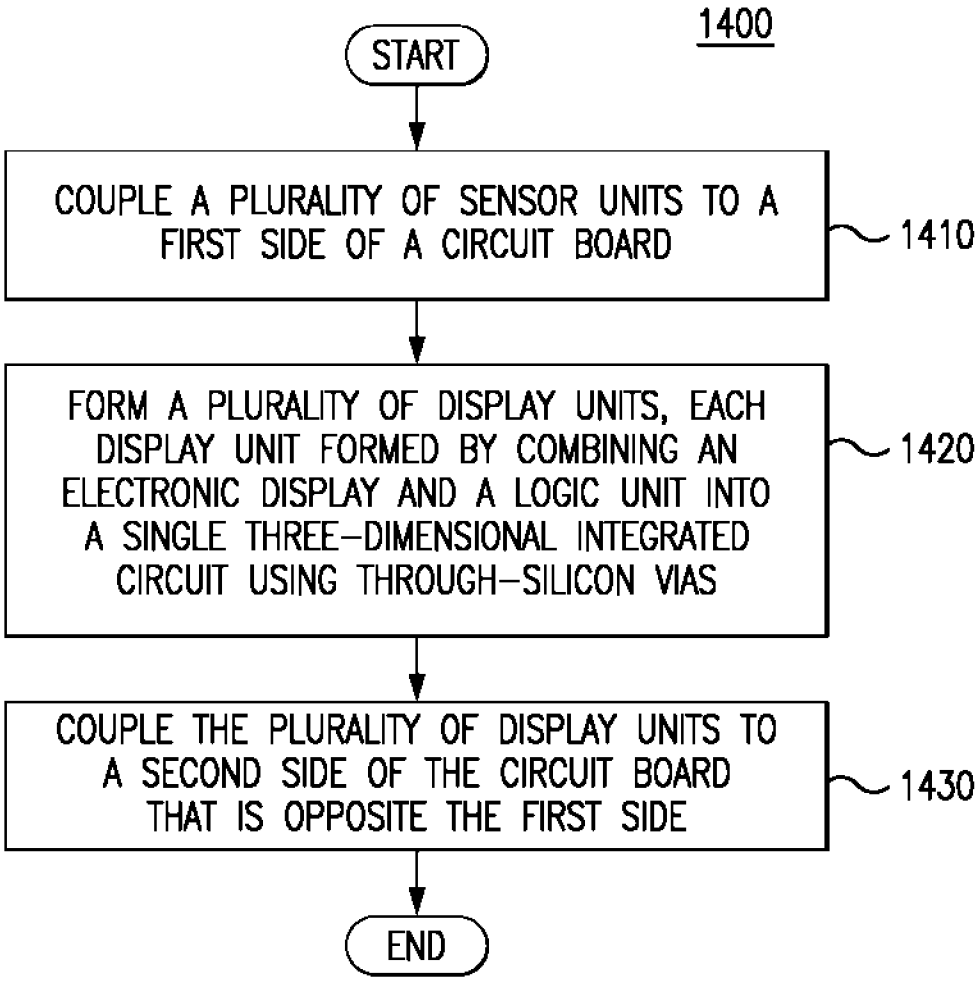
1400
START
COUPLE A PLURALITY OF SENSOR UNITS TO A FIRST SIDE OF A CIRCUIT BOARD
1410
FORM A PLURALITY OF DISPLAY UNITS, EACH DISPLAY UNIT FORMED BY COMBINING AN ELECTRONIC DISPLAY AND A LOGIC UNIT INTO A SINGLE THREE-DIMENSIONAL INTEGRATED CIRCUIT USING THROUGH-SILICON VIAS
1420
COUPLE THE PLURALITY OF DISPLAY UNITS TO A SECOND SIDE OF THE CIRCUIT BOARD THAT IS OPPOSITE THE FIRST SIDE
1430
END

FIG. 14

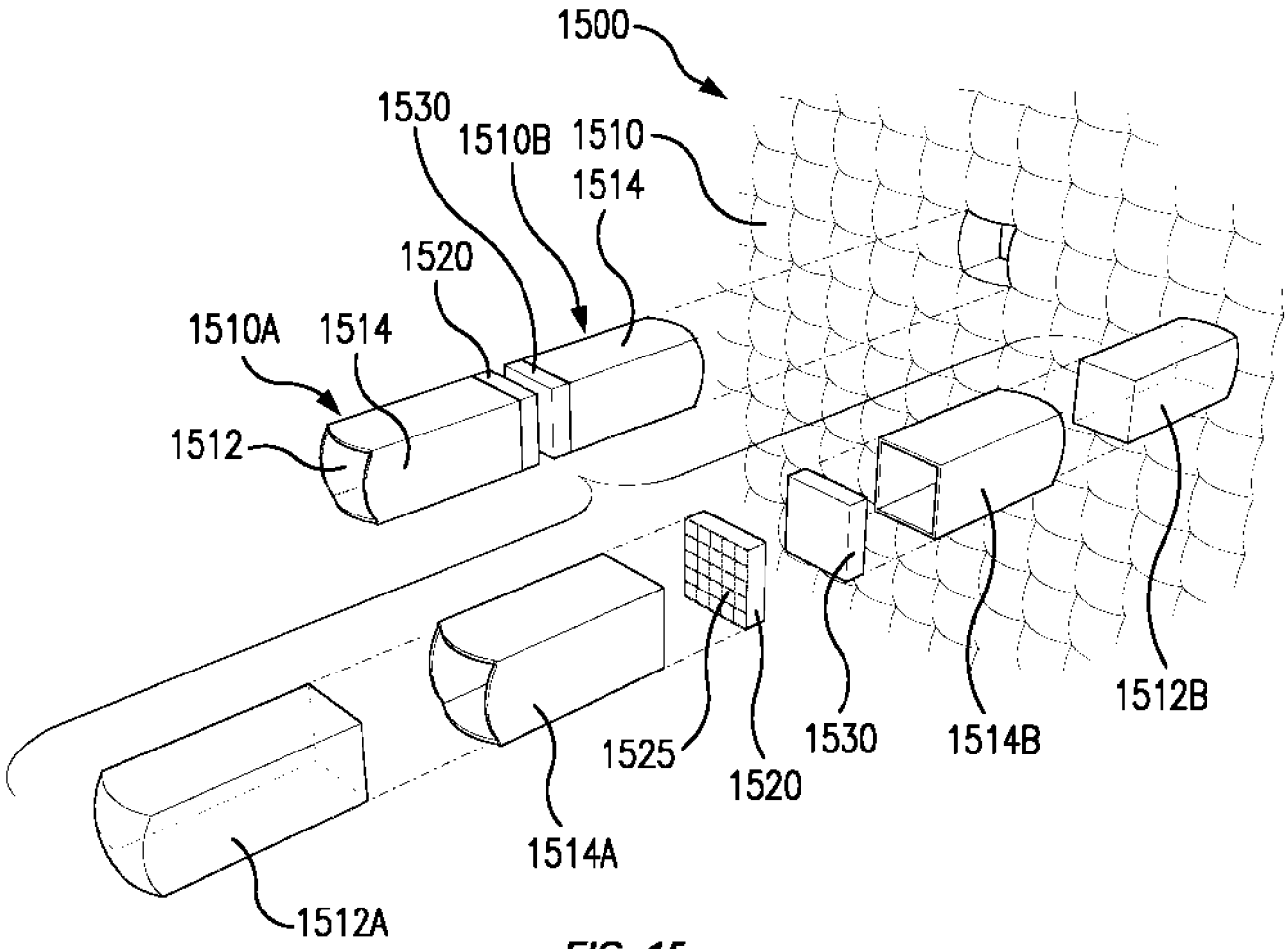
1500
1530
1510B
1510
1514
1520
1510A
1514
1512
1512B
1525
1530
1514B
1520
1514A
1512A

FIG. 15

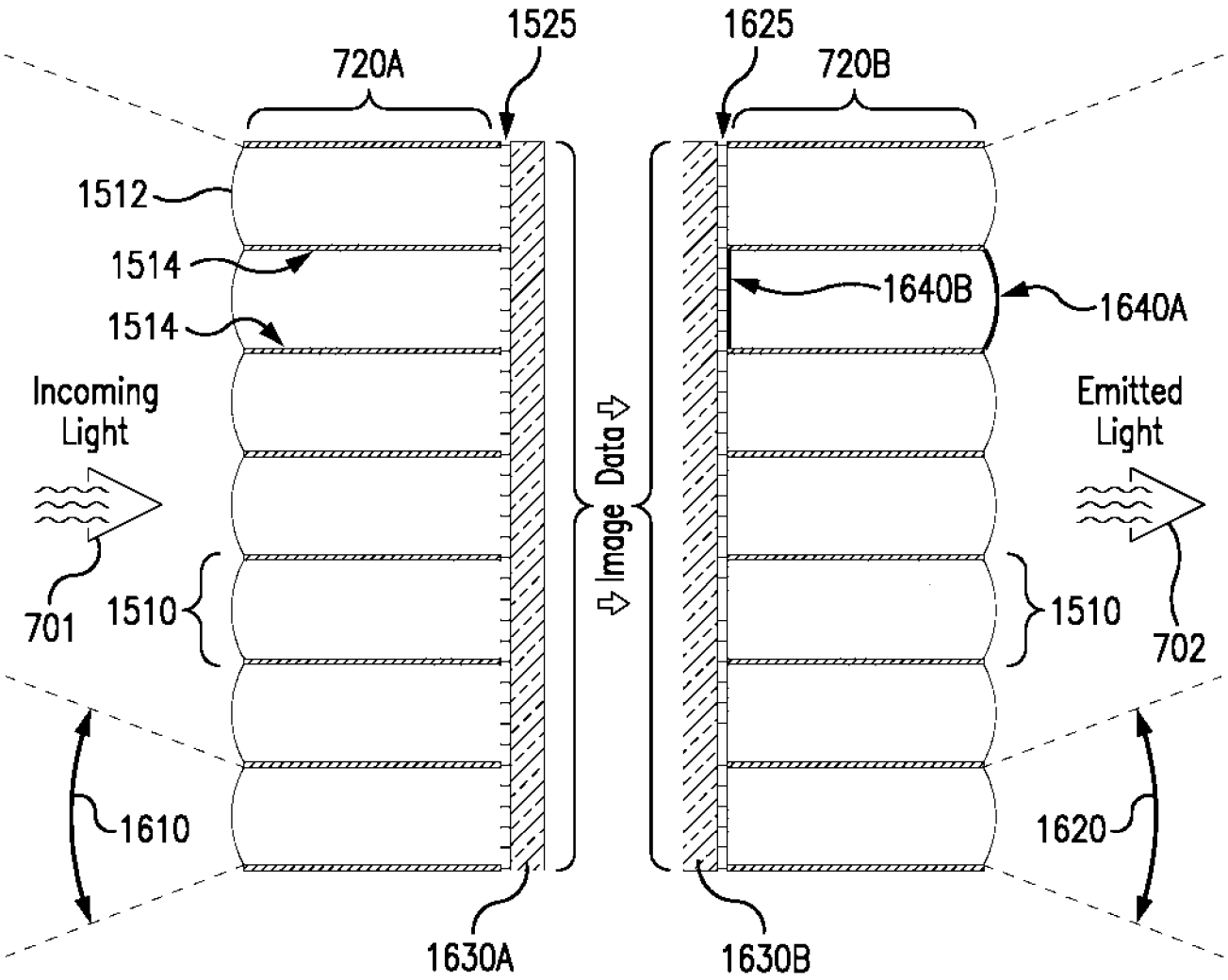
1525
1625
720A
720B
1512
1514
1514
1640B
1640A
Incoming Light
Emitted Light
Image Data
701
1510
1510
702
1610
1620
1630A
1630B

FIG. 16

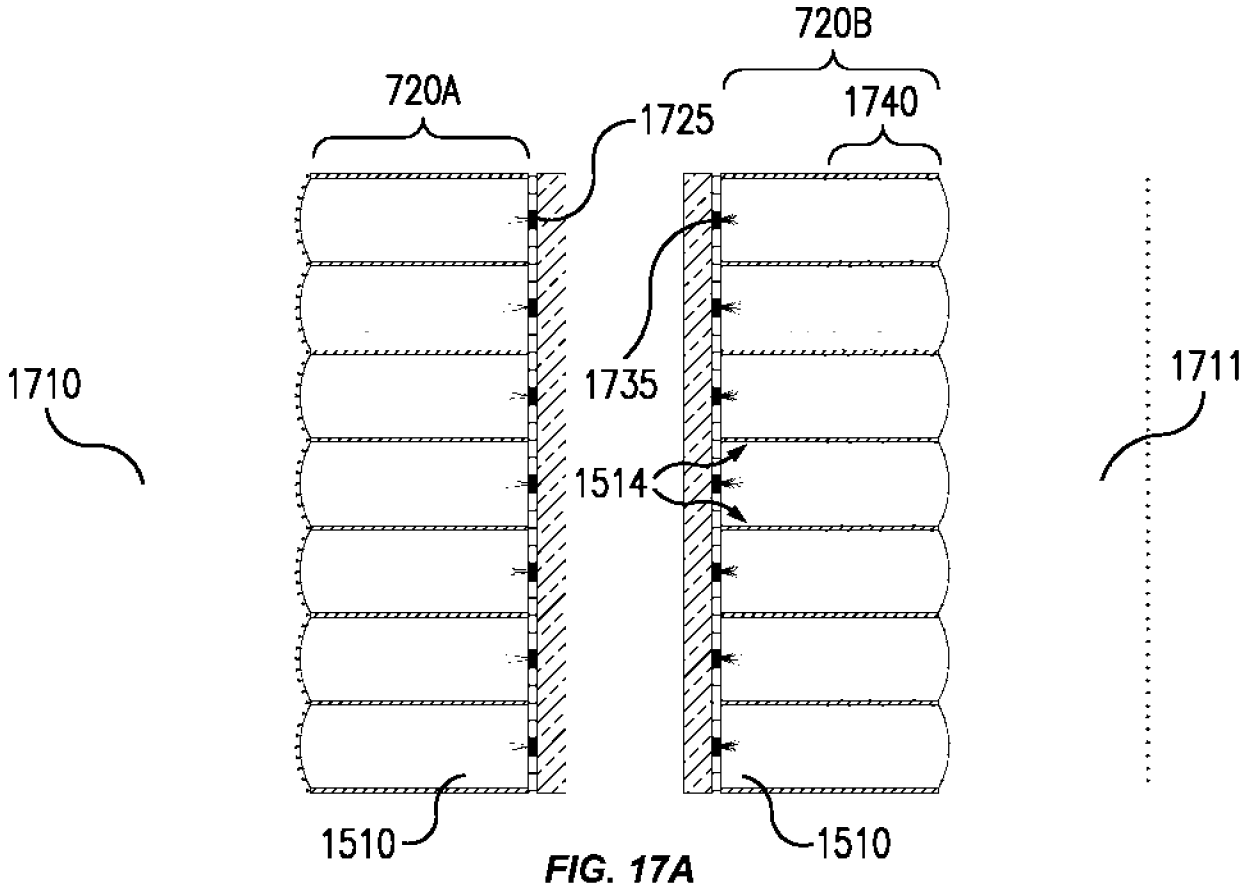

FIG. 17A

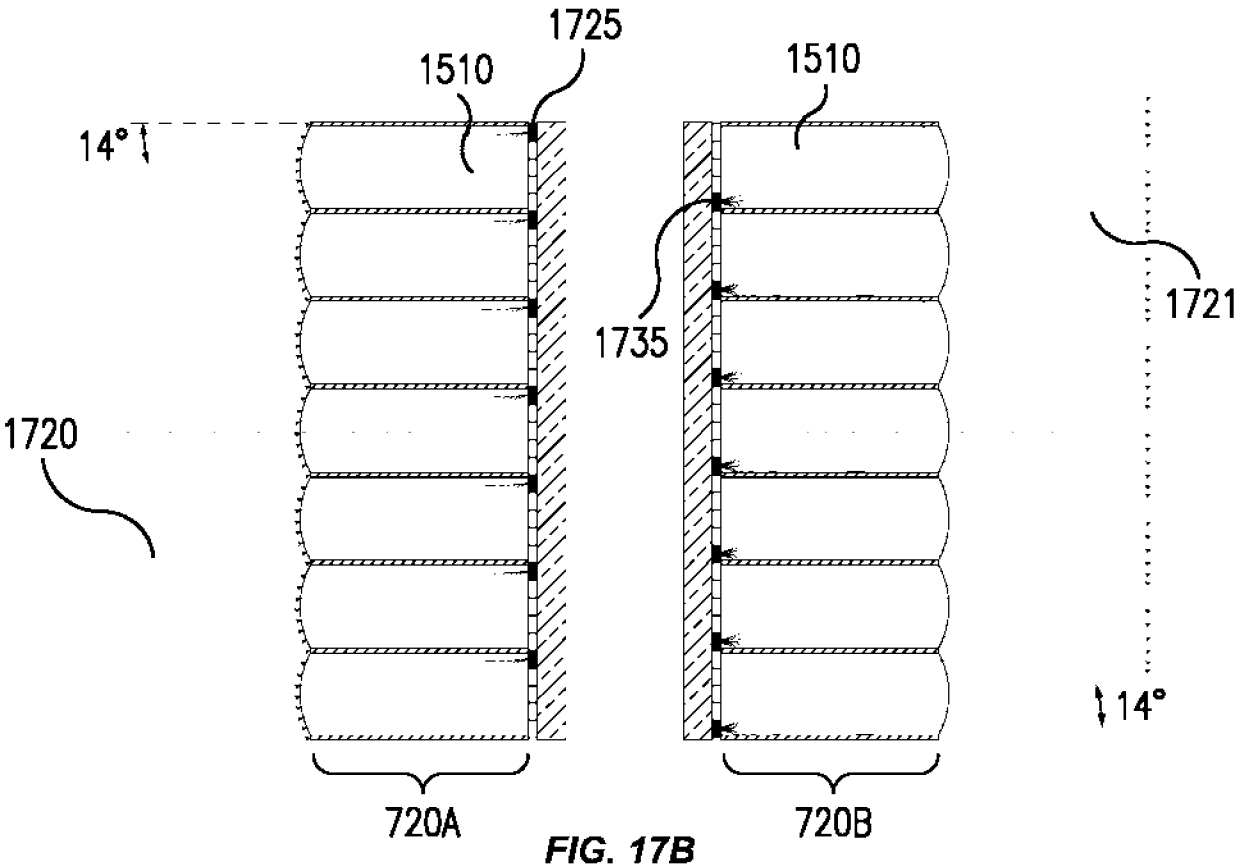

FIG. 17B

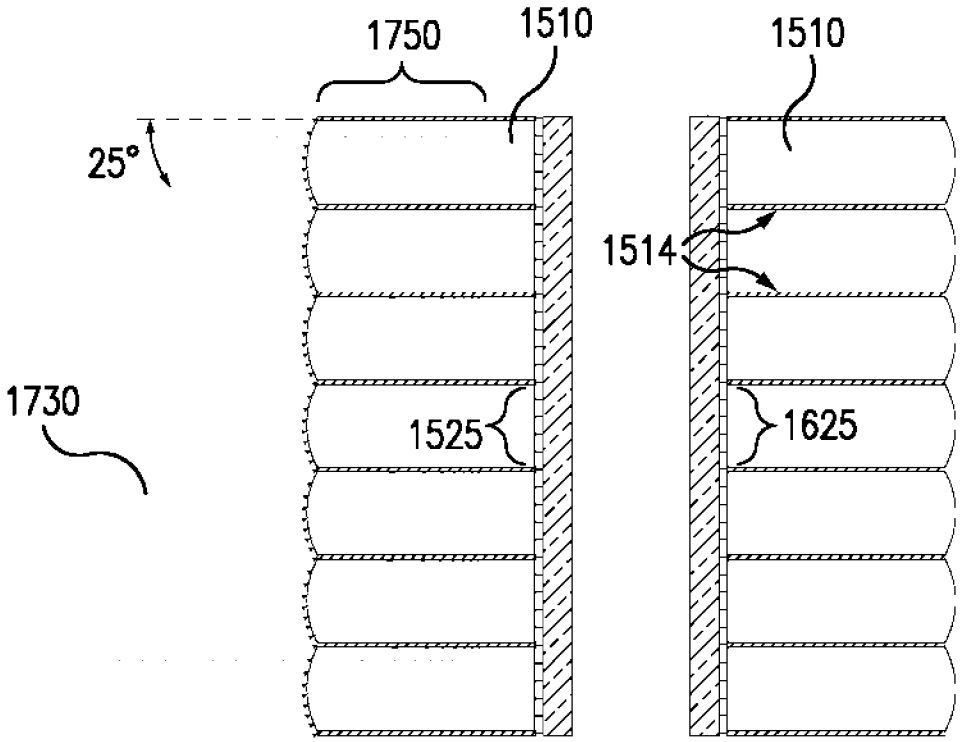

FIG. 17C

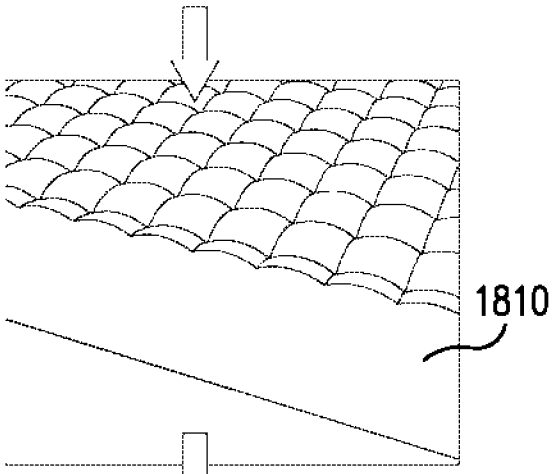

FIG. 18A

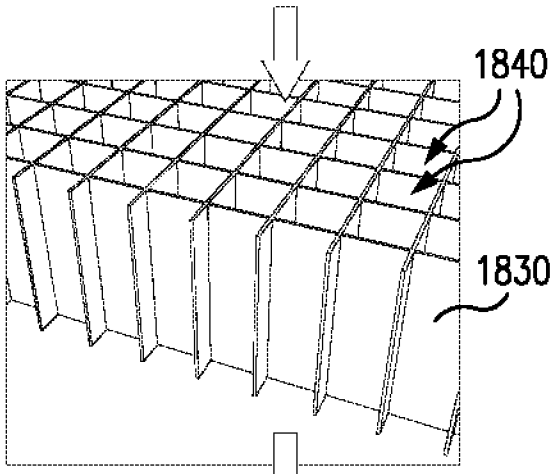

FIG. 19A

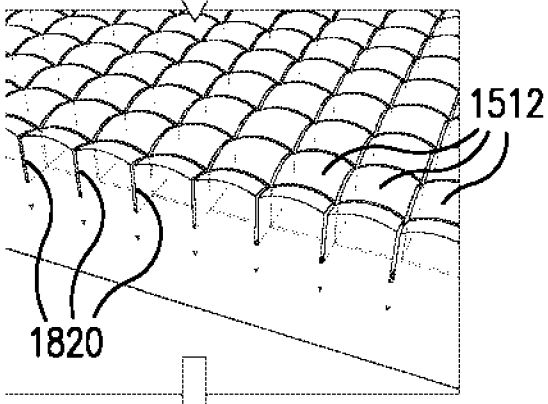

FIG. 18B

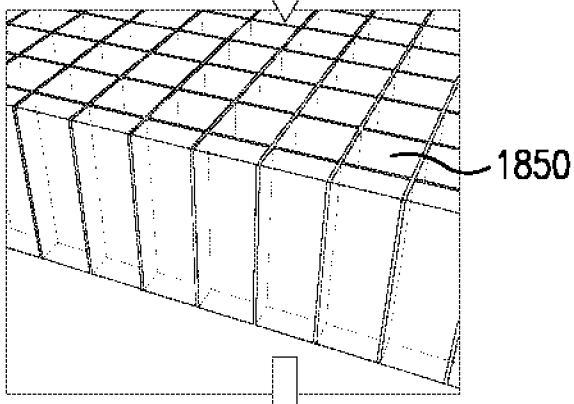

FIG. 19B

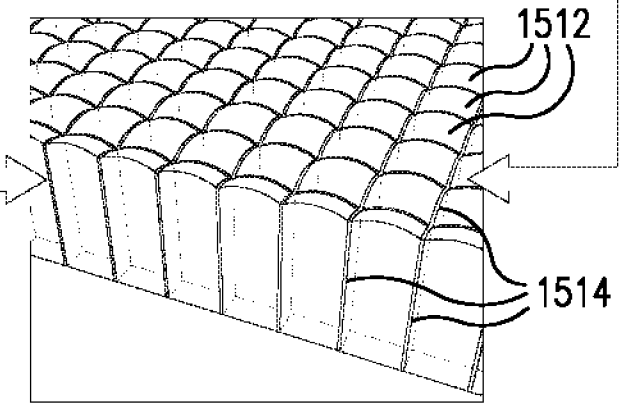

FIG. 20

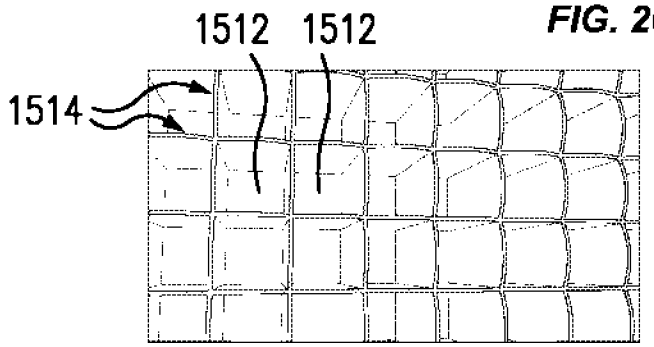

FIG. 21

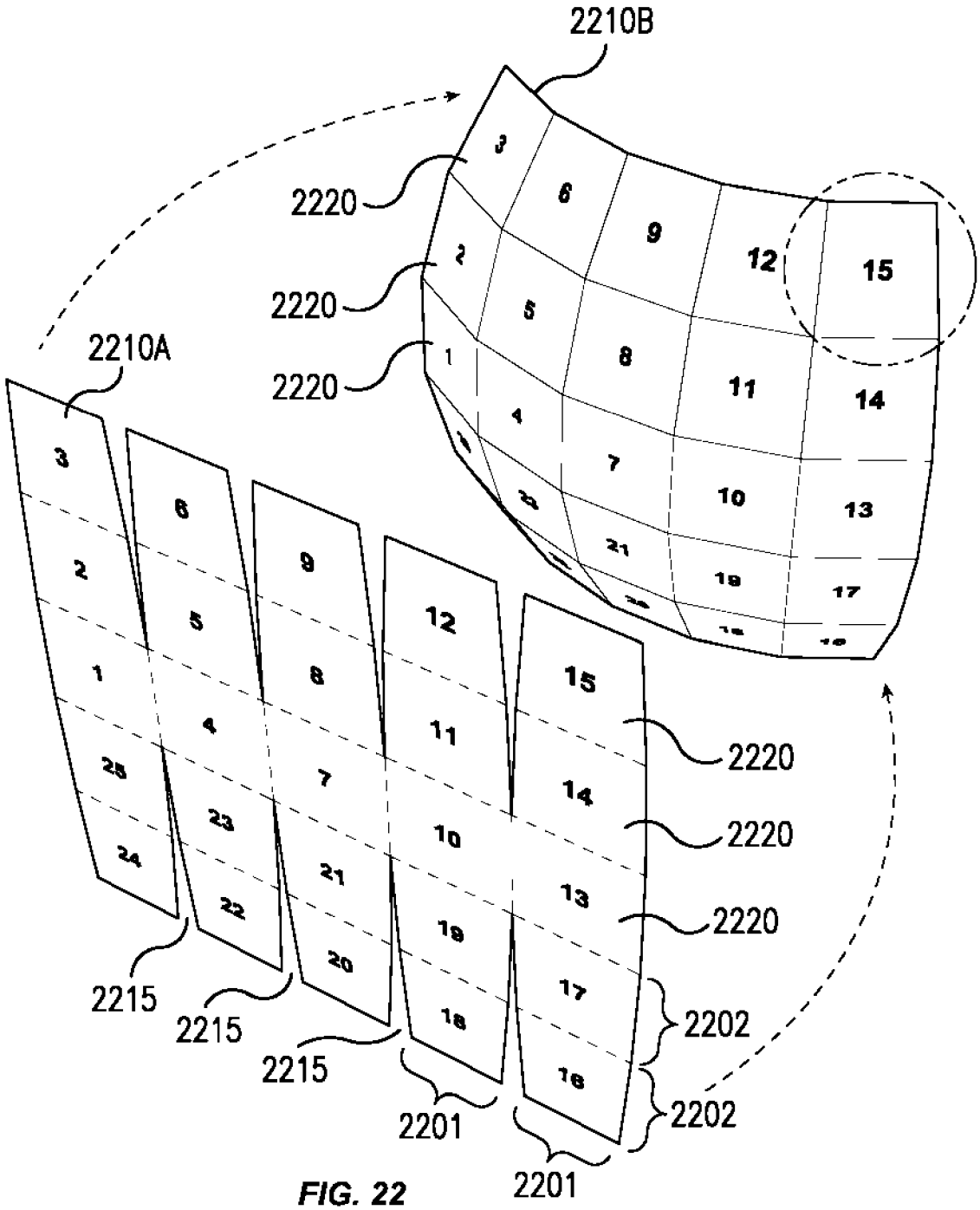
2210B
2220
2220
2220
2210A
2220
2220
2220
2215
2215
2215
2201
2201
2202
2202

FIG. 22

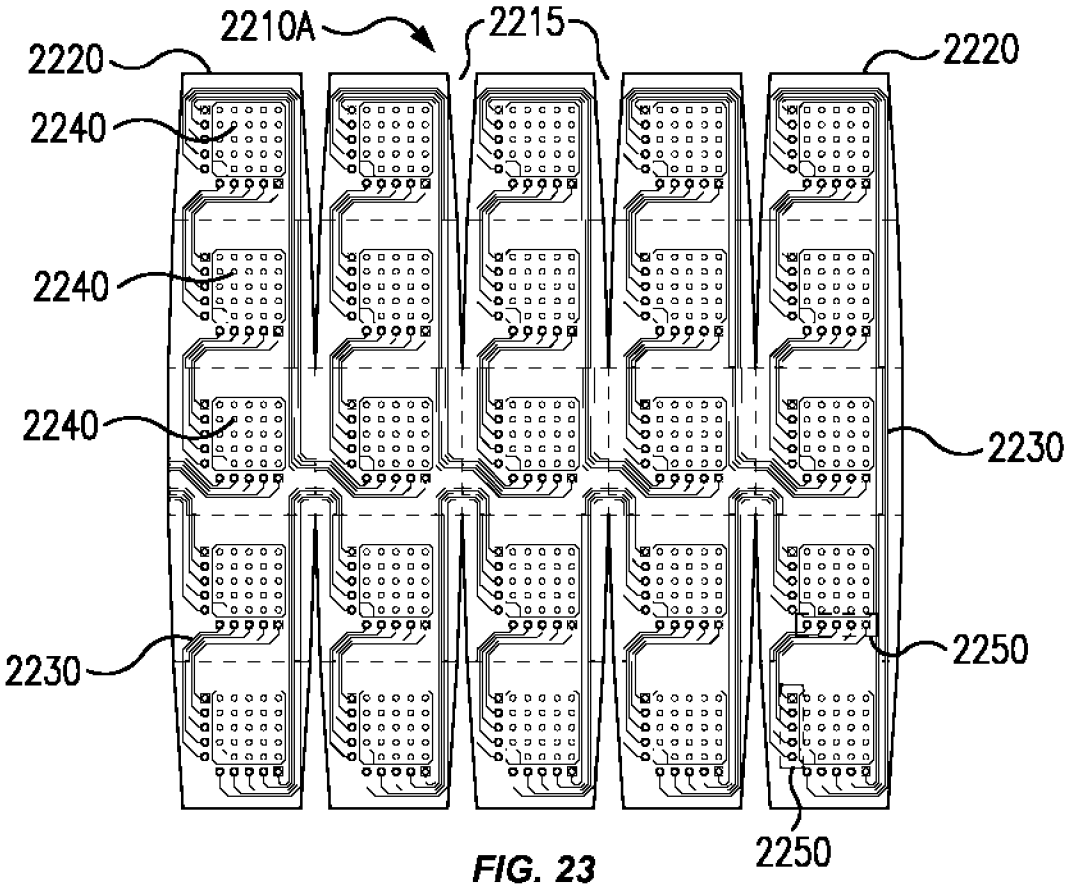
2210A
2215
2220
2220
2240
2240
2240
2230
2230
2250
2250

FIG. 23

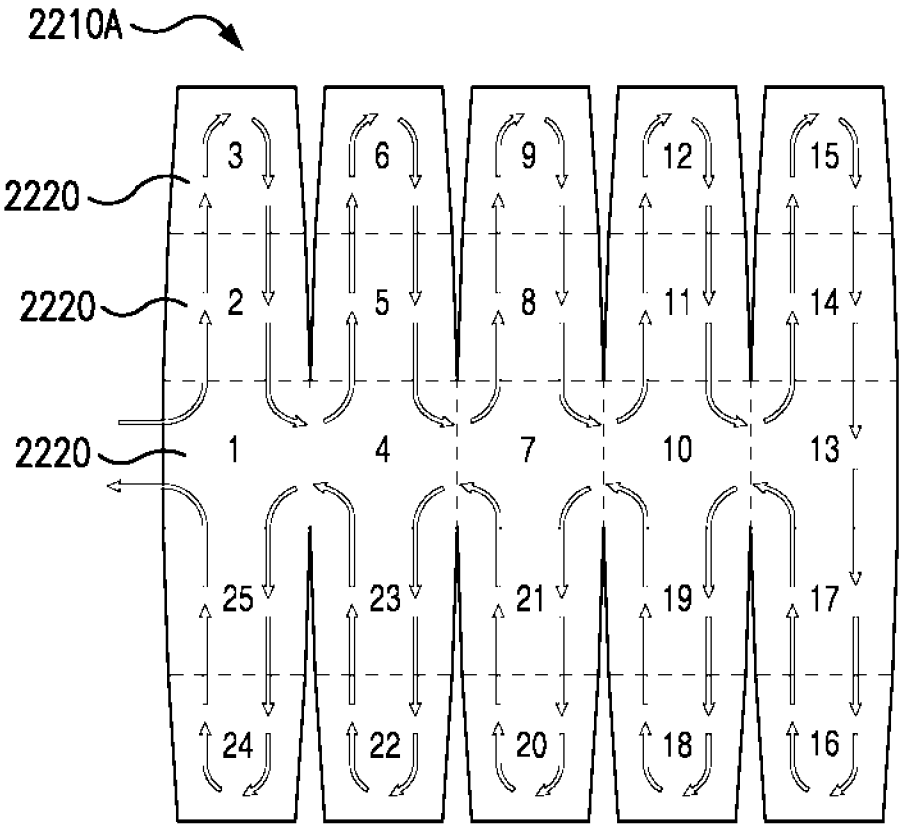
2210A
2220
2220
2220
3
6
9
12
15
2
5
8
11
14
1
4
7
10
13
25
23
21
19
17
24
22
20
18
16

FIG. 24

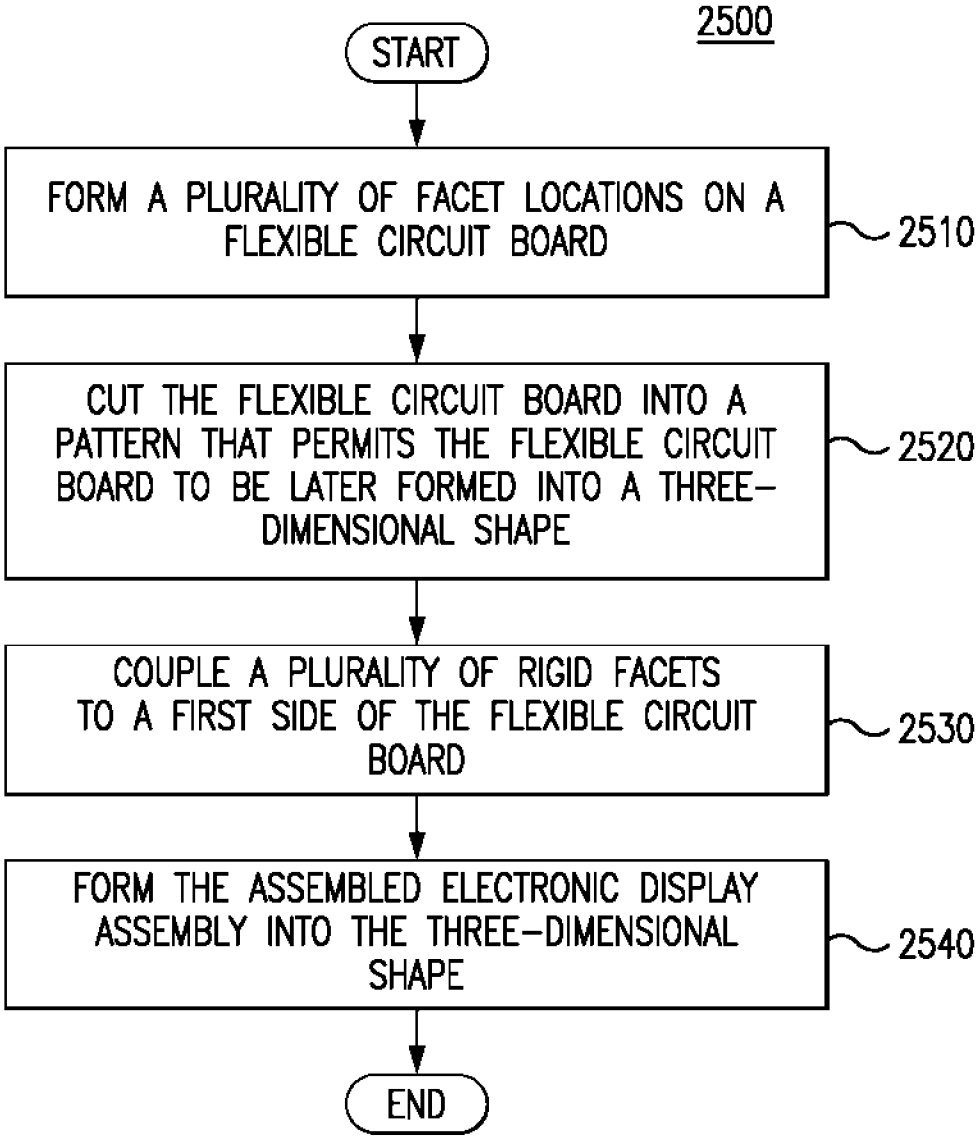
2500
START
FORM A PLURALITY OF FACET LOCATIONS ON A FLEXIBLE CIRCUIT BOARD
2510
CUT THE FLEXIBLE CIRCUIT BOARD INTO A PATTERN THAT PERMITS THE FLEXIBLE CIRCUIT BOARD TO BE LATER FORMED INTO A THREE-DIMENSIONAL SHAPE
2520
COUPLE A PLURALITY OF RIGID FACETS TO A FIRST SIDE OF THE FLEXIBLE CIRCUIT BOARD
2530
FORM THE ASSEMBLED ELECTRONIC DISPLAY ASSEMBLY INTO THE THREE-DIMENSIONAL SHAPE
2540
END

FIG. 25

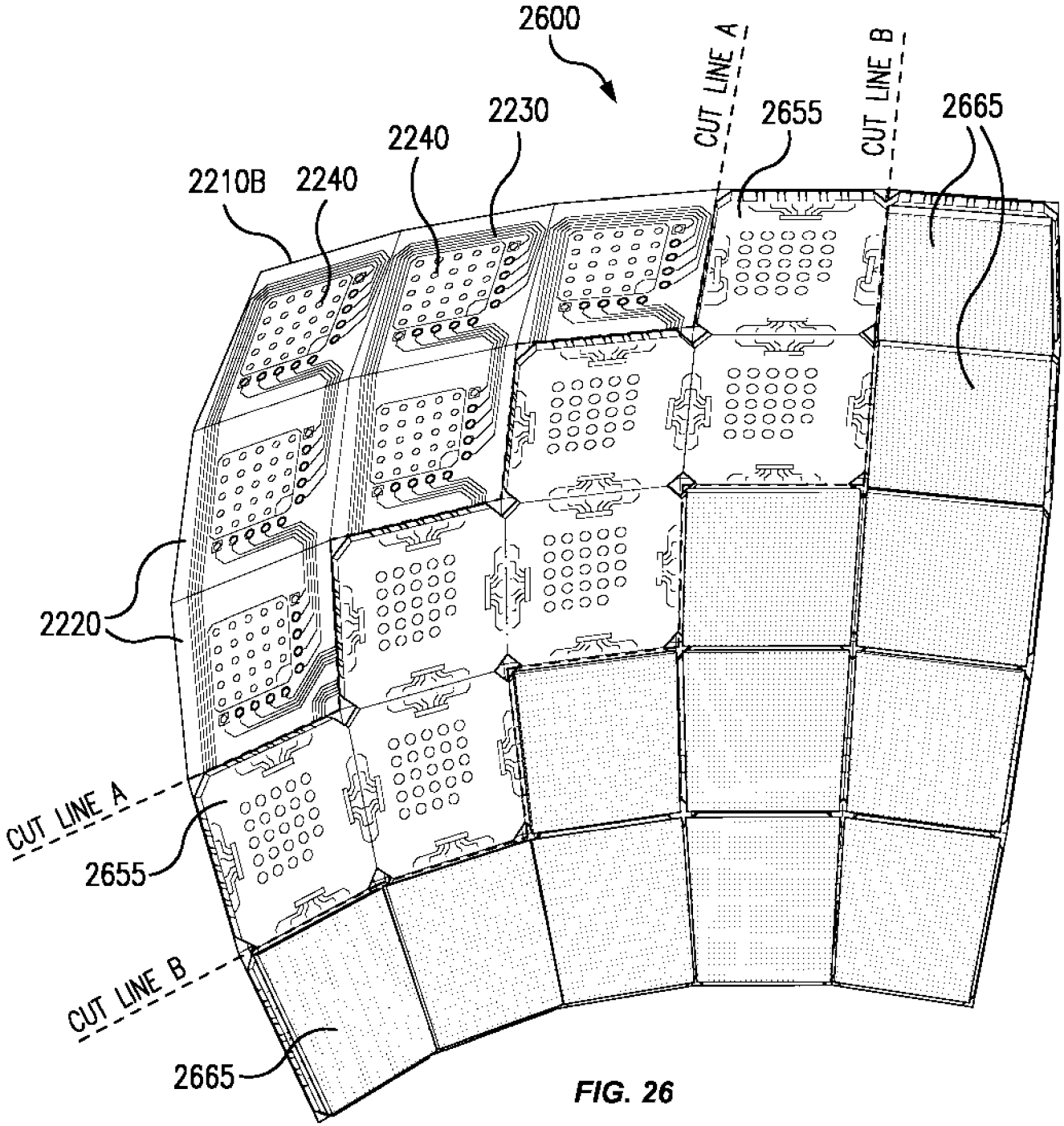
2600
CUT LINE A
2655
CUT LINE B
2665
2230
2240
2210B
2240
2220
CUT LINE A
2655
CUT LINE B
2665

FIG. 26

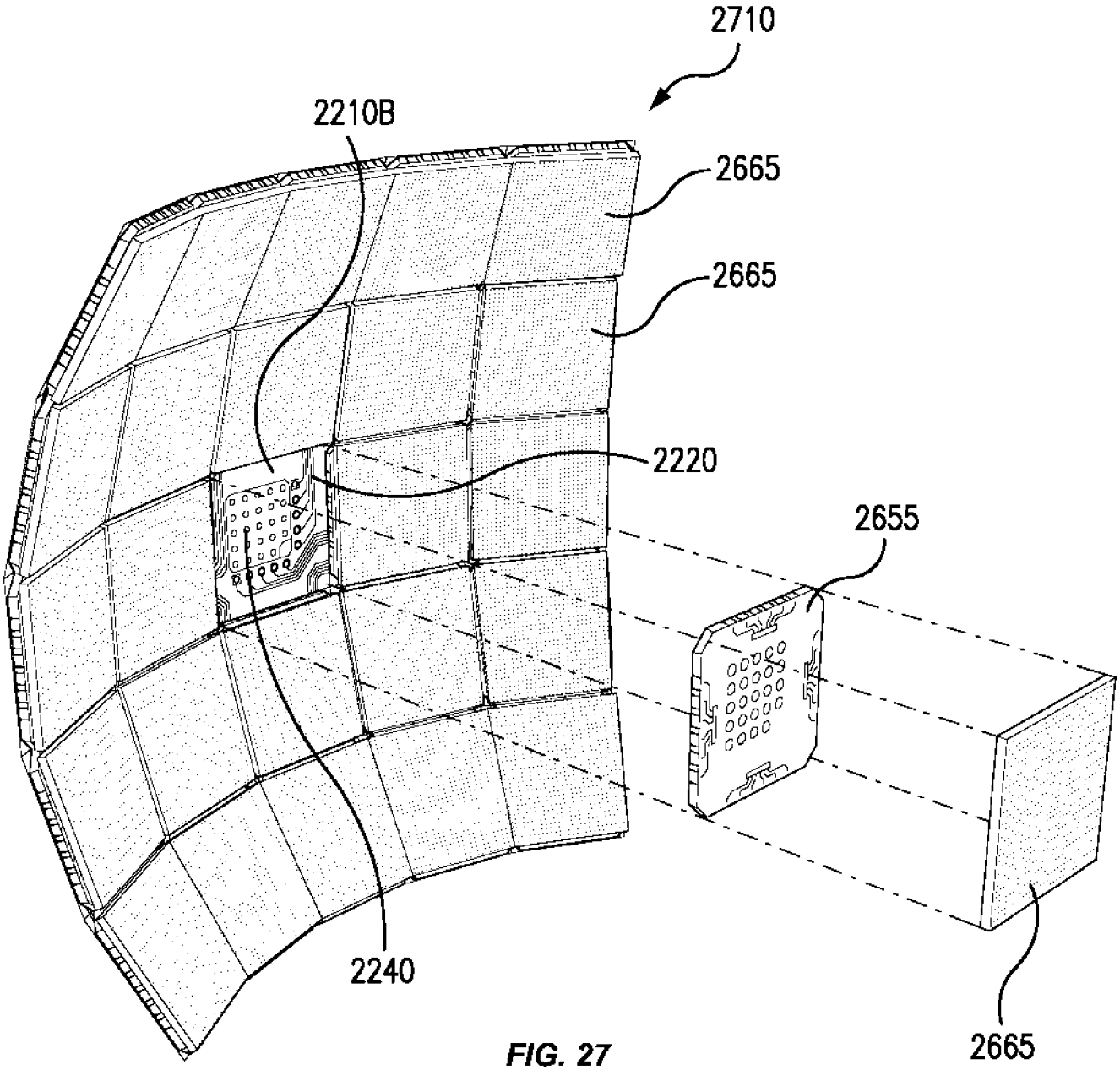

FIG. 27

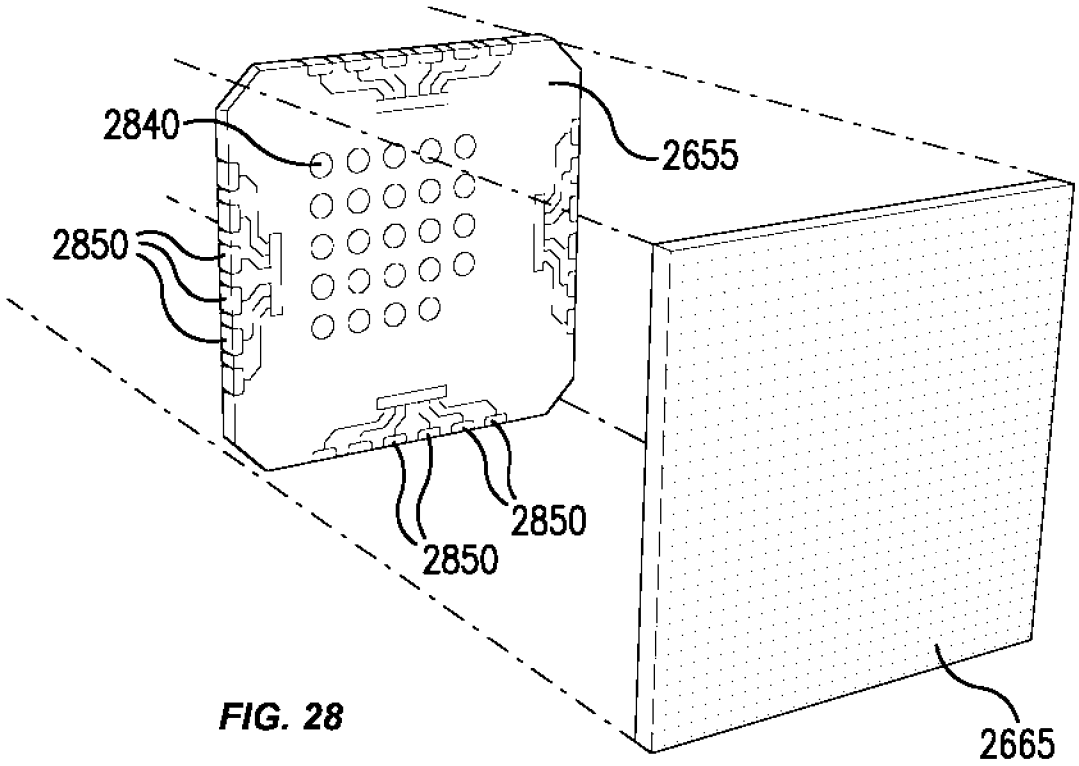

FIG. 28

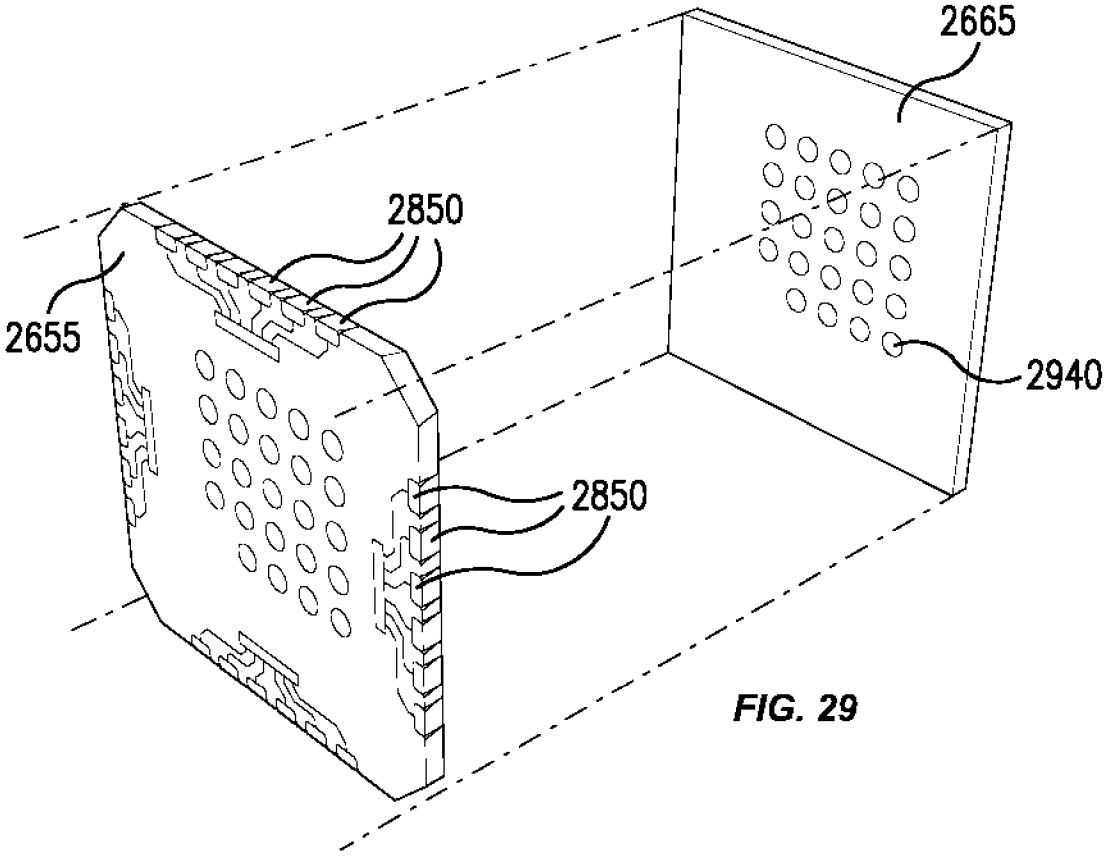

FIG. 29

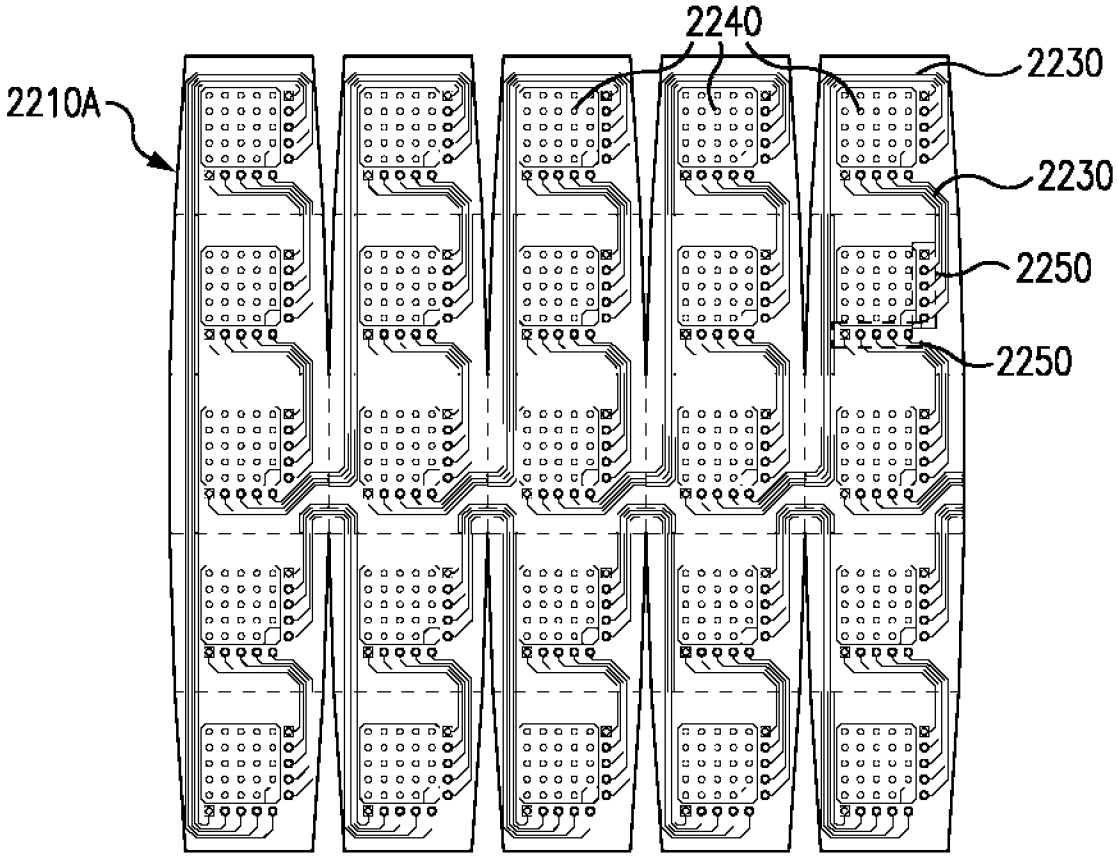
2240
2230
2210A
2230
2250
2250

FIG. 30

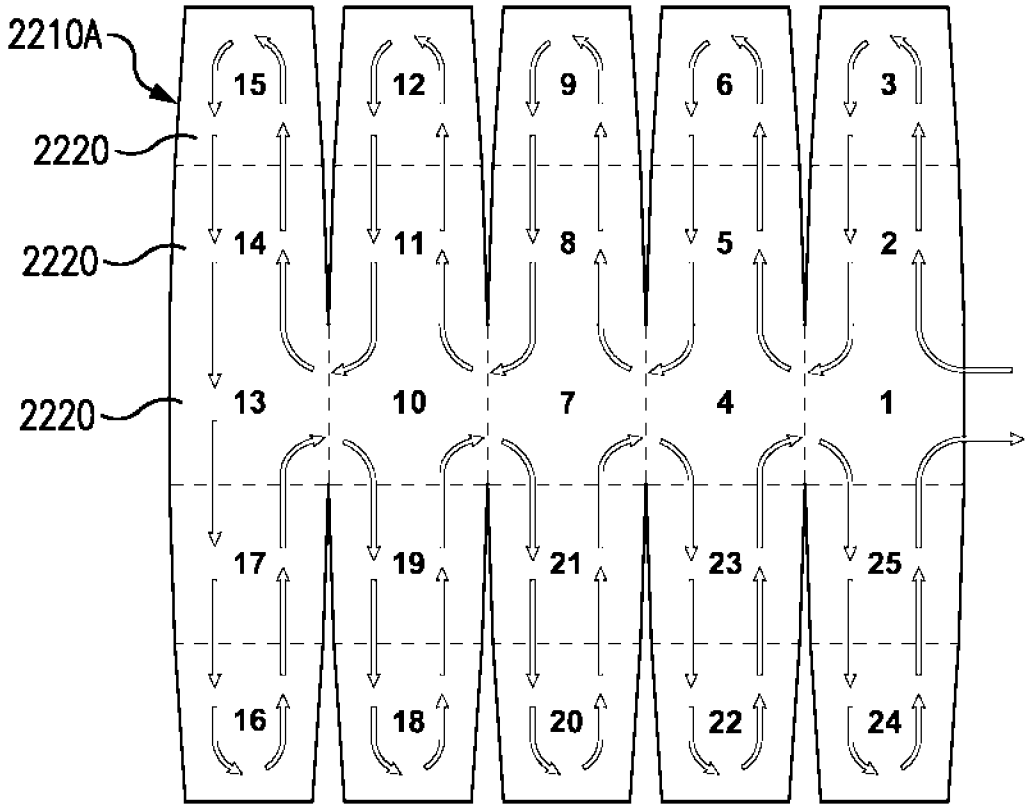
2210A
2220
2220
2220
15
12
9
6
3
14
11
8
5
2
13
10
7
4
1
17
19
21
23
25
16
18
20
22
24

FIG. 31

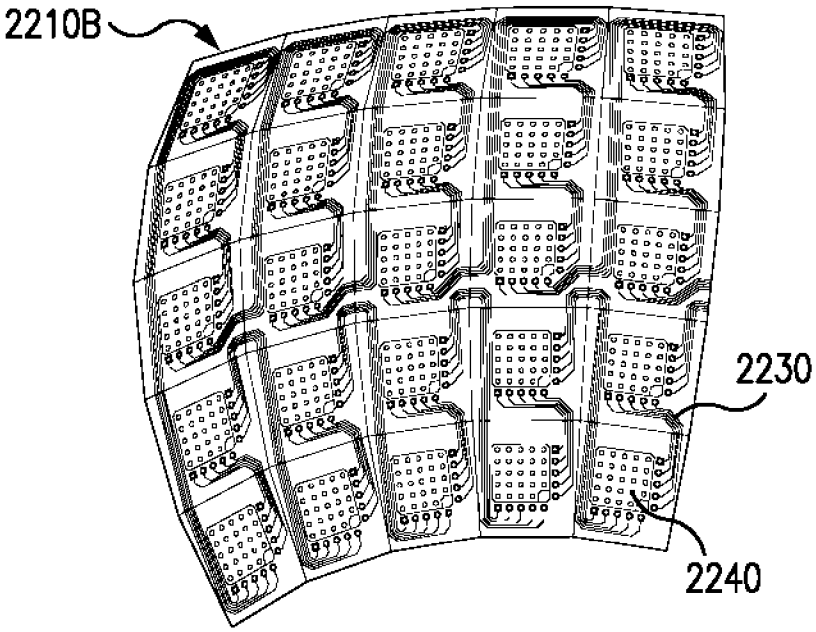
2210B
2230
2240

FIG. 32

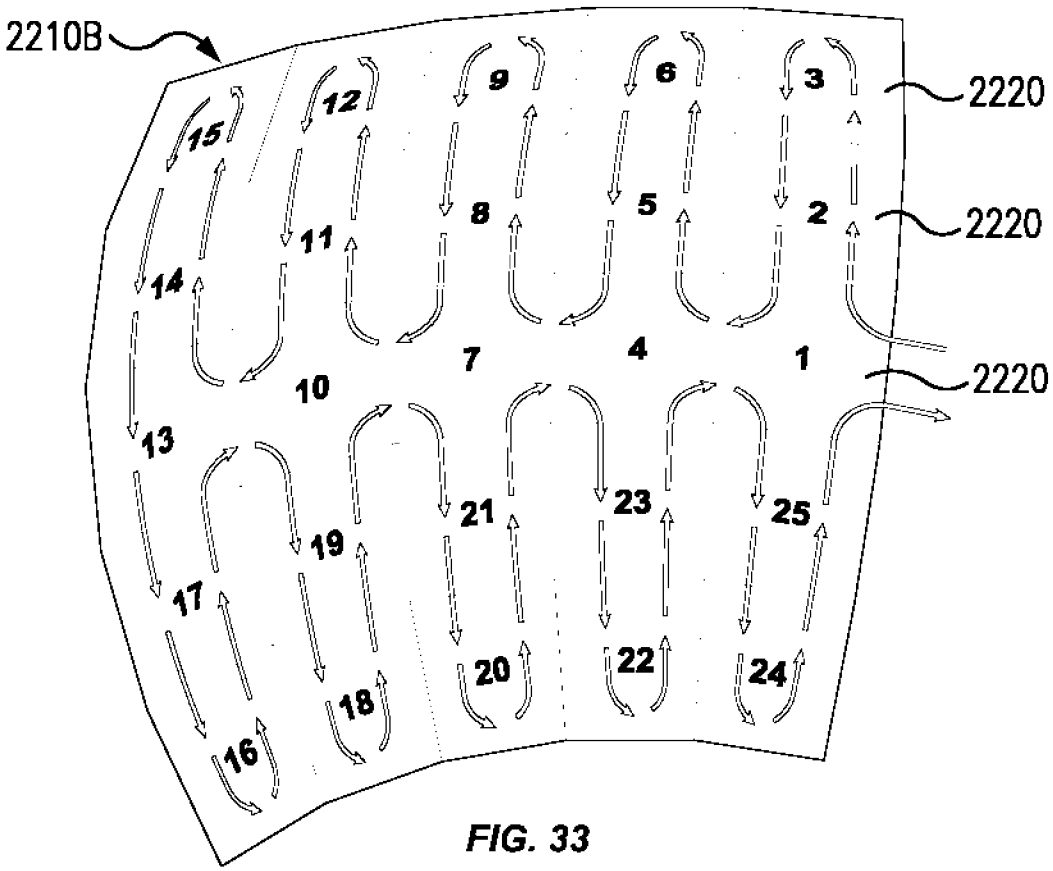
2210B
2220
2220
2220
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

FIG. 33

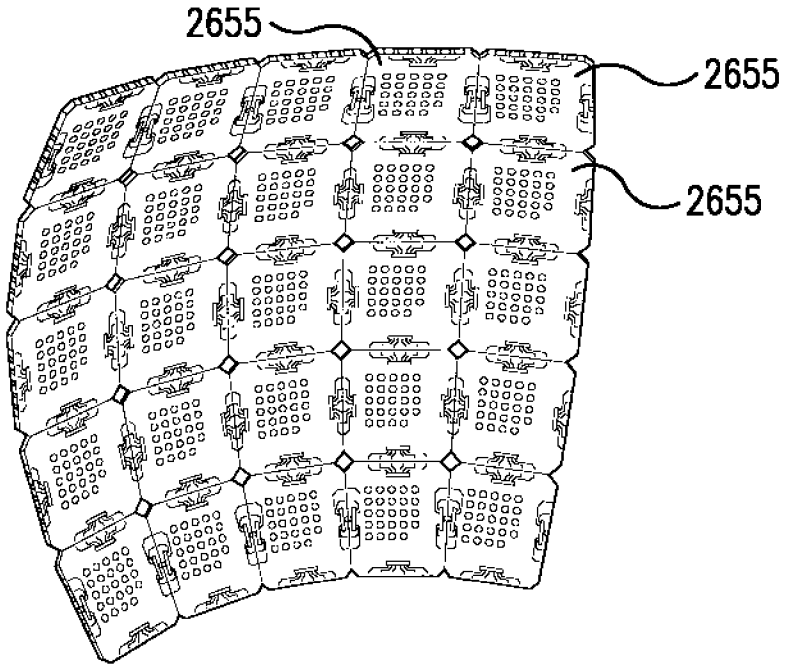
2655
2655
2655

FIG. 34

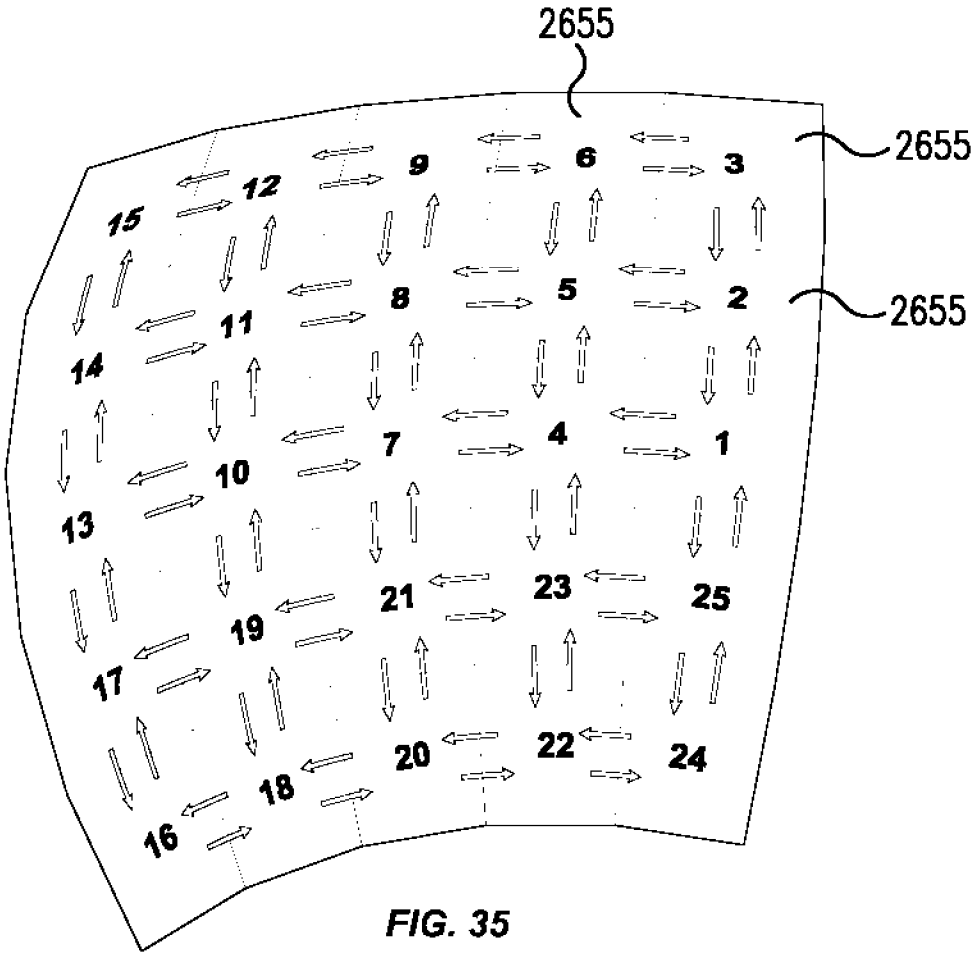
2655
2655
2655
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

FIG. 35

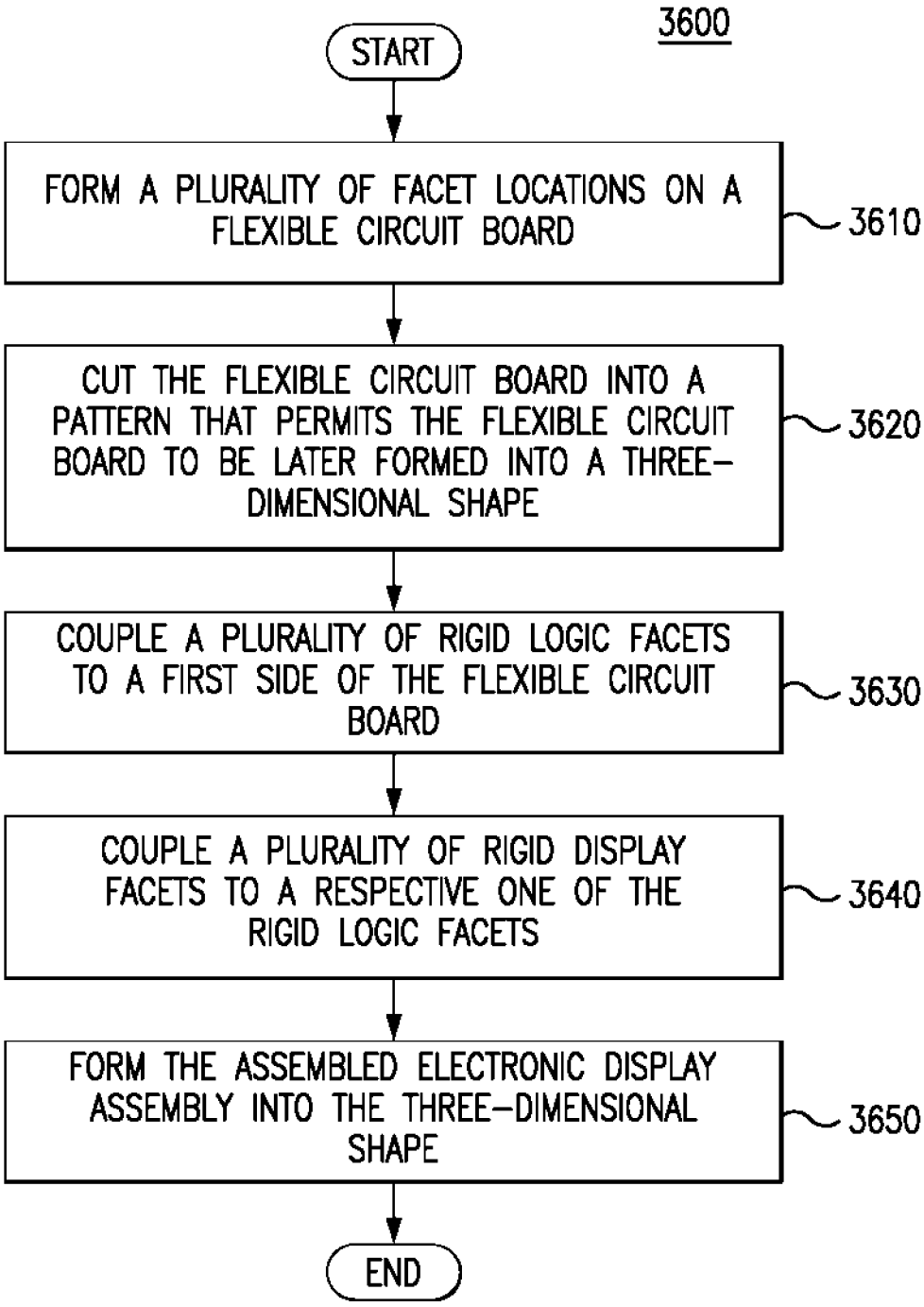
3600
START
FORM A PLURALITY OF FACET LOCATIONS ON A FLEXIBLE CIRCUIT BOARD
3610
CUT THE FLEXIBLE CIRCUIT BOARD INTO A PATTERN THAT PERMITS THE FLEXIBLE CIRCUIT BOARD TO BE LATER FORMED INTO A THREE-DIMENSIONAL SHAPE
3620
COUPLE A PLURALITY OF RIGID LOGIC FACETS TO A FIRST SIDE OF THE FLEXIBLE CIRCUIT BOARD
3630
COUPLE A PLURALITY OF RIGID DISPLAY FACETS TO A RESPECTIVE ONE OF THE RIGID LOGIC FACETS
3640
FORM THE ASSEMBLED ELECTRONIC DISPLAY ASSEMBLY INTO THE THREE-DIMENSIONAL SHAPE
3650
END

FIG. 36

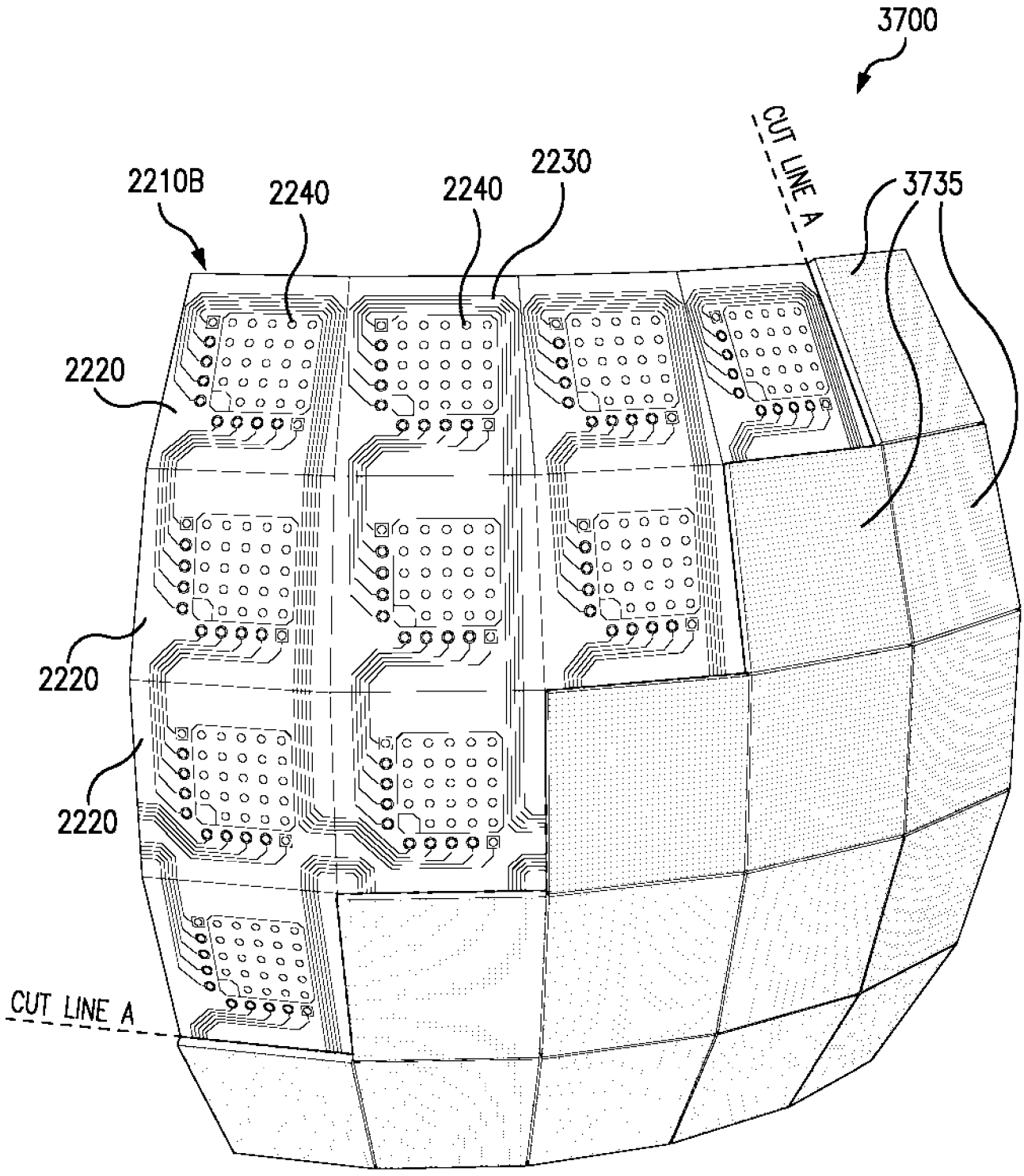
3700
CUT LINE A
2210B
2240
2240
2230
3735
2220
2220
2220
CUT LINE A

FIG. 37

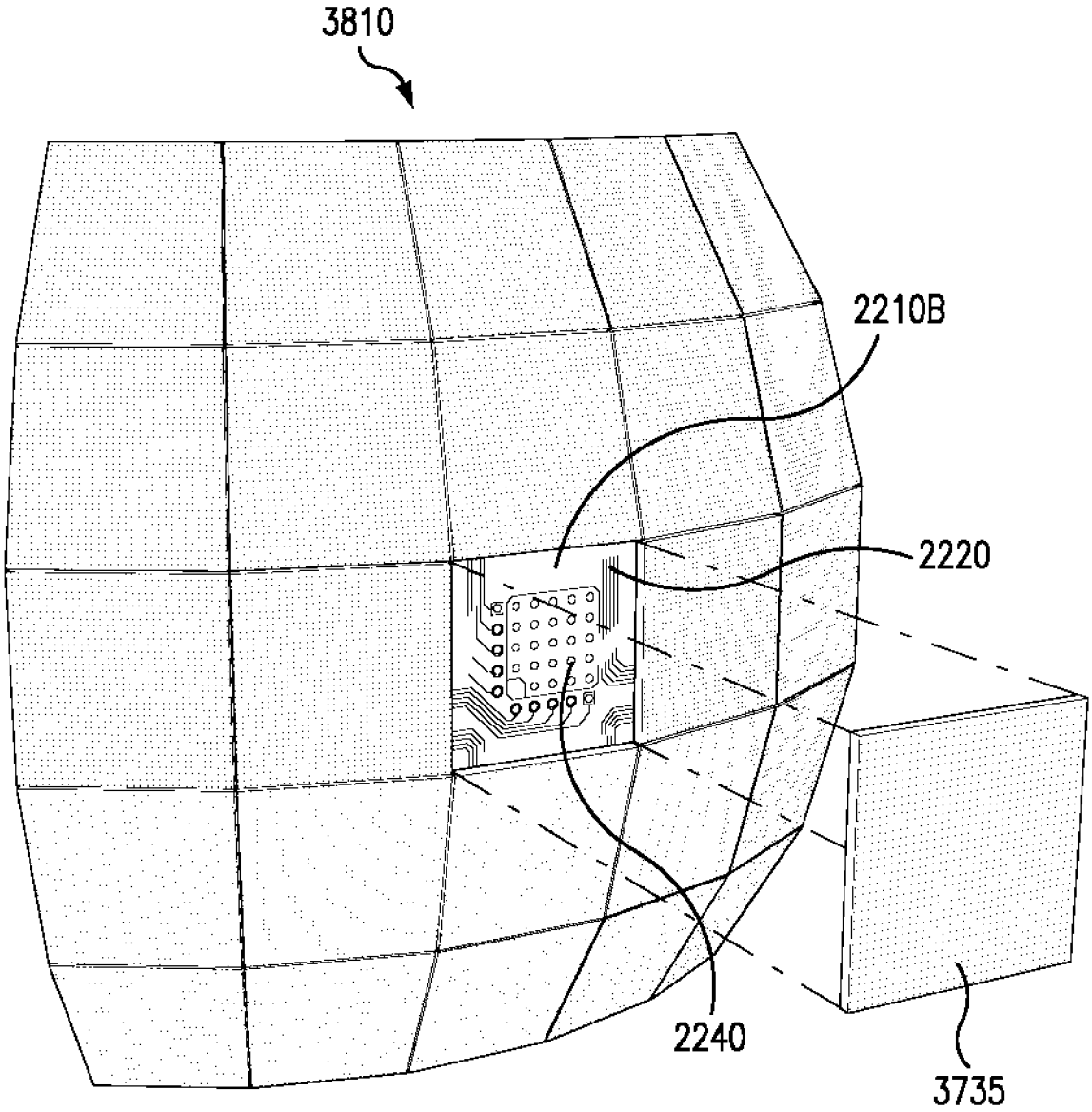

FIG. 38

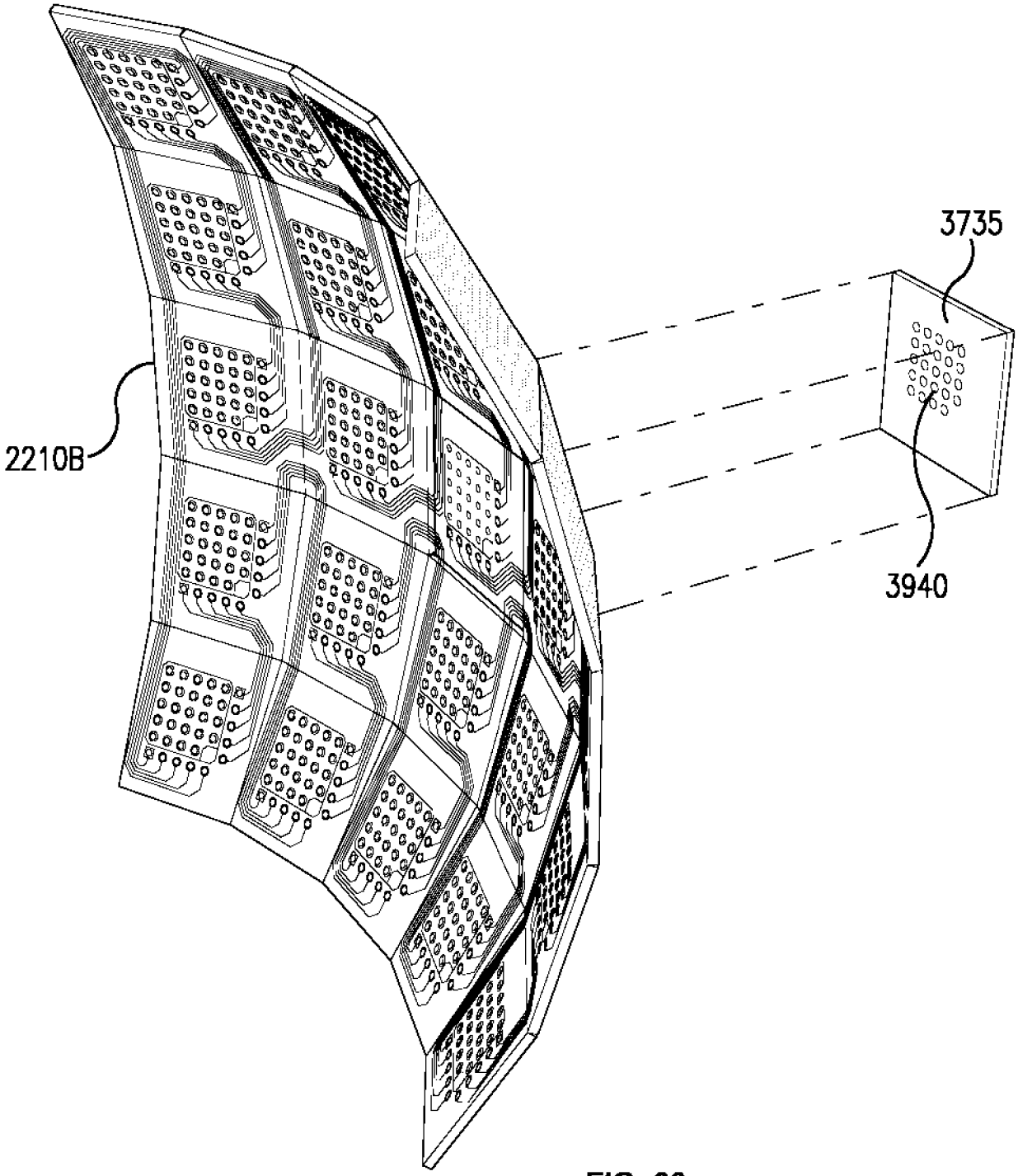

FIG. 39

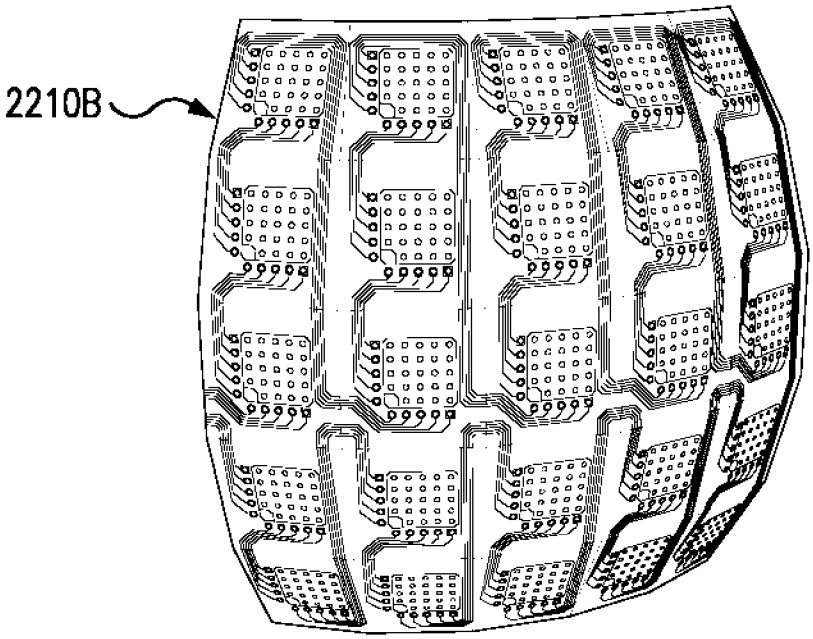

FIG. 40

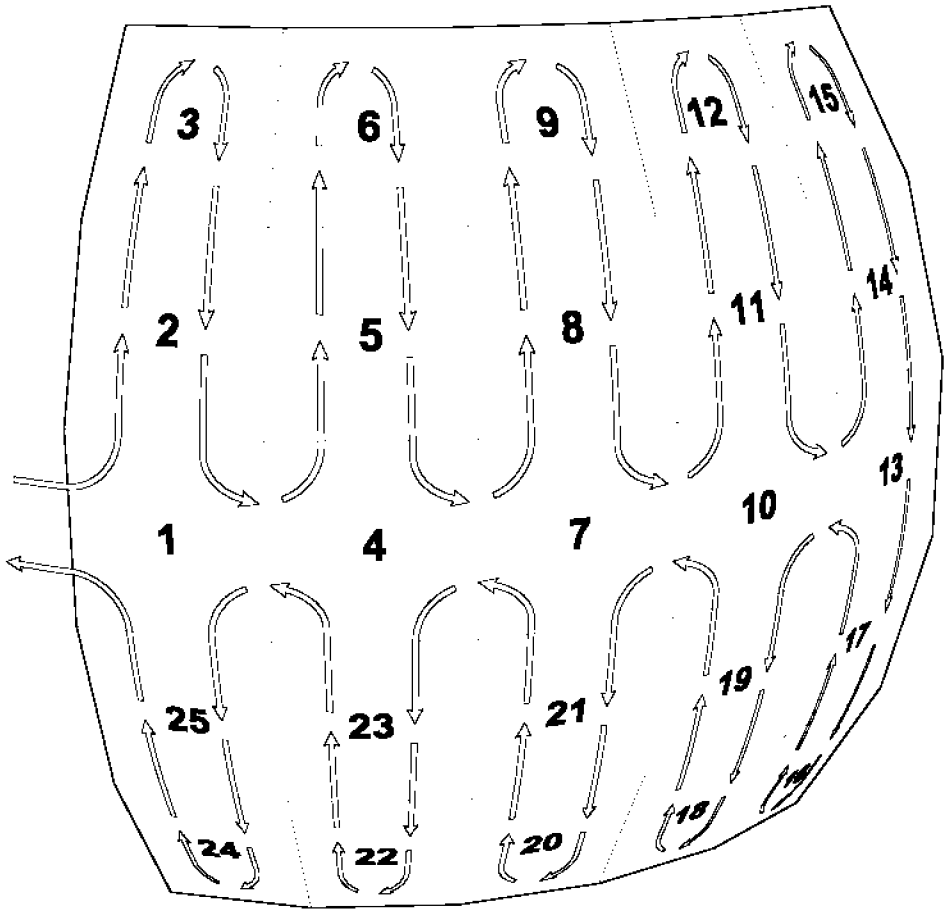

FIG. 41

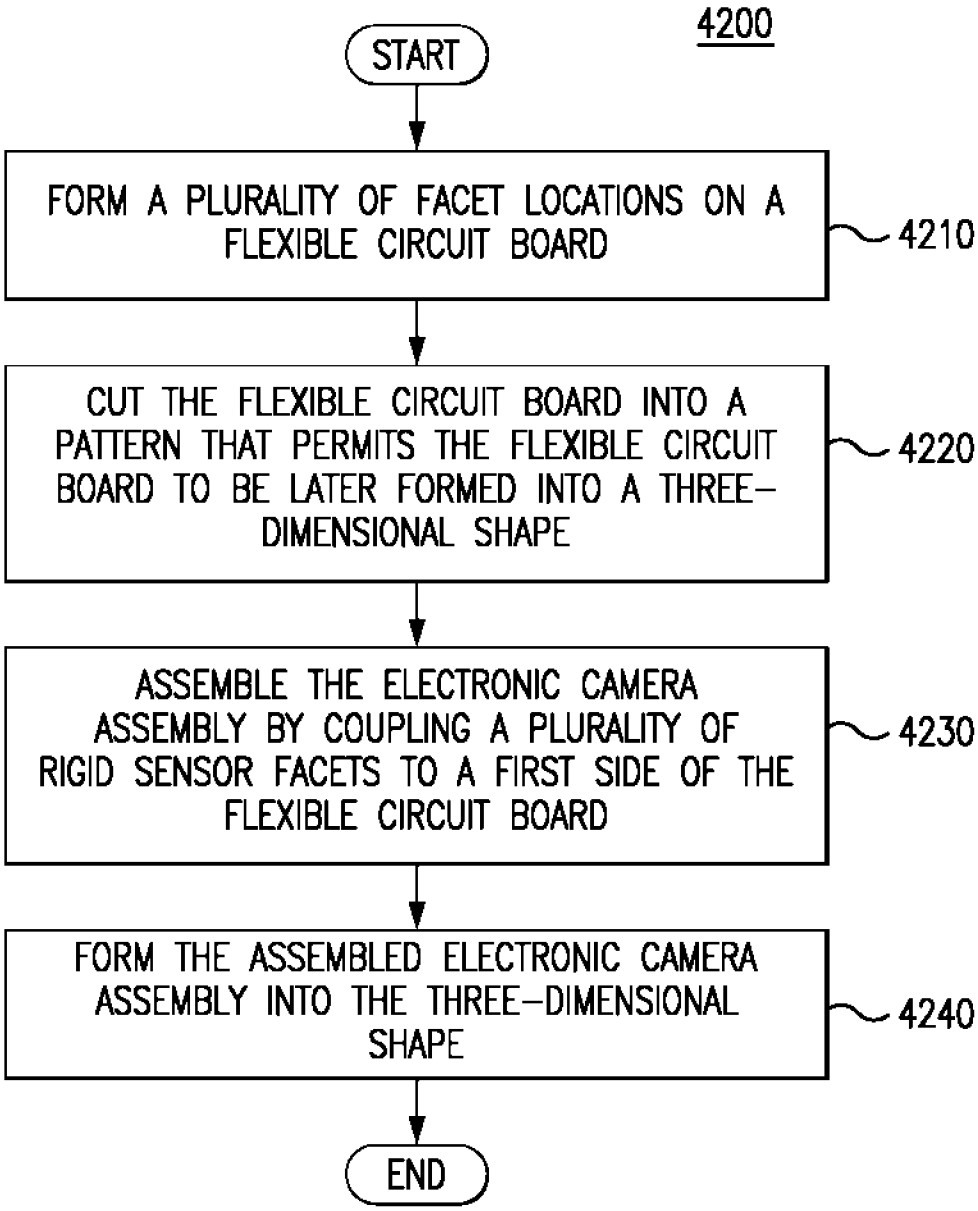
4200
START
FORM A PLURALITY OF FACET LOCATIONS ON A FLEXIBLE CIRCUIT BOARD
4210
CUT THE FLEXIBLE CIRCUIT BOARD INTO A PATTERN THAT PERMITS THE FLEXIBLE CIRCUIT BOARD TO BE LATER FORMED INTO A THREE-DIMENSIONAL SHAPE
4220
ASSEMBLE THE ELECTRONIC CAMERA ASSEMBLY BY COUPLING A PLURALITY OF RIGID SENSOR FACETS TO A FIRST SIDE OF THE FLEXIBLE CIRCUIT BOARD
4230
FORM THE ASSEMBLED ELECTRONIC CAMERA ASSEMBLY INTO THE THREE-DIMENSIONAL SHAPE
4240
END

FIG. 42

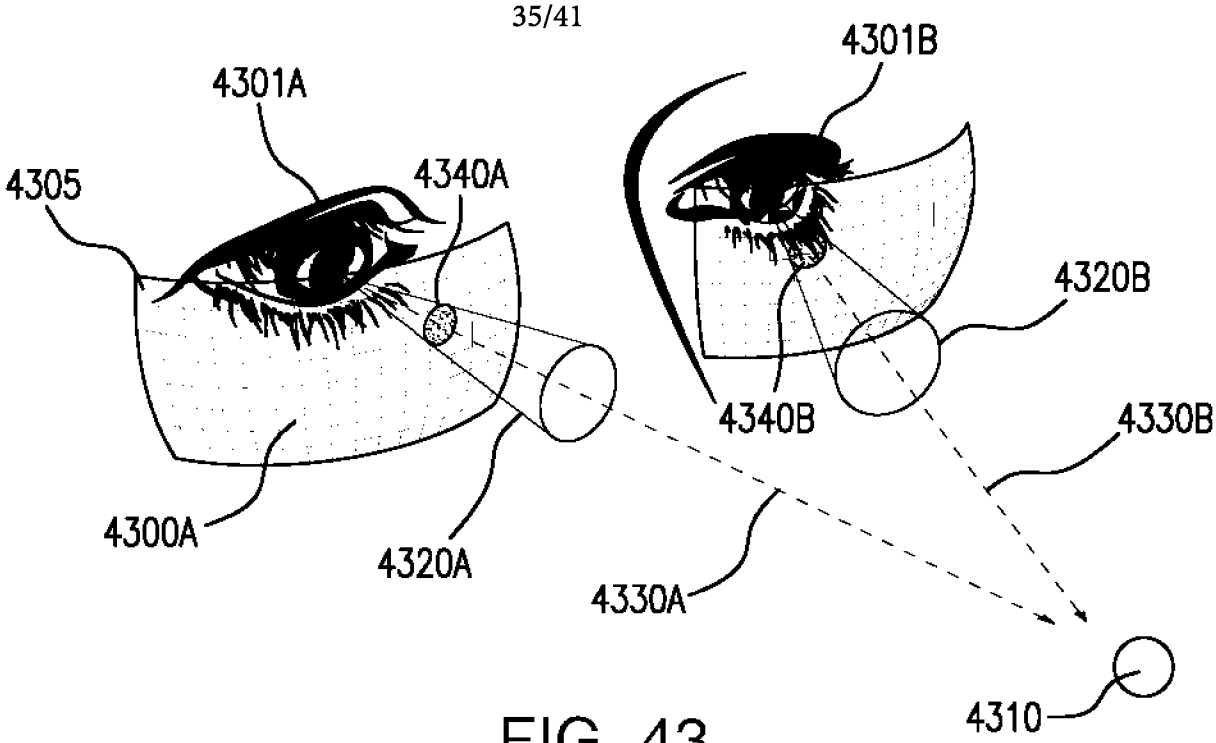
4301A
4301B
4305
4340A
4320B
4340B
4330B
4300A
4320A
4330A
4310

FIG. 43

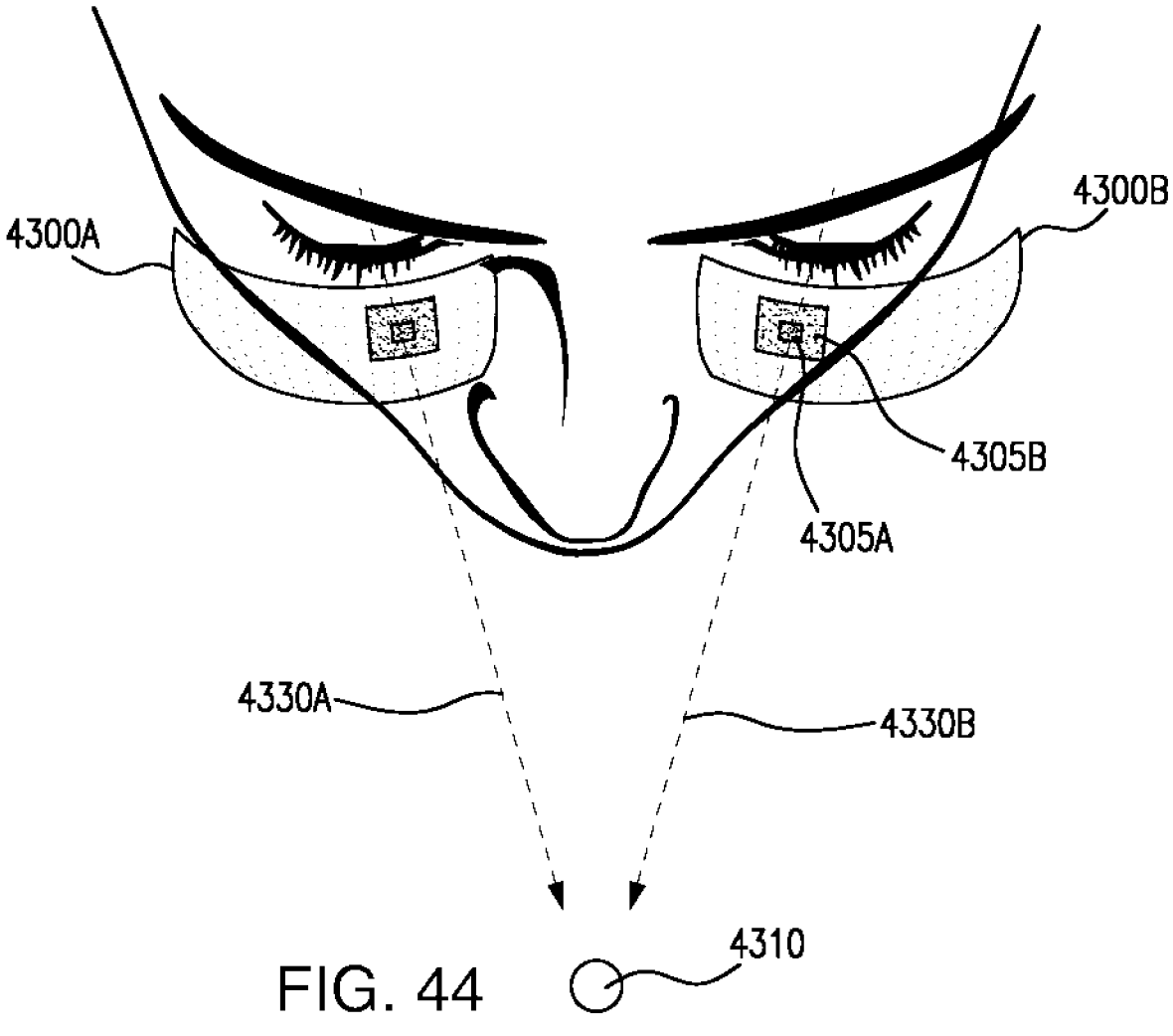
4300A
4300B
4305B
4305A
4330A
4330B
4310

FIG. 44

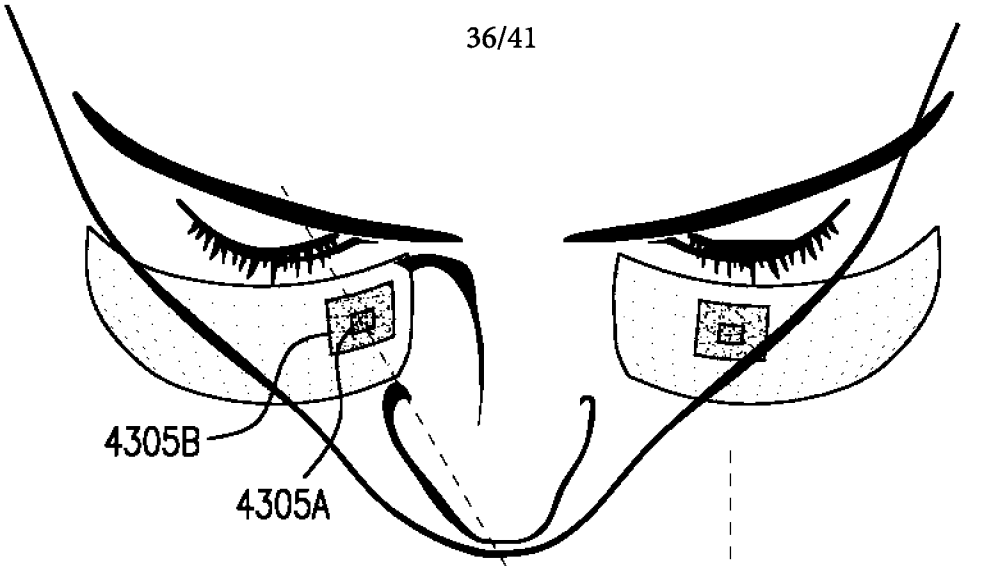

FIG. 45

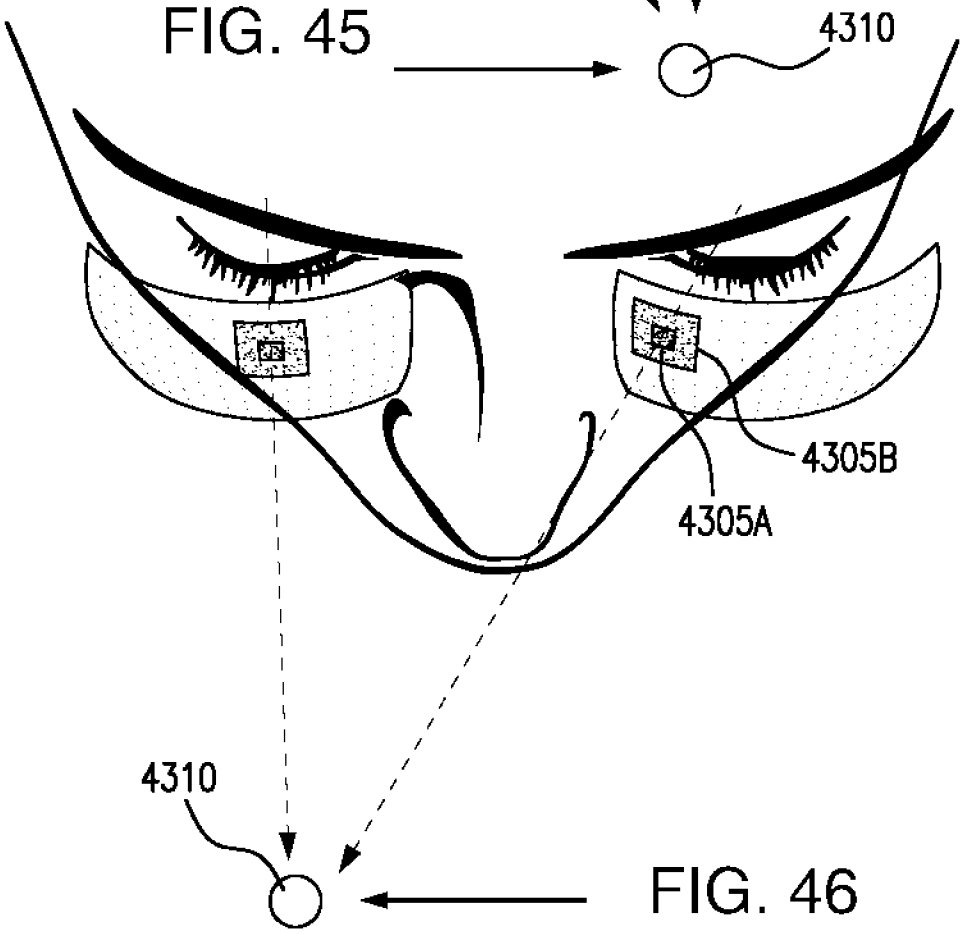

FIG. 46

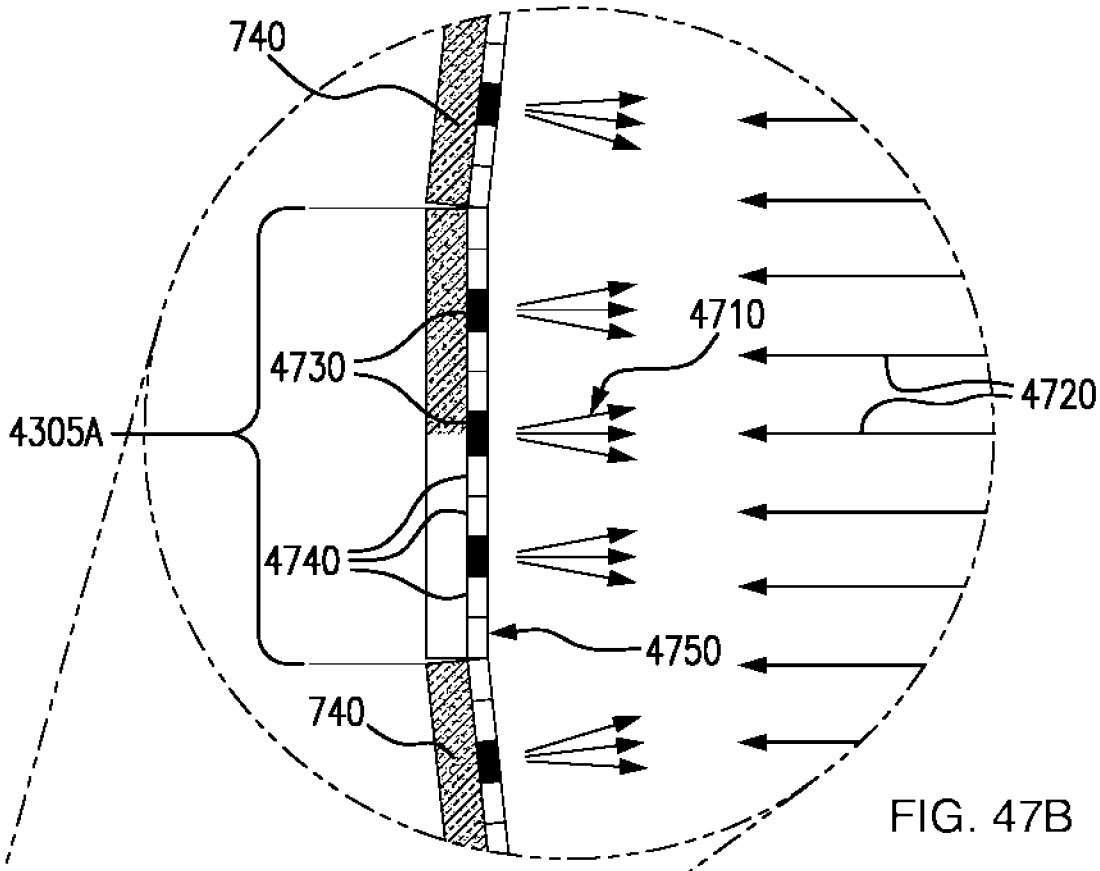

FIG. 47B

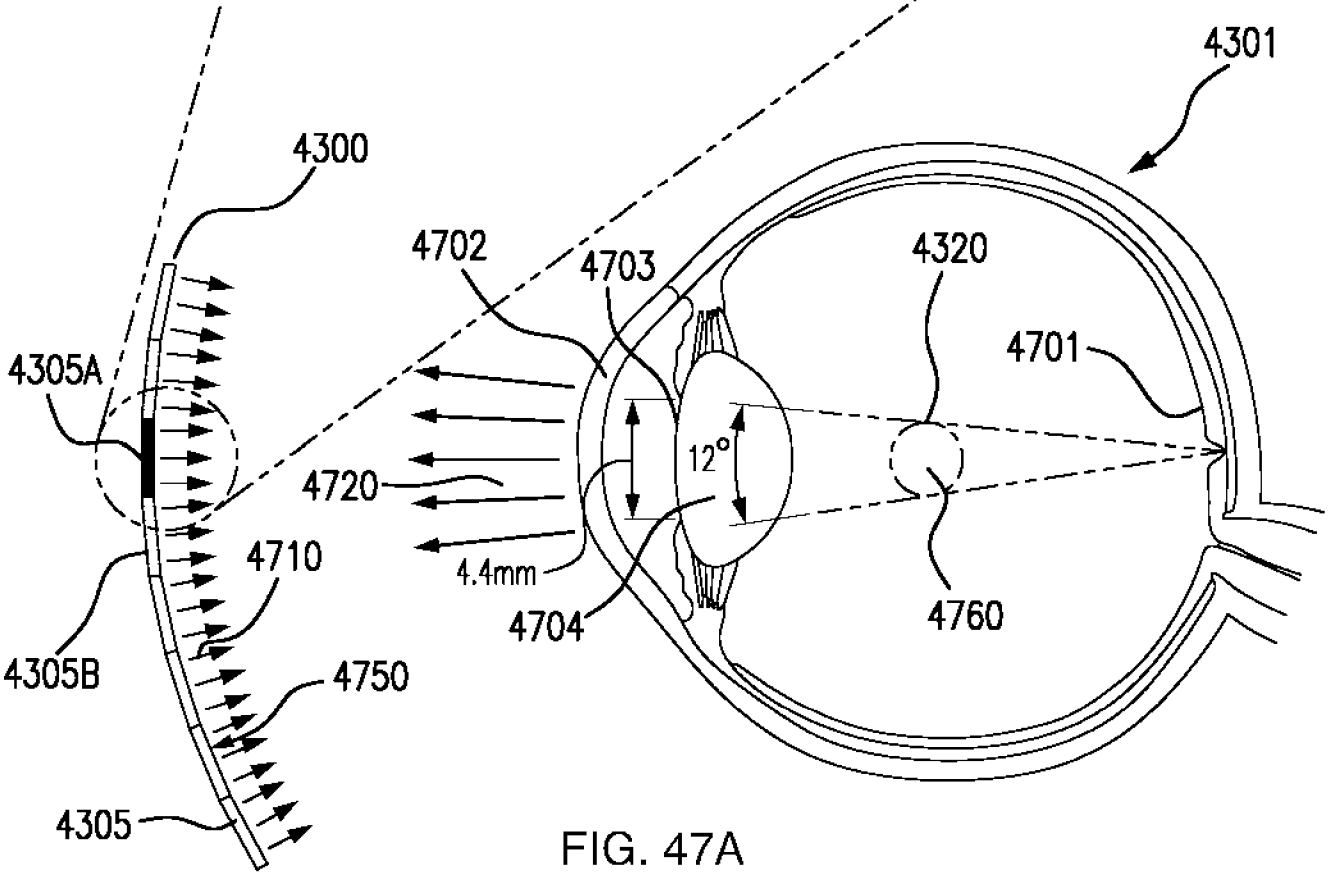

FIG. 47A

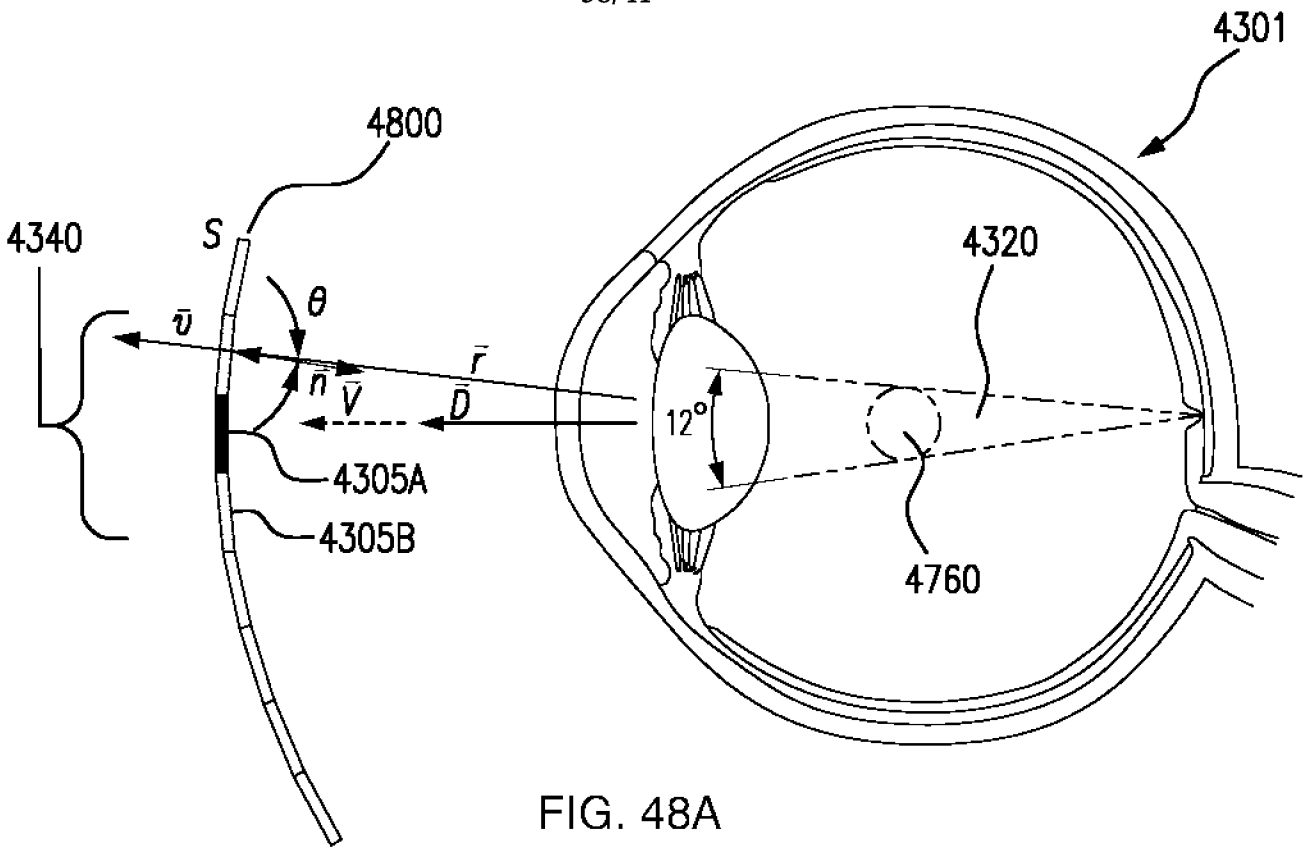

FIG. 48A

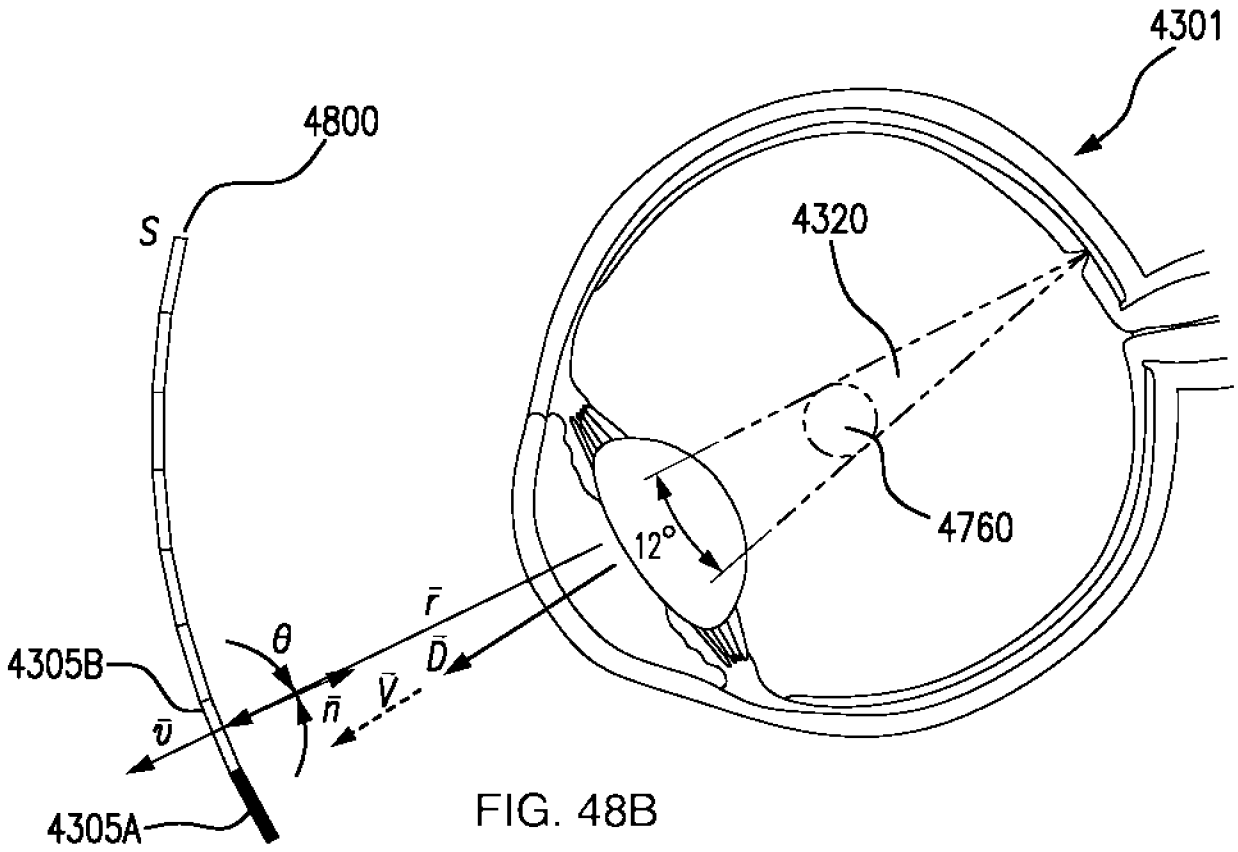

FIG. 48B

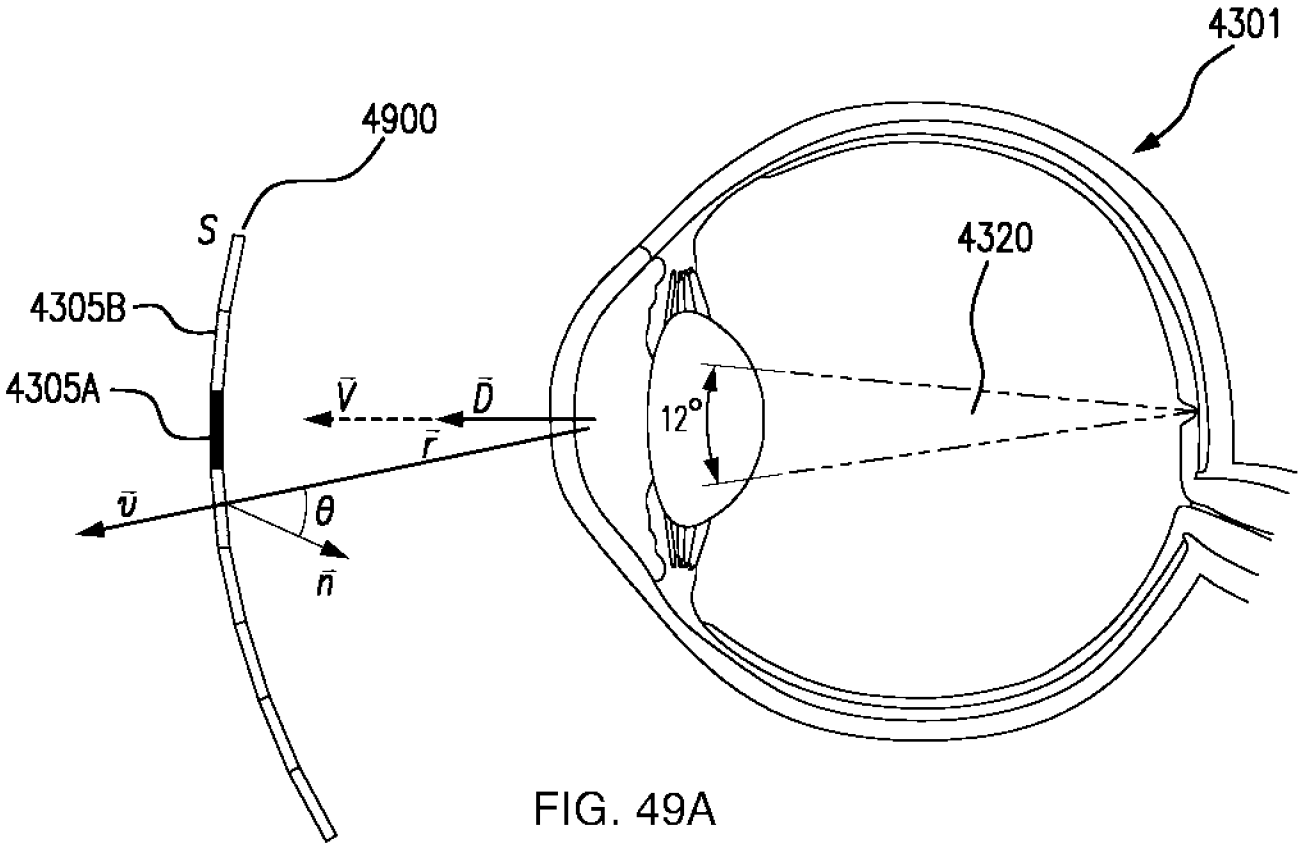

FIG. 49A

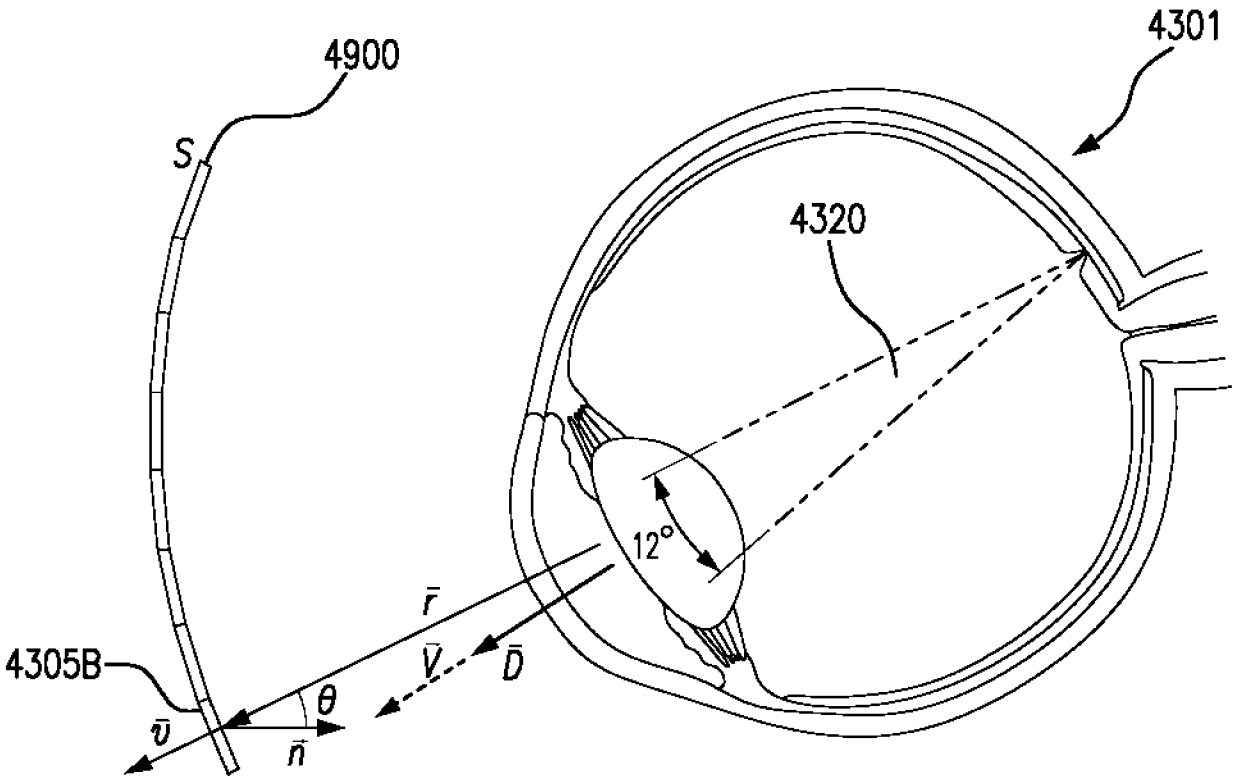

FIG. 49B

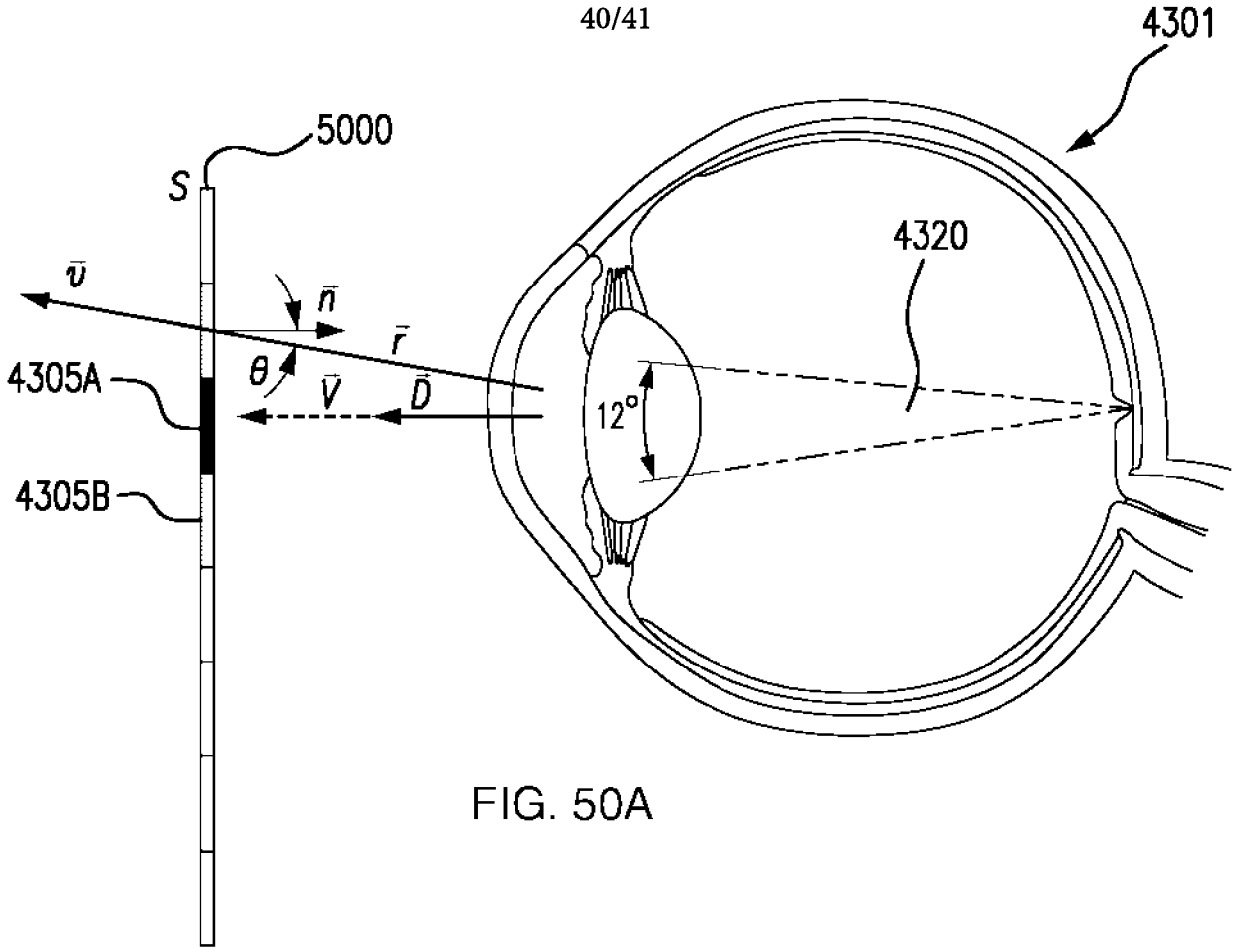

FIG. 50A

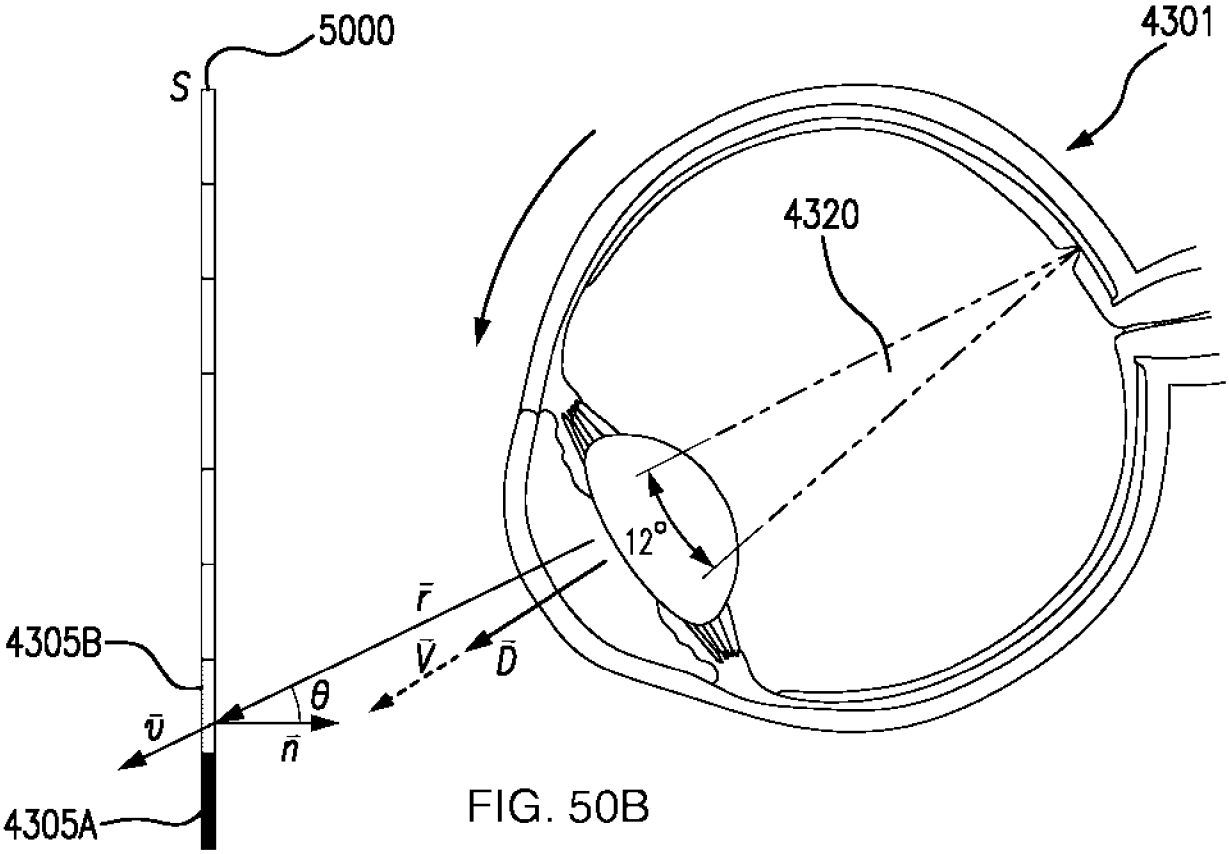

FIG. 50B

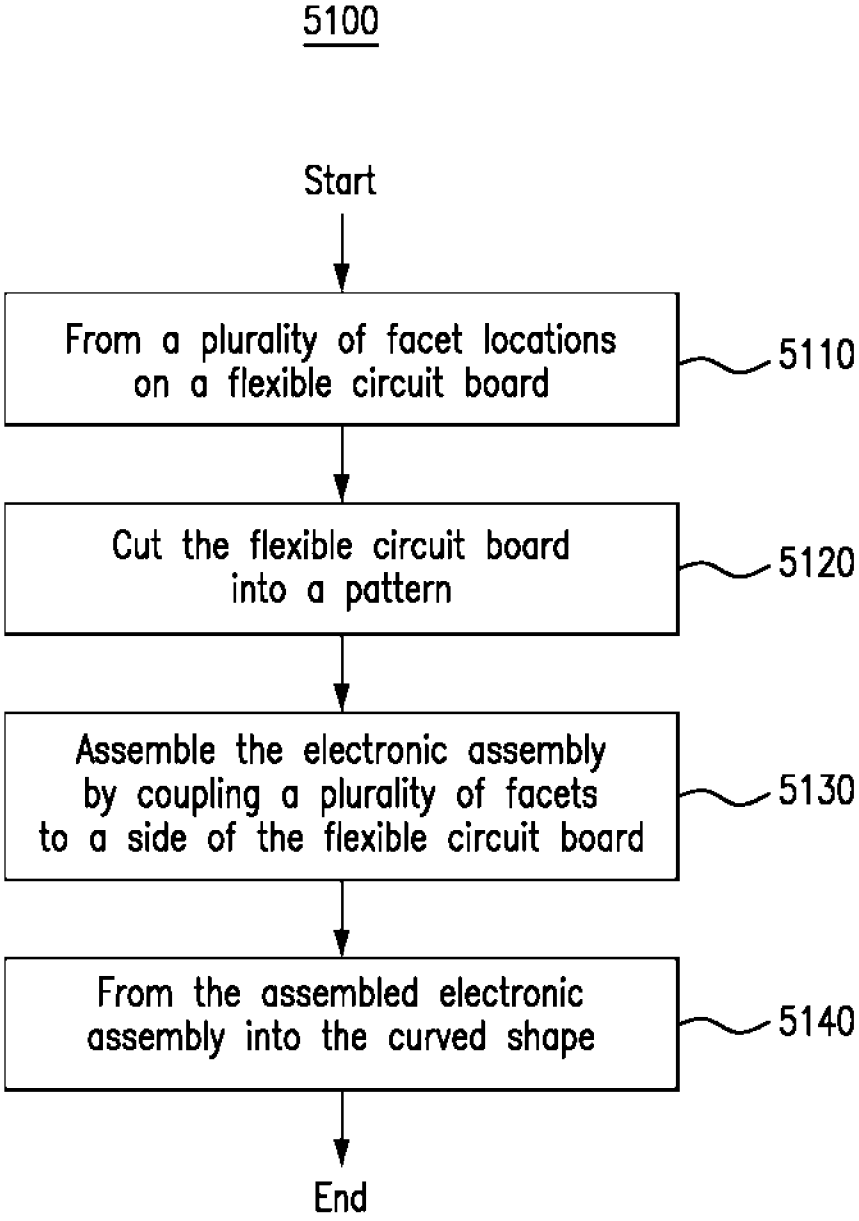
5100
Start
From a plurality of facet locations on a flexible circuit board
5110
Cut the flexible circuit board into a pattern
5120
Assemble the electronic assembly by coupling a plurality of facets to a side of the flexible circuit board
5130
From the assembled electronic assembly into the curved shape
5140
End

FIG. 51

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/061959

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F3/01 G09G3/00 G02B27/00 G02B27/01
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F G09G G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 10 129 984 B1 (LAMKIN MARK A [US] ET AL) 13 November 2018 (2018-11-13) column 8, line 46 - column 9, line 4; figure 7 column 9, lines 5-41; figure 8 column 12, lines 25-43; figures 17A, 17B column 20, line 15 - column 21, line 33; figures 22-25 column 22, line 24 - column 24, line 27; figures 26, 27 column 24, line 45 - column 25, line 23; figure 36 -----	1-20
Y	US 2017/038590 A1 (JEPSEN MARY LOU [US]) 9 February 2017 (2017-02-09) paragraphs [0082] - [0214]; figures 3-11 -----	1-20

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 February 2020	06/03/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Legrand, J

2

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/061959

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2017/108697 A1 (EL-GHOROURY HUSSEIN S [US] ET AL) 20 April 2017 (2017-04-20) paragraphs [0022] - [0058]; figures 1-4 -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2019/061959

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 2017038590 A1	09-02-2017	US 2017038589 A1	09-02-2017
		US 2017038590 A1	09-02-2017
		US 2017038591 A1	09-02-2017
		US 2017038836 A1	09-02-2017
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		KR 20180070626 A	26-06-2018
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		WO 2017066802 A1	20-04-2017