(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification:
G06F 12/00 (2006.01)

(21) International Application Number:
PCT/US2007/061191

(22) International Filing Date: 29 January 2007 (29.01.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/360,926   23 February 2006 (23.02.2006)   US

(71) Applicant (for all designated States except US):
FREESCALE SEMICONDUCTOR INC. [US/US];
6501 William Cannon Drive West, Austin, Texas 78735
(US).

(72) Inventor; and
(75) Inventor/Applicant (for US only): MOYER, William C.
[US/US]; 1111 Meadow Ridge Drive, Dripping Springs,
Texas 78620 (US).

(74) Agents: KING, Robert L. et al.; 7700 W. Parmer Lane,
MD:PL02, Austin, Texas 78729 (US).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS,
JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS,
LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY,
MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS,
RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,
RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA,
GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
—   with international search report
—   before the expiration of the time limit for amending the
     claims and to be republished in the event of receipt of
     amendments

(88) Date of publication of the international search report:
30 October 2008

(54) Title: DATA PROCESSING SYSTEM HAVING ADDRESS TRANSLATION BYPASS AND METHOD THEREFOR
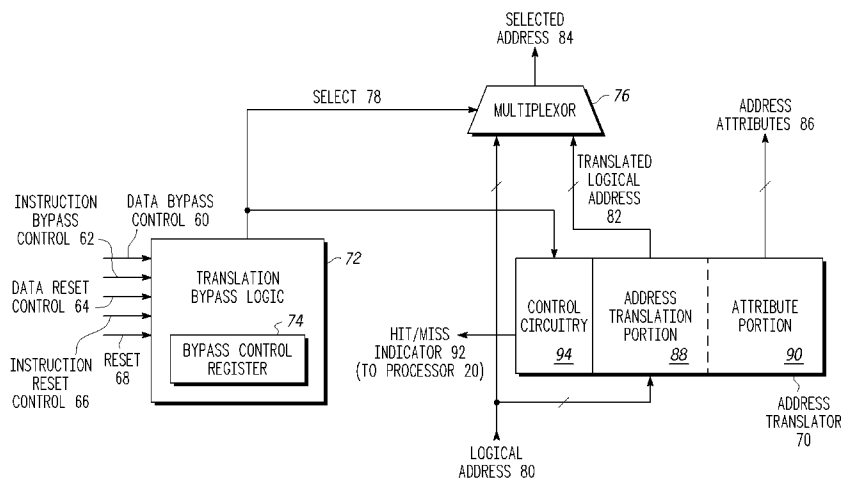

FIG. 2

(57) Abstract: In a data processing system a processor including processing logic performs data processing. An address translator
(70) that is coupled to the processing logic performs address translation and a method thereof. The address translator (70) receives a
logical address (80) and converts the logical address to both a physical address (82) and one or more address attributes (86). Bypass
circuitry (72) that is coupled to the address translator selectively provides the logical address as a translated address of the logical
address which was received. In order to speed up the memory address translation, the logical address is selectively provided as the
translated address prior to providing the one or more address attributes associated with the logical address.

INTERNATIONAL SEARCH REPORT	International application No.
	PCT/US07/61191

A.   CLASSIFICATION OF SUBJECT MATTER
IPC: **G06F 12/00(2006.01)**

USPC: 711/202,203,205,207,138;712/200
According to International Patent Classification (IPC) or to both national classification and IPC

B.   FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
     U.S. : 711/202, 203, 205, 207, 138; 712/200

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
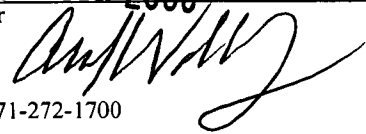Please See Continuation Sheet

C.   DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,732,405 A (HO et al.) 24 March 1998, see entire document.	1-20
A	US 5,666,509 A (MCCARTHY et al.) 09 September 1997, see entire document.	1-20
A	US 5,535,351 A (PENG) 09 July 1996, see entire document.	1-20

☐ Further documents are listed in the continuation of Box C.   ☐   See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier application or patent published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when he document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than he priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 August 2008 (18.08.2008)	**27 AUG 2008**

Name and mailing address of the ISA/US
     Mail Stop PCT, Attn: ISA/US
     Commissioner for Patents
     P.O. Box 1450
     Alexandria, Virginia 22313-1450
Facsimile No. (571) 273-3201
	Authorized officer
	TOM DUNN
	Telephone No. 571-272-1700

Form PCT/ISA/210 (second sheet) (April 2007)

Continuation of B. FIELDS SEARCHED Item 3:
 US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB: virtual, logical, address, page, tag, attribute, protection, access, right, translation, lookaside, buffer, cache, map, convert, multiplex, physical, before, prior, ahead, advance, provid, supply, generat, creat, mak, extract, retriev