



(51) International Patent Classification:

H01L 29/06 (2006.01) H01L 27/092 (2006.01)
H01L 29/15 (2006.01) H01L 21/8238 (2006.01)
H01L 27/088 (2006.01)

(21) International Application Number:

PCT/CN2022/120113

(22) International Filing Date:

21 September 2022 (21.09.2022)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

17/481,353 22 September 2021 (22.09.2021) US

(71) Applicant: INTERNATIONAL BUSINESS

MACHINES CORPORATION [US/US]; New Orchard Road, Armonk, New York 10504 (US).

(71) Applicant (for MG only): IBM (CHINA) CO., LIMIT-

ED [CN/CN]; 7F, Bldg 10, Zhangjiang Innovation Park, 399 Keyuan Road, Zhangjiang High-Tech Campus, Pudong New Area, Shanghai 201203 (CN).

(72) Inventors: CHENG, Kangguo; C/o IBM IPLaw Dept.,

1101 Kitchawan Rd., PO Box 218, Yorktown Heights, NY 10598-0218 (US). MOCHIZUKI, Shogo; 257 Fuller Road,

Albany, NY 12203-3654 (US). LI, Juntao; 257 Fuller Road, Albany, NY 12203-3654 (US).

(74) Agent: ZHONGZI LAW OFFICE; 7F, New Era Building, 26 Pinganli, Xidajie, Xicheng District, Beijing 100034 (CN).

(81) Designated States (unless otherwise indicated, for every

kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every

kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: FORMING STACKED NANOSHEET SEMICONDUCTOR DEVICES WITH OPTIMAL CRYSTALLINE ORIENTATIONS AROUND DEVICES

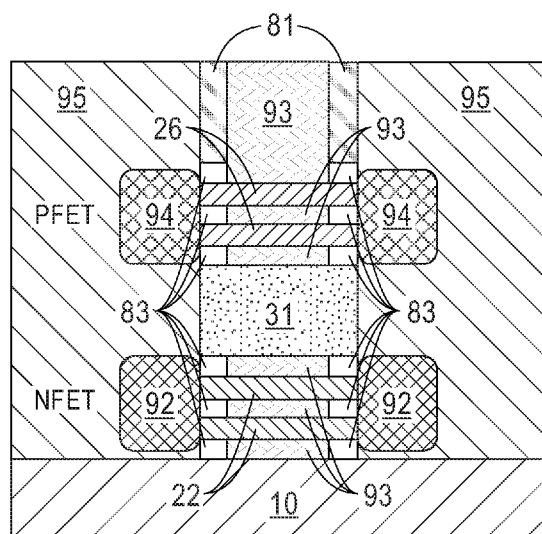


FIG. 10A

(57) Abstract: An approach provides a semiconductor structure with a first crystalline surface orientation and a first nanosheet stack on the semiconductor substrate with the first crystalline surface orientation. The semiconductor substrate structure includes a second nanosheet stack with a second crystalline surface orientation above the first nanosheet stack, wherein the first nanosheet stack and the second nanosheet stack are separated by a dielectric material (31).

Published:

— *with international search report (Art. 21(3))*

FORMING STACKED NANOSHEET SEMICONDUCTOR DEVICES WITH OPTIMAL CRYSTALLINE ORIENTATIONS AROUND DEVICES

BACKGROUND OF THE INVENTION

[0001] The present invention relates generally to the field of semiconductor device formation using two vertically stacked nanosheet stacks and more particularly to the formation of vertically stacked N-type and P-type complementary metal-oxide-semiconductor (CMOS) transistors with where each of the transistors has a device optimal crystal orientation.

[0002] In order to attain both increased circuit density and required electrical performance, semiconductor device fabrication is increasingly using a number of nanosheets stacks composed of very thin layers of semiconductor or other materials in device formation. In particular, the formation of CMOS devices using nanosheet stacks for advanced device structures with less than ten nanometer feature size is becoming more prevalent. Device fabrication utilizing nanosheet stacks is emerging for gate-all-around (GAA) transistors that can be formed as vertical gate-all-around (vGAA) or horizontal gate-all-around (hGAA) devices. Conventionally, adjacent p-type field-effect transistor (PFETs) structures and n-type field-effect transistor (NFET) structures are fabricated as a single type of GAA devices, such as two adjacent hGAA devices or two vGAA devices where the two adjacent devices are either a PFET hGAA device and an NFET hGAA device or a PFET vGAA device and an NFFET vGAA device. In particular, hGAA devices employing nanosheet stacks are becoming more prevalent as feature sizes in CMOS devices continue to scale downward.

SUMMARY

[0003] Embodiments of the present invention disclose a semiconductor substrate structure with a first crystalline surface orientation and a first nanosheet stack on the semiconductor substrate with the first crystalline surface orientation. The semiconductor substrate structure includes a second nanosheet stack with a second crystalline surface orientation above the first nanosheet stack, wherein the first nanosheet stack and the second nanosheet stack are separated by a dielectric material.

[0004] Embodiments of the present invention disclose a semiconductor device structure where the semiconductor device is composed of a p-type field-effect transistor and a n-type field-effect transistor that are vertically stacked in a complementary metal-oxide-semiconductor device (CMOS) device. The semiconductor device structure includes a semiconductor substrate, a p-type field-effect transistor with a first crystalline surface orientation in a channel material in a first nanosheet stack; and an n-type field-effect transistor with a second crystalline surface orientation in a channel material in a second nanosheet stack where the first crystalline surface orientation provides a preferred crystal orientation of the p-type channel material and the second crystalline surface orientation provides the preferred crystal orientation of the n-type channel material. The p-type field-effect transistor and the n-type field-effect transistor are vertically aligned and isolated by a dielectric material. Embodiments of the present invention provide the semiconductor device that is a stacked CMOS with a gate-all-around semiconductor device structure.

[0005] Embodiments of the present invention provide a method of forming a semiconductor substrate structure with two nanosheet stacks where each of the two nanosheet stacks has a different crystalline surface orientation. The method includes epitaxially growing a first nanosheet stack of alternating nanosheet layers of a sacrificial semiconductor material and a channel semiconductor material on a first semiconductor substrate with a first crystalline surface orientation. The method includes epitaxially growing a second nanosheet stack alternating nanosheet layers of the sacrificial semiconductor material and the channel semiconductor material on a second semiconductor substrate with a second crystalline surface orientation. The method includes depositing a dielectric layer on a top layer of the sacrificial semiconductor

material in one of the first nanosheet stack or the second nanosheet stack and bonding a top surface of the first nanosheet stack to a top surface of the second nanosheet stack. The method includes removing one of the first semiconductor substrate or the second semiconductor substrate from under one of the first nanosheet stack or the second nanosheet stack that are bonded together.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The above and other aspects, features, and advantages of various embodiments of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings.

[0007] FIG. 1A depicts a top view of a first semiconductor substrate, in accordance with an embodiment of the present invention.

[0008] FIG. 1B depicts a top view of a second semiconductor substrate, in accordance with an embodiment of the present invention.

[0009] FIG. 2A depicts a cross-sectional view of a semiconductor structure after forming a first nanosheet stack on the first semiconductor substrate, in accordance with an embodiment of the present invention.

[0010] FIG. 2B depicts a cross-sectional view of a semiconductor structure after forming a second nanosheet stack on the second semiconductor substrate, in accordance with an embodiment of the present invention.

[0011] FIG. 3 depicts a cross-sectional view of the semiconductor structure after forming an oxide layer on the second nanosheet stack on the second semiconductor substrate, in accordance with an embodiment of the present invention.

[0012] FIG. 4 depicts a cross-sectional view of the semiconductor structure after joining the second nanosheet stack to the first nanosheet stack, in accordance with an embodiment of the present invention.

[0013] FIG. 5 depicts a top view of the semiconductor structure after depositing a hardmask material on an exposed top surface of the second nanosheet stack, in accordance with an embodiment of the present invention.

[0014] FIG. 6A depicts a cross-sectional view in the X-X direction depicted in FIG. 5 of the semiconductor structure after removing portions of the hardmask, the second nanosheet

stack, the oxide layer, and the first nanosheet stack, in accordance with an embodiment of the present invention.

[0015] FIG. 6B depicts a cross-sectional view in the Y-Y direction depicted in FIG. 5 of the semiconductor structure after removing portions of the hardmask, the second nanosheet stack, the oxide layer, and the first nanosheet stack, in accordance with an embodiment of the present invention.

[0016] FIG. 7A depicts a cross-sectional view in the X-X direction depicted in FIG. 5 after forming a dummy gate structure, in accordance with an embodiment of the present invention.

[0017] FIG. 7B depicts a cross-sectional view in the Y-Y direction depicted in FIG. 5 after forming a dummy gate structure, in accordance with an embodiment of the present invention.

[0018] FIG. 8A depicts a cross-sectional view in the X-X direction depicted in FIG. 5 after forming spacers, in accordance with an embodiment of the present invention.

[0019] FIG. 8B depicts a cross-sectional view in the Y-Y direction depicted in FIG. 5 after forming spacers, in accordance with an embodiment of the present invention.

[0020] FIG. 9A depicts a cross-sectional view in the X-X direction of the semiconductor structure after forming source/drains for an n-type field-effect device and a p-type field-effect device and a replacement gate structure, in accordance with an embodiment of the present invention.

[0021] FIG. 9B depicts a cross-sectional view in the Y-Y direction of the semiconductor structure after forming source/drains for the n-type field-effect device and the p-type field-effect device and a replacement gate structure, in accordance with an embodiment of the present invention.

[0022] FIG. 10A depicts a cross-sectional view in the X-X direction of the semiconductor structure after forming a replacement gate structure, in accordance with an embodiment of the present invention.

[0023] FIG. 10B depicts a cross-sectional view in the Y-Y direction of the semiconductor structure after forming a replacement gate structure, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0024] Embodiments of the present invention recognize that stacked complementary metal-oxide-semiconductor (CMOS) devices are emerging as a method to increase transistor density. Embodiments of the present invention recognize that stacked CMOS devices are conventionally formed by stacking n-type field-effect transistors (NFET) and p-type field-effect transistors (PFET) on top of each other in the CMOS device. Embodiments of the present invention recognize that the performance of CMOS devices is strongly dependent on the crystalline orientation of the device channel. NFET and PFET have different preferred crystalline orientations that provide optimal electrical performance. In NFETs, a {100} crystalline surface orientation for the channel material is preferred for optimal electrical performance. In PFETs, a {110} crystalline surface orientation for the channel material is preferred for optimal electrical performance. Embodiments of the present invention recognize that typical CMOS devices are formed using conventional nanosheet stacks where the NFET and PFETs are both formed with semiconductor nanosheet layers with the same crystalline surface orientation. As known to one skilled in the art, the {100} and the {110} crystalline surface orientation use Miller indices to identify a set of lattice planes in crystallography or material science and that in particular, the family of lattice planes is determined by three integers h , k , and ℓ that are known as the Miller indices.

[0025] In conventional stacked CMOS devices, such as hGAA, the NFET and the PFET devices are typically formed using a single nanosheet stack. In the nanosheet stack, the crystalline surface orientation of the channel material is typically a {100} crystalline surface orientation. Embodiments of the present invention recognize that forming stacked CMOS devices with NFET and PFET hGAA devices with a single nanosheet stack that has a {100} crystalline surface orientation for channel material results in reduced electrical performance of the PFET hGAA device. Embodiments of the present invention recognize that a method of forming stacked CMOS devices that include a PFET hGAA device with a {110} crystalline surface orientation for the PFET device channel and an NFET hGAA device formed with a {100} crystalline surface orientation in the NFET device channel is desirable to improve the performance of stacked CMOS devices.

[0026] Embodiments of the present invention provide a method of forming a semiconductor substrate that provides two vertically stacked nanosheet stacks where the first nanosheet stack has one crystalline surface orientation and a second nanosheet stack has a second crystalline surface orientation. Embodiments of the present invention provide the semiconductor substrate structure with two nanosheet stacks where each of the nanosheet stacks is composed of alternating nanosheet layers of a sacrificial material, such as a silicon-germanium layer and a channel material layer, such as a layer of silicon. While the crystal orientation of each layer in each nanosheet stack is the same, embodiments of the present invention provide a semiconductor substrate structure with two nanosheet stacks where the crystal orientation of the two nanosheet stacks is different.

[0027] Embodiments of the present invention provide the first nanosheet stack with a crystalline surface orientation providing an optimal electrical performance for one type of transistor in a stacked CMOS device. The second nanosheet stack has the crystalline surface orientation providing an optimal electrical performance for a second type of transistor in the stacked CMOS device. More specifically, embodiments of the present invention provide a semiconductor substrate structure where each layer of one nanosheet stack has a {110} crystalline surface orientation that is preferred for PFET hGAA device performance and where each layer of the other nanosheet stack has a {100} crystalline orientation that is preferred for NFET hGAA device performance. The two nanosheet stacks are separated by a dielectric material layer in embodiments of the present invention. The two nanosheet stacks are above a base semiconductor substrate or wafer with a first crystalline surface orientation where the first nanosheet stack on the wafer also has the first crystalline surface orientation.

[0028] Embodiments of the present invention provide the semiconductor substrate structure where the first nanosheet stack has a {100} crystalline surface orientation in the channel material. Embodiments of the present invention also provide the second nanosheet stack with a {110} crystalline surface orientation when the first nanosheet stack has a {100} crystalline surface orientation in the channel material. In this way, embodiments of the present invention provide a semiconductor structure with two different crystalline orientations for the nanosheet stacks, and therefore, the semiconductor substrate can provide preferred crystalline

orientations for both PFETs and NFETs in stacked CMOS devices formed from the semiconductor substrate.

[0029] Embodiments of the present invention provide a method of forming the semiconductor substrate structure with two nanosheet stacks where each nanosheet stack has a different crystal orientation. Each of the nanosheet stacks is epitaxially grown on a base semiconductor substrate or wafer and will have the same crystal orientation as the base semiconductor substrate the nanosheet stack is grown on. The method includes using two different base semiconductor substrates or wafers with two different crystal orientations to grow the two nanosheet stacks where one nanosheet stack is grown on one base semiconductor substrate and the second nanosheet stack is grown on the second base semiconductor substrate.

[0030] Embodiments of the present invention provide a method of using epitaxy to grow one nanosheet stack with a crystalline surface orientation that matches the crystalline surface orientation of the base semiconductor substrate or wafer on which the nanosheet stack is formed and growing a second nanosheet stack on a second base semiconductor substrate with a different crystalline surface orientation. Embodiments of the present invention provide the method where when the base semiconductor substrate has a {100} crystalline surface orientation, then the nanosheet stack grown on the semiconductor substrate has a {100} crystalline surface orientation. A {100} crystalline surface orientation is preferred for NFET electrical performance. When the second semiconductor substrate or wafer has a {110} crystalline surface orientation, then the second nanosheet stack grown on the second semiconductor substrate or wafer has a {110} crystalline orientation. A {110} crystalline surface orientation of the second nanosheet stack is preferred for PFET electrical performance. Embodiments of the present invention also provide the method where when the base semiconductor substrate has a {110} crystalline surface orientation, then the nanosheet stack grown on the semiconductor substrate has a {110} crystalline surface orientation.

[0031] After growing the nanosheet stacks, the method includes depositing a dielectric material, such as an oxide layer by chemical vapor deposition, physical vapor deposition, atomic layer deposition, or another known semiconductor manufacturing deposition method on the top surface of one or both of the two nanosheet stacks formed on the two semiconductor substrates.

After depositing the oxide layer, the two semiconductor substrates or wafers are bonded together (e.g., the top surface of one of the nanosheet stacks is joined to dielectric material on the other nanosheet stack). The wafer bonding joins the top surface of the dielectric material on one nanosheet stack to the top surface of the second nanosheet stack. One of the two semiconductor substrates is removed from the semiconductor stack of the two joined nanosheet stacks. After removing one of the two semiconductor substrates or wafers, the two nanosheet stacks reside on the remaining semiconductor substrate. Embodiments of the present invention provide a single semiconductor substrate structure where two nanosheet stacks with different crystalline surface orientations are vertically stacked on a wafer or substrate and are electrically isolated from each other by a dielectric material.

[0032] Embodiments of the present invention provide the semiconductor substrate with one of a {110} or a {100} crystalline surface orientation and a first nanosheet stack is on the semiconductor substrate with the same crystalline surface orientation as the semiconductor substrate. The first nanosheet stack is under a dielectric material, such as an oxide layer. When the first nanosheet stack has a {110} crystalline surface orientation then, the second nanosheet stack that is on the dielectric material has a {100} crystalline surface orientation in the channel material. In other embodiments, the second nanosheet stack has a {110} crystalline surface orientation when the first nanosheet stack has a {100} crystalline surface orientation in the channel material.

[0033] Using the semiconductor substrate with two stacked and electrically isolated nanosheet stacks where one of the two nanosheet stacks has a {110} crystalline surface orientation and the other nanosheet stack has a {100} crystalline surface orientation, embodiments of the present invention provide a semiconductor device structure and a method of forming a stacked CMOS device with a vertically aligned PFET and NFET that each has a preferred crystalline surface orientation in the channel material. Using the method of forming the semiconductor substrate described in detail above provides the stacked CMOS device with a PFET with a channel material that has a preferred {110} crystalline surface orientation and the NFET with a channel material that has a preferred {100} crystalline surface orientation. In this way, the stacked CMOS device formed from the semiconductor substrate structure with two nanosheet stacks with two different crystal orientations provides improved electrical

performance for the stacked CMOS device. Embodiments of the present invention use semiconductor device formation processes and the semiconductor substrate with two vertically stacked nanosheet stacks with two different crystal orientations to form the stacked CMOS device. Embodiments of the present invention provide a method of forming a semiconductor device structure and a semiconductor device structure for a stacked CMOS device using a horizontal gate-all-around (hGAA) device structure although the methods described hereinafter are not limited to hGAA devices but, may be applied to other types of CMOS devices as well. The PFET hGAA device has a channel material with a {110} crystalline surface orientation and the NFET hGAA device in the stacked CMOS has a channel material with a {100} crystalline orientation.

[0034] The following description with reference to the accompanying drawings is provided to assist in a comprehensive understanding of exemplary embodiments of the invention as defined by the claims and their equivalents. The descriptions of the various embodiments of the present invention have been presented for purposes of illustration but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope of the described embodiments. The terminology used herein was chosen to best explain the principles of the one or more embodiment, the practical application or technical improvement over technologies found in the industry, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein. Accordingly, those of ordinary skill in the art will recognize that various changes and modifications of the embodiments described herein can be made without departing from the scope of the invention. Some of the process steps, depicted, can be combined as an integrated process step. In addition, descriptions of well-known functions and constructions may be omitted for clarity and conciseness.

[0035] The terms and words used in the following description and claims are not limited to the bibliographical meanings but are merely used to enable a clear and consistent understanding of the invention. Accordingly, it should be apparent to those skilled in the art that the following description of exemplary embodiments of the present invention is provided for illustration only and not for the purpose of limiting the invention as defined by the appended claims and their equivalents.

[0036] It is to be understood that the singular forms “a,” “an,” and “the” include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to “a component surface” includes reference to one or more of such surfaces unless the context clearly dictates otherwise.

[0037] For purposes of the description hereinafter, terms such as “upper”, “lower”, “right”, “left”, “vertical”, “horizontal”, “top”, “bottom”, and derivatives thereof shall relate to the disclosed structures and methods, as oriented in the drawing figures. Terms such as “above”, “overlying”, “atop”, “on top”, “positioned on” or “positioned atop” mean that a first element, such as a first structure, is present on a second element, such as a second structure, wherein intervening elements, such as an interface structure may be present between the first element and the second element. The term “direct contact” means that a first element, such as a first structure, and a second element, such as a second structure, are connected without any intermediary conducting, insulating, or semiconductor layers at the interface of the two elements.

[0038] In the interest of not obscuring the presentation of embodiments of the present invention, in the following detailed description, some processing steps or operations that are known in the art may have been combined for presentation and illustration purposes and in some instances may have not been described in detail. In other instances, some processing steps or operations that are known in the art may not be described at all. It should be understood that the following description is rather focused on the distinctive features or elements of various embodiments of the present invention.

[0039] Detailed embodiments of the claimed structures and methods are disclosed herein. The method steps described below do not form a complete process flow for manufacturing integrated circuits on semiconductor chips. The present embodiments can be practiced in conjunction with the integrated circuit fabrication techniques for semiconductor chips and devices currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the described embodiments. The figures represent cross-section portions of a semiconductor chip or a substrate, such as a semiconductor wafer during fabrication, and are not drawn to scale, but instead are drawn to illustrate the features of the described embodiments. Specific structural and functional details disclosed

herein are not to be interpreted as limiting, but merely as a representative basis for teaching one skilled in the art to variously employ the methods and structures of the present disclosure. In the description, details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the presented embodiments.

[0040] References in the specification to “one embodiment”, “other embodiment”, “another embodiment”, “an embodiment,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is understood that it is within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described. It will be understood that, although the terms first, second, etc. can be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, the first element discussed below could be termed a second element without departing from the scope of the present concept.

[0041] Selectively etching as used herein includes but is not limited to patterning using one of lithography, photolithography, an extreme ultraviolet (EUV) lithography process, or any other known semiconductor patterning process followed by one or more the etching processes. Various materials are referred to herein as being removed or “etched” where etching generally refers to one or more processes implementing the removal of one or more materials while leaving other protected areas of the materials that are masked during the lithography processes unaffected. Some examples of etching processes include but are not limited to the following processes, such as a dry etching process using a reactive ion etch (RIE) or ion beam etch (IBE), a wet chemical etch process, or a combination of these etching processes. A dry etch may be performed using a plasma. Ion milling, sputter etching, or reactive ion etching (RIE) bombards the wafer with energetic ions of noble gases that approach the wafer approximately from one direction, and therefore, these processes are an anisotropic or a directional etching process.

[0042] The terms “epitaxially growing and/or depositing” and “epitaxially grown and/or deposited” mean the growth of a semiconductor material on a deposition surface of a semiconductor material, in which the semiconductor material being grown has the same crystalline characteristics as the semiconductor material of the deposition surface. In epitaxy or an epitaxial deposition process, the chemical reactants provided by the source gases are controlled and the system parameters are set so that the depositing atoms arrive at the deposition surface of the semiconductor substrate with sufficient energy to move around on the surface and orient themselves to the crystal arrangement of the atoms of the deposition surface. Therefore, an epitaxial semiconductor material has the same crystalline characteristics as the deposition surface on which it is formed.

[0043] Reference is now made to the figures. The figures provide a schematic cross-sectional illustration of semiconductor devices at intermediate stages of fabrication, according to one or more embodiments of the invention. The device provides schematic representations of the devices of the invention and are not to be considered accurate or limiting with regards to device element scale.

[0044] FIG. 1A depicts a top view of semiconductor substrate 10, in accordance with an embodiment of the present invention. In various embodiments, semiconductor substrate 10 has {100} crystalline surface orientation. As previously discussed, the crystalline surface orientation can be identified using standard crystallographic planes that are any set of parallel and equally spaced planes that may pass through the centers of atoms in crystals and can be identified using Miller Indices with the notation $\{hkl\}$ to denote the set of all planes that are equivalent to (hkl) by the symmetry of the crystal lattice. As known to one skilled in the art, a {100} crystalline surface orientation includes the $(1\ 0\ 0)$, $(0\ 1\ 0)$, $(0\ 0\ 1)$, $(-1\ 0\ 0)$, $(0\ -1\ 0)$, and $(0\ 0\ -1)$ family of crystal planes.

[0045] A {100} crystalline surface orientation provides a preferred crystal orientation for an NFET electrical performance. Also, depicted in FIG. 1A is a location of the X-X section through semiconductor substrate 10 that will be used for the cross-sectional views illustrated in FIG. 2A and FIG. 4.

[0046] Semiconductor substrate 10 is composed of any semiconductor substrate material suitable for a substrate in a CMOS device, such as a but not limited to a horizontal gate-all-around (hGAA) device. In various embodiments, semiconductor substrate 10 is a silicon semiconductor material. In other embodiments, semiconductor substrate 10 is composed of a group IV semiconductor material (e.g., Ge), a group III-V semiconductor material (e.g., gallium arsenide), a group II-VI semiconductor material, or other known semiconductor material or compounds of any known semiconductor material used in semiconductor circuits where the groups are columns or groups of elements in the Periodic Table of Elements. In various embodiments, substrate 10 is a wafer or a portion of a wafer. In some embodiments, semiconductor substrate 10 is composed of a semiconductor material includes one or more of doped, undoped, or contains doped regions, undoped regions, stressed regions, or defect-rich regions. In some examples, semiconductor substrate 10 may include one or more other devices or transistors (not depicted). In an embodiment, semiconductor substrate 10 is one of a layered semiconductor substrate, such as a semiconductor-on-insulator substrate (SOI), germanium on insulator (GeOI), or silicon-on-replacement insulator (SRI).

[0047] FIG. 1B depicts a top view of semiconductor substrate 11, in accordance with an embodiment of the present invention. In various embodiments, semiconductor substrate 11 has {110} crystalline surface orientation. A {110} crystalline surface orientation provides a preferred crystal orientation for a PFET electrical performance. As known to one skilled in the art, a {110} crystalline surface orientation includes the (1 1 0), (1 -1 0), (1 0 1), (1 0 -1), (0 1 1), (0 1 -1) family of crystal planes. In an embodiment, semiconductor substrate 11 has a {111} crystalline surface orientation. Also, depicted in FIG. 1B is a location of a Y-Y section through semiconductor substrate 11 that will be used to depict the cross-sectional views illustrated in FIG. 2B, FIG. 3, and FIG. 4.

[0048] Semiconductor substrate 11 is composed of any semiconductor substrate material suitable for a substrate in a Complementary Metal-Oxide Semiconductor (CMOS) device, such as a but not limited to a hGAA device with a PFET device structure. In various embodiments, semiconductor substrate 11 is a silicon semiconductor material. In other embodiments, semiconductor substrate 11 is composed of a group IV semiconductor material (e.g., Ge), a group III-V semiconductor material, a group II-VI semiconductor material, or other known

semiconductor material or compounds of any known semiconductor material used in semiconductor circuits where the groups are columns or groups of elements in the Periodic Table of Elements. In various embodiments, semiconductor substrate 11 is a wafer or a portion of a wafer. In some embodiments, semiconductor substrate 11 includes one or more of doped, undoped, or contains doped regions, undoped regions, stressed regions, or defect-rich regions. In some examples, semiconductor substrate 11 may include one or more other devices or transistors (not depicted). In an embodiment, substrate 11 is one of a layered semiconductor substrate, such as a semiconductor-on-insulator substrate (SOI), germanium on insulator (GeOI), or silicon-on-replacement insulator (SRI).

[0049] FIG. 2A depicts a cross-sectional view of a semiconductor structure after forming a first nanosheet stack composed of alternating nanosheet layers of sacrificial material 21 and channel material 22 on semiconductor substrate 10, in accordance with an embodiment of the present invention. In various embodiments, the first nanosheet stack on semiconductor substrate 10 depicted in FIG. 2A is comprised of alternating nanosheet layers of sacrificial material 21 and channel material 22 where channel material 12 resides between two nanosheet layers of sacrificial material 21. The nanosheet stack can be formed by epitaxially growing each layer of the nanosheet stack. As depicted, the first layer of sacrificial material 21 can be epitaxially grown on semiconductor substrate 10. Since semiconductor substrate 10 has a {100} crystalline surface orientation, sacrificial material 21 which can be a semiconductor material, such as SiGe grown on semiconductor substrate 10 will have a {100} crystalline surface orientation. A first nanosheet layer of channel material 22 can be grown on the first layer of sacrificial material 21 and will also have a {100} crystalline surface orientation. Subsequent layers of sacrificial material 21 are grown by epitaxy on layers of channel material 22, which in turn, are each grown on a layer of sacrificial material 21. Each of the nanosheet layers of the nanosheet stack grown by epitaxy above semiconductor substrate 10 will have a {100} crystalline surface orientation. As known to one skilled in the art, a semiconductor material grown by epitaxy can produce the same crystalline surface orientation and characteristics as the semiconductor surface or semiconductor substrate on which it is formed. In various embodiments, a layer of sacrificial material 21 is both the bottom and the top nanosheet layer of the nanosheet stack on semiconductor substrate 10.

[0050] Sacrificial material 21 is a layer of a sacrificial material. Sacrificial material 21 may be composed of a semiconductor material. In various embodiments, sacrificial material 21 is composed of SiGe. The composition of SiGe may vary depending on the semiconductor chip application. For example, sacrificial material 21 can be comprised of Si_xGe_y where x and y represent a relative atomic concentration of silicon (Si) and germanium (Ge), respectively. In some embodiments, x and y are less than 1 and their sum is equal to 1. In an embodiment, sacrificial material 21 is composed of another material capable of uniform deposition in a nanosheet layer that is compatible with semiconductor manufacturing processes and is suitable for a selective etch of sacrificial material 21 that is between channel layers 22 in later semiconductor device formation steps.

[0051] A thickness of sacrificial material 21 can be dictated by subsequent process steps and electrical requirements of the completed stacked CMOS device depicted in FIG. 8. For example, the thickness of sacrificial material 21 is between 5 and 20 nanometers but is not limited to these thicknesses.

[0052] Channel material 22 can be composed of any semiconductor material suitable for forming a channel in a CMOS device, such as an NFET hGAA device. In various embodiments, channel material 22 is composed of silicon but is not limited to silicon in other embodiments. As depicted, each nanosheet layer of channel material 22 is surrounded above and below by a nanosheet layer of sacrificial material 21. In one embodiment, two different and alternating semiconductor materials can be used for channel material 22 (i.e., channel material 22A and channel material 22B not depicted). For example, the thickness of channel material 22 is between 3 and 10 nanometers but, is not limited to this range of thickness.

[0053] FIG. 2B depicts a cross-sectional view of the semiconductor structure after forming a second nanosheet stack on semiconductor substrate 11, in accordance with an embodiment of the present invention. In various embodiments, the second nanosheet stack on semiconductor substrate 11 is composed of alternating nanosheet layers of sacrificial layer 25 and channel material 26 where channel material 26 resides between two nanosheet layers of sacrificial layer 25. The nanosheet stack can be formed by epitaxially growing each nanosheet layer of the nanosheet stack where the first nanosheet layer of sacrificial layers 25 is grown on

semiconductor substrate 11. Since semiconductor substrate 11 has a {110} crystalline surface orientation, sacrificial layer 25 which can be a semiconductor material, such as SiGe epitaxially grown on semiconductor substrate 11 can have a {110} crystalline surface orientation.

[0054] A first nanosheet layer of channel material 26 can be grown on the first layer of sacrificial layer 25 and channel material 26 grown on sacrificial layer 25 with a {110} crystalline surface orientation will also have a {110} crystalline surface orientation. Subsequent layers of sacrificial layer 25 are grown by epitaxy on layers of channel material 26, which in turn, are each grown on a layer of sacrificial material 26. Each of the nanosheet layers formed by epitaxy above semiconductor substrate 11 can have a {110} crystalline surface orientation. In various embodiments, a layer of sacrificial layer 25 is both the bottom and the top nanosheet layer of the nanosheet stack on substrate 11.

[0055] Sacrificial layer 25 is a layer of a sacrificial material. Sacrificial layer 25 may be composed of a semiconductor material. In various embodiments, sacrificial layer 25 is composed of SiGe. The composition of SiGe may vary depending on the semiconductor chip application. For example, sacrificial layer 25 can be comprised of Si_xGe_y where x and y represent a relative atomic concentration of silicon (Si) and germanium (Ge), respectively. In some embodiments, x and y are less than 1 and their sum is equal to 1. In an embodiment, sacrificial layer 25 is composed of another material capable of uniform deposition in a nanosheet layer that is compatible with semiconductor manufacturing processes and is suitable for a selective etch of sacrificial layers 25 that are between channel layers 26 in later semiconductor device formation steps. In various embodiments, the material composing sacrificial layer 25 can be the same material as sacrificial material 21 or a different material. In various embodiments, sacrificial layer 25 will have a different crystal orientation than sacrificial material 21.

[0056] A thickness of sacrificial layer 25 can be dictated by subsequent process steps and electrical requirements of the completed PFET CMOS device. The thickness of sacrificial layer 25 is between 5 and 20 nanometers but is not limited to these thicknesses.

[0057] Channel material 26 can be composed of any semiconductor material suitable for forming a channel in a CMOS device, such as a PFET hGAA device. In various embodiments, channel material 26 is composed of silicon but is not limited to silicon in other embodiments.

Each nanosheet layer of channel material 26 is surrounded above and below by a nanosheet layer of sacrificial layer 25. As depicted in FIG. 2B, each layer of channel material 26 alternates with layers of sacrificial layer 25. In one embodiment, two different and alternating semiconductor materials can be used for channel material 26 (i.e., channel material 26A and channel material 26B not depicted). The thickness of channel material 26 is between 3 and 10 nanometers but, is not limited to this range of thickness.

[0058] FIG. 3 depicts a cross-sectional view of the semiconductor structure after forming a dielectric layer 31 (e.g., a silicon oxide, another oxide material, a nitride material, or another suitable dielectric material) on the second nanosheet stack on semiconductor substrate 11, in accordance with an embodiment of the present invention. As depicted, FIG. 3 semiconductor substrate 11 with multiple alternating nanosheet layers of sacrificial layer 25 and channel material 26, and dielectric layer 31 on the top nanosheet layer of channel material 26. Using a known deposition process, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), or any other known dielectric material deposition process used in semiconductor manufacturing, dielectric layer 31 can be deposited on the top of the second nanosheet stack. While FIG. 3 depicts dielectric layer 31 on the top nanosheet layer of sacrificial layer 25 in the second nanosheet stack, in other embodiments, dielectric layer 31 is deposited on the top nanosheet layer of sacrificial material 21 in the first nanosheet stack depicted in FIG. 2A.

[0059] FIG. 4 depicts a cross-sectional view of the semiconductor structure after joining the second nanosheet stack to the first nanosheet stack, in accordance with an embodiment of the present invention. As depicted, FIG. 4 includes the first nanosheet stack composed of sacrificial material 21 and channel material 22 on semiconductor substrate 10, dielectric layer 31 between the first nanosheet stack and the second nanosheet stack, and the second nanosheet stack that is composed of sacrificial layer 25 and channel material 26. Using known wafer bonding processes, the top surface of dielectric layer 31 on sacrificial layer 25 of the second nanosheet stack is bonded to sacrificial material 21 in the first nanosheet stack on semiconductor substrate 10. In other embodiments, when dielectric layer 31 is deposited on the first nanosheet stack, dielectric layer 31 is bonded to the top of the second nanosheet stack. In other embodiments, a dielectric layer can be deposited on the top surfaces of each nanosheet stack on each substrate, and then two nanosheet stacks are joined together by bonding the two dielectric layers. As

depicted, after bonding dielectric layer 31 to sacrificial material 21, semiconductor substrate 11 can be removed using known semiconductor substrate or wafer removal processes, such as a known handler wafer or substrate release process. In other embodiments, semiconductor substrate 10 can be removed rather than semiconductor substrate 11.

[0060] After joining the two nanosheet stacks that are separated by dielectric layer 31, a single semiconductor substrate structure can be formed with two vertically aligned nanosheet stacks. Using this method, one nanosheet stack of channel and sacrificial nanosheet layers have a first crystalline surface orientation and the second nanosheet stack of channel, and sacrificial material nanosheet layer have a second crystalline surface orientation. More specifically, as depicted in FIG. 4, the semiconductor substrate structure on semiconductor substrate 10 has the first nanosheet stack composed of alternating layers of sacrificial material 21 and channel material 22 where each layer of sacrificial material 21 and channel material 22 has a {100} crystalline surface orientation. The first nanosheet stack is separated by dielectric layer 31 from the second nanosheet stack that is composed of alternating layers of sacrificial layer 25 and channel material 26 that each have a {110} crystalline surface orientation.

[0061] After bonding dielectric layer 31 to sacrificial material 21 in the nanosheet stack composed of sacrificial material 21 and channel material 22, semiconductor substrate 11 is removed (e.g., instead of removing semiconductor substrate 11 as depicted in FIG. 4). In these embodiments, the bottom nanosheet stack on semiconductor substrate 10 can provide a {100} crystalline surface orientation preferred for NFET CMOS devices and the second or top nanosheet stack can provide a {110} crystalline surface orientation preferred for PFET CMOS devices.

[0062] In other embodiments, the base semiconductor substrate is semiconductor substrate 11 that has a {110} crystalline surface orientation and in this embodiment, semiconductor substrate 10 is removed instead of semiconductor substrate 11. For example, semiconductor substrate 11 with a {110} crystalline surface orientation is under the first nanosheet stack with a preferred {110} crystalline surface orientation for PFET CMOS devices.

[0063] The semiconductor substrate structure depicted in FIG. 4 includes semiconductor substrate 10 covered by a nanosheet stack with a {100} crystalline surface orientation that is

preferred for NFET CMOS devices. The semiconductor structure depicted in FIG. 4 also provides a second nanosheet stack directly above dielectric layer 31 with a {110} crystalline surface orientation that is preferred for PFET CMOS devices.

[0064] In this way, the semiconductor substrate structure depicted in FIG. 4 can provide the first nanosheet stack on semiconductor substrate 10 where the first nanosheet stack formed on semiconductor substrate 10 has a {100} crystalline surface orientation that will provide good or optimal electrical performance for NFET devices while also providing, on the same semiconductor substrate structure, the second nanosheet stack with a {110} crystalline surface orientation will provide an improved or optimal electrical performance for PFET CMOS devices.

[0065] The method of forming the semiconductor structure depicted in FIG. 4 provides a way to form a single semiconductor substrate with two nanosheet stacks with two different crystalline surface orientations that are electrically isolated by dielectric layer 31 between the two nanosheet stacks.

[0066] FIG. 5 depicts a top view of the semiconductor structure after depositing hardmask 62 on an exposed top surface of the second nanosheet stack, in accordance with an embodiment of the present invention. FIG. 5 depicts a step in forming a stacked CMOS device from the semiconductor substrate structure depicted in FIG. 4. Using known deposition processes, such as CVD or PVD, a layer of hardmask 62 is deposited on the exposed top nanosheet layer of sacrificial layer 25. As depicted in FIG. 5, the top view of the semiconductor structure after hardmask 62 deposition illustrates a location of an X-X cross-section that is perpendicular to a future gate structure of a CMOS device formed in later process steps and a location of a Y-Y cross-section that is parallel to a future gate structure of the CMOS device depicted later in FIG. 10B.

[0067] FIG. 6A depicts a cross-sectional view in the X-X direction of the semiconductor structure after removing portions of hardmask 62, the second nanosheet stack composed of sacrificial layer 25 and channel material 26, dielectric layer 31, and the first nanosheet stack composed of sacrificial material 21 and channel material 22, in accordance with an embodiment of the present invention. The top layer of sacrificial layer 25 of the second nanosheet stack is patterned, for example using lithography and selectively etched, for example using a reactive ion

etching process to remove portions of the second nanosheet stack, dielectric layer 31, and the first nanosheet stack on semiconductor substrate 10. As depicted, FIG. 6A includes the remaining portion of the first nanosheet stack (i.e., alternating layers of sacrificial material 21 and channel material 22) on a portion of semiconductor substrate 10, the remaining portion of dielectric layer 31, and the remaining portion of the second nanosheet stack (i.e., alternating layer of sacrificial layer 25 and channel material 26).

[0068] FIG. 6B depicts a cross-sectional view in the Y-Y direction of the semiconductor structure after removing portions of hardmask 62, the second nanosheet stack composed of sacrificial layer 25 and channel material 26, dielectric layer 31, and the first nanosheet stack composed of sacrificial material 21 and channel material 22, in accordance with an embodiment of the present invention. As depicted, FIG. 6B illustrates the elements depicted in FIG. 6A. Using the processes previously discussed above with respect to FIG. 6A, portions of the second nanosheet stack, dielectric layer 31, and the first nanosheet stack are selectively removed above portions of semiconductor substrate 10.

[0069] FIG. 7A depicts a cross-sectional view in the X-X direction after forming dummy gate structure 73, in accordance with an embodiment of the present invention. As depicted, FIG. 7A includes the elements of FIG. 6A and dummy gate structure 73. Using known processes and materials to deposit dummy gate structure 73, dummy gate structure 73 is formed on the top layer of sacrificial layer 25. In some embodiments, a layer of gate dielectric material, such as a high k dielectric material may be deposited on the top layer of sacrificial layer 25 followed by a deposition of a dummy gate material for dummy gate structure 73. The top surface of dummy gate structure 73 can be patterned and etched, for example, using RIE, to form dummy gate structure 73 on a portion of the top nanosheet layer of sacrificial layer 25 as depicted in FIG. 6A.

[0070] FIG. 7B depicts a cross-sectional view in the Y-Y direction after forming dummy gate structure 73, in accordance with an embodiment of the present invention. As depicted in a cross-sectional view that is parallel to dummy gate structure 73, using the processes discussed above with reference to FIG. 7A, a layer of a dummy gate material may be deposited on sacrificial layer 25 and around the remaining portions of the two nanosheet stacks. In some cases, an optional layer of a gate dielectric material covered a layer of dummy gate material may

be deposited on sacrificial layer 25 and around the exposed sidewalls of the nanosheet stacks. The top surface of dummy gate structure 73 is patterned and selectively etched leaving a portion of dummy gate structure 73 over sacrificial layer 25, over a portion of semiconductor substrate 10, and around the sidewalls of the first nanosheet stack, the second nanosheet stack, and dielectric layer 31 as depicted in FIG. 7B.

[0071] FIG. 8A depicts a cross-sectional view in the X-X direction depicted in FIG. 5 after forming protective spacer 81 and inner spacers 83, in accordance with an embodiment of the present invention. As depicted, FIG. 8A illustrates the elements of FIG. 7A and protective spacer 81. Protective spacer 81 can be formed on a portion of sacrificial layer 25 around dummy gate structure 73 as depicted using known spacer deposition processes, such as atomic layer deposition (ALD), CVD, or plasma-enhanced CVD (PECVD).

[0072] After depositing protective spacer 81, exposed portions of the second nanosheet stack (i.e., nanosheet layer of sacrificial layer 25 and channel material 26), portions of dielectric layer 31 under the exposed portions of the second nanosheet stack, and the portions of the first nanosheet stack (i.e., nanosheet layers of sacrificial material 21 and channel material 22) under the exposed portions of the first nanosheet stack and under the exposed portions of dielectric layer 31 are removed, for example, using RIE or IBE.

[0073] After removing the portions of the two nanosheet stacks and dielectric layer 31 not covered by protective spacer 81 or dummy gate structure 73, a lateral etching process, for example, using a vapor phase hydrochloric acid (HCl) dry etch or a wet etch process containing a mix of ammonia and hydrogen peroxide or another suitable etching process for removing an outside edge portion of sacrificial layer 25 and sacrificial material 21. After performing the lateral etch, inner spacers 83 can be deposited in the recesses formed along an outer edge portion of each layer of sacrificial layer 25 and sacrificial material 21. Each of inner spacers 83 horizontally abuts one of sacrificial layer 25 or sacrificial material 21. Inner spacers 83 vertically separate the outside edges of one of channel material 26 or channel material 22 from other adjacent channel material layers as depicted in FIG. 8A. Inner spacers 83 create a horizontal separation of each layer of sacrificial material (e.g., sacrificial layers 21 and 25) from

the outside edge of the remaining portions of the nanosheet stacks and in the final device depicted in FIG. 10A and 10B, that separates the metal gate from the source/drains.

[0074] FIG. 8B depicts a cross-sectional view in the Y-Y direction after forming protective spacer 81 (not depicted in FIG. 8B) and inner spacers 83 (not depicted in FIG. 8B), in accordance with an embodiment of the present invention. As depicted, FIG. 8B includes the elements of FIG. 7B.

[0075] FIG. 9A depicts a cross-sectional view in the X-X direction of the semiconductor structure after forming source/drains (S/D) 94 for a n-type field-effect device and S/D 92 for a p-type field-effect device, in accordance with an embodiment of the present invention. Using epitaxy, S/D 92 is grown on the exposed sidewall surfaces of channel material 22 with a {100} crystalline surface orientation and inner spacer 83 of the first nanosheet stack for the NFET device. Using epitaxy, S/D 94 is grown on the exposed sidewall surfaces of channel material 26 with a {110} crystalline surface orientation and inner spacer 83 of the second nanosheet stack for the PFET device. In some embodiments, S/D 92 is doped with an n-type dopant and S/D 94 is doped with a p-type dopant.

[0076] FIG. 9B depicts a cross-sectional view in the Y-Y direction of the semiconductor structure after forming source/drains (S/D) 94 (not depicted in FIG. 9B) for an n-type field-effect device and S/D 92 (not depicted in FIG. 9B) for a p-type field-effect, in accordance with an embodiment of the present invention. As depicted, FIG. 9B illustrates essentially the same elements as FIG. 8B in the cross-section parallel to the gate or dummy gate structure 73.

[0077] FIG. 10A depicts a cross-sectional view in the X-X direction of the semiconductor structure after forming replacement gate structure 93, in accordance with an embodiment of the present invention. As depicted in the cross-sectional view perpendicular to replacement gate structure 93, FIG. 10A illustrates a portion of an NFET hGAA device formed with the first nanosheet stack composed of nanosheet layers of channel material 22 with a {100} crystalline surface orientation, replacement gate structure 93, inner spacers 83, and S/D 92. The NFET hGAA device, as depicted, is above a portion of semiconductor substrate 10 and below the PFET hGAA device. The PFET hGAA device, as depicted, is on a portion of dielectric layer 31 and is formed from the second nanosheet stack composed of nanosheet layers of channel

material 26 with a {110} crystalline surface orientation, S/D 94, inner spacers 83, and replacement gate structure 93. As depicted, FIG. 10A also includes ILD 95 above exposed portions of semiconductor substrate 10 and surrounding the NFET hGAA device, the PFET hGAA device, and protective spacer 81 around the upper portion of replacement gate structure 93.

[0078] The semiconductor structure depicted in FIG. 10A can be formed by depositing ILD 95 above exposed portions of semiconductor substrate 10 and around the first nanosheet stack with exposed inner spacers 83, dielectric layer 31, and the second nanosheet stack with exposed inner spacers 83, and protective spacer 81.

[0079] Dummy gate structure 73 can be removed using a dry or a wet etching process. Sacrificial layers 21 and 25 are removed using known dry or wet etching processes used in nanosheet semiconductor device formation.

[0080] After removing dummy gate structure 73 and sacrificial layers 21 and 25, replacement gate structure 93 can be formed. In some examples, using known semiconductor manufacturing processes for forming replacement gate structure 93 with a metal gate electrode (not depicted), a gate dielectric material (not depicted) or a high k metal gate dielectric (e.g., HfO, AlO, ZrO, TaO, etc.) may be deposited first on exposed surfaces in the two nanosheet stacks and between protective spacer 81, for example, using ALD or CVD. A metal gate electrode material (e.g., TiN, TiAl, TiC, TaN, Ta, Al, W, Ru, etc.) is deposited to form replacement gate structure 93.

[0081] FIG. 10B depicts a cross-sectional view in the Y-Y direction of the semiconductor structure after forming replacement gate structure 93, in accordance with an embodiment of the present invention. FIG. 10B is a cross-sectional view parallel the gate of a semiconductor device structure with an NFET hGAA device and a PFET hGAA device on semiconductor substrate 10. As depicted, the elements illustrated in FIG. 10B are essentially the same as the elements illustrated in FIG. 9B except that ILD 95 is deposited, dummy gate structure 73 is removed, and replaced, each of sacrificial material 21 and sacrificial layer 25 are removed and a metal gate structure labeled as replacement gate structure 93 is added to replace dummy gate structure 73

between channel materials 22 and 25, respectively. The semiconductor device structure depicted in FIG. 10B is formed with the processes discussed above with reference to FIG. 10A.

[0082] FIG. 10B illustrates a portion of an NFET hGAA device formed with the first nanosheet stack composed of nanosheet layers of channel material 22 with a {100} crystalline surface orientation with replacement gate structure 93 on semiconductor substrate 10 with inner spacers 83 and S/D 92. FIG. 10B also illustrates a portion of a PFET hGAA device above the NFET hGAA device, where the PFET hGAA is formed from the second nanosheet stack composed of nanosheet layers of channel material 26 with a {110} crystalline surface orientation with replacement gate structure 93 on dielectric layer 31, inner spacers 83, and S/D 94. As depicted, FIG. 10B includes ILD 95 above exposed portions of semiconductor substrate 10 and surrounding the NFET hGAA device, the PFET hGAA device, and protective spacer 81 around the upper portion of replacement gate structure 93.

[0083] Dummy gate structure 73 can be removed after depositing ILD 95 using a known dry etching process (e.g., RIE) or a wet etching process. Sacrificial layers 21 and 25 are removed using known dry or wet etching processes.

[0084] After removing dummy gate structure 73 and sacrificial layers 21 and 25, replacement gate structure 93 can be formed. In some examples, using known semiconductor processes for metal gate formation, a thin layer of a gate dielectric material (not depicted), such as a high k dielectric material (e.g., HfO, AlO, ZrO, TaO, etc.) may be deposited on exposed surfaces in the two nanosheet stacks, inner spacers 83, and protective spacer 81, for example, using ALD or CVD. A metal gate electrode material (e.g., TiN, TiAl, TiC, TaN, Ta, Al, W, Ru, etc.) can be deposited on the gate dielectric material to form replacement gate structure 93.

[0085] In this way, the semiconductor device structures as depicted in FIG. 10A and 10B provide a stacked CMOS device. The stacked CMOS device as depicted in FIGs. 10A and 10B are hGAA devices with a preferred crystal orientation in each of the NFET hGAA device on semiconductor substrate 10 and the PFET hGAA device above the NFET hGAA device. Each of the NFET and the PFET hGAA devices can have the preferred crystal orientation by using two different nanosheet stacks that are each formed on a different semiconductor substrate with different crystal orientations. Using the methods discussed in embodiments of the present

invention, an NFET hGAA device with a preferred {100} crystalline surface orientation and a PFET hGAA device with a preferred {110} crystalline surface orientation can be vertically aligned and formed on a single semiconductor substrate using two nanosheet stacks with two different crystal orientations

[0086] The methods described herein can be used in the fabrication of integrated circuit chips or semiconductor chips. The resulting semiconductor chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case, the semiconductor chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher-level carrier) or in a multichip package (such as a ceramic carrier that has either or both of surface interconnections or buried interconnections). In any case, the semiconductor chip is then integrated with other semiconductor chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes semiconductor chips, ranging from toys and other low-end applications to advanced computer products having a display, memory, a keyboard or other input device, and a central processor.

CLAIMS

What is claimed is:

1. A semiconductor substrate structure, the semiconductor substrate comprising:
a semiconductor substrate with a first crystalline surface orientation;
a first nanosheet stack with the first crystalline surface orientation on the semiconductor substrate; and
a second nanosheet stack with a second crystalline surface orientation above the first nanosheet stack, wherein the first nanosheet stack and the second nanosheet stack are separated by a dielectric material.
2. The semiconductor substrate of claim 1, wherein the first crystalline surface orientation is a {100} crystalline surface orientation.
3. The semiconductor substrate of claim 2, wherein the second crystalline surface orientation is a {110} crystalline surface orientation.
4. The semiconductor substrate of claim 1, wherein the first crystalline surface orientation is a {110} crystalline surface orientation.
5. The semiconductor substrate of claim 4, wherein the second crystalline surface orientation is a {100} crystalline surface orientation.
6. The semiconductor substrate of claim 1, wherein the dielectric material is an oxide layer between the first nanosheet stack and the second nanosheet stack.
7. The semiconductor substrate of claim 4, wherein the first crystalline surface orientation is a preferred crystalline surface orientation for a PFET and the second crystalline surface orientation is a preferred crystalline surface orientation for an NFET.

8. The semiconductor substrate of claim 1, wherein the first nanosheet stack and the second nanosheet are composed of alternating nanosheet layers of a sacrificial semiconductor material and a channel material.

9. The semiconductor substrate of claim 8, wherein the sacrificial semiconductor material is composed of silicon-germanium and the channel material is composed of silicon.

10. A method of forming a semiconductor substrate structure with two nanosheet stacks where each of the two nanosheet stacks has a different crystalline surface orientation, the method comprising:

epitaxially growing a first nanosheet stack of alternating nanosheet layers of a sacrificial semiconductor material and a channel semiconductor material on a first semiconductor substrate with a first crystalline surface orientation;

epitaxially growing a second nanosheet stack alternating nanosheet layers of the sacrificial semiconductor material and the channel semiconductor material on a second semiconductor substrate with a second crystalline surface orientation;

depositing an oxide layer on a top layer of the sacrificial semiconductor material in one of the first nanosheet stack or the second nanosheet stack;

bonding a top surface of the first nanosheet stack to a top surface of the second nanosheet stack; and

removing one of the first semiconductor substrate or the second semiconductor substrate from under one of the first nanosheet stack or the second nanosheet stack.

11. The method of claim 10, wherein the first crystalline surface orientation is one of a {100} crystalline surface orientation when the first semiconductor substrate has the {100} crystalline surface orientation or a {110} crystalline surface orientation when the first semiconductor substrate has the {110} crystalline surface orientation.

12. The method of claim 11, wherein the first crystalline surface orientation is the {100} crystalline surface orientation and the second crystalline surface orientation is the {110} crystalline surface orientation.

13. The method of claim 11, wherein the first crystalline surface orientation is the {110} crystalline surface orientation and the second crystalline surface orientation is the {100} crystalline surface orientation.

14. The method of claim 10, wherein the sacrificial semiconductor material is epitaxially grown on the first semiconductor substrate and the second semiconductor substrate.

15. The method of claim 14, wherein the channel material is epitaxially grown on the sacrificial semiconductor material in each of the first nanosheet stack and the second nanosheet stack.
16. The method of claim 10, wherein the sacrificial semiconductor material is composed of silicon and germanium and the channel material is silicon.

17. A semiconductor device composed of a p-type field-effect transistor and an n-type field-effect transistor that are vertically stacked in the semiconductor device, the semiconductor device comprising:

a semiconductor substrate;

a p-type field-effect transistor with a {110} crystalline surface orientation in a channel material in a first nanosheet stack; and

an n-type field-effect transistor with a {100} crystalline surface orientation in a channel material in a second nanosheet, wherein the p-type field-effect transistor and the n-type field-effect transistor are vertically aligned and isolated by a dielectric material.

18. The semiconductor device of claim 17, wherein the p-type field-effect transistor and the n-type field-effect transistor are a horizontal gate-all-around devices.

19. The semiconductor device of claim 17, wherein the p-type field-effect transistor with the {110} crystalline surface orientation in the channel material has a preferred crystal orientation for the p-type field-effect transistor.

20. The semiconductor device of claim 17, wherein the n-type field-effect transistor with the {100} crystalline surface orientation in the channel material has a preferred crystal orientation for the n-type field-effect transistor.

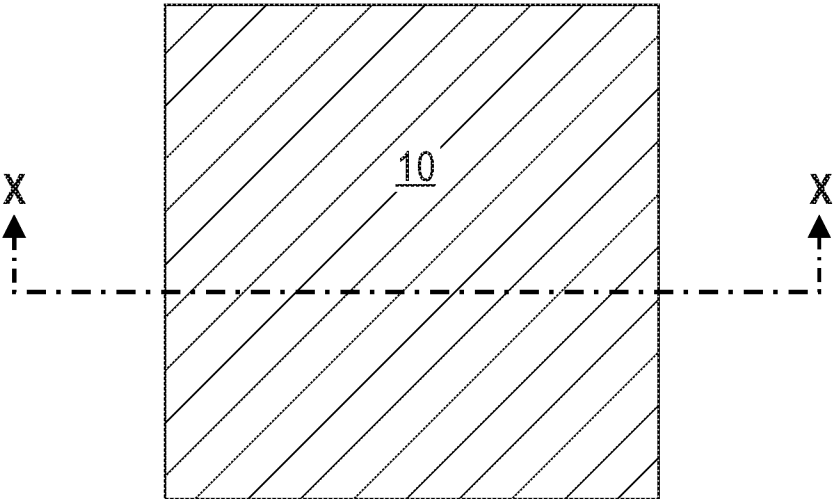


FIG. 1A

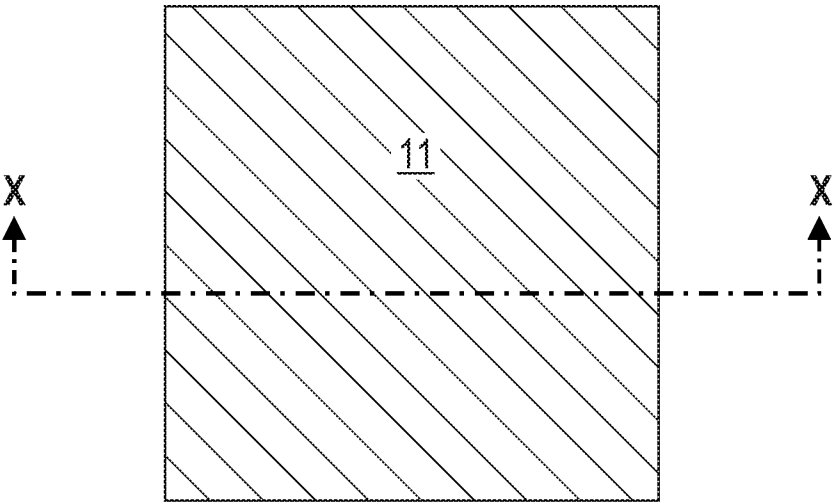


FIG. 1B

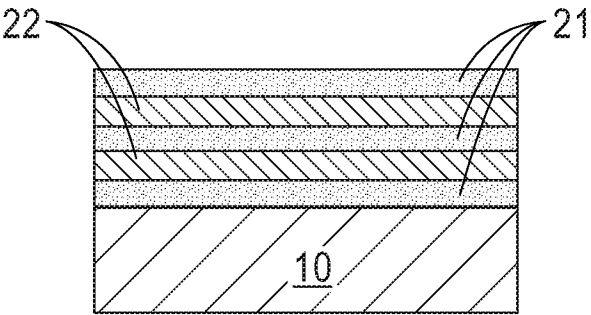


FIG. 2A

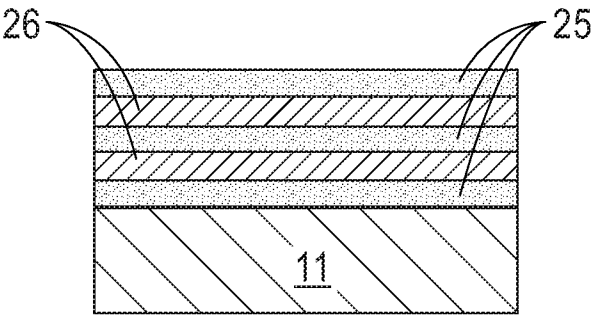


FIG. 2B

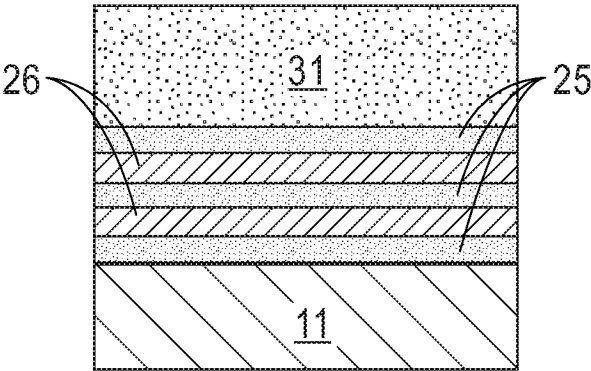


FIG. 3

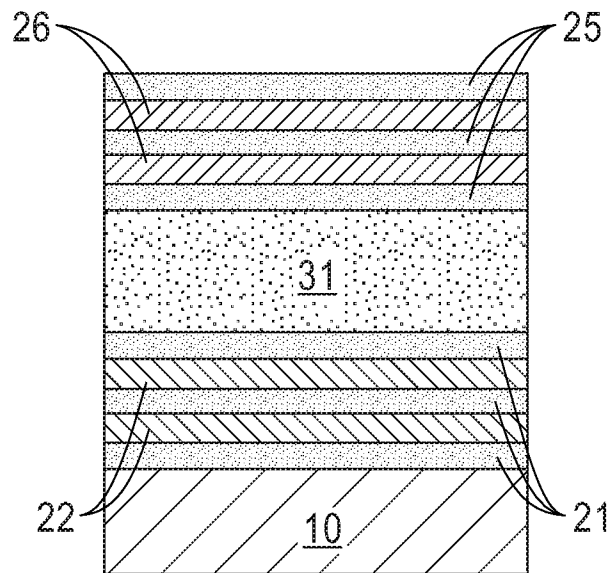


FIG. 4

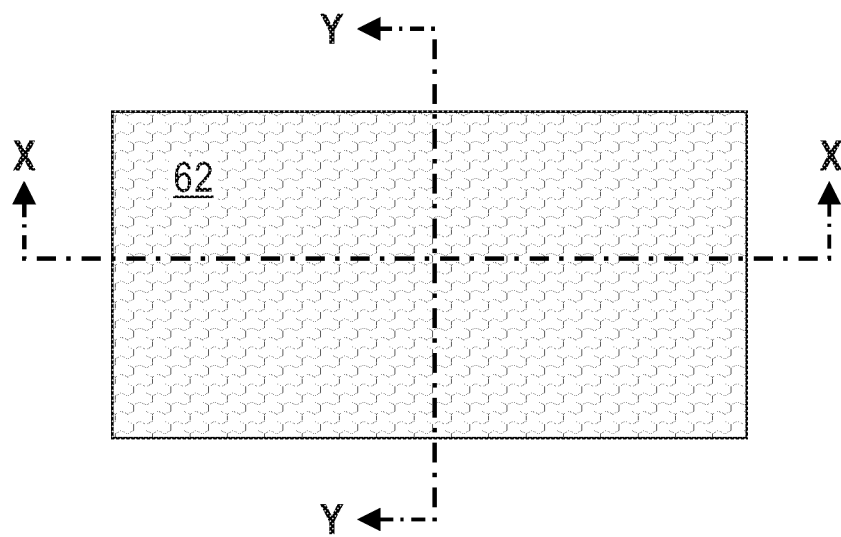


FIG. 5

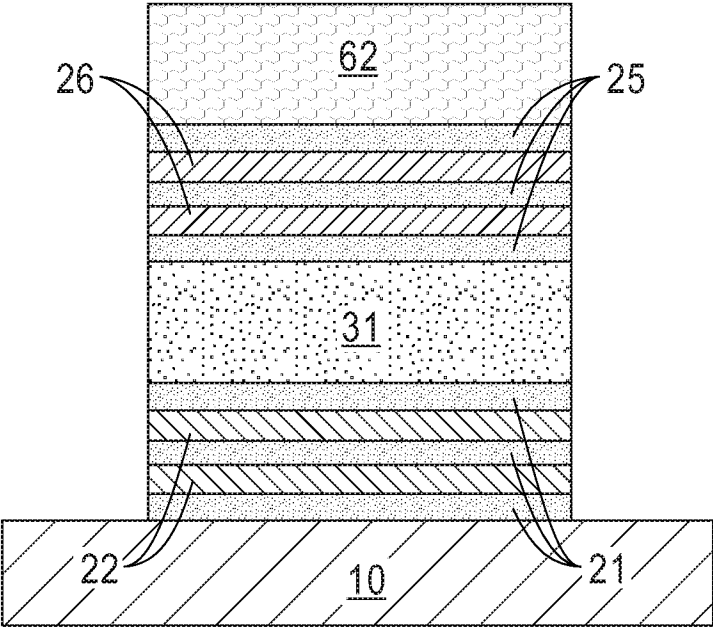


FIG. 6A

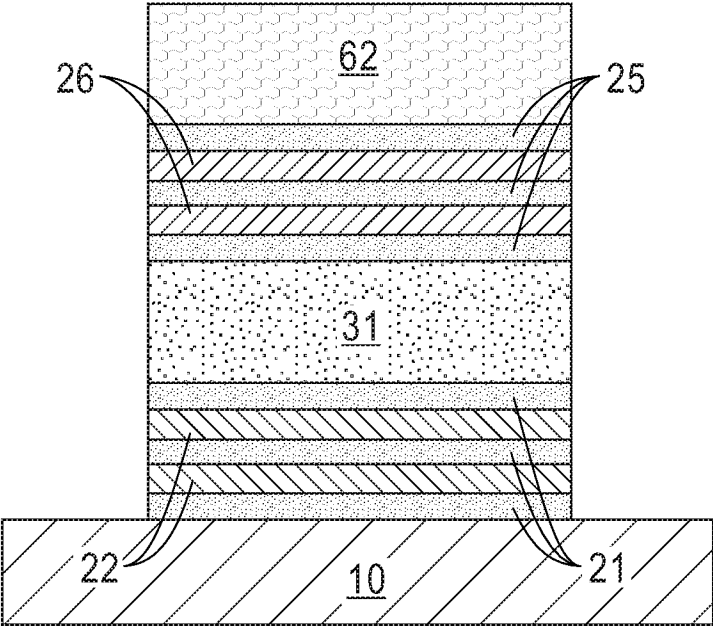


FIG. 6B

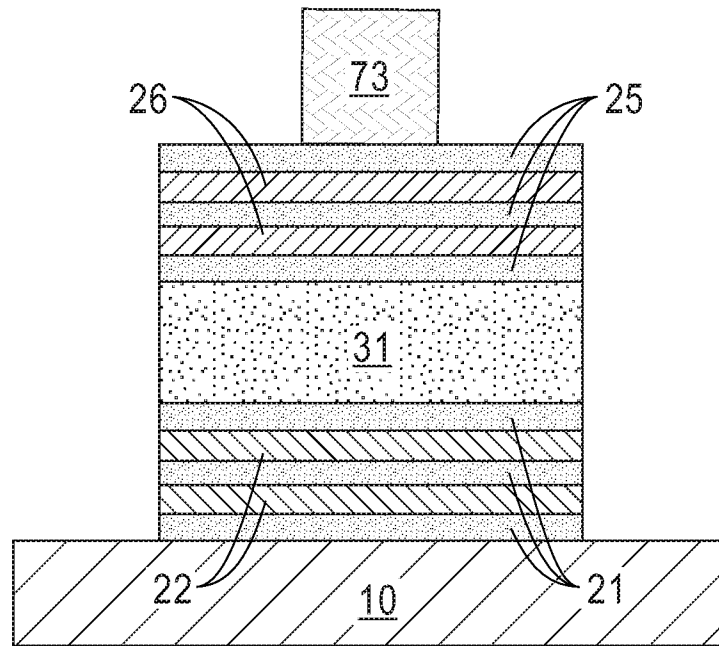


FIG. 7A

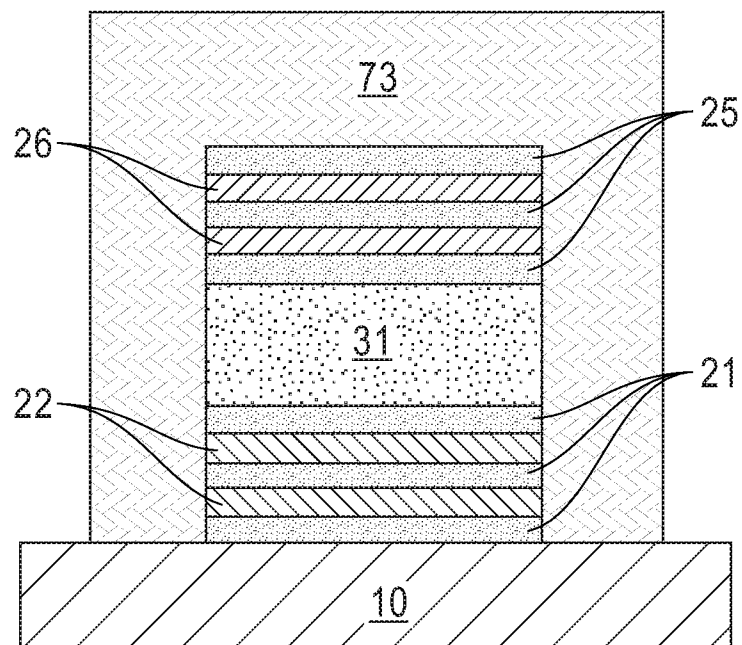


FIG. 7B

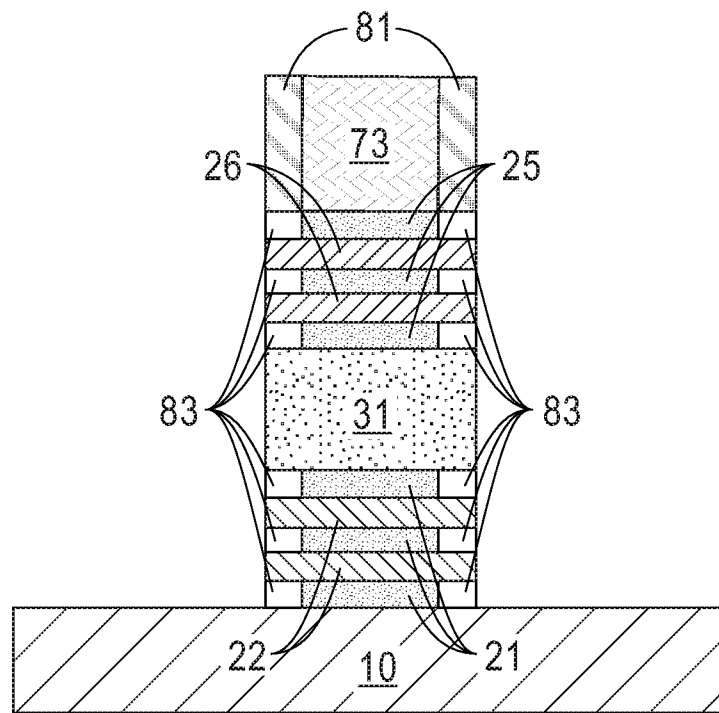


FIG. 8A

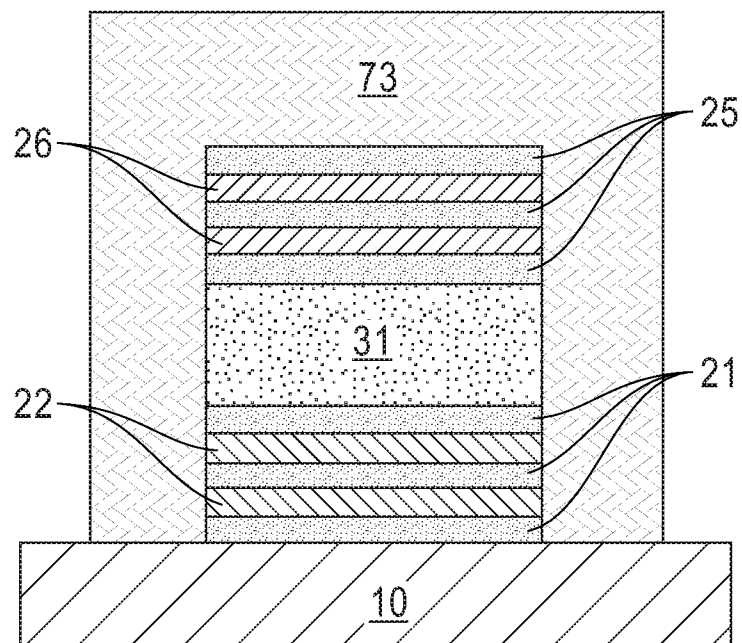


FIG. 8B

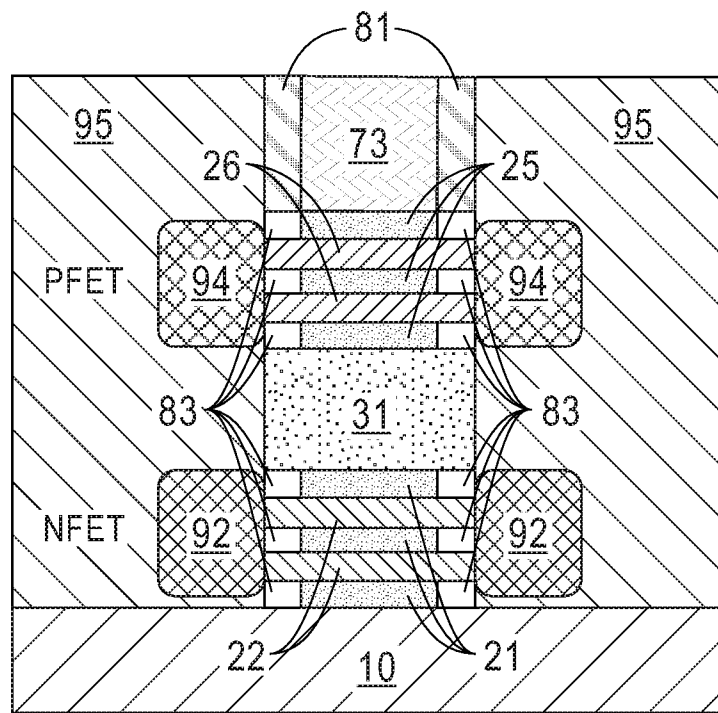


FIG. 9A

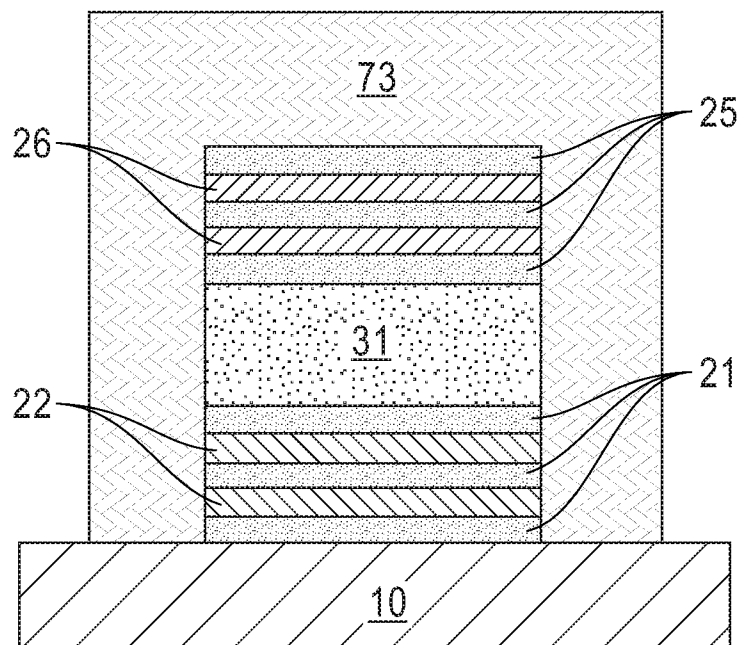


FIG. 9B

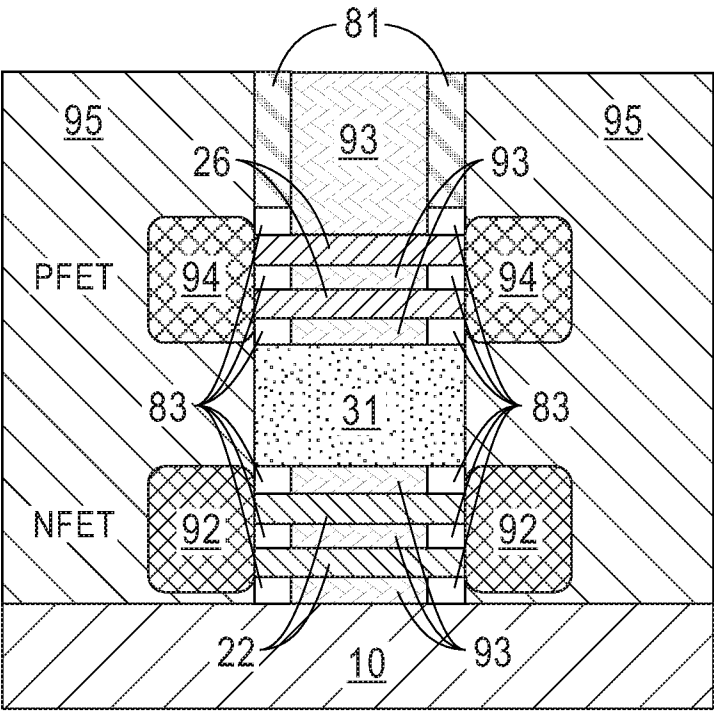


FIG. 10A

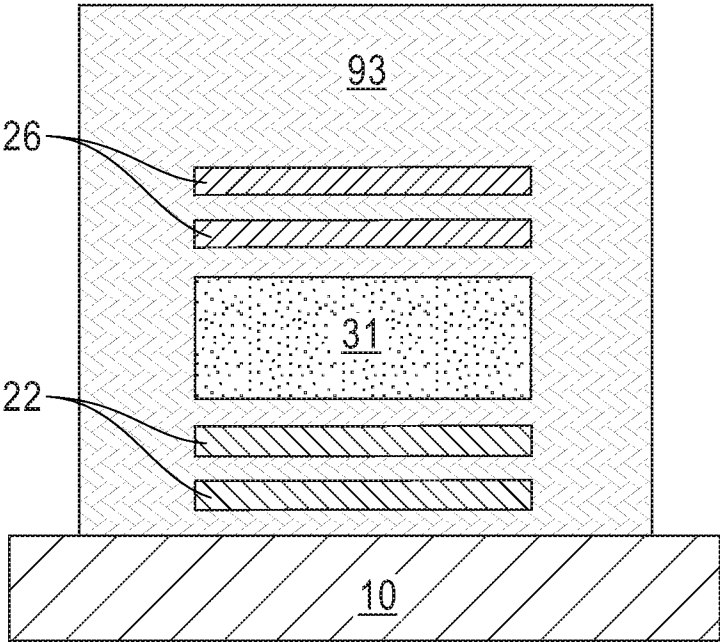


FIG. 10B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2022/120113

A. CLASSIFICATION OF SUBJECT MATTER		
H01L 29/06(2006.01)i; H01L 29/15(2006.01)i; H01L 27/088(2006.01)i; H01L 27/092(2006.01)i; H01L 21/8238(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) CNKI, CNPAT, IEEE, WPI:IBM, stack, nanosheet, nanowire, gaa, gate, all, around, vertical, transistor, MOS, FET, crystal+, orientation, silicon, transfer, bond+, join+, insulat+, dielectric		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2021202326 A1 (SCHWARZENBACH, Walter et al.) 01 July 2021 (2021-07-01) claims 1-20, description, paragraphs [0059]-[0148], figures 1-3	1-20
Y	US 9472555 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 18 October 2016 (2016-10-18) claims 1-10, description, column 2 line 22-column 15 line 53, figures 1-12	1-20
A	US 10483166 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 19 November 2019 (2019-11-19) the whole document	1-20
A	CN 107492552 A (IMEC VZW et al.) 19 December 2017 (2017-12-19) the whole document	1-20
A	CN 106365106 A (HANGZHOU SILAN INTEGRATED CIRCUIT CO., LTD.) 01 February 2017 (2017-02-01) the whole document	1-20
A	US 2015263088 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 17 September 2015 (2015-09-17) the whole document	1-20
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 26 November 2022		Date of mailing of the international search report 16 December 2022
Name and mailing address of the ISA/CN National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China Facsimile No. (86-10)62019451		Authorized officer ZHOU,Zhongtang Telephone No. 86-(10)-53961222

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2022/120113

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2005268438 A (SHARP K.K.) 29 September 2005 (2005-09-29) the whole document	1-20

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2022/120113

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2021202326	A1	01 July 2021	FR	3085536	A1	06 March 2020
				WO	2020049251	A1	12 March 2020
				KR	20210049910	A	06 May 2021
				SG	11202101776X	A	30 March 2021
				CN	112640090	A	09 April 2021
				EP	3847693	A1	14 July 2021
				TW	202018825	A	16 May 2020
US	9472555	B1	18 October 2016	US	2017179128	A1	22 June 2017
				US	9887197	B2	06 February 2018
US	10483166	B1	19 November 2019	US	2020020587	A1	16 January 2020
				US	10896851	B2	19 January 2021
CN	107492552	A	19 December 2017	US	2017358586	A1	14 December 2017
				US	11018235	B2	25 May 2021
CN	106365106	A	01 February 2017	CN	106365106	B	04 September 2018
US	2015263088	A1	17 September 2015	US	9224811	B2	29 December 2015
JP	2005268438	A	29 September 2005	None			