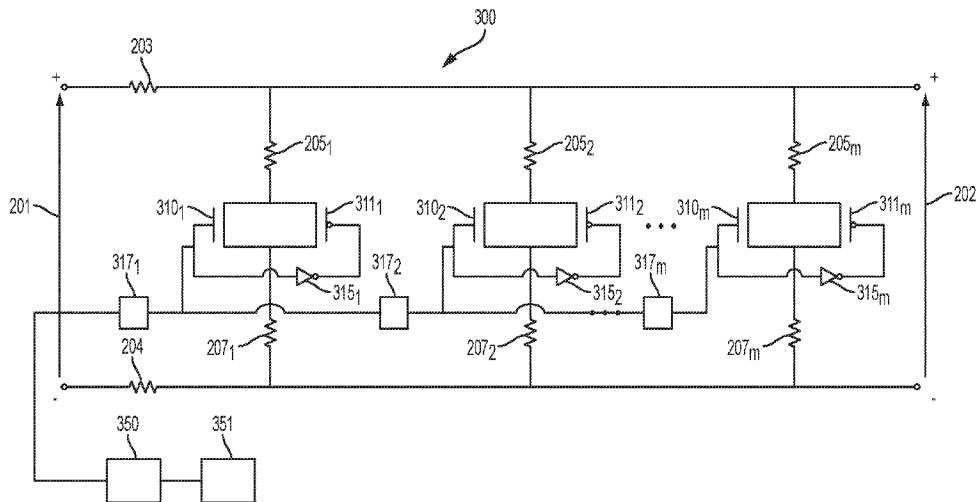




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(57) Abrégé/Abstract:

An ultrasound device, including a profile generator, an encoder configured to receive a profile signal from the profile generator, and an attenuator configured to receive a signal representing an output of an ultrasound sensor and coupled to the encoder to receive a control signal from the encoder, the attenuator including a plurality of attenuator stages, the attenuator configured to produce an output signal that is an attenuated version of the input signal.

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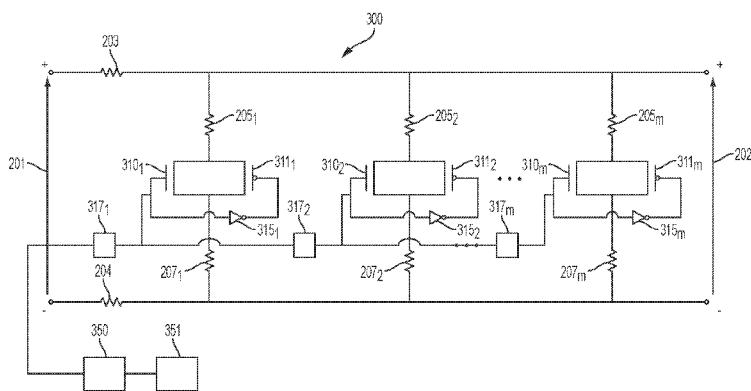


FIG. 3

(57) Abstract: An ultrasound device, including a profile generator, an encoder configured to receive a profile signal from the profile generator, and an attenuator configured to receive a signal representing an output of an ultrasound sensor and coupled to the encoder to receive a control signal from the encoder, the attenuator including a plurality of attenuator stages, the attenuator configured to produce an output signal that is an attenuated version of the input signal.

## TIME GAIN COMPENSATION CIRCUIT AND RELATED APPARATUS AND METHODS

[0001]

### BACKGROUND

#### Field

[0002] The present application relates to ultrasound devices having a time gain compensation circuit.

#### Related Art

[0003] Ultrasound devices may be used to perform diagnostic imaging and/or treatment. Ultrasound imaging may be used to see internal soft tissue body structures. Ultrasound imaging may be used to find a source of a disease or to exclude any pathology. Ultrasound devices use sound waves with frequencies which are higher than those audible to humans. Ultrasonic images are made by sending pulses of ultrasound into tissue using a probe. The sound waves are reflected off the tissue, with different tissues reflecting varying degrees of sound. These reflected sound waves may be recorded and displayed as an image to the operator. The strength (amplitude) of the sound signal and the time it takes for the wave to travel through the body provide information used to produce an image.

[0004] Many different types of images can be formed using ultrasound devices. The images can be real-time images. For example, images can be generated that show two-dimensional cross-sections of tissue, blood flow, motion of tissue over time, the location of blood, the presence of specific molecules, the stiffness of tissue, or the anatomy of a three-dimensional region.

### SUMMARY

[0005] According to an aspect of the present application, there is provided an ultrasound device, comprising a profile generator, an encoder configured to receive a profile

signal from the profile generator, and an attenuator configured to receive a signal representing an output of an ultrasound sensor and coupled to the encoder to receive a control signal from the encoder, the attenuator comprising a plurality of binary attenuator stages, the attenuator configured to produce an output signal that is an attenuated version of the input signal.

**[0006]** According to an aspect of the present application, there is provided an ultrasound device, comprising a profile generator, an encoder configured to receive a profile signal from the profile generator, and an attenuator configured to receive a signal representing an output of an ultrasound sensor and coupled to the encoder to receive a control signal from the encoder, the attenuator comprising a plurality of stages, each stage in the plurality of stages having a predetermined attenuation, the attenuator configured to produce an output signal that is an attenuated version of the input signal.

**[0006a]** According to one aspect of the present invention, there is provided an ultrasound device, comprising: a profile generator; an encoder configured to receive a profile signal from the profile generator; an attenuator configured to receive an input signal representing an output of an ultrasound sensor and coupled to the encoder to receive a control signal from the encoder, the attenuator comprising a plurality of binary attenuator stages, the attenuator configured to produce an output signal that is an attenuated version of the input signal; and a fixed gain amplifier having a gain greater than 0 dB and configured to receive the output signal from the attenuator and amplify the output signal.

**[0006b]** According to another aspect of the present invention, there is provided an ultrasound device, comprising: a profile generator; an encoder configured to receive a profile from the profile generator; an attenuator configured to receive an input signal representing an output of an ultrasound sensor and coupled to the encoder to receive a control signal from the encoder, the attenuator comprising a plurality of stages, each stage in the plurality of stages having a predetermined attenuation, the attenuator configured to produce an attenuated output signal that is an attenuated version of the input signal; and a fixed gain amplifier having a gain greater than 0 dB and configured to receive the output signal from the attenuator and amplify the output signal.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0007]** Various aspects and embodiments of the application will be described with reference to the following figures. It should be appreciated that the figures are not necessarily drawn to scale. Items appearing in multiple figures are indicated by the same reference number in all the figures in which they appear.

**[0008]** FIG. 1 is a block diagram of an ultrasound device including a time gain compensation circuit, according to a non-limiting embodiment of the present application.

**[0009]** FIG. 2A is a circuit diagram illustrating a differential parallel implementation of the attenuator of FIG. 1, according to a non-limiting embodiment of the present application.

**[0010]** FIG. 2B is a circuit diagram illustrating a differential series implementation of the attenuator of FIG. 1, according to a non-limiting embodiment of the present application.

**[0011]** FIG. 2C is a circuit diagram illustrating a single-ended parallel implementation of the attenuator of FIG. 1, according to a non-limiting embodiment of the present application.

**[0012]** FIG. 2D is a circuit diagram illustrating a single-ended series implementation of the attenuator of FIG. 1, according to a non-limiting embodiment of the present application.

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**[0013]** FIG. 3 is a circuit diagram illustrating an implementation of the attenuator of FIG. 1, including complementary switches, according to a non-limiting embodiment of the present application.

**[0014]** FIG. 4 is a circuit diagram illustrating the digital encoder and shift register used to determine the state of the complementary switches of FIG. 3, according to a non-limiting embodiment of the present application.

**[0015]** FIG. 5 is a graph illustrating the temporal evolution of three control signals and the state of the shift register of FIG. 4, according to a non-limiting embodiment of the present application.

**[0016]** FIG. 6 is a graph illustrating a time gain compensation response triggered by the reception of a signal featuring a dip, according to a non-limiting embodiment of the present application.

#### DETAILED DESCRIPTION

**[0017]** The inventors have recognized and appreciated that the power consumption and the accuracy associated with time gain compensation circuits may be improved by replacing variable amplifiers with amplification circuits comprising variable attenuators and fixed gain amplifiers. This approach can significantly simplify the amplifier design shifting the problem from the design of an active circuit to the design of a passive circuit.

**[0018]** Aspects of the present application relate to variable attenuator circuits for time gain compensation comprising a plurality of resistors that are individually digitally enabled. Because the circuits comprise fixed resistors, high degrees of attenuation accuracy, and consequently high degrees of gain accuracy, may be accomplished. Furthermore, the source of power consumption associated with the variable attenuator is the digital circuits enabling the resistors.

**[0019]** The aspects and embodiments described above, as well as additional aspects and embodiments, are described further below. These aspects and/or embodiments may be used individually, all together, or in any combination of two or more, as the application is not limited in this respect.

**[0020]** FIG. 1 illustrates a circuit for processing received ultrasound signals, according to a non-limiting embodiment of the present application. The circuit 100 includes  $N$  ultrasonic transducers 102a...102n, wherein  $N$  is an integer. The ultrasonic transducers are sensors in

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some embodiments, producing electrical signals representing received ultrasound signals. The ultrasonic transducers may also transmit ultrasound signals in some embodiments. The ultrasonic transducers may be capacitive micromachined ultrasonic transducers (CMUTs) in some embodiments. The ultrasonic transducers may be piezoelectric micromachined ultrasonic transducers (PMUTs) in some embodiments. Further alternative types of ultrasonic transducers may be used in other embodiments.

**[0021]** The circuit 100 further comprises  $N$  circuitry channels 104a...104n. The circuitry channels may correspond to a respective ultrasonic transducer 102a...102n. For example, there may be eight ultrasonic transducers 102a...102n and eight corresponding circuitry channels 104a...104n. In some embodiments, the number of ultrasonic transducers 102a...102n may be greater than the number of circuitry channels.

**[0022]** The circuitry channels 104a...104n may include transmit circuitry, receive circuitry, or both. The transmit circuitry may include transmit decoders 106a...106n coupled to respective pulsers 108a...108n. The pulsers 108a...108n may control the respective ultrasonic transducers 102a...102n to emit ultrasound signals.

**[0023]** The receive circuitry of the circuitry channels 104a...104n may receive the electrical signals output from respective ultrasonic transducers 102a...102n. In the illustrated example, each circuitry channel 104a...104n includes a respective receive switch 110a...110n and an amplifier 112a...112n. The receive switches 110a...110n may be controlled to activate/deactivate readout of an electrical signal from a given ultrasonic transducer 102a...102n. More generally, the receive switches 110a...110n may be receive circuits, since alternatives to a switch may be employed to perform the same function. The amplifiers 112a...112n may be trans-impedance amplifiers (TIAs).

**[0024]** The circuit 100 further comprises an averaging circuit 114, which is also referred to herein as a summer or a summing amplifier. In some embodiments, the averaging circuit 114 is a buffer or an amplifier. The averaging circuit 114 may receive output signals from one or more of the amplifiers 112a...112n and may provide an averaged output signal. The averaged output signal may be formed in part by adding or subtracting the signals from the various amplifiers 112a...112n. The averaging circuit 114 may include a variable feedback resistance. The value of the variable feedback resistance may be adjusted dynamically based upon the number of amplifiers 112a...112n from which the averaging circuit receives signals. The averaging circuit 114 is coupled to an auto-zero block 116.

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**[0025]** The auto-zero block 116 is coupled to a time gain compensation circuit 118 which includes an attenuator 120 and a fixed gain amplifier 122. Attenuator 120, as well as attenuator 200 of FIG. 2A, attenuator 220 of FIG. 2B, attenuator 240 of FIG. 2C, and attenuator 260 of FIG. 2D, may be a variable attenuator in some embodiments. As will be described further below, one or more resistors may be enabled/disabled thus adjusting the attenuation associated with the attenuator.

**[0026]** The time gain compensation circuit 118 is coupled to an ADC 126 via ADC drivers 124. In the illustrated example, the ADC drivers 124 include a first ADC driver 125a and a second ADC driver 125b. The ADC 126 digitizes the signal(s) from the averaging circuit 114.

**[0027]** While FIG. 1 illustrates a number of components as part of a circuit of an ultrasound device, it should be appreciated that the various aspects described herein are not limited to the exact components or configuration of components illustrated. For example, aspects of the present application relate to the time gain compensation circuit 118.

**[0028]** The components of FIG. 1 may be located on a single substrate or on different substrates. For example, as illustrated, the ultrasonic transducers 102a...102n may be on a first substrate 128a and the remaining illustrated components may be on a second substrate 128b. The first and/or second substrates may be semiconductor substrates, such as silicon substrates. In an alternative embodiment, the components of FIG. 1 may be on a single substrate. For example, the ultrasonic transducers 102a...102n and the illustrated circuitry may be monolithically integrated on the same semiconductor die. Such integration may be facilitated by using CMUTs as the ultrasonic transducers.

**[0029]** According to an embodiment, the components of FIG. 1 form part of an ultrasound probe. The ultrasound probe may be handheld. In some embodiments, the components of FIG. 1 form part of an ultrasound patch configured to be worn by a patient.

**[0030]** The gain of fixed gain amplifier 122 may have values between approximately 1dB and 100dB, between approximately 3dB and 30dB, between approximately 5dB and 20dB, or any other value or range of values. Other values are also possible.

**[0031]** In some embodiments fixed gain amplifier 122 has a gain of 20dB.

**[0032]** The attenuation of variable attenuator 120 may have values between approximately 1dB and 100dB, between approximately 3dB and 30dB, between approximately 5dB and 20dB, or any other value or range of values. Other values are also possible.

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**[0033]** Circuit 200, shown in FIG. 2A, represents a non-limiting embodiment of attenuator 120. Circuit 200 is arranged in a differential configuration. Circuit 200 has a differential input voltage 201 and a differential output voltage 202. Resistor 203 is associated with the “+” side of the differential circuit. On the other hand, series resistors 204 is associated with the “-“ side of the differential circuit. Resistor 203 may or may not have a resistance equal to that of resistor 204. Placed in parallel, between the output of resistors 203 and 204 and output voltage 202, are circuits 210<sub>i</sub>, where *i* may assume values between 1 and *m*. According to some embodiments, each circuit 210<sub>i</sub> comprises the series of resistor 205<sub>i</sub>, switch 206<sub>i</sub> and resistor 207<sub>i</sub>. Resistor 205<sub>i</sub> may or may not have a resistance equal to that of resistor 207<sub>i</sub>.

**[0034]** Each switch 206<sub>i</sub> may have 2 possible states: closed or open. When switch 206<sub>i</sub> is closed, circuit 210<sub>i</sub> represents a resistor having a resistance equal to the sum of resistors 205<sub>i</sub> and 207<sub>i</sub>. Contrarily, when switch 206<sub>i</sub> open, circuit 210<sub>i</sub> has a resistance equal to infinite. According to some embodiments, the overall resistance seen by the input signal may be varied by changing the state of switches 206<sub>i</sub>. In this configuration, the overall resistance may be defined by a digital code of *m* bits in length, where a bit equal to 1 represents a closed switch and a bit equal to 0 represents an open switch. Each switch 206<sub>i</sub> may assume a closed or open state, independently of the state of the other switches.

**[0035]** Resistors 203 and 204, and each resistor 205<sub>i</sub> and 207<sub>i</sub> may have values between approximately 1Ω and 10GΩ, between approximately 100Ω and 100MΩ, between approximately 1KΩ and 1MΩ, or any other value or range of values. Other values are also possible.

**[0036]** In some embodiments, resistors 205<sub>i</sub> and 207<sub>i</sub> may be chosen to progressively increase or decrease by a constant factor *x* as a function of *i*. For example, if resistor 205<sub>1</sub> is set to *R*, resistor 205<sub>2</sub> may be equal to *xR*, resistor 205<sub>3</sub> may be equal to *x<sup>2</sup>R*, and resistor 205<sub>*m*</sub> may be equal to *x<sup>m-1</sup>R*. Factor *x* may have values between approximately 0.001 and 1000, between approximately 0.1 and 10, between approximately 0.5 and 2, or any other value or range of values. Other values are also possible.

**[0037]** In some embodiments, resistors 205<sub>i</sub> are all equal to each other and resistors 207<sub>i</sub> are all equal to each other, for any value of *i*.

**[0038]** In some embodiments, a fixed attenuation stage may be obtained by closing some or all switches 206<sub>i</sub> and by setting resistors 203, 204 and each of the resistors 205<sub>i</sub> and 207<sub>i</sub> to a predefined value.

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**[0039]** Circuit 220, shown in FIG. 2B, represents another non-limiting embodiment of the attenuator 120. Circuit 220 is also arranged in a differential configuration. Circuit 220 has a differential input voltage 221 and a differential output voltage 222. Resistor 223 is associated with the “+” side of the differential circuit. On the other hand, series resistor 224 is associated with the “-“ side of the differential circuit. Resistor 223 may or may not have a resistance equal to that of resistor 224. In series to resistor 223 is the series of circuits 230<sub>i</sub> where i may assume any value between 1 and m. Similarly, in series to resistor 224 is the series of circuits 231<sub>i</sub>. Each circuit 230<sub>i</sub> comprises resistor 225<sub>i</sub> configured in parallel to switch 226<sub>i</sub> and circuit 231<sub>i</sub> comprises resistor 227<sub>i</sub> configured in parallel to switch 228<sub>i</sub>. Resistors 225<sub>i</sub> may or may not have a resistance equal to that of resistor 227<sub>i</sub>.

**[0040]** Each switch 226<sub>i</sub> and 228<sub>i</sub> may have 2 possible states: closed or open. According to some embodiments, the overall resistance seen by the input signal may be varied by independently adjusting the state of each switch 226<sub>i</sub> and 228<sub>i</sub>. As in the parallel circuit described previously, a bit sequence may be used to determine the state of each switch.

**[0041]** Resistors 223 and 224, and each resistor 225<sub>i</sub> and 227<sub>i</sub> may have values between approximately 1Ω and 10GΩ, between approximately 100Ω and 100MΩ, between approximately 1KΩ and 1MΩ, or any other value or range of values. Other values are also possible.

**[0042]** In some embodiments, resistors 225<sub>i</sub> and 227<sub>i</sub> may be chosen to progressively increase or decrease by a constant factor x as a function of i. For example, if resistor 225<sub>1</sub> is set to R, resistor 225<sub>2</sub> may be equal to xR, resistor 225<sub>3</sub> may be equal to x<sup>2</sup>R, and resistor 225<sub>m</sub> may be equal to x<sup>m-1</sup>R. Factor x may have values between approximately 0.001 and 1000, between approximately 0.1 and 10, between approximately 0.5 and 2, or any other value or range of values. Other values are also possible.

**[0043]** In some embodiments, resistors 225<sub>i</sub> are all equal to each other and resistors 227<sub>i</sub> are all equal to each other, for any value of i.

**[0044]** In some embodiments, a fixed attenuation stage may be obtained by closing some or all switches 226<sub>i</sub> and 228<sub>i</sub> and by setting resistors 223, 224 and each of the resistors 225<sub>i</sub> and 227<sub>i</sub> to a predefined value.

**[0045]** While circuit 200 represents a differential parallel embodiment of attenuator 120, circuit 220 represents a differential series embodiment of attenuator 120. As may be appreciated

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by a person of ordinary skills in the art, any suitable combination of parallel and series arrangements may be used.

**[0046]** Circuit 240, shown in FIG. 2C, represents another non-limiting embodiment of the attenuator 120. Circuit 240 is arranged in a single-ended configuration, as the – side of the circuit is connected to ground. Circuit 240 has a single-ended input voltage 241 and a single-ended output voltage 242. Circuit 240 comprises series resistor 243, and parallel circuits 250<sub>i</sub> where *i* may assume any value between 1 and *m*. Each circuit 250<sub>i</sub> comprises resistor 245<sub>i</sub> connected in series to switch 246<sub>i</sub>.

**[0047]** Each switch 246<sub>i</sub> may have 2 possible states: closed or open. According to some embodiments, the overall resistance seen by the input signal may be varied by independently adjusting the state of each switch 246<sub>i</sub>. As in the parallel circuits described previously, a bit sequence may be used to determine the state of each switch.

**[0048]** Resistors 243, and each resistor 245<sub>i</sub> may have values between approximately 1Ω and 10GΩ, between approximately 100Ω and 100MΩ, between approximately 1KΩ and 1MΩ, or any other value or range of values. Other values are also possible.

**[0049]** In some embodiments, resistors 245<sub>i</sub> may be chosen to progressively increase or decrease by a constant factor *x* as a function of *i*. For example, if resistor 245<sub>1</sub> is set to *R*, resistor 245<sub>2</sub> may be equal to *xR*, resistor 245<sub>3</sub> may be equal to *x<sup>2</sup>R*, and resistor 245<sub>m</sub> may be equal to *x<sup>m-1</sup>R*. Factor *x* may have values between approximately 0.001 and 1000, between approximately 0.1 and 10, between approximately 0.5 and 2, or any other value or range of values. Other values are also possible.

**[0050]** In some embodiments, resistors 245<sub>i</sub> are all equal to each other.

**[0051]** In some embodiments, a fixed attenuation stage may be obtained by closing each switch 246<sub>i</sub> and by setting resistors 243 and each of the resistors 245<sub>i</sub> to a predefined value, for any value of *i*.

**[0052]** Circuit 260, shown in FIG. 2D, represents another non-limiting embodiment of the attenuator 120. Circuit 260 is also arranged in a single-ended configuration. Circuit 260 has a single-ended input voltage 261 and a single-ended output voltage 262. Circuit 260 comprises series resistor 263 connected in series to circuits 270<sub>i</sub> where *i* may assume any value between 1 and *m*. Each circuit 270<sub>i</sub> comprises resistor 265<sub>i</sub> connected in parallel to switch 266<sub>i</sub>.

**[0053]** Each switch 266<sub>i</sub> may have 2 possible states: closed or open. According to some embodiments, the overall resistance seen by the input signal may be varied by independently

adjusting the state of each switch 266<sub>i</sub>. As in the parallel circuits described previously, a bit sequence may be used to determine the state of each switch.

**[0054]** Resistors 263, and each resistor 265<sub>i</sub> may have values between approximately 1Ω and 10GΩ, between approximately 100Ω and 100MΩ, between approximately 1KΩ and 1MΩ, or any other value or range of values. Other values are also possible.

**[0055]** In some embodiments, resistors 265<sub>i</sub> may be chosen to progressively increase or decrease by a constant factor x as a function of i. For example, if resistor 265<sub>1</sub> is set to R, resistor 265<sub>2</sub> may be equal to xR, resistor 265<sub>3</sub> may be equal to x<sup>2</sup>R, and resistor 265<sub>m</sub> may be equal to x<sup>m-1</sup>R. Factor x may have values between approximately 0.001 and 1000, between approximately 0.1 and 10, between approximately 0.5 and 2, or any other value or range of values. Other values are also possible.

**[0056]** In some embodiments, resistors 265<sub>i</sub> are all equal to each other.

**[0057]** According to some embodiments, a fixed attenuation stage may be obtained by closing some or all switches 266<sub>i</sub> and by setting resistors 263 and each of the resistors 265<sub>i</sub> to a predefined value, for any value of i.

**[0058]** While circuit 240 represents a single-ended parallel embodiment of attenuator 120, circuit 260 represents a single-ended series embodiment of attenuator 120. As may be appreciated by a person of ordinary skills in the art, any suitable combination of parallel and series arrangements may be used.

**[0059]** FIG. 3 shows a non-limiting embodiment of attenuator 120. While circuit 300 is presented in a differential parallel configuration, other configurations may be used. For example a differential series configuration or a single-ended parallel configuration or a single-ended series configuration or any other suitable combination thereof may be used. According to some non-limiting aspects of the present application, switched 206<sub>i</sub> may be implemented by complementary switches as shown in FIG. 3. The complementary switches may comprise a nMOS transistor 310<sub>i</sub> and a pMOS transistor 311<sub>i</sub>. The drain of nMOS transistor 310<sub>i</sub> may be connected to the source of pMOS transistor 311<sub>i</sub>. The source of nMOS transistor 310<sub>i</sub> may be connected to the drain of pMOS transistor 311<sub>i</sub>. The gate of nMOS transistor 310<sub>i</sub> may be connected to the input port of inverter 315<sub>i</sub>, whose output port may be connected to the gate of pMOS transistor 311<sub>i</sub>.

**[0060]** As may readily be appreciated by a person of ordinary skill in the art, while FIG. 3 shows complementary switches based on one pMOS transistor and one nMOS transistor, any

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suitable number of pMOS transistors and nMOS transistors may be used. In addition, a non-complementary switch using only nMOS (or only pMOS) transistors may be used.

**[0061]** As may further be appreciated by a person of ordinary skill in the art, while FIG. 3 shows complementary switches based on metal-oxide-semiconductor (MOSFET) transistors, any other type of transistors may be used. Transistors 310<sub>i</sub> and 311<sub>i</sub> may be implemented by BJT, BiCMOS, JFET, IGFET, MESFET or any other suitable type of transistor.

**[0062]** In some embodiments, flip-flops 317<sub>i</sub>, where *i* may assume any value between 1 and *m*, may be used to set the state of complementary switches 206<sub>i</sub>. The output port of each flip-flop 317<sub>i</sub> may be connected to the gate of each nMOS transistor 310<sub>i</sub>. As further described below, in some embodiments, instead of connecting the gates of the two transistors through inverters 315<sub>i</sub>, the Q port of each flip-flop 317<sub>i</sub> may be connected to the gate of each nMOS transistor 310<sub>i</sub> while the  $\overline{Q}$  (Q not) port of each flip-flop 317<sub>i</sub> may be connected to the gate of each pMOS transistor 311<sub>i</sub>. Furthermore, the output port of each flip-flop 317<sub>i</sub> may be connected to the input port of the following flip-flop 317<sub>i+1</sub>, where *i* may assume any value between 1 and *m*-1. According to some aspects of the present application, flip-flops 317<sub>i</sub> collectively represent a shift register.

**[0063]** In some embodiments, flip-flops 317<sub>i</sub> may be controlled by encoder 350. In turn, encoder 350 may be controlled by profile generator 351. According to some aspects of the present application, profile generator 351 may be a circuit that generates a target time gain compensation response and sources the control signals necessary to track the desired profile. The target time gain compensation response may be manually defined by a user, automatically defined by a computer, or defined in any other suitable manner.

**[0064]** FIG. 4 shows a non-limiting embodiment of attenuator circuit 300. While attenuator 400 comprises four attenuation stages each corresponding to one complementary switch, any other suitable number of stages may be used. According to some aspects of the present application, within circuit 400 is digital circuit 401. In the non-limiting example, digital circuit 401 comprises four 2-to-1 multiplexers 470<sub>i</sub>, a shift register 402 consisting of four flip-flops 317<sub>i</sub> (also illustrated in FIG. 3), four inverter pairs 450<sub>i</sub> and 452<sub>i</sub> and four inverter pairs 453<sub>i</sub> and 454<sub>i</sub>. At any moment in time each flip-flop 317<sub>i</sub> may be set to a 1 or 0 state through input port D<sub>i</sub>. When flip-flop 317<sub>i</sub> is triggered by shift signal 490, output port Q<sub>i</sub> is set to the same value as D<sub>i</sub>, while output port  $\overline{Q}$ <sub>i</sub> is set to the opposite value. In some embodiments flip-

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flop  $317_i$  may be triggered by a rising edge or a falling edge. In some other embodiments flip-flop  $317_i$  may be triggered by a 1 pulse or by a 0 pulse. Reset signal 492 may be used to set the state of all flip-flops to 0. Each port  $Q_i$  may be connected to the gate of each nMOS transistor  $310_i$  through an inverter pair  $450_i$  and  $451_i$ . Similarly, each port  $\overline{Q}_i$  may be connected to the gate of each pMOS transistor  $311_i$  through an inverter pair  $451_i$  and  $452_i$ . Inverter pairs may be used to prevent undesired voltage spikes from hitting the complementary switches.

**[0065]** In some embodiments, 2-to-1 multiplexers  $470_i$  may be used to set the state of each bit of shift register 402. Each multiplexer  $470_i$  may have two input ports  $A_i$  and  $B_i$  and one output port  $Z_i$ . When the value of the Inc\_Dec is set to 0,  $Z_i$  may assume the value of  $A_i$ , independently of the value of  $B_i$ . Contrarily, when the value of the Inc\_Dec is set to 1,  $Z_i$  may assume the value of  $B_i$ , independently of the value of  $A_i$ . However any other suitable logic may be used. In some embodiments, ports  $A_1$  and  $B_4$  may be set by the profile generator, while all other port  $A_i$  and  $B_i$  are set by the output  $Q$  of the neighboring flip-flop. In a non-limiting example,  $A_i$  may be set by  $Q_{i-1}$  and  $B_i$  may be set by  $Q_{i+1}$ .

**[0066]** In some embodiments, when Inc\_Dec signal 491 is set to 0 and the register is triggered by shift signal 490, the bits stored in the register may shift from the least significant flip-flop  $317_1$  to the most significant flip-flop  $317_4$ . Contrarily, when Inc\_Dec is set to 1 and the register is triggered by shift signal 490, the bits stored in the register may shift from the most significant flip-flop  $317_4$  to the least significant flip-flop  $317_1$ .

**[0067]** FIG. 5 shows a non-limiting example of operation of digital circuit 401. The top portion of the chart shows three control signals: shift signal 490, Inc\_Dec signal 491 and Reset signal 492. The bottom portion of the chart shows the state of each flip-flop of the shift register in response to the three control signals, where  $FF_i$  represents flip-flop  $317_i$  of FIG. 4. From  $T_1$  through  $T_4$ , in response to the control signal Inc\_Dec being set to 0, the register shifts bits towards  $FF_4$ . The shift occurs when the circuit is triggered by shift signal 490. From  $T_5$  through  $T_8$ , in response to the control signal Inc\_Dec being set to 1, the register shifts bits towards  $FF_1$ . While in the non-limiting example Reset is set to 0 at all times, it may be set to 1 at any time thus setting the state of each flip-flop to 0.

**[0068]** FIG. 6 shows a non-limiting example of a time-dependent response generated by the time gain compensation circuit 118, which may comprise variable attenuator 120 and fixed gain amplifier 122. Chart 600 shows three signals as a function of time. Curve 611 shows the

response received by one or more transducers 102<sub>i</sub>, obtained by sending an ultrasonic wave towards a target. The target may comprise multiple layers, causing multiple reflections having varying magnitude as a function of depth. Curve 611 shows a dip that may be caused by a multilayered target. In some embodiments, in order to obtain a clear ultrasound image it may be desirable to have a uniform response as a function of time as shown by curve 631. Consequently, profile generator 351 may source control signals so as to provide a gain response that compensates losses caused by the depth-dependent reflections. Curve 621 is a non-limiting example of such gain response.

**[0069]** In some embodiments, each binary attenuation stage can provide about 0.2 dB of attenuation.

**[0070]** In some other embodiments, it may be desirable to generate a gain response that causes the compensated signal to have any suitable time-dependent behavior. For example, in order to improve the contrast of an ultrasound image, it may be desirable to magnify the response of one layer of the target while attenuating the response of another layer. The time gain compensation response may be manually defined by the user, automatically defined by a computer, or defined in any other suitable manner.

**[0071]** Having thus described several aspects and embodiments of the technology of this application, it is to be appreciated that various alterations, modifications, and improvements will readily occur to those of ordinary skill in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the technology described in the application. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described.

**[0072]** As described, some aspects may be embodied as one or more methods. The acts performed as part of the method(s) may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

**[0073]** All definitions, as defined and used herein, should be understood to control over dictionary definitions and/or ordinary meanings of the defined terms.

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**[0074]** The phrase “and/or,” as used herein in the specification and in the claims, should be understood to mean “either or both” of the elements so conjoined, *i.e.*, elements that are conjunctively present in some cases and disjunctively present in other cases.

**[0075]** As used herein in the specification and in the claims, the phrase “at least one,” in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements.

**[0076]** As used herein, the term “between” used in a numerical context is to be inclusive unless indicated otherwise. For example, “between A and B” includes A and B unless indicated otherwise.

**[0077]** In the claims, as well as in the specification above, all transitional phrases such as “comprising,” “including,” “carrying,” “having,” “containing,” “involving,” “holding,” “composed of,” and the like are to be understood to be open-ended, *i.e.*, to mean including but not limited to. Only the transitional phrases “consisting of” and “consisting essentially of” shall be closed or semi-closed transitional phrases, respectively.

CLAIMS:

1. An ultrasound device, comprising:
  - a profile generator;
  - an encoder configured to receive a profile signal from the profile generator;
  - an attenuator configured to receive an input signal representing an output of an ultrasound sensor and coupled to the encoder to receive a control signal from the encoder, the attenuator comprising a plurality of binary attenuator stages, the attenuator configured to produce an output signal that is an attenuated version of the input signal; and
  - a fixed gain amplifier having a gain greater than 0 dB and configured to receive the output signal from the attenuator and amplify the output signal.
2. The ultrasound device of claim 1, wherein the profile generator provides a target attenuation profile.
3. The ultrasound device of claim 1, wherein each of the plurality of binary attenuation stages provides about 0.2 dB of attenuation.
4. The ultrasound device of claim 1, wherein each of the plurality of binary attenuation stages comprises at least one complementary switch.
5. The ultrasound device of claim 1, wherein each of the plurality of binary attenuation stages is single-ended.
6. The ultrasound device of claim 1, wherein each of the plurality of binary attenuation stages is differential.
7. The ultrasound device of claim 1, wherein the plurality of binary attenuation stages are connected in parallel to form the attenuator.

8. The ultrasound device of claim 1, wherein the plurality of binary attenuation stages are connected in series to form the attenuator.

9. The ultrasound device of claim 1, wherein the plurality of binary attenuation stages are connected in series and parallel to form the attenuator.

10. An ultrasound device, comprising:

a profile generator;

an encoder configured to receive a profile from the profile generator;

an attenuator configured to receive an input signal representing an output of an ultrasound sensor and coupled to the encoder to receive a control signal from the encoder, the attenuator comprising a plurality of stages, each stage in the plurality of stages having a predetermined attenuation, the attenuator configured to produce an attenuated output signal that is an attenuated version of the input signal; and

a fixed gain amplifier having a gain greater than 0 dB and configured to receive the output signal from the attenuator and amplify the output signal.

11. The ultrasound device of claim 10, wherein the profile generator provides a target attenuation profile.

12. The ultrasound device of claim 10, wherein each of the plurality of stages provides about 0.2 dB of attenuation.

13. The ultrasound device of claim 10, wherein each of the plurality of stages comprises at least one complementary switch.

14. The ultrasound device of claim 10, wherein each of the plurality of stages is single-ended.

15. The ultrasound device of claim 10, wherein each of the plurality of stages is differential.

16. The ultrasound device of claim 10, wherein the plurality of stages are connected in parallel to form the attenuator.
17. The ultrasound device of claim 10, wherein the plurality of stages are connected in series to form the attenuator.
18. The ultrasound device of claim 10, wherein the plurality of stages are connected in series and parallel to form the attenuator.
19. The ultrasound device of claim 1, wherein the fixed gain amplifier has a gain between approximately 1 dB and 100 dB.
20. The ultrasound device of claim 1, wherein the attenuator and the fixed gain amplifier are configured to perform time-gain compensation on the input signal.
21. The ultrasound device of claim 10, wherein the fixed gain amplifier has a gain between approximately 1 dB and 100 dB.
22. The ultrasound device of claim 10, wherein the attenuator and the fixed gain amplifier are configured to perform time-gain compensation on the input signal.

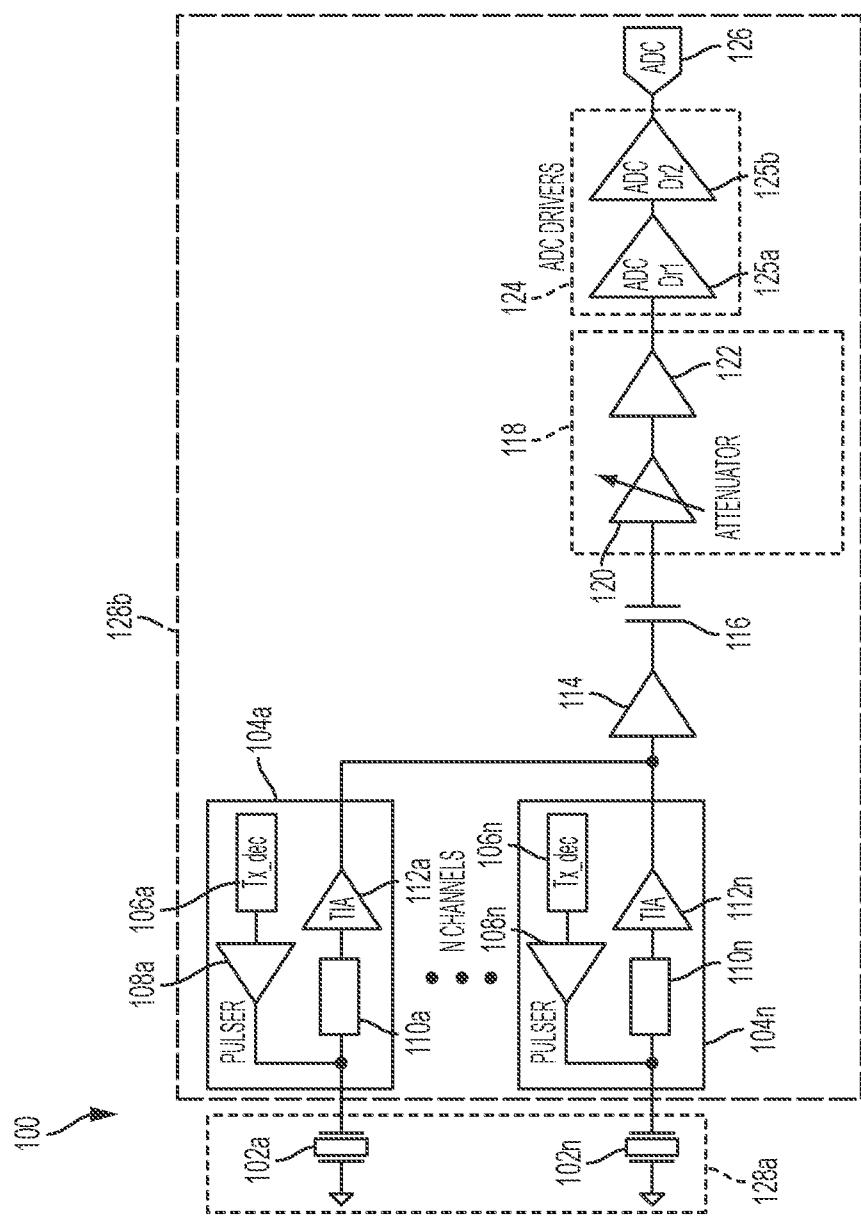


FIG. 1

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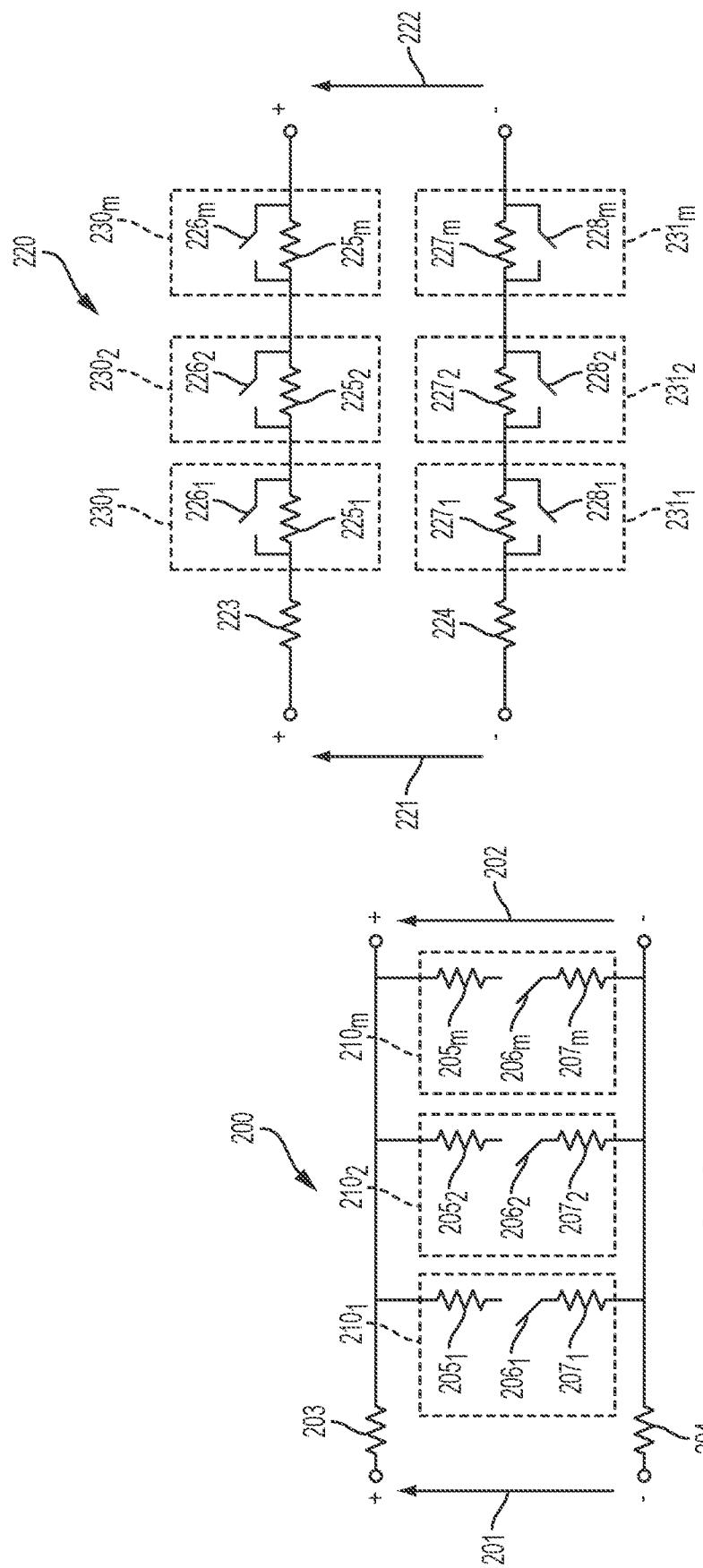


FIG. 2A

FIG. 2B

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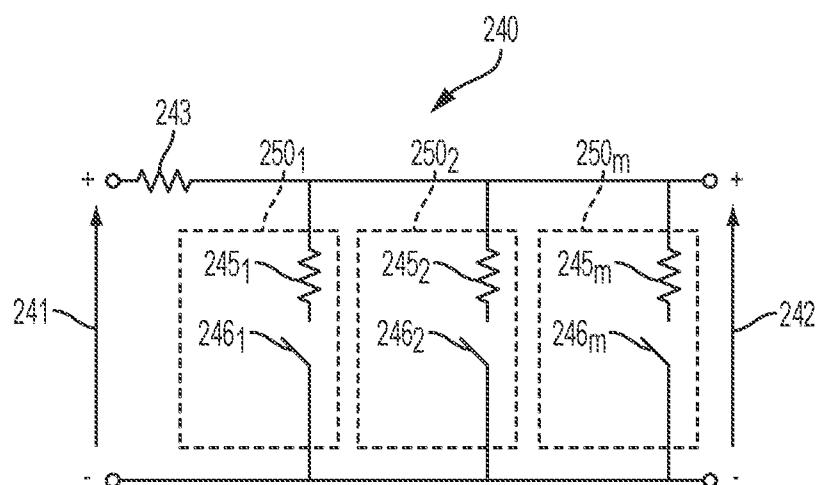


FIG. 2C

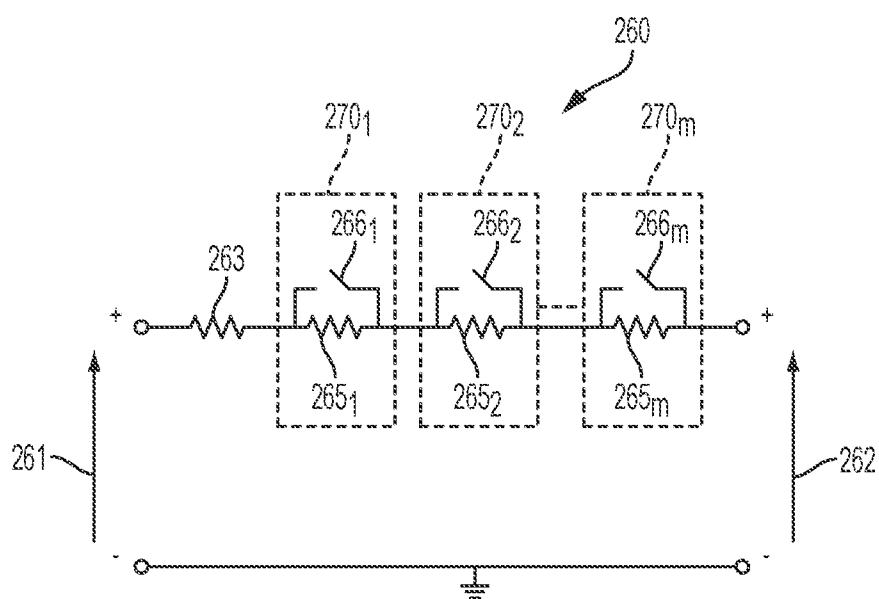


FIG. 2D

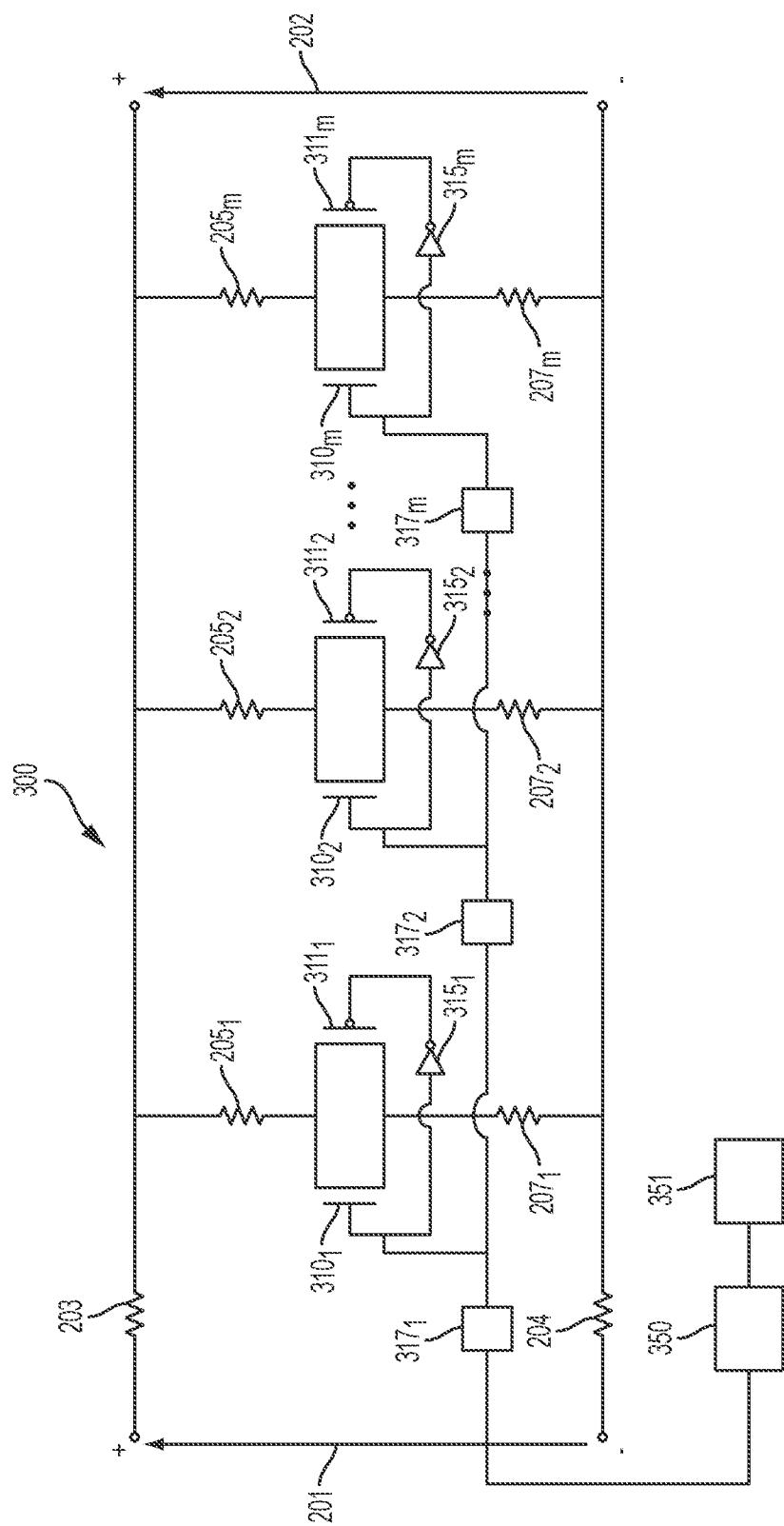


FIG. 3

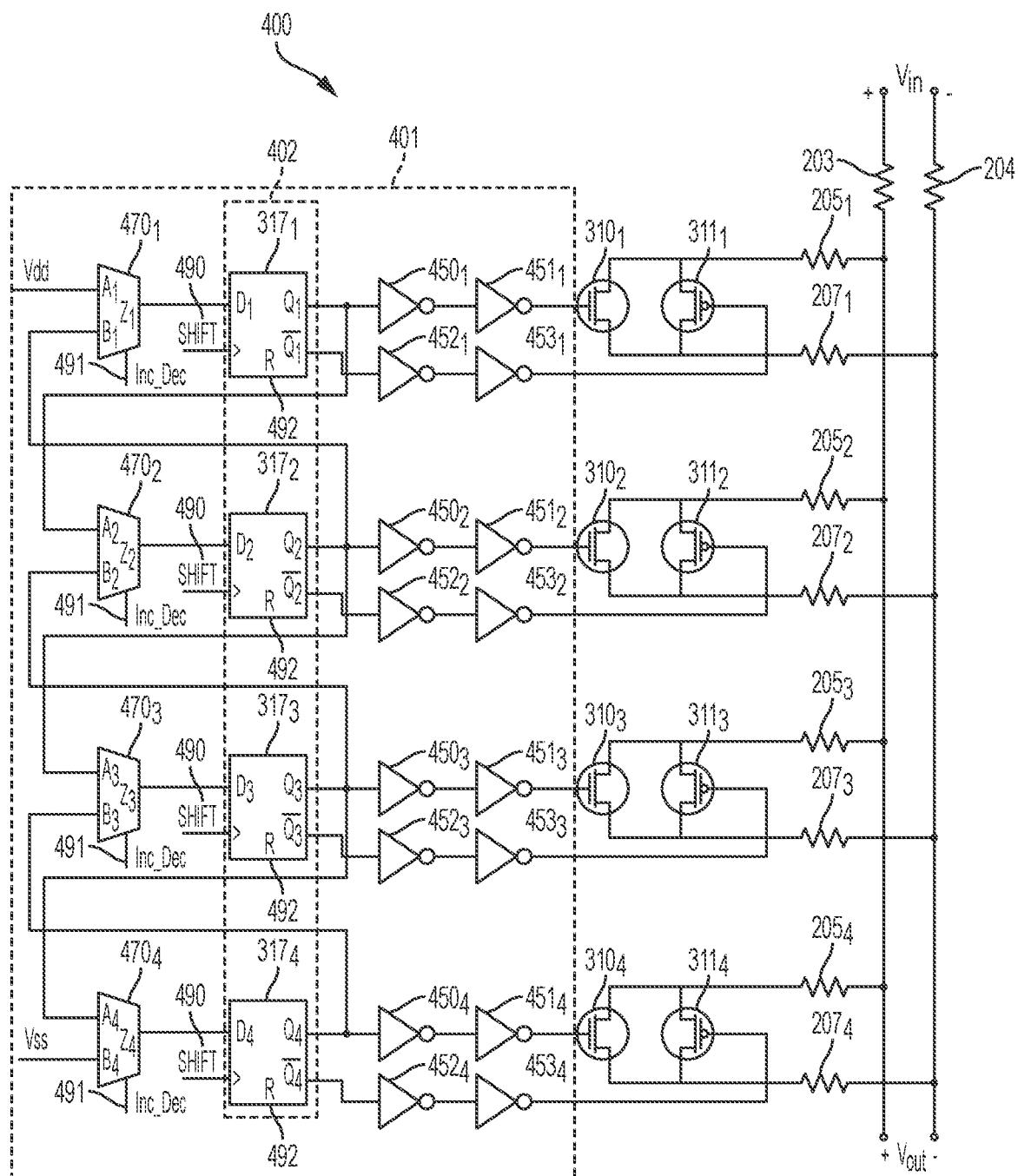


FIG. 4

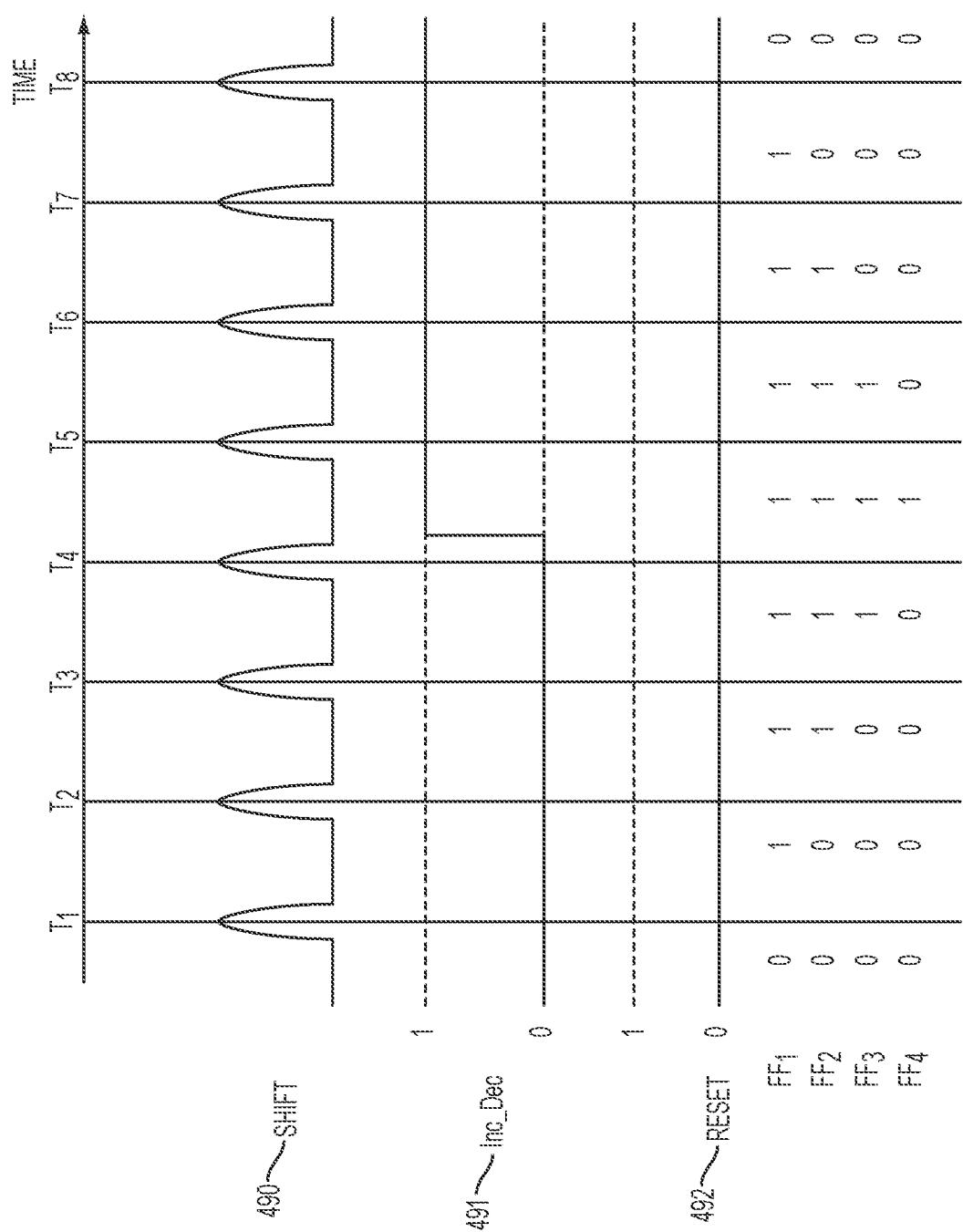


FIG. 5

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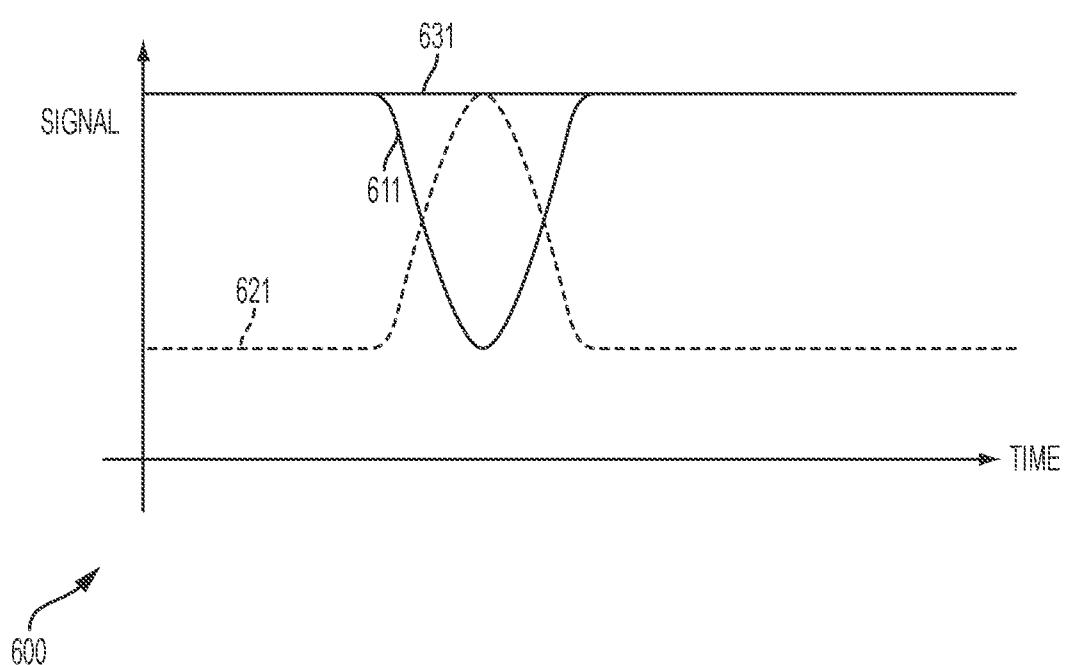


FIG. 6

