(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 December 2010 (29.12.2010)

PCT

(10) International Publication Number
WO 2010/151375 A1

(51) International Patent Classification:
H01L 23/12 (2006.01) *H01L 23/48* (2006.01)

(21) International Application Number:
PCT/US2010/033536

(22) International Filing Date:
4 May 2010 (04.05.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/459,226 26 June 2009 (26.06.2009) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) **Title**: STACKED-CHIP PACKAGES IN PACKAGE-ON-PACKAGE APPARATUS, METHODS OF ASSEMBLING SAME, AND SYSTEMS CONTAINING SAME

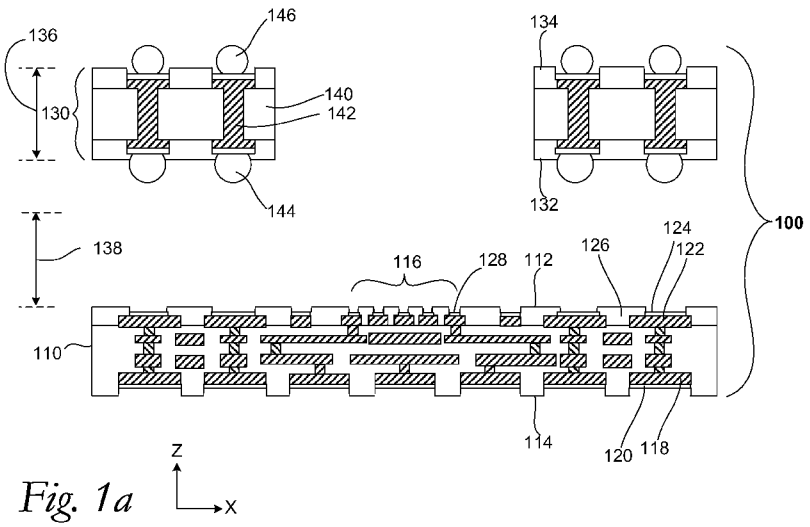


Fig. 1a

(57) **Abstract**: A stacked-chip apparatus includes a package substrate and an interposer with a chip stack disposed with a standoff that matches the interposer. A package-on-package stacked-chip apparatus includes a top package disposed on the interposer.

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STACKED-CHIP PACKAGES IN PACKAGE-ON-PACKAGE APPARATUS, METHODS OF ASSEMBLING SAME, AND SYSTEMS CONTAINING SAME

TECHNICAL FIELD

Disclosed embodiments relate to semiconductor microelectronic devices and processes of packaging them.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to understand the manner in which embodiments are obtained, a more particular description of various embodiments briefly described above will be rendered by reference to the appended drawings. These drawings depict embodiments that are not necessarily drawn to scale and are not to be considered to be limiting in scope. Some embodiments will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

FIG. 1a is a cross-section elevation of a mounting substrate and interposer apparatus for a stacked-die package according to an example embodiment;

FIG. 1b is a cross-section elevation of the apparatus depicted in FIG. 1a after further processing according to an embodiment;

FIG. 1c is a cross-section elevation of the apparatus depicted in FIG. 1b after further processing according to an embodiment;

FIG. 1d is a cross-section elevation of the apparatus depicted in FIG. 1c after further processing according to an embodiment;

FIG. 1e is a cross-section elevation of a package-on-package stacked chip apparatus that has been assembled with the apparatus depicted in FIG. 1d after further processing according to an example embodiment;

FIG. 2a is a cross-section elevation of a mounting substrate and interposer apparatus for a stacked-die package according to an example embodiment;

FIG. 2b is a cross-section elevation of a package-on-package stacked-chip apparatus that has assembled from the apparatus depicted in FIG. 2a after further processing according to an example embodiment;

FIG. 3a is a cross-section elevation of a mixed-die apparatus during processing according to an example embodiment;

FIG. 3b is a cross-section elevation of the apparatus depicted in FIG. 3a after further processing according to an embodiment;

FIG. 4 is a cross-section elevation of an interposer apparatus for a stacked-die package according to an example embodiment;

FIG. 5 is a cross-section elevation of a mixed-die apparatus that will support a package-on-package apparatus according to an embodiment;

FIG. 6 is a cross-section elevation of a mixed-die apparatus that will support a package-on-package mixed-die apparatus according to an embodiment;

FIG. 7 is a cross-section elevation of a mixed-die apparatus that will support a package-on-package apparatus according to an embodiment;

FIG. 8 is a process and method flow diagram according to an example embodiment; and

FIG. 9 is a schematic of a computer system according to an embodiment.

DETAILED DESCRIPTION

Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments most clearly, the drawings included herein are diagrammatic representations of integrated circuit structures. Thus, the actual appearance of the fabricated structures, for example in a photomicrograph, may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may only show the structures necessary to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings. Although a processor chip and a memory chip may be mentioned in the same sentence, it should not be construed that they are equivalent structures.

Reference throughout this disclosure to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with which the embodiment is included in at least one embodiment of the present invention. The appearance of the phrases "in one embodiment" or "in an embodiment" in various places throughout this disclosure are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

Terms such as “upper” and “lower” may be understood by reference to the X-Z or Y-Z coordinates, and terms such as “adjacent” may be understood by reference to the illustrated X-Y coordinates.

FIG. 1a is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The "board" may be an external- or near-external structure for a hand-held device such as a wireless communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.

The package substrate 110 includes a land-side ball-grid array, one ball pad of which is indicated with reference numeral 118. In an embodiment, the ball pad 118 includes a surface finish 120. The surface finish 120 is configured to be a less electronegative metal than the ball pad 118. The surface finish 120 is formed by electroplating according to an embodiment. Alternatively, the surface finish 120 is formed by electroless plating.

In an example embodiment, the ball pad 118 is copper and the surface finish 120 is a nickel-palladium-gold alloy plated onto the copper. In an embodiment, the surface finish 120 is a nickel-gold alloy plated onto the copper. In an embodiment, the surface finish 120 is copper-gold plated onto the copper.

In an example embodiment, the ball pad 118 is copper and the surface finish 120 is an organic solderability preservative (OSP) composition such as aryl-phenylimidazole. In an example embodiment, the surface finish 120 has a thickness from 1,000 Å to 2,000 Å and is aryl-phenylimidazole.

Similarly, the package substrate 110 includes a die-side ball-grid array, one ball pad of which is indicated with reference numeral 122 and the ball pad 122 includes a surface finish 124. The ball pad 122 and surface finish 124 may be an embodiment similar to those found on the board side 114. In an embodiment, the die-side ball-grid array 122 is defined by a solder resist 126. Similarly, the solder resist 126 may define die-bump pads found within the bottom chip footprint 116, and one of which is indicated with reference numeral 128. The package substrate 110 is depicted between the die side 112 and the land side 114 with interconnect and interlayer dielectric structures that are illustrative but not limiting.

The apparatus 100 is assembled with the interposer 130 that mates to the die-side ball grid array 122. The interposer 130 includes a die side 132 and a top side 134 and has an offset height 136 configured to match an offset height 138 above the package substrate 110 for a multiple die stack (MDS) that will occupy the bottom-chip footprint 116. The interposer 130 may include a core 140 and interconnects 142. In an embodiment, die-side electrical bumps 144 and top-side electrical bumps 146 are coupled to the interconnects 142.

FIG. 1b is a cross-section elevation of the apparatus depicted in FIG. 1a after further processing according to an embodiment. The apparatus 101 illustrates that the interposer offset height 136 matches the package-substrate offset height 138 (FIG. 1a). The bottom-chip footprint 116 is surrounded by the interposer 130 and will surround the multiple-die stack that is to be assembled as part of the apparatus 101.

FIG. 1c is a cross-section elevation of the apparatus depicted in FIG. 1b after further processing according to an embodiment. The apparatus 102 has been fortified with an interposer fill material 148 that stabilizes bonding between the package substrate 110 and the interposer 130.

A bottom chip 150 is placed within the bottom-chip footprint 116 (FIG. 1b). In an embodiment, the bottom chip 150 is a flip chip 150 that has been flip-chip bonded though a chip ball array, one electrical bump of which is referenced with numeral 152. In an embodiment, an underfill 154 has been flowed to fortify bonding between the bottom chip 150 and the package substrate 110. In a processing embodiment, reflow of the electrical bumps 152 is carried our during simultaneous curing of the underfill 154. In a processing embodiment, reflow of the electrical bumps 152 is carried our during simultaneous curing of the fill material 148.

In an embodiment, the bottom chip 150 is processed to reflow the electrical bumps 152, followed by placement of the underfill 154 after bump reflow.

FIG. 1d is a cross-section elevation of the apparatus depicted in FIG. 1c after further processing according to an embodiment. The apparatus 102 depicted in FIG. 1c has been further processed to achieve a mixed-die apparatus 103 that will become part of a package-on-package (PoP) stacked chip apparatus. The mixed-die apparatus 103 includes an inter-die adhesive 156 that has been formed on the bottom chip 150, and a top chip 158 has been mounted on the adhesive 156. The top chip 158 is supported by the bottom chip 150. Hereinafter, a chip stack that originates with a bottom chip (e.g. chip 150) disposed

on the package substrate 110 and that terminates with a subsequent chip (e.g. chip 158) may also be referred to as a 3-dimensional (3D) chip stack.

In an embodiment, the top chip 158 is coupled to the package substrate 110 by wire bonds, one of which is indicated by reference numeral 160. Consequently, the mixed-stack apparatus 103 includes a flip chip 150 mounted on the package substrate 110 and a wire-bond chip 158 disposed above the flip chip 150. The offset height 136 of the interposer 130 therefore accommodates the height of the mixed-stack that includes the wire bonds 160 as well as the top chip 158 the adhesive 156, the bottom chip 150, and the offset created by the electrical bumps 152 (seen in FIG. 1c).

In a process embodiment, a stack encapsulation 162 has been filled to isolate the mixed-die stack and to further prevent the bond wires 160 from moving. The stack encapsulation 162 may be used also to protect the mixed-die stack from environmental and handling dangers. The stack encapsulation 162 may also be used to facilitate heat transfer away from the mixed-die stack. In an embodiment, no stack encapsulation is used.

In an embodiment, the bottom chip 150 is a processor and the top chip 158 is a radio-frequency (RF) device. The mixed-die stack may be used in a wireless communicator (e.g. a cellular telephone) such as a smart phone.

FIG. 1e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.

In an embodiment, a top-package fill material 172 stabilizes bonding between the interposer 130 and the top package164.

It can be seen that the mixed stack of the bottom chip 150 and top chip 158 have been accommodated by the interposer offset 136 such that the top package 164 does not interfere with the mixed stack. Consequently, the PoP stacked-chip apparatus is assembled with sufficient interposer offset 136 to accommodate an offset height of the chip stack that may vary depending upon a specific application.

FIG. 2a is a cross-section elevation of a mounting substrate and interposer apparatus 200 for a stacked-die package according to an example embodiment. The apparatus 200 is similar to the apparatus 103 depicted in FIG. 1d and has been processed similarly by seating an interposer 230 upon a package substrate 210.

A stacked-chip apparatus 200 is depicted. The stacked-chip apparatus 200 includes a bottom chip 250 and a top chip 258. In an embodiment, the bottom chip 250 is a processor and the top chip 258 is a memory die that is coupled by through-silicon via (TSV) technology. A single TSV 274 is detailed within the dashed circle. In an embodiment, the top chip 258 is a level-2 (L2) memory cache (where L0 and L1 are within the processor 250) such as a static random-access memory (SRAM) for the processor 250. The bottom chip 250 and the top chip 258 are a 3D

Consequently, the stacked-chip apparatus 200 includes the flip chip 250 mounted on the package substrate 210 and the TSV-coupled chip 258 disposed above the flip chip 250. The offset height 236 of the interposer 230 therefore accommodates the height of the stacked-chip configuration. Processing of the bottom chip 250 may be done by any embodiment disclosed with respect to the bottom chip 150 depicted in FIG. 1c and elsewhere.

In an embodiment, the top chip 258 is a memory die such as a random-access memory (RAM) die 258. In an embodiment, the top chip 258 is a memory die such as a dynamic random-access memory (DRAM) die 258. In an embodiment, the top chip 258 is a memory die such as a static random-access memory (SRAM) die 258. In an embodiment, the top chip 258 is a memory die such as a erasable programmable memory (EPROM) die 258. Other memory die configurations may be used according to a specific application.

In an embodiment, the top chip 258 includes a radio-frequency device (RF) tag. In an embodiment, the top chip 258 includes a radio-frequency device for wireless communication.

In a process embodiment, a stack encapsulation 262 has been filled to isolate the chip stack. The stack encapsulation 262 may be used also to protect the chip stack from environmental and handling dangers. The stack encapsulation 262 may also be used to facilitate heat transfer away from the chip stack. In an embodiment, no stack encapsulation is used.

FIG. 2b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset 236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2a is provided to accommodate a top package 264 such as for a smart phone.

It can be seen that the chip stack of the bottom chip 250 and top chip 258 have been accommodated by the interposer offset 236 such that the top package 264 does not interfere with the chip stack.

Details illustrated and described with respect to FIG. 1e may also be inferred by observing similar structures and spaces depicted in FIG. 2b where appropriate.

It can now be understood that processing to achieve the PoP stacked-chip apparatus 201 may be similar to processing to achieve the PoP stacked-chip apparatus 104 depicted in FIG. 1e.

In an example embodiment, I/O density between the bottom chip 150 and the top chip 158 is in a range between 128 bits per die (such as when the top chip 258 is a DRAM die) and 252 bits/die. In an example embodiment, I/O speed between the processor 250 and the subsequent chip 258 is between 10 Gb/s and 1 Tb/s (tera bits per second). Along a 10 mm edge section of the subsequent chip 250 as a DRAM device, total bandwidth is from 160 GB/s to 320 GB/s. As a package, the PoP apparatus 201 has a total package bandwidth between 640 GB/s to 6400 GB/s according to an embodiment, where the processor 250 and the subsequent chip 258 each may operate at or above 256 bits. The I/O speed may run slower below 10 Gb/s (such as below 7 Gb/s) where a given application may be useful at this range.

FIG. 3a is a cross-section elevation of a mixed-die apparatus 300 during processing according to an example embodiment. A bottom chip 350 is placed on a package substrate 310 that may be similar to the package substrate 110 depicted in FIG. 1c. In an embodiment, the bottom chip 350 is a flip chip 350 that has been flip-chip bonded though a chip ball array, one electrical bump of which is referenced with numeral 352. In an embodiment, an underfill 354 has been flowed to fortify bonding between the bottom chip 350 and the package substrate 310. In a processing embodiment, reflow of the electrical bumps 352 is carried our during simultaneous curing of the underfill 354.

Processing of the bottom chip 350 may be done by any embodiment disclosed with respect to the bottom chips 150, 250, and elsewhere depicted in this disclosure.

FIG. 3b is a cross-section elevation of the apparatus depicted in FIG. 3a after further processing according to an embodiment. The apparatus 301 depicted in FIG. 3b has been further processed to achieve a mixed-stack apparatus 301 that will be part of a PoP stacked-chip apparatus. The mixed-stack apparatus 301 includes an inter-die adhesive 356 that has been formed on the bottom chip 350, and a top chip 358 has been mounted on the adhesive 356. The top chip 358 is supported by the bottom chip 350.

In an embodiment, the top chip 358 is coupled to the package substrate 310 by wire bonds, one of which is indicated by reference numeral 360. Consequently, the mixed-stack apparatus 301 includes a flip chip 350 mounted on the package substrate 310 and a wire-bond chip 358 disposed above the flip chip 350. An offset height 336 will be matched by the offset height of an interposer in further processing. It will now be clear that assembly of the mixed-stack precedes assembly of an interposer to the package substrate 310.

Similar to the mixed-die stack apparatus embodiment depicted in FIG. 1d, the interposer to be assembled will accommodate the height of the mixed-die stack that includes the wire bonds 360 as well as the top chip 358 the adhesive 356, the bottom chip 350 and the offset created by the electrical bumps 352. In an embodiment, no stack encapsulation is used.

In an embodiment, the bottom chip 350 is a processor and the top chip 358 is a RF device. The mixed-die stack may be used in a wireless communicator such as a smart phone. Details illustrated and described with respect to previously disclosed embodiments may also be inferred by observing similar structures and spaces depicted in FIG. 3b where appropriate. Additionally, previously disclosed I/O- and bandwidth capabilities may be

inferred with respect to the PoP stacked-chip embodiments depicted and described in FIG. 3b.

FIG. 4 is a cross-section elevation of an interposer apparatus 400 for a stacked-die package according to an example embodiment. The apparatus 400 is similar to the apparatus 200 depicted in FIG. 2a except assembly of an interposer is carried out after assembly of the stacked dice 450 and 458.

A stacked-chip apparatus 400 is depicted. The stacked-chip apparatus 400 includes a bottom chip 450 and a top chip 458. In an embodiment, the bottom chip 450 is a processor and the top chip 458 is a memory die that is coupled by through-silicon via (TSV) technology. A single TSV 474 is detailed within the dashed circle. In an embodiment, the top chip 558 is a level-2 (L2) memory cache (where L0 and L1 are within the processor 450) such as a static random-access memory (SRAM) for the processor 450. Processing of the bottom chip 450 may be done by any embodiment disclosed with respect to the bottom chips 150, 250, 350, and elsewhere depicted in this disclosure.

Consequently, the stacked-chip apparatus 400 includes the flip chip 450 mounted on the package substrate 410 and the TSV-coupled chip 458 disposed above the flip chip 450. The offset height 436 of the stacked chips 450 and 458 will be matched by an interposer that will be assembled. The interposer will therefore accommodate the height of the stacked-chip configuration.

In an embodiment, the top chip 458 is a memory die such as a random-access memory (RAM) die 458. In an embodiment, the top chip 458 is a memory die such as a dynamic random-access memory (DRAM) die 458. In an embodiment, the top chip 458 is a memory die such as a static random-access memory (SRAM) die 458. In an embodiment, the top chip 458 is a memory die such as a erasable programmable memory (EPROM) die 458. Other memory die configurations may be used according to a specific application.

In an embodiment, the top chip 458 includes a radio-frequency device(RF) tag. In an embodiment, the top chip 458 includes a radio-frequency device for wireless communication. In a process embodiment, a stack encapsulation will be filled into the recess the interposer will form around the chip stack.

Details illustrated and described with respect to previously disclosed embodiments may also be inferred by observing similar structures and spaces depicted in 4 where

appropriate. Additionally, previously disclosed I/O- and bandwidth capabilities may be inferred with respect to the PoP stacked-chip embodiments depicted and described in FIG. 4.

FIG. 5 is a cross-section elevation of a mixed-die apparatus 500 that will support a package-on-package apparatus according to an embodiment. The mixed-die apparatus 500 includes a bottom chip 550, a top chip 558, and an intermediate chip 551. The top chip 558 and the intermediate chip 551 are supported by the bottom chip 550. The bottom chip 550 is a flip chip that may be referred to as a first chip, the intermediate chip 551 is a TSV-coupled chip that may be referred to as a second chip 551, and the top chip 558 is a wire-bonded chip that may be referred to as a subsequent chip 558. In an embodiment, the number of TSV-coupled chips disposed immediately above the bottom chip 550 is in a range from 2 to 8, followed by the top chip 556. Processing of the bottom chip 550 may be done by any embodiment disclosed with respect to the bottom chips depicted in this disclosure.

In an embodiment, the top chip 558 is coupled to the package substrate 510 by wire bonds, one of which is indicated by reference numeral 560. The offset height 536 of the interposer 530 therefore accommodates the height of the mixed-die stack that includes the wire bonds 560 as well as the top chip 558, the intermediate chip 551, the bottom chip 550, and the offset created by the electrical bumps and inter-chip adhesives and spacers as illustrated.

In a process embodiment, a stack encapsulation 562 has been filled to isolate the mixed-die stack and to further prevent the bond wires 560 from moving. The stack encapsulation 562 may be used also to protect the mixed-die stack from environmental and handling dangers. The stack encapsulation 562 may also be used to facilitate heat transfer away from the mixed-die stack. In an embodiment, no stack encapsulation is used.

In an embodiment, the first chip 550 is a processor, the intermediate chip 551 is a TSV RAM chip, and the top chip 558 is an RF device. The mixed-die stack may be used in a wireless communicator such as a smart phone.

Details illustrated and described with respect to previously disclosed embodiments may also be inferred by observing similar structures and spaces depicted in FIG. 5 where appropriate. Additionally, previously disclosed I/O- and bandwidth capabilities may be inferred with respect to the PoP stacked-chip embodiments depicted and described in FIG. 5.

FIG. 6 is a cross-section elevation of a mixed-die apparatus 600 that will support a PoP mixed-die apparatus according to an embodiment. The mixed-die apparatus 600 includes a bottom chip 650, a top chip 659, and several intermediate chips 651, 653, and 658. The top chip 659 and the intermediate chips 651, 653, and 658 are supported by the bottom chip 650. Processing of the bottom chip 650 may be done by any embodiment disclosed with respect to the bottom chips depicted in this disclosure.

The mixed-die apparatus 600 is an embodiment with multiple TSV chips and multiple wire-bond chips. The bottom chip 650 is a flip chip that may be referred to as a first chip. The intermediate chip 651 is a TSV-coupled chip that may be referred to as a second chip 651. The intermediate chip 653 is a TSV-coupled chip that may be referred to as a third chip 653. The intermediate chip 658 is a wire-bonded chip that may be referred to as a fourth chip 658. And the top chip 659 is a wire-bonded chip that may be referred to as a subsequent chip 659. In an embodiment, the number of TSV-coupled chips disposed immediately above the bottom chip 550 and below the wire-bond chip 658 is in a range from 2 to 8.

In an embodiment, both the wire-bond chip 658 and the wire-bond chip 559 are coupled to the package substrate 610 by wire bonds 660 and 661, respectively. The offset height 636 of the interposer 630 therefore accommodates the height of the mixed-die stack that includes the wire bonds 660 and 661 as well the entire chip stack and electrical bumps and inter-chip adhesives and spacers as illustrated.

In a process embodiment, a stack encapsulation 662 has been filled to isolate the mixed-die stack and to further prevent the bond wires 660 and 661 from moving. The stack encapsulation 662 may be used also to protect the mixed-die stack from environmental and handling dangers. The stack encapsulation 662 may also be used to facilitate heat transfer away from the mixed-die stack. In an embodiment, no stack encapsulation is used.

Details illustrated and described with respect to previously disclosed embodiments may also be inferred by observing similar structures and spaces depicted in FIG. 6 where appropriate. Additionally, previously disclosed I/O- and bandwidth capabilities may be inferred with respect to the PoP stacked-chip embodiments depicted and described in FIG. 6.

FIG. 7 is a cross-section elevation of a mixed-die apparatus 700 that will support a package-on-package apparatus according to an embodiment. The mixed-die apparatus 700

includes a bottom chip 750, a top chip 759, and several intermediate chips 751, 753, and 758. The top chip 759 and the intermediate chips 751, 753, and 758 are supported by the bottom chip 750. The mixed-die apparatus 700 is an embodiment with multiple TSV chips and multiple wire-bond chips where a wire-bond chip is below a TSV chip.

The bottom chip 750 is a flip chip that may be referred to as a first chip. The intermediate chip 751 is a TSV-coupled chip that may be referred to as a second chip 751. The intermediate chip 758 is a wire-bonded chip that may be referred to as a third chip 758. The intermediate chip 753 is a TSV-coupled chip that may be referred to as a fourth chip 753. And the top chip 759 is a wire-bonded chip that may be referred to as a subsequent chip 759. In an embodiment, the second chip 751 is a memory cache chip that supports the bottom chip 750. Processing of the bottom chip 750 may be done by any embodiment disclosed with respect to the bottom chips depicted in this disclosure.

In an embodiment, the fourth chip 753 is a TSV memory cache chip the supports the subsequent chip 759. In an example embodiment, the mixed-die apparatus 700 is part of a PoP stacked-chip apparatus such as a super-smart phone. The bottom chip 750 in this embodiment is a processor and the second chip 751 is a memory cache. The intermediate chip 758 is a wire-bonded device for processing online communications. The top chip 759 is a global-positioning system (GPS) chip that is supported by the fourth chip 753, which acts as a cache for the GPS chip 759. Further in an example embodiment, a top package

In an embodiment, the fourth chip 753 is used as a support and interface between the intermediate chip 758 and the top chip 759. For example, the fourth chip 753 has a TSV that allows direct communication between the top chip 759 and the intermediate chip 758. .

In an embodiment, both the wire-bond chip 758 and the wire-bond chip 759 are coupled to the package substrate 710 by wire bonds 760 and 761, respectively. The offset height 736 of the interposer 730 therefore accommodates the height of the mixed-die stack that includes the wire bonds 760 and 761 as well the entire chip stack and electrical bumps and inter-chip adhesives and spacers as illustrated.

In a process embodiment, a stack encapsulation 762 has been filled to isolate the mixed-die stack and to further prevent the bond wires 760 and 761 from moving. The stack encapsulation 662 may be used also to protect the mixed-die stack from environmental and handling dangers. The stack encapsulation 762 may also be used to

facilitate heat transfer away from the mixed-die stack. In an embodiment, no stack encapsulation is used.

Details illustrated and described with respect to previously disclosed embodiments may also be inferred by observing similar structures and spaces depicted in FIG. 6 where appropriate. Additionally, previously disclosed I/O- and bandwidth capabilities may be inferred with respect to the PoP stacked-chip embodiments depicted and described in FIG. 6.

FIG. 8 is a process and method flow diagram 800 according to an example embodiment.

At 810, a process includes forming an interposer on a package substrate. The interposer is configured to have an offset that will match a chip stack to be placed on the package substrate.

At 820, the process includes forming a chip stack on the package substrate. Where process 820 precedes process 810, the interposer is placed on the package substrate after forming the chip stack. Where process 820 follows process 810, the chip stack is formed within a recess left by the interposer. In an embodiment, the process commences at 810 and terminates at 820.

At 830, the process includes filling a stack encapsulation to isolate the chip stack. In an embodiment, the process commences at 810 and terminates at 830.

At 840 the process includes forming a top package on the interposer. In an embodiment, the process commences and terminates at 840.

FIG. 9 is a schematic of a computer system 900 according to an embodiment. The computer system 900 (also referred to as the electronic system 900) as depicted can embody a PoP stacked-chip apparatus according to any of the several disclosed embodiments and their equivalents as set forth in this disclosure. In an embodiment, the electronic system 900 is a computer system that includes a system bus 920 to electrically couple the various components of the electronic system 900. The system bus 920 is a single bus or any combination of busses according to various embodiments. The electronic system 900 includes a voltage source 930 that provides power to the integrated circuit 910. In some embodiments, the voltage source 930 supplies current to the integrated circuit 910 through the system bus 920.

The integrated circuit 910 is electrically coupled to the system bus 920 and includes any circuit, or combination of circuits according to an embodiment. In an

embodiment, the integrated circuit 910 includes a processor 912 that can be of any type. As used herein, the processor 912 may mean any type of circuit such as, but not limited to, a microprocessor, a microcontroller, a graphics processor, a digital signal processor, or another processor. In an embodiment, SRAM embodiments are found in memory caches of the processor. Other types of circuits that can be included in the integrated circuit 910 are a custom circuit or an application-specific integrated circuit (ASIC), such as a communications circuit 914 for use in wireless devices such as cellular telephones, pagers, portable computers, two-way radios, and similar electronic systems. In an embodiment, the processor 910 includes on-die memory 916 such as static random-access memory (SRAM) and the SRAM may include a 6T SRAM cell with independent S/D sections of the access and pull-down regions. In an embodiment, the processor 910 includes embedded on-die memory 916 such as embedded dynamic random-access memory (eDRAM).

In an embodiment, the electronic system 900 also includes an external memory 940 that in turn may include one or more memory elements suitable to the particular application, such as a main memory 942 in the form of RAM, one or more hard drives 944, and/or one or more drives that handle removable media 946, such as diskettes, compact disks (CDs), digital variable disks (DVDs), flash memory drives, and other removable media known in the art. The external memory 940 may also be embedded memory 948 such as the microelectronic die embedded in a processor mounting substrate according to an embodiment.

In an embodiment, the electronic system 900 also includes a display device 950, an audio output 960. In an embodiment, the electronic system 900 includes an input device such as a controller 970 that may be a keyboard, mouse, trackball, game controller, microphone, voice-recognition device, or any other input device that inputs information into the electronic system 900.

As shown herein, the integrated circuit 910 can be implemented in a number of different embodiments, including a PoP stacked-chip apparatus according to any of the several disclosed embodiments and their equivalents, an electronic system, a computer system, one or more methods of fabricating an integrated circuit, and one or more methods of fabricating an electronic assembly that includes a PoP stacked-chip apparatus according to any of the several disclosed embodiments as set forth herein in the various embodiments and their art-recognized equivalents. The elements, materials, geometries,

dimensions, and sequence of operations can all be varied to suit particular I/O coupling requirements including array contact count, array contact configuration for a microelectronic die embedded in a processor mounting substrate according to any of the several disclosed PoP stacked-chip apparatus embodiments and their equivalents.

The Abstract is provided to comply with 37 C.F.R. §1.72(b) requiring an abstract that will allow the reader to quickly ascertain the nature and gist of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

In the foregoing Detailed Description, various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments of the invention require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate preferred embodiment.

It will be readily understood to those skilled in the art that various other changes in the details, material, and arrangements of the parts and method stages which have been described and illustrated in order to explain the nature of this invention may be made without departing from the principles and scope of the invention as expressed in the subjoined claims.

CLAIMS

What is claimed is:

1. A package-on-package apparatus comprising:

a package substrate including a die side and a land side;

a chip stack disposed on the die side, wherein the chip stack includes a bottom chip disposed on the die side and a top chip disposed above the bottom chip, wherein the top chip is supported by the bottom chip, and wherein the chip stack has an offset height; and

an interposer disposed on the die side and surrounding the chip stack, wherein the interposer matches the offset height.

2. The apparatus of claim 1, wherein the interposer has a ball-grid array, the apparatus further including:

a top package, wherein the top package includes at least one microelectronic device, and wherein the top package mates to the interposer ball-grid array.

3. The apparatus of claim 1, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side; and

the top chip is a wire-bond chip disposed on the flip chip.

4. The apparatus of claim 1, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side;

a wire-bond second chip disposed above the flip chip; and

the top chip is a wire-bond subsequent chip disposed above the wire-bond second chip.

5. The apparatus of claim 1, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side;

a through-silicon via (TSV) second chip disposed on the flip chip; and

the top chip is a wire-bond subsequent chip disposed on the TSV second chip.

6. The apparatus of claim 1, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side;

a through-silicon via (TSV) second chip disposed on the flip chip;

a TSV third chip disposed on the TSV second chip; and

the top chip is a wire-bond fourth chip disposed on the TSV third chip.

7. The apparatus of claim 1, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side;

a through-silicon via (TSV) second chip disposed on the flip chip;

a TSV third chip disposed on the TSV second chip, wherein the TSV third chip is a plurality of TSV chips in a range from 2 to 8 TSV chips; and

the top chip is a wire-bond subsequent chip disposed above the TSV third chip.

8. The apparatus of claim 1, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side;

a through-silicon via (TSV) second chip disposed on the flip chip;

a TSV third chip disposed above the TSV second chip;

a wire-bond fourth chip disposed above the TSV second chip; and

the top chip is a wire-bond subsequent chip disposed above the wire-bond fourth chip.

9. The apparatus of claim 1, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side;

a wire-bond second chip disposed above the TSV first chip;

a through-silicon via (TSV) third chip disposed above the wire-bond second chip; and

the top chip is a wire-bond subsequent chip disposed above the TSV third chip.

11. The apparatus of claim 1, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side; and

the top chip is a through-silicon via (TSV) chip disposed on the flip chip.

12. The apparatus of claim 1, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side;

the top chip is a through-silicon via (TSV) subsequent chip disposed above the flip chip; and

at least one TSV chip disposed between the bottom chip and the top chip in a range from 2 to 7.

13. A package-on-package stacked-chip apparatus comprising:

a package substrate including a die side and a land side;

a chip stack disposed on the die side, wherein the chip stack includes a bottom chip disposed on the die side and a top chip disposed above the bottom chip, wherein the top chip is supported by the bottom chip, and wherein the chip stack has an offset height;

an interposer disposed on the die side and surrounding the chip stack, wherein the interposer matches the offset height; and

a top package disposed on the interposer, wherein the top package includes at least one microelectronic device.

14. The apparatus of claim 13, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side; and

the top chip is a through-silicon via (TSV) chip disposed on the flip chip.

15. The apparatus of claim 13, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side;

the top chip is a through-silicon via (TSV) subsequent chip disposed above the flip chip; and

at least one TSV chip disposed between the bottom chip and the top chip in a range from 2 to 7.

16. The apparatus of claim 13, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side; and

the top chip is a wire-bond chip disposed on the flip chip.

17. The apparatus of claim 13, wherein the chip stack includes:

the bottom chip is a flip chip mounted on the substrate die side;

a wire-bond second chip disposed on the flip chip; and

the top chip is a wire-bond subsequent chip disposed above the wire-bond second chip.

18. A method of assembling a package-on-package stacked-chip apparatus, comprising:

assembling a top package with a ball-grid array to a matching ball-grid array of a 3-dimensional (3D) stacked-chip apparatus, the 3D stacked-chip apparatus including:

a package substrate including a land side and a die side;

a chip stack disposed on the die side, wherein the chip stack has a stack height; and

an interposer including a die side and a top side, wherein the interposer produces an offset height that matches the stack height, and wherein assembling includes mating the top package to the interposer.

19. The method of claim 18, wherein the chip stack is assembled on the package substrate before assembling the interposer to the package substrate.

20. The method of claim 18, wherein the interposer is assembled on the package substrate before assembling the chip stack to the package substrate.

21. The method of claim 18, further including forming a stack encapsulation over the chip stack.

22. The method of claim 18, wherein the chip stack is formed including:

flip-chip mounting a bottom chip on the substrate die side; and

wire-bond mounting a top chip above the flip chip.

23. The method of claim 18, wherein the chip stack is formed including:

flip-chip mounting a bottom chip on the substrate die side;

wire-bond mounting a second chip above the bottom chip; and

wire-bond mounting a top chip above the second chip.

24. The apparatus of claim 18, wherein the chip stack is formed including:

flip chip-mounting a bottom chip on the substrate die side;

through-silicon via (TSV) mounting a second chip on the flip chip; and

wire-bond mounting a subsequent chip as a top chip above the second chip.

25. A computing system, comprising:

a package substrate including a die side and a land side;

a chip stack disposed on the die side, wherein the chip stack includes a bottom chip disposed on the die side and a top chip disposed above the bottom chip, wherein the top chip is supported by the bottom chip, and wherein the chip stack has an offset height;

an interposer disposed on the die side and surrounding the chip stack, wherein the interposer matches the offset height; and

a top package disposed on the interposer, wherein the top package includes at least one microelectronic device; and

a device housing that contains the top package.

26. The computing system of claim 25, wherein the computing system is part of one of a cellular telephone, a pager, a portable computer, a desktop computer, and a two-way radio.

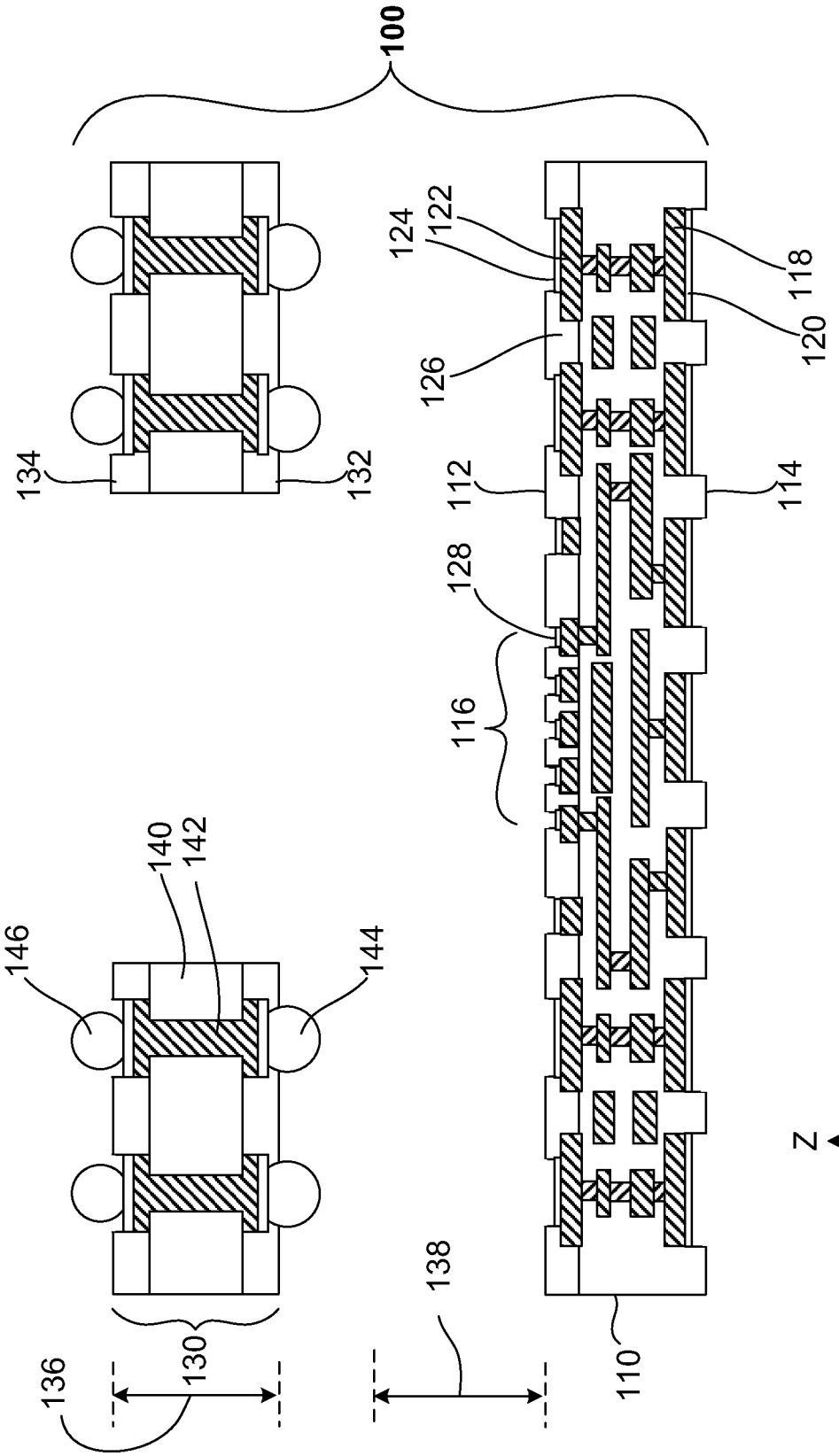

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Fig. 1a

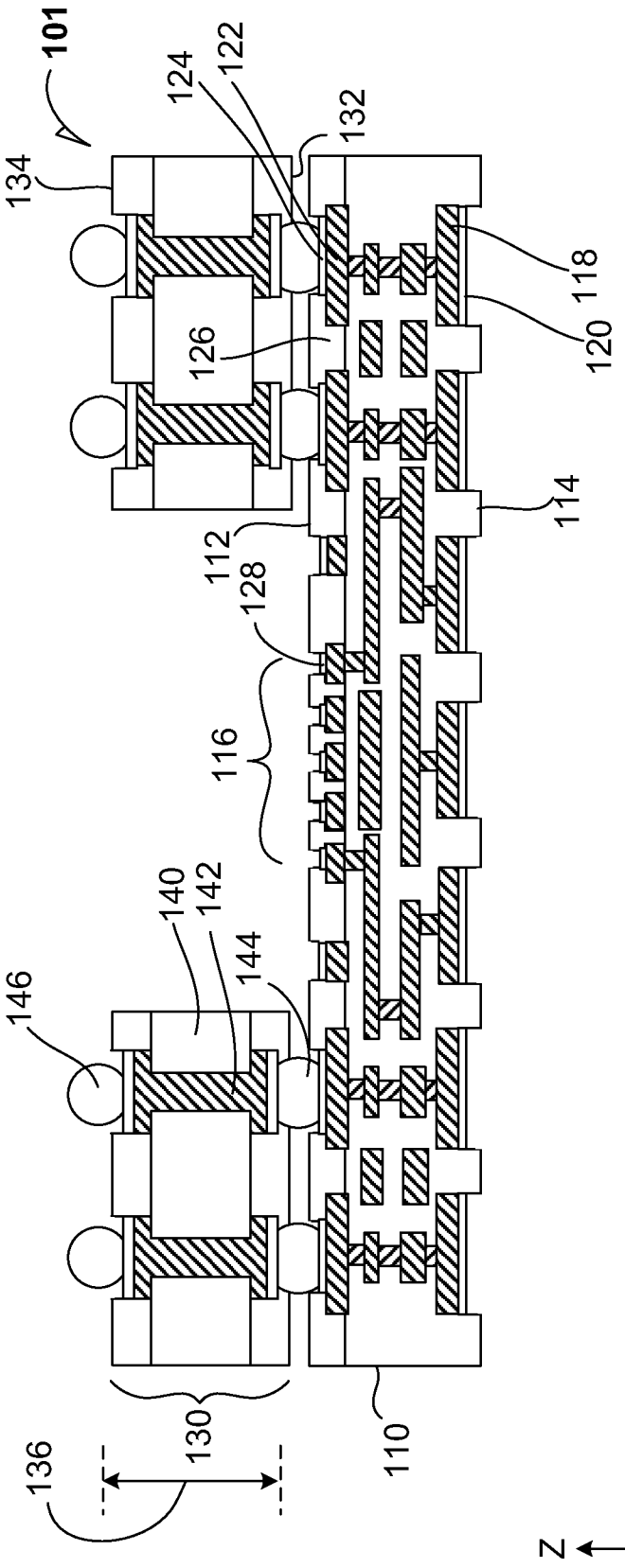

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Fig. 1b

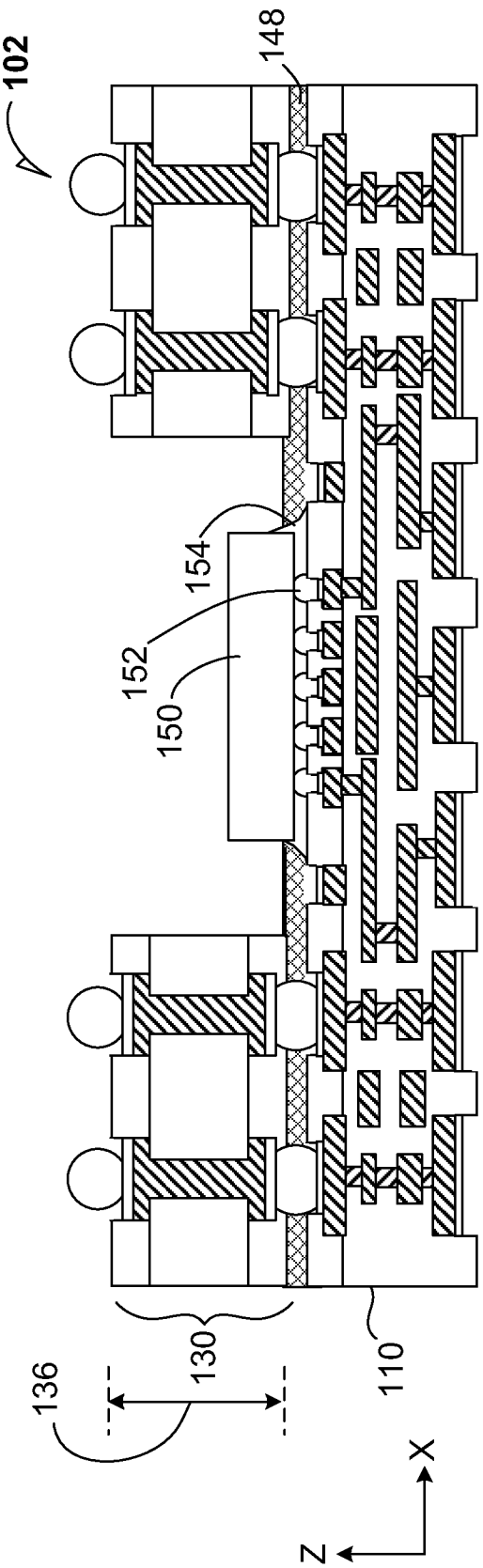

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Fig. 1c

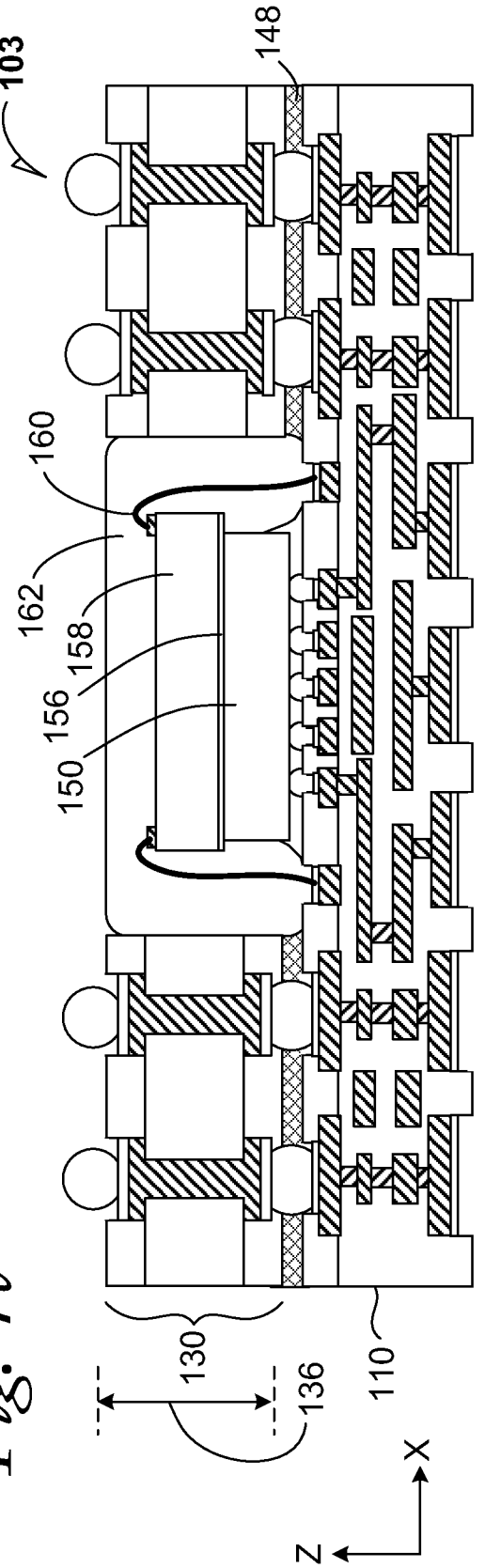

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Fig. 1d

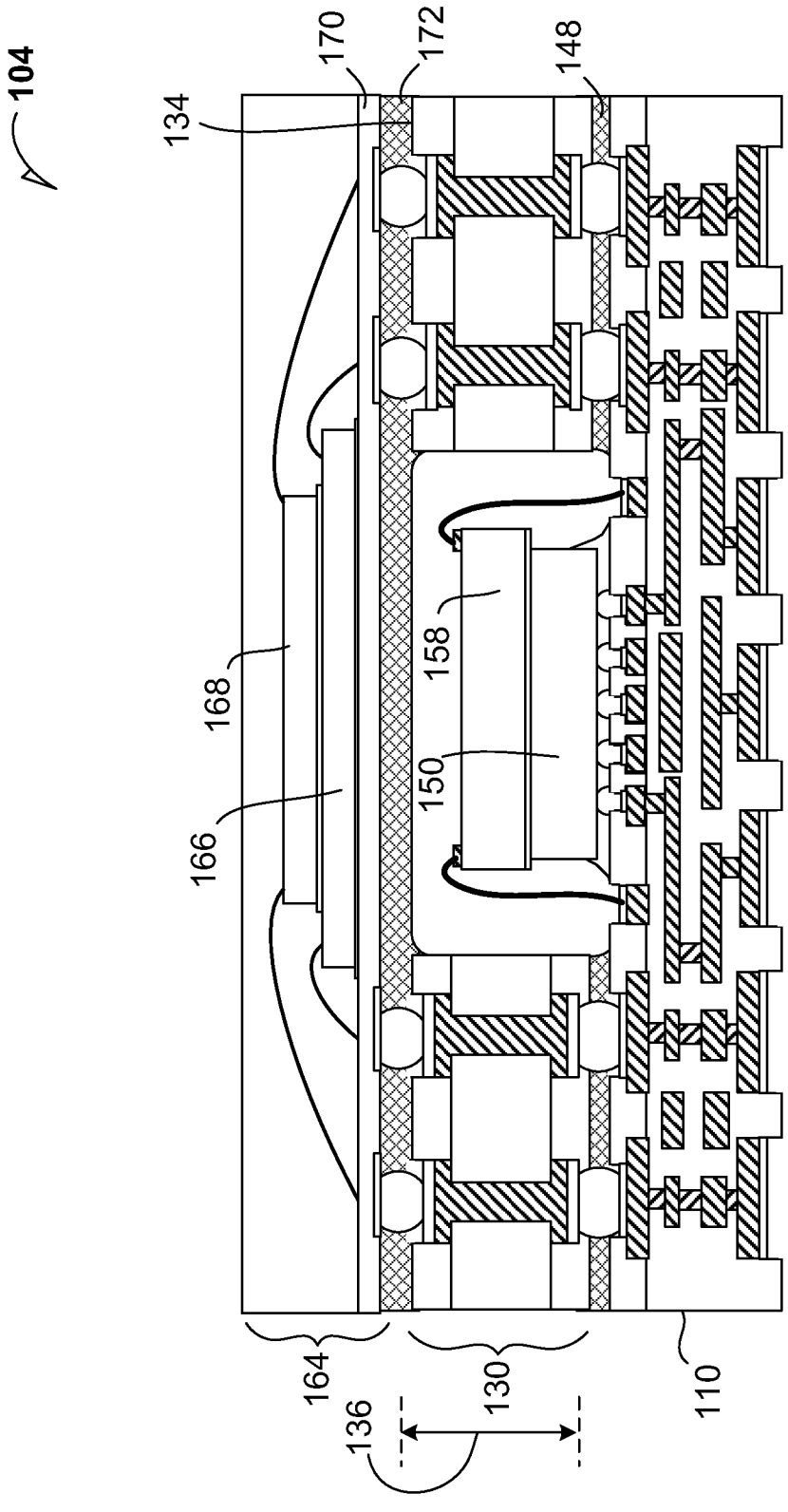


Fig. 1e

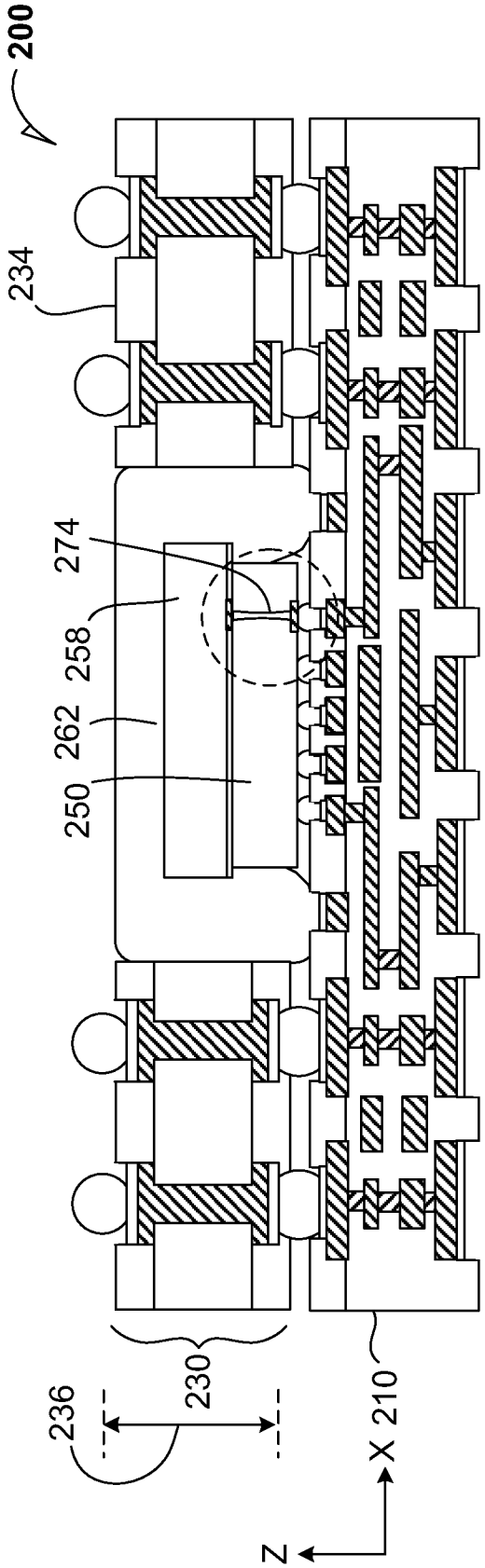

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Fig. 2a

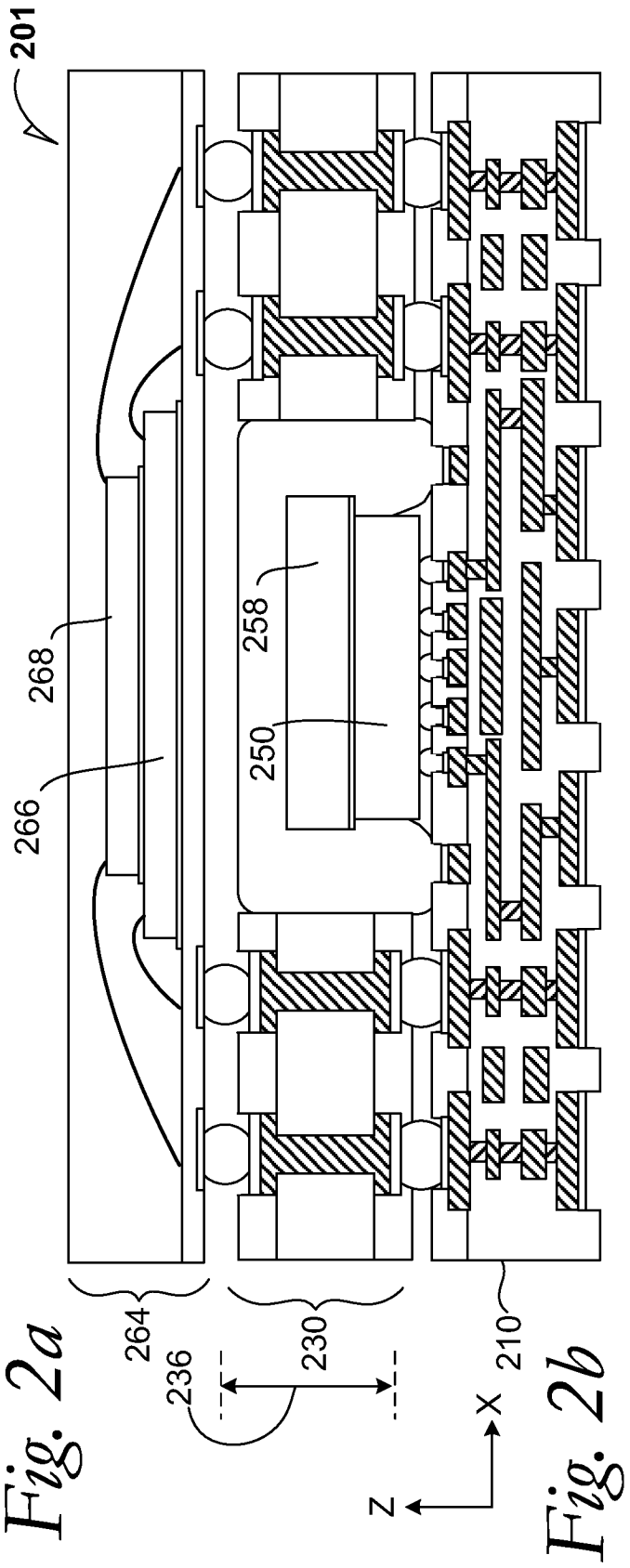

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Fig. 2b

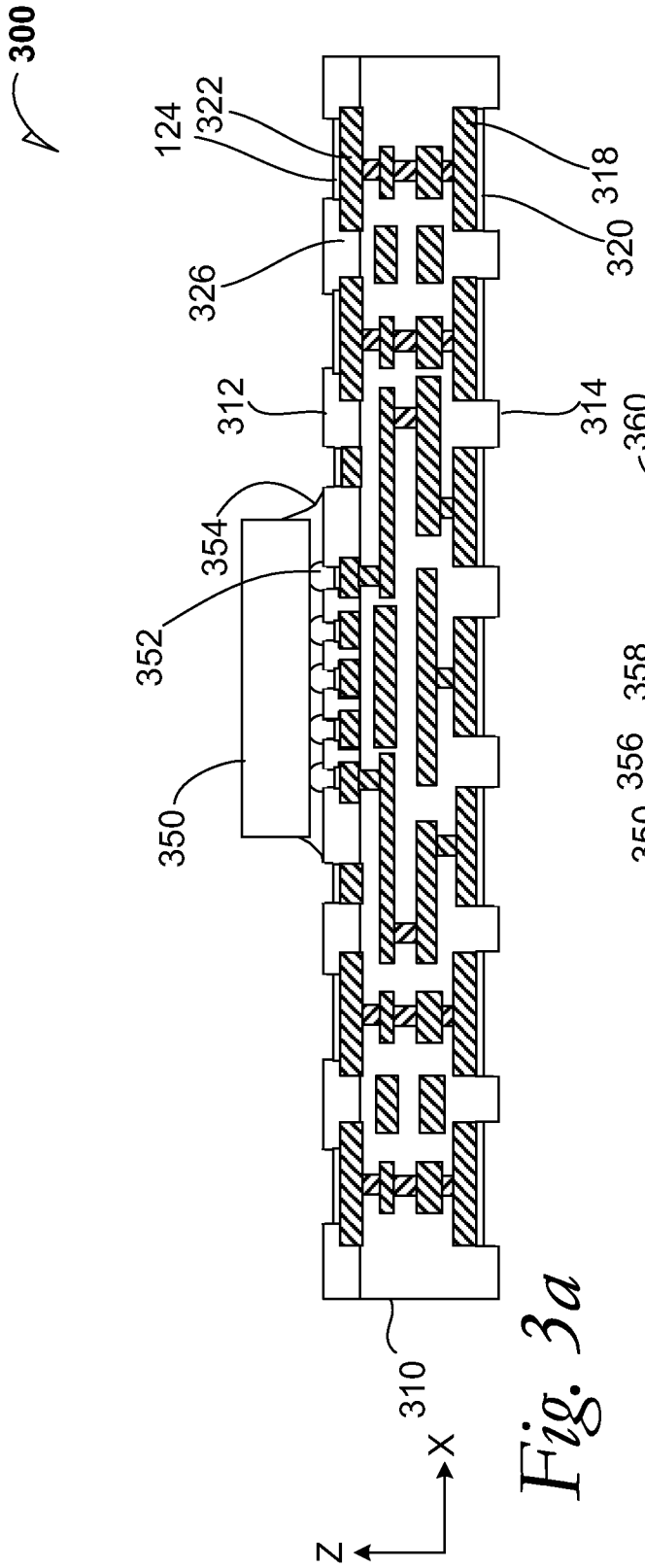

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Fig. 3a

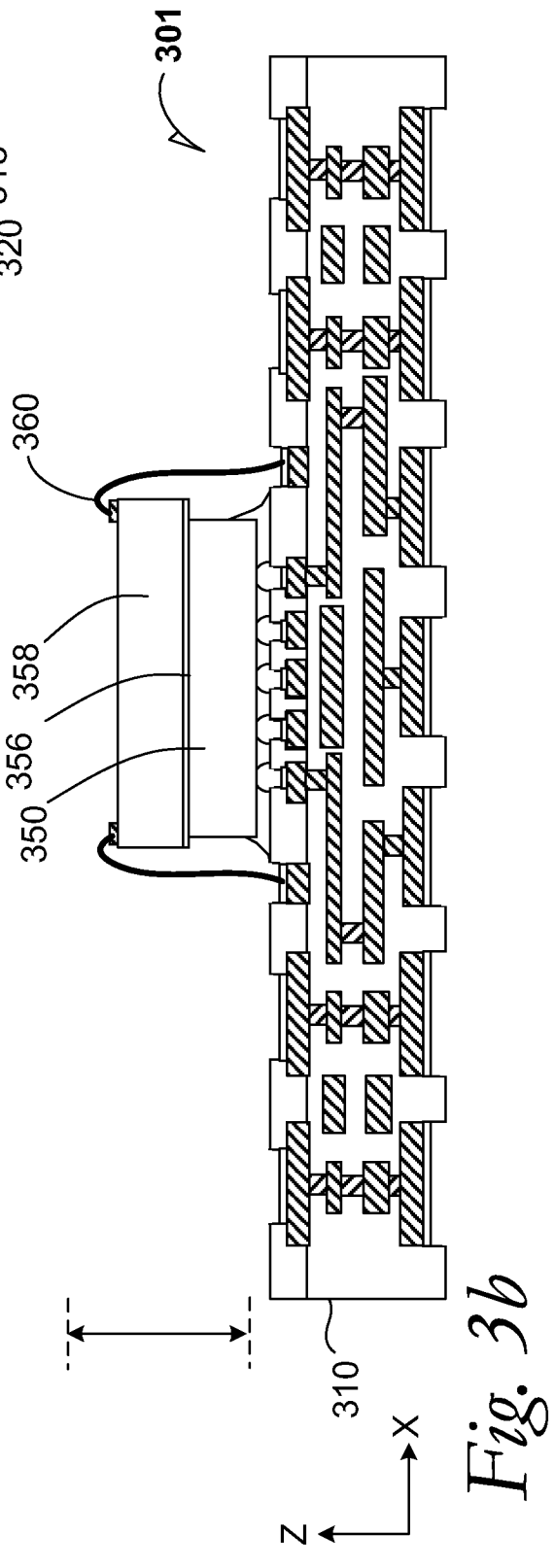

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Fig. 3b

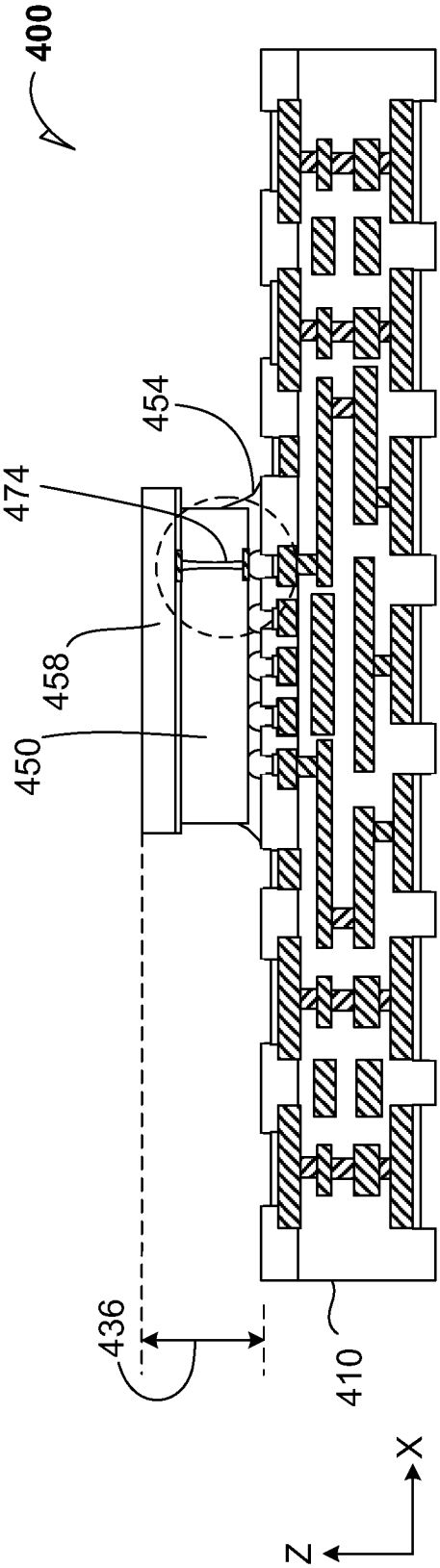

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Fig. 4

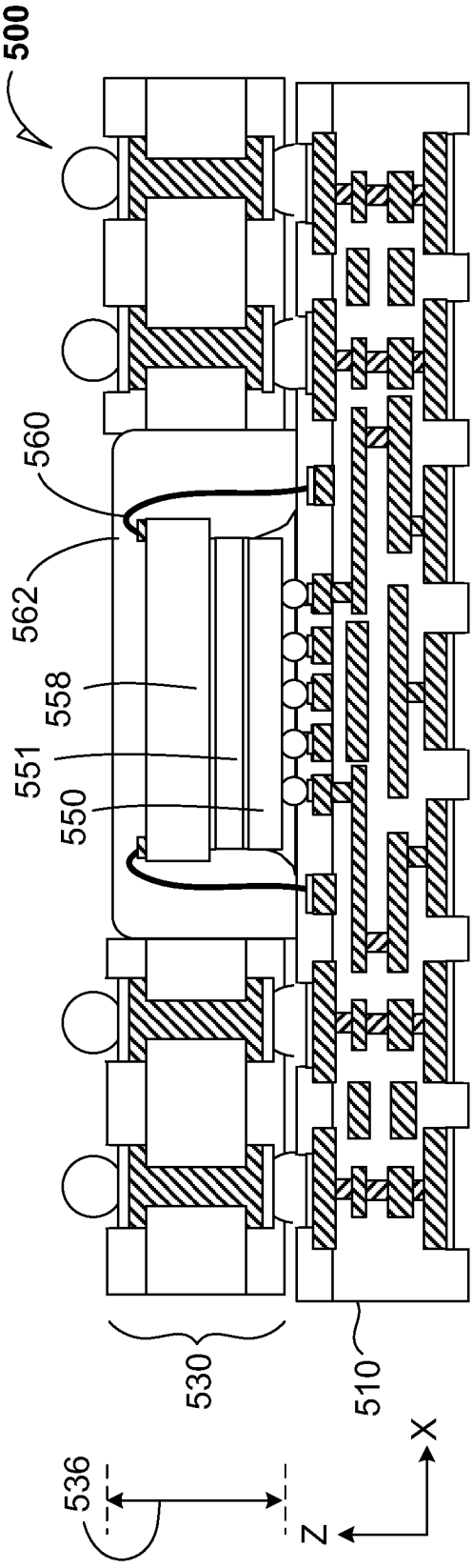

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510
536
X
Z

Fig. 5

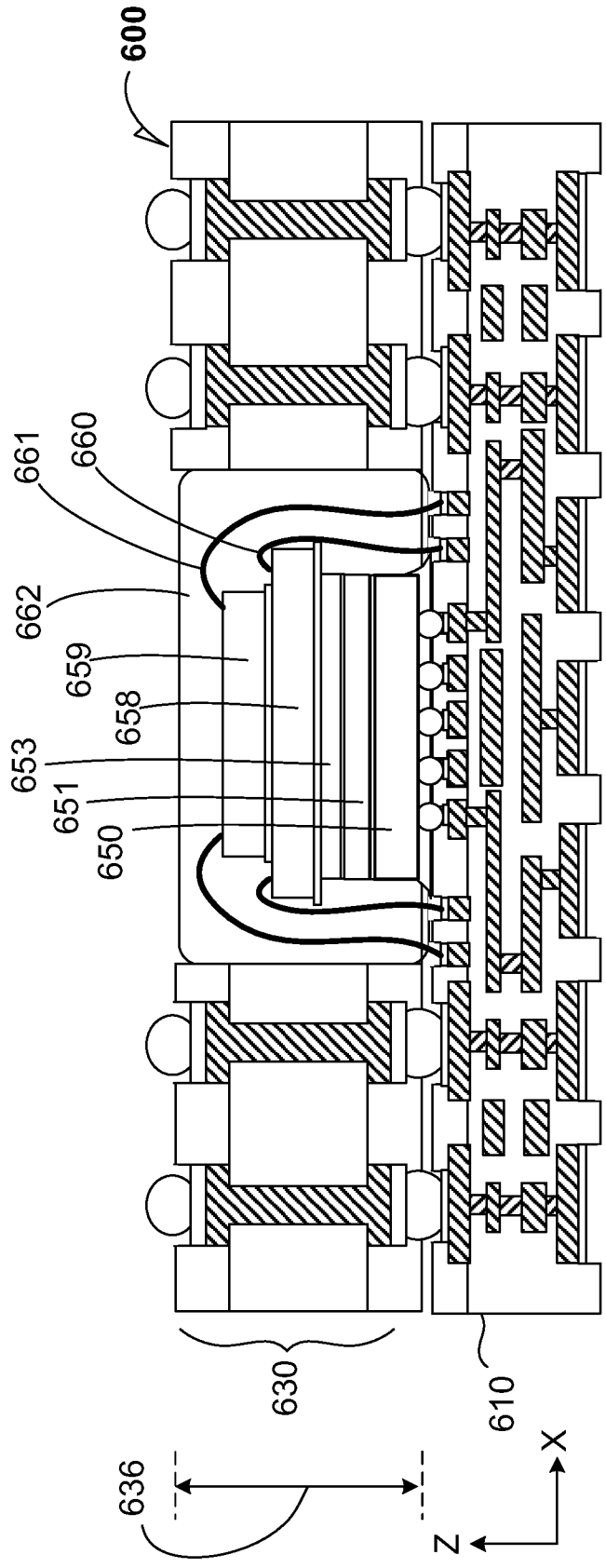


Fig. 6

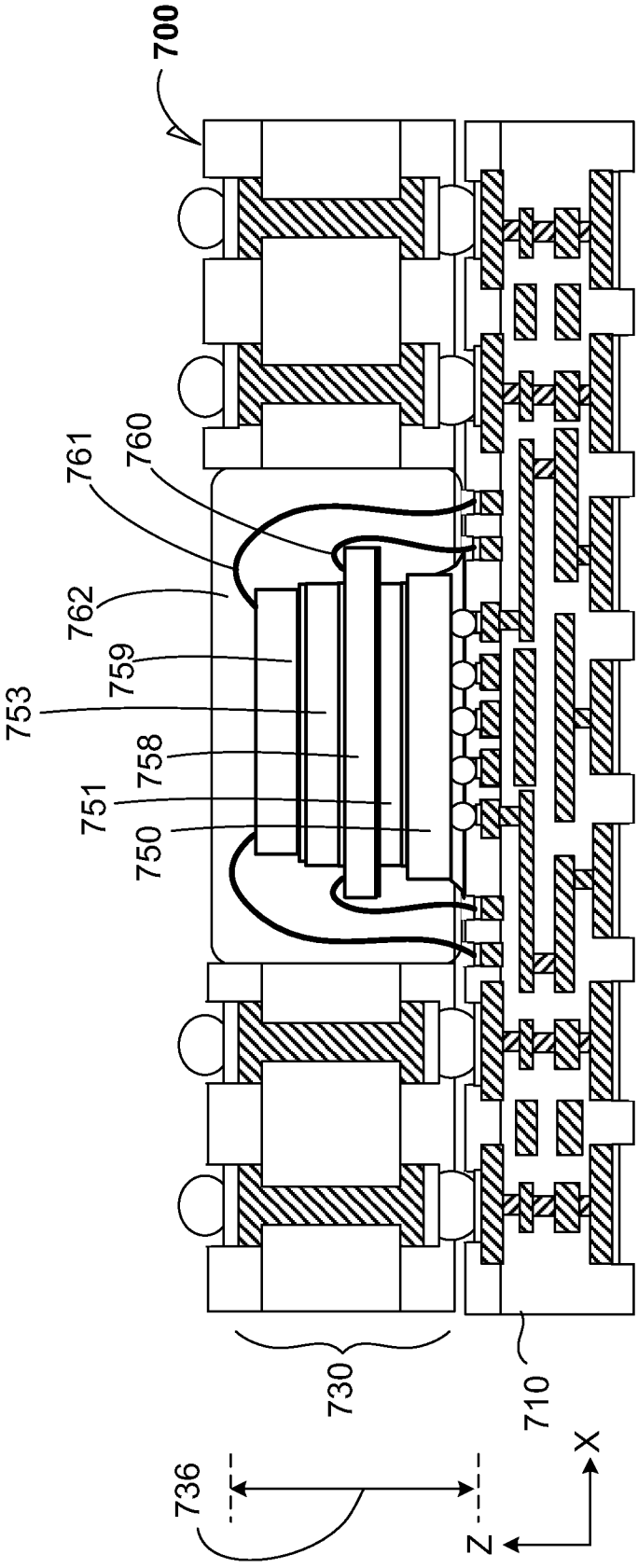


Fig. 7

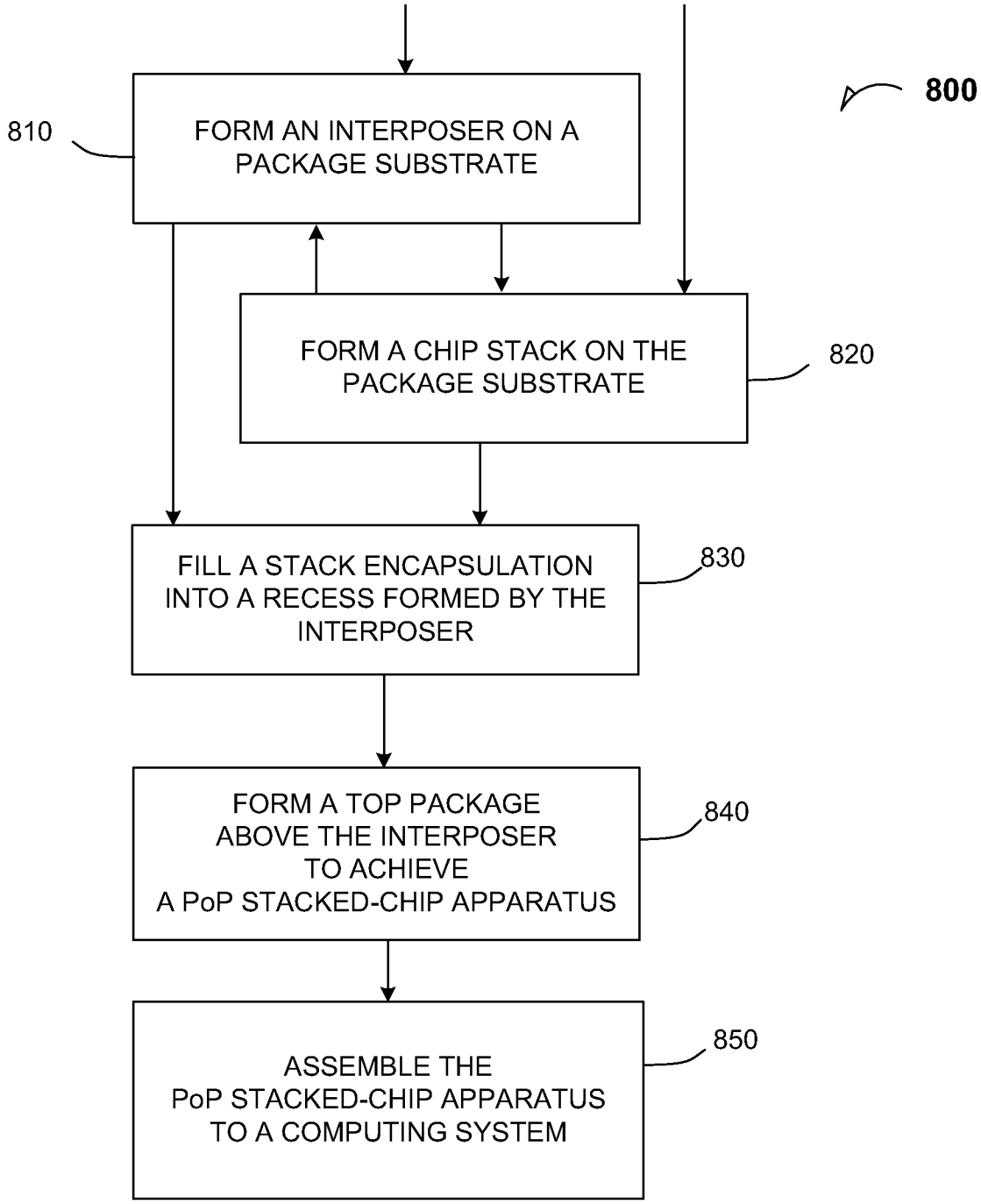

800
810
FORM AN INTERPOSER ON A PACKAGE SUBSTRATE
FORM A CHIP STACK ON THE PACKAGE SUBSTRATE
820
FILL A STACK ENCAPSULATION INTO A RECESS FORMED BY THE INTERPOSER
830
FORM A TOP PACKAGE ABOVE THE INTERPOSER TO ACHIEVE A PoP STACKED-CHIP APPARATUS
840
ASSEMBLE THE PoP STACKED-CHIP APPARATUS TO A COMPUTING SYSTEM
850

Fig. 8

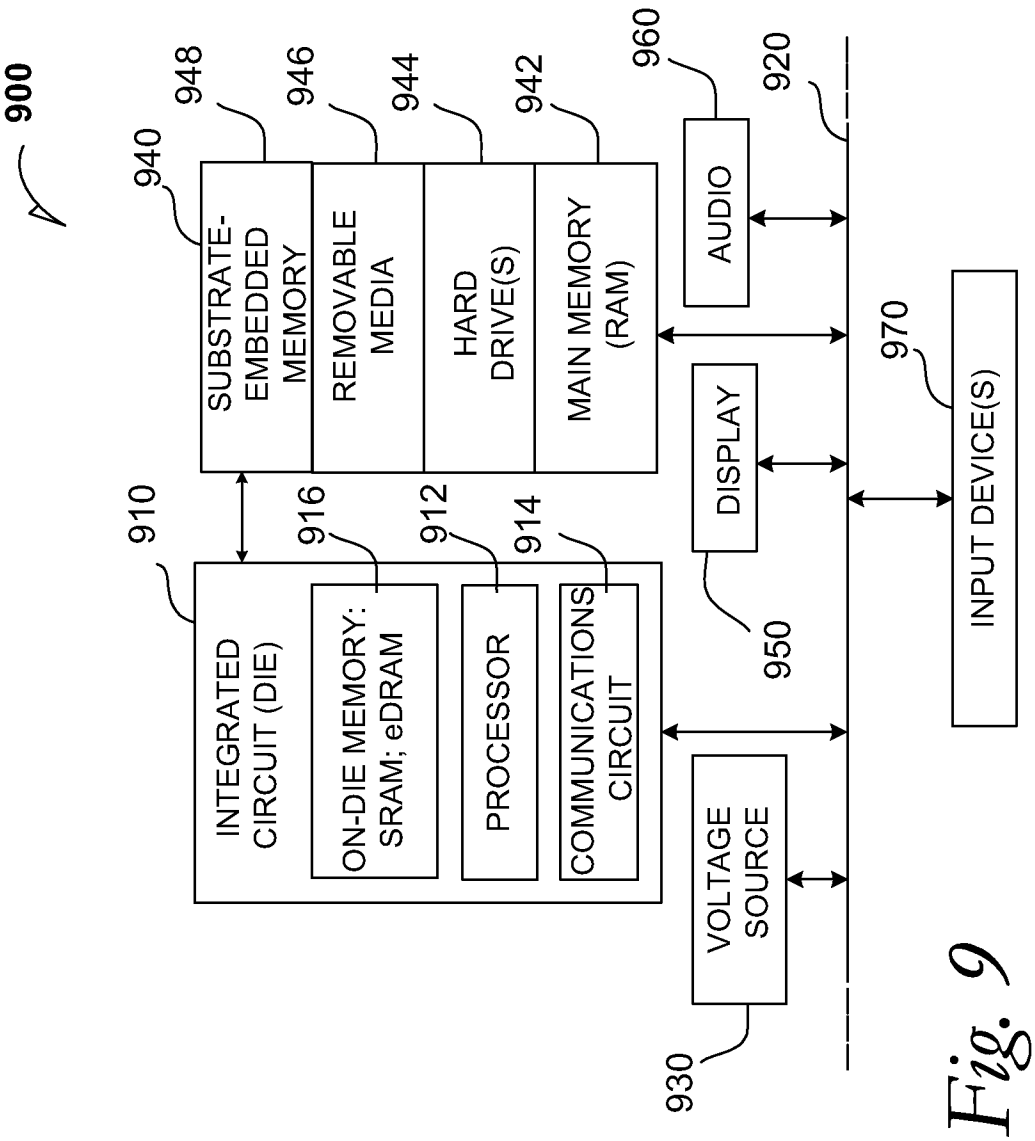

900
940
948
946
944
942
960
920
SUBSTRATE-EMBEDDED MEMORY
REMOVABLE MEDIA
HARD DRIVE(S)
MAIN MEMORY (RAM)
AUDIO
910
916
912
914
970
INTEGRATED CIRCUIT (DIE)
ON-DIE MEMORY: SRAM; eDRAM
PROCESSOR
COMMUNICATIONS CIRCUIT
DISPLAY
INPUT DEVICE(S)
950
VOLTAGE SOURCE
930

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/033536

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/12(2006.01)i, H01L 23/48(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/12; H01L 21/60; H01L 21/50; H01L 23/02; H01L 23/538; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: dual, multi die, interposer,

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0157326 A1 (HAN HYUN JOO et al.) 03 July 2008 See abstract, paragraphs 32-42, claim 1 and figures 2-5.	1-26
A	US 2006-0175695 A1 (MYUNG KIL LEE) 10 August 2006 See abstract, paragraphs 27-30, 32, 37-41, claims 6-8 and figures 1, 6-9.	1-26
A	US 2008-0111224 A1 (BYUN HAK-KYOON et al.) 15 May 2008 See abstract, paragraphs 24-26, 28, 30-31, claims1,2 and figure 2.	1-26
A	US 2008-0283992 A1 (PALANIAPPAN PREMA et al.) 20 November 2008 See abstract, paragraphs 21,22, 30-33, claims 1-6 and figures 1A-D,2.	1-26

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 NOVEMBER 2010 (16.11.2010)	**22 NOVEMBER 2010 (22.11.2010)**

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Facsimile No. 82-42-472-7140

Authorized officer

CHO, Cheon Whan

Telephone No. 82-42-481-8328

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2010/033536

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