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(71) Applicant and
(72) Inventor: **ABROSIMOV, Igor Anatolievich** [RU/RU]; Moskovsky pr-t, 36-7, St.Petersburg, 198013 (RU).

(74) Agent: **NILOVA, Maria Innokentievna**; PATENTICA, Moika Embankment, 58, St.Petersburg, 190000 (RU).

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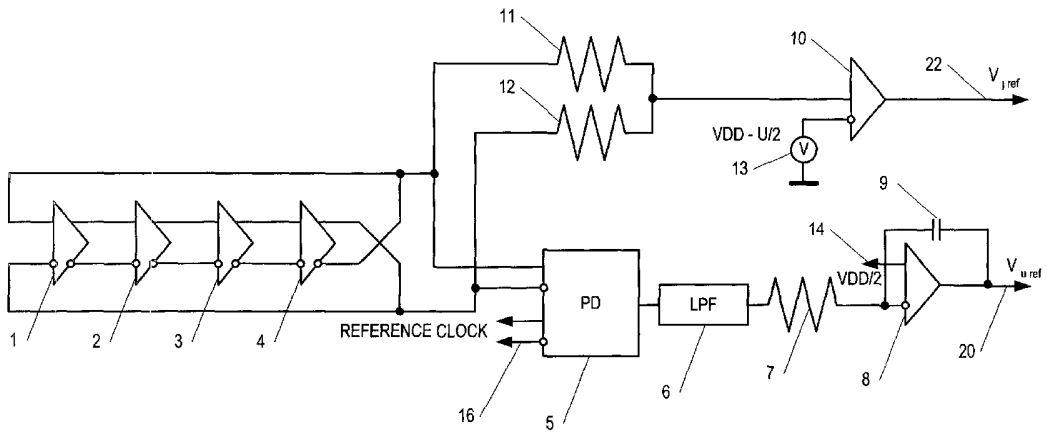
(54) Title: REFERENCE VOLTAGE GENERATOR FOR LOGIC ELEMENTS PROVIDING STABLE AND PREDEFINED GATE PROPAGATION TIME



(57) Abstract: A reference voltage generator employs a ring oscillator having a plurality of logic stages and a phase/frequency detector, for generating a first feedback signal on the basis of a phase/frequency difference between the phase/frequency of a reference clock and the phase/frequency of the ring oscillator; and to generate a second feedback signal on the basis of a voltage swing of the oscillator circuit; both feedback signals to be applied to said plurality of logic stages of the ring oscillator; whereby a constant delay is created through each logic stage of the logic device. In another aspects of the invention, a method of generating a reference voltage for a logic device by using the reference voltage generator as above and a logic device with a controlled propagation delay of each of the logic stages are provided.

WO 03/100973 A2

REFERENCE VOLTAGE GENERATOR FOR LOGIC ELEMENTS PROVIDING STABLE AND PREDEFINED GATE PROPAGATION TIME

Technical Field

The present invention relates to a circuit for generating a reference voltage. In particular, the invention creates to generating a voltage reference that is a function of the gate propagation time, to create circuits where a constant time characteristic is beneficial.

Background of the Invention

Voltage references are used widely in electronics to create a stable current or voltage. The voltage references are normally chosen either to be fixed, or to track temperature or process variations.

Most of the known circuits which generate a reference voltage use a structure of the bandgap type which is based on the principle of the thermal dependence of both the voltage drop across the base-emitter junction, VBE, and the thermal voltage VT (VT =k*T/q) of a bipolar transistor. These two voltage values have a negative and a positive thermal coefficient, respectively, i.e. they are respectively increased and decreased with the device temperature. Thus, by an appropriate weighted sum, it is possible to obtain from them a voltage generating circuit which has a null thermal coefficient, i.e. is unaffected by variations in temperature. The circuit of this type is disclosed in US 5,747,978 for generating a reference voltage and detecting a drop in a supply voltage.

Another widely used approach is to implement a replica bias structure. According to US 5,847,616, a replica biasing circuit producing the impedance control voltage immune to variations in the semiconductor manufacturing process, fluctuations in the power supply voltage source, and changes in operating temperature is provided for a voltage reference generator to produce a stable reference voltage that is coupled to the voltage reference input terminal of the replica biasing circuit.

The above approach is typically used also in differential current mode inverters/buffers such as shown in Fig.2, to provide a predefined current through

the MOSFET 1 and another one for the pull-ups. It can be used also to control of pull ups in single ended open drain logic and in totem pole logic, etc.

Whilst the present invention has wide application, for the sake of clarity, consider the case where a voltage reference is required in a differential current mode inverter/buffer as shown in Figure 2.

This circuit in Figure 2 has a voltage reference 22 to control the current in the MOSFET 21, and a further voltage reference 20 is required to control the voltage swing of a MOSFET for the pull up devices 25 and 26.

These voltage references are normally chosen either to be fixed, or to track temperature or process variations. Usually the voltage reference has the same structure as the transistor to be controlled, with constant logic levels, controlling the logic low voltage level based on the required swing. However, in this case, all variations in temperature, process technology and power supply cause variations in the propagation time of the gate.

Libraries of leaf cells used in the design of integrated circuits quote a range of propagation delays for each cell. At the same time, it is not usually of any advantage when the cell operates faster than the slowest case: circuits must be simulated using worst case figures.

Object of the present invention

It is a primary object of the present invention to provide a voltage reference which is a function of gate propagation delay.

It is another primary object of the present invention to apply that voltage reference to translate variations in temperature, power supply voltage and process variation that would otherwise be wasted, into savings in power consumption.

It is another object of the present invention to provide a reference that can control circuits such that they have a constant propagation delay characteristic, or switching characteristics such as slew rate and bandwidth. Such gates can be used in high frequency filters, oscillators, drivers, verniers and in other applications.

A particular form of the invention is suitable for use with differential current mode circuits that normally have a high power consumption per stage.

Summary of The Invention

The present invention relates to use of a ring oscillator and phase detector to generate a signal, which is filtered to provide a voltage reference which varies as a function of the ring oscillator gate delays, which in turn vary with temperature, process variation and power supply voltages.

According to the invention, a reference voltage generator for generating a reference voltage for a logic device comprises a ring oscillator having a plurality of logic stages incorporating the said logic device, a reference clock generator; a means for detecting a phase or frequency difference between the reference clock and the ring oscillator, to generate a first feedback signal that causes the current of said plurality of logic stages to vary as a function of the period of the ring oscillator; and a means for measuring a voltage swing of the oscillator circuit, to generate a second feedback signal that causes the current of said plurality of logic stages to vary as a function of the amplitude variations in the ring oscillator; whereby a constant delay is created through each logic stage of the logic device.

In another aspects of the invention, a method of generating a reference voltage for a logic device by using the reference voltage generator as above and a logic device with a controlled propagation delay of each of the logic stages are provided.

Brief Description of The Drawings

For a better understanding of the present invention and the advantages thereof and to show how the same may be carried into effect, reference will now be made, by way of example, without loss of generality to the accompanying drawings in which:

Fig.1 shows a block diagram of one of the embodiments of the present invention. Fig. 2 shows a simple differential stage which can be used as an inverter or a non-inverting buffer, which are well known in the prior art.

Detailed Description Of The Invention

The invention will now be described in detail without limitation to the generality of the present invention with the aid of example embodiments and accompanying drawings.

Figure 1 shows a block diagram of an example embodiment of the reference voltage generator according to the present invention. The reference voltage generator comprises a ring oscillator 1 to 4, which incorporates as its logic stages, the logic device, to which the reference voltage generated by said reference voltage generator is applied.

Further, the reference voltage generator shown in Fig.1 comprises a phase/frequency detector 5, amplifier 10, summing resistors 11, 12, low pass filter 6, an integrator consisting of resistor 7, amplifier 8 and capacitor 9, with voltage sources 13,14, and a reference clock 16.

The reference clock 16, can be generated with very high accuracy and stability, for example using a signal derived from a crystal oscillator. The reference clock shall be defined first, to define the number of gates needed in the ring oscillator 1,2,3,4. The period of the ring oscillator 1 - 4 should be the same as the period of the reference clock 16 for the slowest conditions of temperature, power supply and process. In general case, the number of stages can be defined, thus, by dividing the half period of the reference clock by the delay of each logic stage. If the ratio of frequencies is too large, a divider can be placed between the ring oscillator 1 - 4 and the phase detector 5 as is normal practice in phase locked clock synthesisers.

The phase detector 5, converts the phases of the reference clock 16 and the phase of the ring oscillator 1 - 4 into an error signal, expressed as a pulse width modulated signal. In the simplest case the phase detector 5 can be implemented using an XOR gate. The low pass filter 6, converts this signal into a voltage, which is then integrated to provide a voltage reference 20, for controlling pull up strength.

It is appreciated that within the present application, the term "phase detector" incorporates a phase detector or a phase/frequency detector. The voltage swing of the oscillation in the ring oscillator 1, 2, 3, 4, assuming the highest voltage is Vdd, is measured using equal summing resistors 11 and 12, which is compared with a voltage source 13, which is set to (Vdd – half of the required amplitude). This difference is amplified by amplifier 10, which is then applied as the second feedback signal to the gates in the ring oscillator to control their

current, in the case they are controlled by current sources, such as 21 in the pull down structure in differential current mode gates.

In the prior art clock synthesisers, the frequency of the ring oscillators are controlled through current of the pull down structure for the differential stage. The propagation delay is relatively insensitive to the pull down current.

The reference voltage 20, as applied to the pull up devices, acts directly because it changes the product of the pull up resistance and parasitic capacitance of the gate, and the input parasitic capacitance of the load.

In Fig. 2, a simple prior art differential stage is shown which can be used as an inverter or a non-inverting buffer depending on the connection polarity of the outputs to the next differential stage. The key features of this differential stage is a current source 21, implemented in the simplest case using a transistor with a fixed voltage on the gate from a voltage source 22, the two transistors 23 and 24, forming the logic function of the inverter/buffer, with a pull up structure 25, 26 which can be in the simplest case two resistors. These differential gates are well known in the prior art and date back for many decades.

Consider now how the structure in Figure 1 may be used for providing a reference voltage for the circuit shown in Figure 2. It is appreciated that Figure 2 is generic: one could use the same Figure 1 with a single ended circuit comprising the left and middle portions of the circuit in Figure 2, and with various other configurations thereof.

It shall be also appreciated that in this example embodiment, the first feedback signal, being represented by voltage reference 20 in Figure 1 is used for the voltage reference 20 in Figure 2, and the second feedback signal represented by voltage reference 22 in Figure 1 is used as voltage reference, 22, in Figure 2 to control the current. Alternatively, the voltage reference 20 in Fig. 1 can be used as voltage reference 22 in Fig.22, while the voltage reference 22 from Fig. 1 will be fed in this case as voltage reference 20 in Fig.2. It shall be taken into account that the feedback loops are negative type feedbacks, and accordingly, the polarity of feeding feedbacks shall be checked each time. In case the feedback is positive, an inverter stage is added to the feedback.

The gates 1, 2, 3 and 4 are all as described in Figure 2 and the voltage references generated by the device in Figure 1 can be applied to the gates in the ring oscillator 1, 2, 3, 4, as well as to the gates in the external circuitry for which it is desired to have a controlled propagation delay characteristic.

The operation of the circuit of the present invention will now be described in detail.

Where the process, temperature or Vdd causes the propagation time through the gates in the ring oscillator 1 - 4 to reduce, this is translated into a fall in the reference voltage 20. This in turn causes the pull up devices 25, 26 to reduce their strength, which causes an increase in the RC product of the pull up and parasitic capacitance of the circuitry. This then causes a drop in the frequency.

In turn, due to the higher resistance of the pull up 25, 26, the voltage on the voltage divider built using resistors 11 and 12, will go down, which will cause the output of the operational amplifier 10 to go down as well. This reduces the current in the logic stages 1-4 by reducing the voltage 22 on the gate of the current source in the differential stages. This is a closed loop, which will continue until the voltage Vj ref on the output of the divider will settle.

The time constant for the integrator is not critical, but depends on the requirements of the ring oscillator; whether it is to be used elsewhere as a clock source, then the time constant should be optimised to reduce jitter.

The cut off frequency of the low pass filter 6 is also not critical: the filter can be a high frequency just to reduce ripple and hunting of the loop.

Both the low pass filter 6 and the integrator 7, 8, 9, can be replaced by a typical charge pump circuit.

When the propagation delay of the gate becomes too big, then the circuit operates in the opposite way to that described above, to increase the pull up strength and increase the current, thus for a predefined propagation time the circuit will generate reference voltages that minimise the power consumption current and stablise the propagation time.

CLAIMS:

1. A reference voltage generator for generating a reference voltage for a logic device comprising at least one logic stage, the generator comprising:

- a ring oscillator circuit having a plurality of logic stages incorporating the above at least one logic stage of the logic device,
- a reference clock generator;
- a means for detecting a phase/frequency difference between the phase/frequency of the reference clock and the phase/frequency of the ring oscillator, to generate a first feedback signal to be applied to a plurality of logic stages; and
- a means for measuring a voltage swing of the oscillator circuit, to generate a second feedback signal to be applied to said plurality of logic stages;
- whereby a constant delay is maintained through each logic stage of the logic device.

2. A reference voltage generator according to claim 1, wherein the logic device is a single ended circuit.

3. A reference voltage generator according to claims the logic device is a differential circuit.

4. A reference voltage generator according to claim 3, wherein the differential circuit is selected from a current mode buffer and current mode inverter.

5. A reference voltage generator according to claims 3 or 4, wherein the differential circuit comprises a current source, a pair of transistors and a pull up device.

6. A reference voltage generator according to any one of claim 5, wherein the pull up strength of the pull up device is varied using any one of the

feedback signals, while the current of the current source is varied using the other feedback signal.

7. A reference voltage generator according to claims 1 to 6 wherein the current through the logic stage is reduced to the minimum level needed to maintain a particular propagation delay through the logic stage.

8. A reference voltage generator according to claims 1 to 7, wherein the means for detecting a phase/frequency difference is a phase detector.

9. A reference voltage generator according to claim 8 wherein the phase detector is integral with a phase locked clock synthesiser.

10. A reference voltage generator according to claims 5 to 9 wherein the feedback signal is applied to an N Type MOSFET acting as part of the pull up device to reduce power consumption.

11. A reference voltage generator according to claims 5 to 10 wherein the feedback signal is applied to an N Type MOSFET acting as part of the pull up device to control the propagation delay of the logic stage.

12. A method of generating a reference voltage for a logic device, comprising the steps of:

- providing a ring oscillator circuit having a plurality of logic stages incorporating the said at least one logic stage of said logic device,
- providing a reference clock signal;
- detecting a phase/frequency difference between the phase/frequency of the reference clock and the phase/frequency of the ring oscillator, to generate a first feedback signal to be applied to said plurality of logic stages; and
- measuring a voltage swing of the oscillator circuit, to generate a second feedback signal to be applied to said plurality of logic stages;
- whereby a constant delay is maintained through each logic stage of the logic device.

13. A logic device comprising a plurality of at least one logic stage, comprising a current source, a pair of transistors and at least one pull up device, wherein, to provide a controlled propagation delay of each of

the logic stages, the logic device is incorporated in a ring oscillator circuit having a plurality of similar logic stages, and is further provided with:

- a first feedback signal generated on the basis of a phase/frequency difference between the phase/frequency of a reference clock and the phase/frequency of the ring oscillator; and
- a second feedback signal generated on the basis of a voltage swing of the oscillator circuit.

14. A logic device according to claim 13 wherein the feedback signal causes the current of said plurality of logic stages to vary as a function of the period of the ring oscillator.

15. A logic device according to claim 13 or 14 wherein the feedback signal causes the current of said plurality of logic stages to vary as a function of the amplitude variations in the ring oscillator.

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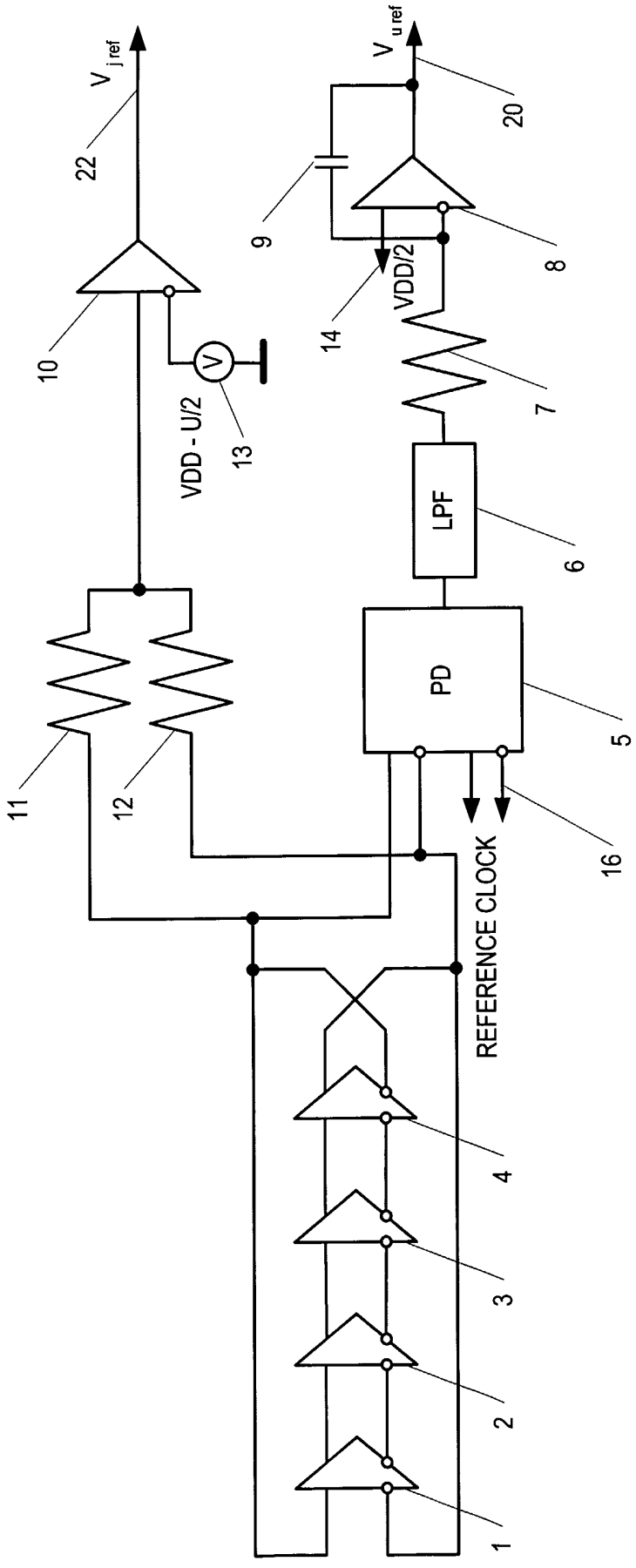
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Fig.1

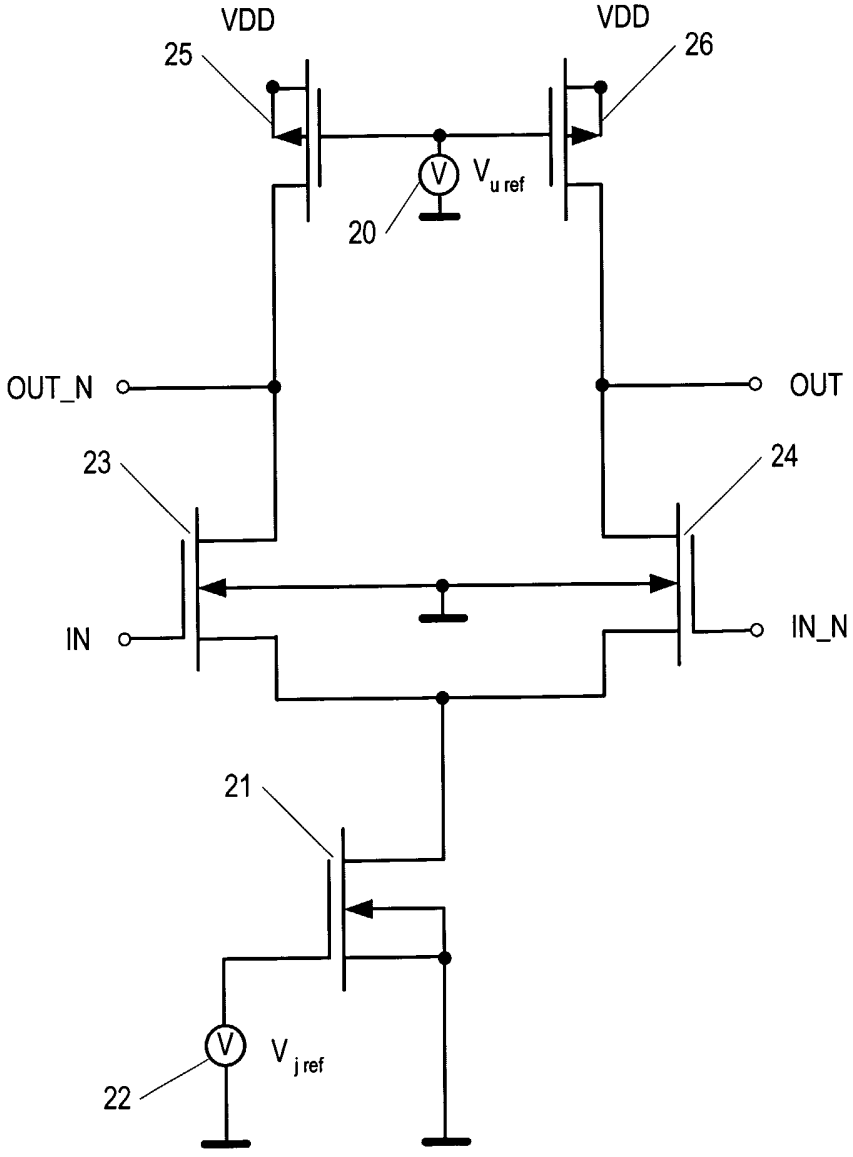

Fig.2