(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 November 2015 (26.11.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/178754 A1

(51) International Patent Classification:
G01N 27/00 (2006.01)

(21) International Application Number:
PCT/MY2015/000032

(22) International Filing Date:
13 May 2015 (13.05.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
PI 2014701279 20 May 2014 (20.05.2014) MY

(71) Applicant: **MIMOS BERHAD** [MY/MY]; Technology Park Malaysia, 57000 Kuala Lumpur (MY).

(72) Inventors: **BIEN, Daniel Chia Sheng**; c/o Mimos Berhad, Technology Park Malaysia, 57000 Kuala Lumpur (MY). **LEE, Hing Wah**; c/o Mimos Berhad, Technology Park Malaysia, 57000 Kuala Lumpur (MY). **MD RAZIB, Nadia**; c/o Mimos Berhad, Technology Park Malaysia, 57000 Kuala Lumpur (MY).

(74) Agent: **TAY, Wee Chao**; c/o Author IP, No. 2-3, Taman Arosa, Jalan Haji Jaib, 84000 Muar, Johor (MY).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *of inventorship (Rule 4.17(iv))*

[Continued on next page]

(54) Title: ISFET INTEGRATED WITH A MICRO-HEATER AND FABRICATION METHOD THEREOF

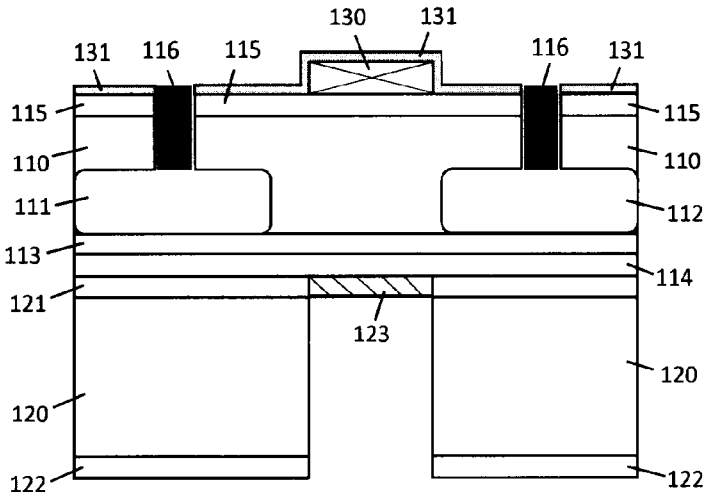

Figure 1J

(57) Abstract: The present invention relates to an ISFET integrated with a heating element, particularly a micro-heater, for gas sensing application. A method for fabricating the ISFET with the micro-heater is also disclosed in the present invention. By using the method of the present invention, the ISFET with the micro-heater has optimum performance and detection sensitivity to its environment changes, while reducing potential damage on the sensing membrane element. Furthermore, the configuration of the ISFET which includes at least two silicon substrates enables the fabrication of the ISFET device with the micro-heater to be more effective, leaves no air gap, and does not block the micro-heater and the sensing membrane element during detection. Thus, the sensing membrane element and the micro-heater are fully exposed the change of its environment.

WO 2015/178754 A1

Published:

— *with international search report (Art. 21(3))*

ISFET INTEGRATED WITH A MICRO-HEATER AND FABRICATION METHOD THEREOF

TECHNICAL FIELD OF THE INVENTION

This invention relates to a device for gas sensing application, more particularly to a device comprising an ion-selective field-effect transistor (ISFET) with a micro-heater.

BACKGROUND OF THE INVENTION

Micro-electromechanical system (MEMS) is a technology that has been improving over the past decades. MEMS researchers have demonstrated a large interest in one of the most notable elements of MEMS that is the microsensors and applying them in almost every possible sensing modality including temperature, pressure, inertial forces, chemical species, magnetic fields, and radiation. Not only is the performance of MEMS devices exceptional, but the cost production per-device is relatively low.

One of the applications of MEMS is in sensor-driven heating and cooling system. MEMS technology plays an important role in producing chemical and gas micro-sensors where an elevated temperature heating platform is required to improve the sensitivity of a device.

Field effect transistor (FET) device has been used as a gas sensing system. However, a higher temperature is still required to improve the sensitivity of the device against the environment it is in. In order to improve the FET device, many prior arts have come up with the idea of integrating a heating element into the device and that should be able to increase the sensitivity of the sensing membrane towards the environment. However, there are shortcomings in some of these inventions disclosed in the prior arts.

For example, in US patent 5,693,545 and US patent 6,028,331, the sensing membrane element and the heating element are separated by an air gap. The air gap may cause the sensing membrane element to be exposed to possible chemical etchant produced when sacrificial layer of the device is removed. Such occurrence may potentially damage the sensing membrane element.

Furthermore, in US patent 5,693,545, the heating element is formed directly above the sensing membrane element and the exposed surface of the heating element and the sensing membrane element are facing each other. This configuration will partially block the sensing membrane element and reduce the performance of the sensing membrane.

Micro-heater is an example of device used as a heating element. The micro-heater usually comes with a metal oxide sensing membrane that is able to detect the changes in the environment including gaseous ions. It is an improvement to the existing prior arts if the FET device can be integrated with a micro-heater to increase the level of sensitivity of the device as a sensor.

However, there are also some prior arts, for example in EP 0140460 B1 and US patent 6,387,724 B1, both inventions do not have a heating element in their proposed devices.

The prior arts demonstrated different ways to improve on the existing FET devices. However, none of them is able to provide a FET device with a heating element that can perform optimally in the environment. It is therefore a need to improve the existing FET devices to have a higher sensitivity towards the environment and to be able to detect the changes in the environment quickly and efficiently without blocking the sensing membrane element and the heating element.

Accordingly, it can be seen in the prior arts that there exists a need to provide a method for fabricating an ISFET device integrated with a heating element, particularly a micro-heater.

SUMMARY OF THE INVENTION

The present invention is generally related to a method for fabricating a device used in gas sensing applications. Said method involves a device comprises an ion-selective field-effect transistor (ISFET) integrated with a micro-heater.

It provides a fabrication method which allows optimum efficiency for the ISFET and micro-heater to operate without blocking the sensing membrane layer of the ISFET. The fabrication method of the present invention includes the bonding of two silicon substrates to form a device for gas sensing.

Accordingly, this may be achieved in accordance with a preferred embodiment of the present invention a method for fabricating a device for gas sensing application comprising an ion-selective field effect transistor (ISFET) integrated with a micro-heater, the method is characterized by the steps of: providing an active silicon substrate; doping the active silicon substrate to form a source region and a drain region; forming a gate oxide layer on a surface of the active silicon substrate layering above the source region and the drain region; forming a first sensing membrane layer on the gate oxide layer; preparing a handle silicon substrate with a field oxide layer on a surface of the handle silicon substrate; inverting the active silicon substrate to bind the first sensing membrane layer of the active silicon substrate to the field oxide layer of the handle silicon substrate; thinning the active silicon substrate; depositing an insulation layer on an exposed top surface of the active silicon substrate; depositing an oxide layer on a bottom surface of the handle silicon substrate; etching the insulation layer to form a pair of openings for providing an electrical contact pad access to each of the source region and the drain region ; depositing the micro-heater on the insulation layer; forming a cavity at the bottom of the handle silicon substrate exposing the first sensing membrane layer of the active silicon substrate, and wherein the cavity is on opposing side of the micro-heater; forming a second sensing membrane layer in the cavity, wherein the second

sensing membrane layer is in contact with the first sensing membrane layer; and depositing a passivation layer on the micro-heater.

Further in accordance with a preferred embodiment of the present invention, the first sensing membrane is a nitride sensing membrane layer; and the second sensing membrane is a metal oxide sensing membrane layer.

The present invention also provides a device for gas sensing application wherein the sensing membrane layer is optimally exposed to the environment while reducing the risk of damaging the sensing membrane element. It is an objective of the present invention that the sensing membrane layer is not blocked by any structure of the device. The device of the present invention has a configuration of two silicon substrates and a micro-heater.

Accordingly, this may be achieved in accordance with a preferred embodiment of the present invention, a device for gas sensing application comprising an ion-selective field effect transistor (ISFET) integrated with a micro-heater, the device is characterised by: the ISFET further comprising: an active silicon substrate; an insulation layer on a top surface of the active silicon substrate; a gate oxide layer at the bottom of the active silicon substrate; a nitride sensing membrane layer at the bottom of the gate oxide layer; a doped source region on the gate oxide layer; a doped drain region on the gate oxide layer; a pair of openings etched on the active silicon substrate for providing an electrical contact pad access to each of the source region and the drain region; a handle silicon substrate; a field oxide layer between the nitride sensing membrane layer and the handle silicon substrate; an oxide layer on the bottom of the handle silicon substrate; a cavity at the bottom of the handle silicon substrate exposing the nitride sensing membrane layer; a metal oxide sensing membrane layer in the cavity which is in contact with the nitride sensing membrane layer of the active silicon substrate; and the micro-heater further comprising: a passivation layer on the micro-heater; and wherein the micro-heater is deposited on the insulation layer and on opposing side of the cavity of the handle silicon substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention will be more readily understood and appreciated from the following detailed description when read in conjunction with the accompanying drawings of the preferred embodiment of the present invention, in which:

Figure 1A shows a schematic side sectional view of the ISFET with a source region and a drain region on an active silicon substrate;

Figure 1B shows a schematic side sectional view of the layering on the active silicon substrate;

Figure 1C shows a schematic side sectional view of the active silicon substrate and a handle silicon substrate;

Figure 1D shows a schematic side sectional view of the ISFET with an insulation layer on an exposed top surface of the active silicon substrate and an oxide layer on a bottom surface of the handle silicon substrate;

Figure 1E shows a schematic side sectional view of the ISFET with a pair of openings for providing an electrical contact pad access with the source region and drain region;

Figure 1F shows a schematic side sectional view of the micro-heater on the ISFET;

Figure 1G shows a schematic side sectional view of the ISFET with a cavity at the bottom of the handle silicon substrate;

Figure 1H shows a schematic side sectional view of a second sensing membrane deposited in the cavity of the handle silicon substrate;

Figure 1J shows a schematic side sectional view of a passivation layer on the micro-heater; and

Figure 2 shows a schematic side sectional view of a device comprising the ISFET and the micro-heater according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The above mentioned and other features and objects of this invention will become more apparent and better understood by reference to the following detailed description. It should be understood that the detailed description made known below is not intended to be exhaustive or to limit the invention to the precise disclosed form as the invention may assume various alternative forms. On the contrary, the detailed description covers all the relevant modifications and alterations made to the present invention, unless the claims expressly state otherwise.

The present invention relates to a method for fabricating a device for gas sensing application comprising an ion-selective field effect transistor (ISFET) integrated with a micro-heater (130), the method is characterized by the steps of: providing an active silicon substrate (110); doping the active silicon substrate (110) to form a source region (111) and a drain region (112) (Figure 1A); forming a gate oxide layer (113) on a surface of the active silicon substrate (110) layering above the source region (111) and the drain region (112) (Figure 1B);forming a first sensing membrane layer (114) on the gate oxide layer (113) (Figure 1B); preparing a handle silicon substrate (120) with a field oxide layer (121) on a surface of the handle silicon substrate (120); inverting the active silicon substrate (110) to bind the first sensing membrane layer (114) of the active silicon substrate (110) to the field oxide layer (121) of the handle silicon substrate (120) (Figure 1C); thinning the active silicon substrate (110) (Figure 1D); depositing an insulation layer (115) on an exposed top surface of the active silicon substrate (110) (Figure 1D); depositing an oxide layer (122) on a bottom surface of the

handle silicon substrate (120) (Figure 1D); etching the insulation layer (115) to form a pair of openings for providing an electrical contact pad (116) access to each of the source region (111) and the drain region (112) (Figure 1E); depositing the micro-heater (130) on the insulation layer (115) (Figure 1F); forming a cavity at the bottom of the handle silicon substrate (120) exposing the first sensing membrane layer (114) of the active silicon substrate (110), and wherein the cavity is on opposing side of the micro-heater (130) (Figure 1G); forming a second sensing membrane layer (123) in the cavity, wherein the second sensing membrane layer (123) is in contact with the first sensing membrane layer (114) (Figure 1H); and depositing a passivation layer (131) on the micro-heater (130) (Figure 1H).

In an embodiment of the present invention, the active silicon substrate (110) is doped by performing diffusion method or implantation method to form the source region (111) and the drain region (112).

In the method of the present invention, the first sensing membrane layer (114) is a nitride sensing membrane layer (114A) deposited on the active silicon substrate (110) using chemical vapour deposition method.

In a further embodiment of the present invention, the active silicon substrate (110) is thinned by a combination of grinding and chemical-mechanical polishing (CMP) method, or a combination of plasma etching and wet chemical etching process.

In an embodiment of the present invention, the step of forming the cavity at the bottom of the handle silicon substrate (120) involves only a portion of the handle silicon substrate (120) and the oxide layer (122) being etched. The etching goes up to the field oxide layer (121) and expose a portion of the first sensing membrane layer (114) of the active silicon substrate (110). The formation of the cavity which is on the opposing side of the micro-heater (130) allows optimum detection and exposure of the first sensing membrane layer (114) to the environment. During the formation of the cavity, the oxide layer (122) may act as

an etching mask. After the formation of the cavity, the oxide layer (122) that is not etched may also act as an insulator.

In another embodiment of the present invention, the second sensing membrane layer (123) is a metal oxide sensing membrane layer (123A) formed in the cavity through radio frequency (RF) sputtering method. The step of depositing the second sensing membrane layer (123) is performed towards the end of the method to eliminate any possibility of damaging the second sensing membrane layer (123) possibly by chemical etchants produced throughout the method.

The passivation layer (131) described in the method is preferably comprising a silicon dioxide layer or a silicon nitride layer. The formation of the passivation layer (131) on the micro-heater (130) is may be performed by using radio frequency (RF) sputtering method or plasma enhanced chemical deposition method.

The micro-heater (130) which is on opposing side of the second sensing membrane layer (123) allows the exposing surface of the micro-heater (130) and the second sensing membrane layer (123) to be fully exposed to its environment for detection. Furthermore, the micro-heater (130) and the second sensing membrane layer (123) are not blocked by any structure and does not have air gap to separate them. This feature helps to increase the sensitivity of the micro-heater (130) and the second sensing membrane layer (123) to its environment and ensures optimum performance of the device.

Referring to Figure 2, it is also disclosed in accordance to an embodiment of the present invention, a device for gas sensing application comprising an ion-selective field effect transistor (ISFET) integrated with a micro-heater (130), the device is characterised by: the ISFET further comprising: an active silicon substrate (110); an insulation layer (115) on a top surface of the active silicon substrate (110); a gate oxide layer (113) at the bottom of the active silicon substrate (110); a nitride sensing membrane layer (114A) at the bottom of the gate oxide layer (113); a doped source region (111) on the gate oxide layer (113);

a doped drain region (112) on the gate oxide layer (113); a pair of openings etched on the active silicon substrate (110) for providing an electrical contact pad (116) access to each of the source region (111) and the drain region (112); a handle silicon substrate (120); a field oxide layer (121) between the nitride sensing membrane layer (114A) and the handle silicon substrate (120); an oxide layer (122) on the bottom of the handle silicon substrate (120); a cavity at the bottom of the handle silicon substrate (120) exposing the nitride sensing membrane layer (114A); a metal oxide sensing membrane layer (123A) in the cavity which is in contact with the nitride sensing membrane layer (114A) of the active silicon substrate (110); and the micro-heater (130) further comprising: a passivation layer (131) on the micro-heater (130); and wherein the micro-heater (130) is deposited on the insulation layer (115) and on opposing side of the cavity of the handle silicon substrate (120).

In an embodiment of the device disclosed in the present invention, the micro-heater (130) has a coiled or a serpentine wired structure. Furthermore, the micro-heater (130) in the device is able to withstand a temperature of above 400°C, which is suitable to be used in gas sensing applications.

Although the present invention has been described with reference to specific embodiments, it will be apparent for those skilled in the art that many variations and modifications can be done within the scope of the invention as described in the specification and defined in the following claims.

CLAIMS

1) A method for fabricating a device for gas sensing application comprising an ion-selective field effect transistor (ISFET) integrated with a micro-heater (130), the method is characterized by the steps of:

a) providing an active silicon substrate (110);

b) doping the active silicon substrate (110) to form a source region (111) and a drain region (112);

c) forming a gate oxide layer (113) on a surface of the active silicon substrate (110) layering above the source region (111) and the drain region (112);

d) forming a first sensing membrane layer (114) on the gate oxide layer (113);

e) preparing a handle silicon substrate (120) with a field oxide layer (121) on a surface of the handle silicon substrate (120);

f) inverting the active silicon substrate (110) to bind the first sensing membrane layer (114) of the active silicon substrate (110) to the field oxide layer (121) of the handle silicon substrate (120);

g) thinning the active silicon substrate (110);

h) depositing an insulation layer (115) on an exposed top surface of the active silicon substrate (110);

i) depositing an oxide layer (122) on a bottom surface of the handle silicon substrate (120);

j) etching the insulation layer (115) to form a pair of openings for providing an electrical contact pad (116) access to each of the source region (111) and the drain region (112);

k) depositing the micro-heater (130) on the insulation layer (115);

l) forming a cavity at the bottom of the handle silicon substrate (120) exposing the first sensing membrane layer (114) of the active silicon substrate (110), wherein the cavity is on opposing side of the micro-heater (130);

m) forming a second sensing membrane layer (123) in the cavity, wherein the second sensing membrane layer (123) is in contact with the first sensing membrane layer (114); and

n) depositing a passivation layer (131) on the micro-heater (130).

2) A method, according to claim 1, wherein the active silicon substrate (110) is doped by performing diffusion method or implantation method to form the source region (111) and the drain region (112).

3) A method, according to claim 1, wherein the gate oxide layer (113) is deposited on the surface of the active silicon substrate (110) by performing thermal oxidation.

4) A method, according to claim 1, wherein the first sensing membrane layer (114) is a nitride sensing membrane layer (114A) deposited on the active silicon substrate (110) using chemical vapour deposition method.

5) A method according to claim 1, wherein the active silicon substrate (110) is thinned by a combination of grinding and chemical-mechanical polishing (CMP) method, or a combination of plasma etching and wet chemical etching process.

6) A method according to claim 1, wherein the second sensing membrane layer (123) is a metal oxide sensing membrane layer (123A) formed in the cavity through radio frequency (RF) sputtering method.

7) A method, according to claim 1, wherein the passivation layer (131) comprises a silicon dioxide layer or a silicon nitride layer, formed on the micro-heater (130) by using radio frequency (RF) sputtering method or plasma enhanced chemical deposition method.

8) A device for gas sensing application comprising an ion-selective field effect transistor (ISFET) integrated with a micro-heater (130), the device is characterised by:

a) the ISFET further comprising:

i) an active silicon substrate (110);

ii) an insulation layer (115) on a top surface of the active silicon substrate (110);

iii) a gate oxide layer (113) at the bottom of the active silicon substrate (110);

iv) a nitride sensing membrane layer (114A) at the bottom of the gate oxide layer (113);

v) a doped source region (111) on the gate oxide layer (113);

vi) a doped drain region (112) on the gate oxide layer (113);

vii) a pair of openings etched on the active silicon substrate (110) for providing an electrical contact pad (116) access to each of the source region (111) and the drain region (112);

viii) a handle silicon substrate (120);

ix) a field oxide layer (121) between the nitride sensing membrane layer (114A) and the handle silicon substrate (120);

x) an oxide layer (122) on the bottom of the handle silicon substrate (120);

xi) a cavity at the bottom of the handle silicon substrate (120) exposing the nitride sensing membrane layer (114A);

xii) a metal oxide sensing membrane layer (123A) in the cavity which is in contact with the nitride sensing membrane layer (114A) of the active silicon substrate (110); and

b) the micro-heater (130) further comprising:

i) a passivation layer (131) on the micro-heater (130), wherein the micro-heater (130) is deposited on the insulation layer (115) and on opposing side of the cavity of the handle silicon substrate (120).

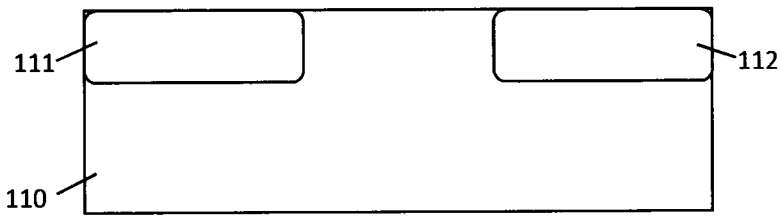

Figure 1A

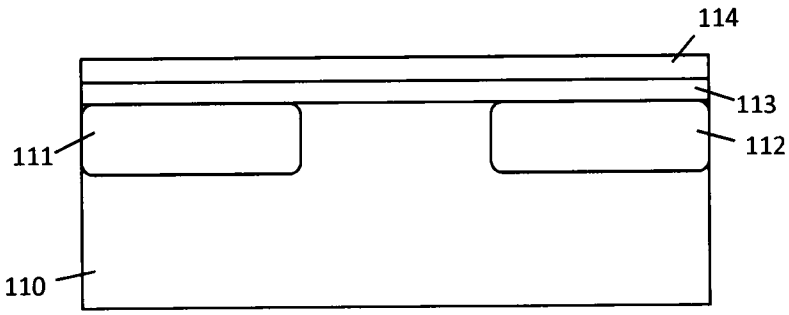

Figure 1B

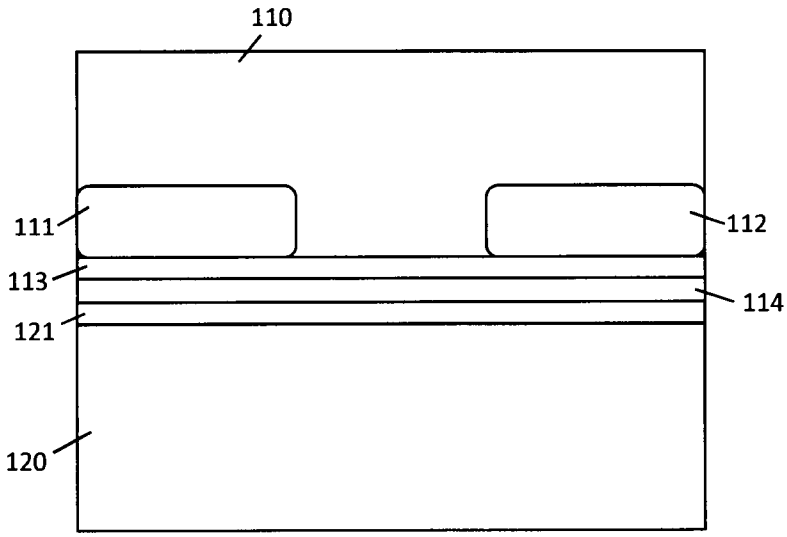

Figure 1C

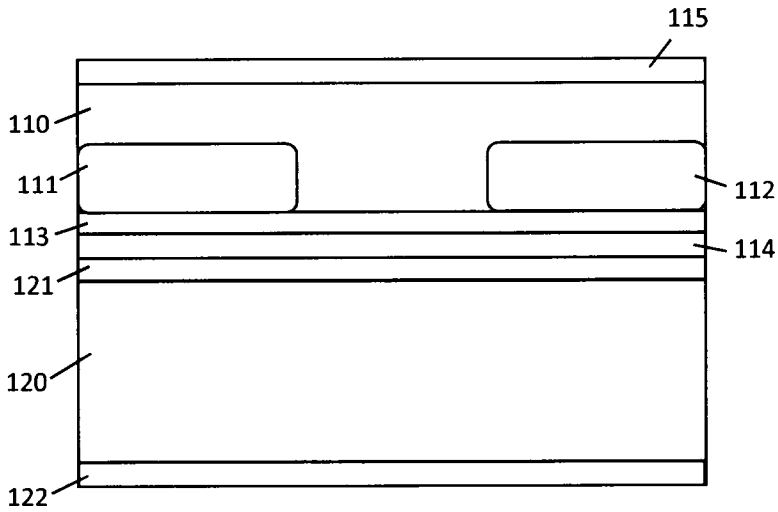

Figure 1D

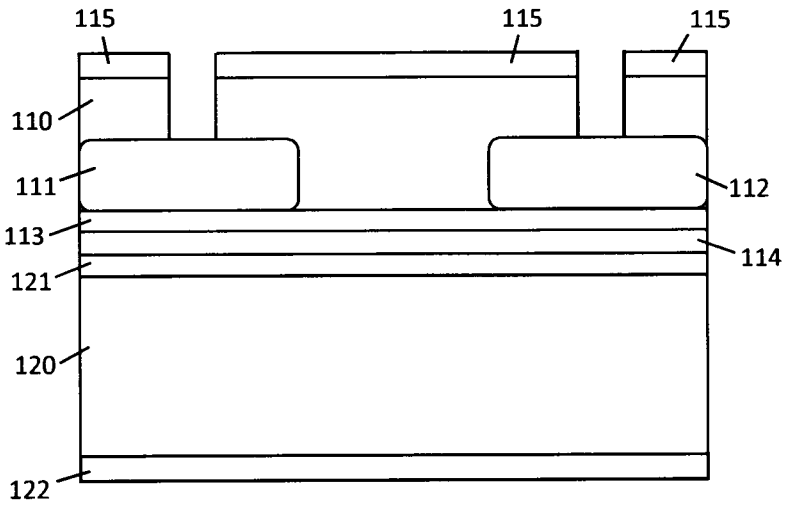

Figure 1E

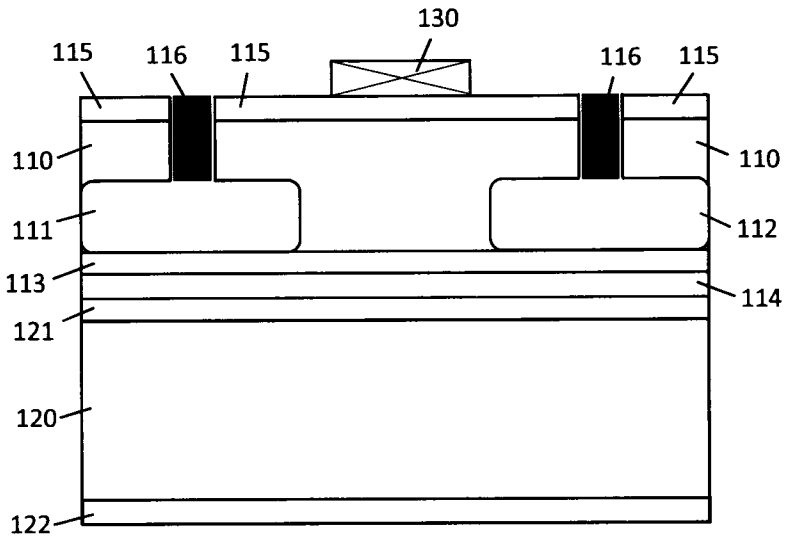

Figure 1F

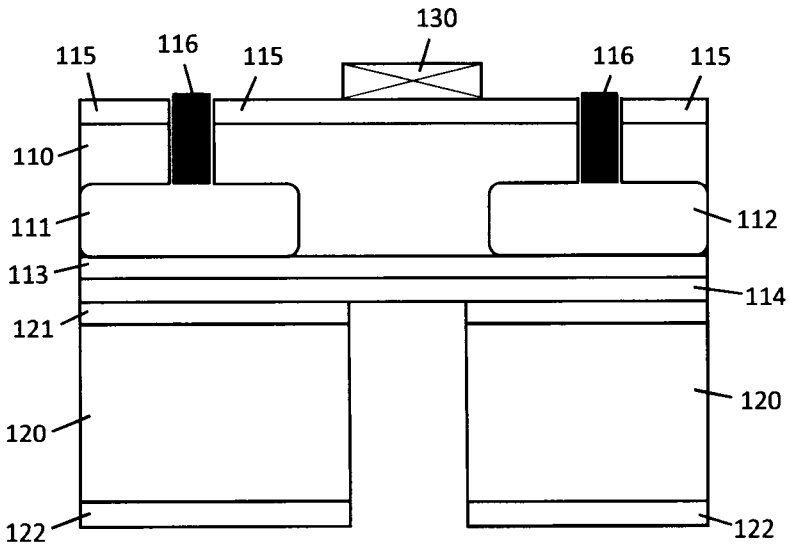

Figure 1G

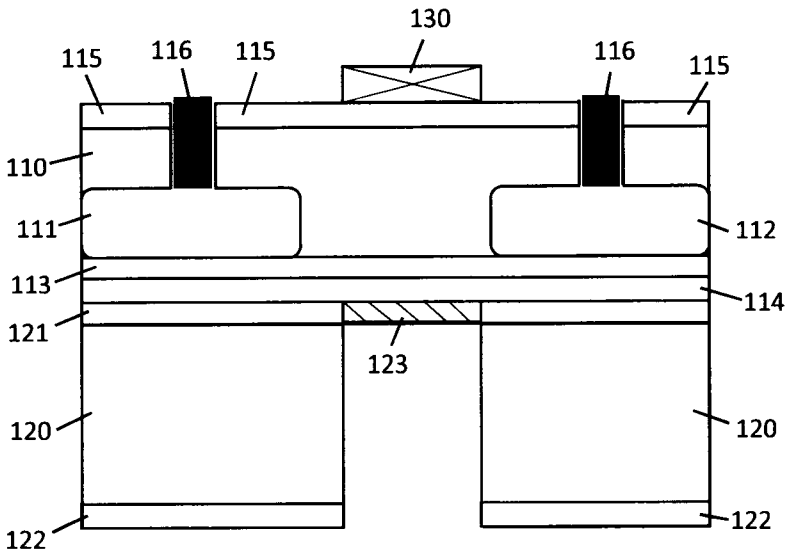

Figure 1H

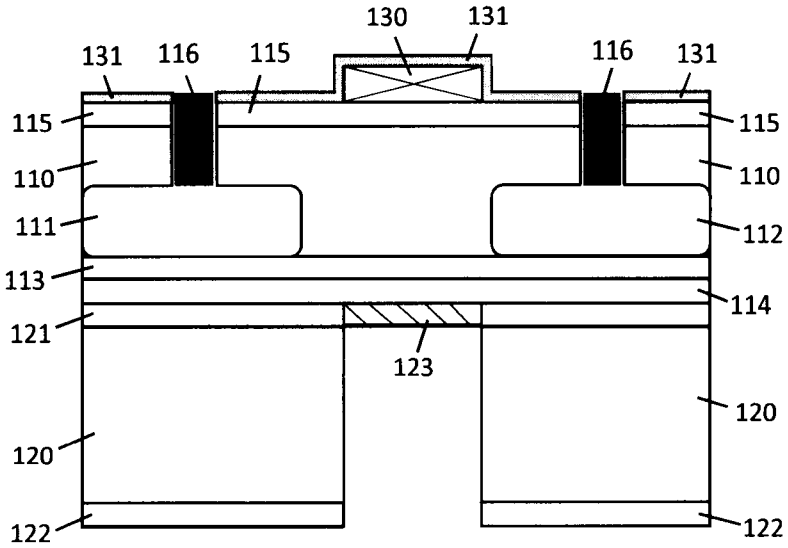

Figure 1J

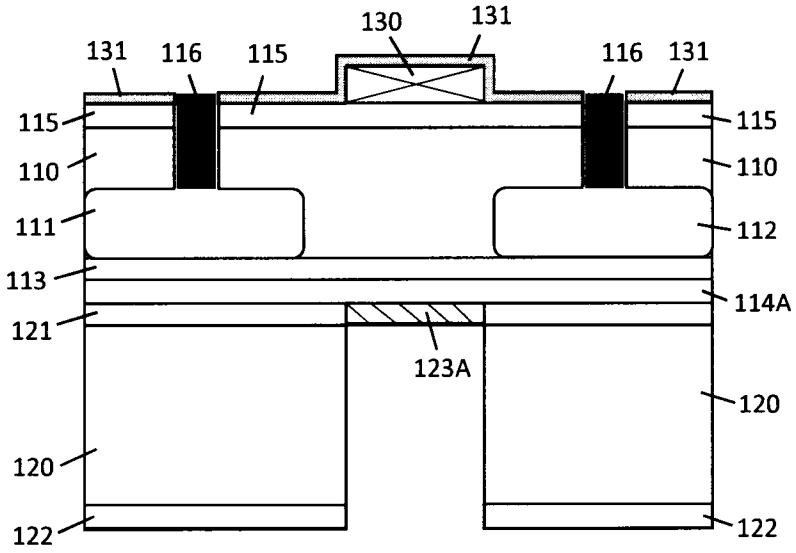

Figure 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2015/000032

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. G01N27/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. G01N27/00-27/49, H01L29/78-29/792

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2015
Registered utility model specifications of Japan 1996-2015
Published registered utility model applications of Japan 1994-2015

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

JSTPlus/JMEDPlus/JST7580 (JDreamIII)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6111280 A (University of Warwick) 2000.08.29, col.6, lines.14-22, Figs.5a,5b & US 6111280 A & WO 1998/032009 A1 & EP 953152 A	1-8
A	WO 2012/118364 A1 (MIMOS BERHAD) 2012.09.07, the whole document (No Family)	1-8
A	JP 2706252 B2 (Japan Science and Technology Corporation) 1998.01.28, the whole document (No Family)	1-8
A	WO 2011/049428 A1 (MIMOS BERHAD) 2011.04.28, the whole document (No Family)	1-8
A	JP 2008-145128 A (Okayama University) 2008.06.26, the whole document (No Family)	1-8

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03.08.2015	18.08.2015

Name and mailing address of the ISA/JP
Japan Patent Office
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer
Yosuke TANAKA
2W 3009
Telephone No. +81-3-3581-1101 Ext. 3250

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2015/000032

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 63-101740 A (Nippon Telegraph and Telephone Corporation) 1988.05.06, the whole document (No Family)	1-8