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(54) **Title:** SEMICONDUCTOR STRUCTURE AND METHOD FOR FORMING THE SAME

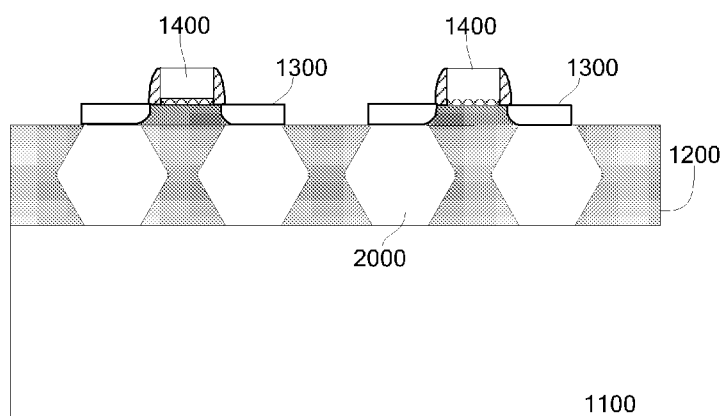


Fig. 1

(57) **Abstract:** A semiconductor structure and a method for forming the same are provided. The semiconductor structure comprises: a substrate (1100); a plurality of convex structures (1200) formed on the substrate (1100), in which every two adjacent convex structures (1200) are separated by a cavity in a predetermined pattern, and the cavity between every two adjacent convex structures (1200) is less than 50nm in width; a plurality of floated films (1300), in which the floated films (1300) are partitioned into a plurality of sets, a channel layer is formed on a convex structure (1200) between the floated films (1300) in each set, a source region and a drain region are formed on two sides of the channel layer respectively, and the cavity between the every two adjacent convex structures (1200) is filled with an insulating material (2000); and a gate stack (1400) formed on each channel layer.



SEMICONDUCTOR STRUCTURE AND METHOD FOR FORMING THE SAME

FIELD

The present disclosure relates to a semiconductor manufacture and design, and
5 more particularly to a semiconductor structure and a method for forming the same.

BACKGROUND

For a long time, in order to achieve a higher chip density, a faster working speed and
a lower power consumption, a feature size of a MOSFET (metal-oxide-semiconductor
10 field effect transistor) is continuously scaled down according to Moore's law, and a
working speed of the MOSFET is faster and faster. Currently, the feature size of the
MOSFET has reached a nanometer level. However, a serious challenge is an emergence
of a short-channel effect, such as a subthreshold voltage roll-off (V_t roll-off), a DIBL
(drain-induced barrier lowering) and a source-drain punch through, thus increasing an
15 off-state leakage current. Therefore, a performance of the MOSFET may be deteriorated.

In addition, a leakage may be alleviated by a SOI (silicon on insulator) structure,
however, a heat conductivity of a SiO_2 insulating material in the SOI structure is low, so
that a heat generated in a channel in a small size device may be difficult to dissipate.
Therefore, a heat dissipation of the SOI structure may be inhibited.

20 Therefore, for a conventional device, large leakage and difficult heat dissipation is a
main constraint for scaling down.

SUMMARY

The present disclosure is aimed to solve at least one of the above mentioned
25 technical problems.

According to an aspect of the present disclosure, a semiconductor structure is
provided. The semiconductor structure comprises: a substrate; a plurality of convex
structures formed on the substrate, wherein every two adjacent convex structures
are separated by a cavity in a predetermined pattern, and the cavity between every
30 two adjacent convex structures is less than 50nm in width; a plurality of floated films,
wherein each floated film is formed between the every two adjacent convex

structures and connected with tops of the every two adjacent convex structures, the floated films are partitioned into a plurality of sets, a channel layer is formed on a convex structure between the floated films in each set, a source region and a drain region are formed on two sides of the channel layer respectively, and the cavity
5 between the every two adjacent convex structures is filled with an insulating material so as to produce a strain in each channel layer; and a gate stack formed on each channel layer.

In one embodiment, a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two
10 adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

In one embodiment, each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $\text{Si}_{1-x}\text{C}_x$ layer, a SiGe layer with high Ge content or a Ge layer.

15 In one embodiment, the plurality of floated films are formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

In one embodiment, the insulating material comprises at least one material selected from a group consisting of Si_xN_y , SiO_2 , and SiO_xN_y .

20 In one embodiment, the insulating material comprises: a first insulating material; and a second insulating material filled between the first insulating material and the convex structures and between the first insulating material and the substrate.

In one embodiment, the first insulating material is Si_xN_y or SiO_xN_y , and the second insulating material is SiO_2 .

25 In one embodiment, the first insulating material is doped with C.

In one embodiment, the semiconductor structure further comprises: a side wall of one or more layers formed on sides of the gate stack.

According to another aspect of the present disclosure, a method for forming a semiconductor structure is provided. The method comprises steps of: providing a
30 substrate; forming a plurality of convex structures on the substrate, wherein every two adjacent convex structures are separated by a cavity in a predetermined pattern,

and the cavity size between every two adjacent convex structures is less than 50nm in width; filling the cavity between the every two adjacent convex structures with an insulating material; forming a semiconductor film on tops of the plurality of convex structures, wherein a first part of the semiconductor film on the cavity is spaced apart
5 from the substrate to form a plurality of floated films, wherein the plurality of floated films are partitioned into a plurality of sets; doping the semiconductor film on a convex structure between the floated films in each set so that a channel layer is formed and the floated films on two sides of the channel layer are set as a source region and a drain region respectively; and forming a gate stack on each channel
10 layer.

In one embodiment, a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

15 In one embodiment, the plurality of floated films are formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

In one embodiment, the method further comprises: etching a second part of the semiconductor film on a convex structure between two adjacent sets of floated films
20 so that the convex structure between two adjacent sets of floated films is used as an isolation portion.

In one embodiment, the method further comprises: forming a side wall of one or more layers on sides of the gate stack.

In one embodiment, the insulating material is at least one material selected from
25 a group consisting of Si_xN_y , SiO_2 , and SiO_xN_y .

In one embodiment, the step of filling the cavity between the every two adjacent convex structures with an insulating material comprises: oxidizing sides of the convex structures and an exposed part of the substrate to form a second insulating material; and forming a first insulating material on the second insulating material by
30 deposition.

In one embodiment, the method further comprises: doping the first insulating material with C (carbon).

In one embodiment, the first insulating material is Si_xN_y or a SiO_xN_y , and the second insulating material is SiO_2 .

5 In one embodiment, the step of forming a semiconductor film on the plurality of convex structures comprises: forming the semiconductor film on the plurality of convex structures by epitaxy.

In one embodiment, the step of forming a plurality of convex structures on the substrate comprises: forming a first semiconductor layer on the substrate; implanting
10 Si or Ge ions into the first semiconductor layer to form an ion-implanted layer in the first semiconductor layer; and selectively etching the first semiconductor layer to form the plurality of convex structures.

According to an embodiment of the present disclosure, the floated films are set as a source region and a drain region respectively. In this way, on one hand, dopants in the
15 source and the drain may be prevented from diffusing into a substrate, so that an ultra-shallow junction may be easy to fabricate. On the other hand, the source and the drain may not contact with the substrate, thus inhibiting band-to-band tunneling (BTBT) leakage between the source and the substrate and between the drain and the substrate. In addition, according to an embodiment of the present disclosure, an insulating material
20 is filled in the cavity between the every two adjacent convex structures so as to produce a strain in each channel layer, thus further improving the performance of the device. Furthermore, parasitic junction capacitance of the source and the drain may be reduced, thus improving the performance of the device. Moreover, with the semiconductor structure according to an embodiment of the present disclosure, the
25 floated films, for example, a $\text{Si}_{1-x}\text{C}_x$ layer, a SiGe layer with high Ge content, a Ge layer, or an III-V group compound semiconductor layer, may be formed, thus improving the performance of the device. Conventionally, if a SOI structure is used, a heat dissipation of a channel may be hindered by an insulating material. However, with the semiconductor structure according to an embodiment of the present disclosure, by using the convex
30 structures as a channel, a problem of inhibiting the heat dissipation of the channel by the insulating material in the SOI structure may be effectively alleviated, and a leakage of the

device may be reduced like the SOI structure, thus improving the performance of the device. In one embodiment, the first insulating material may be doped with C, and a concentration of C is preferably lower than 10%, thus largely improving the strain degree of the convex structures.

5 Additional aspects and advantages of the embodiments of the present disclosure will be given in part in the following descriptions, become apparent in part from the following descriptions, or be learned from the practice of the embodiments of the present disclosure.

10 BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects and advantages of the disclosure will become apparent and more readily appreciated from the following descriptions taken in conjunction with the drawings in which:

Fig. 1 is a cross-sectional view of a semiconductor structure according to an
15 embodiment of the present disclosure;

Fig. 2 is a cross-sectional view of a semiconductor structure according to another embodiment of the present disclosure;

Fig. 3 is a cross-sectional view of a semiconductor structure according to still another embodiment of the present disclosure;

20 Fig. 4 is a cross-sectional view of a semiconductor structure with a common source region or a common drain region according to an embodiment of the present disclosure;

Fig. 5 is a cross-sectional view of a semiconductor structure with a common source region or a common drain region according to another embodiment of the present disclosure; and

25 Fig. 6 is a flow chart of a method for forming a semiconductor structure according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

Embodiments of the present disclosure will be described in detail in the following
30 descriptions, examples of which are shown in the accompanying drawings, in which the same or similar elements and elements having same or similar functions are denoted by

like reference numerals throughout the descriptions. The embodiments described herein with reference to the accompanying drawings are explanatory and illustrative, which are used to generally understand the present disclosure. The embodiments shall not be construed to limit the present disclosure.

5 Various embodiments and examples are provided in the following description to implement different structures of the present disclosure. In order to simplify the present disclosure, certain elements and settings will be described. However, these elements and settings are only examples and are not intended to limit the present disclosure. In addition, reference numerals may be repeated in different examples in the disclosure.

10 This repeating is for the purpose of simplification and clarity and does not refer to relations between different embodiments and/or settings. Furthermore, examples of different processes and materials are provided in the present disclosure. However, it would be appreciated by those skilled in the art that other processes and/or materials may be also applied. Moreover, a structure in which a first feature is "on" a second

15 feature may include an embodiment in which the first feature directly contacts the second feature and may include an embodiment in which an additional feature is prepared between the first feature and the second feature so that the first feature does not directly contact the second feature.

Fig. 1 is a cross-sectional view of a semiconductor structure according to an

20 embodiment of the present disclosure. Fig. 2 is a cross-sectional view of a semiconductor structure according to another embodiment of the present disclosure. The semiconductor structure comprises a substrate 1100; a plurality of convex structures 1200 formed on the substrate 1100, in which every two adjacent convex structures 1200 are separated by a predetermined pattern. In some embodiments, a cavity size between every two adjacent

25 convex structures is less than 50nm in width, preferably, 30 nm. It should be noted that, in some embodiments, the convex structures 1200 may be a vertical structure. However, in other embodiments, as shown in Figs. 1-2, a width of each convex structure 1200 increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two adjacent convex structures 1200 is less than that between

30 middle parts of the two adjacent convex structures 1200. Therefore, a plurality of floated films 1300 may be formed by annealing the convex structures 1200 or by epitaxy. If the

cavity size between top parts of two adjacent convex structures 1200 is less than that between middle parts of the two adjacent convex structures 1200, the cavity size between every two adjacent convex structures is the nearest cavity size between the two adjacent convex structures 1200, i.e., the cavity size between the top parts of the two adjacent convex structures 1200. The semiconductor structure according to an embodiment of the present disclosure may be applied to a small size device, particularly used for alleviating a leakage of a small size device.

The semiconductor structure further comprises a plurality of floated films 1300, in which each floated film 1300 is formed between the every two adjacent convex structures 1200 and connected with tops of the every two adjacent convex structures 1200, the floated films 1300 are partitioned into a plurality of sets, a channel layer is formed on a convex structure 1200 between the floated films 1300 in each set, and a source region and a drain region are formed on two sides of the channel layer respectively. The semiconductor structure further comprises a gate stack 1400 formed on each channel layer. The gate stack 1400 comprises a gate dielectric layer and a gate electrode, for example, a high k gate dielectric layer. In this embodiment, two independent semiconductor structures are shown, each semiconductor structure forms a device, and the two devices are isolated from each other. Particularly, a convex structure 1200 between two adjacent sets of floated films 1300 is an isolation portion. In some embodiments, there are two floated films 1300 in each set. In some embodiments, the floated films 1300 are very thin, and are below about 10nm, and consequently may be used for fabricating an ultra-shallow junction.

In one embodiment, an insulating material 2000 is filled in the predetermined pattern between the every two adjacent convex structures so as to produce a strain in each channel layer. Particularly, the insulating material 2000 may be at least one material selected from a group consisting of Si_xN_y , SiO_2 , and SiO_xN_y . For example, the insulating material 2000 may be Si_xN_y . In one embodiment, the first insulating material is doped with C, and a concentration of C is preferably lower than 10%, thus largely improving the strain degree of the convex structures.

In one preferred embodiment, the insulating material 2000 comprises a first insulating material and a second insulating material. The second insulating material

is filled between the first insulating material and the convex structures 1200 and between the first insulating material and the substrate 1100, that is, the second insulating material surrounds the first insulating material. In one embodiment, the first insulating material is Si_xN_y or SiO_xN_y , and the second insulating material is SiO_2 .

5 Preferably, because Si_xN_y is active, SiO_2 is used to surround the Si_xN_y .

In one embodiment, the substrate 1100 is a Si substrate or a SiGe substrate with low Ge content, and each floated film 1300 is a $\text{Si}_{1-x}\text{C}_x$ layer, a SiGe layer with high Ge content or a Ge layer. In another embodiment, if the floated films 1300 are formed by epitaxy, each floated film 1300 may also be an III-V group compound semiconductor
10 layer.

In some embodiments, the plurality of floated films 1300 may be formed by annealing the plurality of convex structures 1200. In some embodiments, the annealing is performed at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen to migrate atoms on surfaces of the plurality of convex
15 structures 1200. Since the ambient contains hydrogen, hydrogen may effectively facilitate a migration of atoms on surfaces of the plurality of convex structures 1200. Preferably, when the material forming each convex structure 1200 comprises SiGe with high Ge content or Ge, the ambient further comprises at least one gas selected from a group consisting of SiH_4 , GeH_4 , SiH_2Cl_2 , and SiHCl_3 . A small amount of Si and/or Ge
20 atoms are deposited on the surface of the floated films 1300 by decomposing the at least one gas, so that the surface of the floated films 1300 may be flattened, and a required flatness is achieved. After the annealing, the top parts of two adjacent convex structures 1200 may be connected with each other to form the floated films 1300. In this embodiment, the higher the content of Ge in the floated films 1300, the lower the
25 annealing temperature is. For example, if the floated films 1300 are a Ge layer, the annealing temperature may be 300 degrees Celsius.

In another embodiment, each convex structure 1200 comprises a bottom layer and a top layer. Fig. 3 is a cross-sectional view of a semiconductor structure according to still another embodiment of the present disclosure. In some embodiments, the bottom
30 layer is a Si layer, and the top layer is a $\text{Si}_{1-x}\text{C}_x$ layer, a SiGe layer with high Ge content or a Ge layer. For example, as shown in Fig. 3, in each convex structure 1200, the

bottom layer is a SiGe layer with low Ge content, and the top layer is a Ge layer. In this way, the SiGe layer with low Ge content may be used as a buffer layer between the substrate 1100 and the Ge layer.

In one embodiment, the semiconductor structure further comprises a side wall of one or more layers formed on sides of the gate stack 1400. Therefore, an interface layer between the channel layer and the source region and another interface layer between the channel layer and the drain region may extend to the convex structures, thus improving interfacial characteristics of a junction and further improving a performance of a device.

In other embodiments, a semiconductor structure with a common source region and a common drain region may also be formed, as shown in Figs. 4-5. In this embodiment, there are three floated films 1300 in each set, and the three floated films 1300 are set as a source region, a drain region and a source region sequentially, or the three floated films 1300 are set as a drain region, a source region and a drain region sequentially.

Fig. 6 is a flow chart of a method for forming a semiconductor structure according to an embodiment of the present disclosure. The method comprises the following steps.

Step S601, a substrate is provided. The substrate is a Si substrate or a SiGe substrate with low Ge content.

Step S602, a plurality of convex structures are formed on the substrate, in which every two adjacent convex structures are separated by a cavity in a predetermined pattern. In some embodiments, the cavity size between every two adjacent convex structures is less than 50nm in width, and preferably, 30nm. A width of each convex structure increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures. Therefore, a floated film may be formed by annealing the convex structures or by epitaxy. Particularly, in some embodiments, at least one first semiconductor layer is formed on the substrate by epitaxy, and then the at least one first semiconductor layer is etched to form the plurality of convex structures, in which the at least one first semiconductor layer is a SiGe layer with high Ge content or a Ge layer. Certainly, in other embodiments, a surface layer of the

substrate is used as the first semiconductor layer, that is, a surface of the substrate is directly etched to form the plurality of convex structures.

Preferably, in order to form the plurality of convex structures shown in Fig. 1, the first semiconductor layer may be etched by an anisotropic wet etching.

5 Alternatively, in another preferred embodiment, Si or Ge ions are implanted into the first semiconductor layer to form an ion-implanted layer in the first semiconductor layer, and then the first semiconductor layer is selectively etched by a dry etching to form the plurality of convex structures. Because crystal structures in the ion-implanted layer are damaged seriously, an etching rate in the ion-implanted layer is greater than that in other
10 parts of the first semiconductor layer, thus forming the plurality of convex structures shown in Fig. 2.

Step S603, an insulating material, for example, Si_xN_y or SiO_2 , is filled in the cavity between the every two adjacent convex structures. In some embodiments, the insulating material is at least one material selected from a group consisting of Si_xN_y ,
15 SiO_2 , and SiO_xN_y . Preferably, sides of the convex structures and an exposed part of the substrate are first oxidized to form a second insulating material, and then a first insulating material is formed on the second insulating material. In one embodiment, the first insulating material is Si_xN_y or SiO_xN_y , for example, Si_xN_y , and the second insulating material is SiO_2 . In one embodiment, the first insulating material is doped
20 with C.

In one embodiment, after the insulating material is formed, excess insulating materials on tops of the convex structures may be removed. In one embodiment, excess insulating materials on tops of the convex structures may be removed, provided that the top parts sealing up of the convex structures is not affected in a subsequent process.

25 Step S604, a semiconductor film is formed on tops of the plurality of convex structures, in which a first part of the semiconductor film on the cavity is spaced apart from the substrate to form a plurality of floated films. The plurality of floated films are partitioned into a plurality of sets. In some embodiments, each floated film is a $\text{Si}_{1-x}\text{C}_x$ layer, a SiGe layer with high Ge content or a Ge layer.

30 In one embodiment, the plurality of floated films may be formed by annealing the plurality of convex structures. In some embodiments, the annealing is performed at a

temperature of 300-1350 degrees Celsius in an ambient containing hydrogen to migrate atoms on surfaces of the plurality of convex structures. Preferably, the ambient further comprises at least one gas selected from a group consisting of SiH_4 , GeH_4 , SiH_2Cl_2 , and SiHCl_3 . A small amount of Si and/or Ge atoms are deposited on the surface of the floated films by decomposing the at least one gas, so that the surface of the floated films may be flattened. In this embodiment, the higher the content of Ge in the floated films 1300, the lower the annealing temperature is. For example, if the floated films 1300 are a Ge layer, the annealing temperature may be 300 degrees Celsius.

In another embodiment, the floated films may also be formed by epitaxy. In this embodiment, the semiconductor film is formed on the plurality of convex structures by epitaxy. In some embodiments, the substrate may be a Si substrate, a $\text{Si}_{1-x}\text{C}_x$ substrate, a SiGe substrate or a Ge substrate with a surface of a crystal orientation (100), in which x is within a range from 0 to 0.1. Because a lateral epitaxial growth rate of the floated films with a certain crystal orientation is not less than a longitudinal growth rate thereof, a gap between top parts of two adjacent convex structures may be quickly sealed up by epitaxial materials. Therefore, the floated films may not contact with the substrate directly, so that a part of the floated film may be spaced apart from the substrate. In another embodiment, if the floated films are formed by epitaxy, the floated films may also be an III-V group compound semiconductor layer. In one embodiment, each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $\text{Si}_{1-x}\text{C}_x$ layer, a SiGe layer with high Ge content or a Ge layer.

In one preferred embodiment, after the annealing or the epitaxy, if the floated films are thick, the floated films may be subjected to an etching or a thinning process.

Step S605, the semiconductor film on a convex structure between the floated films in each set is doped so that a channel layer is formed and the floated films on two sides of the channel layer are set as a source region and a drain region respectively.

Step S606, a gate stack is formed on each channel layer.

In one embodiment, a side wall of one or more layers is formed on sides of the gate stack.

In one embodiment, there are two floated films in each set. In another embodiment, there are three floated films in each set, and the three floated films are set as a source region, a drain region and a source region sequentially, or the three floated films are set as a drain region, a source region and a drain region sequentially.

In one preferred embodiment, a second part of the semiconductor film on a convex structure between two adjacent sets of floated films is etched so that the convex structure between two adjacent sets of floated films is used as an isolation portion.

According to an embodiment of the present disclosure, the floated films are set as a source region and a drain region respectively. In this way, on one hand, dopants in the source and the drain may be prevented from diffusing into a substrate, so that an ultra-shallow junction may be easy to fabricate. On the other hand, the source and the drain may not contact with the substrate, thus inhibiting BTBT leakage between the source and the substrate and between the drain and the substrate. In addition, according to an embodiment of the present disclosure, an insulating material is formed in the cavity between the every two adjacent convex structures so as to produce a strain in each channel layer, thus further improving the performance of the device. Furthermore, parasitic junction capacitance of the source and the drain may be reduced, thus improving the performance of the device. Moreover, with the semiconductor structure according to an embodiment of the present disclosure, the floated films, for example, a $\text{Si}_{1-x}\text{C}_x$ layer, a SiGe layer with high Ge content, a Ge layer, or an III-V group compound semiconductor layer, may be formed, thus improving the performance of the device. Conventionally, if a SOI structure is used, a heat dissipation of a channel may be hindered by an insulating material. However, with the semiconductor structure according to an embodiment of the present disclosure, by using the convex structures as a channel, a problem of inhibiting the heat dissipation of the channel by the insulating material in the SOI structure may be effectively alleviated, and a leakage of the device may be reduced like the SOI structure, thus improving the performance of the device. In one embodiment,

the first insulating material may be doped with C, and a concentration of C is preferably lower than 10%, thus largely improving the strain degree of the convex structures.

Although explanatory embodiments have been shown and described, it would be appreciated by those skilled in the art that changes, alternatives, and modifications all falling into the scope of the claims and their equivalents may be made in the
5 embodiments without departing from spirit and principles of the disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor structure, comprising:

a substrate;

5 a plurality of convex structures formed on the substrate, wherein every two adjacent convex structures are separated by a cavity in a predetermined pattern, and the cavity between every two adjacent convex structures is less than 50nm in width;

a plurality of floated films, wherein each floated film is formed between the every two adjacent convex structures and connected with tops of the every two adjacent
10 convex structures, the floated films are partitioned into a plurality of sets, a channel layer is formed on a convex structure between the floated films in each set, a source region and a drain region are formed on two sides of the channel layer respectively, and the cavity size between the every two adjacent convex structures is filled with an insulating material so as to produce a strain in each channel layer; and

15 a gate stack formed on each channel layer.

2. The semiconductor structure according to claim 1, wherein a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two adjacent convex structures is less than
20 that between middle parts of the two adjacent convex structures.

3. The semiconductor structure according to claim 1, wherein each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer.

25

4. The semiconductor structure according to claim 1, wherein the plurality of floated films are formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

5. The semiconductor structure according to claim 1, wherein the insulating material comprises at least one material selected from a group consisting of Si_xN_y , SiO_2 , and SiO_xN_y .

5 6. The semiconductor structure according to claim 1, wherein the insulating material comprises:

 a first insulating material; and

 a second insulating material filled between the first insulating material and the convex structures and between the first insulating material and the substrate.

10

7. The semiconductor structure according to claim 6, wherein the first insulating material is Si_xN_y or SiO_xN_y , and the second insulating material is SiO_2 .

15 8. The semiconductor structure according to claim 7, wherein the first insulating material is doped with C.

9. The semiconductor structure according to claim 1, further comprising:
 a side wall of one or more layers formed on sides of the gate stack.

20 10. A method for forming a semiconductor structure, comprising steps of:
 providing a substrate;

 forming a plurality of convex structures on the substrate, wherein every two adjacent convex structures are separated by a cavity in a predetermined pattern, and the cavity size between every two adjacent convex structures is less than 50nm in
25 width;

 filling the cavity between the every two adjacent convex structures with an insulating material;

 forming a semiconductor film on tops of the plurality of convex structures, wherein a first part of the semiconductor film on the cavity is spaced apart from the
30 substrate to form a plurality of floated films, wherein the plurality of floated films are partitioned into a plurality of sets;

doping the semiconductor film on a convex structure between the floated films in each set so that a channel layer is formed and the floated films on two sides of the channel layer are set as a source region and a drain region respectively; and

forming a gate stack on each channel layer.

5

11. The method according to claim 10, wherein a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

10

12. The method according to claim 10, wherein the plurality of floated films are formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

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13. The method according to claim 10, further comprising:

etching a second part of the semiconductor film on a convex structure between two adjacent sets of floated films so that the convex structure between two adjacent sets of floated films is used as an isolation portion.

20

14. The method according to claim 10, further comprising:

forming a side wall of one or more layers on sides of the gate stack.

15. The method according to claim 10, wherein the insulating material is at least one material selected from a group consisting of Si_xN_y , SiO_2 , and SiO_xN_y .

25

16. The method according to claim 10, wherein the step of filling the cavity between the every two adjacent convex structures with an insulating material comprises:

oxidizing sides of the convex structures and an exposed part of the substrate to

30 form a second insulating material; and

forming a first insulating material on the second insulating material by deposition.

17. The method according to claim 16, further comprising:

5 doping the first insulating material with C.

18. The method according to claim 16, wherein the first insulating material is Si_xN_y or a SiO_xN_y , and the second insulating material is SiO_2 .

10 19. The method according to claim 10, wherein the step of forming a semiconductor film on the plurality of convex structures comprises:

forming the semiconductor film on the plurality of convex structures by epitaxy.

15 20. The method according to claim 10, wherein the step of forming a plurality of convex structures on the substrate comprises:

forming a first semiconductor layer on the substrate;

implanting Si or Ge ions into the first semiconductor layer to form an ion-implanted layer in the first semiconductor layer; and

20 selectively etching the first semiconductor layer to form the plurality of convex structures.

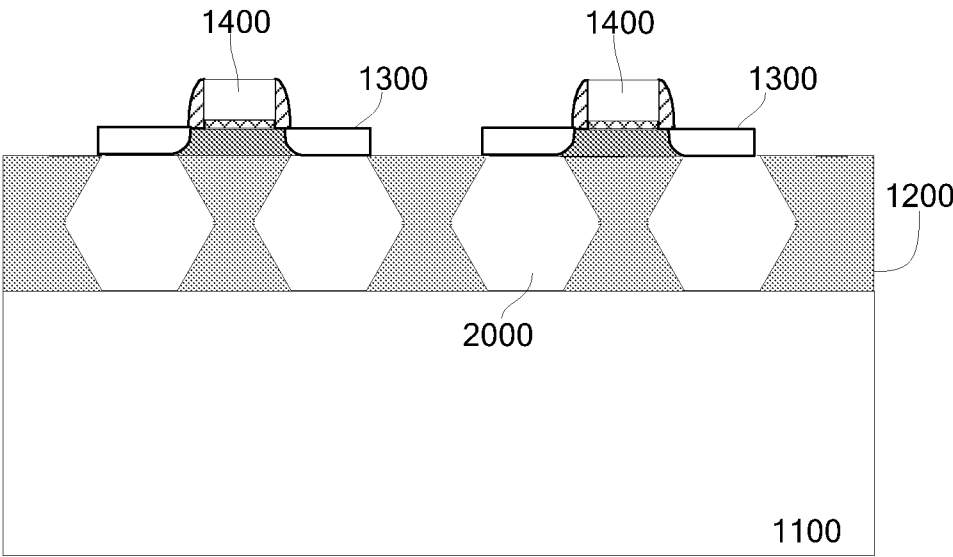


Fig. 1

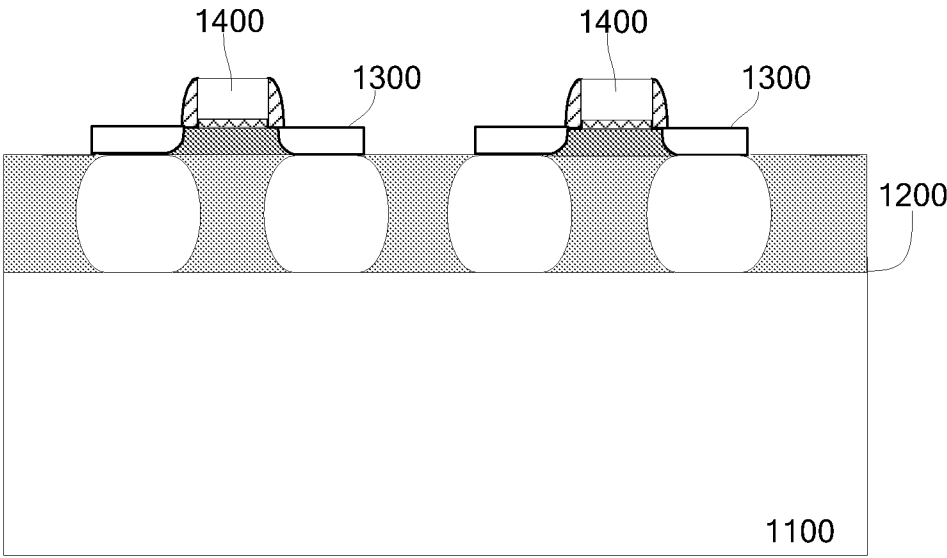


Fig. 2

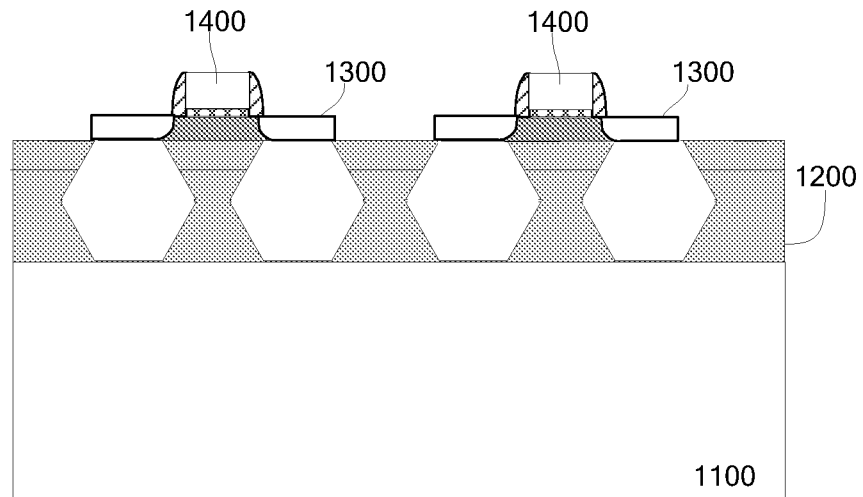


Fig. 3

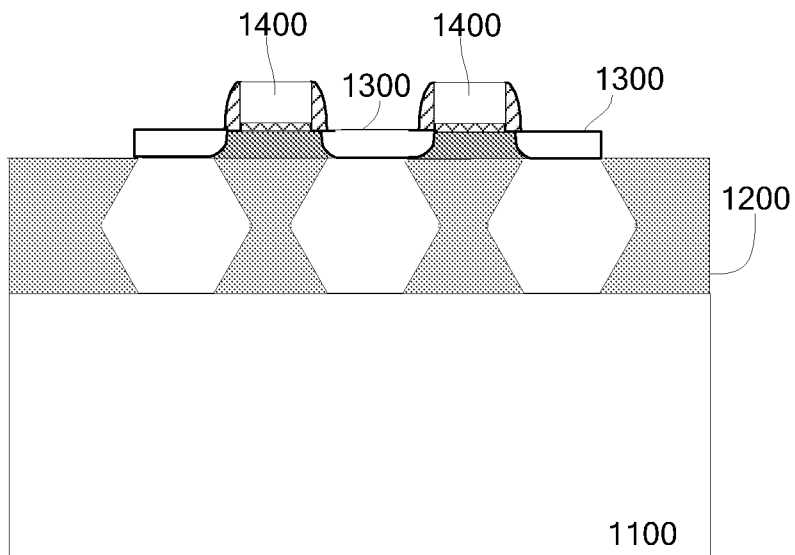


Fig. 4

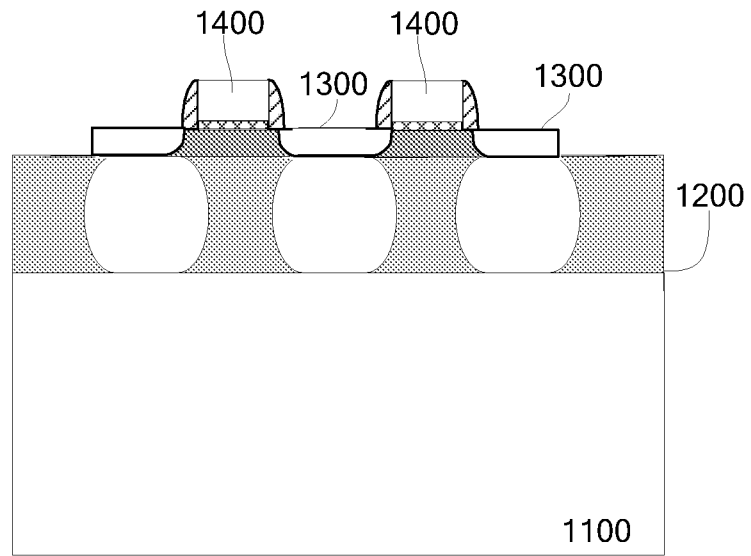


Fig. 5

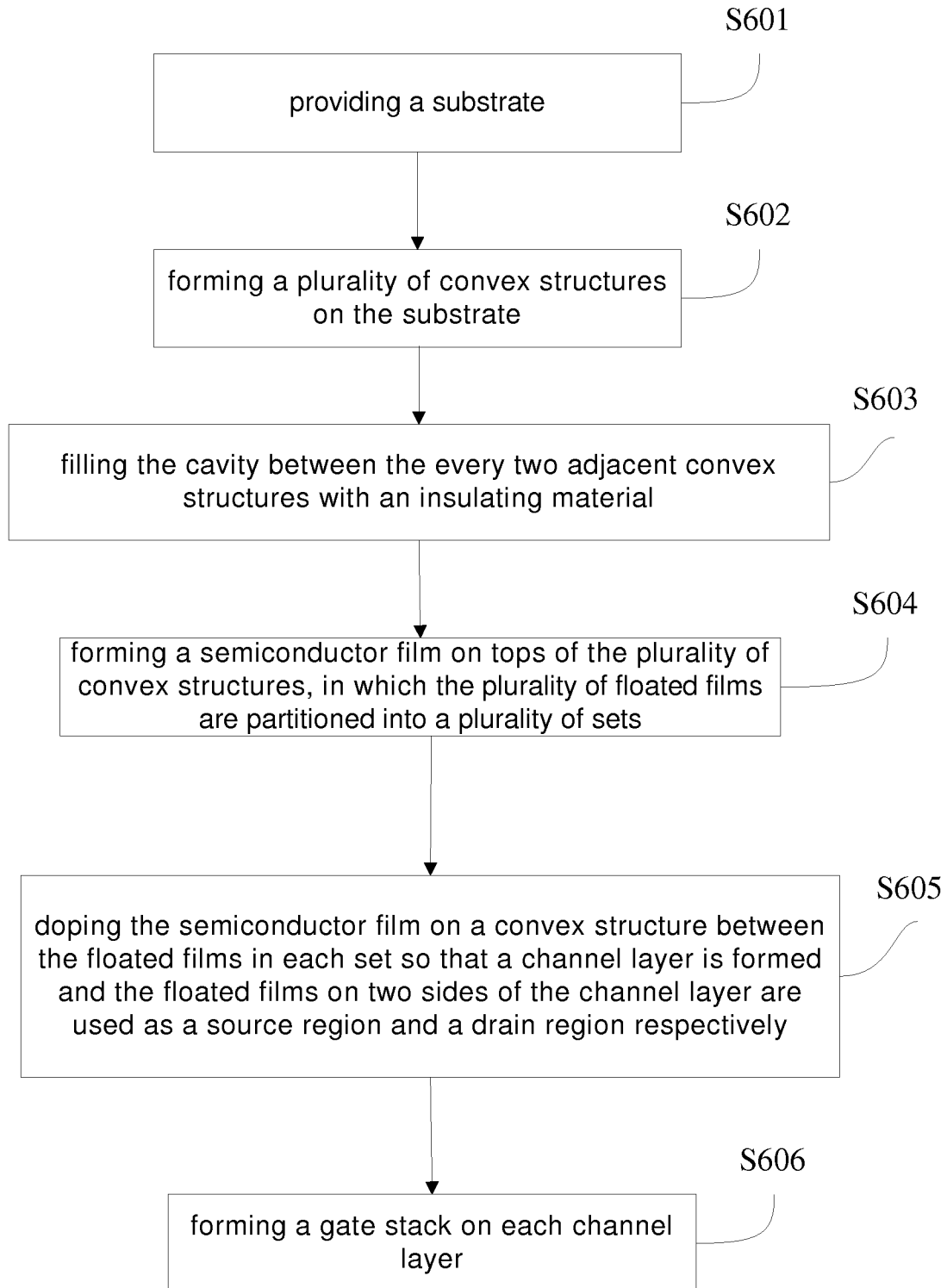


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/082111

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI,CPRS,WPI,EPDOC: convex protrusion cavity trench groove recess gap floated

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN100524653C (IBM CORP) 05 Aug.2009 (05.08.2009) The embodiment of the description, figs. 1-7	1-20
A	CN1906762A (IBM CORP) 31 Jan.2007 (31.01.2007) The whole document	1-20
PX	CN102214684A (UNIV QINGHUA) 12 Oct.2011 (12.10.2011) The whole document	1-20

☒ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“E” earlier application or patent but published on or after the international filing date	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“L” document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	“&” document member of the same patent family
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 24 Feb.2012 (24.02.2012)	Date of mailing of the international search report 08 Mar. 2012 (08.03.2012)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer ZHONG Yi Telephone No. (86-10)62411594

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/082111

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP2290697A1 (STMICROELECTRONICS SRL) 02 Mar.2011 (02.03.2011) The whole document	1-20
A	US2006054969A1 (JANG ET AL) 16 Mar.2006 (16.03.2006) The whole document	1-20

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/082111

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN100524653C	05.08.2009	US2007166900A1	19.07.2007
		CN101005035A	25.07.2007
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CN1906762A	31.01.2007	US2005151193A1	14.07.2005
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US2006054969A1	16.03.2006	JP200608529A	23.03.2006
		KR100555573B1	03.03.2006
		US7592686B2	22.09.2009
CN102214684A	12.10.2011	None	

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/082111

A. CLASSIFICATION OF SUBJECT MATTER

H01L29/06 (2006.01) i

H01L27/088 (2006.01) i

H01L21/8234 (2006.01) i