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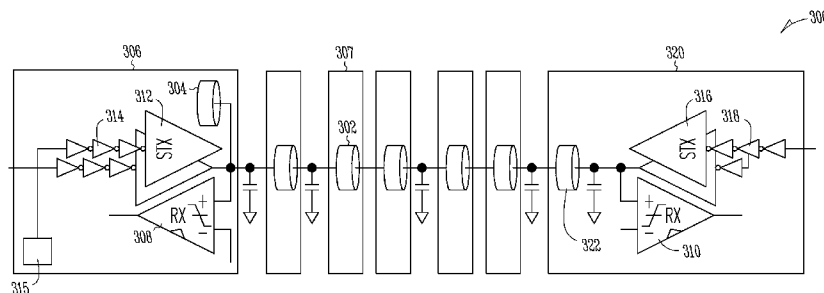


Fig. 3

(57) Abstract: Apparatuses and methods are described that include a plurality of drivers corresponding to a single via. A number of drivers can be selected to operate individually or together to drive a signal through a single via. Additional apparatus and methods are described.

APPARATUSES INCLUDING SCALABLE DRIVERS AND METHODS

5 **Priority Application**

[0001] This application claims the benefit of priority to U.S. Application Serial No. 13/431,674, filed March 27, 2012, which is incorporated herein by reference in its entirety.

10 **Background**

[0002] In semiconductor devices, there is continuous pressure in industry to reduce component dimensions and fit more components in a given amount of chip area. As dimensions shrink, numerous technical hurdles become more significant.

15 **[0003]** In many electronic systems, particularly in mobile systems, there may be competing goals of increasing device speed versus decreasing power consumption. It is desirable to provide reduced power consumption without sacrificing speed. Improved electronic systems are desired to meet these and other challenges with efficient manufacturing processes.

Brief Description of the Drawings

[0004] FIG. 1 shows an isometric view of a semiconductor device according to an embodiment of the invention.

[0005] FIG. 2 shows a cross section of the semiconductor device from
25 Figure 1, along line 2-2 according to an embodiment of the invention.

[0006] FIG. 3 shows a block diagram of a semiconductor device according to an embodiment of the invention.

[0007] FIG. 4 shows a block diagram of another semiconductor device according to an embodiment of the invention.

30 **[0008]** FIG. 5 shows a schematic diagram of an example driver according to an embodiment of the invention.

[0009] FIG. 6 shows a schematic diagram of another example driver according to an embodiment of the invention.

[0010] FIG. 7 shows a schematic diagram of drivers according to an embodiment of the invention.

[0011] FIG. 8 shows an information handling system, including a memory device according to an embodiment of the invention.

5

Detailed Description

[0012] In the following detailed description of various embodiments of the invention, reference is made to the accompanying drawings that form a part hereof and in which are shown, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made.

[0013] Integrated circuits (ICs) may include many devices and circuit members that are formed on a single semiconductor die. The current trends in IC technology are towards faster and more complicated circuits. However, as more complex ICs are manufactured, various speed-related problems become more apparent. This is especially true when ICs having different functions are used to create electronic systems, for example, computing systems including processor and memory ICs, where different ICs are electrically connected by a network of global interconnects. As global interconnects become longer and more numerous in electronic systems, resistive-capacitive (RC) delay and power consumption, as well as system performance, tend to become limiting factors.

[0014] One proposed solution to these problems is three-dimensional (3-D) integration or packaging technology. 3-D integration refers to the vertical stacking of multiple dice (e.g., chips) including ICs within a package. In some 3-D integration technology, multiple dice are coupled (e.g., electrically connected) using through silicon vias (TSVs) that form vertical connectors or 3-D conductive structures. TSVs extend (at least partially) through a thickness of one or more of the dice and may be aligned when the die are stacked to provide electrical communication among the ICs in the stack. Such TSVs are often formed of a conductive material, such as aluminum or copper. 3-D integration

typically results in a reduction of the packaged IC's footprint as well as a reduction in power consumption, and an increase in performance.

[0015] In many electronic systems, including mobile systems, there may be competing goals of increasing device speed and decreasing power consumption. It is sometimes desirable to provide reduced power consumption without sacrificing speed. In some cases, efficient manufacturing processes may be used to help achieve these goals.

[0016] Referring to Figures 1 and 2, an example 3-D IC device will now be described. The illustrated 3-D IC device 100 includes four dice 110a-110d stacked over one another. Although a four die configuration is shown in Figure 1, other configurations may include fewer stacked dice, or more stacked dice, such as 8 stacked dice, for example. The first die 110a is the uppermost die, and the fourth die 110d is the lowermost die. The second and third dice 110b, 110c are interposed between the first and fourth dice 110a, 110d. In other examples, a 3-D IC device can include a greater or lesser number of dice than the device of Figure 1.

[0017] One or more of the first to fourth dice 110a - 110d may include an IC array 112, a transceiver 114, first interconnect lines 116, second interconnect lines 118 and landing pads 130a - 130d. Each of the dice 110a - 110c, may also include vias 120a-120c (Figure 2).

[0018] In silicon examples, the via may be termed a TSV. Although the term TSV refers to dice formed from silicon, one of ordinary skill in the art, having the benefit of the present disclosure, will recognize that other semiconductor materials may be used in fabricating dice, and the term TSV applies to other vertical connectors or 3-D conductive structures that pass at least partially through dice of different materials. In one example, as illustrated in Figure 1, the lowermost die 110d does not include a via. In one example, the lowermost die may include a logic die without vias. In other examples, the lowermost die may include one or more vias.

[0019] The IC array 112 may include one or more integrated circuits, including, but not limited to, one or more memory cells (for example, volatile and/or non-volatile memory cells) and one or more processors. In one example, one or more of the dice 110a - 110d comprises a memory die. Examples of

memory dice include dynamic random access memory (DRAM) dice, static random access memory (SRAM) dice, flash memory dice, resistive random access memory (RRAM) dice etc. 3-D memory configurations using DRAM configurations are advantageous in complex processing operations due to their relative high access and programming speed.

[0020] In one example, one or more of the dice 110a - 110d includes a logic die. One example of a logic die includes a die including processing circuitry, addressing circuitry, or other memory management circuitry. In one example, a logic die does not include a memory array. One example of a 3-D IC device 100 includes a number of stacked memory dice and a single logic die (which may or may not be stacked with the memory dice). In one example, the logic die is located on the edge of the stack of dice, such as to provide easier access to the logic die.

[0021] The first interconnect lines 116 provide data paths between the IC array 112 and the transceiver 114 on a respective one of the dice 110a - 110d. The second interconnect lines 118 provide data paths between the transceiver 114 and the landing pads 130a - 130d of a respective one of the dice 110a - 110d.

[0022] The vias 120a - 120c provide communication paths between the landing pads 130a - 130d of dice 110a - 110d that are stacked immediately next to each other, thereby completing parts of data paths between the IC arrays 112 on the two dice. In certain cases, the vias 120a - 120c of two or more dice 110a - 110d that are stacked over one another are aligned in series, and can together provide serial data paths among the two or more dice.

[0023] Figure 3 shows an example of a block diagram for a stack of eight dice 300 according to an embodiment of the invention. Although eight dice are illustrated in the block diagram configuration, other configurations may include fewer dice or more dice than eight.

[0024] A number of vias 302 are illustrated. Each via 302 corresponds to a die 307 in a stack of semiconductor dice, similar to the stack of dice 110a - 110d shown in Figures 1 and 2. In one example, vias 302 are configured similar to vias 120a-120c from Figures 1 and 2. Via 304 is included in die 306 in the

stack of dice, and is illustrated to be within the same die 306 as drivers 312, pre-drivers 314 and a receiver 308.

[0025] Figure 3 shows a plurality of drivers 312 corresponding to a single via 304 in the die 306. One or more of the drivers 312 are selectable to
5 operate individually or together (e.g., in parallel) to drive a signal through vias 304, 302 to a selected die in the stack of dice 300. A receiver 308 is shown, and is operable to receive a signal from other dice 307 in the stack of dice 300. In one example, the drivers 312 and receiver 308 are located in a transceiver, such as transceiver 114 from Figure 1. The block diagram of Figure 3 is simplified
10 for ease of illustration. Each die 307 may include not only the vias 302, but also drivers and a receiver in a transceiver, such as transceiver 114.

[0026] The example of Figure 3 further shows an embodiment that includes one or more pre-drivers 314. A pre-driver may be coupled to one or more of the drivers 312 to improve speed and/or performance in signal
15 transmission. In one example, one or more pre-drivers 314 are staggered with an associated driver 312 to reduce a slew rate in a signal. In one example, timing for an enable signal for each driver (through the pre-driver) is staggered, which in turn makes the signal transition smoother at a final output. Configurations with slew rate control may reduce overshoot and/or undershoot of the output and
20 improve signaling.

[0027] In one example, a plurality of pre-drivers 314 are associated with a corresponding plurality of drivers 312, in a one-to-one correspondence. In another example, one pre-driver is associated with a plurality of drivers. For example, Figure 3 illustrates a second plurality of drivers 316 in a die 320
25 corresponding to a single via 322. A single pre-driver 318 is associated with the plurality of drivers 316. Similar to die 306, die 320 is also shown with a receiver 310.

[0028] Configurations with a plurality of drivers that correspond to a single via provide flexibility in driving signals in stacks of different numbers of
30 dice. For example, in order to drive a signal in an eight die stack, a driver may be configured to provide enough power to drive the signal through at least seven dice to ensure that the largest possible distance is covered. However, if the same driver configuration is used in a four die stack, the additional power capability is

wasted. A lower power configuration can thus provide power savings in a four die stack. Configurations such as Figures 3 and 4 with a plurality of drivers that correspond to a single via can be configured to use multiple drivers when needed to drive signals in large stacks of dice, and configured to use fewer drivers in smaller stacks of dice when the additional power drive capability is not needed.

[0029] For example, Figure 4 shows an example of a block diagram for a stack of four dice 400 according to an embodiment of the invention. A number of vias 402 are illustrated. Each via 402 corresponds to a die 407 in the stack of semiconductor dice, as in Figure 3. Via 404 is included in die 406 in the stack of dice 400, and is illustrated to be within the same die 406 as drivers 412, pre-drivers 414 and a receiver 408. Similar to Figure 3, in one example, a plurality of pre-drivers 414 are included, with a pre-driver 414 associated with each driver 412 in the plurality of drivers. Also similar to Figure 3, a second plurality of drivers 416 in a die 420 corresponding to a single via 422. A single pre-driver 418 is associated with the plurality of drivers 416. Similar to die 406, die 420 is also shown with a receiver 410.

[0030] In one example, the die 406 is substantially identical to die 306 from Figure 3. The number of drivers 412, 312 that are used can be selected to correspond to power needs in an eight die stack, as in Figure 3, or a four die stack as in Figure 4, or in stacked die configurations with other numbers of dice. A single die configuration can be manufactured, with a selectable number of drivers to meet performance goals, and at the same time reduce power needs to accommodate the number of dice in the stack.

[0031] Returning to Figure 3 as an example, in one embodiment, there are two drivers 312 in the plurality of drivers. In other examples, three or more drivers 312 may be included in the number of drivers. Other numbers of drivers may be included, depending on the degree of flexibility desired for numbers of dice in a stacked die device.

[0032] In one example, the drivers 312 are substantially equal in size.

For example a single driver may be used to drive a signal in a four die stack, and an additional second driver of substantially equal size may be added to the first driver to provide the capability to drive the signal in an eight die stack. In another example, the drivers are not substantially equal in size. For example a

single driver may be used to drive a signal in a two die stack, and an additional second driver of greater size may be added to provide the capability to drive the signal in an eight die stack.

[0033] In one example the plurality of drivers may be in one die within
5 the stack of dice. The die with the plurality of drivers may be a logic die coupled to a plurality of memory dice. In other examples, each die in the stack of dice includes a plurality of drivers as described in embodiments above. One advantage of including a plurality of drivers in each die includes manufacturing efficiency. One physical die configuration can be manufactured, and later
10 electrically configured to use one or more drivers in a plurality of drivers to efficiently power any selected number of dice in a 3-D stacked configuration.

[0034] Figure 3 shows a selector 315 that can be used to select a number of drivers 312 and/or pre-drivers 314. In one example, the selector 315 is actuated at the time of manufacture. In another example, the selector 315 is actuated at
15 power up, for example, using instructions from a host processor (not shown). Figure 4 is shown also including a selector 415 that can be used to select a number of drivers 412 and/or pre-drivers 414. In one example, a single driver is selected by default (e.g., it is configured to be always enabled when in operation), and an additional driver(s) may be selectively added to meet the needs of larger numbers
20 of dice in a stack of dice. In other words, an additional driver is configured to be optionally selected.

[0035] Figure 5 shows one example of a driver 500 that may be used to form a plurality of drivers, as in example configuration such as those shown in Figures 3 or 4. The driver 500 includes a first voltage supply node 502, a second
25 voltage (e.g., ground) supply node 504, and an input 508. The example driver 500 of Figure 5 includes a P channel transistor 510 and an N channel transistor 512 that operate with a single input signal from input 508. A feedback transistor 514 is driven by a feedback circuit 516 to control the voltage at output 506.

[0036] Figure 6 shows an example of another driver 600 that may be
30 used to form a plurality of drivers, as in example configuration such as those shown in Figures 3 or 4. The driver 600 includes a first voltage supply node 602, a second voltage (e.g., ground) supply node 604, a first input 608, and a second input 610. The example driver 600 of Figure 6 uses the first and second inputs

608, 610 to select a high or low signal to be transmitted to an output 606. A feedback transistor 614 is driven by a feedback circuit 616 to control the voltage at output 606.

[0037] Figure 7 shows one example of a plurality of drivers 700,
5 including a first driver 702 and a second driver 704 similar to the driver 600 from Figure 6. The first driver 702 includes a first feedback transistor 706 and the second driver 704 includes a second feedback transistor 708. A number of inputs 714 are used to control the high or low level at the output 712. The inputs 714 are selected by a selector similar to selectors 315, 415 from Figures 3 and 4
10 to turn drivers and/or pre-drivers on or off. A swing level is dictated by feedback circuit 710.

[0038] The configuration of Figure 7 uses a shared feedback circuit 710 coupled to both the first feedback transistor 706 and the second feedback transistor 708. Configurations with a shared feedback circuit 710 may provide
15 greater efficiency of power and reduced circuit real estate on the die.

[0039] As used herein, the term “apparatus” is used to refer to a variety of structures and configurations, including, without limitation, systems, devices, circuitry, chip assemblies, etc. An embodiment of an apparatus such as a computer is included in Figure 8 to show an embodiment of a high-level device
20 application. Figure 8 is a block diagram of an apparatus 800 incorporating at least one 3-D IC device 804 according to an embodiment of the invention. The apparatus 800 shown in Figure 8 is merely one example of a system in which the present invention can be used. Other examples include, but are not limited to, mainframe systems, tablet computers, personal data assistants (PDAs), cellular
25 telephones, MP3 players, aircraft, satellites, military vehicles, etc.

[0040] In this example, apparatus 800 comprises a data processing system that includes a system bus 802 to couple the various components of the system. System bus 802 provides communications links among the various components of the information handling system 800 and may be implemented as
30 a single bus, as a combination of busses, or in any other suitable manner.

[0041] Chip assembly 804 is coupled to the system bus 802. Chip assembly 804 may include any circuit or operably compatible combination of circuits. In one embodiment, chip assembly 804 includes a processor 806 that

can be of any type. As used herein, “processor” means any type of computational circuit such as, but not limited to, a microprocessor, a microcontroller, a graphics processor, a digital signal processor (DSP), or any other type of processor or processing circuit. Multiple processors such as “multi-core” devices are also within the scope of embodiments of the invention.

[0042] In one embodiment, a memory device 807, such as a 3-D semiconductor device described in embodiments above, is included in the chip assembly 804. Those of ordinary skill in the art will recognize that a wide variety of memory device configurations may be used in the chip assembly 804.

Acceptable types of memory chips include, but are not limited to, Dynamic Random Access Memory (DRAMs) such as SDRAMs, SLDRAMs, RRAMs and other DRAMs. Memory chip 807 can also include non-volatile memory such as NAND memory or NOR memory.

[0043] In one embodiment, additional logic chips 808 other than processor chips are included in the chip assembly 804. An example of a logic chip 808 other than a processor includes an analog to digital converter. Other circuits on logic chips 808 such as custom circuits, an application-specific integrated circuit (ASIC), etc. are also included in one embodiment of the invention.

[0044] Apparatus 800 may also include an external memory 811, which in turn can include one or more memory elements suitable to the particular application, such as one or more hard drives 812, and/or one or more drives that handle removable media 813 such as floppy diskettes, compact disks (CDs), digital video disks (DVDs), and the like. A memory constructed as described in examples above is included in the apparatus 800.

[0045] Apparatus 800 may also include a display device 809 such as a monitor, additional peripheral components 810, such as speakers, etc. and a keyboard and/or controller 814, which can include a mouse, or any other device that permits a system user to input information into and receive information from the apparatus 800.

[0046] While a number of embodiments of the invention are described, the above lists are not intended to be exhaustive. Although specific embodiments have been illustrated and described herein, it will be appreciated

by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to

5 be illustrative and not restrictive. Combinations of the above embodiments, and other embodiments, will be apparent to those of skill in the art upon studying the above description.

What is claimed is:

1. An apparatus, comprising a plurality of semiconductor dice, wherein:
at least some of the plurality of semiconductor dice are stacked and
coupled by vias; and
5 at least one of the plurality of semiconductor dice includes a plurality of
drivers corresponding to a single via of the plurality of vias, wherein one or more
of the plurality of drivers are selectable to operate individually or together to
drive a signal through the single via.
- 10 2. The apparatus of claim 1, wherein one driver of the plurality of drivers is
configured to be always enabled when in operation, and an additional driver of
the plurality of drivers is configured to be optionally selected.
3. The apparatus of claim 1, wherein the stacked semiconductor dice
15 includes a plurality of memory dice.
4. The apparatus of claim 3, wherein the stacked semiconductor dice
include a number of dynamic random access memory dice.
- 20 5. The apparatus of claim 1, wherein the stacked semiconductor dice
includes a logic die.
6. The apparatus of claim 1, wherein the plurality of semiconductor dice
includes a logic die, and further including a host processor coupled to the logic
25 die.
7. The apparatus of claim 1, further comprising shared feedback circuitry
between the plurality of drivers.
- 30 8. The apparatus of claim 1, wherein the plurality of drivers are
substantially equal in size.

9. The apparatus of claim 1, wherein one driver of the plurality of drivers is configured to drive the signal in a stack of four dice, and when all of the plurality of drivers are selected, the plurality of drivers are configured to drive the signal in a stack having eight dice.
- 5
10. The apparatus of claim 1, wherein the plurality of drivers is two drivers.
11. An apparatus comprising a stack of memory chips coupled by vias, wherein the apparatus comprises:
- 10 a plurality of drivers corresponding to a single via of the plurality of vias, wherein one or more drivers in the plurality of drivers are selectable to operate individually or together to drive a signal through the via to one or more of the chips in the stack of memory chips; and
- a pre-driver coupled to at least one of the plurality of drivers.
- 15
12. The apparatus of claim 11, wherein the pre-driver is coupled to each driver of the plurality of drivers.
13. The apparatus of claim 11, wherein the pre-driver is staggered to provide
- 20 slew rate control.
14. The apparatus of claim 11, wherein the plurality of drivers is two drivers and the pre-driver comprises two pre-drivers, wherein each of the two pre-drivers is associated with a respective one of the two drivers.
- 25
15. The apparatus of claim 11, wherein the stack of memory chips are coupled with a logic die, wherein the logic die includes the plurality of drivers and the pre-driver.
- 30
16. The apparatus of claim 15, wherein the logic die is stacked with the stack of memory chips.

17. The apparatus of claim 11, wherein the plurality of drivers and the pre-driver are in a memory chip of the stack of memory chips.
18. A semiconductor chip, comprising:
5 a plurality of drivers corresponding to a single via of a plurality of vias, wherein the single via is to pass a signal through at least a portion of a thickness of a semiconductor chip; and
a selector to enable one or more of the plurality of drivers to operate individually or together to drive a signal through the single via.
- 10 19. The semiconductor chip of claim 18, further including a pre-driver associated with each driver in the plurality of drivers.
20. The semiconductor chip of claim 19, wherein the pre-driver is staggered
15 to reduce a slew rate in its associated driver.
21. The semiconductor chip of claim 18, wherein the plurality of drivers comprise two drivers.
- 20 22. The semiconductor chip of claim 18, wherein the plurality of drivers are substantially equal in size.
23. The semiconductor chip of claim 18, wherein the plurality of drivers share feedback circuitry.
- 25 24. A method of operating an apparatus comprising a plurality of semiconductor dice, wherein at least some of the plurality of semiconductor dice are stacked and coupled by vias and at least one of the plurality of semiconductor dice includes a plurality of drivers corresponding to a single via
30 of the plurality of vias, comprising:
selecting one or more of the plurality of drivers to operate individually or together to drive a signal through the single via.

25. The method of claim 24, wherein selecting one or more of the plurality of drivers to operate individually or together to drive a signal through the single via comprises selecting the one or more of the plurality of drivers at a time of manufacture of the apparatus.

5

26. The method of claim 24, wherein selecting one or more of the plurality of drivers to operate individually or together to drive a signal through the single via comprises selecting the one or more of the plurality of drivers at power up of the apparatus.

10

27. The method of claim 24, wherein at least some of the plurality of semiconductor dice that are stacked are memory dice.

28. The method of claim 24, wherein the at least one of the plurality of semiconductor dice is a logic die.

15

29. The method of claim 24, wherein selecting one or more of the plurality of drivers to operate individually or together comprises electrically configuring the plurality of drivers.

20

30. The method of claim 23, wherein selecting one or more of the plurality of drivers to operate individually or together to drive a signal through the single via comprises selecting the one or more of the plurality of drivers to operate individually or together to drive the signal through the single via responsive to instructions received from a host processor.

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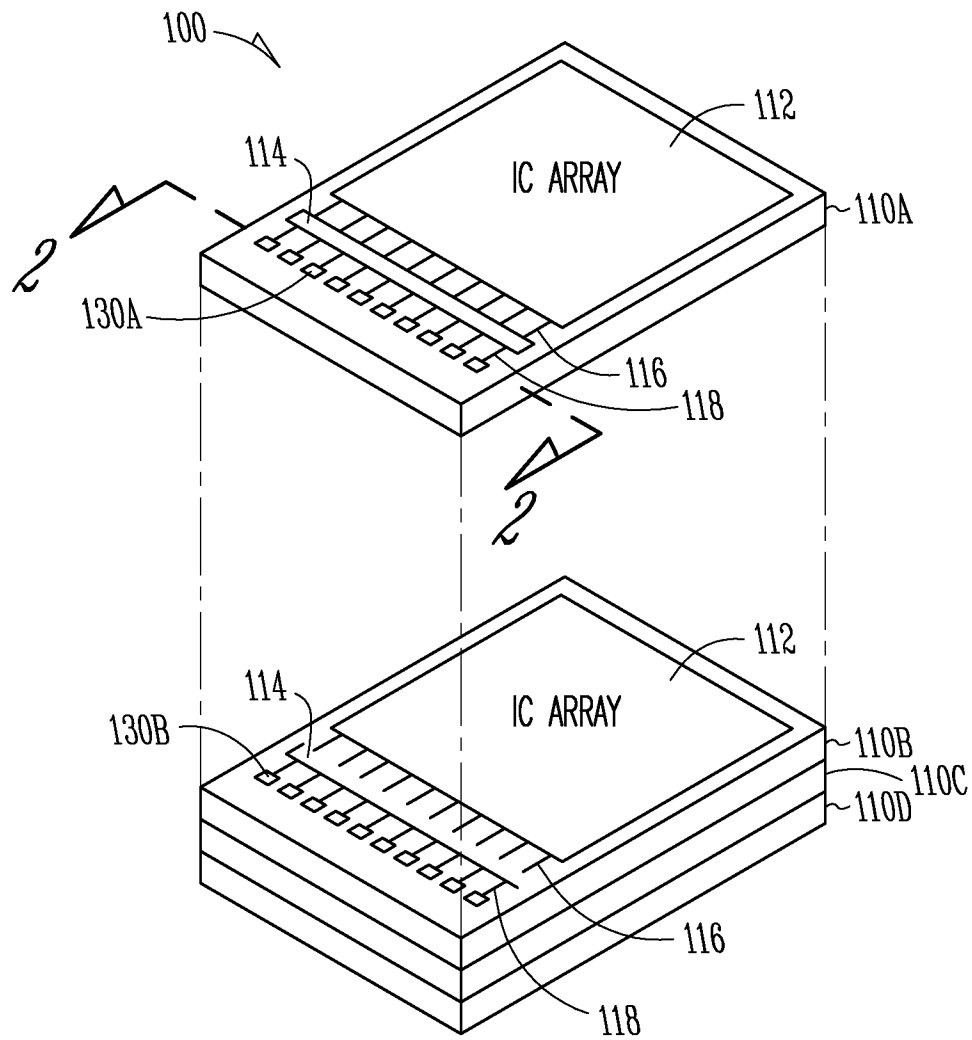


Fig. 1

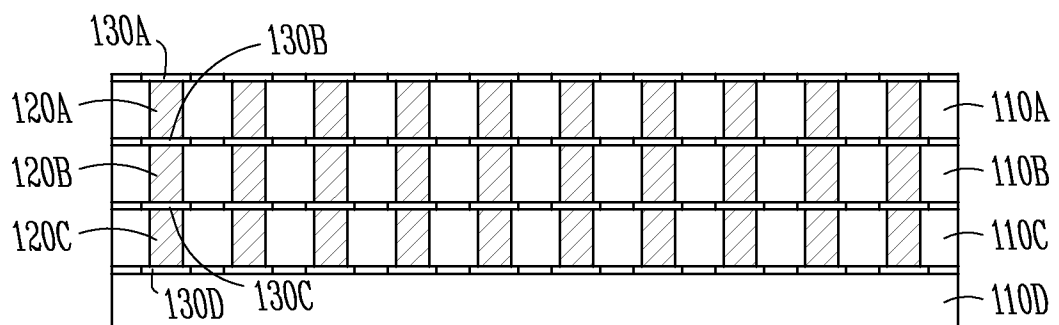


Fig. 2

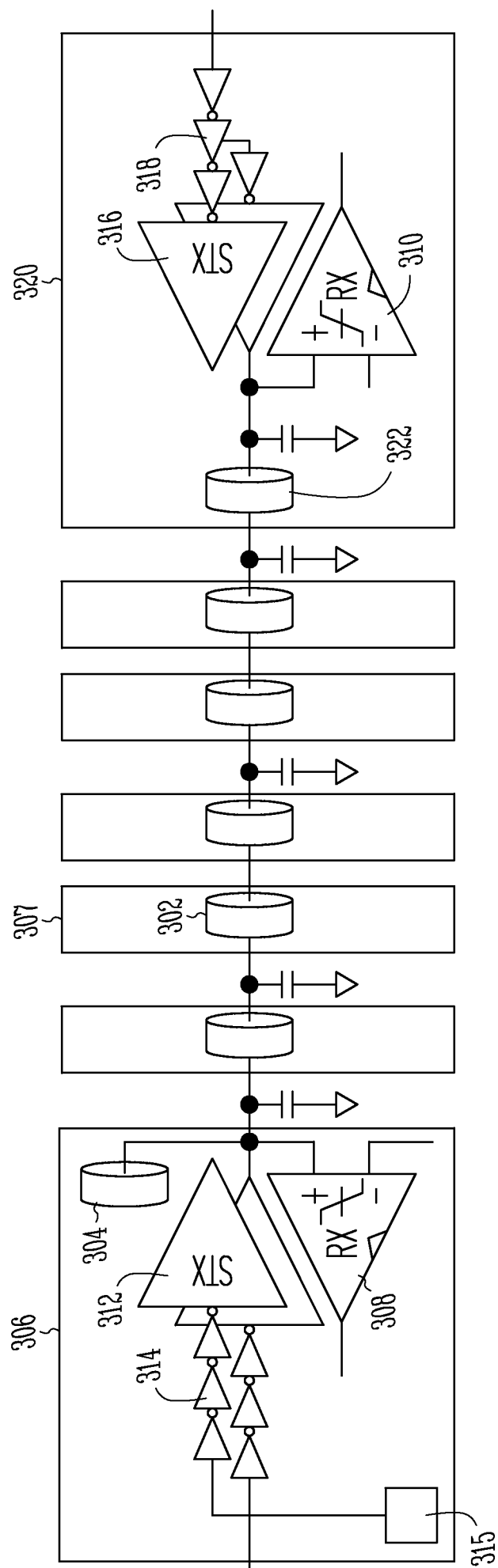


Fig. 3

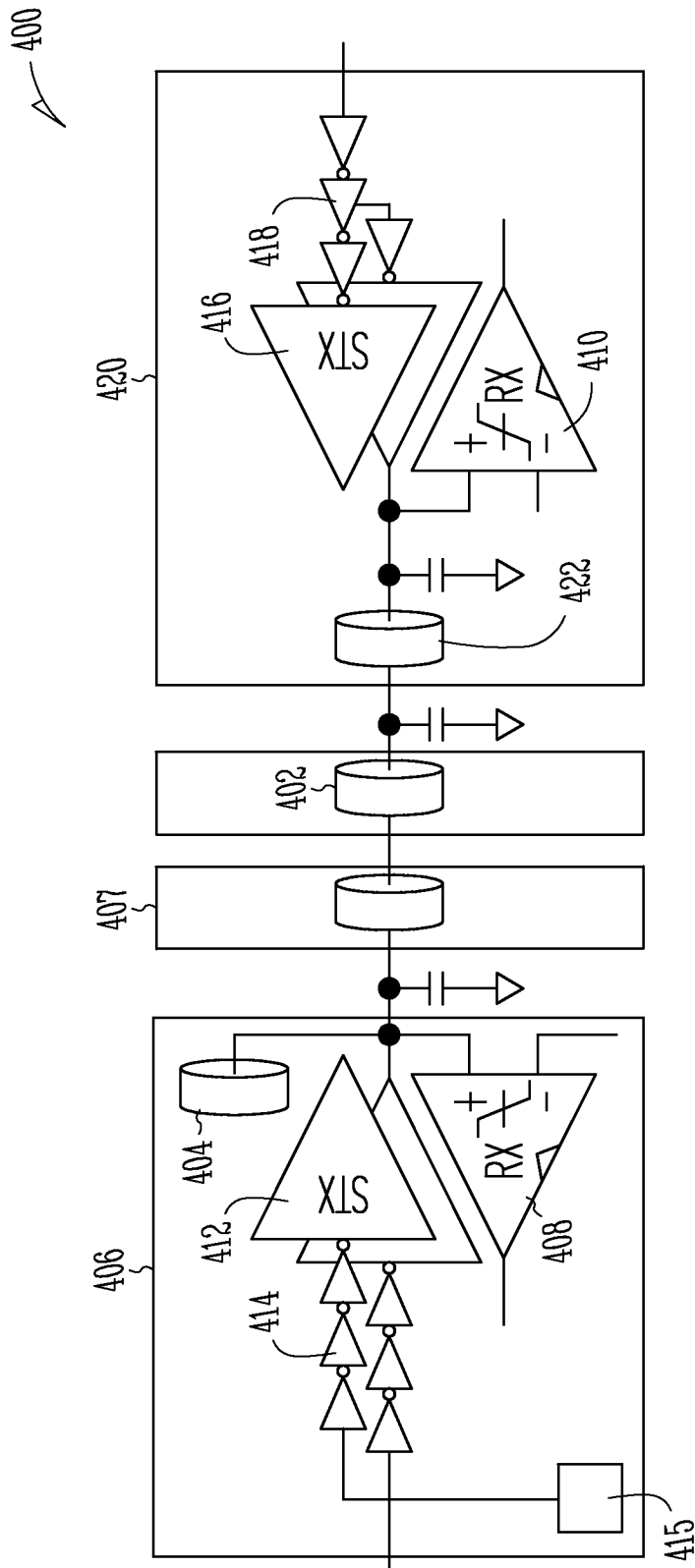


Fig. 4

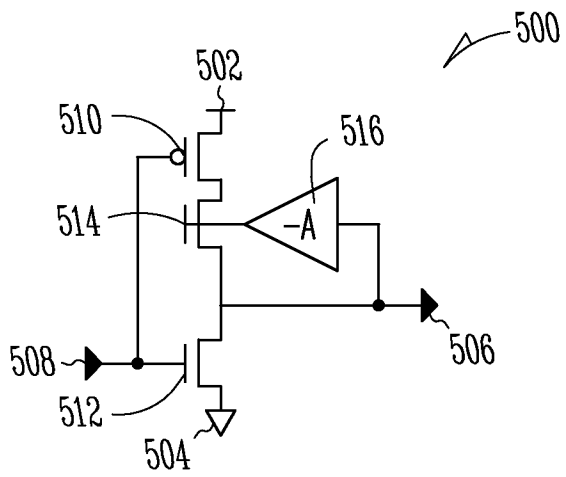


Fig. 5

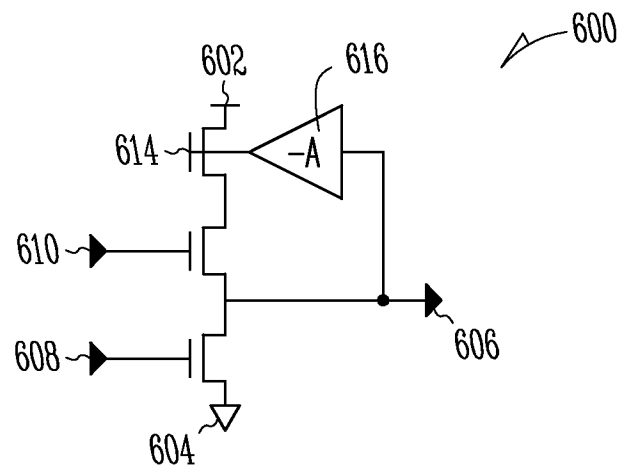


Fig. 6

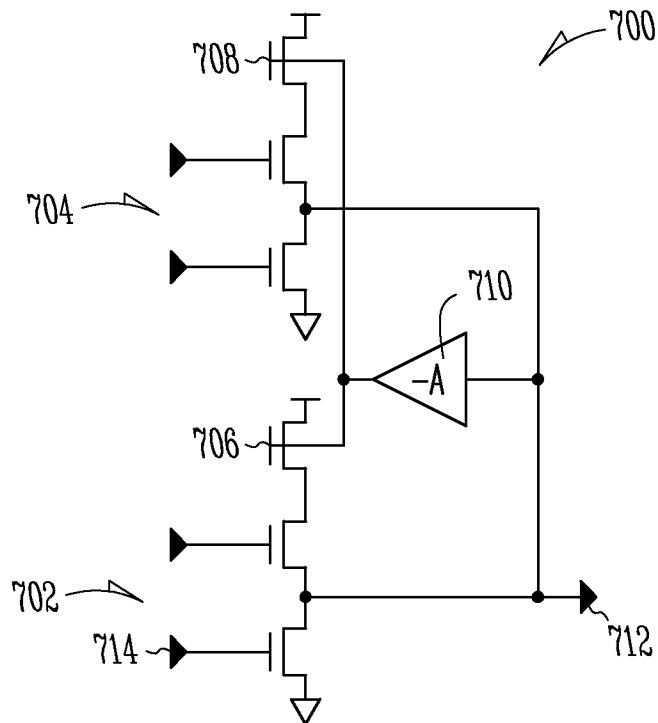
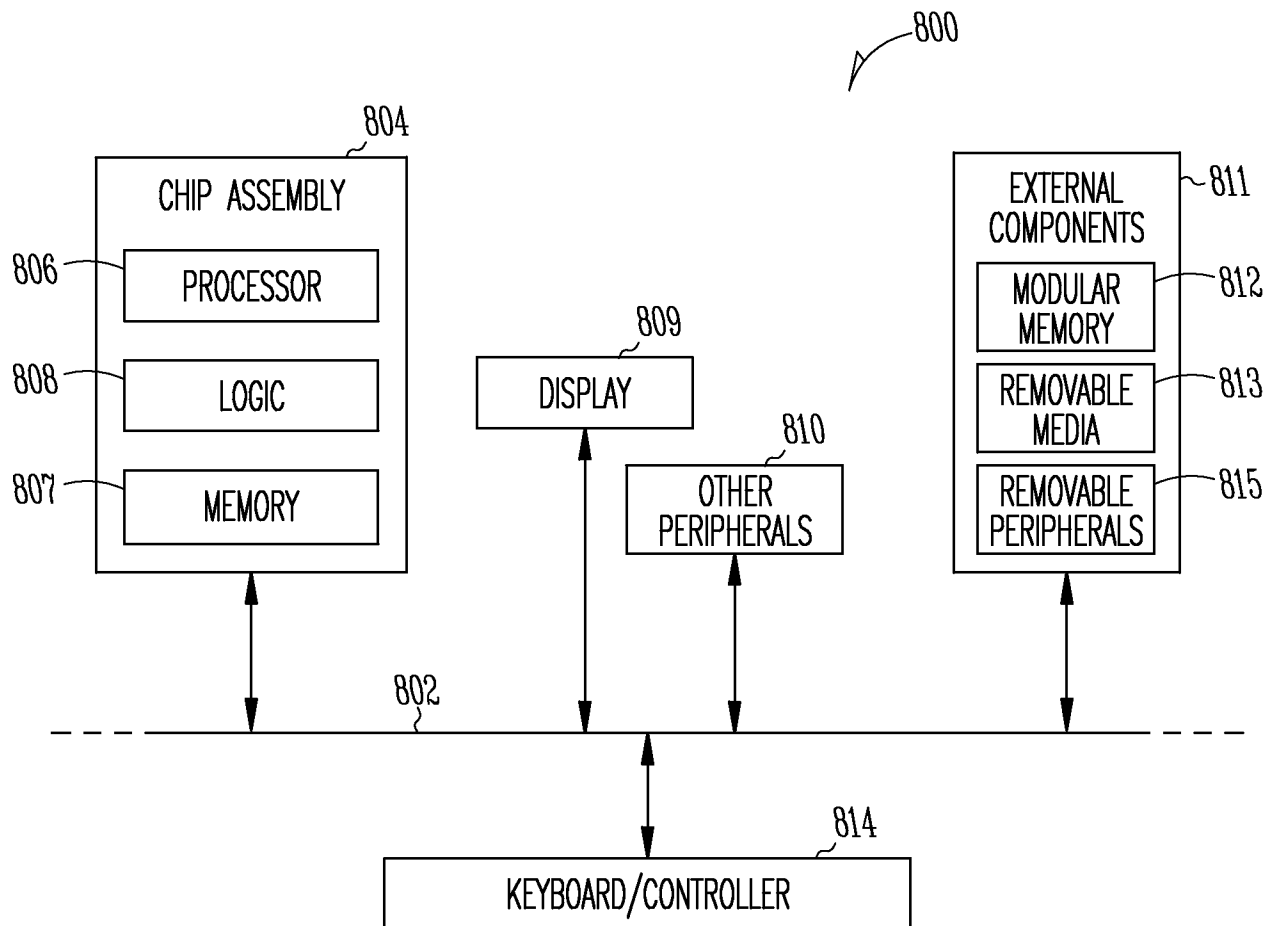


Fig. 7

*Fig. 8*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/030900**A. CLASSIFICATION OF SUBJECT MATTER****G11C 5/02(2006.01)i, G11C 7/10(2006.01)i, G11C 7/22(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 5/02; H01L 29/40; H01L 21/301; H01L 23/488; H01L 21/44; G11C 8/08; G11C 29/00; G11C 7/10; G11C 7/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: semiconductor, dice, vias, single, via, driver, signal, power, consumption, and similar terms.**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7129567 B2 (KYLE K. KIRBY et al.) 31 October 2006 See column 2, lines 63-67; column 3, lines 32-40; column 19, lines 29-31; column 22, lines 40-44; and claim 1.	1-30
A	US 2008-0142959 A1 (EDWARD M. DEMULDER et al.) 19 June 2008 See paragraph 34; and figure 5.	1-30
A	US 2004-0121563 A1 (WARREN M. FARNWORTH et al.) 24 June 2004 See paragraphs 9, 13, 19, 181-182; and figure 8A.	1-30
A	KR 10-2010-0105040 A (SK HYNIX INC.) 29 September 2010 See paragraphs 11-18; and figure 3.	1-30



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