METHOD FOR FORMING PHASE CHANGE MEMORY DEVICE

FIG. 1

Phase change memory (PCM) device structures are described, in which the phase change material is seamless, thereby obviating void issues that are associated with decreased device performance. Such PCM device structures can be readily formed by a trench technique in which phase change material is conformally deposited on trench side wall and bottom surfaces, followed by removal of the phase change material from the bottom surface, deposition of a dielectric passivation layer and thereafter oxide and/or nitride material, followed by CMP to remove dielectric and oxide/nitride material, and expose top surfaces of the phase change material. A top electrode then is formed in contact with the exposed top surfaces of the phase change material to provide a top electrode/PCM device structure including the seamless PCM material.
METHOD FOR FORMING PHASE CHANGE MEMORY DEVICE

Technical Field
The present disclosure relates generally to phase change memory devices and, more particularly, to methods for forming phase change memory devices employing germanium antimony tellurides.

Background
Phase change memory (PCM) is a form of non-volatile memory used in computer applications. In PCM, the behavior of a chalcogenide material (typically an alloy of germanium, antimony, and tellurium (GST)) is altered by changing the material between crystalline and amorphous phases. A thermistor or any other suitable device operates to apply heat to effect the phase changes in the chalcogenide material. The crystalline and amorphous phases have different electrical resistivities, which can be used to represent binary codes for storing data. In order to reduce the power needed to induce the change between the two phases, small volumes of GST are used. In particular, small volumes of GST are confined within relatively small trenches, holes (vias), or similar structures.

However, in producing PCM for computer applications, highly conformal deposition of GST through either chemical vapor deposition (CVD) or atomic layer deposition (ALD) is used to fill the structure thereby confining the GST within the structure. In some methods of producing such PCM, even with a 100% conformal process, a seam (interface when GST films on sidewalls meet) is formed. The seam is usually not an overly dense collection of GST, and it becomes a void in the GST after cycling (alternating high and low temperatures to cause the material to alternate between amorphous and crystalline phases). Such a void often leads to early reliability failure in a device utilizing the PCM, the reliability failure typically being characterized as short endurance or low retention of data.

In other methods, PCM cells are produced using cross-spacers. In at least one method employing cross-spacers, tantalum nitride (TaN) is deposited into cup-like structures, which are then filled with a low temperature oxide (LTO). A chemical mechanical polish (CMP) process is then used to reveal the top edge(s) of the TaN. A low temperature nitride (LTN) is deposited onto portions of the top edges, as are
layers of LTO and titanium tungsten (TiW) with the TiW on top to form top electrodes. Spacers of GST are subsequently deposited adjacent the stacked LTO and TiW and the LTN to operate as the phase change material, and the cup-like structures are coated with LTO. Aluminum/TaN interconnect lines are disposed in contact with the TiW through the bottoms of the cup-like structures, and bottom electrodes are added. In such a method, complex masking procedures are used to pattern the GST, and the GST contact with the top electrode is along a vertical edge, which is difficult to scale, thereby adding substantial costs to the method.

In other methods of forming PCM devices, trench structures in which GST has typically been confined are replaced with walls. The use of walls allows phase change material (GST or other chalcogenide material) to be deposited onto flat surfaces adjacent the walls using a flow process. However, in such methods the phase change material is not suitably confined as it is in PCM devices employing trenches. Thus, performance and scalability of such PCM devices is compromised relative to PCM devices in which the phase change material is deposited in trenches.

What is needed is a method for forming a PCM device structure in which the phase change material is suitably confined without the incorporation of seams that could compromise the integrity of the device.

**Summary**

The present disclosure relates to phase change memory devices and methods of making same.

In one aspect, the present disclosure is directed to a phase change memory device comprising a substrate, materials disposed on first and second surfaces of the substrate, a top electrode located in the material on the first surface, at least one bottom electrode located in the material on the second surface, and at least one slab structure located in the substrate and in communication with the top electrodes and the bottom electrode(s). The materials on the first and second surfaces of the substrate are at least one of a low temperature oxide and a low temperature nitride. The slab structure is a substantially seamless and substantially voidless structure of a phase change material.

In another aspect, the present disclosure is directed to a method of forming a phase change memory device. In this method, a substrate having a first surface and an opposing second surface is provided. A trench is formed in the first surface, and
one or more bottom electrodes are located in the second surface and in
communication with the trench. A phase change material is deposited in the trench.
Dielectric passivation and fill layers are also deposited in the trench, and a top
electrode is deposited on the first surface such that communication is maintained with
the bottom electrodes via interconnect lines formed by the phase change material.

In another aspect, the present disclosure is also directed to a method of
forming a phase change memory device. In this method, a substrate having top and
bottom layers is provided, and a trench is formed in the top layer. At least one bottom
electrode is formed in the bottom layer. A phase change material is deposited in the
trench and in communication with the at least one bottom electrode. A dielectric
passivation layer is deposited on the phase change material, and a fill layer is
deposited on the dielectric passivation layer. A top electrode is then deposited on the
top layer and in communication with the phase change material. Electrical
communication is maintained between the top electrode and the bottom electrode via
interconnect lines formed by the phase change material.

Other aspects, features and embodiments of the present disclosure will be
more fully apparent from the ensuing description and appended claims.

**Brief Description of the Drawings**

FIG. 1 is a schematic representation of a trench formed in a top surface of a
substrate and two bottom electrodes located in a bottom surface of the substrate.

FIG. 2 is a schematic representation of the substrate of FIG. 1 having a phase
change material deposited in the trench and on the top surface of the substrate.

FIG. 3 is a schematic representation of the substrate in which portions of the
phase change material in the trench and on the top surface of the substrate are
removed.

FIG. 4 is a schematic representation of the substrate of FIG. 3 in which a
dielectric passivation layer and a fill layer are deposited in the trench and on the top
surface of the substrate.

FIG. 5 is a schematic representation of the substrate of FIG. 4 in which
portions of the dielectric passivation layer and the fill layer are removed to expose the
phase change material on the top surface.

FIG. 6 is a schematic representation of a top electrode deposited on the top
surface of the substrate.
FIG. 7 is a schematic perspective representation of the substrate having top and bottom electrodes being in electrical communication via interconnect lines formed by the phase change material.

**Detailed Description**

A PCM device formed by a method of the present invention is shown below. The PCM device comprises top and bottom electrodes connected by phase change material. Dielectric material(s) provide for isolation of the top and bottom electrodes from each other and for isolation of the phase change material.

Referring to FIG. 1, in a first step of forming the PCM device, a trench 10 is formed in a substrate 12. As is shown, the substrate 12 comprises a top layer 14 and a bottom layer 16 interfacially positioned on each other. The top layer 14 comprises silicon dioxide (SiO$_2$) (or other LTO), silicon nitride (SiN) (or other LTN), or a combination of the foregoing materials as a dielectric to provide insulative properties. The bottom layer 16 comprises the same or similar materials, and the composition thereof may be disparate from the composition of the top layer 14. The substrate 12 is not limited to comprising a top layer 14 and a bottom layer 16, however, as the substrate may be a unitary member comprising one or more of SiO$_2$ and SiN.

Bottom electrodes 20 are located in the bottom layer 16 of the substrate 12 such that bottom edges of opposing walls 22 of the trench 10 are in communication with surfaces of the bottom electrodes at points 26. Bottom electrodes 20 are each of width $f$ and are separated from each other by a width $f$. The length of each bottom electrode 20 (i.e. the dimension of the bottom electrode perpendicular to the width) is any desired length. Accordingly, in the PCM device, the bottom electrode 20 extends in all three dimensions to have any desired configuration. The bottom layer 16 is also configured to include any suitable topography to accommodate the location of the bottom electrodes 20 therein. Although the bottom electrodes 20 are shown as having angular configurations, the present invention is not limited in this regard, and the bottom electrodes may be cylindrical. Materials from which the bottom electrodes 20 may be fabricated include, but are not limited to, TiAIN, TiNW, combinations of the foregoing materials, and the like.

To form the trench 10, a lithographic mask may be disposed on the top layer 14, and an etching process (e.g., using a wet etching chemical) may be used to form
the trench. The width of the trench is 2f. The length of the trench (i.e. the dimension of the trench in the dimension perpendicular to the width) may also be 2f.

Referring now to FIG. 2, in a second step of forming the PCM device, the phase change material is deposited on the top layer 14 of the substrate 12 and the walls and bottom surface that at least partially define the trench 10. The phase change material, which is designated by the reference number 30, is deposited using a technique that distributes the phase change material to as uniform a thickness and as conformally as possible. Such techniques include, but are not limited to, CVD, digital CVD, pulsed CVD, metal oxide CVD, and ALD. Variants of such techniques are also within the scope of the disclosed methods. The phase change material 30 is hereinafter referred to as being GST 30, although the methods disclosed herein are not so limited as other phase change materials may be used. For example, the phase change material 30 may be germanium, germanium antimony, germanium telluride, antimony telluride, or any combination thereof. In depositing the GST 30, the ratios of germanium (Ge) to antimony (Sb) to tellurium (Te) (atomic % (at. %)) may be about 2:2:5, about 4:1:5, about 30:15:55, or the like. In embodiments in which the ratio is 2:2:5, Ge is about 20-25 at.%, Sb is about 20-25 at.%, and Te is about 50-60 at.%. In embodiments in which the ratio is 4:1:5, Ge is about 40-45 at.%, Sb is about 5-10 at.%, and Te is about 50-55 at.%. In embodiments in which the ratio is 30:15:55, Ge is about 27-33 at.%, Sb is about 15-20 at.%, and Te is about 50-60 at.%.

Referring now to FIG. 3, the GST 30 is optionally removed from the top surface of the top layer 14 using a directional plasma etching process (a spacer etching process). The GST 30 is then removed from the bottom of the trench 10 using the same directional plasma etching process. In the directional plasma etching process, a horizontally oriented film (in this case GST 30) is removed. Upon completion of the removal of the GST 30 from the bottom surface of the trench 10 and optionally the top surface of the top layer 14, the GST remains on the sidewalls of the trench, thereby forming slabs of the GST material that are substantially seamless and include substantially no voids. Because the slabs are deposited using deposition processes, the dimensions thereof (e.g., the height and width) are defined independently of the particular deposition process employed. The methods and devices are not so limited, however, as the GST 30 can be selectively applied to the sidewalls and not the bottom surface of the trench, thereby avoiding the step of removing GST from the bottom surface of the trench. In embodiments in which the
GST 30 is not completely removed from the top layer 14 using the directional plasma etching process, the residue GST on the top layer can be removed using a CMP process.

In a forth step as is shown in FIG. 4, material is substantially conformally deposited on the top surface of the top layer 14 and on the GST-covered sidewalls and bottom surface of the trench 10 to form a dielectric passivation layer 34. The material used to form the dielectric passivation layer 34 is SiN. However, this material is not limited to being SiN, as any other material that is not reactive with GST can be used. The SiN forming the dielectric passivation layer 34 is deposited substantially conformally on the top layer 14 and sidewalls at a temperature of less than about 450 degrees C using any suitable deposition technique.

Also in the fourth step, a fill layer, designated generally by the reference number 36 and comprising SiO$_2$ and/or SiN, is deposited on the dielectric passivation layer 34. Deposition of the fill layer 36 is effected using high-deposition rate CVD (or a similar suitable technique) such that a substantially uniform and conformally deposited layer of SiO$_2$ and/or SiN is formed on the top surface of the top layer 14. The fill layer 36 can be continuous with the top layer 14 (e.g., the fill layer can comprise the same material as the dielectric passivation layer 34).

Referring now to FIG. 5, a CMP process is applied to the fill layer 36 deposited on the dielectric passivation layer 34. In doing so, both the material of the dielectric passivation layer 34 and the SiO$_2$ and/or SiN material of the fill layer 36 and the GST on the top surface are removed to leave the trench filled with dielectric material and the top edges of the GST 30 exposed to receive top electrodes.

Referring now to FIG. 6, electrode material to form the top electrode (designated by the reference number 40) is deposited on the top layer 14 such that the electrode material is in direct communication with the GST 30, the material of the passivation layer 34, and the material of the fill layer 36. The electrode material is deposited using a physical vapor deposition (PVD) technique, although the method disclosed herein is not so limited and other techniques may be employed. Furthermore, the electrode material is shown as being TiN, although other materials may be used.

Referring now to FIG. 7, the electrode material is patterned to form the top electrode 40 as an elongated element that extends laterally across the GST 30. Patterning of the electrode material can be performed using any suitable technique.
(e.g., etching). If patterned using an etching technique, the electrode material, dielectric material, and GST 30 are etched down to the level of the bottom electrodes 20, thereby removing the GST material that extends laterally from under the edges of the top electrode 40 and causing the GST 30 to be defined by slabs that provide communication (interconnect lines) from the bottom electrodes 20 to the top electrode 40.

In another step, dielectric material is conformally deposited using any suitable technique (e.g., CVD, ALD, or the like) to seal any exposed GST 30 and dielectric fill material located between the top electrode 14 and the bottom electrodes 20.

The methods described herein are scalable, controllable, and suitable for use with high-volume manufacturing (HVM) techniques with regard to the formation of modified PCM devices.

The devices resulting from the methods and techniques described herein exhibit several advantages over devices of the prior art. First, since there is no filling of gaps between surfaces on which GST is deposited, there are no seams formed. Because voids generally develop over time at seams and because no seams are formed, the voids do not develop. Thus, without the development of voids, there is less opportunity to compromise the integrity of PCM devices resulting from the use of the methods described herein.

Second, the dimensions of the GST-active region are well defined by the GST film thickness and photolithographic techniques used to define the GST dimensions to facilitate contact with the electrodes. Additionally, the GST-active region is self-aligned with the top electrode in the formed PCM device.

Third, by sizing the trench to have a dimension of 2f, the photolithographic technique used to define the dimensions of the GST-active regions can be more easily, efficiently, and cost-effectively carried out as compared to other hole/trench fill structures in which the photolithography is carried out at much smaller dimensions.

Fourth, the PCM device and the methods used to form it are easily scalable due to the ability of the thickness of the GST-active region to be controlled to be as thin as desired and further due to this region being made the same as the width of the top electrode. The improvement in the scalability is also due to the lack of filling of gaps. Thus, there is no limit to scaling beyond the patterning of the top electrode.

In relation to the PCM cell fabrication method employing cross-spacers that is described in the Background section hereof, the PCM device fabrication method of
the present disclosure utilizes a different process flow and fabrication sequence, which in turn produce corresponding structural differences in the PCM device. In the prior cell fabrication method described in the Background section hereof, the phase change material, e.g., GST, is deposited against the (already formed) stacked LTO and TiW top electrode, so that the GST contact with the top electrode is along a vertical edge, which is difficult to scale, thereby adding substantial costs to the method. By contrast, the phase change memory material, e.g., GST, in the fabrication method of the present disclosure can be deposited well before the top electrode formation, so that the phase change material/top electrode contact is along a horizontal surface, which is easier to scale, and simpler and less expensive to fabricate.

Although this invention has been shown and described with respect to the detailed embodiments thereof, it will be understood by those of skill in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiments disclosed in the above detailed description, but that the invention will include all embodiments falling within the scope of the appended claims.
What is claimed is:

1. A phase change memory device, comprising:
   a substrate;
   at least one of a low temperature oxide and a low temperature nitride disposed on a first surface of the substrate;
   at least one of a low temperature oxide and a low temperature nitride disposed on a second surface of the substrate;
   a top electrode located in the at least one of a low temperature oxide and a low temperature nitride disposed on the first surface of the substrate;
   at least one bottom electrode located in the at least one of a low temperature oxide and a low temperature nitride disposed on the second surface of the substrate;
   and
   at least one slab structure located in the substrate and in communication with the top electrode and the at least one bottom electrode, the slab structure comprising a seamless and voidless structure of a phase change material.

2. The phase change memory device of claim 1, wherein dimensions of the at least one slab structure are defined independently of a process by which the phase change material of the slab structure is located in the substrate.

3. The phase change memory device of claim 1, wherein the phase change material comprises GST.

4. The phase change memory device of claim 3, wherein the GST comprises about 20-25 at.% Ge, about 20-25 at.% Sb, and about 50-60 at.% Te.

5. The phase change memory device of claim 3, wherein the GST comprises about 40-45 at.% Ge, about 5-10 at.% Sb, and about 50-55 at.% Te.

6. The phase change memory device of claim 3, wherein the GST comprises about 27-33 at.% Ge, about 15-20 at.% Sb, and about 50-60 at.% Te.
A method of forming a phase change memory device, the method comprising the steps of:

- providing a substrate having a first surface and an opposing second surface;
- forming a trench in the first surface of the substrate, the trench having at least one defining wall and a bottom surface;
- locating at least one bottom electrode in the second surface of the substrate, the at least one bottom electrode being in communication with the at least one defining wall;
- depositing a phase change material on the defining wall and the bottom surface of the trench such that communication is maintained with the at least one bottom electrode;
- removing at least a portion of the deposited phase change material;
- depositing a dielectric passivation layer on the phase change material and on the bottom surface of the trench;
- depositing a fill layer on the dielectric passivation layer; and
- depositing a top electrode on the substrate such that communication is maintained between the top electrode and the at least one bottom electrode via the phase change material.

The method of claim 7, wherein the step of forming the trench comprises disposing a lithographic mask on the first surface of the substrate and using an etching process to form the trench.

The method of claim 7, wherein the step of depositing the phase change material on the defining wall of the trench comprises depositing the phase change material using a technique selected from the group consisting of chemical vapor deposition (CVD) and atomic layer deposition (ALD).

The method of claim 7, further comprising applying a chemical mechanical polish (CMP) process to the deposited phase change material, the deposited dielectric passivation layer, and the deposited fill layer prior to depositing the top electrode.
11. The method of claim 7, wherein the step of removing at least a portion of the deposited phase change material comprises using a directional plasma etching process to remove deposited phase change material from at least the bottom surface of the trench.

12. The method of claim 7, wherein the phase change material is germanium antimony telluride (GST).

13. The method of claim 12, wherein the GST comprises about 20-25 at.% Ge, about 20-25 at.% Sb, and about 50-60 at.% Te.

14. The method of claim 12, wherein the GST comprises about 40-45 at.% Ge, about 5-10 at.% Sb, and about 50-55 at.% Te.

15. The method of claim 12, wherein the GST comprises about 27-33 at.% Ge, about 15-20 at.% Sb, and about 50-60 at.% Te.

16. The method of claim 7, wherein the top electrode is fabricated from TiN.

17. The method of claim 7, wherein the bottom electrodes are fabricated from a material selected from the group consisting of TiAlN, TiNW, and combinations of the foregoing materials.

18. A method of forming a phase change memory device, the method comprising the steps of:
   - providing a substrate having a top layer and an opposing bottom layer;
   - forming a trench in the top layer;
   - locating at least one bottom electrode in the bottom layer;
   - depositing a phase change material in the trench and in communication with the at least one bottom electrode;
   - depositing a dielectric passivation layer on the phase change material;
   - depositing a fill layer on the dielectric passivation layer; and
   - depositing a top electrode on the top layer and in communication with the phase change material;
wherein electrical communication is maintained between the top electrode and the bottom electrode via the phase change material forming an interconnect line between the top electrodes and the bottom electrodes.

19. The method of claim 18, wherein the step of depositing the phase change material in the trench comprises depositing the phase change material using a technique selected from the group consisting of CVD and ALD.

20. The method of claim 18, wherein the step of depositing the phase change material in the trench comprises depositing the phase change material on the top layer of the substrate, a sidewall at least in part defining the trench, and a bottom surface at least in part defining the trench.

21. The method of claim 20, further comprising applying a directional plasma etching process to remove phase change material from the bottom surface of the trench and optionally from the top layer of the substrate.

22. The method of claim 18, wherein the steps of depositing the dielectric passivation layer and depositing the fill layer comprises depositing the dielectric passivation layer and depositing the fill layer on the top layer of the substrate.

23. The method of claim 22, further comprising applying a CMP process to the dielectric passivation layer and the fill layer on the top layer of the substrate to expose the phase change material on the top layer.