A signal shaping circuit (100) shapes an input signal (DATA INPUT) of a digital data stream provided at an input terminal and generates an output signal (OUTPUT) at an output (122) having sinusoidally shaped transition regions between logic level transitions of the digital data stream. The signal shaping circuit (100) comprises the input terminal (102) for receiving digital pulses of the digital data stream, a delay circuit (106) for delaying the digital pulses at the input terminal (102) for a predetermined time delay, and a ringing filter circuit (124) coupled to the input terminal (102) and the delay circuit (106) for generating the output signal (OUTPUT) responsive to the digital data stream. The ringing filter circuit (124) has a ringing period about equal to or less than twice a period of the digital data stream and the predetermined time delay of the delay circuit (106) is about equal to half of a ringing period. The output waveform of the output signal (OUTPUT) has a lower bandwidth than the corresponding input signal and no intersymbol interference associated with it.
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BACKGROUND OF THE INVENTION

The present invention generally relates to the transmission of digital signals and more specifically to a circuit for shaping digital pulse data transmissions, such as non-return to zero (NRZ) type digital transmissions.

Digital data transmissions are often in the form of a series of transmitted pulses wherein each pulse is transmitted at an amplitude of one of at least two binary states. Such transmissions are often referred to as amplitude shift keyed transmissions and generally are associated with pulses that are transmitted with one of two amplitude
levels.

One example of a data transmission format for transmitting digital information is known as the non-return-to-zero (NRZ) format. The NRZ format is a binary amplitude shift keyed format. Fig. 1 illustrates an exemplary NRZ digital transmission comprising a plurality of serial data pulses or "symbols" 10, each of which has a symbol period or width T. Since the NRZ format is a binary data format, the data symbols 10 may have one of only two amplitude states.

FIG. 2 illustrates the frequency spectrum of a single data pulse of the exemplary digital pulse transmission. As shown, the frequency spectrum is centered at a frequency \( F_c \) which, for example, may be at baseband or at the frequency of a modulated carrier. The frequency spectrum includes a main lobe 14 followed by multiple side lobes, such as at 16 and 18, that decrease in magnitude along the frequency axis. The information carried by the digital data pulse is principally found in the main lobe 14 having a bandwidth \( f \), where \( f \) equals \( 1/T \), and where \( T \) equals the pulse width of a single symbol. It is therefore preferable to filter out the frequency components above the frequency \( f \) because the side lobes 16 and 18 above frequency \( f \) have substantial amplitudes and thus, contain a significant amount of high frequency energy. Consequently, complex, high order filters would normally be required to filter out an acceptable amount of the high frequency energy. It is, however, undesirable to use complex filters.

It has been proposed to "smooth" the waveform of an NRZ data pulse stream prior to transmission. As shown in Fig. 3, the NRZ digital data stream has been
modified to include transition regions, such as 22 and 24, which are substantially sinusoidally shaped. Fig. 2 illustrates the frequency spectrum associated with a single pulse of the waveform of Fig. 3. As shown at 25 of Fig. 2, the frequency spectrum includes a main lobe 26 followed by side lobes 28, 30 and 32. The side lobes 28, 30 and 32 are significantly smaller in amplitude than the side lobes 16 and 18 associated with a non-smoothed NRZ data bit stream (Fig. 1). Consequently, a much simpler filter may be used to filter out signals at frequencies above frequency $F_1$ prior to transmission.

"Smoothing" of a digital data pulse transmission has several advantageous effects. First, the reduced bandwidth means that more such transmissions can be transmitted within a given allocated bandwidth. This, in turn, means that more intelligent information can be transmitted in a given bandwidth.

One system of note in connection with such an approach to digital data transmissions is set forth in USP 4,339,724 titled "Filter" by Dr. Kamilo Feher. The ’724 patent seeks to prevent intersymbol interference and jitter, while reducing the bandwidth of the data signals. The ’724 patent discloses a filter that includes an input for receiving a pulse type of input signal and for providing an output signal correlated to the input signal. The filter comprises means for comparing the output signal with the input signal and four waveform generators. The first waveform generator produces a first predetermined output signal waveform when the input and output signal amplitudes differ and the input signal equals a logical 1. The second waveform generator produces a second predetermined output signal waveform when the input and
output signal amplitudes differ and the input signal equals a logical zero. The third waveform generator produces a third predetermined output signal waveform when the input and output signal amplitudes equal and the input signal equals a logical 1. The fourth waveform generator produces a fourth predetermined output signal waveform when the input and output signal amplitudes equal and the input signal equals a logical zero. The first through fourth waveform generators correspond to a sine wave generator, a cosine wave generator, a positive DC signal generator and a negative DC signal generator, respectively. Each signal generator is turned on and off by switches controlled by the aforementioned logic.

However, the filter of the '724 patent is unduly complex as it requires separate waveform generators to produce each desired segment of the output signal, along with a complex logic and switching network to analyze the input signal and turn on and off corresponding signal generators. The filter of the '724 patent draws a significant amount of power to drive the multiple waveform generators that construct the output signal.
BRIEF SUMMARY OF THE INVENTION

A signal shaping circuit for shaping amplitude shift keyed digital pulses of a digital data stream is set forth. The digital data stream is comprised of a plurality of symbols from which the signal shaping circuit generates an output signal having sinusoidally shaped transition regions between logic level transitions of the digital data stream. The signal shaping circuit comprises an input lead receiving each of the digital pulses of the digital data stream. A delay circuit receives each of the digital pulses of the digital data stream at the input lead and, after a predefined time delay, outputs delayed digital pulses corresponding to each of the digital pulses received at the input lead. A ringing filter circuit having a linear response receives each of the digital pulses of the digital data stream provided from the input lead and each of the digital pulses provided at the output of the delay circuit. The ringing filter circuit has a ringing period about equal to or less than twice the symbol period of the digital data stream which, in turn, sets the value of the predefined delay. More particularly, the predefined delay of the delay circuit is about equal to half of the ringing period. As a result, the ringing filter circuit generates an output amplitude shift keyed digital data stream directly corresponding to the digital data stream provided at the input lead which has sinusoidally shaped transition regions between its logic level transitions. The resulting waveform has a lower bandwidth than the corresponding input signal and, further, has no intersymbol interference associated with it.

The construction of the foregoing system may be extended to provide
sinusoidal transitions to a multilevel, non-binary output data stream that is generated from a plurality of digital input data streams. Again, such a system provides an output signal having a lower bandwidth than the corresponding input signals and, further, has no intersymbol interference associated with it.
BRIEF DESCRIPTION OF THE DRAWINGS
SEVERAL VIEWS OF THE DRAWINGS

Fig. 1 illustrates a serial stream of amplitude shift keyed data pulses, such as found in an NRZ data transmission.

Fig. 2 illustrates a frequency spectrum associated with a pulse of the stream of data pulses illustrated in Fig. 1.

Fig. 3 illustrates a stream of smoothed amplitude shift keyed data pulses.

Fig. 4 is a schematic diagram of an ideal LC circuit used to illustrate some of the principles upon which the present invention is based.

Fig. 5 illustrates component waveforms and a resultant composite signal generated by the circuit of Fig. 4.

Fig. 6 is a schematic diagram of non-ideal LC circuit which experiences damping circuit used to illustrate some of the principles upon which the present invention is based.

Fig. 7 illustrates component waveforms and a resultant composite signal generated by the non-ideal circuit of Fig. 6.

Fig. 8 illustrates a schematic diagram of a first embodiment of the present invention.

Figs. 9A-9G illustrate signal responses produced by the circuit illustrated a the schematic diagram of Fig. 8.

Fig. 10 illustrates a schematic diagram of an embodiment of the present
invention for providing a multi-level, non-binary output signal.

Figs. 11A and 11B illustrate input and output signals associated with the circuit of Fig. 10.

Fig. 12 is a schematic diagram of a basic RF communications system that may employ the present invention.
DETAILED DESCRIPTION OF THE INVENTION

Prior to explanation of the preferred embodiments of the present invention, the following general explanation is provided to better illustrate the fundamentals upon which the subject invention is premised.

Fig. 4 illustrates a circuit diagram of an ideal circuit including an inductor $L$ connected in series with a capacitor $C$. Two voltage sources $V_1$ and $V_2$ are also provided in series with the inductor $L$ and capacitor $C$. The first and second voltage sources $V_1$ and $V_2$ are equal step forcing functions (e.g., one volt sources). An output $V_{\text{OUT}}$ of the circuit of Fig. 4 is illustrated in Fig. 5. It is assumed that the initial current and voltages within the circuit of Fig. 4 are zero prior to a time $T_0$. At time $T_0$, switch $S_1$ is closed, thereby connecting the first voltage source $V_1$, in series with the inductor $L$ and capacitor $C$. The negative terminal of the source $V_1$ is initially connected to ground through switch $S_2$. When the switch $S_1$ is closed, a step voltage equal to $V_1$ is applied to the LC circuit which produces a first sinusoidal waveform $S_{v1}$ (as shown in Fig. 5). The sinusoidal waveform $S_{v1}$ continuously "rings" or repeats at a ringing period $P_{\text{RNG}}$ since the circuit of Fig. 4 is presumed to be ideal, and without internal resistance.

Again referring to Fig. 4, it is now assumed that the second switch $S_2$ is moved in the direction indicated by the arrow at time $T_1$ to connect the first and second voltage sources $V_1$ and $V_2$ in series. At time $T_1$, a second component waveform $S_{v2}$ (generally illustrated in dashed lines) is output at $V_{\text{OUT}}$ in response to the second step input voltage $V_2$. The second sinusoidal or "ringing" waveform $S_{v2}$ is offset in time from the first
sinusoidal signal $S_{v1}$ by a time differential $T_1 - T_0$. This time differential is selected to be half of the ring period of the LC circuit.

The resultant or composite output signal $S_{OUT}$ (Fig. 4) may be calculated based on superposition of the first and second waveforms $S_{v1}$ and $S_{v2}$ since the circuit of Fig. 4 is linear, and, thus, obeys the laws of superposition. According to the principle of superposition, the output response at any particular time in a linear circuit in which more than one independent source is applied may be obtained by summing the responses caused by each independent source acting alone at the particular time. As illustrated, the resultant signal $S_{OUT}$ includes a smooth transition region and maintains a constant voltage after time $T_1$.

In the circuit of Fig. 6, input pulses are applied at times $T_0$ and $T_1$ to input lines 44 and 46 through resistors $R_1$ and $R_2$ and therefrom to the LC circuit. The circuit thus exhibits a damped response. Fig. 7 illustrates the signal response of the circuit of Fig. 6. The pulse introduced at time $T_0$ is acted upon by the RLC circuit to generate the signal waveform $S_{T0}$. Similarly, the pulse introduced at time $T_1$ is acted upon by the RLC circuit to generate a signal waveform $S_{T1}$. The circuit of Fig. 7, as noted, exhibits some damping, as evidenced in Fig. 7 by the reduction in amplitude of the first and second signal responses $S_{T0}$ and $S_{T1}$ over time. It is preferable to include damping in the circuit since the input pulses applied at lines 44 and 46 may differ. Without damping, a substantial output ripple error may accumulate over time.

The resistors $R_1$ and $R_2$ may be adjusted to coordinate, as closely as possible, the amplitudes of the first and second signal response waveforms. By way of example
only, the resistors $R_1$ and $R_2$ may be set such that the amplitude at the peak 48 (Fig. 7) of the second signal waveform $S_{T2}$ adds to (i.e., combines with) the amplitude at the valley 50 of the first signal $S_{T1}$ to maintain a generally constant output equal to the first peak 53 of the first signal $S_{T1}$. By way of example only, if one volt step functions are applied to leads 44 and 46, the resistors $R_1$ and $R_2$ may be set to 0.513 ohms and 0.855 ohms while $L$ may be a 0.314 H inductor and $C$ may be a 0.314 F capacitor.

Turning to Figs. 8 and 9A-9G, a first embodiment of the present invention is described and illustrated. Fig. 8 illustrates a pulse shaping circuit (generally denoted by the reference numeral 100). The pulse shaping circuit includes an input lead 102 which receives a stream of data bits that, for example, carry information using a binary NRZ data format (although multiple level signals having more than two states may also be applied). A tap line 104 connects the input lead 102 with a delay circuit 106. The signals of both the delay circuit 106 and the input lead 102 are provided (either directly or through one or more buffers) to a ringing filter circuit 124 that is specifically designed to have a ringing characteristic with a predetermined ringing period. The ringing period of the ringing filter circuit 124 is selected to be less than or about equal to two symbol periods of the data stream provided at the data input of the circuit 100. Preferably, the ringing period is equal to about two symbol periods. In some instances, it may be desirable to select the ringing period to be about one symbol period in duration.

By way of example only, the delay circuit 106 may represent a one bit shift register which shifts data pulses therethrough based on a data clock signal applied upon
line 108. The delay circuit 106 receives and stores each data bit entered upon the input lead 102 for a predetermined propagation delay. The propagation delay of the delay circuit 106 is preferably about equal to half of the ringing period of the ringing filter circuit. In an even more preferable embodiment, the propagation delay is equal to about one symbol period. The delay module 106 outputs a stream of delayed data symbols upon line 110. In the illustrated embodiment, the clock signal supplied to the shift register would have a clock period equal to the propagation delay. If an N-bit shift register were used, the clock signal would have a period equal to the propagation delay divided by N.

Fig. 9A illustrates an exemplary stream of data symbols 101 labeled as symbols A through D. An exemplary delayed data stream 103 is illustrated in Fig. 9B, in which each data symbol (A'-D') follows a corresponding data symbol (A-D) in the original input data stream 101 by a time T equal to the propagation delay. The original and delayed data streams are supplied to the ringing filter circuit 124. More particularly, in the present embodiment, the original and delayed symbol streams are supplied through resistors 112 and 114 to a common node 116 and to an inductor 118 and capacitor 120 that are arranged in a low-pass configuration. The resistors 112 and 114, the inductor 118 and the capacitor 120 cooperate to define the ringing filter circuit 124 that combines the symbol streams received upon lines 102 and 110 to produce a converted output data stream at line 122.

With reference again to the principles described in connection with Figs. 4 - 8, the response of the ringing filter can be understood. To this end, the individual
responses of the ringing filter circuit 124 to pulses A - D are illustrated in Figs. 9C - 9F, respectively. These signals are combined in the ringing filter circuit 124 to generate resultant composite waveform illustrated in Fig. 9G. As illustrated, the composite waveform includes transition regions 126, 128, 130, 132 and the like, which have a substantially sinusoidal shape. As such, the resulting waveform has a substantially reduced bandwidth when compared to the bandwidth of the input data stream of Fig. 9A. Additionally, the resulting waveform has no intersymbol interference associated with it. Preferably, the resulting waveform is acquired at times corresponding to \( t_1, t_2, t_3, \text{ etc.} \) by any receiver to which the data is supplied.

Figs. 10, 11A and 11B illustrate an alternative embodiment of the present invention. In the embodiment of Fig. 10, the shaping and filtering circuit has been modified for use in a transmission system which supports a multi-level data signal output stream having more than two potential logic levels. In the embodiment of Fig. 10, four logical levels are available through the use of two main input leads 150 and 152, each of which may receive a stream of binary data symbols 153 and 155 (although the input data stream may itself be a multilevel, non-binary stream). The symbols within the data streams 153 and 155 are aligned in time to define one of four logic levels. For example, when leads 150 and 152 both receive 0-state bits, they define a logic level zero. When leads 150 and 152 receive a 0-state bit and a 1-state bit, respectively, they define a logic level one. When leads 150 and 152 receive a 1-state bit and a 0-state bit, they define a logic level two, and when leads 150 and 152 both receive 1-state bits, they define a logic level three. The data streams 153 and 155 are
passed through buffers 154 and 156 to a ringing filter circuit 157 which may include resistors 158, 160, 162 and 164, inductor 166 and capacitor 168. The ringing filter circuit 157 has a ringing period such as described above.

The input leads 150 and 152 are connected at nodes 170 and 172 with tap lines 174 and 176 to deliver the incoming streams of data symbols 153 and 155 to a delay module 178. The delay module 178 outputs data bit values upon leads 180 and 182 which are received upon incoming tap lines 174 and 176, respectively, after a predefined delay (such as explained above in connection with the embodiment of Fig. 8). The delayed data bit streams are passed along lines 180 and 182 through buffers 184 and 186 to the ringing filter circuit 157 via resistors 162 and 164. By way of example only, the delay module may include two one-bit shift registers aligned in parallel to receive separately data symbols incoming from lines 174 and 176 and output same in parallel to lines 180 and 182. Other configurations are likewise suitable, such as described above.

The values of resistors 158, 160, 162 and 164 may be defined in a predetermined relationship to one another. Optionally, resistors 158 and 162 may be defined as a function of resistors 160 and 164, respectively. By way of example only, resistor 158 may equal 1/2 the value of resistor 160, while resistor 162 may equal 1/2 the value of resistor 164. Resistors 158 and 160 may be set with respect to resistors 162 and 164, to minimize ripple errors.

Turning to Figs. 11A and 11B, Fig. 11A illustrates an exemplary digital signal defined by the binary data bit streams 153 and 155. The digital signal of Fig. 11A
includes four discrete logic levels 202, 204, 206 and 208, each of which is defined by a unique bit combination received upon the leads 150 and 152. In Fig. 10, as data bit values are supplied via leads 150, 152, 180 and 182 to the ringing filter circuit 157, each data pulse introduces a corresponding component waveform response into the resultant signal on output lead 169. Resistors 158, 160, 162 and 164 are assigned values as explained above in order to ensure proper attention therebetween of the associated component waveform responses. It will be recognized that the logic levels need not be equally spaced.

The ringing filter circuit 157 outputs a resultant or composite signal on line 169 (Fig. 10) which resembles the signal illustrated in Fig. 11B in response to the signal illustrated in Fig. 11A. Within the resultant signal 220, transition regions between logic levels are shaped to be substantially sinusoidal (see transition regions 222, 224, 226 and the like).

In the foregoing embodiments, the transition regions between logic levels may occupy a complete clock cycle corresponding to the width of a data bit pulse. However, the transitions need not be so slow. Instead, the propagation of the delay module may be adjusted in order that the transitions occur in a shorter period of time in which case the transitions may be less smooth.

Fig. 12 illustrates a system in which the foregoing pulse shaping circuits may be used. More particularly, the system, shown generally at 300, is basic RF digital communications system comprising a transmitter 305 and receiver 310 that respectively transmit and receive data over a transmission medium 315, such as air,
cable, etc.. The pulse shaping circuits described herein may be incorporated in the baseband filter 320 of the receiver 310.

While particular elements, embodiments and applications of the present invention have been shown and described, it will be understood, of course, that the invention is not limited thereto since modifications may be made by those skilled in the art, particularly in light of the foregoing teachings. It is therefore contemplated by the appended claims to cover such modifications as incorporate those features which come within the spirit and scope of the invention.
CLAIMS

1. A signal shaping circuit for shaping amplitude shift keyed digital pulses of a digital data stream comprised of a plurality of symbols, the signal shaping circuit generating an output signal having sinusoidally shaped transition regions between logic level transitions of the digital data stream, said circuit comprising:

an input lead receiving each of the digital pulses of the digital data stream;

a delay circuit receiving each of the digital pulses of the digital data stream at the input lead and, after a predefined time delay, outputting delayed digital pulses corresponding to each of the digital pulses received at the input lead;

a ringing filter circuit having a linear response, the ringing filter circuit receiving each of the digital pulses of the digital data stream provided from the input lead and each of the digital pulses provided at the output of the delay circuit, the ringing filter circuit having a ringing period about equal to or less than twice the symbol period of the digital data stream, the predefined delay of the delay circuit being about equal to half of the ringing period, the ringing filter circuit generating an output amplitude shift keyed digital data stream directly corresponding to the digital data stream provided at the input lead wherein the output digital data stream has sinusoidally shaped transition regions between logic level transitions thereof.
2. A signal shaping circuit as claimed in claim 1 wherein the ringing filter circuit comprises:
   a first resistor;
   a second resistor;
   an inductor;
   a capacitor;
   the first resistor connected to receive the digital data stream from the input lead, the second resistor connected to receive the delayed digital pulses from the delay circuit, the inductor having a first lead connected at a common node with the first and second resistors and a second lead connected to the output of the ringing filter circuit, the capacitor being connected in a non-series circuit branch extending from the output of the ringing filter circuit.

3. A signal shaping circuit as claimed in claim 2 wherein the capacitor is connected between the output of the ringing filter circuit and circuit ground.

4. A signal shaping circuit as claimed in claim 1 wherein the delay circuit comprises a shift register.
5. A signal shaping circuit as claimed in claim 1 wherein the ringing period is about equal to the twice symbol period.

6. A signal shaping circuit as claimed in claim 1 wherein the ringing period is about equal to the symbol period.

7. A signal shaping circuit as claimed in claim 1 wherein the digital data stream is in a binary format.

8. A signal shaping circuit as claimed in claim 7 wherein the ringing filter circuit comprises:
   a first resistor;
   a second resistor;
   an inductor;
   a capacitor;
   the first resistor connected to receive the digital data stream from the input lead, the second resistor connected to receive the delayed digital pulses from the delay circuit, the inductor having a first lead connected at a common node with the first and second resistors and a second lead connected to the output of the ringing filter circuit, the capacitor being connected in a non-series circuit branch extending from the output of the ringing filter circuit.
9. A signal shaping circuit as claimed in claim 8 wherein the capacitor is connected between the output of the ringing filter circuit and circuit ground.

10. A signal shaping circuit as claimed in claim 7 wherein the delay circuit comprises a shift register.

11. A signal shaping circuit as claimed in claim 7 wherein the ringing period is about equal to the twice symbol period.

12. A signal shaping circuit as claimed in claim 7 wherein the ringing period is about equal to the symbol period.

13. A signal shaping circuit for shaping amplitude shift keyed digital pulses of a digital data stream comprised of a plurality of symbols, the signal shaping circuit generating an output signal having sinusoidally shaped transition regions between logic level transitions of the digital data stream, said circuit comprising:
   - an input lead receiving each of the digital pulses of the digital data stream;
   - a shift register having an input connected to receive each of the digital pulses of the digital data stream at the input lead and further having
an output, the shift register shifting data pulses therethrough to the output thereof in response to a clock signal having a clock period;
a ringing filter circuit having a linear response, the ringing filter circuit receiving each of the digital pulses of the digital data stream provided from the input lead and each of the digital pulses provided at the output of the shift register, the ringing filter circuit having a ringing period about equal to or less than twice the symbol period of the digital data stream, the clock period of the clock signal to the shift register being selected to delay a signal received at the input of the shift register by a delay period about equal to half of the ringing period, the ringing filter generating an output amplitude shift keyed digital data stream directly corresponding to the digital data stream provided at the input lead wherein the output digital data stream has sinusoidally shaped transition regions between logic level transitions thereof.

14. A signal shaping circuit as claimed in claim 13 wherein the ringing filter circuit comprises:
a first resistor;
a second resistor;
an inductor;
a capacitor;
the first resistor connected to receive the digital data stream from the input lead, the second resistor connected to receive the delayed digital pulses from the delay circuit, the inductor having a first lead connected at a common node with the first and second resistors and a second lead connected to the output of the ringing filter circuit, the capacitor being connected in a non-series circuit branch extending from the output of the ringing filter circuit.

15. A signal shaping circuit as claimed in claim 14 wherein the capacitor is connected between the output of the ringing filter circuit and circuit ground.

16. A signal shaping circuit as claimed in claim 13 wherein the shift register is a one bit shift register and the clock period is about equal to half of the ringing period.

17. A signal shaping circuit as claimed in claim 14 wherein the shift register is a one bit shift register and the clock period is about equal to half of the ringing period.

18. A signal shaping circuit as claimed in claim 13 wherein the ringing period is equal to the symbol period.
19. A signal shaping circuit as claimed in claim 13 wherein the ringing period is equal to about one symbol period.

20. A signal shaping circuit as claimed in claim 13 wherein the digital data stream is in a binary format.

21. A signal shaping circuit as claimed in claim 20 wherein the ringing filter circuit comprises:
   a first resistor;
   a second resistor;
   an inductor;
   a capacitor;
   the first resistor connected to receive the digital data stream from the input lead, the second resistor connected to receive the delayed digital pulses from the delay circuit, the inductor having a first lead connected at a common node with the first and second resistors and a second lead connected to the output of the ringing filter circuit, the capacitor being connected in a non-series circuit branch extending from the output of the ringing filter circuit.
22. A signal shaping circuit as claimed in claim 21 wherein the capacitor is connected between the output of the ringing filter circuit and circuit ground.

23. A signal shaping circuit as claimed in claim 20 wherein the shift register is a one bit shift register and the clock period is about equal to half of the ringing period.

24. A signal shaping circuit as claimed in claim 21 wherein the shift register is a one bit shift register and the clock period is about equal to half of the ringing period.

25. A signal shaping circuit as claimed in claim 20 wherein the ringing period is equal to the symbol period.

26. A signal shaping circuit as claimed in claim 20 wherein the ringing period is equal to about one symbol period.

27. A signal shaping circuit for shaping amplitude shift keyed digital pulses of a plurality of digital data streams each comprised of a plurality of symbols, the signal shaping circuit generating an output signal having sinusoidally shaped transition regions between logic level transitions of an output digital
data stream generated from the plurality of digital data streams, said circuit comprising:
a plurality of input leads each receiving data pulses from a respective one of the plurality of digital data streams;
a delay circuit comprising a plurality of input lines, each input line receiving data pulses from a respective one of the plurality of digital data streams and, after a predefined time delay, outputting delayed digital pulses corresponding to each of the digital pulses received at the input leads on respective corresponding output lines;
a ringing filter circuit having a linear response, the ringing filter circuit receiving each of the digital pulses provided at the input leads and each of the digital pulses provided at the outputs of the delay circuit, the ringing filter circuit having a ringing period about equal to or less than twice the symbol period of the digital data streams, the predefined delay of the delay circuit being about equal to half of the ringing period, the ringing filter circuit generating an output amplitude shift keyed digital data stream directly corresponding to the digital data streams provided at the input leads wherein the output digital data stream has sinusoidally shaped transition regions between logic level transitions thereof.
28. A signal shaping circuit as claimed in claim 27 wherein the output digital data stream comprises \( N \) levels wherein \( N > 2 \).

29. A signal shaping circuit as claimed in claim 27 wherein each of the plurality of digital data streams is a binary data stream.

30. A signal shaping circuit as claimed in claim 27 wherein the ringing filter circuit comprises:

    a first plurality of resistors each having a first lead connected to receive pulses from and respectively associated with each output of the delay circuit, each of the first plurality of resistors having a respective second lead;

    a second plurality of resistors each having a first lead connected to receive pulses from and respectively associated with each input lead, each of the second plurality of resistors having a respective second lead;

    each of the second leads of the first and second plurality of resistors being connected to a common node input to an inductor and capacitor connected in a low-pass filter configuration.
31. A signal shaping circuit for shaping non-return to zero (NRZ) digital pulses to form an output signal having sinusoidally shaped transition regions between logic levels, said circuit comprising:

an input lead receiving an NRZ input digital pulse having non-sinusoidally shaped transition regions between logic levels;

a delay module receiving said input digital pulse from said input lead and, after a predefined time delay, outputting a corresponding delayed digital pulse;

a conversion module, in response to said input digital pulse and said delayed digital pulse, producing corresponding input and delayed component signal waveforms, respectively, having sinusoidally shaped transition regions between at least first and second states, said conversion module superimposing said input and delayed component waveforms over one another to form a resultant output signal having substantially sinusoidally shape transition regions between at least first and second amplitudes.

32. A circuit according to claim 31, wherein said conversion module includes a linear circuit producing component waveforms in response to incoming digital pulses.
33. A circuit according to claim 31, wherein said conversion module includes an LC circuit.

34. A circuit according to claim 31, wherein said delay module includes a one-bit shift register.

35. A circuit according to claim 31, wherein said input lead includes first and second input leads receiving first and second streams of NRZ input digital pulses; and wherein said delay module includes at least two one-bit shift registers aligned in parallel to receive said first and second streams of input digital pulses and, after predefined time delays, outputting corresponding first and second delayed digital pulses, said conversion module, in response to said first and second input digital pulses and said first and second delayed digital pulses, producing a resultant output signal having at least four potential amplitudes.

36. A circuit according to claim 31, wherein said conversion module includes first and second resistors for adjusting amplitudes of said input digital pulse and said delayed digital pulse such that said input and delayed component waveforms offset one another after a predefined time interval.
37. A circuit according to claim 31, wherein said delay module includes a one bit shift register and said predefined time delay is no greater than a pulse width of an NRZ data pulse.

38. A circuit according to claim 31, wherein said input lead supplies parallel streams of first and second input digital pulses, and wherein said delay module applies parallel streams of delayed digital pulses, said conversion module including at least four resistors for adjusting amplitudes of said first and second input and delayed digital pulses.
FIG. 12

INPUT DATA STREAM

BASEBOARD FILTER

MODULATOR

OUTPUT FILTER

TRANSMISSION MEDIUM

DEMODULATOR

BASEBOARD FILTER

IF FILTER

IF

LO1

LO3

LO2

SUBSTITUTE SHEET (RULE 26)
### A. CLASSIFICATION OF SUBJECT MATTER

<table>
<thead>
<tr>
<th>IPC(6)</th>
<th>US Cl.</th>
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<tr>
<td>HO3M 176, HO3K 5/00</td>
<td>327/100, 165, 167, 311, 552, 558, 559</td>
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According to International Patent Classification (IPC) or to both national classification and IPC

### B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

| U.S. | 327/100, 165, 167, 311, 552, 558, 559 |

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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<td>1-38.</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

Date of the actual completion of the international search: 11 JUNE 1998

Date of mailing of the international search report: 30 JUL 1998

Name and mailing address of the ISA/US

Commissioner of Patents and Trademarks

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Authorized officer

Telephone No. (703) 305-7900

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US98/05583

INTERNATIONAL SEARCH REPORT

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