



(51) International Patent Classification:

H01L 31/072 (2006.01) H01L 31/0392 (2006.01)
H01L 31/0376 (2006.01) H01L 31/18 (2006.01)

(21) International Application Number:

PCT/US2016/023315

(22) International Filing Date:

18 March 2016 (18.03.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

14/671,781 27 March 2015 (27.03.2015) US

(71) Applicant: SUNPOWER CORPORATION [US/US]; 77
Rio Robles, San Jose, California 95134 (US).

(72) Inventors: WESTERBERG, Staffan; 1042 Valley Forge
Drive, Sunnyvale, California 94087 (US). RIM, Seung
Bum; 1618 San Hill Road, Apt. 319, Palo Alto, California
94304 (US).

(74) Agents: VINCENT, Lester J. et al.; BLAKELY SOKO-
LOFF TAYLOR & ZAFMAN LLP, 1279 Oakmead Park-
way, Sunnyvale, California 94085 (US).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: SOLAR CELL EMITTER REGION FABRICATION WITH DIFFERENTIATED P-TYPE AND N-TYPE ARCHITECTURES AND INCORPORATING A MULTI-PURPOSE PASSIVATION AND CONTACT LAYER

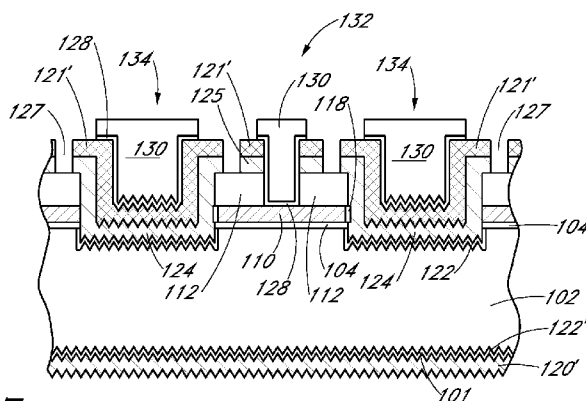


FIG. 7

(57) Abstract: Methods of fabricating solar cell emitter regions with differentiated P-type and N-type architectures and incorporating a multi-purpose passivation and contact layer, and resulting solar cells, are described. In an example, a solar cell includes a substrate having a light-receiving surface and a back surface. A P-type emitter region is disposed on the back surface of the substrate. An N-type emitter region is disposed in a trench formed in the back surface of the substrate. An N-type passivation layer is disposed on the N-type emitter region. A first conductive contact structure is electrically connected to the P-type emitter region. A second conductive contact structure is electrically connected to the N-type emitter region and is in direct contact with the N-type passivation layer.



SOLAR CELL EMITTER REGION FABRICATION WITH DIFFERENTIATED P-TYPE AND N-TYPE ARCHITECTURES AND INCORPORATING A MULTI-PURPOSE PASSIVATION AND CONTACT LAYER

TECHNICAL FIELD

[0001] Embodiments of the present disclosure are in the field of renewable energy and, in particular, methods of fabricating solar cell emitter regions with differentiated P-type and N-type architectures and incorporating a multi-purpose passivation and contact layer, and the resulting solar cells.

BACKGROUND

[0002] Photovoltaic cells, commonly known as solar cells, are well known devices for direct conversion of solar radiation into electrical energy. Generally, solar cells are fabricated on a semiconductor wafer or substrate using semiconductor processing techniques to form a p-n junction near a surface of the substrate. Solar radiation impinging on the surface of, and entering into, the substrate creates electron and hole pairs in the bulk of the substrate. The electron and hole pairs migrate to p-doped and n-doped regions in the substrate, thereby generating a voltage differential between the doped regions. The doped regions are connected to conductive regions on the solar cell to direct an electrical current from the cell to an external circuit coupled thereto.

[0003] Efficiency is an important characteristic of a solar cell as it is directly related to the capability of the solar cell to generate power. Likewise, efficiency in producing solar cells is directly related to the cost effectiveness of such solar cells. Accordingly, techniques for increasing the efficiency of solar cells, or techniques for increasing the efficiency in the manufacture of solar cells, are generally desirable. Some embodiments of the present disclosure allow for increased solar cell manufacture efficiency by providing novel processes for fabricating solar cell structures. Some embodiments of the present disclosure allow for increased solar cell efficiency by providing novel solar cell structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figures 1-7 illustrate cross-sectional views of various stages in the fabrication of a solar cell, in accordance with an embodiment of the present disclosure, wherein:

[0005] Figure 1 illustrates a cross-sectional view of a stage in solar cell fabrication involving forming a P-type silicon layer on a first thin dielectric layer formed on a back surface of a substrate, and forming an insulating layer on the P-type silicon layer;

[0006] Figure 2 illustrates a cross-sectional view of the structure of Figure 1 following patterning of the insulating layer and the P-type silicon layer to form P-type silicon regions having an insulating cap thereon;

[0007] Figure 3 illustrates a cross-sectional view of the structure of Figure 2 following texturing of the surfaces of the trenches to form texturized recesses or trenches having texturized surfaces within the substrate;

[0008] Figure 4 illustrates a cross-sectional view of the structure of Figure 3 following formation of second and third thin dielectric layers and an N-type silicon layer;

[0009] Figure 5 illustrates a cross-sectional view of the structure of Figure 4 following formation of an N-type amorphous silicon layer on the N-type silicon layer;

[0010] Figure 6 illustrates a cross-sectional view of the structure of Figure 5 following patterning of the N-type amorphous silicon layer and the N-type silicon layer to form isolated N-type emitter regions and to form contact openings in regions of the N-type amorphous silicon layer and the N-type silicon layer above the insulating cap of the P-type silicon regions; and

[0011] Figure 7 illustrates a cross-sectional view of the structure of Figure 6 following formation of a plurality of conductive contacts.

[0012] Figure 8 is a flowchart listing operations in a method of fabricating a solar cell as corresponding to Figures 1-7, in accordance with an embodiment of the present disclosure.

[0013] Figure 9 is a flowchart listing operations in another method of fabricating a solar cell, in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0014] The following detailed description is merely illustrative in nature and is not intended to limit the embodiments of the subject matter or the application and uses of such embodiments. As used herein, the word “exemplary” means “serving as an example, instance, or illustration.” Any implementation described herein as exemplary is not necessarily to be construed as preferred or advantageous over other implementations. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

[0015] This specification includes references to “one embodiment” or “an embodiment.” The appearances of the phrases “in one embodiment” or “in an embodiment” do

not necessarily refer to the same embodiment. Particular features, structures, or characteristics may be combined in any suitable manner consistent with this disclosure.

[0016] Terminology. The following paragraphs provide definitions and/or context for terms found in this disclosure (including the appended claims):

[0017] “Comprising.” This term is open-ended. As used in the appended claims, this term does not foreclose additional structure or steps.

[0018] “Configured To.” Various units or components may be described or claimed as “configured to” perform a task or tasks. In such contexts, “configured to” is used to connote structure by indicating that the units/components include structure that performs those task or tasks during operation. As such, the unit/component can be said to be configured to perform the task even when the specified unit/component is not currently operational (e.g., is not on/active). Reciting that a unit/circuit/component is “configured to” perform one or more tasks is expressly intended not to invoke 35 U.S.C. §112, sixth paragraph, for that unit/component.

[0019] “First,” “Second,” etc. As used herein, these terms are used as labels for nouns that they precede, and do not imply any type of ordering (e.g., spatial, temporal, logical, etc.). For example, reference to a “first” solar cell does not necessarily imply that this solar cell is the first solar cell in a sequence; instead the term “first” is used to differentiate this solar cell from another solar cell (e.g., a “second” solar cell).

[0020] “Coupled” – The following description refers to elements or nodes or features being “coupled” together. As used herein, unless expressly stated otherwise, “coupled” means that one element/node/feature is directly or indirectly joined to (or directly or indirectly communicates with) another element/node/feature, and not necessarily mechanically.

[0021] “Inhibit” – As used herein, inhibit is used to describe a reducing or minimizing effect. When a component or feature is described as inhibiting an action, motion, or condition it may completely prevent the result or outcome or future state completely. Additionally, “inhibit” can also refer to a reduction or lessening of the outcome, performance, and/or effect which might otherwise occur. Accordingly, when a component, element, or feature is referred to as inhibiting a result or state, it need not completely prevent or eliminate the result or state.

[0022] In addition, certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, and “below” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, “side”, “outboard”, and “inboard” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated

drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

[0023] Methods of fabricating solar cell emitter regions with differentiated P-type and N-type architectures and incorporating a multi-purpose passivation and contact layer, and the resulting solar cells, are described herein. In the following description, numerous specific details are set forth, such as specific process flow operations, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known fabrication techniques, such as lithography and patterning techniques, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

[0024] Disclosed herein are solar cells. In one embodiment, a solar cell includes a substrate having a light-receiving surface and a back surface. A P-type emitter region is disposed on the back surface of the substrate. An N-type emitter region is disposed in a trench formed in the back surface of the substrate. An N-type passivation layer is disposed on the N-type emitter region. A first conductive contact structure is electrically connected to the P-type emitter region. A second conductive contact structure is electrically connected to the N-type emitter region and is in direct contact with the N-type passivation layer.

[0025] In another embodiment, a solar cell includes a substrate having a light-receiving surface and a back surface. An N-type emitter region is disposed on the back surface of the substrate. A P-type emitter region is disposed in a trench formed in the back surface of the substrate. A P-type passivation layer is disposed on the P-type emitter region. A first conductive contact structure is electrically connected to the N-type emitter region. A second conductive contact structure is electrically connected to the P-type emitter region and is in direct contact with the P-type passivation layer.

[0026] In another embodiment, a back contact solar cell includes a substrate having a light-receiving surface and a back surface. A P-type polycrystalline silicon emitter region is disposed on a first thin dielectric layer disposed on the back surface of the substrate. An N-type polycrystalline silicon emitter region is disposed on a second thin dielectric layer disposed in a trench formed in the back surface of the substrate. A third thin dielectric layer is disposed laterally directly between the N-type and P-type polycrystalline silicon emitter regions. An N-type silicon layer is disposed on the N-type polycrystalline silicon emitter region. A first

conductive contact structure is electrically connected to the P-type polycrystalline silicon emitter region. A second conductive contact structure is electrically connected to the N-type polycrystalline silicon emitter region and in direct contact with the N-type silicon layer.

[0027] Also disclosed herein are methods of fabricating solar cells. In one embodiment, a method of fabricating alternating N-type and P-type emitter regions of a solar cell involves forming a P-type silicon layer on a first thin dielectric layer formed on a back surface of a substrate. The method also involves forming an insulating layer on the P-type silicon layer. The method also involves patterning the insulating layer and the P-type silicon layer to form P-type silicon regions having an insulating cap thereon. The method also involves forming a second thin dielectric layer on exposed sides of the P-type silicon regions. The method also involves forming an N-type silicon layer on a third thin dielectric layer formed on the back surface of the substrate, and on the second thin dielectric layer and the insulating cap of the P-type silicon regions. The method also involves forming an N-type amorphous silicon layer on the N-type silicon layer. The method also involves patterning the N-type amorphous silicon layer and the N-type silicon layer to form isolated N-type emitter regions and to form contact openings in regions of the N-type amorphous silicon layer and the N-type silicon layer above the insulating cap of the P-type silicon regions. The method also involves patterning the insulating cap through the contact openings to expose portions of the P-type silicon regions. The method also involves forming conductive contacts to the P-type silicon regions and to the N-type emitter regions, the conductive contacts to the P-type silicon regions formed in the contact openings, and the conductive contacts to the N-type emitter regions formed in direct contact with the N-type amorphous silicon layer of the N-type emitter regions.

[0028] One or more embodiments described herein are directed to fabrication and use of an amorphous silicon (a-Si) layer for passivation of and to enable a simplified contact process for an underlying a polycrystalline silicon emitter region of a differentiated or hybrid architecture. In one particular embodiment, the amorphous silicon layer is included to provide hydrogen for passivation of the underlying a polycrystalline silicon emitter region. In one particular embodiment, effectively no contact process is required for an underlying emitter regions since suitable electrical contact is made to the amorphous silicon layer.

[0029] To provide context, one issue for differentiated or hybrid back contact solar cell architecture is the lack of a hydrogen source for N-type polycrystalline silicon emitters. A hydrogen source may be used to reduce an otherwise high saturation current density (J_0), which can be a particular issue for N-type emitter regions. The inclusion of silicon nitride (SiN) or other dielectrics which can provide hydrogen may not be the best approach since such dielectric

layers require additional contact process consideration for forming conductive contacts to an underlying emitter region.

[0030] Addressing one or more of the above issues, in an embodiment, a layer of N-type a-Si is deposited on an N-type polycrystalline silicon emitter region. The N-type a-Si layer is included to provide hydrogen to the underlying N-type emitter region. The N-type a-Si layer is also included for maintaining direct metal contact without having to implement a contact opening process. Accordingly, the N-type a-Si may be incorporated without having to modify a typical hybrid process flow metallization process. In one embodiment, the N-type a-Si protects the underlying N-type emitter region during contact formation, e.g., by inhibiting a reaction between an aluminum layer and the underlying N-type emitter region.

[0031] In an exemplary process flow, Figures 1-7 illustrate cross-sectional views of various stages in the fabrication of a solar cell, in accordance with an embodiment of the present disclosure. Figure 8 is a flowchart 800 listing operations in a method of fabricating a solar cell as corresponding to Figures 1-7, in accordance with an embodiment of the present disclosure.

[0032] Referring to Figure 1 and corresponding operation 802 of flowchart 800, a method of fabricating alternating N-type and P-type emitter regions of a solar cell involves forming a P-type silicon layer 106 on a first thin dielectric layer 104 formed on a back surface of a substrate 102.

[0033] In an embodiment, the substrate 102 is a monocrystalline silicon substrate, such as a bulk single crystalline N-type doped silicon substrate. It is to be appreciated, however, that substrate 102 may be a layer, such as a multi-crystalline silicon layer, disposed on a global solar cell substrate. In an embodiment, the first thin dielectric layer 104 is a thin oxide layer such as a tunnel dielectric silicon oxide layer having a thickness of approximately 2 nanometers or less.

[0034] In an embodiment, the P-type silicon layer 106 is a P-type polycrystalline silicon layer that is doped either through *in situ* doping, post deposition implanting, or a combination thereof. In another embodiment the P-type silicon layer 106 is first formed as an amorphous silicon layer such as a hydrogenated silicon layer represented by a-Si:H which is implanted with dopants subsequent to deposition of the amorphous silicon layer. In one such embodiment, the P-type silicon layer 106 is subsequently annealed (at least at some subsequent stage of the process flow) to ultimately form a P-type polycrystalline silicon layer. In an embodiment, for either a polycrystalline silicon layer or an amorphous silicon layer, if post deposition implantation is performed, the implanting is performed by using ion beam implantation or plasma immersion implantation. In one such embodiment, a shadow mask is

used for the implanting. In a specific embodiment, the P-type conductivity is achieved using boron impurity atoms.

[0035] Referring again to Figure 1 and now to corresponding operation 804 of flowchart 800, an insulating layer 108 is formed on the P-type silicon layer 106. In an embodiment the insulating layer 108 includes silicon dioxide.

[0036] Referring to Figure 2 and corresponding operation 806 of flowchart 800, the insulating layer 108 and the P-type silicon layer 106 are patterned to form first P-type silicon regions 110 each having an insulating cap 112 thereon. In an embodiment, a laser ablation process (e.g., direct write) is used to pattern the insulating layer 108 and the P-type silicon layer 106. Where applicable, in one embodiment, the first thin dielectric layer 104 is also patterned in the process, as is depicted in Figure 2.

[0037] In an embodiment, the insulating layer 108 and the P-type silicon layer 106 are patterned using a laser ablation process. In one such embodiment, the laser ablation process exposes a plurality of regions 109 of an N-type monocrystalline silicon substrate 102. Each of the plurality of regions 109 of the N-type monocrystalline silicon substrate 102 can be viewed as a plurality of non-continuous trenches formed in the N-type monocrystalline silicon substrate 102. The option that the trenches 109 have a depth or thickness 111 into the substrate 102 is depicted in Figure 2. In one such embodiment, each of the plurality of non-continuous trenches 109 is formed to a non-zero depth 111 less than approximately 10 microns into the substrate 102 upon laser ablation. In an embodiment, using the laser ablation process provides each of the plurality of non-continuous trenches with a width (e.g., maximum diameter) approximately in the range of 30 – 60 microns. In an embodiment, the laser ablation process involves using a laser beam having an approximately Gaussian profile or having an approximately flat-top profile.

[0038] Referring to Figure 3, optionally, the surfaces of the trenches 109 may be texturized to form texturized recesses or trenches 114 having texturized surfaces 116 within the substrate 102. In a same or similar process, a light receiving surface 101 of the substrate 102 may also be texturized, as is depicted in Figure 3. In an embodiment, a hydroxide-based wet etchant is used to form at least a portion of the recesses 114 and/or to texturize exposed portions of the substrate 102. A texturized surface may be one which has a regular or an irregular shaped surface for scattering incoming light, decreasing the amount of light reflected off of the light-receiving and/or exposed surfaces of the solar cell. It is to be appreciated, however, that the texturizing of the back surface and even the recess formation may be omitted

from the process flow. It is also to be appreciated that, if applied, the texturizing may increase the depth of the trenches 109 from the originally formed depth.

[0039] Referring to Figure 4 and corresponding operation 808 of flowchart 800, a second thin dielectric layer 118 is formed on exposed sides of the P-type silicon regions 118. In an embodiment, the second thin dielectric layer 118 is formed in an oxidation process and is a thin oxide layer such as a tunnel dielectric silicon oxide layer having a thickness of approximately 2 nanometers or less. In another embodiment, the second thin dielectric layer 118 is formed in a deposition process and is a thin silicon nitride layer or silicon oxynitride layer.

[0040] Referring again to Figure 4 and now to corresponding operation 810 of flowchart 700, an N-type silicon layer 120 is formed on a third thin dielectric layer 122 formed on the exposed portions of the back surface of the substrate 102 (e.g., formed in each of the plurality of non-continuous trenches 109 of each of the plurality of regions of the N-type monocrystalline silicon substrate 102). The N-type silicon layer 120 is further formed on the second thin dielectric layer 118 and on the insulating cap 112 of the P-type silicon regions 110. The N-type silicon layer 120 covers (from a top-down perspective) the trench regions 109.

[0041] Referring again to Figure 4, corresponding thin dielectric layer 122' and N-type silicon layer 120' may also be formed on the light-receiving surface 101 of the substrate 102, in same or similar process operations. Additionally, although not depicted, an anti-reflective coating (ARC) layer may be formed on the corresponding N-type silicon layer 120'.

[0042] In an embodiment, the third thin dielectric layer 122 is formed in an oxidation process and is a thin oxide layer such as a tunnel dielectric silicon oxide layer having a thickness of approximately 2 nanometers or less. In an embodiment, the N-type silicon layer 120 is a polycrystalline silicon layer that is doped either through *in situ* doping, post deposition implanting, or a combination thereof. In another embodiment the N-type silicon layer 120 is an amorphous silicon layer such as a hydrogenated silicon layer represented by a-Si:H which is implanted with dopants subsequent to deposition of the amorphous silicon layer. In one such embodiment, the N-type silicon layer 120 is subsequently annealed (at least at some subsequent stage of the process flow) to ultimately form an N-type polycrystalline silicon layer. In an embodiment, for either a polycrystalline silicon layer or an amorphous silicon layer, if post deposition implantation is performed, the implanting is performed by using ion beam implantation or plasma immersion implantation. In one such embodiment, a shadow mask is used for the implanting. In a specific embodiment, the N-type conductivity is achieved using phosphorus atoms or arsenic impurity atoms.

[0043] Referring to Figure 5 and corresponding operation 812 of flowchart 800, an N-type amorphous silicon layer 121 is formed on the N-type silicon layer 120. In an embodiment, the N-type amorphous silicon layer 121 is formed by depositing N-type amorphous silicon using plasma-enhanced chemical vapor deposition (PECVD) at a temperature below approximately 400 degrees Celsius. In one such embodiment, the N-type amorphous silicon layer 121 is formed to have a total hydrogen concentration approximately in the range of 5-20% of total film composition, and a total phosphorous dopant concentration approximately in the range of $1\text{E}19 - 5\text{E}20$ atoms/cm³. In one embodiment, the N-type amorphous silicon layer 121 is formed to a thickness approximately in the range of 5-50 nanometers. In another embodiment, however, the N-type amorphous silicon layer 121 is formed to a thickness of greater than approximately 50 nanometers.

[0044] Referring to Figure 6 and corresponding operation 814 of flowchart 800, the N-type amorphous silicon layer 121 and the N-type silicon layer 120 are patterned to form to form patterned N-type amorphous silicon layer 121' and isolated N-type emitter regions 124. The patterning is used to form contact openings 126 and isolation openings 127 in regions of the patterned N-type amorphous silicon layer 121' and the N-type silicon layer (formerly layer 120) above the insulating cap 112 of the P-type silicon regions 110. In an embodiment, each isolated N-type silicon region 124 is electrically coupled to a corresponding one (or more) of the plurality of regions 109 of the N-type monocrystalline silicon substrate 102. In an embodiment, discrete regions of N-type silicon 125 may remain as an artifact of the patterning process. In an embodiment, a laser ablation process is used to pattern the N-type amorphous silicon layer 121 and the N-type silicon layer 120.

[0045] Referring again to Figure 6 and now to corresponding operation 816 of flowchart 800, the insulating cap 112 is patterned through the contact openings 126 to expose portions of the P-type silicon regions 110. In an embodiment, the insulating cap 112 is patterned using a laser ablation process. For example, in one embodiment, a first laser pass is used to pattern the N-type amorphous silicon layer 121 and the N-type silicon layer 120, including initiating formation of the contact opening 126. A second laser pass in the same location as the initiated contact opening 126 is the used to pattern the insulating cap 112, providing contact opening 126.

[0046] Referring to Figure 7 and corresponding operation 818 of flowchart 800, a plurality of conductive contacts is formed, each conductive contact electrically connected to one of the P-type silicon regions or one of the isolated N-type silicon regions. In particular, conductive contacts 132 are formed in the contact openings 126 for the P-type silicon regions

110. In one embodiment, the conductive contacts 130 are in directed contact with the corresponding P-type silicon regions 110. Conductive contacts 134 are formed on portions of the patterned N-type amorphous silicon layer 121' for the N-type emitter regions (isolated N-type emitter regions 124 of the N-type silicon layer 120). In one embodiment, the conductive contacts 134 are formed in direct contact with the N-type amorphous silicon layer 121' without exposing the surface of the isolated N-type emitter regions 124.

[0047] In an exemplary embodiment, a metal seed layer 128 is formed on the exposed portions of the P-type silicon regions 110 and on the isolated N-type silicon regions 124. A metal layer 130 is then plated on the metal seed layer to form conductive contacts 132 and 134, respectively, for the P-type silicon regions 110 and the isolated N-type silicon regions 124. In an embodiment, the metal seed layer 128 is an aluminum-based metal seed layer, and the metal layer 130 is a copper layer. In an embodiment, a mask is first formed to expose only the exposed portions of the P-type silicon regions 110 and the isolated N-type silicon regions 124 in order to direct the metal seed layer 128 formation to restricted locations.

[0048] Thus, one or more embodiments described herein are directed to forming P+ and N+ polysilicon emitter regions for a solar cell where the respective structures of the P+ and N+ polysilicon emitter regions are different from one another. Such an approach can be implemented to simplify a solar cell fabrication process. Furthermore, the resulting structure may provide a lower breakdown voltage and lower power losses associated as compared with other solar cell architectures.

[0049] With reference again to Figure 7, in an embodiment, a finalized solar cell includes a substrate 102 having a light-receiving surface 101 and a corresponding back surface. A P-type polycrystalline silicon emitter region 110 is disposed on a first thin dielectric layer 104 disposed on the back surface of the substrate 102. An N-type polycrystalline silicon emitter region 124 is disposed on a second thin dielectric layer 122 disposed in a trench (shown as recess in cross-sectional view of Figure 7) in the back surface of the substrate 102. An N-type silicon layer 121' is disposed on the N-type polycrystalline silicon emitter region 124.

[0050] In an embodiment, the N-type silicon layer 121' is included as a multi-purpose passivation and contact layer. In an embodiment, the substrate 102 is an N-type monocrystalline silicon substrate. In an embodiment, the solar cell is a back contact solar cell, as is depicted in Figure 7. In an embodiment, the N-type silicon layer 121' is further disposed over, but not in contact with, the P-type polycrystalline silicon emitter region 110, as is also depicted in Figure 7.

[0051] In an embodiment, the N-type silicon layer 121' is an N-type amorphous silicon layer. In one such embodiment, a total composition of the N-type amorphous silicon layer has a total hydrogen concentration approximately in the range of 5-20% of total film composition. In another embodiment, a total composition of the N-type amorphous silicon layer has a total phosphorous dopant concentration approximately in the range of $1\text{E}19 - 5\text{E}20$ atoms/cm³.

[0052] In an embodiment, the N-type silicon layer 121' has a thickness approximately in the range of 5-50 nanometers. In an embodiment, the N-type polycrystalline silicon emitter region 124 has a thickness of approximately 30 nanometers, and the N-type silicon layer 121' has a thickness of approximately 20 nanometers. In one embodiment, the N-type polycrystalline silicon emitter region 124 is formed in a trench having a texturized surface, as is depicted in Figure 7. In another embodiment, the N-type amorphous silicon layer 121' has a thickness of greater than approximately 50 nanometers.

[0053] Referring again to Figure 7, in an embodiment, the solar cell further includes a third thin dielectric layer 118 disposed laterally directly between the first 110 and second 124 polycrystalline silicon emitter regions. In an embodiment, the solar cell further includes a first conductive contact structure 132 electrically connected to the P-type polycrystalline silicon emitter region 110. A second conductive contact structure 134 electrically connected to the N-type polycrystalline silicon emitter region 124. The second conductive contact structure 134 is in direct contact with the N-type silicon layer 121'.

[0054] In an embodiment, the solar cell further includes an insulator layer 112 disposed on the P-type polycrystalline silicon emitter region 110, as is depicted in Figure 7. The first conductive contact structure 132 is disposed through the insulator layer 112. In one such embodiment, a portion of the N-type polycrystalline silicon emitter region 124 overlaps the insulator layer 112 but is separated from the first conductive contact structure 132, as is depicted in Figure 7. In a further embodiment, an N-type polycrystalline silicon region 125 (e.g., as an isolated portion from the N-type polycrystalline silicon emitter region 124) is disposed on the insulator layer 112. A portion of the N-type silicon layer 121' is disposed on the portion of the N-type polycrystalline silicon emitter region 124 that overlaps the insulator layer 112 and on the N-type polycrystalline silicon region 125. The first conductive contact structure 132 is disposed through the N-type silicon layer 121', through the N-type polycrystalline silicon region 125 of the second conductivity type, and through the insulator layer 112, as is depicted in Figure 7.

[0055] Referring again to Figure 7, the solar cell further includes a fourth thin dielectric layer 122' disposed on the light-receiving surface 101 of the substrate 102. A polycrystalline

silicon layer 120' is disposed on the fourth thin dielectric layer 122', which may be an N-type polycrystalline silicon layer 120'. Although, not depicted, an anti-reflective coating (ARC) layer may be disposed on the polycrystalline silicon layer 102'. In a particular embodiment, the substrate 102 is an N-type monocrystalline silicon substrate, and all of the first, second and third (and, if present, fourth) thin dielectric layers include silicon dioxide.

[0056] Although certain materials are described specifically with reference to above described embodiments, some materials may be readily substituted with others with other such embodiments remaining within the spirit and scope of embodiments of the present disclosure. For example, in an embodiment, a different material substrate, such as a group III-V material substrate, can be used instead of a silicon substrate. Additionally, although reference is made significantly to back contact solar cell arrangements, it is to be appreciated that approaches described herein may have application to front contact solar cells as well. In other embodiments, the above described approaches can be applicable to manufacturing of other than solar cells. For example, manufacturing of light emitting diode (LEDs) may benefit from approaches described herein.

[0057] Furthermore, it is to be appreciated that, where N+ and P+ type doping is described specifically, other embodiments contemplated include the opposite conductivity type, e.g., P+ and N+ type doping, respectively. As such, in an embodiment, it is possible to fabricate an architecture having a P-type passivation layer by processing a P-type emitter subsequent to processing an N-type emitter. Such an embodiment may be applicable when a P-type silicon substrate is used. As an example, Figure 9 is a flowchart 900 listing operations in another method of fabricating a solar cell, in accordance with an embodiment of the present disclosure.

[0058] Referring to operation 902 of flowchart 900, a method of fabricating alternating N-type and P-type emitter regions of a solar cell involves forming an N-type silicon layer on a first thin dielectric layer formed on a back surface of a substrate. Referring to operation 904 of flowchart 900, an insulating layer is formed on the N-type silicon layer. Referring to operation 906 of flowchart 900, the insulating layer and the N-type silicon layer are patterned to form first N-type silicon regions each having an insulating cap thereon. Referring to operation 908 of flowchart 900, a second thin dielectric layer is formed on exposed sides of the N-type silicon regions. Referring to corresponding operation 910 of flowchart 900, a P-type silicon layer is formed on a third thin dielectric layer formed on the exposed portions of the back surface of the substrate. Referring to operation 912 of flowchart 900, a P-type amorphous silicon layer is formed on the P-type silicon layer. Referring to operation 914 of flowchart 900, the P-type amorphous silicon layer and the P-type silicon layer are patterned to form a patterned P-type

amorphous silicon layer and isolated P-type emitter regions. Referring to operation 916 of flowchart 900, the insulating cap is patterned through the contact openings to expose portions of the N-type silicon regions. Referring to operation 918 of flowchart 900, a plurality of conductive contacts is formed, each conductive contact electrically connected to one of the N-type silicon regions or one of the isolated P-type silicon regions.

[0059] Thus, methods of fabricating solar cell emitter regions with differentiated P-type and N-type architectures and incorporating a multi-purpose passivation and contact layer, and the resulting solar cells, have been disclosed.

[0060] Although specific embodiments have been described above, these embodiments are not intended to limit the scope of the present disclosure, even where only a single embodiment is described with respect to a particular feature. Examples of features provided in the disclosure are intended to be illustrative rather than restrictive unless stated otherwise. The above description is intended to cover such alternatives, modifications, and equivalents as would be apparent to a person skilled in the art having the benefit of this disclosure.

[0061] The scope of the present disclosure includes any feature or combination of features disclosed herein (either explicitly or implicitly), or any generalization thereof, whether or not it mitigates any or all of the problems addressed herein. Accordingly, new claims may be formulated during prosecution of this application (or an application claiming priority thereto) to any such combination of features. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the appended claims.

CLAIMS

What is claimed is:

1. A solar cell, comprising:
 - a substrate having a light-receiving surface and a back surface;
 - a P-type emitter region disposed on the back surface of the substrate;
 - an N-type emitter region disposed in a trench formed in the back surface of the substrate;
 - an N-type passivation layer disposed on the N-type emitter region;
 - a first conductive contact structure electrically connected to the P-type emitter region; and
 - a second conductive contact structure electrically connected to the N-type emitter region and in direct contact with the N-type passivation layer.
2. The solar cell of claim 1, wherein the N-type passivation layer is an N-type amorphous silicon layer.
3. The solar cell of claim 2, wherein a total composition of the N-type amorphous silicon layer has a total hydrogen concentration approximately in the range of 5-20% of total film composition.
4. The solar cell of claim 2, wherein a total composition of the N-type amorphous silicon layer has a total phosphorous dopant concentration approximately in the range of $1\text{E}19 - 5\text{E}20$ atoms/cm³.
5. The solar cell of claim 1, wherein the N-type passivation layer has a thickness approximately in the range of 5-50 nanometers.
6. A back contact solar cell, comprising:
 - a substrate having a light-receiving surface and a back surface;
 - a P-type polycrystalline silicon emitter region disposed on a first thin dielectric layer disposed on the back surface of the substrate;
 - an N-type polycrystalline silicon emitter region disposed on a second thin dielectric layer disposed in a trench formed in the back surface of the substrate;
 - a third thin dielectric layer disposed laterally directly between the N-type and P-type polycrystalline silicon emitter regions;
 - an N-type silicon layer disposed on the N-type polycrystalline silicon emitter region;

a first conductive contact structure electrically connected to the P-type polycrystalline silicon emitter region; and

a second conductive contact structure electrically connected to the N-type polycrystalline silicon emitter region and in direct contact with the N-type silicon layer.

7. The back contact solar cell of claim 6, wherein the N-type silicon layer is further disposed over, but not in contact with, the P-type polycrystalline silicon emitter region.

8. The back contact solar cell of claim 6, wherein the N-type silicon layer is an N-type amorphous silicon layer.

9. The back contact solar cell of claim 8, wherein a total composition of the N-type amorphous silicon layer has a total hydrogen concentration approximately in the range of 5-20% of total film composition.

10. The back contact solar cell of claim 8, wherein a total composition of the N-type amorphous silicon layer has a total phosphorous dopant concentration approximately in the range of $1\text{E}19 - 5\text{E}20$ atoms/cm³.

11. The back contact solar cell of claim 6, wherein the N-type silicon layer has a thickness approximately in the range of 5-50 nanometers.

12. The back contact solar cell of claim 11, wherein the N-type polycrystalline silicon emitter region has a thickness of approximately 30 nanometers, and the N-type silicon layer has a thickness of approximately 20 nanometers.

13. The back contact solar cell of claim 6, further comprising:

an insulator layer disposed on the P-type polycrystalline silicon emitter region, wherein the first conductive contact structure is disposed through the insulator layer, and wherein a portion of the N-type polycrystalline silicon emitter region and a portion of the N-type silicon layer overlap the insulator layer.

14. The back contact solar cell of claim 6, wherein the trench has a texturized surface.

15. The back contact solar cell of claim 6, further comprising:

a fourth thin dielectric layer disposed on the light-receiving surface of the substrate;
a polycrystalline silicon layer disposed on the fourth thin dielectric layer; and
an anti-reflective coating (ARC) layer disposed on the polycrystalline silicon layer.

16. The back contact solar cell of claim 6, wherein the substrate is an N-type monocrystalline silicon substrate, and wherein all of the first, second and third thin dielectric layers comprise silicon dioxide.

17. A method of fabricating alternating N-type and P-type emitter regions of a solar cell, the method comprising:

forming a P-type silicon layer on a first thin dielectric layer formed on a back surface of a substrate;

forming an insulating layer on the P-type silicon layer;

patterning the insulating layer and the P-type silicon layer to form P-type silicon regions having an insulating cap thereon;

forming a second thin dielectric layer on exposed sides of the P-type silicon regions;

forming an N-type silicon layer on a third thin dielectric layer formed on the back surface of the substrate, and on the second thin dielectric layer and the insulating cap of the P-type silicon regions;

forming an N-type amorphous silicon layer on the N-type silicon layer;

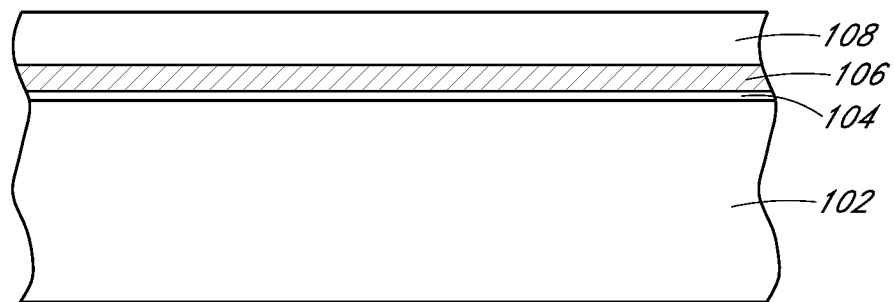
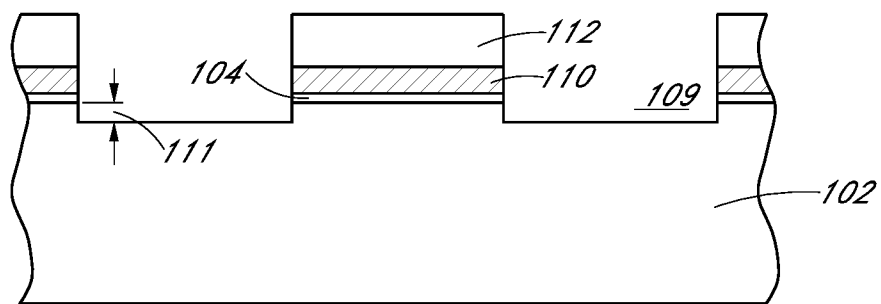
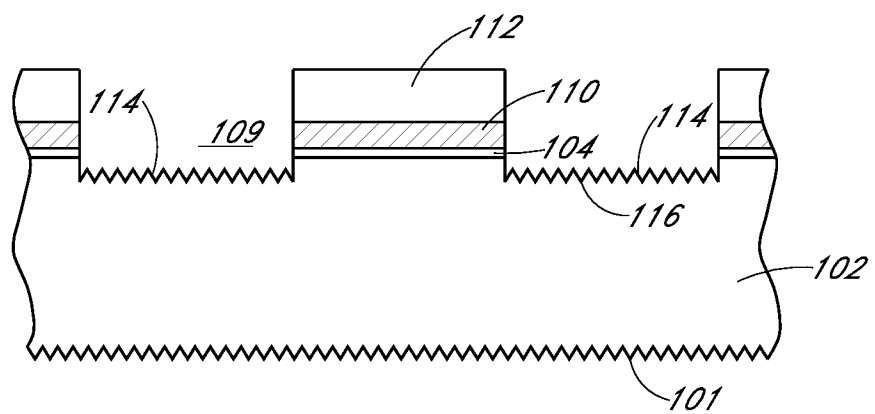
patterning the N-type amorphous silicon layer and the N-type silicon layer to form isolated N-type emitter regions and to form contact openings in regions of the N-type amorphous silicon layer and the N-type silicon layer above the insulating cap of the P-type silicon regions;

patterning the insulating cap through the contact openings to expose portions of the P-type silicon regions;

forming conductive contacts to the P-type silicon regions and to the N-type emitter regions, the conductive contacts to the P-type silicon regions formed in the contact openings, and the conductive contacts to the N-type emitter regions formed in direct contact with the N-type amorphous silicon layer of the N-type emitter regions.

18. The method of claim 17, wherein forming the N-type amorphous silicon layer comprises depositing N-type amorphous silicon by plasma-enhanced chemical vapor deposition (PECVD) at a temperature below approximately 400 degrees Celsius.

19. The method of claim 18, wherein forming the N-type amorphous silicon layer comprises forming an N-type amorphous silicon layer having a total hydrogen concentration approximately in the range of 5-20% of total film composition, and having a total phosphorous dopant concentration approximately in the range of $1\text{E}19 - 5\text{E}20$ atoms/cm³, and to a thickness approximately in the range of 5-50 nanometers.
20. A solar cell fabricated according to the method of claim 17.
21. A solar cell, comprising:
- a substrate having a light-receiving surface and a back surface;
 - an N-type emitter region disposed on the back surface of the substrate;
 - a P-type emitter region disposed in a trench formed in the back surface of the substrate;
 - a P-type passivation layer disposed on the P-type emitter region;
 - a first conductive contact structure electrically connected to the N-type emitter region; and
 - a second conductive contact structure electrically connected to the P-type emitter region and in direct contact with the P-type passivation layer.
22. The solar cell of claim 21, wherein the P-type passivation layer is a P-type amorphous silicon layer.
23. The solar cell of claim 22, wherein a total composition of the P-type amorphous silicon layer has a total hydrogen concentration approximately in the range of 5-20% of total film composition.
24. The solar cell of claim 22, wherein a total composition of the P-type amorphous silicon layer has a total phosphorous dopant concentration approximately in the range of $1\text{E}19 - 5\text{E}20$ atoms/cm³.
25. The solar cell of claim 21, wherein the P-type passivation layer has a thickness approximately in the range of 5-50 nanometers.

*FIG. 1**FIG. 2**FIG. 3*

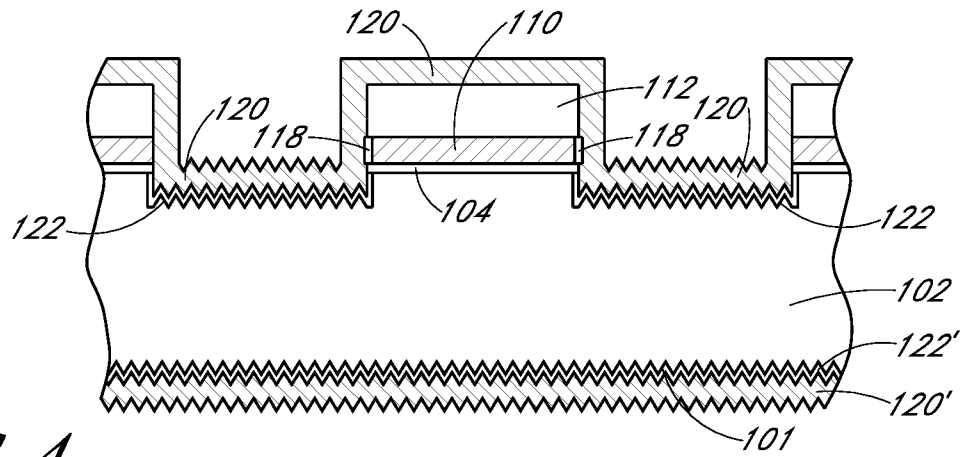


FIG. 4

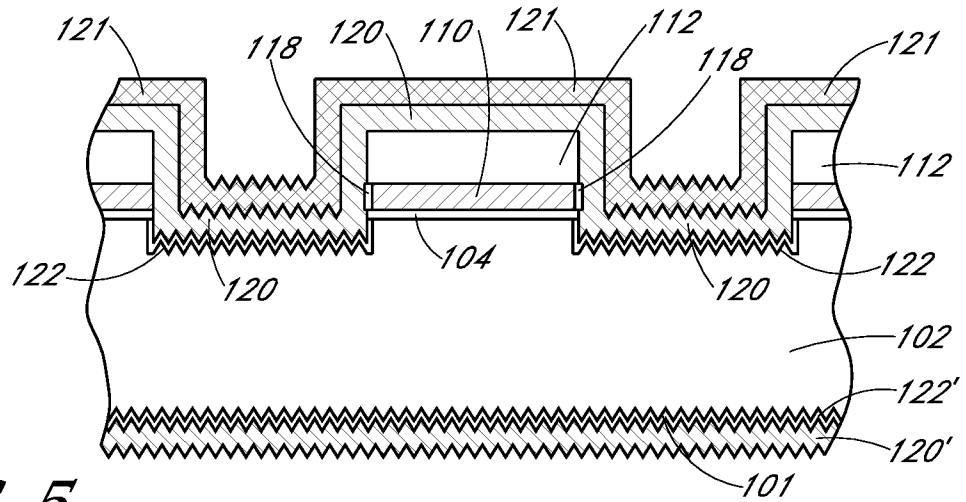


FIG. 5

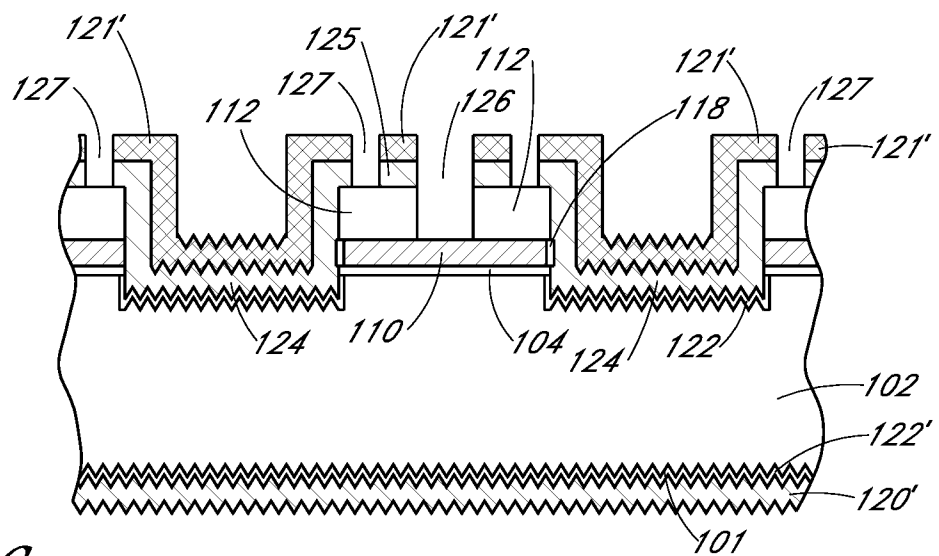


FIG. 6

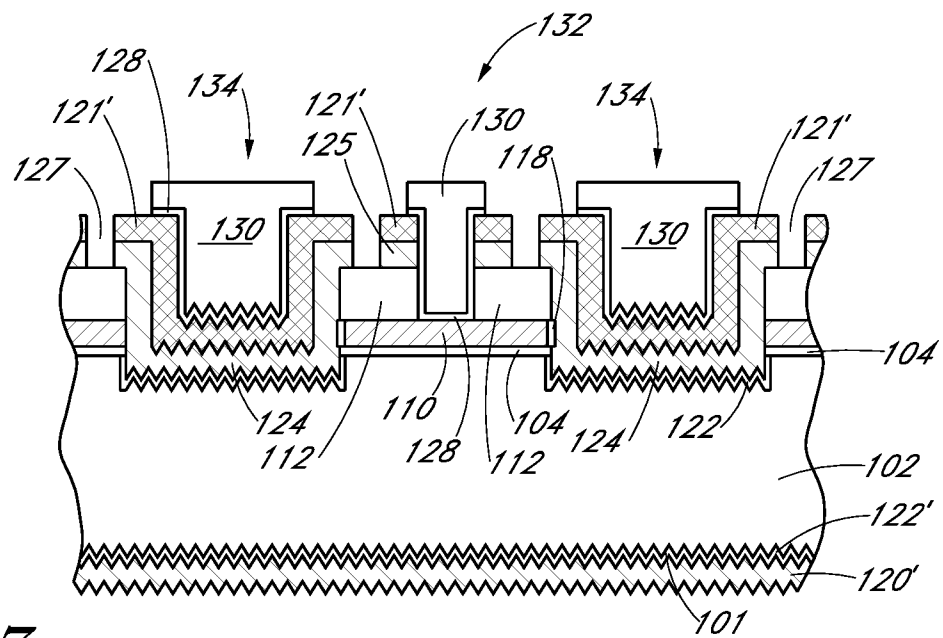
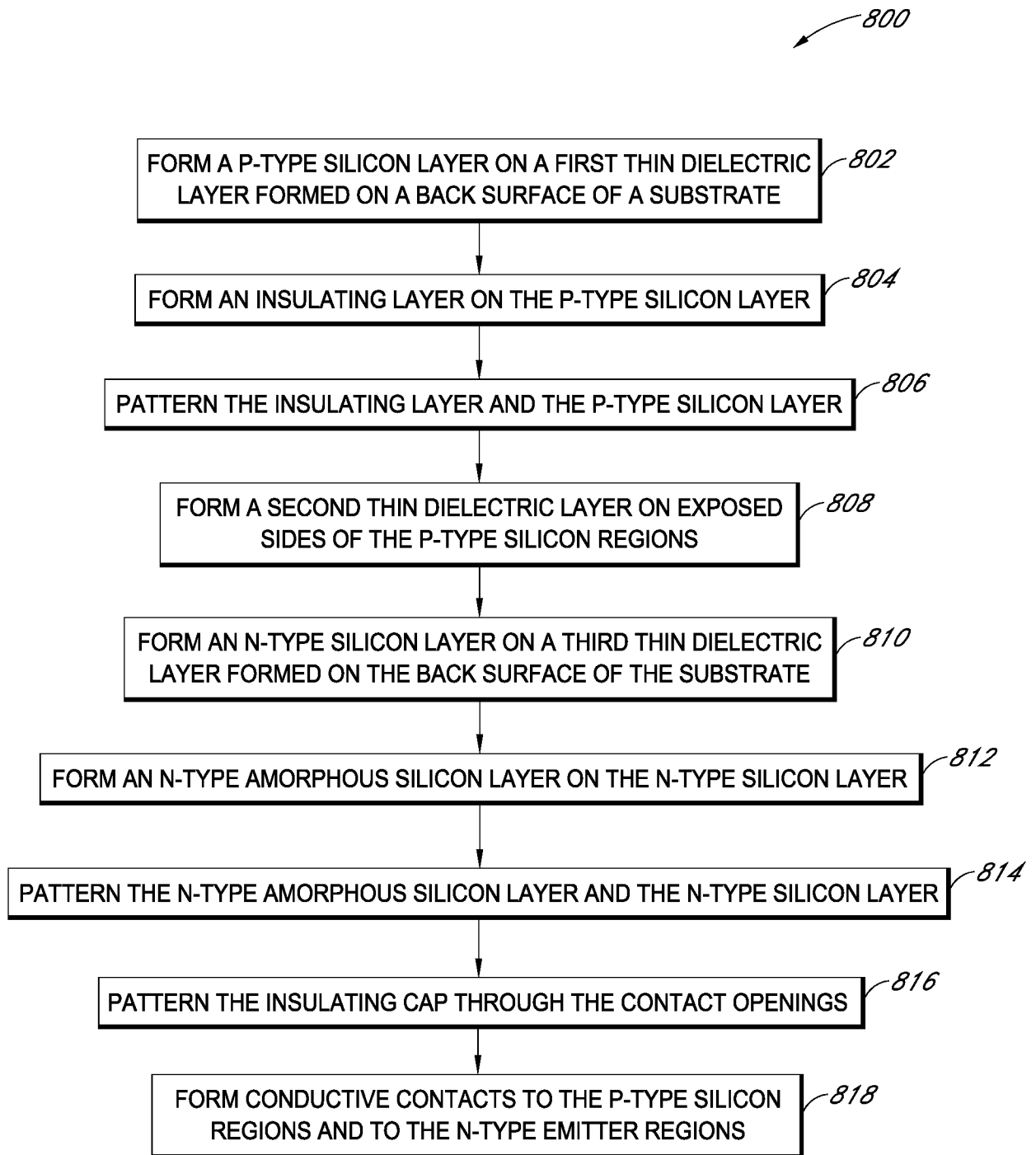
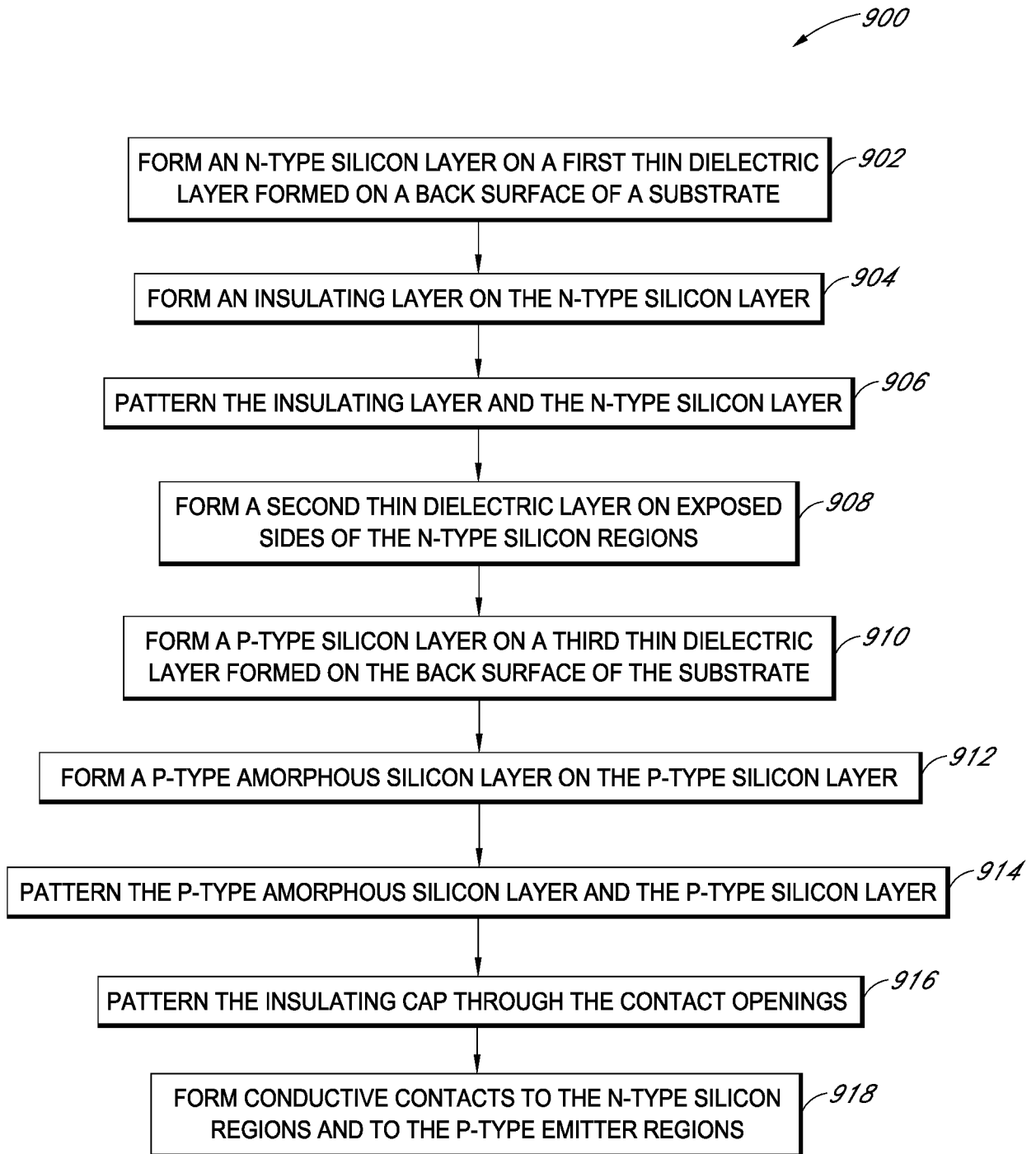


FIG. 7

*FIG. 8*

*FIG. 9*

A. CLASSIFICATION OF SUBJECT MATTER**H01L 31/072(2006.01)i, H01L 31/0376(2006.01)i, H01L 31/0392(2006.01)i, H01L 31/18(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 31/072; H01L 31/0216; H01L 31/06; H01L 31/0352; H01L 31/18; H01L 31/042; H01L 31/0376; H01L 31/0392

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: solar cell, p-type emitter region, n-type emitter region, n-type passivation layer, trench

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0186456 A1 (DAISUKE IDE et al.) 25 July 2013 See paragraphs [0035]-[0071]; claims 1, 10; and figures 3, 6.	1-5, 21-25
Y		6-20
Y	WO 2013-096500 A1 (SUNPOWER CORPORATION) 27 June 2013 See paragraphs [0016]-[0020]; and figures 5, 6, 9.	6-20
A	US 2013-0240029 A1 (DAVID D. SMITH) 19 September 2013 See paragraphs [0016]-[0038]; and figures 1-10.	1-25
A	US 2014-0027875 A1 (SANYO ELECTRIC CO., LTD.) 30 January 2014 See paragraphs [0021]-[0066]; and figures 2-7.	1-25
A	US 2012-0285518 A1 (JOEL P. DE SOUZA et al.) 15 November 2012 See paragraphs [0009]-[0021], [0036]-[0040]; and figures 2A-2L.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 June 2016 (23.06.2016)

Date of mailing of the international search report

23 June 2016 (23.06.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

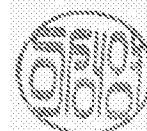
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

LEE, Seoung Young

Telephone No. +82-42-481-3535



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/023315

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013-0186456 A1	25/07/2013	CN 102725858 A	10/10/2012
		CN 102725858 B	09/12/2015
		EP 2530729 A1	05/12/2012
		EP 2530729 A4	29/10/2014
		JP 05845445 B2	20/01/2016
		WO 2011-093329 A1	04/08/2011
WO 2013-096500 A1	27/06/2013	AU 2012-358982 A1	03/07/2014
		AU 2012-358982 B2	07/05/2015
		AU 2015-210421 A1	03/09/2015
		CN 104011881 A	27/08/2014
		DE 112012005381 T5	04/09/2014
		JP 2015-505167 A	16/02/2015
		KR 10-2014-0106701 A	03/09/2014
		TW 201344931 A	01/11/2013
		US 2013-0164878 A1	27/06/2013
		US 2013-0164879 A1	27/06/2013
		US 8597970 B2	03/12/2013
		US 8679889 B2	25/03/2014
US 2013-0240029 A1	19/09/2013	AU 2009-257973 A1	17/12/2009
		AU 2009-257973 B2	02/04/2015
		AU 2009-257974 A1	17/12/2009
		AU 2009-257974 B2	22/01/2015
		CN 102057497 A	11/05/2011
		CN 102057497 B	12/06/2013
		CN 103325861 A	25/09/2013
		CN 202307920 U	04/07/2012
		CN 202930394 U	08/05/2013
		EP 2297788 A1	23/03/2011
		EP 2297788 A4	02/07/2014
		EP 2297789 A1	23/03/2011
		EP 2297789 A4	02/07/2014
		EP 2297789 B1	05/08/2015
		JP 05524194 B2	18/06/2014
		JP 05625167 B2	19/11/2014
		JP 05780565 B2	16/09/2015
		JP 05860101 B2	16/02/2016
		JP 2011-523230 A	04/08/2011
		JP 2011-523231 A	04/08/2011
		JP 2014-160843 A	04/09/2014
		JP 2014-212339 A	13/11/2014
		JP 2016-036056 A	17/03/2016
		KR 10-1466753 B1	01/12/2014
		KR 10-1492683 B1	12/02/2015
		KR 10-2011-0025826 A	11/03/2011
		KR 10-2011-0030561 A	23/03/2011
		US 2009-0308438 A1	17/12/2009
		US 2009-0308457 A1	17/12/2009

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/023315

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 2011-0003423 A1	06/01/2011
		US 2011-0059571 A1	10/03/2011
		US 2013-0237007 A1	12/09/2013
		US 2014-0224319 A1	14/08/2014
		US 2015-0155417 A1	04/06/2015
		US 2016-0071991 A1	10/03/2016
		US 7812250 B2	12/10/2010
		US 7851698 B2	14/12/2010
		US 8450134 B2	28/05/2013
		US 8460963 B2	11/06/2013
		US 8673673 B2	18/03/2014
		US 8772894 B2	08/07/2014
		US 8975717 B2	10/03/2015
		US 9231145 B2	05/01/2016
		WO 2009-151808 A1	17/12/2009
		WO 2009-151809 A1	17/12/2009
US 2014-0027875 A1	30/01/2014	JP 05842173 B2	13/01/2016
		US 9224905 B2	29/12/2015
		WO 2012-132836 A1	04/10/2012
US 2012-0285518 A1	15/11/2012	None	