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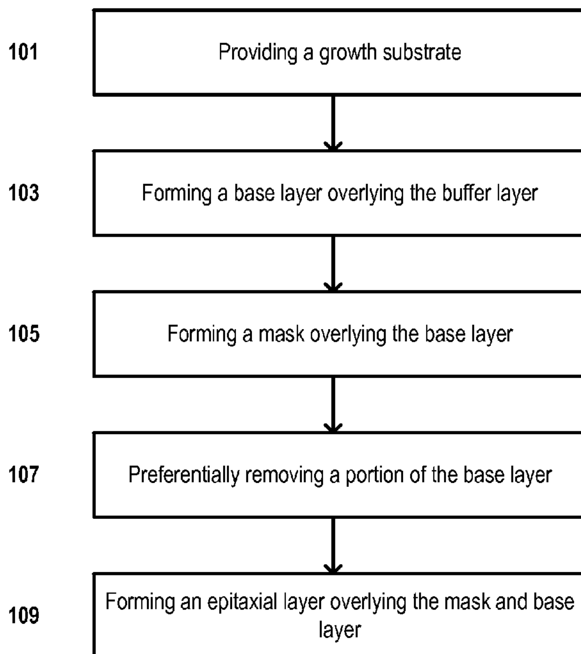

FIG. 1

(57) Abstract: A method of forming a semiconductor substrate including forming a base layer of a Group 13-15 material on a growth substrate during a growth process, forming a mask having mask regions and gap regions overlying the base layer during the growth process, and preferentially removing a portion of the base layer underlying the mask during the growth process.

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SEMICONDUCTOR SUBSTRATE AND METHOD OF FORMING

BACKGROUND

Field of the Disclosure

The following is directed to a method of forming a semiconductive substrate, and particularly, a method of forming a semiconductive substrate using a mask.

Description of the Related Art

Semiconductive-based compounds, including Group 13-15 materials, such as gallium nitride (GaN), ternary compounds, such as, indium gallium nitride (InGaN) and gallium aluminum nitride (GaAlN), and even the quaternary compounds (AlGaInN) are direct band gap semiconductors. Such materials have been recognized as having great potential for short wavelength emission, and thus suitable for use in the manufacturing of light emitting diodes (LEDs), laser diodes (LDs), UV detectors, and high-temperature electronics devices.

However, the development of such semiconductive materials has been hampered by difficulties surrounding the processing of such materials, particularly the formation of high-quality single crystalline forms of the material, which are required for manufacturing of short wavelength emission electronics. GaN is not found as a naturally occurring compound, and thus cannot be melted and pulled from a boule like silicon, gallium arsenide, or sapphire, because at usual pressures its theoretical melting temperature exceeds its dissociation temperature. As an alternative, the industry has turned to formation of bulk GaN crystals using epitaxial growth processes. However, problems still remain with the epitaxial approach, including the formation of suitable low defect density bulk GaN material.

The existence of extended defects (threading dislocations, stacking faults, and antiphase boundaries) leads to significantly deteriorated performances and results in a shortened operating lifetime of devices. More specifically, the dislocations behave as non-radiative centers, thus reducing the light-emitting efficiency of light-emitting diodes and laser diodes made from these materials. These dislocations also increase the dark current. Although threading dislocations have not prevented the

development of high-brightness light-emitting diodes, the dislocations cause excessive reverse-bias leakage currents in p-n junction devices such as high-electron-mobility transistors, field-effect transistors and other electronic devices. Further, the dislocations can act as strong scattering centers for carriers, thus reducing the mobility of electrons and holes, limiting the performance of many semiconductor devices.

SUMMARY

A method of forming a semiconductor substrate including forming a base layer of a Group 13-15 material on a growth substrate during a growth process, forming a mask comprising mask regions and gap regions overlying the base layer during the growth process, and preferentially removing a portion of the base layer underlying the mask during the growth process.

According to another aspect, a method of forming a semiconductor substrate includes a) forming a base layer of a Group 13-15 material on a growth substrate, b) forming a mask comprising a nitride material overlying the base layer, and c) etching and preferentially removing portions of the base layer and the mask after forming the mask. The steps a), b), and c) can be conducted in-situ during a single operation within a growth chamber.

In another aspect, a method of forming a semiconductor substrate can include forming a base layer comprising GaN on a growth substrate during a growth process, the growth substrate having a sapphire base substrate and a buffer layer overlying the growth substrate and disposed between the base substrate and the base layer. The method further includes forming a mask comprising mask regions and gap regions between the mask regions overlying the base layer, and preferentially removing a portion of the base layer underlying the mask.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure may be better understood, and its numerous features and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

FIG. 1 includes a flowchart providing a method of forming a semiconductive substrate material for an electronic device in accordance with embodiment.

FIGs. 2A-2D includes illustrations of a semiconductive substrate forming process in accordance embodiment.

5 The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION

The following is generally directed to substrate materials, and particular, substrates comprising semiconductive materials, and which can include a plurality of 10 semiconductive layers (i.e., semiconductive substrates) and methods of forming such articles. The semiconductive substrate may include Group 13-15 materials including for example gallium nitride (GaN). It will be appreciated that reference to Group 13-15 materials, include compounds including at least one element from Group 13 of the Periodic Table of Elements and at least one element from Group 15 of the Periodic 15 Table of Elements based on the IUPAC Periodic Table of Elements, version dated January 21, 2011.

FIG. 1 includes a flow chart illustrating a method of forming a semiconductive substrate in accordance with the embodiment. As illustrated, the process can be initiated at step 101 by providing a growth substrate. The growth substrate can be a 20 structure suitable for supporting a plurality of layers thereon. The growth substrate may further provide a structure and surface suitable for conducting heteroepitaxial growth of semiconductive layers thereon. In accordance with one embodiment, the growth substrate can be a composite article, including more than one structure or type of material. For example, the growth substrate can include a base substrate and a 25 buffer layer overlying the base substrate.

According to one embodiment, the base substrate can include an inorganic material. Some suitable inorganic materials can include oxides, carbides, nitrides, borides, oxycarbides, oxyborides, oxynitrides, and a combination thereof. In certain instances the base substrate can include alumina, and more particularly, may include

single crystal alumina (i.e., sapphire). One embodiment utilizes a substrate consisting essentially of sapphire.

The buffer layer of the growth substrate can overlie the base substrate. Turning briefly to FIG. 2A, a semiconductive substrate 200 is illustrated in accordance with embodiment. Notably, the semiconductive substrate 200 can include a growth substrate 201 including a base substrate 202 and a buffer layer 203 overlying the base substrate 202. In particular, the buffer layer 203 can overlie an upper major surface of the base substrate 202, and more particularly, the buffer layer 203 can be in direct contact with upper major surface of the base substrate 202.

According to one embodiment, the growth substrate 201 may be obtained from a manufacturer, or alternatively, may be formed prior to conducting other processes. For example, the buffer layer 203 can be formed on the upper surface of the base substrate 202 using a deposition process. For example, the buffer layer 203 can be deposited on an upper major surface of the base substrate 202 within a reaction chamber. According to one process, the base substrate 202 can be loaded into a reaction chamber, and after providing a suitable environment within the reaction chamber, a buffer layer 203 can be deposited on the base substrate 202. According to one embodiment, a suitable deposition technique can include chemical vapor deposition. In one particular instance, the deposition process can include metal-organic chemical vapor deposition (MOCVD).

In certain instances, the buffer layer 203 may be formed from a plurality of films. For example, as illustrated in FIG. 2A, the buffer layer 203 can include a film 204 and a film 206. In accordance with an embodiment, at least one of the films 204 or 206, can include a crystalline material. In more particular instances, the film 204, which can be in direct contact with the surface of the substrate 201, can include silicon, and may consist essentially of silicon. The film 204 may facilitate separation between the substrate 201 and semiconductive layers overlying the film 204 as described herein.

As illustrated in FIG. 2A, the film 206 can overlie the film 204, and more particularly, can be in direct contact with the film 204. The film 206 can have suitable crystallographic features for epitaxial formation of layers thereon. Notably,

in one embodiment the film 204 can include a semiconductive material. Suitable semiconductive material can include a Group 13-15 material. In one particular instance, the film 206 can include a nitride material. In another example, the film 206 can include gallium, aluminum, indium and a combination thereof. Still, in one
5 particular embodiment, the film 206 can comprise aluminum nitride, and more particularly, may consist essentially of aluminum nitride.

Accordingly, in an exemplary structure, the buffer layer 203 can be formed such that the film 204 includes silicon and is directly contacting a major surface of the substrate 201. Furthermore, the film 206 can directly contact a surface of the film 204
10 and include aluminum nitride.

After providing a substrate at step 101, the process can continue at step 103 by forming a base layer overlying the growth substrate. Referring briefly to FIG. 2A, the semiconductive substrate 200 can include a base layer 205 overlying the growth substrate 201 that includes the base substrate 202 and the buffer layer 203. In
15 particular, the base layer 205 can be formed such it is overlying a surface of the buffer layer 203, and more particularly, the base layer 205 can be in direct contact with the film 206 of the buffer layer 203.

According to an embodiment, upon suitably forming a buffer layer 203, the substrate 201 and buffer layer 203 may be placed within a reaction chamber to
20 conduct a continuous growth process. A continuous growth process can include a process that is carried out in a single chamber, without removing the work piece (e.g., semiconductive substrate) from the chamber. A continuous growth process can also include a growth process, such as an epitaxial growth process, wherein a series of semiconductive layers can be formed without significant cooling of the work piece
25 from the growth temperature, such that all layers can be formed with each other in-situ. A continuous growth process can further include a growth process wherein all semiconductive layers are formed using the same process (e.g., hydride vapor phase epitaxy), and within the same temperature, at substantially the same growth temperature.

30 In accordance with the embodiment, the continuous growth process can utilize an epitaxial growth process. More particularly, the continuous growth process can

include hydride vapor phase epitaxy (HVPE). Accordingly, the base layer 205 can be formed through an epitaxial growth process, such as hydride vapor phase epitaxy (HVPE). Such a process may be particularly useful for forming a low defect density and thick base layer 205, and particularly, a base layer 205 having an average
5 thickness greater than about 10-20 microns.

Alternatively, the base layer 205 can be formed using a deposition process, such as chemical vapor deposition. In one particular embodiment, the base layer 205 can be formed via metalorganic chemical vapor deposition (MOCVD). In particular instances, MOCVD may be used to form a particularly thin base layer 205, including
10 for example, a base layer having an average thickness less than about 10 microns, and more particularly less than about 3 microns.

In one particular instance, the base layer 205 can be made of a Group 13-15 material. Some suitable Group 13-15 materials can include nitride materials. Furthermore, the base layer 205 may include gallium. In particular instances, the base
15 layer 205 may include gallium nitride (GaN), and more particularly may consist essentially of gallium nitride.

Particular methods of forming the base layer 205 can be undertaken. For example, in utilizing a HVPE process, the formation of the base layer material can be conducted in various growth modes. For example, in one embodiment the base layer
20 is initially formed as an epitaxial layer grown in a 3-dimensional (3D) growth mode. A 3D growth mode can include the simultaneous growth of the base layer 205 material along multiple crystallographic directions. In such instances, formation of the base layer 205 in a 3D growth process can include spontaneous formation of island features on the buffer layer 203. The spontaneously formed island features can
25 be randomly positioned on the buffer layer 203, defining various mesas having multiple facets and valleys between the mesas.

Alternatively, or additionally, forming of the base layer 205 can include epitaxial growth in a 2-dimensional (2D) growth mode. A 2Dgrowth mode is characterized by preferential growth of the material in one crystallographic direction
30 and limited growth of the crystalline material along other crystallographic directions. For example, in one embodiment, formation of a base layer 205 comprising GaN in a

2D growth mode includes preferential growth of the GaN in the c-plane (0001), such that vertical growth of the base layer material is stabilized over lateral growth.

Still, forming of the base layer can incorporate a combination of 3D and 2D growth modes. For example, the base layer 205 may be initially formed in a 3D growth mode, wherein island features are spontaneously formed on the buffer layer 203 as a non-continuous layer of material. Following the 3D growth mode, growth parameters can be altered to change to a 2D growth mode, wherein vertical growth is accelerated over lateral growth. Upon switching from a 3D growth mode to a 2D growth mode, the spontaneously formed islands may coalesce into a continuous layer of uniform thickness. Combining 3D and 2D growth modes can facilitate formation of a base layer having desirable characteristics, such as a particular dislocation density.

Certain growth parameters include growth temperature, growth rate, pressure of vapor phase reactant and non-reactant materials, ratio of reactant and non-reactant materials in the reaction atmosphere, growth chamber pressure, and a combination thereof. Reference herein to a reactant material includes reactant materials such as nitrogen-containing materials, such as ammonia. Other reactant materials can include halide phase components, including for example, metal halide components such as gallium chloride. Non-reactant materials can include certain types of gases including for example noble gases, inert gases, and the like. In particular instances the non-reactant material can include gases such as nitrogen and or hydrogen.

During formation of the base layer 205, including production of the base layer 205 in a 3D growth mode, the growth temperature can be at least about 750°C. In other embodiments, the growth temperature can be greater, such as at least about 800°C, at least about 850°C, at least about 875°C, at least about 900°C, or even at least about 925°C. According to one method of forming, the growth temperature during formation of the base layer 205 can be not greater than about 1200°C, such as not greater than about 1150°C, not greater than about 1125°C, not greater than about 1050°C, or even not greater than about 1000°C. It will be appreciated that the growth temperature can be within a range between any of the minimum and maximum values noted above.

For certain processes, the growth temperature may be changed to facilitate a change between 3D and 2D growth modes. For example, in changing from 3D to 2D growth modes, the temperature may be changed by at least about 5°C, such as at least about 10°C, at least about 15°C, at least about 20°C, at least about 30°C, at least about 35°C, or even at least about 40°C. In still other embodiments, in changing from a 3D to 2D growth mode, the growth temperature can be changed by not greater than about 100°C, such as not greater than about 90°C, not greater than about 80°C, not greater than about 70°C, or even not greater than about 60°C. Change of the growth temperature can include an increase in the growth temperature in changing from 3D to 2D growth modes. It will be appreciated that the change in growth temperature can be within a range between any of the minimum and maximum values noted above.

In accordance with embodiment, the process of forming the base layer 205 can be conducted at a growth rate of at least 50 microns per hour. In other embodiments, the rate of forming the base layer 205 can be greater, such as at least about 75 micron per hours, at least about 100 microns per hour, at least about 150 microns per hour, at least about 200 microns per hour, or even at least about 250 microns per hour. Another embodiment, the process of forming the base layer 205 can be conducted at a rate of not greater than about 1 mm per hour, such as not greater than 750 microns per hour not great 500 microns per hour, or even not greater than about 300 microns per hour. It will be appreciated the process of forming the base layer can be constructed at a rate within a range within any of the minimum maximum values noted above.

For certain processes, the growth rate may be changed to facilitate a change between 3D and 2D growth modes. For example, in changing from 3D to 2D growth, the growth rate may be changed by at least about 5 microns per hour, such as at least about 10 microns per hour, at least about 15 microns per hour, at least about 20 microns per hour, at least about 40 microns per hour, at least about 50 microns per hour, or even at least about 75 microns per hour. In still other embodiments, in changing from a 3D to 2D growth mode, the growth rate can be changed by not greater than about 200 microns per hour, such as not greater than about 175 microns per hour, not greater than about 150 microns per hour, not greater than about 125 microns per hour, or even not greater than about 100 microns per hour. It will be appreciated that the change in growth rate can be a decrease in the growth rate when

changing from a 3D to a 2D growth mode. It will be appreciated that the change in growth rate can be within a range between any of the minimum and maximum values noted above.

According to other embodiments, the process of changing from 3D to 2D growth modes may be induced by a change in growth rate by at least a factor of 2. For example, the growth rate can be decreased by a factor of at least 2 in changing from a 3D growth mode to a 2D growth mode. In other embodiments, the growth rate can be decreased by a factor of at least about 3, at least about 4, or even at least about 5. In particular instances, the decrease in the growth rate is not greater than about a factor of 8, not greater than a factor of about 7, or not greater than a factor of about 6.

It will be appreciated that in changing the growth mode, one or more of the above-identified factors can be changed. For example, the growth temperature can be changed, while the growth rate is held steady. Alternatively, the growth rate can be changed while the growth temperature is maintained. And still, in another embodiment, both the growth rate and growth temperature may be changed to effectuate the change in growth modes.

The base layer 205 can be formed to have a particular thickness to facilitate further processes and the formation of a high quality material according to embodiments herein. For example, the base layer 205 may have an average thickness of not greater than about 5 mm. In other embodiments, the base layer 205 may have an average thickness of not greater than about 3 mm, such as not greater than about 2 mm, not greater than about 1 mm, not greater than about 0.5 mm, not greater than about 0.2 mm, not greater than about 100 microns, not greater than about 50 microns, not greater than about 1 micron, or even not greater than about 0.1 microns. Still, in other embodiments, the base layer 205 can be formed to have an average thickness of at least about 1 nm, such as at least about 10 nm, at least about 20 nm, at least about 50 nm, or even at least about 70 nm. It will be appreciated that the base layer 205 can be formed to have an average thickness within a range between any of the minimum and maximum values noted above.

The base layer 205 can be formed to have a particular dislocation density. The dislocation density of the base 205 can be measured at the upper surface of the base

layer upon forming. A suitable method of measuring the dislocation density includes use of cathode luminescence microscopy operated at room temperature and polychromatic light detection without monochromator under 10 keVe-beam, spot size 70, wherein the machine is an SEM JSM-5510, commercially available from JEOL
5 Corporation. For a dislocation density measurement of approximately 10^8 cm^{-2}, the magnification is 4000X and the area is typically 700 μm^2. For a dislocation density measurement of approximately 10^6 cm^{-2}, the magnification is typically 500-1000X and the area is typically 0.1 mm^2.

For example, the base layer 205 can have a dislocation of density not greater
10 than about $1x10^8$ dislocation/cm^2, as measured at an upper surface of the base layer 205. In other embodiments, the dislocation density of the base layer 205 can be less, such that it is not greater than about 1x 10^7dislocation/cm^2, not greater than about $6x10^6$dislocation/cm^2, or even not greater than about $1x10^6$dislocation/cm^2. Still, the base layer 205 may have a dislocation density that is at least about
15 $1x10^5$dislocation/cm^2, such as at least $2x10^5$dislocation/cm^2, at least $3x10^5$dislocation/cm^2,or even at least $5x10^5$dislocation/cm^2. It will be appreciated that the base layer can have a dislocation density within a range within any of the minimum and maximum values noted above.

Referring again to FIG. 1, after forming a base layer overlying the buffer layer
20 at step 103, the process can continue at step 105 by forming a mask overlying the base layer. The process of forming the mask can include the introduction of one or more particular chemical species within the growth chamber. According to a particular embodiment, the process of forming the mask can include providing a silicon-containing material within the growth chamber. In particular instances, the silicon-
25 containing material can be provided in-situ within the growth chamber used during the growth process. More particularly, the silicon-containing material can be introduced during a growth process, wherein the growth of the base layer 205 can be interrupted to introduce the silicon-containing material.

In one embodiment, the silicon-containing material can include hydrogen. In
30 certain processes, the silicon containing material can include a combination of silicon and hydrogen, including for example silane (SiH_4). More particularly, in one non-limiting embodiment, the silicon-containing material can consist essentially of silane.

In addition to the introduction of a silicon-containing material, other materials can be introduced to the growth chamber to facilitate forming a mask. For example, the growth chamber may include a nitrogen-containing material, and more specifically, a nitrogen-containing material including hydrogen. For example, the nitrogen-containing material can include ammonia (NH_3). In one particular embodiment, the nitrogen-containing material can consist essentially of ammonia. It will be appreciated that formation of the mask can be a result of a chemical reaction between the nitrogen-containing material and silicon-containing material. For example, in one particular instance, the silicon-containing material can react with the nitrogen-containing material to form a silicon nitride (SiN_x) material, and wherein the mask can comprise silicon nitride.

Referring briefly to FIG. 2B, a cross–sectional illustration of a portion of a semiconducting substrate during processing according to an embodiment is provided. As illustrated, the semiconducting substrate 220 can include a growth substrate 201, a base layer 205 overlying the growth substrate 201, and a mask 221 having mask regions 222 and gap regions 223 overlying an upper surface 224 of the base layer 205. In accordance with an embodiment, the mask 221 can be formed at a temperature substantially close to the growth temperature utilized in formation of the base layer 205. For example, the process of forming the mask can be conducted at a temperature with 800°C of the growth temperature utilized in forming of the base layer 205. In other embodiments, the process of forming the mask can be conducted at a temperature that is within 600°C of the growth temperature, such as within at least 500°C of the growth temperature, within at least about 400°C of the grown temperature, within at least 300°C of the growth temperature, or even within at least about 200°C of the growth temperature.

In accordance with an embodiment, the mask regions 222 can be include silicon and nitrogen. In one instance, the mask regions 222 can be formed of silicon nitride (SiN_x), and in particular, the mask regions 222 may consist essentially of silicon nitride.

As further illustrated, the mask regions 222 can be formed in a manner such that they have a random orientation relative to each other. For example, the mask regions 222 can be essentially free of short range order or long range ordering. More

particularly, the mask regions 222 can be arranged relative to each other such that there is no discernable pattern or repeating arrangement. Moreover, the mask regions 222 can have a random spacing between each other, as defined by the size of the gap regions 223.

5 The mask regions 222 can have various sizes relative to each other and relative to any crystallographic directions of the base layer 205. For example, each mask region may have a width (W) of at least about 0.5 nm or at least about 1 nm. Each mask region may have a width (W) of submicron size, for example, not greater than about 0.8 microns, not greater than about 0.5 microns, or even not greater than 10 about 0.1 microns. It will be appreciated that the majority of mask regions 222 can have a size within a range between any of the minimum and maximum values noted above

Furthermore, the mask regions 222 can be defined by gap regions 223 extending between the mask regions 222 and defining openings wherein the upper 15 surface 224 of the base layer 225 may be exposed, and not covered by mask regions 222. The gap regions 223 can be arranged randomly relative to each other on the surface 224 of the base layer 205. That is, in particular instances, the gap regions 223 can have various widths and orientations relative to each other. The gap regions 223 can also have random orientations relative to one or more crystallographic directions 20 of the base layer 205, such that the gap regions do not necessarily align with any crystallographic directions or planes of the base layer.

In accordance with an embodiment, each of the gap regions 223 can have a width (W_g) of at least about 0.5 nm or at least about 1 nm. Each gap region may have a width (W_g) of submicron size, for example, not greater than about 0.8 microns, not 25 greater than about 0.5 microns, or even not greater than about 0.1 microns. It will be appreciated that the majority of gap regions 223 can have a size within a range between any of the minimum and maximum values noted above

In another embodiment, the mask 221 can be formed such that mask regions 222 have a particular average thickness (t_m). In accordance with an embodiment, the 30 mask regions 222 can be formed to have an average thickness that is less than the average thickness of the base layer (t_b). In other instances, the mask regions 222 can

be formed to have an average thickness that is less than about 0.5 microns, such as less than about 0.3 microns, less than about 0.1 microns, or even less than about 0.08 microns. The mask regions 222 can have an average thickness of at least about 0.001 microns. In accordance with an embodiment, the mask regions 222 can have an average thickness within a range between any of the minimum and maximum values noted above.

In accordance with an embodiment, the process of forming the mask 221 can be conducted for a particular duration. For example, the duration can include a time suitable for the introduction of materials used to form the mask 221. As such, in at least one embodiment, the process of forming the mask 221 can last for a duration of not greater than about 60 min, such as not greater than about 20 min, not greater than about 10 min, or even not greater than about 5 min.

Furthermore, other processing conditions within the growth chamber may be controlled to facilitate proper formation of the mask 221. For example, the pressure within the growth atmosphere during formation of the mask can be within a range between about 50 and about 800 Torr.

After forming a mask at step 105, the process can continue at step 107 by preferentially removing a portion of the base layer. In accordance with an embodiment, the process of preferentially removing a portion of the base layer can include an etching process. In accordance with one embodiment, the etching process can include the incorporation of an etchant material within the growth chamber. Some suitable etchant materials can include compositions including a halogen element, and more particularly chlorine. In other embodiments, the etchant material may include hydrogen. In an exemplary embodiment, the etchant material can include hydrogen chloride (HCl), and more particularly, may consist essentially of hydrogen chloride.

In some instances, the etchant material may include a combination of materials. For example, the etchant material can include a combination of hydrogen chloride and a nitrogen-containing material. One suitable nitrogen-containing material can include ammonia (NH_3). It will be appreciated that in particular instances the etchant material may be introduced in the growth chamber as a gas-

phase species. Still, in other embodiment, the etchant material may be a liquid-phase species, depending upon the processing conditions.

According to one embodiment, the process of preferentially removing a portion of the base layer can be conducted at a temperature that is substantially the same as the growth temperature. In other embodiments, the process of preferentially removing a portion of the base layer can be conducted at elevated temperatures, and more notably, temperatures close to the growth temperature utilized in forming the base layer 205. For example, the process of preferentially removing can be conducted at a temperature within 800°C of the growth temperature, such as within 600°C of the growth temperature, within 500°C of the growth temperature, within 400°C of the growth temperature, within 300°C of the growth temperature, within 200°C of the growth temperature, within 100°C of the growth temperature, or even within 50°C of the growth temperature. In one non-limiting embodiment, the process of preferentially removing a portion of the base layer can be conducted at a temperature between 600°C and 1100°C.

As noted herein, the process of preferentially removing a portion of the base layer can include an etching operation. Notably, the etching process may selectively remove portions of the base layer 205. In accordance with an embodiment, the process of etching can last for a duration not greater than about 2 hours, such as not greater than about 100 min., not greater than about 90 min., not greater than about 70 min., not greater than about 60 min., not even not greater than 30 min, not even not greater than 10 min, or not even not greater than 1min. Notably, the duration of etching may depend upon certain other factors, including, for example the concentration of etchant material within the growth chamber.

FIG. 2C includes a cross-sectional view of a semiconductor substrate after conducting a process of preferentially removing a portion of the base layer in accordance with an embodiment. As illustrated, the semiconductor substrate 250 can include a growth substrate 201, a base layer 205 overlying the growth substrate 201 and a mask 221 overlying the base layer 205. As illustrated, the process of preferentially removing a portion of the base layer 205 can include the formation of pits 253 in an upper surface 224 of the base layer 205. In accordance with an embodiment, the pits 253 can be formed to have a certain depth depending upon the

processing conditions. In particular instances, the pits 253 can have various depths compared to each other, depending upon the processing conditions.

According to one non-limiting embodiment, the pits 253 can have an average depth (d) less than an average thickness (t_b) of the base layer 205. In particular
5 instances, the pits 253 can be formed to have an average depth less than about 10 microns, such as less than about 8 microns, less than about 5 microns, less than about 2 microns, less than about 1 micron, less than about 0.8 microns, less than about 0.5 microns, or even less than about 0.5 microns or even less than about 0.2 microns. Still, the average depth of the pits 253 can be at least about 1 nm. It will be
10 appreciated that the depth of the pits 253 can be within a range between any of the minimum or maximum values above.

In certain other instances, while not illustrated in FIG. 2C, at least a portion of the pits 253 may extend for an entire thickness of the base layer 205. That is, for example, during the process of preferentially removing a portion of the base layer
15 205, in some areas, substantially all of the base layer can be removed until a portion of the underlying buffer layer 203 is exposed. In more particular instances, the buffer layer 203 can function as an etch-stop layer, limiting the depth of the pits 253 when the etchant material reaches the buffer layer 203. Such embodiments may be particularly suited to a base layer 205 having a particular thickness, for example, a
20 base layer 205 having an average thickness of less than about 10 microns, such as less than about 5 microns, less than about 1 micron, or even less than about 0.1 microns. Notably, in particular instances, the etching process can be conducted such that the pits 253 can have a depth (d) that is substantially equivalent to (within 10% of a measurement or even within 5% of a measurement) of the average width of the mask
25 regions 222 and the gap regions 223.

The process of preferentially removing a portion of the base layer 205 can include preferential removal of portions of the upper surface 224 of the base layer 205. More particularly, the process of preferentially removing can include the preferential removal of high dislocation density regions 254 at the upper surface 224
30 of the base layer 205. For example, the etchant material can preferentially remove regions at the upper surface 224 of the base layer 205 having a higher dislocation density (i.e., a higher concentration of defects) as compared to regions 225 of the

upper surface 224 of the base layer 205 having a lower concentration of defects (i.e., low dislocation density regions). As such, the process of preferentially removing can remove highly defected regions in the upper surface 224, facilitating the formation of a new (e.g., etched) upper surface of the base layer 205 having a significantly lower concentration of defects in totality as compared to the upper surface 224 prior to the process of selectively removing.

In accordance with an embodiment, the process of preferentially removing a portion of the base layer 205 can also include preferentially removing portions of the mask 221, and more notably, portions of the mask regions 222. For example, as illustrated in FIG. 2C, within regions 254 having high dislocation densities, portions of the mask regions (previously illustrated as mask regions 222) within the region 254 can be removed, such that mask portions 252 remain after processing. As illustrated in FIG. 2C, mask portions 252 represent mask regions 222 that have been at least partially removed and reduced in size due to the process of selectively removing a portion of the base layer 205.

The process of preferentially removing a portion of the base layer can include anisotropic etching of the upper surface 224 such that regions having high dislocation density are preferentially removed before regions having lower dislocation densities. As further illustrated in FIG. 2c the process of preferentially removing a portion of the base layer can include an isotropic etching process wherein portions of the base layer 205 underlying mask regions 222 can be removed. For example, the etchant material may preferentially remove portions of the base layer 205 before removing mask portions 252 such that the mask portions 252 may extend over and cover regions in the base layer 205 where the material has been completely removed.

Referring again to FIG. 1, after preferentially removing a portion of the base layer at step 107, the process can continue at step 109 by forming an epitaxial layer. The epitaxial layer can be formed such that it is overlying the mask portions 252 and the base layer 205. More particularly, the epitaxial layer can be formed such that it is epitaxially grown from the modified (e.g., etched) upper surface of the base layer 205 after processing. In particular, the epitaxial layer can be formed from regions of the base layer 205 having significantly low dislocation densities because the process of

preferentially removing eliminated a substantial portion of high dislocation density regions of the base layer 205.

Referring to FIG. 2D, an epitaxial layer 271 is illustrated as being formed over the release base layer 205 and mask portions 252. In particular instances, the epitaxial layer 271 can be formed such as it is directly contacting the upper surface of the base layer 205 between the mask portions 252. The epitaxial layer 271 can be initially grown from the pits 253 formed in the surface of the base layer 205. As further illustrated, during initial stages of growth of the epitaxial layer 217, voids 261 can be formed between the mask portions 252. The voids may be, but not necessarily, present in the final article.

The process of forming the epitaxial layer 271 can include an epitaxial growth process utilizing one or more growth modes as noted herein. For example, formation of the epitaxial layer 271 can include formation through a 3D growth mode, a 2D growth mode, or a combination of 3D and 2D growth modes. In one embodiment, the formation of the epitaxial layer 271 is completed entirely in a 2D growth mode.

Forming of the epitaxial layer 271 can be conducted via a continuous growth process, such that the epitaxial layer 271 is formed in-situ with the other semiconductive layers (e.g., the base layer 205). Notably, the process can be continuous and conducted within the same growth chamber during formation of the base layer 205, to formation of the mask 221, and further to formation of the epitaxial layer 271.

In accordance with embodiment, the epitaxial layer 271 can include a Group 13-15 material. In particular instances, the epitaxial layer can include a nitride material. In still another embodiment, the epitaxial layer can include gallium, and more particularly, may include gallium nitride. Certain epitaxial layers may consist essentially of gallium nitride.

In one embodiment, the epitaxial layer 271 can be grown at substantially the same rate as the base layer 205. The epitaxial layer 271 may be formed such it has an average thickness (t_e) that is at least the same as the base layer 205, and may have an average thickness that is significantly greater than the average thickness than the base

layer 205. For example, the epitaxial layer 271 can be formed such as it has an average thickness of at least about 5 microns. In other embodiments, the average thickness may be greater, such as at least about 10 microns, at least about 50microns, at least about 100 microns, at least about 200 microns, at least about 400 microns, at
5 least about 500 microns, or even at least about 800 microns. Still, the epitaxial layer 271 may be formed such that it has an average thickness that is not greater than about 10 mm, such as it is not greater about 5 mm, not greater than about 3 mm, or even not greater than about 2 mm. It will be appreciated that the epitaxial layer 271 can have an average thickness within a range between any of the minimum and maximum
10 values noted above.

The epitaxial layer 271 may be formed to have a particular dislocation density as measured in upper surface. For example, the epitaxial layer 271 can have a dislocation density that is not greater than about $1x10^8$dislocations/cm^2, such as not greater than about $1x10^7$dislocations/cm^2, or even not greater than about
15 $1x10^6$dislocations/cm^2. In other embodiments, the epitaxial layer 271 can have a dislocation density that is at least about $1x10^5$dislocations/cm^2, such as at least $2x10^5$dislocations/cm^2, or even at least $5x10^5$ dislocations/cm^2. It will be appreciated that the epitaxial layer 271 can have a dislocation density within a range between any of the minimum and maximum values noted above.

20 During the process of forming, including for example, the base layer 205, mask 221, and epitaxial layer 271, the growth substrate 201 may be separated from the base layer 205. The separation can be facilitated by the dissociation of a portion of the buffer layer 203, and particularly, a film within the buffer layer 203. In accordance with an embodiment, the buffer layer 203 can include a film, such as
25 silicon, wherein at elevated temperatures utilized during the continuous growth process, the film is thermally dissociated. Thermal dissociation facilitates separation between the substrate 201 and the plurality of semiconductive layers. Accordingly, upon completion of the continuous growth process, the base layer 205, mask 221, and epitaxial layer 271 can be completely removed from the substrate 201.

30 EXAMPLE

A sample is formed according to an embodiment by first growth of a two part buffer layer via MOVPE on a sapphire substrate. The buffer layer includes a first layer of silicon directly on the sapphire substrate, followed by epitaxial growth of AlN. After loading the sapphire substrate in the MOVPE reactor, the sapphire substrate has to be annealed under N_2 before growth of the silicon film. Preferably the temperature 870°C. Silicon growth is formed from pyrolysis of silane in the N_2 atmosphere at 100 Torr to a thickness of about 0.4 microns.

The temperature is raised to about 1140°C, the growth vapor still being pure N_2 at 70 torrs. NH_3 is first introduced into the reaction chamber, and thereafter, a TMAl organometallic material is introduced to begin forming the AlN layer on the silicon. After approximately 20 minutes of growth, a 0.2 μm thick AlN layer is deposited on top of the Si layer, forming the buffer layer.

A base layer of about 3-10 microns thick is formed using MOCVD on the buffer layer. After forming the base layer, a SiNx mask is formed by simultaneously introducing silane (SiH_4) and NH_3 at approximately 1000°C into the growth chamber for approximately 30 minutes. The growth chamber is first purged of gaseous components used to grow the GaN base layer. The mask is in the form of a SiNx nanonet characterized by mask regions of various sizes, shapes, and orientations relative to each other. The gap regions in the mask are approximately 1 nanometer to 100 nanometers in size. The mask regions have a thickness between approximately 1 and 50 nanometers.

After forming the mask, the wafer is brought in the HVPE growth chamber and an etching process is conducted using HCl. Some NH_3 may be present in the growth chamber. The etching process preferentially removes regions of the upper surface of the base layer having a greater concentration of dislocations as compared to regions of the upper surface of the base layer having a lower concentration of dislocations. Etching is conducted at approximately 400 to 1000 °C, for a duration of about 1 to 10min, removing less than about 1 micron in depth of GaN from the surface of the base layer. The buffer layer acted like an etch stop layer for certain pits formed in the base layer beneath the mask of significant depth.

After etching process, a porous GaN upper surface of the base layer is created with a skeleton of high quality GaN with low dislocation densities. An epitaxial layer is formed via HVPE in the gap regions of the mask (i.e., the openings) from the low dislocation density regions. The epitaxial layer is formed using the same parameters used to growth the GaN base layer, including at least one alternation between 3D and 2D growth modes, including for example, using at least in part, the following sequence: 350μm 3D + 50 μm 2D + 350 μm 3D + 50 μm 2D + 200 μm 3D.The epitaxial layer is formed to have a thickness of at least1 mm.

The embodiments herein represent a departure from the state-of-the-art. While certain ELO growth processes have utilized masks in the past, such masks have a been formed through particular techniques, including photolithography, to facilitate the formation of masks having precisely formed openings with controlled pitch parameters and alignment with crystallographic directions of the underlying material (e.g., sapphire or GaN). The present application discloses a process for forming a compound semiconductive substrate including a plurality of layers, and an intervening mask, formed in the middle of the growth process, which is used to improve the quality of the final epitaxial layer. Notably, the method of forming the mask and the process of preferentially removing portions of the underlying layer after forming the mask can be conducted in a manner to streamline processing and further improve the quality of the finally-formed epitaxial layer. The processes of the embodiments herein utilize a particular combination of growth parameters, including growth rate, ratio of reactant materials, ratio of non-reactant materials, growth modes, growth temperatures, growth pressure, material components, mask-forming conditions, and etching conditions.

In the foregoing, reference to specific embodiments and the connections of certain components is illustrative. It will be appreciated that reference to components as being coupled or connected is intended to disclose either direct connection between said components or indirect connection through one or more intervening components as will be appreciated to carry out the methods as discussed herein. As such, the above-disclosed subject matter is to be considered illustrative, and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments, which fall within the true scope of the present invention. Thus, to

the maximum extent allowed by law, the scope of the present invention is to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

5 The Abstract of the Disclosure is provided to comply with Patent Law and is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, various features may be grouped together or described in a single embodiment for the purpose of streamlining the disclosure. This disclosure is not to be interpreted as reflecting an 10 intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter may be directed to less than all features of any of the disclosed embodiments. Thus, the following claims are incorporated into the Detailed Description, with each claim standing on its own as defining separately claimed subject matter.

WHAT IS CLAIMED IS:

1. A method of forming a semiconductor substrate comprising:

forming a base layer of a Group 13-15 material on a growth substrate during a growth process;

forming a mask comprising mask regions and gap regions overlying the base layer during the growth process; and

preferentially removing a portion of the base layer underlying the mask during the growth process.

2. The method of claim 1, wherein the growth substrate comprises a base substrate including an inorganic material, wherein the base substrate comprises a material selected from the group consisting of oxides, carbides, nitrides, borides, oxycarbides, oxyborides, oxynitrides, and a combination thereof, wherein the base substrate comprises alumina, wherein the base substrate comprises sapphire, wherein the base substrate consists essentially of sapphire.

3. The method of claim 1, wherein the growth substrate comprises a buffer layer underlying the base layer and overlying a base substrate, wherein the buffer layer is in direct contact with a surface of the base substrate, wherein forming the buffer layer comprises depositing material overlying a major surface of the base substrate, wherein depositing comprises metal-organic chemical vapor deposition (MOCVD).

4. The method of claim 3, wherein the buffer layer comprises a plurality of films, wherein at least one film of the plurality of films comprises a Group 13-15 material, wherein the at least one film of the plurality of films comprises a nitride material, wherein the at least one film comprises an element selected from the group consisting of Ga, Al, In, and a combination thereof, wherein at least one film of the plurality of films comprises a crystalline material, wherein at least one film of the plurality of films comprises silicon.

5. The method of claim 3, wherein the buffer layer comprises:
a first film comprising silicon directly contacting a surface of the base substrate; and
a second film comprising a Group 13-15 material directly contacting a surface of the first film.

6. The method of claim 1, wherein forming the base layer comprises hydride vapor phase epitaxy (HVPE).

7. The method of claim 1, wherein the base layer comprises a Group 13-15 material, wherein the base layer comprises a nitride material, wherein the base layer comprises gallium, wherein the base layer comprises gallium nitride, wherein the base layer consists essentially of gallium nitride.

8. The method of claim 1, wherein the base layer comprises an average thickness of not greater than about 5 mm, wherein the base layer comprises an average thickness of not greater than about 3 mm, not greater than about 2 mm, not greater than about 1 mm, not greater than about 0.5 mm, and wherein the base layer has an average thickness of at least about 1 nm, at least about 10 nm, at least about 50 nm, at least about 70nm.

9. The method of claim 1, wherein the base layer comprises a dislocation density of not greater than about $1x10^8$ dislocations/cm^2 as measured at an upper surface, not greater than about $1x10^7$ dislocations/cm^2, and at least about $1x10^5$ dislocations/cm^2, at least about $2x10^5$dislocations/cm^2.

10. The method of claim 1, wherein forming the base layer is conducted at a rate of at least about 50 microns/hr.

11. The method of claim 1, wherein forming the base layer comprises forming in a three-dimensional growth mode, wherein forming the base layer comprises a spontaneous formation process comprising the formation of island features including semiconductive material, wherein forming further comprises coalescence of the island features into a continuous layer of semiconductive material.

12. The method of claim 1, wherein forming a mask comprises providing a silicon-containing material in a growth chamber during the growth process, wherein the silicon-containing material comprises hydrogen, wherein the silicon containing material comprises silane (SiH_4), wherein the silicon-containing material consists essentially of silane, further comprising providing a silicon-containing material in a growth chamber comprising a nitrogen-containing material, wherein the nitrogen-containing material comprises hydrogen, wherein the nitrogen-containing material comprises NH_3, wherein the nitrogen-containing material consists essentially of NH3, wherein the NH_3 reacts with silane to form silicon nitride (SiNx).

13. The method of claim 1, wherein the mask regions comprise silicon nitride (SiNx), wherein the mask regions consists essentially of silicon nitride, wherein the method includes first forming the mask and subsequently removing a portion of the base layer, wherein the mask regions comprise a random orientation relative to each other, wherein the mask regions comprise random sizes relative to each other, wherein the gap regions have random sizes relative to each other.

14. The method of claim 1, wherein preferentially removing a portion of the base layer comprises etching, wherein etching comprises an etchant material including a halogen element, wherein the halogen element comprises chlorine (Cl), wherein the etchant material comprises hydrogen, wherein the etchant material comprises hydrogen chloride (HCl), wherein the etchant material consists essentially of hydrogen chloride, wherein the etchant material comprises a gas phase species, wherein etching is conducted in an atmosphere comprising ammonia (NH_3).

15. The method of claim 1, wherein preferentially removing a portion of the base layer is conducted at a growth temperature, wherein etching is conducted at a temperature within 800°C of a growth temperature, within 600°C of the growth temperature, within 500°Cof the growth temperature, within 400°Cof the growth temperature, within 300°Cof the growth temperature, within 200°C of the growth temperature, within 100°C of the growth temperature, within 50°C of the growth temperature.

16. The method of claim 1, wherein preferentially removing a portion of the base layer comprises forming pits in an upper surface of the base layer, wherein at least a portion of the pits extend for an entire thickness of the base layer, wherein removing a portion of the base layer is conducted until a portion of the buffer layer is exposed, wherein the buffer layer is an etch-stop layer, wherein the pits have an average depth of less than an average thickness of the base layer, wherein the pits have an average depth of less than about 10 microns, less than about 8 microns, less than about 5 microns, less than about 2 microns, less than about 1 micron, less than about 0.8 microns, less than about 0.5 microns, less than about 0.2 microns.

17. The method of claim 1, wherein preferentially removing a portion of the base layer comprises etching an upper surface of a base layer for a duration of not greater than about 2 hours, not greater than about 100 minutes, not greater than about 30 minutes.

18. The method of claim 1, wherein preferentially removing a portion of the base layer comprises preferentially removing a high dislocation density region at an upper surface of the base layer, wherein preferentially removing comprises anisotropic etching of a portion of an upper surface of the base layer having a higher concentration of defects as compared to a region of the upper surface having a lower concentration of defects.

19. The method of claim 1, wherein preferentially removing a portion of the base layer further comprises removing a portion of the mask, removing a portion of the mask region, wherein preferentially removing a portion of the base layer further comprises removing a portion of an upper surface underlying a mask region.

20. The method of claim 1, wherein the mask regions have an average thickness less than an average thickness of the base layer, wherein the mask regions have an average thickness of less than about 0.5 microns, such as less than about 0.3 microns, less than about 0.1 microns, less than about 0.08 microns and an average thickness of at least about 0.001 microns.

21. The method of claim 1, further comprising forming an epitaxial layer overlying the mask and base layer, wherein the epitaxial layer comprises a nitride material, wherein the epitaxial layer comprises gallium, wherein the epitaxial layer comprises gallium nitride, wherein the epitaxial layer consists essentially of gallium nitride.

22. The method of claim 21, wherein the epitaxial layer comprises an average thickness of at least greater than 5 microns, at least about 10 microns, at least about 100 microns, at least about 200 microns, at least about 400 microns, at least about 500 microns, or even at least about 800 microns, and an average thickness that is not greater than about 10 mm, such as not greater about 5 mm, not greater than about 3 mm.

23. The method of claim 21, wherein the epitaxial layer comprises a dislocation density at an upper surface less than a dislocation density of an upper surface of the base layer, wherein the epitaxial layer comprises a dislocation density of not greater than about $1x10^8$ dislocations/cm^2 as measured at an upper surface, wherein the epitaxial layer comprises a dislocation density of not greater than about $1x10^7$ dislocations/cm^2, wherein the epitaxial layer comprises a dislocation density of not greater about $8x10^6$ dislocations/cm^2, wherein the epitaxial layer comprises a dislocation density of at least about $1x10^5$ dislocations/cm^2.

24. The method of claim 21, wherein forming the epitaxial layer is conducted in a three-dimensional growth mode, wherein forming comprises forming the epitaxial layer in a two-dimensional growth mode, wherein forming comprises changing at least one of the growth process parameters during growth of the epitaxial layer as compared to the process parameters.

25. The method of claim 21, further comprising separating the base layer, mask, and epitaxial layer from the growth substrate during forming of at least one of the base layer, mask, and epitaxial layer, wherein separating comprises thermal decomposition of at least a portion of a buffer layer between the growth substrate and the base layer.

26. A method of forming a semiconductor substrate comprising:

a) forming a base layer of a Group 13-15 material on a growth substrate;

b) forming a mask comprising a nitride material overlying the base layer;

c) etching and preferentially removing portions of the base layer and the mask after forming the mask; and

wherein steps a), b), and c) are conducted in-situ during a single operation within a growth chamber.

27. A method of forming a semiconductor substrate comprising:

forming a base layer comprising GaN on a growth substrate during a growth process, the growth substrate comprising:

a sapphire base substrate; and

a buffer layer overlying the growth substrate and disposed between the base substrate and the base layer;

forming a mask comprising mask regions and gap regions between the mask regions overlying the base layer; and

preferentially removing a portion of the base layer underlying the mask.

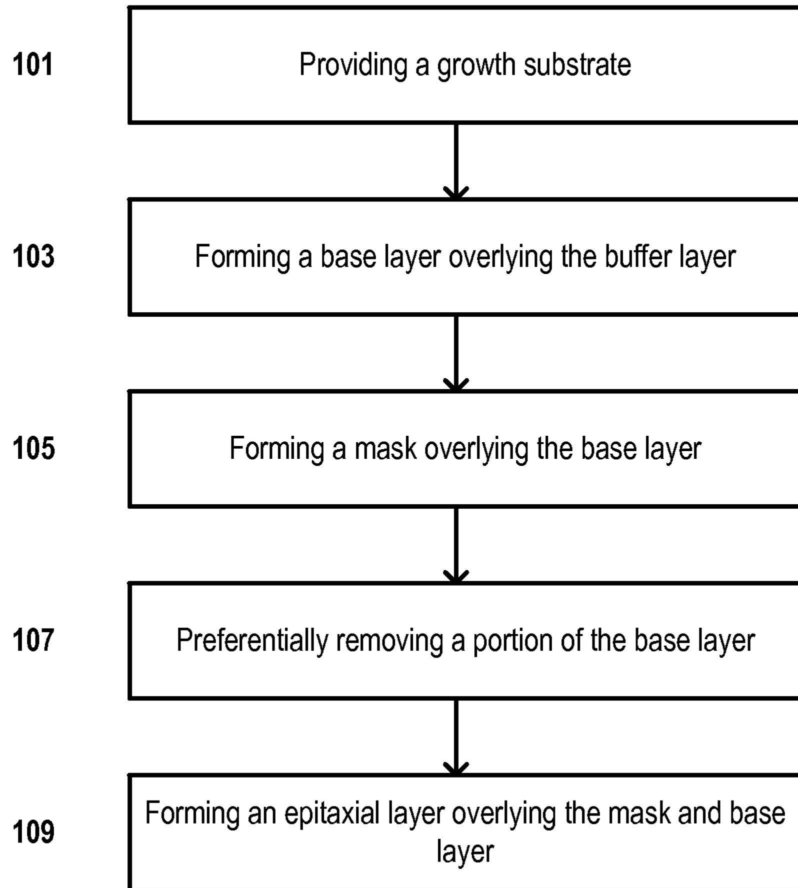

FIG. 1

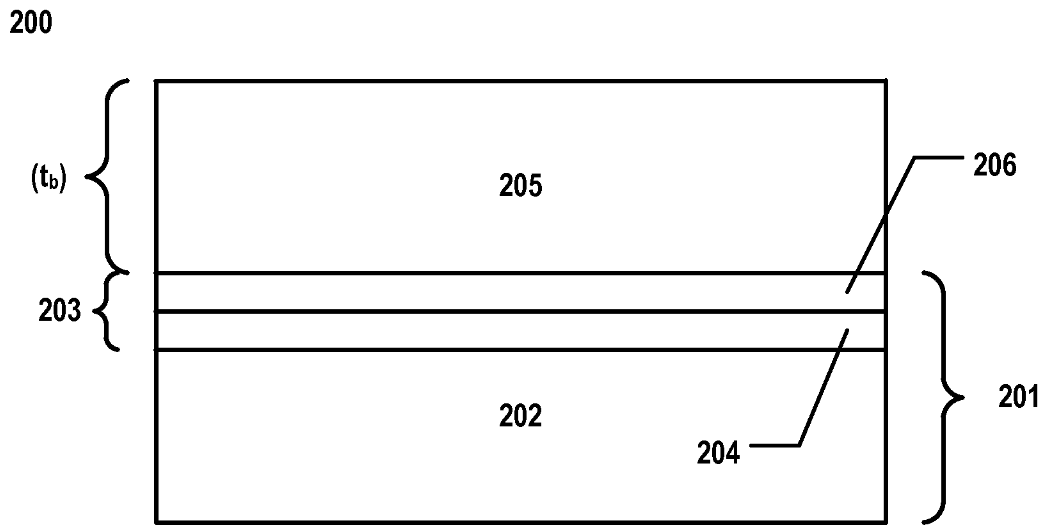

FIG. 2A

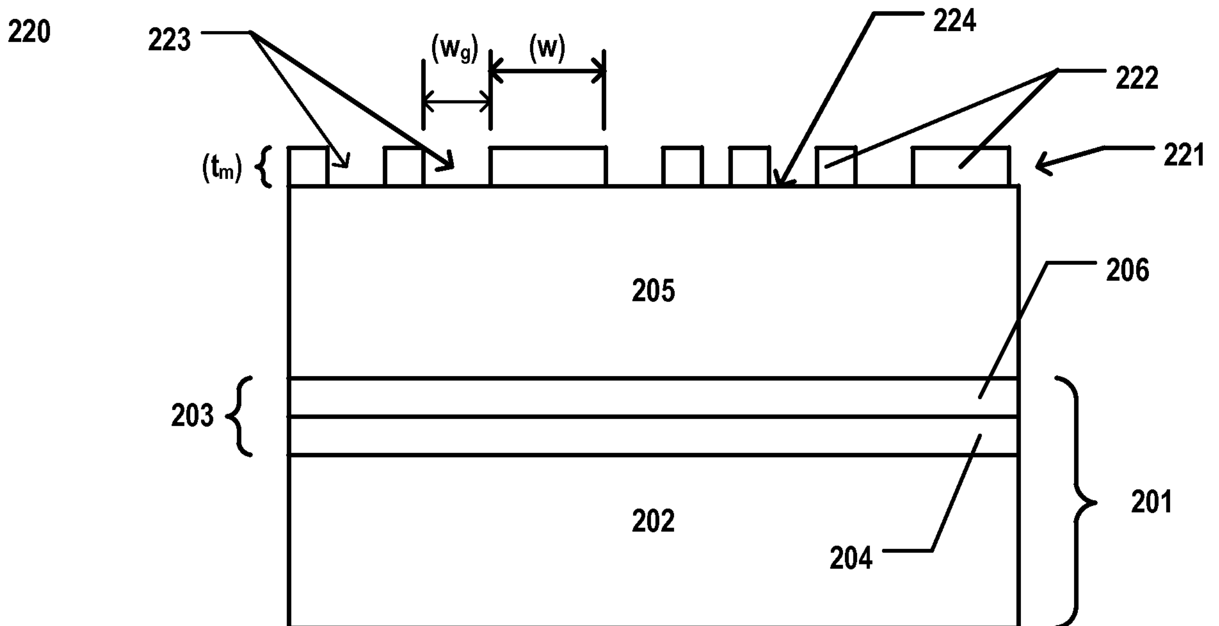

FIG. 2B

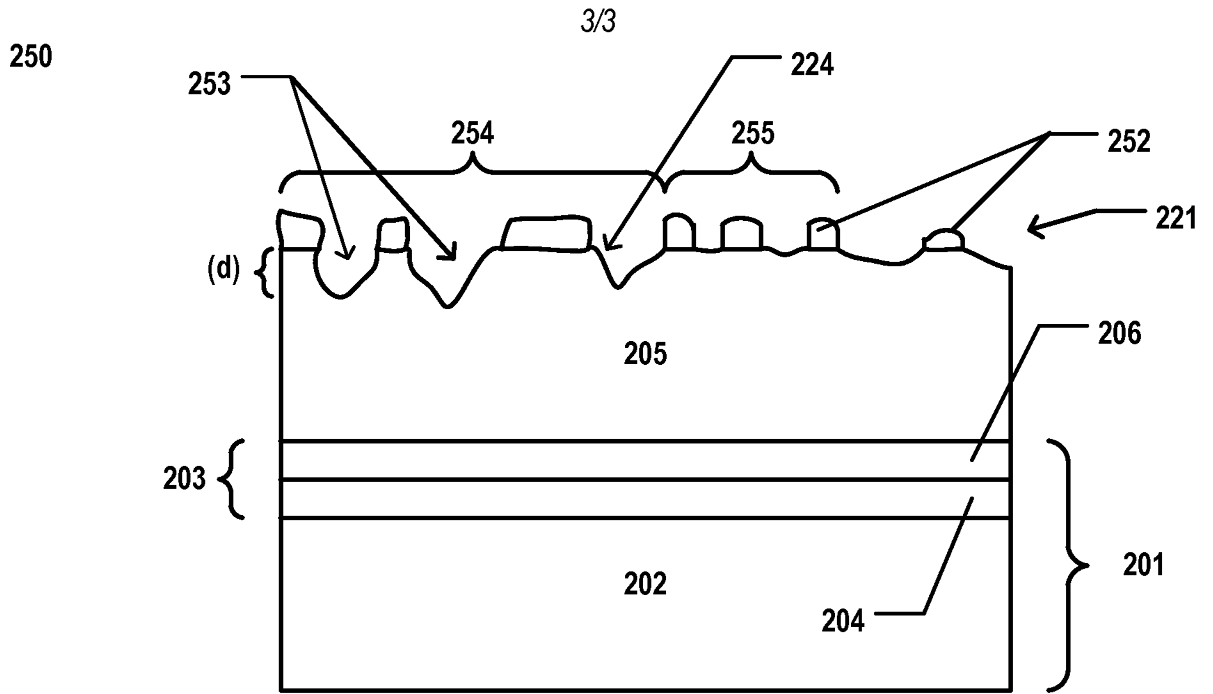

FIG. 2C

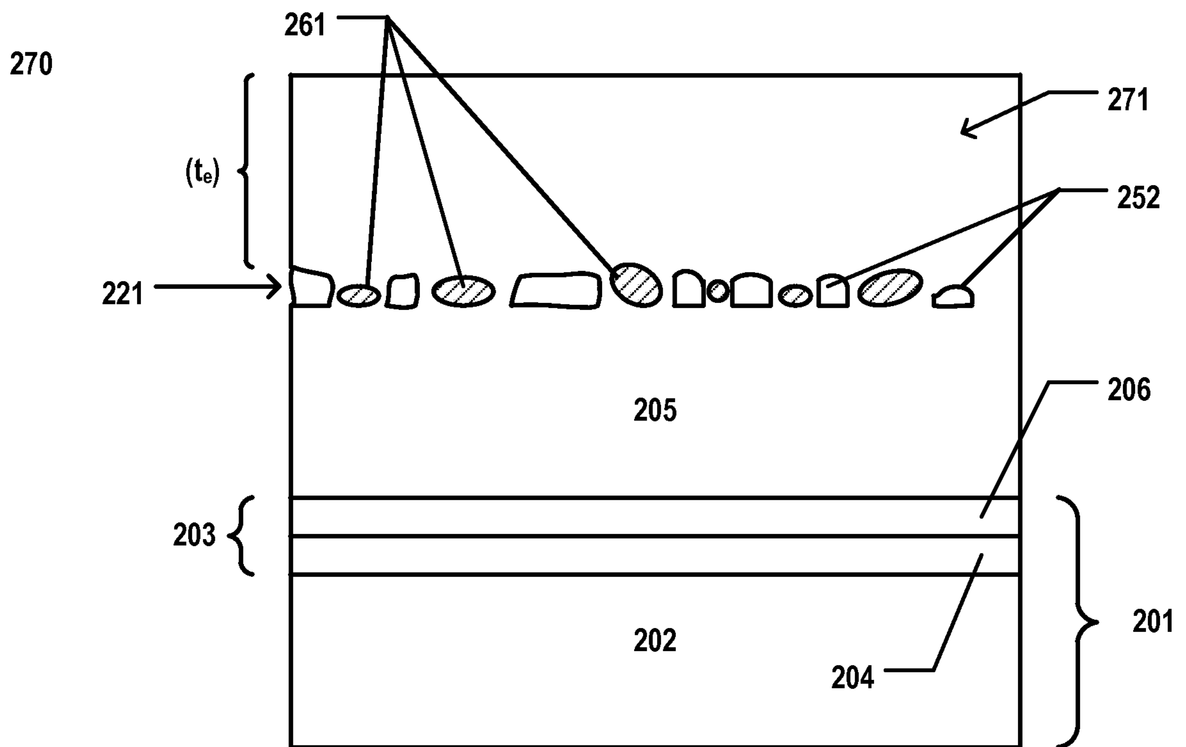

FIG. 2D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/065886

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/20(2006.01)i, H01L 33/00(2010.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/20; H01S 3/18; H01L 29/778; H01L 21/302; C30B 33/08; H01L 21/338; H01L 33/00; H01L 29/205; H01L 29/20; C30B 29/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords:layer,gallium,mask,etch,remove

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2008-124262 A (OKI ELECTRIC IND CO., LTD.) 29 May 2008 See claim 1,pages 6-7, figures 1-2.	1-27
A	JP 11-035397 A (MITSUBISHI CABLE IND LTD.) 09 February 1999 See abstract, claim 1, figure 1.	1-27
A	US 2008-0105903 A1 (KODAMA MASAHITO et al.) 08 May 2008 See abstract, pages 3-4.	1-27
A	US 2010-0244197 A1 (ARENA CHANTAL et al.) 30 September 2010 See abstract, claim 1, figure 1.	1-27
A	JP 10-335749 A (SHARP CORP.) 18 December 1998 See abstract, claim 1, figure 1.	1-27

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 March 2013 (29.03.2013)	**01 April 2013 (01.04.2013)**

Name and mailing address of the ISA/KR

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Facsimile No. 82-42-472-7140

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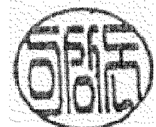
LEE, Sang Don

Telephone No. 82-42-481-5665



INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2012/065886

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2008-124262 A	29.05.2008	CN 101183647 A0	21.05.2008
		US 2008-0176366 A1	24.07.2008
JP 11-035397 A	09.02.1999	JP 3569111 B2	22.09.2004
US 2008-0105903 A1	08.05.2008	JP 04-283840 B2	27.03.2009
		JP 2008-108843 A	08.05.2008
		JP 4283840 B2	24.06.2009
		US 7696071 B2	13.04.2010
US 2010-0244197 A1	30.09.2010	US 8178427 B2	15.05.2012
		WO 2010-112540 A1	07.10.2010
JP 10-335749 A	18.12.1998	JP 04-033519 B2	16.01.2008
		JP 11-017272 A	22.01.1999
		US 06091083A A	18.07.2000