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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :		(11) International Publication Number:
H03K 19/23	A1	WO 92/20159
		(43) International Publication Date: 12 November 1992 (12.11.92)

(21) International Application Number: PCT/US92/03575

(22) International Filing Date: 6 May 1992 (06.05.92)

(30) Priority data:
696,462 6 May 1991 (06.05.91) US

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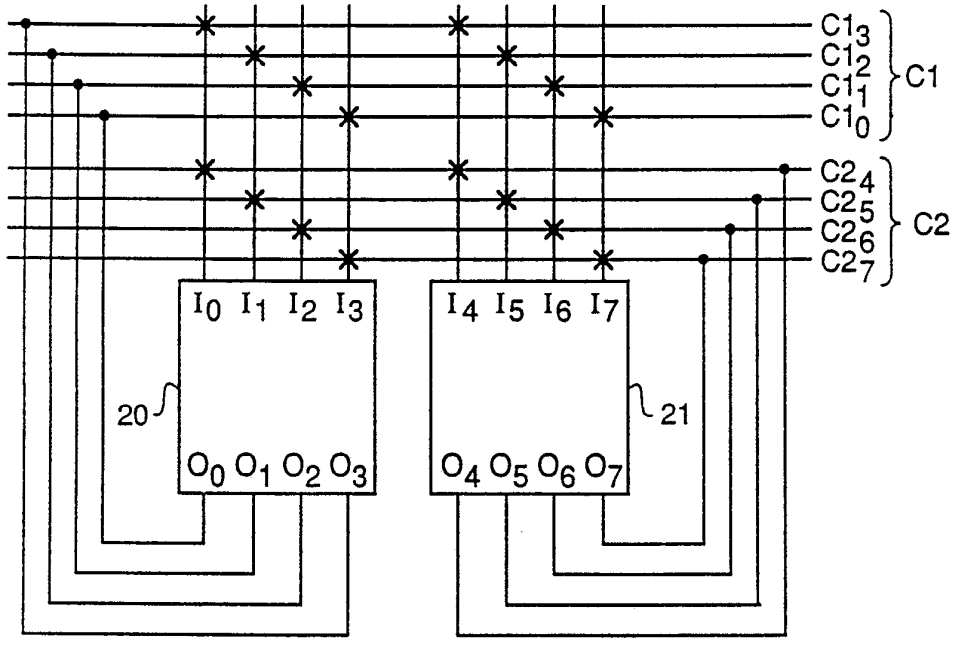
(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, KR, LU (European patent), MC (European patent), NL (European patent), SE (European patent).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: PROGRAMMABLE INTERCONNECT STRUCTURE FOR LOGIC BLOCKS



(57) Abstract

A structure for making programmable connections (X) between the input (I_0-I_7) and (O_0-0_7) output terminals of individual logic (20, 21) blocks in a logic device is disclosed. In one embodiment, each output terminal (O_0-0_7) is programmably connected to only one input terminal (I_0-I_7) of each logic block (20, 21). The same principle is followed in making connections between the input pins of the device and the input terminals of the logic blocks.

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PROGRAMMABLE INTERCONNECT STRUCTURE FOR LOGIC BLOCKS

FIELD OF THE INVENTION

This invention relates to programmable interconnect structures which link the respective inputs and outputs of a plurality of logic blocks, such as in field programmable gate arrays and high density programmable logic arrays, and which link the inputs and outputs of a logic device to each other and to the inputs and outputs of the logic blocks.

BACKGROUND OF THE INVENTION

Logic devices such as field programmable gate arrays (FPGA's) and high density programmable logic devices (HDPLD's) normally consist of a plurality of "logic blocks", each having a number of inputs and a number of outputs. Internally, the typical structure of the logic block consists of a programmable AND array whose outputs feed an OR array. Fig. 1 shows a simplified prior art logic block in the form of a programmable logic device (PLD) wherein inputs I_0 and I_1 feed through a programmable array 10 to four AND gates 11. The outputs of AND gates 11 feed through an array 12 to OR gates 13, and thence to outputs O_0 and O_1. The logic block shown in Fig. 1 is in the familiar sum of the products form, the outputs of AND gates 11 often referred to as the "product terms". In the representative structure shown in Fig. 1 either one of inputs I_0 and I_1 may be connected by means of the array 10 to the inputs of any one or more of AND gates 11.

In a logic device consisting of a number of individual logic blocks, any output of a logic block may need to be connected to an input of the same logic block or an input of one of the other logic blocks. This is accomplished in an area of the chip known as the interconnect area. Also, the external device inputs can be routed to the logic block inputs using the interconnect

area, and similarly the logic block outputs can be routed to external pins and input/output cells as outputs using the same interconnect area. The interconnect area normally comprises a matrix or latticework of intersecting input and output lines, with each output of a logic block intersecting all inputs of the same logic block and all other logic blocks once. Thus, in a device with X inputs and Y outputs, the number of such intersections equals XY.

The prior art solution to the interconnect problem is to place a programmable connection at each of the intersections, thereby allowing every output to be connected to any input in the entire device. Since each of the programmable connections takes up space, this type of arrangement increases the total size of the interconnect area and of the device itself. This increases the cost of the device. Moreover, the number of programmable connections on a given input or output line increases the loading on the line and reduces the speed of the device.

SUMMARY OF THE INVENTION

In one embodiment of an interconnect structure in accordance with this invention, each of a plurality of logic blocks in a logic device has an equal number of inputs and outputs. At each intersection between a group of outputs of a logic block and a group of inputs of a logic block, each individual output line is programmably interconnected with only one of the input lines, forming a diagonal pattern of programmable interconnects. This assures that each output line can be connected to any given logic block through one input to that logic block. A programmable array internal to the block is then used to route the signal as desired within that block. By this technique the number of programmable interconnects required in the interconnect area may be reduced from N^2 (N being the total number of inputs, which equals the total number of outputs) to a minimum of N. This dramatically

reduces the size and cost of the device and improves the speed at which the signals are transmitted from the outputs to the various inputs of the logic blocks. In accordance with this invention, it is not required that the number of programmable connections be reduced to the minimum of N. Any number between N and N^2 may also be selected within in broad principles of this invention.

In the embodiment just described, each logic block has an equal number of inputs and outputs. In many situations this is not an optimal structure, since most logic blocks have fewer outputs than inputs. To overcome this problem, in a second embodiment of the invention, the logic blocks are grouped into what are called "megacells", the logic blocks in each megacell having a combined number of outputs equal to the number of inputs to each block within the megacell. This means that each intersection between the outputs of a megacell and the inputs to a particular logic block will have an equal number of lines crossing each other, and the diagonal pattern of programmable interconnects described above can be implemented, thereby assuring that each output may be connected to one input of every logic block. Use of the programmable interconnect structure of this invention requires that the inputs to the logic block be to some extent interchangeable in the sense that a signal on one input can be programmably transferred within the block. Preferably, there is complete interchangeability, as in the logic block of Fig. 1 where either of inputs I_0 and I_1, can be routed to any or all of AND gates 11. However, this invention is also applicable to logic blocks (e.g., combinations of multiplexers) which have less than complete interchangeability.

The interconnect structure of this invention requires that the interconnections be planned so as to assure complete connectivity, i.e., that the reduced number of programmable connections are used as efficiently as

possible so that every required connection between an output and an input can in fact be made.

DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates the structure of a typical logic block.

Fig. 2 illustrates an interconnect structure in accordance with the invention for logic blocks having an equal number of inputs and outputs.

Fig. 3 illustrates an interconnect structure with the logic blocks grouped into megacells, the number of outputs from a megacell equaling the number of inputs to each logic block within the megacell.

Fig. 4 is an overview of an interconnect structure for a high density programmable logic device consisting of 32 logic blocks.

Figs. 5A, 5B, and 5C illustrate the placement of interconnects at the intersection between a routing channel and, respectively, the outputs of a megacell, the input lines from the input/output cells, and the input lines to the logic blocks, in the embodiment of Fig. 4.

Fig. 6 illustrates an output routing resource arrangement in accordance with another aspect of the invention.

Fig. 7 illustrates another embodiment of an output routing resource arrangement.

Figs. 8A-8E illustrate alternative types of programmable connections which may be used in embodiments of the invention.

DESCRIPTION OF THE INVENTION

Fig. 2 shows a logic block 20 and a logic block 21, each of which has four inputs and four outputs. The inputs and outputs of logic block 20 are designated I_0-I_3 and O_0-O_3, respectively. The inputs and outputs of logic block 21 are designated I_4-I_7 and O_4-O_7, respectively. The outputs O_0-O_3 of logic block 20 are connected respectively

to interconnect lines $C1_0$-$C1_3$ of a routing channel C1. The outputs O_4-O_7 of logic block 21 are connected respectively to interconnect lines $C2_4$-$C2_7$ of a routing channel C2. The connections between the outputs of logic block 20 and routing channel C1 and between the outputs of logic block 21 and routing channel C2 are hard-wired and are not programmable.

Routing channels C1 and C2 intersect the inputs to logic blocks 20 and 21 in a 4X4 matrix. As described above, the prior art solution to providing interconnect capability between the outputs and the inputs of logic blocks 20 and 21 would be to provide a programmable connection at each point of a 4X4 matrix, requiring 16 programmable connections. However, in accordance with the invention, each of the outputs of logic blocks 20 and 21 is provided with a programmable connection with only one of the inputs to logic blocks 20 and 21. The programmable connections are designated by "X's" in Fig. 2. For example, output O_0 may be connected to the inputs of logic block 20 via input I_3 and to the inputs of logic block 21 via input I_7. Similarly, output O_5 of logic block 21 may be connected to the inputs of logic block 21 via input I_5 and to the inputs of logic block 20 via input I_1.

As described above (see Fig. 1), the AND array within a typical field programmable gate array or programmable logic device allows the designer to connect the inputs to the AND gates within the device in any desired manner. For example, if outputs O_0 and O_5 are to be ANDed in logic block 21, a connection can be programmed between output O_0 ($C1_0$) and the line to input I_7, and a connection can be programmed between output O_5 ($C2_5$) and the line to input I_5. Inputs I_5 and I_7 can then be connected to respective inputs of an AND gate within logic block 21.

The technique of this invention accordingly allows the total number of programmable inputs in the structure shown in Fig. 2 to be reduced from a total of 64 to a minimum of 16.

Relatively few logic blocks have an equal number of inputs and outputs like logic blocks 20 and 21. Generally, there are fewer outputs than inputs. To apply the principles of this invention to logic blocks having unequal numbers of inputs and outputs, a structure such as that shown in Fig. 3 is used. In Fig. 3, logic blocks 30 and 31 each have four inputs and two outputs. Logic blocks 30 and 31 are grouped in a megacell 32 which has outputs O_0-O_3. These outputs are connected to lines $C1_0$-$C1_3$, respectively, of a routing channel C1. Respective sets of four programmable connections (designated by X's) connect lines $C1_0$-$C1_3$ to inputs I_0-I_3 and inputs I_4-I_7.

An examination of Fig. 3 will indicate that each of outputs O_0-O_3 may be linked via the programmable connections with one input of each of logic blocks 30 and 31. For example, output O_1 has access to logic block 31 via the programmable connection between line $C1_1$ and the line to input I_5. Similarly, output O_3 has access to logic block 30 via the programmable connection between line $C1_3$ and the line to input I_3. Since inputs I_0-I_3 of logic block 30 can be ANDed in any desired combination at the AND gates within logic block 30, outputs O_0-O_3 can be ANDed in the same ways via the programmable connections between lines $C1_0$-$C1_3$ and the lines to inputs I_0-I_3, respectively. Outputs O_0-O_3 can likewise be ANDed in logic block 31 by means of the programmable connections between lines $C1_0$-$C1_3$ and the lines to inputs I_4-I_7, respectively.

Fig. 4 shows an HDPLD containing 32 logic blocks designated A-0 to A-7, B-0 to B-7, C-0 to C-7, and D-0 to D-7. Each of these logic blocks has 16 inputs (an "input channel") and 4 outputs. To preserve the clarity of the drawing, individual input and output lines are not shown. Instead, a single line represents all of the inputs to a logic block, and another single line represents all of the outputs from a logic block. Logic blocks A-0 to D-7 have been grouped into 8 megacells, as follows: A-0 to A-3, A-4 to A-7, B-0 to B-3, B-4 to B-7, C-0 to C-3, C-4 to C-

7, D-0 to D-3, and D-4 to D-7. The 16 outputs of each megacell are shown as output channels Q_0-Q_3 and Q_8-Q_{11}, each of which contains 16 output lines. Routing channels C_0-C_{11}, each containing 16 interconnect lines, are also shown. Signals flow to and from the HDPLD through input/output (I/O) blocks IO-1, IO-2, IO-3 and IO-4, each of which contains 16 I/O pins.

Input channels Q_4-Q_7 from I/O blocks IO-1 to IO-4 (each input channel containing 16 input lines) are hard-wired to routing channels C_4-C_7, respectively, one line of input channels Q_4-Q_7 being hard-wired to one line of routing channels C_4-C_7, respectively. The connections between output channels Q_0-Q_3 and Q_8-Q_{11} and routing channels C_0-C_3 and C_8-C_{11} are hard wired so that one line of each output channel is connected to one line of the corresponding routing channel. Thus each of routing channels C_0-C_{11} is an extension of a corresponding one of output channels Q_0-Q_3 and Q_8-Q_{11} or of I/O blocks IO-1 to IO-4.

Figure 5A shows in detail the hard-wire connections between the outputs of the megacell consisting of logic blocks A-0 to A-3 and the interconnect lines in routing channel C_0. As shown, output 0 of logic block A-0 is connected to interconnect line R0, output 1 of logic block A-0 is connected to interconnect line R1, etc. A similar pattern is followed in making the connection between the outputs of the megacells consisting of logic blocks A-4 to A-7, B-0 to B-3, B-4 to B-7, C-0 to C-3, C-4 to C-7, D-0 to D-3, and D-4 to D-7 with routing channels C_1 to C_3 and C_8 to C_{11}, respectively.

Fig. 5B shows in detail the hard-wire connections between the lines of input channel Q_4 and the interconnect lines in routing channel C_4. Line Z0 of channel Q_4 is connected to interconnect line S0, line Z1 of channel Q_4 is connected to interconnect line S1, etc. A similar pattern is followed in making the hard-wire connections between

input/output blocks IO-2, IO-3 and IO-4 and routing channels C_5, C_6 and C_7, respectively.

Fig. 5C shows in detail the programmable connections between routing channel C_0 and the input channels to logic blocks B-7 and C-0. The input channel to logic block B-7 includes input lines X0 to X15. The input channel to logic block C-0 includes input lines Y0 to Y15. Routing channel C_0 includes interconnect lines R0 to R15. Each of interconnect lines R0-R15 is programmable connected to one of lines X0-X15 and one of lines Y0-Y15. Thus line R0 is programmably connected to lines X0 and Y0, line R1 is programmably connected to lines X1 and Y1, etc.

This pattern is repeated throughout the array. In general, a line in a particular position in an input channel is programmably connected to lines in the equivalent position of routing channels C_0-C_{11}. For example, line Y0 is programmably connected to the line in the "0" position of routing channels C_0-C_{11}. Line Y1 is programmably connected to the corresponding line in the "1" position of each of these routing channels. This enables any given output to be connected to one input of each of logic blocks A-0 to D-7. For example, referring to Figs. 5A and 5C, output 10 of logic block A-2, which is connected to interconnect line R10, would have access to logic block B-7 through input line X10 and to logic block C-0 through input line Y10. As described previously, once a signal on input lines X10 or Y10 reaches logic blocks B-7 or C-0, respectively, it can be ANDed with any of the other inputs to those logic blocks by means of internal programmable connections. Similarly, referring to Fig. 5B, line Z10 of input channel Q_4, which is connected to interconnect line S10, would have access to logic block B-7 through input line X10 and logic block C-0 through input line Y10.

Accordingly, the programmable interconnect structure of this invention permits the total number of programmable connections at each intersection of one of routing

channels C_0 to C_{11} with the input channels to one of logic blocks A-0 to D-7 to be reduced from a total of 256 to a minimum of 16. In accordance with this invention, it is not necessary that the number of programmable connections be reduced to the minimum number of 16. Any number between 16 and 256 could also be selected, depending on the routing demands of the particular application. In practice, the selection of the number of programmable connections to be used will often require a balancing of the space limitations imposed on the interconnect structure against the need to provide maximum routability.

A constraint of the interconnect structure shown in Fig. 4 is that once a particular line of a routing channel has been used to gain access to a logic block, no interconnect line in the same position of any other routing channel may be used for inputting signals to the same logic block. No two signals that are input to a particular logic block may be located on interconnect lines in the same position. In the example given above, if interconnect line R10 of routing channel C_0 is used to connect output 10 of logic block A-3 to an input of logic block B-7, no interconnect line in the "10" position of routing channels C_1-C_{11} may be used to transmit a signal to logic block B-7.

The transfer function to be performed by the HDPLD shown in Fig. 4 is partitioned by known techniques into the individual logic blocks. The resulting logic blocks are then placed in the available positions on the device, and the outputs of each logic block are arranged so as to assure that all required connections between the inputs and outputs of the logic blocks and the I/O cells can be made.

I/O blocks I0-1 to I0-4 each contain 16 I/O cells of the kind disclosed in U.S. Application Serial No. 07/696,907, filed May 6, 1991, which is incorporated herein by reference, as well as an output routing resource arrangement of the kind illustrated in Fig. 6, described

below, wherein 32 logic block outputs are programmably connected through a programmable matrix to 16 I/O cells. As described in the above-noted U.S. Application Serial No. 07/696,907 (see Fig. 6 thereof), each I/O cell contains an I/O pin.

In the routing process, as the logic blocks are placed and their outputs are assigned a sequence, a conflict may occur between the configuration required for routing purposes and the external pin assignments of the device. For example, a given output may be assigned to a particular position where it is connected to a pin which is required for an input or for a different output. If the external requirements of pin assignment are satisfied, the routability of the device may become more difficult.

This problem is minimized by the output routing resource arrangement which is shown in Fig. 6. Fig. 6 shows logic blocks A-0 to A-7 and the 16 I/O cells IO_0-IO_{15} associated with I/O block IO-1. Each of routing resource channels RR0, RR1, RR2 and RR3 contains four lines 0, 1, 2 and 3. Each of cells IO_0-IO_{15} is hard-wired to one of the lines in channels RR0 to RR3. For example, cell IO_0 is connected to line 0 of channel RR0; cell IO_1 is connected to line 1 of channel RR0; etc. Each output of logic blocks A-0 to A-7 is programmably connected to a line in a given position of each of channels RR0 to RR3. For example, output 0 of logic block A-0 is programmably connected to line 0 of each of channels RR0 to RR3; output 1 of logic block A-0 is programmably connected to line 1 of each of channels RR0 to RR3; etc. This structure permits any output of logic blocks A-0 to A-7 to be shifted among four of cells I_0-I_{15}. For example, output 0 of logic block A-0 may be routed to cells IO_0, IO_4, IO_8 or IO_{12}. If cell IO_0 is needed for a particular external purpose, the arrangement of logic blocks A-0 to A-7 need not be affected. The remaining cells IO_1-IO_{15} may be used to handle the outputs of logic blocks A-0 to A-7.

As illustrated in Fig. 7, a similar flexibility in assigning pins can be provided by providing programmable connections between the I/O pins and the routing channels which are used to link the inputs of the logic blocks with the I/O cells and the outputs of the logic blocks, as described above. Fig. 7 is an expansion of Fig. 3, showing in addition I/O pins P_0, P_1, P_2, and P_3 which are programmably connected to interconnect lines $C1_0$-$C1_3$ of routing channel C1, in an interconnect matrix 70. By making the appropriate connections in matrix 70 each of outputs O_0-O_3 may be connected to any of pins P_0-P_3.

The programmable interconnect structure of this invention can be used with any type of logic block having a plurality of inputs and a plurality of outputs, including but not limited to programmable logic devices (PLD's), such as programmable array logic/generic array logic circuits (PAL/GAL's) and programmable logic arrays (PLA's), random access memories (RAM's), programmable read only memories (PROM's), erasable programmable read only memories (EPROM's), electrically erasable programmable read only memories (EEPROM's) and combinations of multiplexers.

Moreover, the programmable connections used in embodiments of this invention may be made by any means or technique of programming a connection between electrical conductions paths, including but not limited to bipolar fuses (Figs. 8A and 8B), antifuses, and CMOS pass gates (Fig. 8C) or antifused tristate buffers with enable/disable fuses (Figs. 8D and 8E) controlled by SRAM's, EPROM's, EEPROM's or other memory cells. The programmable connection described in application Serial No. 07/696543 co-owned and filed May 6, 1991, which is hereby incorporated herein by reference, may also be used.

While certain embodiments of this invention have been described, other embodiments of this invention will be obvious to those skilled in the art as a result of this description.

CLAIMS:

We claim:

1. A programmable interconnect matrix between a plurality of outputs of at least one logic block and a plurality of inputs to at least one logic block wherein not every one of said inputs is programmably connected to each of said outputs.

2. A programmable interconnect structure comprising:

one or more logic blocks;

an input channel to each of said one or more logic blocks, each said input channel comprising a plurality of input lines;

a plurality of signal routing channels, each of said signal routing channels comprising a plurality of signal routing lines; and

a matrix of programmable connections between each of said input channels and each of said signal routing channels wherein the number of said programmable connections in each said matrix is less than the number of input lines multiplied by the number of signal routing lines and equal to or greater than the number of input lines.

3. The programmable interconnect structure of Claim 2 comprising a plurality of output lines from each of said logic blocks, the output lines from each of said logic blocks being connected to predetermined signal routing lines in a predetermined one of said signal routing channels.

4. The programmable interconnect structure of Claim 3 comprising a plurality of device terminals, said device terminals being separated into groups, the device terminals in each of said groups being connected to

predetermined signal routing lines in a predetermined one of said signal routing channels.

5. The programmable interconnect structure of Claim 4 wherein said logic blocks are grouped into megacells, the output lines from the logic blocks in each of said megacells being connected to predetermined signal routing lines in a predetermined one of said signal routing channels, the number of output lines from the logic blocks in each of said megacells being equal to the number of signal routing lines in the signal routing channel to which said output lines are connected.

6. The programmable interconnect structure of Claim 5, the number of signal routing lines in each of said signal routing channels being equal to the number of input lines in each of said input channels.

7. The programmable interconnect structure of Claim 3 comprising a plurality of resource routing lines and a plurality of device terminals, predetermined ones of said output lines being programmably connectable to predetermined ones of said resource routing lines, predetermined ones of said resource routing lines being connected to predetermined ones of said device terminals.

8. The programmable interconnect structure of Claim 7 wherein said logic blocks are grouped into megacells, the output lines from the logic blocks in each of said megacells being connected to predetermined signal routing lines in a predetermined one of said signal routing channels, the number of output lines from the logic blocks in each of said megacells being equal to the number of signal routing lines in the signal routing channel to which said output lines are connected.

9. The programmable interconnect structure of Claim 3 comprising:

a plurality of device terminals, said device terminals being separated into groups, the device terminals in each of said groups being connected to predetermined signal routing lines in a predetermined one of said signal routing channels; and

a plurality of resource routing lines, predetermined ones of said output lines being programmably connectable to predetermined ones of said resource routing lines, predetermined ones of said resource routing lines being connected to predetermined ones of said device terminals.

10. The programmable interconnect structure of Claim 9 wherein said logic blocks are grouped into megacells, the output lines from the logic blocks in each of said megacells being connected to predetermined signal routing lines in a predetermined one of said signal routing channels, the number of output lines from the logic blocks in each of said megacells being equal to the number of signal routing lines in the signal routing channel to which said output lines are connected.

11. The programmable interconnect structure of Claim 2 comprising a plurality of device terminals, said device terminals being separated into groups, the device terminals in each of said groups being connected to predetermined signal routing lines in a predetermined one of said signal routing channels.

12. The programmable interconnect structure of Claim 11 comprising a plurality of output lines from each of said logic blocks and a plurality of resource routing lines, predetermined ones of said output lines being programmably connectable to predetermined ones of said resource routing lines, predetermined ones of said

resource routing lines being connected to predetermined ones of said device terminals.

13. The programmable interconnect structure of Claim 12 wherein said logic blocks are grouped into megacells, the output lines from the logic blocks in each of said megacells being connected to predetermined signal routing lines in a predetermined one of said signal routing channels, the number of output lines from the logic blocks in each of said megacells being equal to the number of signal routing lines in the signal routing channel to which said output lines are connected.

14. The programmable interconnect structure of Claim 2 comprising a plurality of output lines from each of said logic blocks, a plurality of device terminals, and a plurality of resource routing lines, predetermined ones of said output lines being programmably connectable to predetermined ones of said resource routing lines, predetermined ones of said resource routing lines being connected to predetermined ones of said device terminals.

15. The programmable interconnect structure of Claim 2 comprising a plurality of output lines from each of said logic blocks, said output lines being connected to predetermined ones of said signal routing lines, and comprising a plurality of device terminals, each of said device terminals being programmably connectable to predetermined ones of said signal routing lines.

16. A programmable logic device comprising a plurality of logic blocks, each of said logic blocks having a plurality of input terminals connected to respective input lines and a plurality of output terminals connected to respective output lines, each of said output lines being programmably connectable to at least one but

less than all of the input lines for each of said logic blocks.

17. The programmable logic device of Claim 16 wherein each of said output lines is programmably connectable to only one input line for each of said logic blocks.

18. A programmable logic device comprising a plurality of logic blocks, each of said logic blocks having a plurality of input terminals connected to respective input lines and a plurality of device terminals, each of said device terminals being programmably connectable to at least one but less than all of the input lines for each of said logic blocks.

19. The programmable logic device of Claim 18 wherein each of said device terminals is programmably connectable to only one input line for each of said logic blocks.

20. A programmable logic device comprising a plurality of logic blocks, each of said logic blocks having a plurality of output terminals connected to respective output lines, and a plurality of device terminals, each of said output terminals being programmably connectable to a plurality of said device terminals.

21. A programmable logic device comprising:

a plurality of logic blocks, each of said logic blocks having a plurality of input terminals connected to respective input lines and a plurality of output terminals connected to respective output lines, and

a plurality of device terminals,

wherein each of said output lines is programmably connectable to at least one but less than all of the input lines for each of said logic blocks, and each of said device terminals is programmably connectable to at least one but less than all of the input lines for each of said logic blocks.

22. A programmable logic device comprising a plurality of logic blocks, each of said logic blocks having a plurality of input terminals connected to respective input lines and a plurality of output terminals connected to respective output lines, and a plurality of device terminals, wherein each of said output lines is programmably connectable to at least one but less than all of the input lines for each of said logic blocks, and each of said output terminals is programmably connectable to a plurality of said device terminals.

23. A programmable logic device comprising a plurality of logic blocks, each of said logic blocks having a plurality of input terminals connected to respective input lines and a plurality of output terminals connected to respective output lines, and

a plurality of device terminals,

wherein each of said device terminals is programmably connectable to at least one but less than all of the input lines for each of said logic blocks, and each of said output terminals is programmably connectable to a plurality of said device terminals.

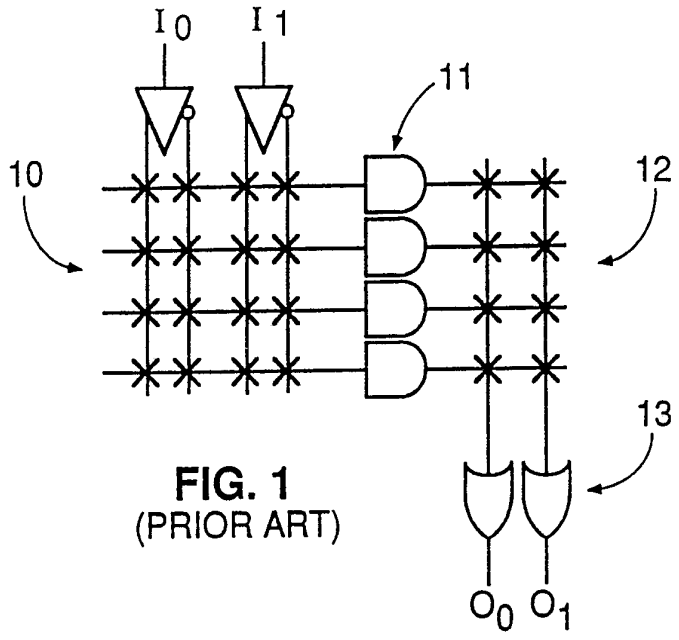


FIG. 1
(PRIOR ART)

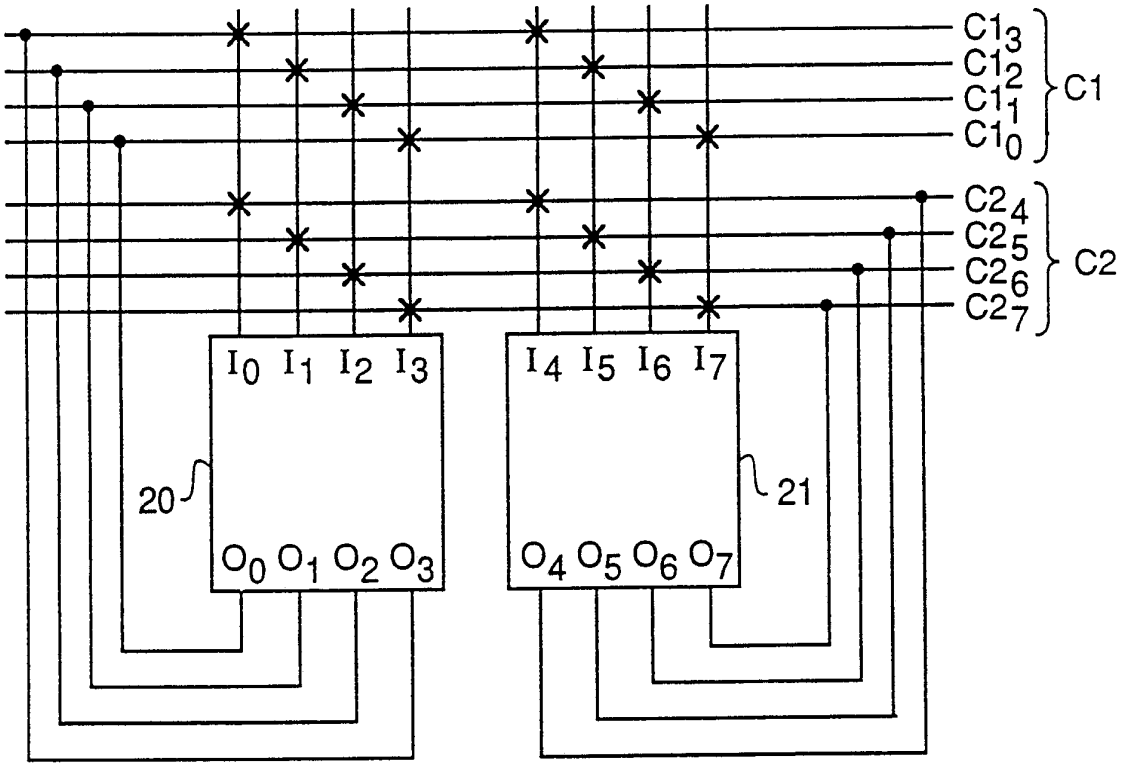


FIG. 2

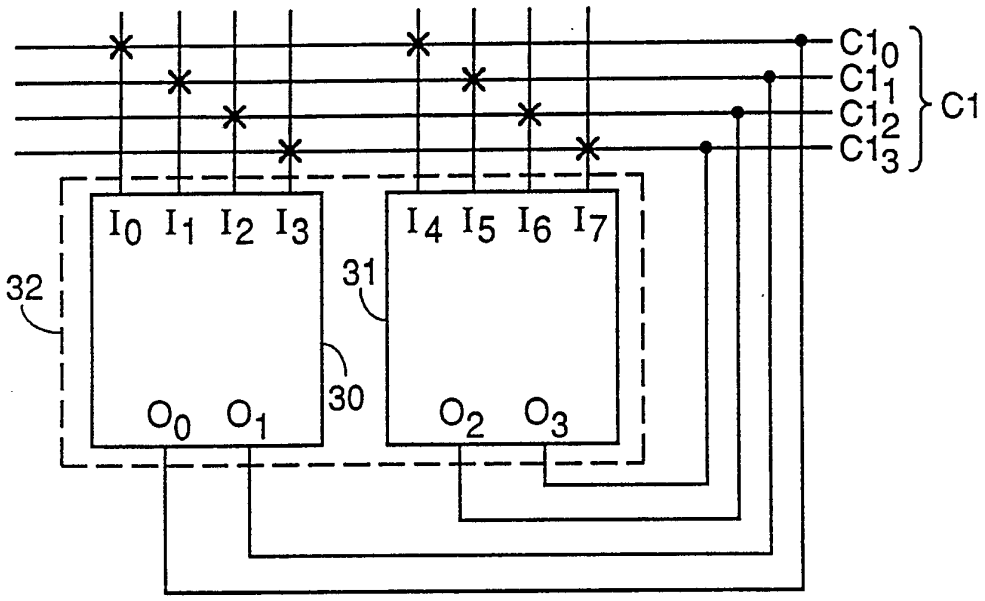


FIG. 3

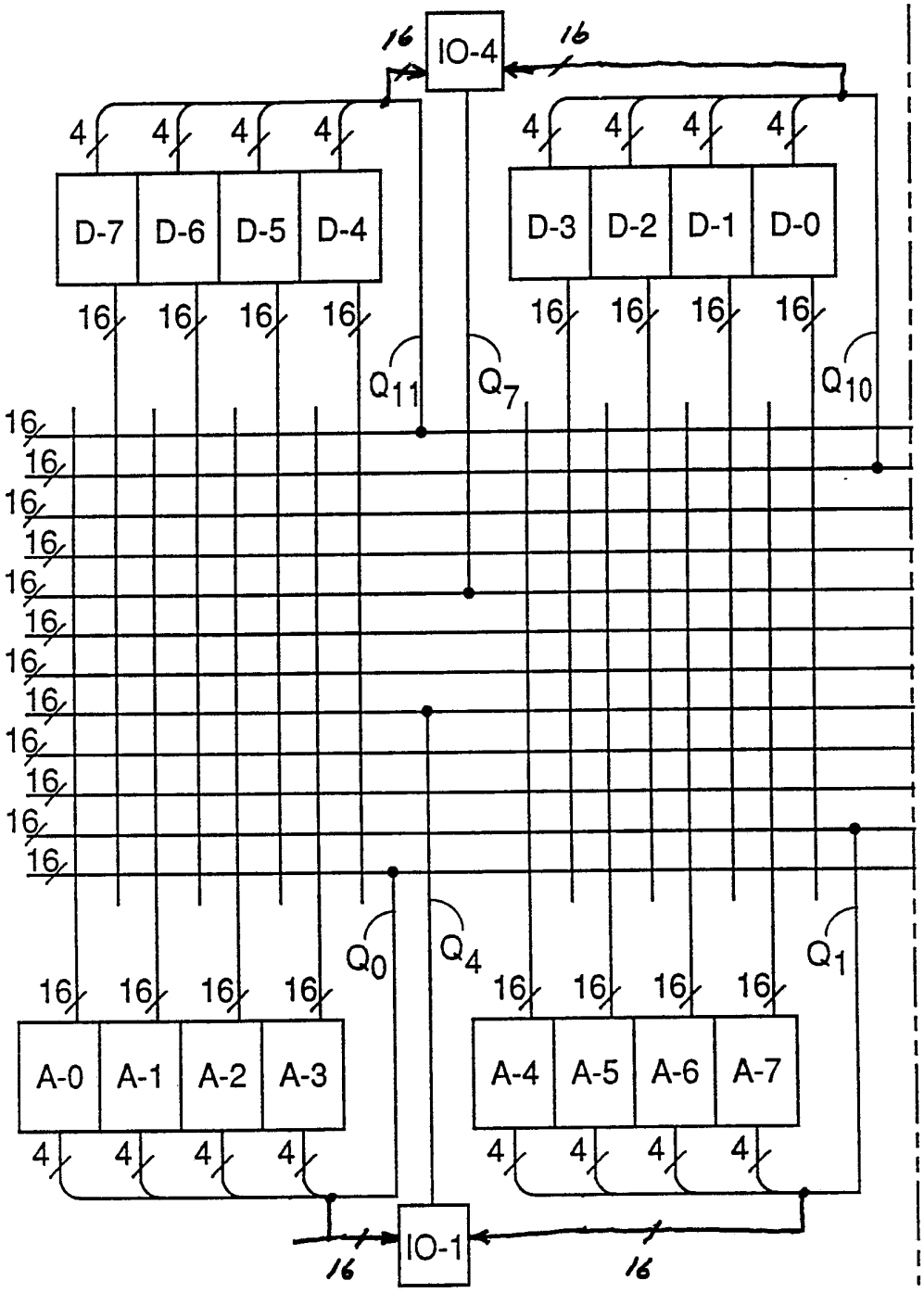


FIG. 4A

KEY TO FIG. 4

FIG. 4A	FIG. 4B

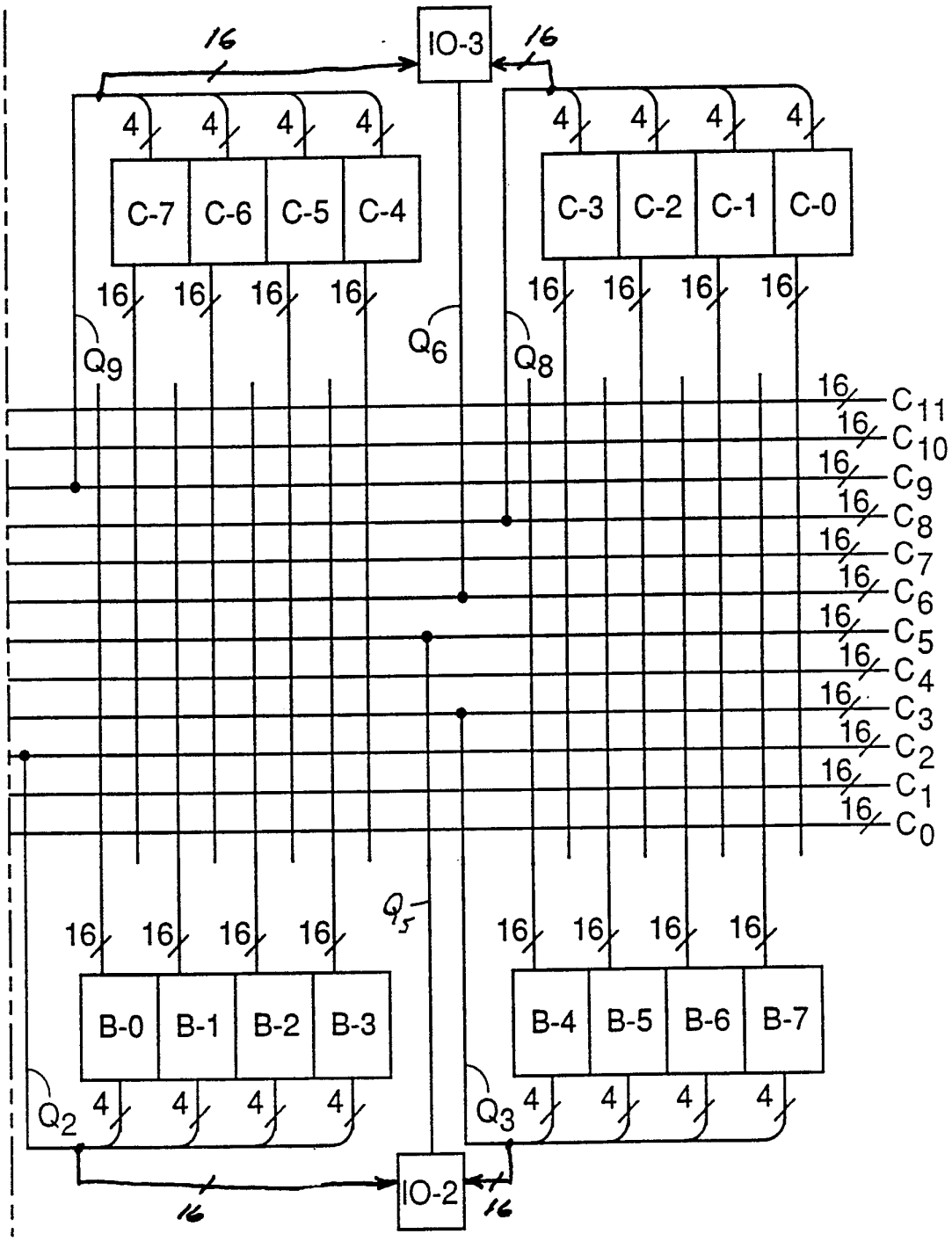

IO-3
IO-2
C-7
C-6
C-5
C-4
C-3
C-2
C-1
C-0
B-0
B-1
B-2
B-3
B-4
B-5
B-6
B-7
16
4
Q9
Q6
Q8
Q5
Q2
Q3
C11
C10
C9
C8
C7
C6
C5
C4
C3
C2
C1
C0

FIG. 4B

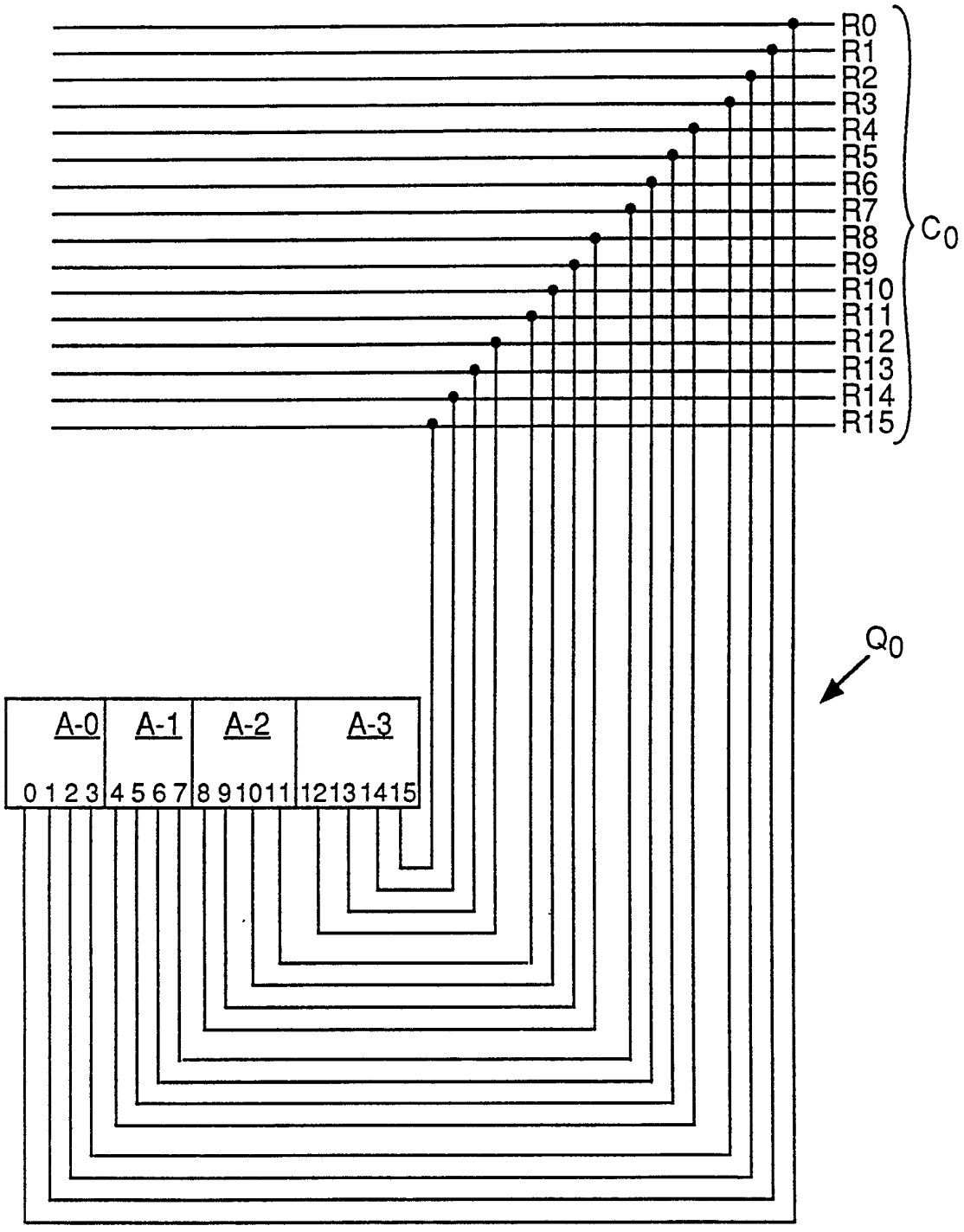

R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
C0
Q0
A-0
A-1
A-2
A-3
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

FIG. 5A

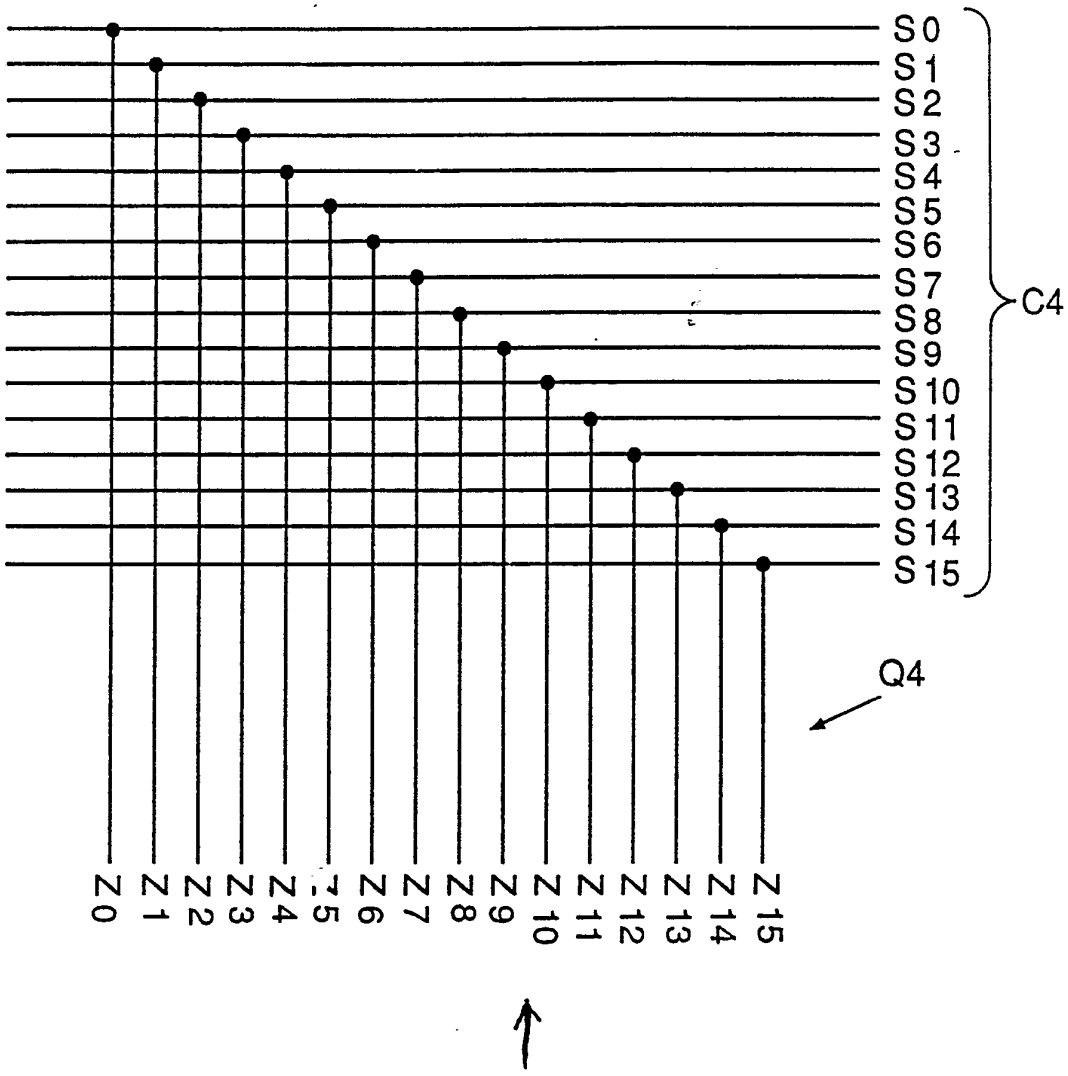

S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
C4
Q4
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
Z9
Z10
Z11
Z12
Z13
Z14
Z15
FROM I/O CELL I/O-1

FIG. 5B

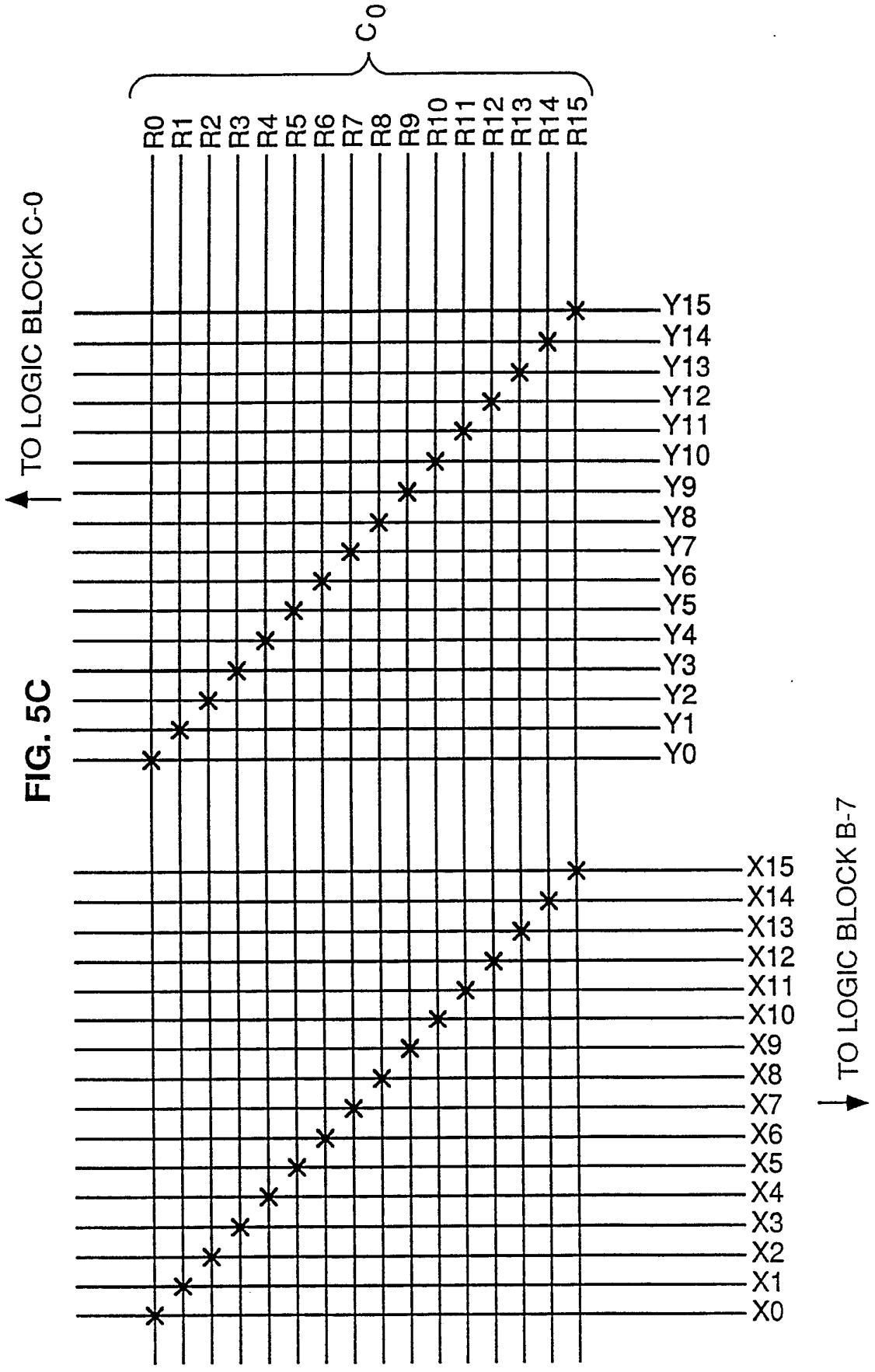
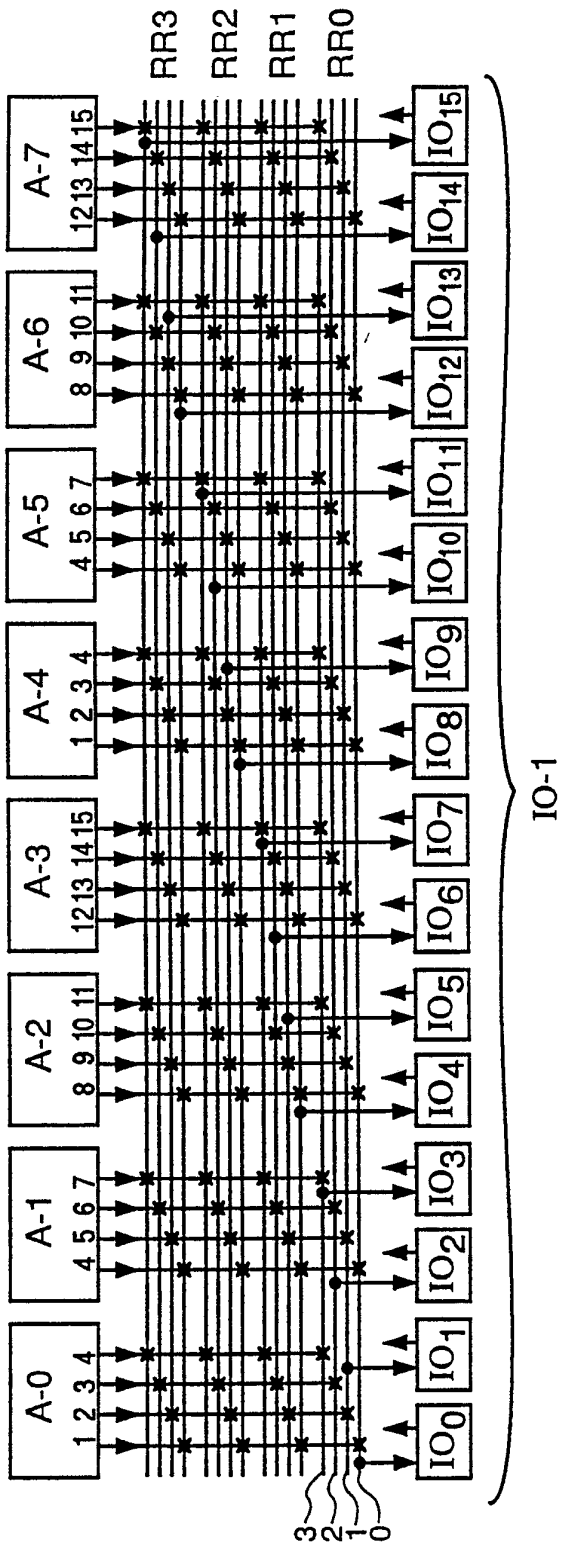

C0
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
TO LOGIC BLOCK C-0
Y15
Y14
Y13
Y12
Y11
Y10
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
X15
X14
X13
X12
X11
X10
X9
X8
X7
X6
X5
X4
X3
X2
X1
X0
TO LOGIC BLOCK B-7

FIG. 5C

FIG. 6


RR3
RR2
RR1
RR0
A-0
1 2 3 4
A-1
4 5 6 7
A-2
8 9 10 11
A-3
12 13 14 15
A-4
1 2 3 4
A-5
4 5 6 7
A-6
8 9 10 11
A-7
12 13 14 15
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
IO-1
3
2
1
0

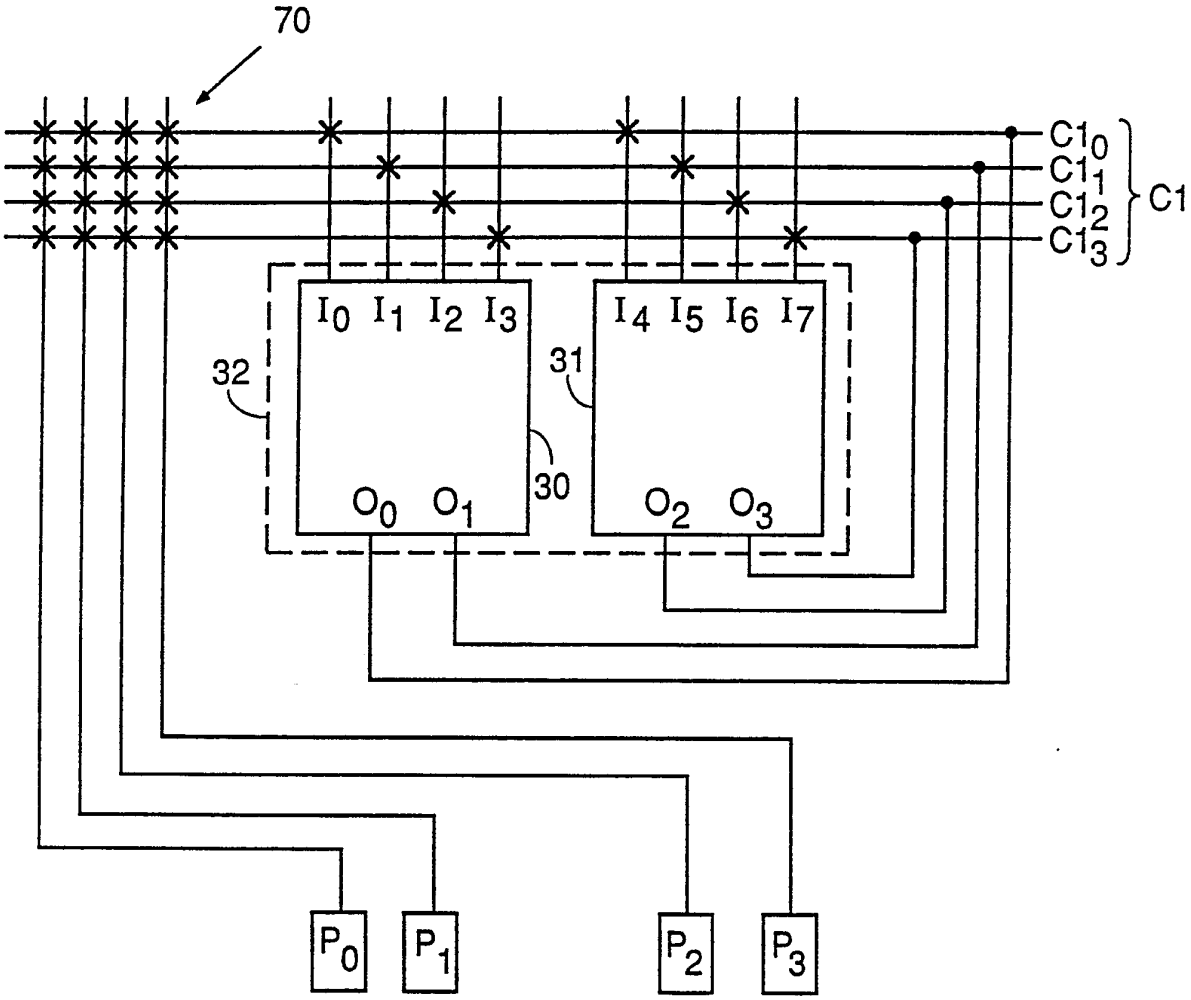
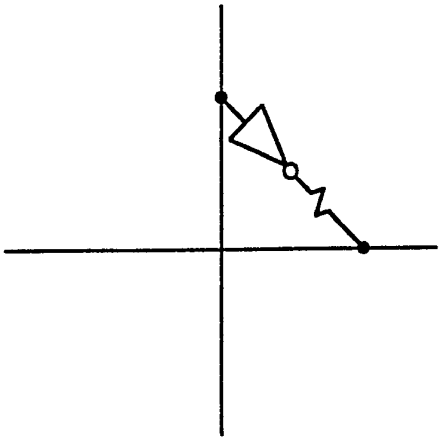
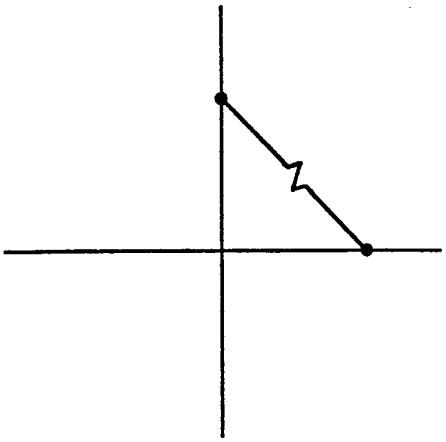

70
C1₀
C1₁
C1₂
C1₃
C1
I₀ I₁ I₂ I₃
I₄ I₅ I₆ I₇
32
31
30
O₀ O₁
O₂ O₃
P₀
P₁
P₂
P₃

FIG. 7



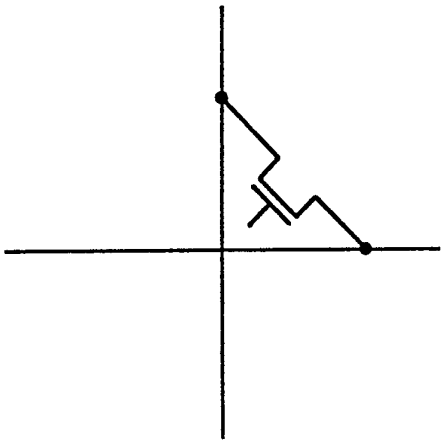
BIPOLAR FUSE

FIG. 8A



BIPOLAR FUSE

FIG. 8B



CMOS PASS GATE

FIG. 8C

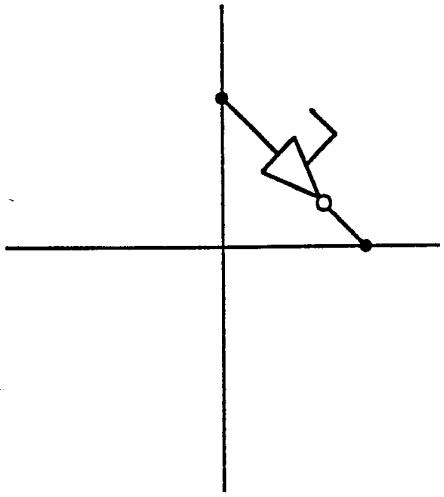


FIG. 8D

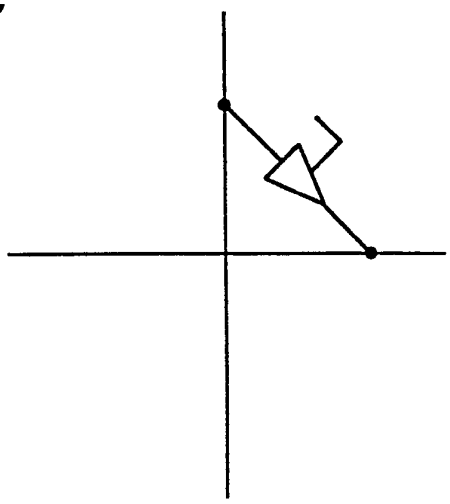


FIG. 8E

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/03575

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H03K 19/23
US CL :307/465.1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 307/465,482.1,303,303.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A, 4,910,508 (Yamazaki) 20 March 1990 see abstract and lines 50-64 of column 1.	1
A	US,A, 4,965,472 (Anderson) 23 October 1990.	
A P	US,A, 5,015,884 (Agrawal et al.) 14 May 1991.	
A	US,A, 4,717,844 (Shima et al.) 05 January 1988.	
A	US,A, 4,992,680 (Benedetti) 12 February 1991.	

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 18 AUGUST 1992	Date of mailing of the international search report 07 OCT 1992
Name and mailing address of the ISA/ Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer RICHARD ROSEEN Telephone No. (703) 309-4831

Form PCT/ISA/210 (second sheet)(July 1992)★