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(71) **Applicant (for all designated States except US):** **SPIN-NAKER SEMICONDUCTOR, INC.** [US/US]; 7550 Market Place Drive, Eden Prairie, MN 55344 (US).

(72) **Inventors; and**

(75) **Inventors/Applicants (for US only):** **SNYDER, John, P.** [US/US]; 5705 Lois Lane, Edina, MN 55439 (US). **LARSON, John, M.** [US/US]; 419 College Street, Northfield, MN 55057 (US).

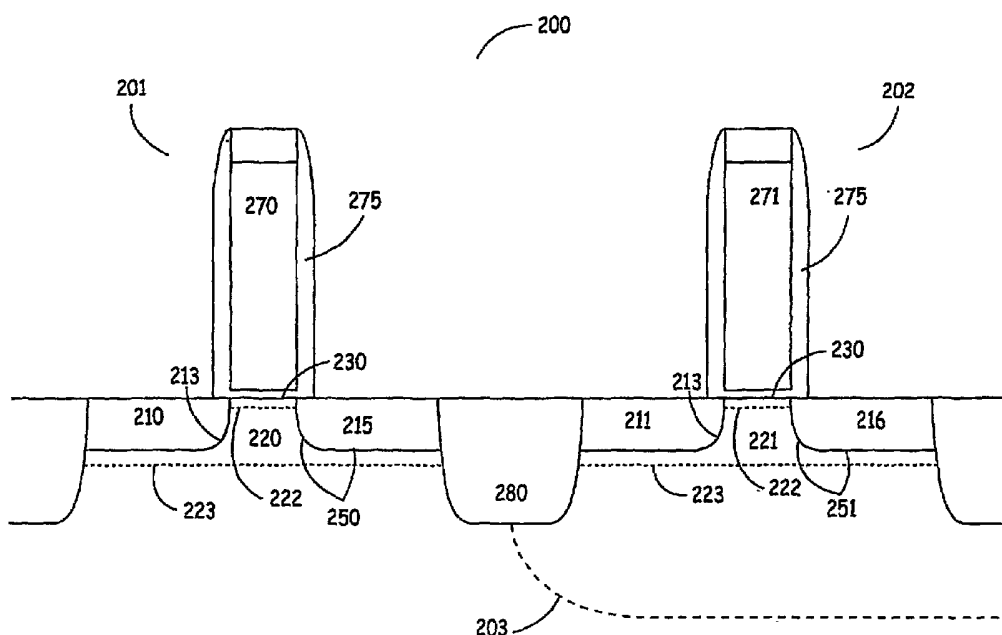
(74) **Agents:** **MIN, (Amy) Xu, S. et al.;** Dorsey & Whitney LLP, Intellectual Property Department, Suite 1500, 50 South Sixth Street, Minneapolis, MN 55402-1498 (US).

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[Continued on next page]

(54) Title: SCHOTTKY BARRIER INTEGRATED CIRCUIT



(57) Abstract: A Schottky barrier integrated circuit is disclosed, the circuit having at least one PMOS device or at least one NMOS device, at least one of the PMOS device or NMOS device having metal source-drain contacts forming Schottky barrier or Schottky-like contacts to the semiconductor substrate. The device provides a new distribution of mobile charge carriers in the bulk region of the semiconductor substrate, which improves device and circuit performance by lowering gate capacitance, improving effective carrier mobility, reducing noise, reducing gate insulator leakage, reducing hot carrier effect and improving reliability.

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B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 4 485 550 A (KOENEKE ET AL) 4 December 1984 (1984-12-04) the whole document figures 16,17	1,4-6, 8-10,12, 16,25, 26, 29-31, 33-35, 37,41,50
X	WO 03/015181 A (SPINNAKER SEMICONDUCTOR, INC) 20 February 2003 (2003-02-20) the whole document	1,16
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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Bernabé Prieto, A

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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X	----- WANG C ET AL: "Sub-40 nm PtSi Schottky source/drain metal&ndash;oxide&ndash;semicond uctor field-effect transistors" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 74, no. 8, 22 February 1999 (1999-02-22), pages 1174-1176, XP012023320 ISSN: 0003-6951 the whole document figure 2	1,16
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