**(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)**

**(54) Title: SYSTEM AND METHOD FOR A DIRECT CONVERSION MULTI-CARRIER PROCESSOR**

**(57) Abstract:** A radio communications device such as a receiver, transmitter or transceiver provides direct conversion of quadrature signals between a radio frequency signal and a plurality of resolved channels. The device provides block processing of multiple RF carriers in a wireless communication system using a direct conversion transmitter/receiver and baseband signal processing.

[0001]          SYSTEM AND METHOD FOR A DIRECT
                CONVERSION MULTI-CARRIER PROCESSOR

[0002]                   FIELD OF INVENTION

[0003]      The present invention generally relates to communication systems.
More specifically, the invention relates to communication systems using multiple
access air interfaces and direct conversion/modulation for multi-carrier
processing.

[0004]                      BACKGROUND

[0005]      A digital communication system typically transmits information or
data using a continuous frequency carrier with modulation techniques that vary
its amplitude, frequency or phase. After modulation, the signal is transmitted
over a communication medium. The communication medium may be guided or
unguided, comprising copper, optical fiber or air and is commonly referred to as
the physical communication channel.

[0006]      The information to be transmitted is input in the form of a
bitstream which is mapped onto a predetermined constellation of symbols that
defines the modulation scheme. The mapping of each bit as symbols is referred
to as modulation.

[0007]      A prior art base station is typically required to utilize multiple
carriers converging continuous frequency spectrum. A block diagram of prior
art superheterodyne receiver 11 which may be implemented in the base station is
shown in FIG. 1. An operator is typically assigned two (2) or more channels Ch1-
Ch4 (carriers), and desires to use them in each cell (frequency reuse=1). If this is
not possible due to certain constraints which result in a frequency re-use factor
that is lower, the operator has a finite number of channels, and will partition
them in contiguous sections of spectrum so that a number of adjacent channels
are used in each cell. In this case, the receiver 11 is required to process all
channels (carriers) simultaneously. This minimizes hardware cost, size, and
power consumption.

[0008]     In the past, the high demanding requirements of base station receivers could only be met with a superhetrodyne architecture. The direct conversion architecture has many inherent problems that result from downconverting the RF signal directly to baseband. These problems include self-mixing which creates DC offsets in the baseband signal; even-order distortion which converts strong interfering signals to baseband; 1/f noise which is inherent in all semiconductor devices and which is inversely proportioned to the frequency (f) and which masks the baseband signal; and spurious emissions of the LO signal which interferes with other users. Direct conversion receivers also stress the state-of-the-art capabilities of the analog baseband processing components because gain control and filtering must all be done at baseband. This requires expensive amplifiers that possess high dynamic range and a wide bandwidth.

[0009]     Conventional multi-carrier radios are based on a superheterodyne radio architecture that utilizes an intermediate frequency (IF) and direct digital sampling to block convert multiple carriers to and from baseband, as shown in Figure 1 for the receiver. Because the IF is typically located above 50 MHz, direct digital sampling requires expensive high-speed or sub-sampling data converters, such as analog-to-digital converters (ADC) and digital-to-analog converters (DACs) capable of sampling rates greater than 100 MHz and requiring very low clock jitter.

[0010]     Another disadvantage to direct digital sampling is the IF Surface Acoustic Wave (SAW) filters needed to reject interference in adjacent channels. The maximum number of carriers supported by the radio determines the bandwidth of the SAW filter. Support for a different number of carriers requires additional SAW filters. As an alternative, one IF filter can be used that covers the entire band of interest, but then additional dynamic range is needed in the ADC to handle the additional interference.

[0011]     This can be understood from the dynamic range of the received signal. When the uplink channels are all under the control of the same base station, the radio frequency (RF) carriers will be received at similar power levels,

requiring relatively less dynamic range in the ADC. However, if the IF filter bandwidth covers the entire band, uplink channels belonging to other base stations will be present at the input to the ADC. These channels can be at a very high level, thus requiring more dynamic range in the ADC.

[0012]     Referring back to Figure 1, the receiver 11 is used for digital multi-carrier wireless communication, for example a Code Division Multiple Access (CDMA) communication. As a signal is received at the antenna 15, it passes a first bandpass filter 16 and a linear amplifier 17. A second bandpass filter 18 receives the signal from the amplifier 17 and provides the signal to a mixer 19. A local oscillator 20 is connected to the mixer 19 and the mixer 19 translates the signal from RF to IF and is then filtered by a bandpass filter 21.

[0013]     The bandpass filter 21 is connected to an ADC 22 which provides its digitized output to a digital downconverter 23. A complex numerically-controlled oscillator 24 is used to control the digital downconverter 23 to translate each channel at IF to baseband. The digital downconverter 23 provides quadrature baseband signals to a bank of finite impulse response (FIR) filters 25, which perform pulse shaping and interference rejection. The outputs from the FIR filters 25 are provided to respective digital automatic gain control circuits (DAGCs) 35 which provide outputs in four (4) respective channels 45. The digital data from each channel is sent to a digital processor (not shown) for further processing, such as data demodulation and decoding. Although four (4) channels are shown as an example, those of skill in the art would realize that there could be any number of channels.

[0014]     A similar process is used on the transmission side, as shown in Figure 2, which is a block diagram showing prior art transmitter 51 using four (4) input channels Ch1 – Ch4 65. The four (4) input channels 65 are provided to respective power control circuits 75 which, in turn, provide their outputs to respective FIR filters 85. The FIR filters 85 are typically used for pulse shaping purposes. The outputs from the FIR filters 85 are provided in quadrature to a digital up converter 95, which is connected to a complex numerically-controlled

oscillator 96. The output of the digital up converter 95 is provided to a digital-to-analog (DAC) circuit 97, which supplies its analog output to a first bandpass filter 98, which in turn is provided to an IF mixer 99. The IF mixer 99 receives its local oscillator signal from an oscillator 100 and provides an output to a second bandpass filter 102. The output bandpass filter is amplified at an amplifier 103, filtered at an output bandpass filter 104 and provided for transmission via antenna 105.

[0015]　　　In these configurations (Figures 1 and 2), various conversions are performed with RF components. The manufacturing costs of these RF components is significant. Therefore, it would be advantageous to provide a circuit which avoids multiple RF conversions to the maximum extent practical. Additionally, a direct conversion design for a receiver and transmitter are desired.

[0016]　　　The major problem with prior art direct conversion receivers is the generation of DC offsets at the output of the receiver. The major sources of DC offset are local oscillator self-mixing and second order intermodulation (IP2) of the mixer. DC offsets may be quite large, leading to saturation in the ADC and other performance problems in the receiver.

[0017]　　　Solutions to the direct conversion problems have been understood for some time, but they were not practical or cost effective until recent technology developments made possible integrated solutions on monolithic RF integrated circuits (RFICs). These solutions to the problems include balanced (differential) structures that eliminate even-order distortion, SiGe semiconductor technology which exhibits low 1/f noise and excellent linearity, and harmonic mixing that eliminates self-mixing and LO spurious emissions. The move to wideband wireless technologies has also reduced the contribution of the 1/f noise to the overall noise floor of the direct conversion receiver. In addition, high-speed, high linearity amplifiers are now available to meet the analog baseband processing requirements.

[0018]     However, there are still major problems with direct conversion receivers in the generation of DC offsets at the output of the receiver. The major sources of DC offset are LO self-mixing and second order intermodulation of the mixer. DC offsets may be quite large leading to saturation of the ADC and other performance problems in the receiver. Accordingly, although there have been advances with the prior art, these prior art techniques these still fall far short of the optimum performance.

[0019]                              SUMMARY

[0020]     The present invention is a radio communication device, such as a receiver, transmitter or transceiver, that includes a direct conversion, multi-carrier processor. The multi-carrier processor frequency translates RF channels to and from a baseband using a quadrative modulator (transmitter) or demodulator (receiver). Because the analog signals are translated close to DC, conventional adjustable filters may be programmed via a bandwith control unit to support different number of channels (carriers) and channel bandwidths.

[0021]         BRIEF DESCRIPTION OF THE DRAWINGS

[0022]     Figure 1 is a block diagram of a prior art superhetrodyne with direct digital sampling multi-carrier receiver.

[0023]     Figure 2 is a block diagram of a prior art superhetrodyne with direct digital transmitter.

[0024]     Figure 3 is a block diagram of a direct conversion multi-carrier receiver made in accordance with the present invention.

[0025]     Figure 4 is a block diagram of a direct conversion multi-carrier transmitter made in accordance with the present invention.

[0026] DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027]     The present invention will be described with reference to the figures where like numerals represent like elements throughout.

[0028]    This present invention enables block processing of multiple RF carriers  in a wireless communication system using a direct conversion transmitter/receiver and baseband signal processing. Such a multi-carrier radio reduces cost by simultaneously processing multiple carriers within a single radio, rather than processing each carrier in separate radios.

[0029]    Figure 3 is a block diagram showing an exemplary embodiment of a communication receiver 130 constructed in accordance with the invention. The receiver 130 receives a plurality of communication signals $Ch_1$, $Ch_2$...$Ch_n$, each of which is sent over a carrier frequency $F_1$, $F_2$...$F_n$, respectively. These signals will be referred to collectively hereinafter as multi-carrier signal S1.

[0030]    The receiver 130 has an antenna 131, a first bandpass filter 132, a radio frequency amplifier 133 and a second bandpass filter 134. Also included are first and second mixers 141, 142, connected to a local oscillator 143, first and second low pass filters (LPFs) 145, 146, a bandwidth control circuit 147 and first and second baseband amplifiers 151, 152. The first and second mixers 141, 142 coupled with the local oscillator 143 comprise a demodulator 144.

[0031]    A first automatic gain control (AGC) circuit 153 is connected to the baseband amplifiers 151, 152, and the outputs from the baseband amplifiers 151, 152 are provided to ADC circuits 161, 162. The digitized outputs from the ADCs 161, 162 are provided to a second AGC circuit 163. The second AGC circuit 163 provides an AGC output to a DAC 164, which in turn provides an input to the first AGC circuit 153, thereby controlling the gain of baseband amplifiers 151, 152.

[0032]    The output from the second AGC circuit 163 is provided to a digital downconverter 171, which provides separate outputs to a plurality FIR filters 181-185, and in turn to a plurality DAGCs 191-195 to provide outputs to a plurality of channels $Ch_1$-$Ch_n$ 198-202. The use of the digital-analog AGC loop 163, 164, 153 reduces the dynamic range at the output and therefore reduces the requisite dynamic range of digital AGC circuits 191-194 downstream.

[0033]    The antenna 131 captures the multi-carrier signal S1 and inputs the signal S1 to bandpass filter 132, which provides band filtering to reject out-of-

band interference. After filtering, the signal is input to the low noise amplifier (LNA) 133 which sets the noise floor of the receiver 130. The output of the LNA 133 is filtered through bandpass filter (BPF) 134 to filter any intermodulation distortion produced by the LNA 133.

[0034]    The output of the LNA 133 is sent to the demodulator 144, which consists of mixers 141 and 143 and the stable local oscillator (LO) 143. The LO 143 has two outputs, one in-phase (I) and one in quadrature (Q), relative to the carrier. The frequency of the LO 143 is the center frequency of the input channels $Ch_1$-$Ch_n$, $(F_1 - F_n)/2$; where $F_1$ is the carrier frequency of the first channel $Ch_1$ and $F_n$ is the carrier frequency of the nth channel $Ch_n$. The demodulator 144 translates the desired signal from RF to baseband, centering the signal around DC.

[0035]    The I and Q signals are sent to LPFs 145 and 146, which provide interference rejection in order to minimize the dynamic range of the downstream baseband processing elements 151-194. Since the analog signals are translated close to DC, conventional adjustable filters 145 and 146 may be programmed via bandwith control 147 to support different number of channels and channel bandwidths.

[0036]    ADCs 161, 162 are pair of conventional low cost ADCs which digitize the I/Q signals from the demodulator 144. The individual channels $Ch_1$-$Ch_n$ are down-converted to baseband by the DDC 171.

[0037]    Channel filtering and pulse shaping is applied to each channel $Ch_1$-$Ch_n$ by the FIR filters 181-185.

[0038]    The AGC process is performed in two steps. The first step is performed in the first and second AGC circuits 151, 163 to adjust the gain of the baseband amplifiers 151, 152 to maintain the signal within the dynamic range of the ADCs 161, 162. The second step of the AGC process is performed digitally in the DAGC block 191-195 and is used to reduce the bitwidth of the I/Q signals to the minimum required for each channel 198-202.

[0039]    As shown in Figure 3, the receiver 130 operates as a multi-carrier direct conversion receiver. The frequency block containing the multiple RF channels is thereby down-converted directly to baseband as a block of frequencies.

[0040]    Figure 4 is a block diagram showing an exemplary embodiment of a direct conversion communication transmitter 230 constructed in accordance with the invention. The individual channels (Ch$_1$-Ch$_n$) 231-234 are first sent through FIR filters 241 -244 and are digitally upconverted by a digital upconverter DUC 247. This provides a digital baseband signal, which is used to drive a pair of low cost DACs 251, 252. The DUC 247 converts an input signal into I/Q signal components by shifting the center frequency from zero to +/- one half of the bandwidth.

[0041]    The output of the DUC 247, comprises two digital outputs which are separated in quadrature. These I/Q outputs are input to the DACs 251 and 252, which convert the digital signals to analog. The analog outputs from DACs 251, 252 are provided to LPFs 253, 254, the bandwidth of which are controlled by bandwidth control circuit 255. The LPFs 253, 254 filter the analog signals and provide their respective filtered outputs to a modulator 260, comprising two mixers 261, 262, the LO 263 and the summer 264. The mixers 261, 262 are controlled by the LO 263 and provide mixed outputs to the summer 264. The modulator 260 provides an output to the bandpass filter 265 and, in turn, to a first RF amplifier 266. The RF amplifier 266 is controlled by gain control circuit 267 and provides an output to bandpass filter 268 and RF power amplifier 269 which amplifies the signal for transmission, via antenna 270.

[0042]    As can be clearly seen in Figures 3 and 4, the direct conversion multi-carrier processor in accordance with the present invention avoids the disadvantages of the superheterodyne radio by eliminating the IF stage. This reduces cost in the radio and allows the data converters to operate at baseband at a lower clock rate, which further reduces cost. Adjustable bandwidth filters are readily realizable at baseband, allowing flexible support for variable carrier

spacing and the number of carriers to be processed in the radio. This also reduces the dynamic range required in the ADC because only the desired carriers are present at the ADC, again reducing cost.

[0043]     The present invention is applicable to wireless communication systems, including wireless local loop, wireless LAN applications, and cellular systems such as WCDMA (both UTRATDD and UTRAFDD), TDSCDMA, CDMA2000, 3xRT, and OFDMA systems.

[0044]     While the present invention has been described in terms of the preferred embodiment, other variations, which are within the scope of the invention as outlined in the claims below will be apparent to those skilled in the art.

CLAIMS

What is claimed:

1.      A multi-carrier direct conversion receiver for receiving and processing a multi-carrier radio frequency (RF) signal, comprising:

an antenna for receiving the multi-carrier RF signal;

an RF amplifier which provides an interface between the antenna and a demodulator, the RF amplifier for amplifying the received multi-carrier RF signal;

the demodulator coupled to the RF amplifier for converting the multi-carrier RF signal into in-phase (I) and quadrature (Q) baseband signals;

a pair of baseband stages, each stage comprising a low pass filter and amplifier, and each for processing one of the I and Q baseband signals;

a pair of digital to analog circuits, each in communication with one of the converters for converting one of the I and Q baseband signals to a digital I and Q signal, respectively; and

a direct conversion circuit, connected to the digital to analog circuits, for converting the digital I and Q signals into a plurality of channels.


2.      The receiver of claim 1, further comprising a plurality of finite impulse response (FIR) filters, one for each of the plurality of channels, for filtering one of said plurality of channels.


3.      The receiver of claim 1, wherein the bandwidth of each of the low pass filters is adjustable.


4.      The receiver of claim 3, further comprising a bandwidth control circuit for controlling the bandwidth of the low pass filters.


5.      A multi-carrier direct modulation transmitter for processing and transmitting a plurality of channels, the transmitter comprising:


-10-

a digital up converter, for receiving said plurality of channels and outputting a pair of digital in-phase (I) and quadrature (Q) signals;

a pair of digital-to-analog converters, each for receiving one of said digital I and Q signals and outputting a respective I and Q analog signal at a baseband frequency;

a modulator for receiving said baseband digital I and Q signals and for providing a single radio frequency (RF) signal; and
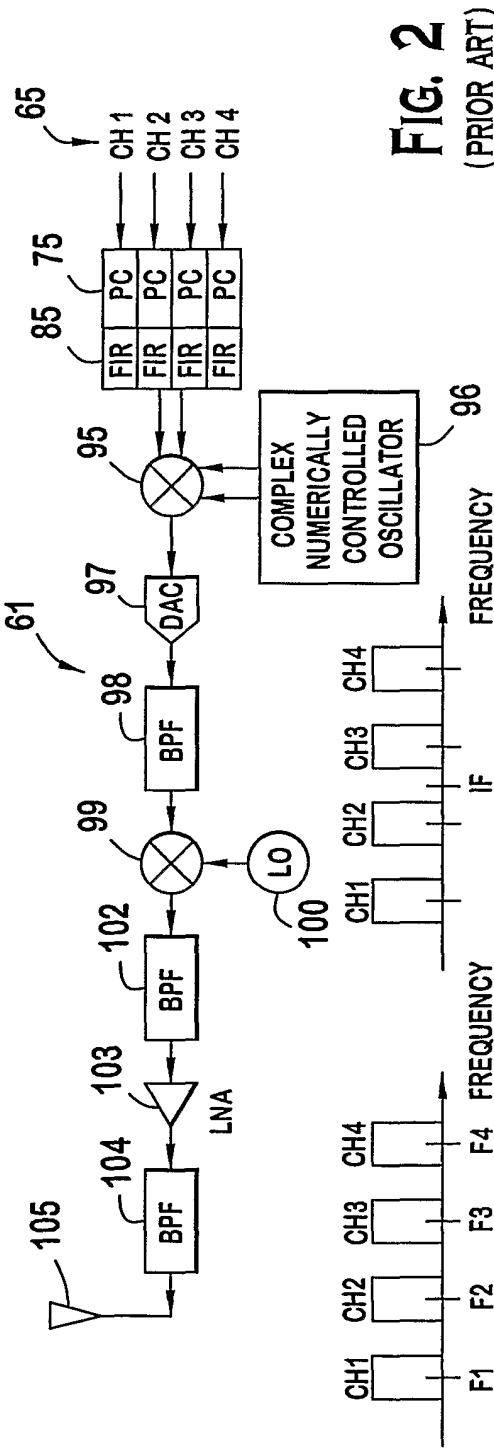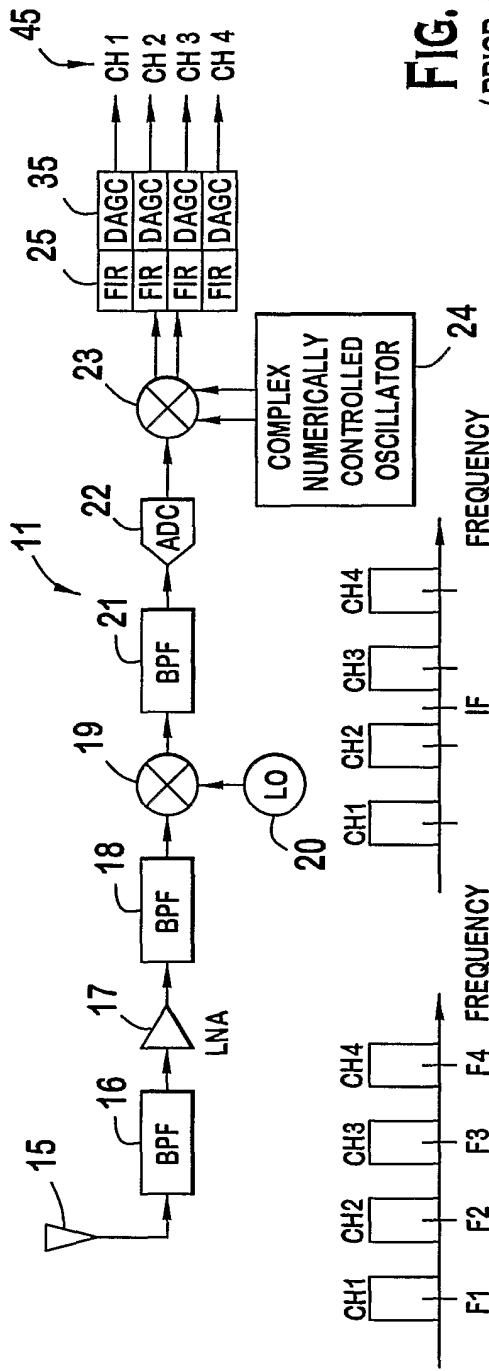
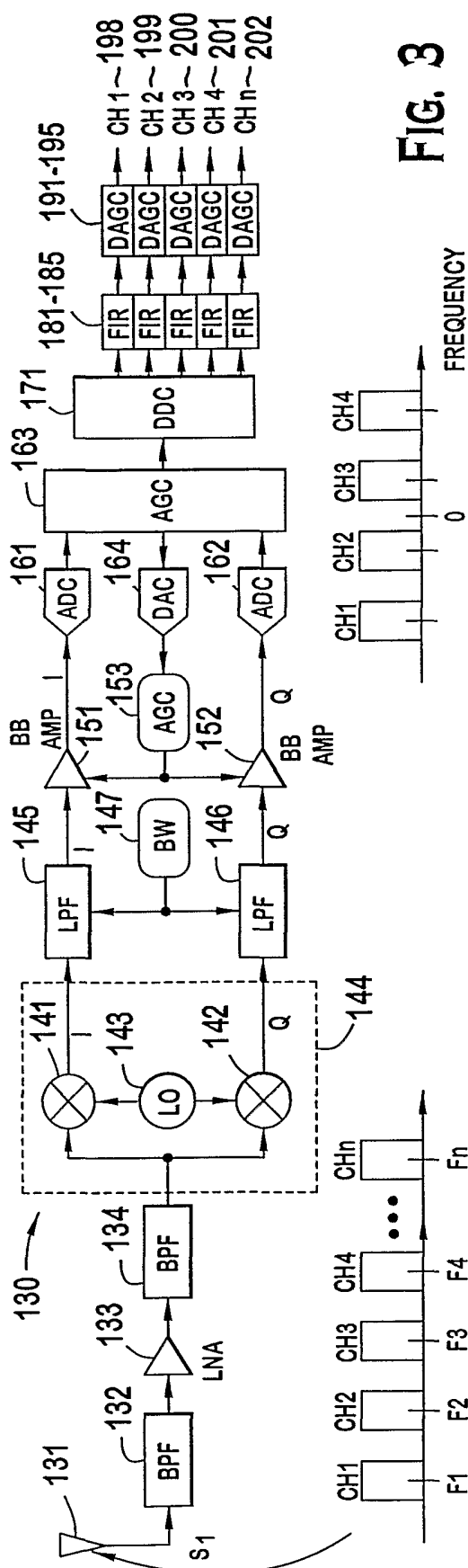a transmitter for transmitting said RF signal.

6.    The transmitter of claim 5, further comprising an RF amplifier, for amplifying said RF signal prior to transmission.

7.    The transmitter of claim 6, further comprising a pair of low pass filters, each of which is coupled to a respective one of said digital-to-analog converters, for filtering one of said analog I and Q signals.

8.    The transmitter of claim 7, further including a bandwidth control circuit for controlling the frequency response of the transmitter by controlling the bandwidth of said low pass filters.

9.    The transmitter of claim 8, further comprising a plurality of finite impulse response (FIR) filters, each FIR filter corresponding to one of the plurality of channels, each FIR filter for receiving one of said plurality of channels and for providing a filtered output to the digital up converter.
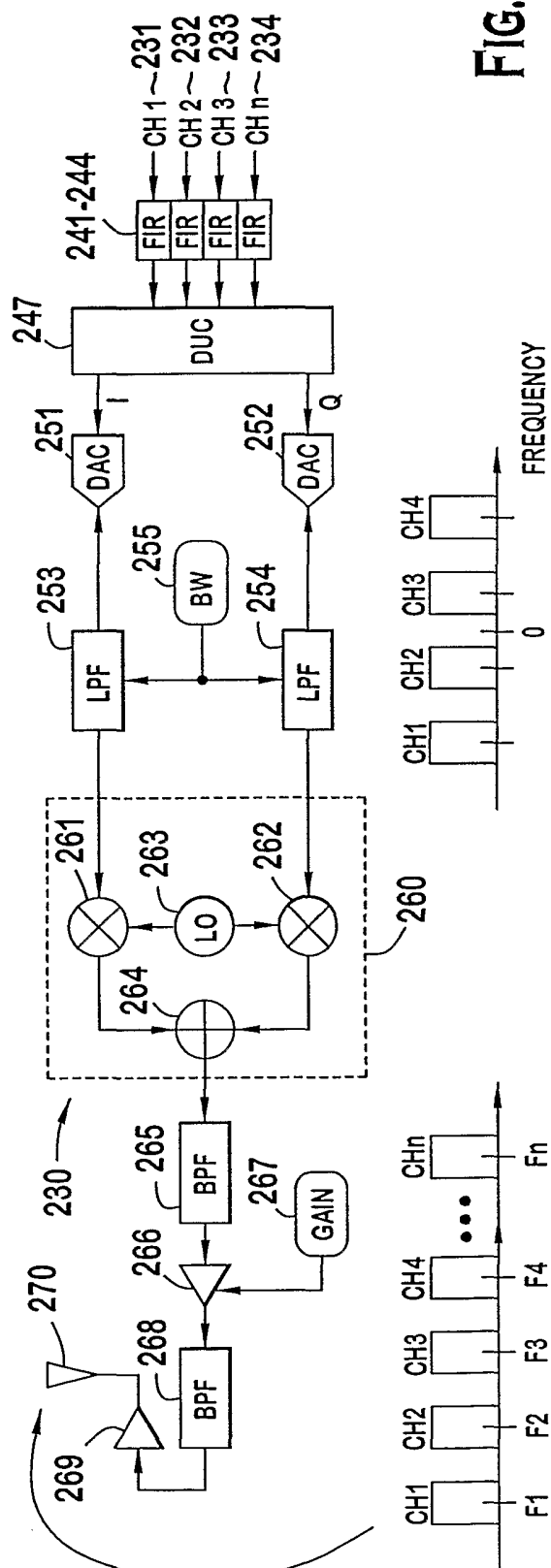
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FIG. 1
(PRIOR ART)



FIG. 2
(PRIOR ART)

2/2

FIG. 3

FIG. 4