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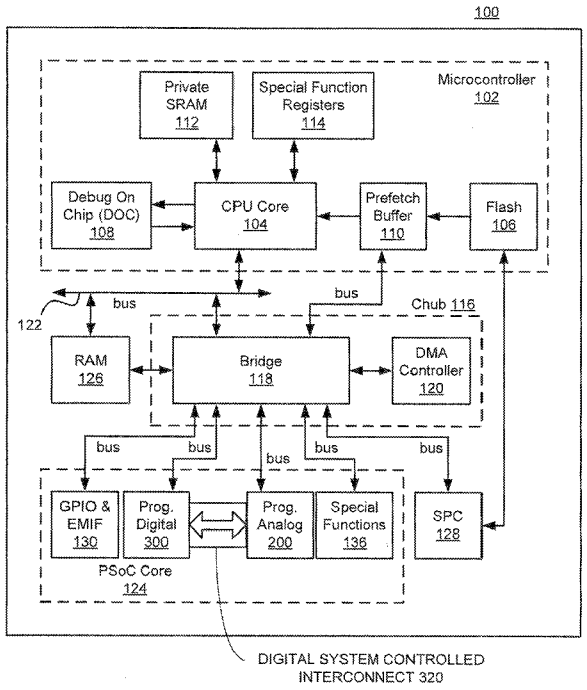
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(54) Title: AUTONOMOUS CONTROL IN A PROGRAMMABLE SYSTEM

(57) Abstract: A programmable system includes a programmable analog system that is reconfigurable to perform various analog operations, and includes a programmable digital system that is reconfigurable to perform various digital operations. The programmable system also includes a microcontroller capable of reconfiguring and controlling the programmable analog system and the programmable digital system. The programmable digital system is configured to control the programmable analog system autonomously of the microcontroller.

Figure 1



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AUTONOMOUS CONTROL IN A PROGRAMMABLE SYSTEM

RELATED APPLICATION

This patent application claims benefit of and priority to U.S. Provisional Patent Application No. 61/175,086, filed May 4, 2009, which is incorporated by reference herein.

TECHNICAL FIELD

This disclosure relates generally to electronic circuits, and, more particularly, to autonomous control in a programmable system.

BACKGROUND

Many electronic systems include circuits that provide fixed functionality. For instance, a signal processing device can include fixed function circuits, such as signal filters and analog-to-digital converters, to perform signal processing operations. By arranging these fixed-function circuits in particular configurations, electronic systems can be built to perform specific tasks.

Programmable electronic systems include more generalized circuits or blocks, such as digital and analog programmable blocks, that can be configured to implement a large number of peripherals. The digital blocks can include programmable circuitry configured to provide various digital functions. The analog blocks can be used for development of analog elements, such as analog filters, comparators, inverting amplifiers, as well as analog-to-digital and digital-to-analog converters. The programmable electronic system can combine the analog and digital blocks to form a wide variety of functional modules, which implement mixed-signal applications.

The programmable electronic systems include a microcontroller and firmware to control applications performed by the programmable analog blocks and programmable digital blocks. For instance, when the programmable electronic system implements a mixed-signal

application, such as an analog-to-digital converter, the microcontroller and firmware can configure or reconfigure the programmable analog blocks and programmable digital blocks into an analog-to-digital converter configuration, control the routing of analog data (to be converted) to the programmable analog blocks, control the output of digital (converted) data from the programmable digital blocks, and possibly receive status, state, and mode signaling from the programmable analog blocks and programmable digital blocks during performance of the analog-to-digital conversion.

SUMMARY

This patent application discloses a system that includes a programmable analog system that is reconfigurable to perform various analog operations, and includes a programmable digital system that is reconfigurable to perform various digital operations. The system also includes a microcontroller capable of reconfiguring and controlling the programmable analog system and the programmable digital system. The programmable digital system is configured to control the programmable analog system autonomously of the microcontroller.

In some embodiments, a method includes receiving configuration data that prompts a digital system to implement a digital control device and sending, with the digital control device, one or more commands to an analog system over an interconnect controlled by the digital control device. The one or more commands are configured to prompt a reconfiguration of the analog system. The method further includes controlling, with the digital control device, analog data operations performed by the reconfigured analog system independently of a microcontroller.

In some embodiments, a system includes a programmable analog system including one or more analog circuits that are reconfigurable to perform analog data operations. The

system further includes a programmable digital system including one or more universal digital block devices that are reconfigurable to perform digital data operations. At least one of the universal digital block devices is reconfigured to implement a digital control device that controls the programmable analog system.

DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates an embodiment of a core architecture of a Programmable System-on-Chip (PSoC™), such as that used in the PSoC3™ family of products offered by Cypress Semiconductor Corporation (San Jose, California).

Figure 2 is a block diagram example of the analog system shown in Figure 1.

Figure 3 is a block diagram example of the digital system shown in Figure 1.

Figure 4 is a block diagram example of the universal digital block shown in Figure 3.

Figure 5 is another block diagram example of a programmable system with autonomous digital system control according to embodiments of the invention.

Figure 6 is an example operational flowchart of the programmable system on a chip according to embodiments of the invention.

DETAILED DESCRIPTION

A Programmable System-on-Chip (PSoC™), such as that used in the PSoC™ family of products offered by Cypress Semiconductor Corporation (San Jose, California), or other electronic system can include a core processing device and programmable analog and digital components that can work in conjunction to perform various data operations. The programmable digital components can be configured into a digital control device, which can control the operations performed by the programmable analog and digital components autonomously of the core processing device. Embodiments are shown and described below in greater detail.

Figure 1 illustrates an embodiment of a core architecture 100 of a Programmable System-on-Chip (PSoC™), such as that used in the PSoC3™ family of products offered by Cypress Semiconductor Corporation (San Jose, California). Referring to Figure 1, in one embodiment, the core architecture 100 includes a microcontroller 102. The microcontroller 102 includes a CPU (central processing unit) core 104, flash program storage 106, DOC (debug on chip) 108, a prefetch buffer 110, a private SRAM (static random access memory) 112, and special functions registers 114. In an embodiment, the DOC 108, prefetch buffer 110, private SRAM 112, and special function registers 114 are coupled to the CPU core 104, while the flash program storage 106 is coupled to the prefetch buffer 110.

The core architecture 100 may also include a CHub (core hub) 116, including a bridge 118 and a DMA (direct memory access) controller 120, that is coupled to the microcontroller 102 via bus 122. The Chub 116 may provide the primary data and control interface between the microcontroller 102 and its peripherals and memory, and a programmable core 124. The DMA controller 120 may be programmed to transfer data between system elements without burdening the CPU core 104. In various embodiments, each of these subcomponents of the microcontroller 102 and CHub 116 may be different with each choice or type of CPU core 104. The Chub 116 may also be coupled to shared SRAM 126 and an SPC (system performance controller) 128. The private SRAM 112 is independent of the shared SRAM 126 that is accessed by the microcontroller 102 through the bridge 118. The CPU core 104 accesses the private SRAM 112 without going through the bridge 118, thus allowing local register and RAM accesses to occur simultaneously with DMA access to shared SRAM 126. Although labeled here as SRAM, these memory modules may be any suitable type of a wide variety of (volatile or non-volatile) memory or data storage modules in various other embodiments.

In various embodiments, the programmable core 124 may include various combinations of subcomponents (not shown), including, but not limited to, a digital logic array, digital peripherals, analog processing channels, global routing analog peripherals, DMA controller(s), SRAM and other appropriate types of data storage, IO ports, and other suitable types of subcomponents. In one embodiment, the programmable core 124 includes a GPIO (general purpose IO) and EMIF (extended memory interface) block 130 to provide a mechanism to extend the external off-chip access of the microcontroller 102, a programmable digital system 300, a programmable analog system 200, and a special functions block 136, each configured to implement one or more of the subcomponent functions. In various embodiments, the special functions block 136 may include dedicated (non-programmable) functional blocks and/or include one or more interfaces to dedicated functional blocks, such as USB, a crystal oscillator drive, JTAG, and the like. The system resources 130 can also include a memory device (not shown) to store configuration data.

The programmable digital system 300 may include a digital logic array including an array of digital logic blocks and associated routing. In one embodiment, the digital block architecture is comprised of UDBs (universal digital blocks). For example, each UDB may include an ALU together with CPLD functionality.

In various embodiments, one or more UDBs of the programmable digital system 300 may be configured to perform various digital functions, including, but not limited to, one or more of the following functions: a basic I2C slave; an I2C master; a SPI master or slave; a multi-wire (e.g., 3-wire) SPI master or slave (e.g., MISO/MOSI multiplexed on a single pin); timers and counters (e.g., a pair of 8-bit timers or counters, one 16 bit timer or counter, one 8-bit capture timer, or the like); PWMs (e.g., a pair of 8-bit PWMs, one 16-bit PWM, one 8-bit deadband PWM, or the like), a level sensitive I/O interrupt generator; a quadrature encoder, a

UART (e.g., half-duplex); delay lines; and any other suitable type of digital function or combination of digital functions which can be implemented in a plurality of UDBs.

In other embodiments, additional functions may be implemented using a group of two or more UDBs. Merely for purposes of illustration and not limitation, the following functions can be implemented using multiple UDBs: an I2C slave that supports hardware address detection and the ability to handle a complete transaction without CPU core (e.g., CPU core 104) intervention and to help prevent the force clock stretching on any bit in the data stream; an I2C multi-master which may include a slave option in a single block; an arbitrary length PRS or CRC (up to 32 bits); SDIO; SGPIO; a digital correlator (e.g., having up to 32 bits with 4x over-sampling and supporting a configurable threshold); a LINbus interface; a delta-sigma modulator (e.g., for class D audio DAC having a differential output pair); an I2S (stereo); an LCD drive control (e.g., UDBs may be used to implement timing control of the LCD drive blocks and provide display RAM addressing); full-duplex UART (e.g., 7-, 8- or 9-bit with 1 or 2 stop bits and parity, and RTS/CTS support), an IRDA (transmit or receive); capture timer (e.g., 16-bit or the like); deadband PWM (e.g., 16-bit or the like); an SMbus (including formatting of SMbus packets with CRC in software); a brushless motor drive (e.g., to support 6/12 step commutation); auto BAUD rate detection and generation (e.g., automatically determine BAUD rate for standard rates from 1200 to 102200 BAUD and after detection to generate required clock to generate BAUD rate); and any other suitable type of digital function or combination of digital functions which can be implemented in a plurality of UDBs.

As will be described below in greater detail, the digital system 300 can also be configured to implement a digital control device, which can control the analog system 200 and the digital system 300 autonomously of the microcontroller 102. The configuration data

can be any combination of commands and/or data that, when provided to the digital system 300, causes the digital system 300 to implement a digital control device that is capable of controlling the operations in the analog system 200 and the digital system 300 independently of the microcontroller 102.

The programmable analog system 200 may include analog resources including, but not limited to, comparators, mixers, PGAs (programmable gain amplifiers), TIAs (trans-impedance amplifiers), ADCs (analog-to-digital converters), DACs (digital-to-analog converters), voltage references, current sources, sample and hold circuits, and any other suitable type of analog resources. The programmable analog system 200 may support various analog functions including, but not limited to, analog routing, LCD drive IO support, capacitive sensing, voltage measurement, motor control, current to voltage conversion, voltage to frequency conversion, differential amplification, light measurement, inductive position monitoring, filtering, voice coil driving, magnetic card reading, acoustic doppler measurement, echo-ranging, modem transmission and receive encoding, or any other suitable type of analog function.

The analog system 200 and the digital system 300 can be reconfigured and their operation controlled responsive to commands and/or data from the microcontroller 102, the analog system 200, and/or the digital system 300, e.g., when the digital system 300 is configured into the digital control device. The microcontroller 102 can provide commands to the analog and digital systems 200 and 300 via one or more buses, which prompts the analog and digital systems 200 and 300 to configure their reconfigurable analog circuits and the programmable digital circuits, respectively. The microcontroller 102 can subsequently control operations performed by the configured components of the analog and digital systems 200 and 300 and provide the analog and digital systems 200 and 300 data to be processed.

When the digital system 300 is configured into the digital control device, the digital system 300 can control the operation of the analog system 200 and the digital system 300 autonomously of the microcontroller 102. Thus, the analog system 200 and the digital system 300 can be reconfigured and their operations controlled responsive to commands and/or data from the digital system 300 configured as the digital control device. In some embodiments, the digital control device can also control operations of the special functions block 136. By configuring the digital system 300 into the digital control device, the digital system 300 can configure and control the analog and digital systems 200 and 300, which reduces the processing load of the microcontroller 102.

Once configured by the microcontroller 102, the digital control device, or in response to commands from the memory device, the analog system 200 can provide feedback and/or control signals to the digital system 300, which can direct (re)configuration of the digital system 300 or prompt the digital system 300 to change an operational state. By enabling the analog system 200 to control the configuration of at least part of the digital system 300 or to control the operational states of the digital system 300, the analog system 200 and/or the digital system 300 configured as a digital control device can reduce the processing load of the microcontroller 102.

The core architecture 100 includes a digital system controlled interconnect 320 coupled between the digital system 300 and the analog system 200, which allows the digital system 300 the ability to bi-directionally communicate with the analog system 200. The digital control device can utilize the digital system controlled interconnect 320 to pass commands and data to the analog system 200, and receive operational feedback and possibly data from the analog system 200. Since the digital control device and the digital system controlled interconnect 320 form a closed-loop between the digital system 300 and the analog

system 200, the digital system 300 has the ability to direct the (re)configuration of the analog system 200 and control operations performed by the analog system 200. The digital system controlled interconnect 320 allows the digital control device to react in real-time, for example, within two clock cycles, to status indications from the analog system 200, as opposed to an interrupt-based alert and response scheme implemented by the microcontroller 102.

In some embodiments, the analog system 200 can control the digital system 300 through the digital system controlled interconnect 320. For example, the analog system 200 can prompt the digital system 300 to change its operation—vary a count range, step size, or sensitivity to various data inputs, or direct a change of states when the digital system 300 implements a state machine.

The analog system 200 can also reconfigure the digital system 300, for example, by providing commands or control signals to the digital system 300. These commands or control signals can be similar to those the microcontroller 102 can provide to the digital system 300 during (re)configuration operations. Since the analog system 200 and digital system 300 can be enabled to reconfigure each other over the digital system controlled interconnect 320, the analog system 200 and the digital system 300 can alleviate the load from the microcontroller 102.

The digital system controlled interconnect 320 can include control connections, status connections, and data connections between the digital system 300 and the analog system 200. The digital system 300 can utilize the control connections to provide the analog system 200 with clocking information, a start trigger, dynamic mode controls, and dynamic routing controls, etc. The analog system 200 can utilize the status connections to provide the digital system 300 with various signals corresponding to the performance of operations by the analog system 200. For instance, the analog system 200 can provide process complete

signals, comparator signals, etc, to the digital system 300 during the performance of various applications. The digital system 300 can utilize the data connections to exchange data with the analog system 200. For instance, in a digital-to-analog conversion application, the digital system 300 can provide digital data to the analog system 200 for conversion. When in an analog-to-digital conversion application, the analog system 200 can provide the output of the analog-to-digital conversion back to the digital system 300.

The digital system 300 can be configured into the digital control device responsive to configuration data stored in the memory device of the special functions block 136. This configuration data can be provided to the digital system 300 through one or more direct memory access (DMA) operations with the DMA controller 120, for example, via one or more buses. The use of the DMA controller 120 to provide the configuration data to the digital system 300 can allow the digital system 300 to begin controlling the configuration and operation of the analog system 200 and the digital system 300 upon boot of the core architecture 100 before the microcontroller 102 is initialized and available to control the analog system 200 and the digital system 300. In some embodiments, the digital system 300 can be configured into the digital control device based on configuration data received from the microcontroller 102, for example, via one or more buses. Embodiments of the analog system 200, digital system 300, and the digital system controlled interconnect 320 will be described below in greater detail.

Figure 2 is a block diagram example of the analog system 200 shown in Figure 1. Referring to Figure 2, the analog system 200 includes an analog block array 210 having a plurality of reconfigurable analog circuits (not shown) that can be utilized individually or be variously combined to implement analog or mixed-signal applications. The analog block array 210 includes multiple programmable analog blocks 220 that each can be (re)configured

by the digital system 300 (or microcontroller 102) to implement discrete-time functions or continuous-time functions.

The analog system 200 includes routing interfaces 205 to connect the Chub 116 and/or microcontroller 102, the digital system 300, and other fixed function peripherals to the analog block array 210. The analog block array 210 can include a programmable interconnect matrix 212 and 214 that connects together different programmable analog blocks 220. The routing interfaces 205 can be an extension of the interconnect matrix 212 and 214, for example, at the top and bottom of the analog block array 210. The routing interfaces 205 can couple to various buses and the digital system controlled interconnect 320.

The interconnect matrix 212 and 214 and the routing interfaces 205 can combine to provide data, voltages, configuration signaling, etc, to the programmable analog blocks 220 from various on-chip devices and possibly from external resources via I/O ports 202A-202D. The interconnect matrix 212 and 214 can also allow the programmable analog blocks 220 to send output data or control/status information to other on-chip devices via one or more buses or digital system controlled interconnect 320 or to external devices via I/O ports 202A-202D, for example, to the microcontroller 102 or the digital system 300.

Figure 3 is a block diagram example of the digital system 300 shown in Figure 1. Referring to Figure 3, the digital system 300, in some embodiments, includes a universal digital block (UDB) array 310 having a programmable interconnect matrix 330 that connects together different UDBs 400. The individual UDBs 400 each include a collection of uncommitted logic in the form of Programmable Logic Devices (PLDs) and structural dedicated logic elements that form a datapath shown in more detail in below.

The UDB array 310 can be arranged into UDB pairs 322 that are connected together through the interconnect matrix 330. The UDB pairs 322 each include two UDBs 400 that

can be tightly coupled to a shared horizontal routing channel 332. The UDB pairs 322 can also be programmably connected to the horizontal routing channels 332 of other UDB pairs 322 either in the same horizontal row or in different rows through vertical routing channels 334. The horizontal and vertical routing channels and other switching elements are all collectively referred to as the interconnect matrix 330.

A digital routing interface 305 connects the microcontroller 102, the analog system 200, and other system resources to the UDB array 310. The digital routing interface 305 can be an extension of the interconnect matrix 330 at the top and bottom of the UDB array 310. The digital routing interface 305 can couple to various buses and the digital system controlled interconnect 320.

Figure 4 is a block diagram example of the universal digital block 400 shown in Figure 3. Referring to Figure 4, the major blocks include a pair of Programmable Logic Devices (PLDs) 422 and 424. The PLDs 422 and 424 can take inputs from the system bus 106 or the digital system controlled interconnect 320 and can form registered or combinational sum-of-products logic to implement state machines, control for datapath operations, conditioning inputs and driving outputs. The PLD blocks 422 and 424 can implement state machines, perform input or output data conditioning, and create look-up tables. The PLDs 422 and 424 can also be configured to perform arithmetic functions, sequence datapath 410, and generate status information.

The datapath block 410 contains highly structured dedicated logic that implements a dynamically programmable arithmetic logic unit (ALU), comparators, and condition generation. A status and control block 404 allows the microcontroller firmware or the digital system 300 (as the digital control device) to interact and synchronize with the UDB 400 by writing to control inputs and reading status outputs. In some embodiments, the digital system

300 can access the status and control block 404 of the UDB 400 through the digital system controlled interconnect 320.

A clock and reset control block 402 can provide global clock selection, enabling, and reset selection for the UDB 400. The clock and reset block 402 can select a clock for each of the PLD blocks 422 and 424, the datapath block 410, and status and control block 404 from available global system clocks, a bus clock, or signaling from the digital system 300 through the digital system controlled interconnect 320. The clock and reset block 402 can also supply dynamic and firmware resets to the UDBs 400.

A routing channel connects to UDB I/O through a programmable switch matrix and provides connections between the different elements of the UDBs 400 in Figure 2. An interface to the bus or the digital system controlled interconnect 320 can map registers and memory in the UDBs 400 into a system address space and are accessible by the microcontroller 102 or the digital system 300 through the digital system controlled interconnect 320.

The PLDs 422 and 424 and the datapath 410 have chaining signals 412 and 414, respectively, which enable neighboring UDBs 400 to be linked to create higher precision functions. The PLD carry chain signals 412 are routed from the previous adjacent UDB 400 in the chain, and routed through each macrocell in both of the PLDs 422 and 424. The carry out can then be routed to the next UDB 400 in the chain. A similar connectivity can be provided for the set of conditional signals generated by the datapath chain 414 between datapaths 410 in adjacent UDBs 400.

Figure 5 is another block diagram example of a programmable system 500 with autonomous digital system control according to embodiments of the invention. Referring to Figure 5, the programmable system 500 includes a digital system 300 with one or more

programmable digital blocks having been configured to implement a digital control device 510. The digital system 300 can be configured to implement the digital control device 510 based on configuration data provided to the digital system 300 via a DMA controller 120. By using a DMA controller 120 to provide the configuration data to the digital system 300, the programmable system 500 can configure the digital system 300 autonomously of the microcontroller 102. Although this autonomous configuration of the digital system 300 can reduce the consumption of processing resources and also allow the digital system 300 begin performing operations more quickly after a system boot, as the digital system 300 does not have to wait for firmware initiation before being configured, in some embodiments, the microcontroller 102 can provide the configuration data to the digital system 300.

The digital control device 510 can configure the analog system 200 and the digital system 300 to perform various analog, digital, and mixed-signal applications, including an analog-to-digital conversion as shown in Figure 5, and control the analog system 200 and the digital system 300 during the performance of the application. In an analog-to-digital converter configuration, a plurality of analog blocks 220-1 to 220-N in the analog system 200 are configured by the digital control device 510 into switch capacitance modulators, and a plurality of digital blocks 520-1 to 520-M in the digital system are configured into digital integrators. In some embodiments, the switch capacitance modulators can each include an operational amplifier 221, a comparator 220, and a capacitance network (not shown) to perform the modulations for the analog-to-digital conversion.

The digital control device 510 can direct the configuration of the analog blocks 220-1 to 220-N into switch capacitance modulators by passing commands and/or data to the analog system 200 over the analog programmable interconnect 530 or the digital programmable interconnect 540. The analog programmable interconnect 530 can be reconfigured by the

digital control device 510 to route analog data and signals from I/O ports 202 or between the analog blocks 220. The reconfigurability of the analog programmable interconnect 530 allows the digital control device 510, and in some embodiments, the microcontroller 102, the ability to configure the routing of the analog programmable interconnect 530 based on the particular application performed by the programmable system 500. The digital programmable interconnect 540 can route digital data, commands, and signals between the digital system 300 and the analog system 200. In some embodiments, the analog programmable interconnect 530 and the digital programmable interconnect 540 comprise the digital system controlled interconnect 320 shown in Figure 1.

Once the analog system 200 and digital system 300 are configured to perform analog-to-digital conversion, the digital control device 510 can direct analog data be provided to the analog system 200, for example, from one or more I/O ports 202 via the analog programmable interconnect 530. The switch capacitance modulators can be configured to modulate the analog data and provide the modulated data to the digital integrators 520-1 to 520-M over the digital programmable interconnect 540.

In some embodiments, the digital control device 510 can direct analog data to be provided to an input terminal of the operational amplifier 221 and/or the capacitor network in the switch capacitance modulators. The operational amplifier 221 can generate an output, which can be supplied to the analog programmable interconnect 530 for use by the digital control device 510 and fed to the comparator 222 for comparison against a known reference voltage. Based on the operation of the switch capacitance modulators, the digital control device 510 can provide feedback to the operational amplifier 221 of the switch capacitance modulators, adjusting the generation of the output from the analog data. This feedback can be provided in real-time by the digital control device 510 in response to status signaling that

the digital control device 510 receives from the switch capacitance modulators over either the analog programmable interconnect 530 or the digital programmable interconnect 540.

The digital integrators 520-1 to 520-M can receive and integrate digital data, such as the output of the comparator 222, over the digital programmable interconnect 540. The digital control device 510 can control the digital integrators 520-1 to 520-M and other digital blocks in the digital system 300 to provide a digital data output to a selected output, such as an I/O port 202 coupled to the digital programmable interconnect 540. In some embodiments, the analog system 200 can provide commands or control signals to the digital system 300 through either the analog programmable interconnect 530 or the digital programmable interconnect 540. These commands or control signals can direct (re)configuration of the digital system 300 or prompt the digital system 300 to change an operational state. For example, the analog system 200 can provide control signals to the digital system 300 that direct the digital system 300 to configure into the series of digital integrators 520-1 to 520-M. In some embodiments, the control signals provided by the analog system 200 can direct the digital system 300 to alter its operational state while in its current configuration.

Figure 6 is an example operational flowchart of the programmable system on a chip according to embodiments of the invention. Referring to Figure 6, in a block 610, the digital system 300 can be configured to receive configuration data 137 that prompts the digital system 300 to implement a digital control device 510. The digital system 300 can be configured to implement the digital control device 510 based on configuration data provided to the digital system 300 via the DMA controller 120 or by the microcontroller 102. When receiving the configuration data from the DMA controller 120 after a system boot of the programmable system, the digital system 300 can be configured autonomously of the

microcontroller 102 and before firmware corresponding to the microcontroller 102 is fully initiated.

In block 620 and 630, the digital control device 510 can be configured to send one or more commands that are configured to prompt reconfiguration of the analog system 200 and the digital system 300, respectively. Based on the application that the digital control device 510 intends to initiate, i.e., analog application, digital application, or mixed-signal application, the digital control device 510 can send commands to the analog system 200 and/or the digital system 300. For instance, when implementing a mixed-signal application, the digital control device 510 can send commands to both the analog system 200 and the digital system 300. When, however, implementing an analog application, the digital control device 510 can send commands to the analog system 200 without sending the commands to the digital system 300, as the digital system 300 may not be utilized to implement to the analog application.

In a block 640, the digital control device 510 can be configured to control data operations performed by the (re)configured analog system 200 and/or digital system 300 independently of the microcontroller 102. The digital control device 510 can utilize an interconnect coupled between the analog system 200 and digital system 300 to control the operations performed by the analog system 200 and digital system 300. The interconnect can be controlled by the digital system 300 and be utilized by the digital control device 510 to provide data and commands to the analog system 200 and to receive status signaling and data from the analog system 200. During the performance of some applications, the digital control device 510 can react to the status signaling provided by the analog system 200 in real-time and provide control feedback to the analog system 200 over the interconnect, allowing for increased throughput and system performance.

One of skill in the art will recognize that the concepts taught herein can be tailored to a particular application in many other ways. In particular, those skilled in the art will recognize that the illustrated embodiments are but one of many alternative implementations that will become apparent upon reading this disclosure.

The preceding embodiments are examples. Although the specification may refer to "an", "one", "another", or "some" embodiment(s) in several locations, this does not necessarily mean that each such reference is to the same embodiment(s), or that the feature only applies to a single embodiment.

CLAIMS

1. A system comprising:

a programmable analog system that is reconfigurable to perform various analog operations;

a programmable digital system that is reconfigurable to perform various digital operations; and

a microcontroller capable of reconfiguring and controlling the programmable analog system and the programmable digital system, wherein the programmable digital system is configured to control the programmable analog system autonomously of the microcontroller.

2. The system of claim 1, further comprising a system interconnect controlled by the programmable digital system, wherein the programmable digital system is configured to direct reconfiguration of the programmable analog system and control the programmable analog system over the system interconnect.

3. The system of claim 1, wherein the programmable analog system includes multiple analog circuits that are reconfigurable to perform various analog data operations, and wherein the programmable digital system includes multiple digital circuits that are reconfigurable to perform various digital data operations.

4. The system of claim 3, wherein one or more digital circuits in the programmable digital system are configured to implement a digital controller, wherein the digital controller is configured to direct the reconfiguration of the analog circuits in the programmable analog

system and direct the reconfiguration of other digital circuits in the programmable digital system.

5. The system of claim 4, further comprising a memory device to store configuration data that, when provided to the programmable digital system, causes the programmable digital system to reconfigure the one or more digital circuits to implement the digital controller.

6. The system of claim 5, further comprising a direct memory access engine to retrieve the configuration data from the memory device when the system is initially booted and send the configuration data to the programmable digital system.

7. The system of claim 3, wherein the microcontroller is configured to reconfigure the one or more digital circuits in the programmable digital system to implement a digital controller.

8. The system of claim 1, wherein the programmable digital system is configured to direct the programmable analog system and programmable digital system to implement at least one mixed-signal application autonomously of the microcontroller.

9. A method comprising:

receiving configuration data that prompts a digital system to implement a digital control device;

sending, with the digital control device, one or more commands to an analog system over an interconnect controlled by the digital control device, wherein the one or more commands are configured to prompt a reconfiguration of the analog system; and

controlling, with the digital control device, analog data operations performed by the reconfigured analog system independently of a microcontroller.

10. The method of claim 9, wherein the digital system includes one or more universal digital block devices that are reconfigurable to perform digital data operations, and wherein the configuration data, when provided to the digital system, causes the digital system to reconfigure at least one of the universal digital block devices to implement the digital control device.

11. The method of claim 9, wherein analog system including one or more analog circuits that are reconfigurable to perform the analog data operations, and wherein the digital control device is configured to direct the reconfiguration of the analog circuits in the analog system and configured to control the analog data operations performed by the reconfigured analog circuits in the programmable analog system.

12. The method of claim 9, wherein the configuration data is received from a direct memory access engine performing direct memory access operations that retrieve the configuration data from a memory device.

13. The method of claim 9, wherein the configuration data is received from the microcontroller.

14. A system comprising:

a programmable analog system including one or more analog circuits that are reconfigurable to perform analog data operations; and

a programmable digital system including one or more universal digital block devices that are reconfigurable to perform digital data operations, wherein at least one of the universal digital block devices is reconfigured to implement a digital control device that controls the programmable analog system.

15. The system of claim 14, wherein the digital control device is configured to direct the reconfiguration of the analog circuits in the programmable analog device and configured to control the analog data operations performed by the reconfigured analog circuits in the programmable analog system.

16. The system of claim 14, further comprising a microcontroller capable of controlling the programmable analog system and the programmable digital system, wherein the programmable digital system is configured to direct the reconfiguration of the analog circuits and control the analog data operations performed by the programmable analog system independently of the microcontroller.

17. The system of claim 14, further comprising a system interconnect controlled by the programmable digital system, wherein the programmable digital system is configured to direct reconfiguration of the programmable analog system and control the programmable analog system over the system interconnect.

18. The system of claim 14, further comprising a memory device to store configuration data that, when provided to the programmable digital system, causes the programmable digital system to reconfigure at least one of the universal digital block devices to implement the digital control device.

19. The system of claim 18, further comprising a direct memory access engine to retrieve the configuration data from the memory device when the system is initially booted and send the configuration data to the programmable digital system.

20. The system of claim 14, wherein the programmable analog system is configured to control the programmable digital system autonomously of a microcontroller.

Figure 1

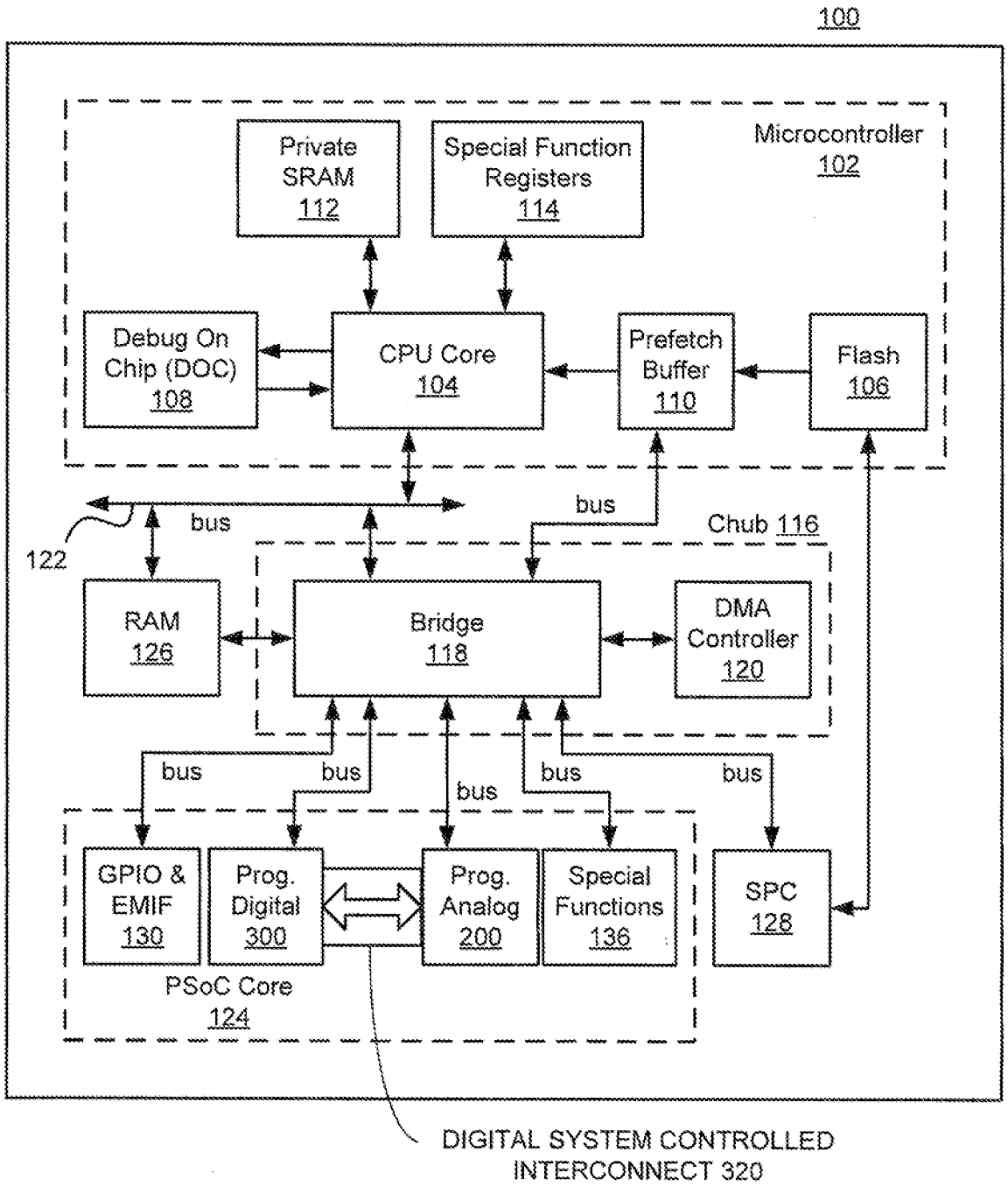

100
Microcontroller
102
Private SRAM
112
Special Function Registers
114
Debug On Chip (DOC)
108
CPU Core
104
Prefetch Buffer
110
Flash
106
bus
bus
122
Chub 116
RAM
126
Bridge
118
DMA Controller
120
bus
bus
bus
bus
bus
GPIO & EMIF
130
Prog. Digital
300
Prog. Analog
200
Special Functions
136
SPC
128
PSoC Core
124
DIGITAL SYSTEM CONTROLLED INTERCONNECT 320

Figure 2

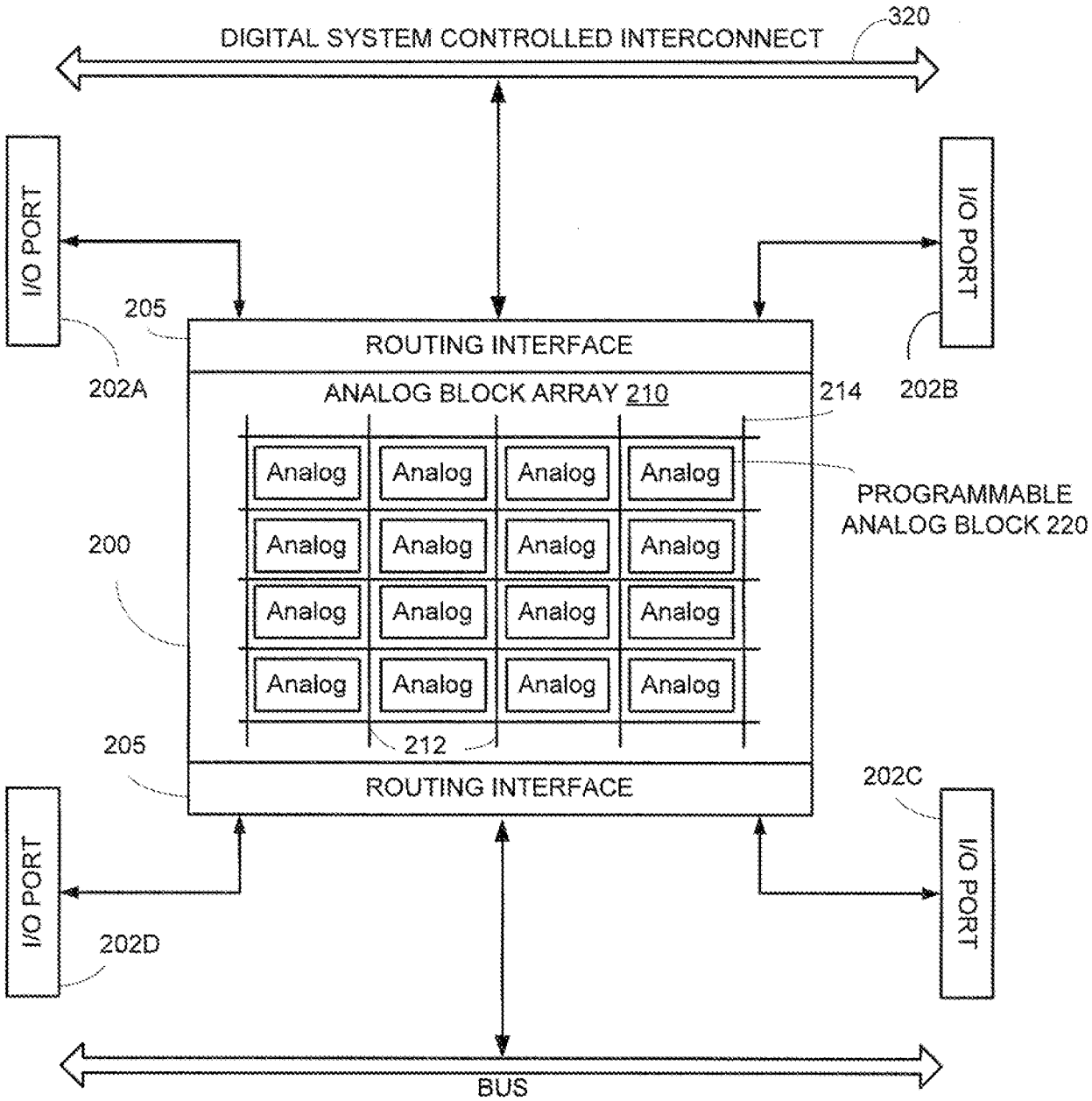

DIGITAL SYSTEM CONTROLLED INTERCONNECT
320
I/O PORT
I/O PORT
205
ROUTING INTERFACE
202A
ANALOG BLOCK ARRAY 210
214
202B
Analog
PROGRAMMABLE
ANALOG BLOCK 220
200
205
212
ROUTING INTERFACE
202C
I/O PORT
I/O PORT
202D
BUS

Figure 3

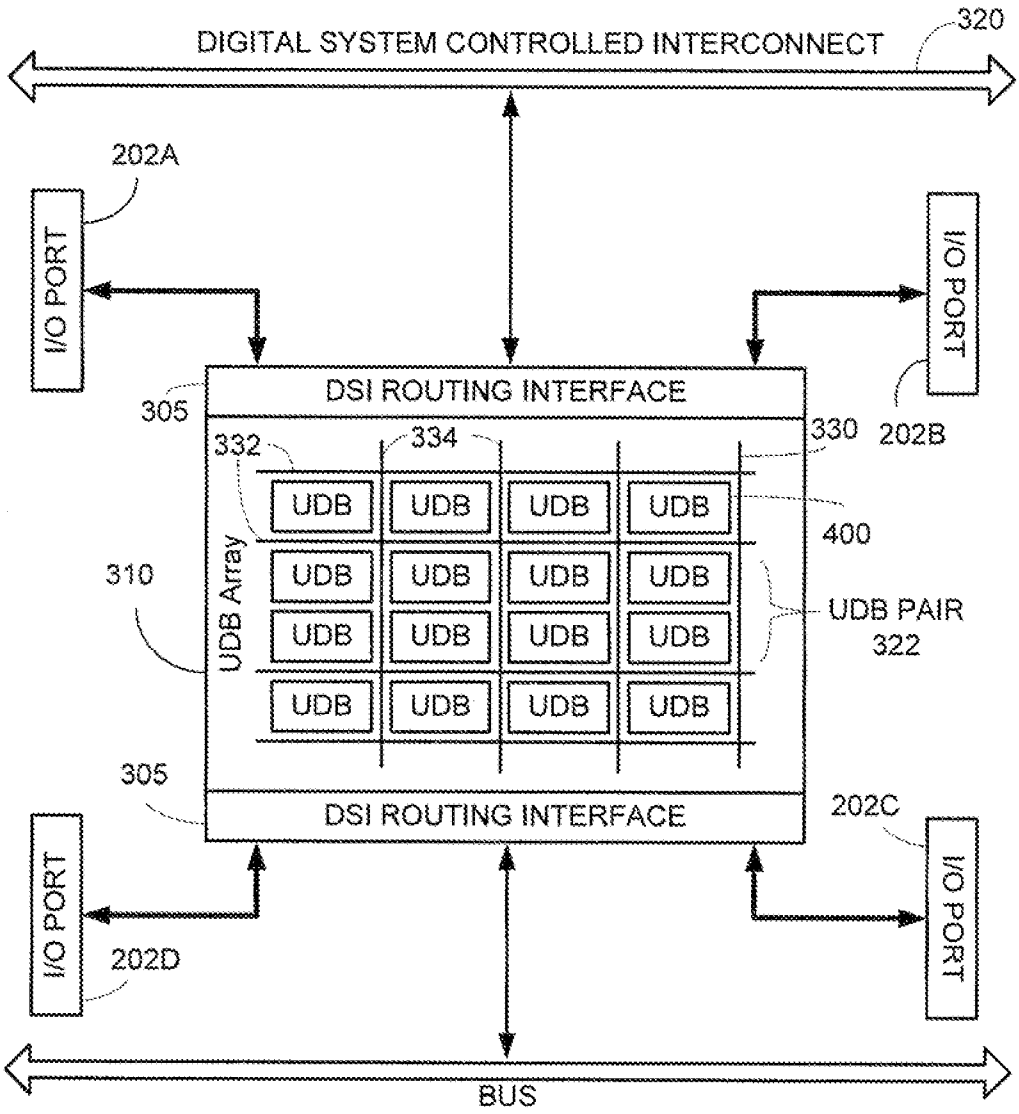

DIGITAL SYSTEM CONTROLLED INTERCONNECT
320
202A
I/O PORT
I/O PORT
202B
305
DSI ROUTING INTERFACE
330
332
334
UDB
400
UDB Array
310
UDB PAIR
322
305
DSI ROUTING INTERFACE
202C
I/O PORT
I/O PORT
202D
BUS

Figure 4

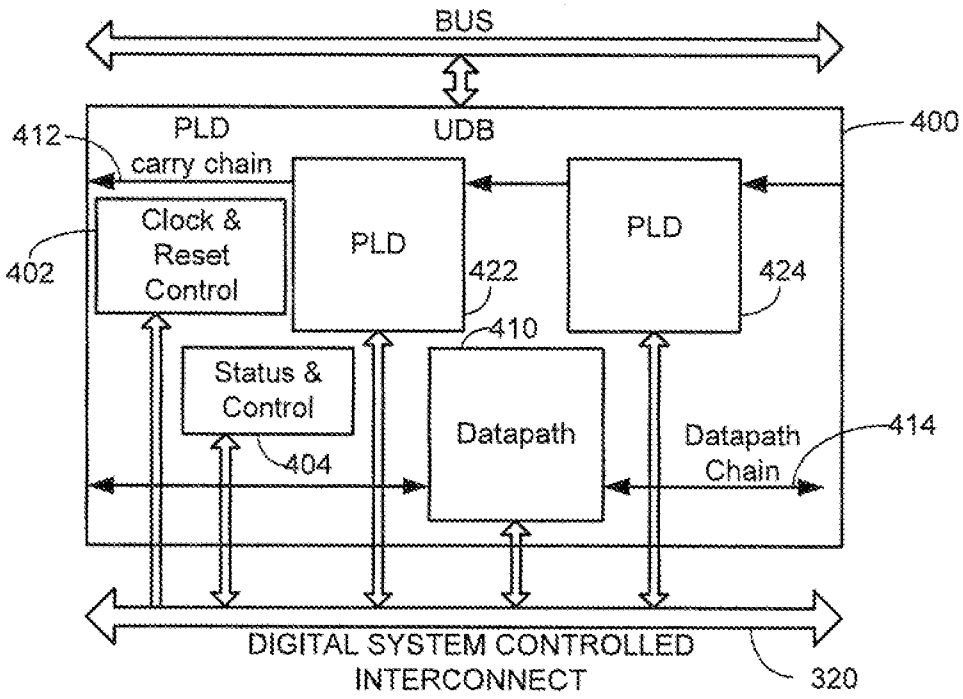

BUS
412
PLD
carry chain
UDB
400
Clock &
Reset
Control
402
PLD
422
PLD
424
410
Status &
Control
404
Datapath
Datapath
Chain
414
DIGITAL SYSTEM CONTROLLED
INTERCONNECT
320

Figure 5

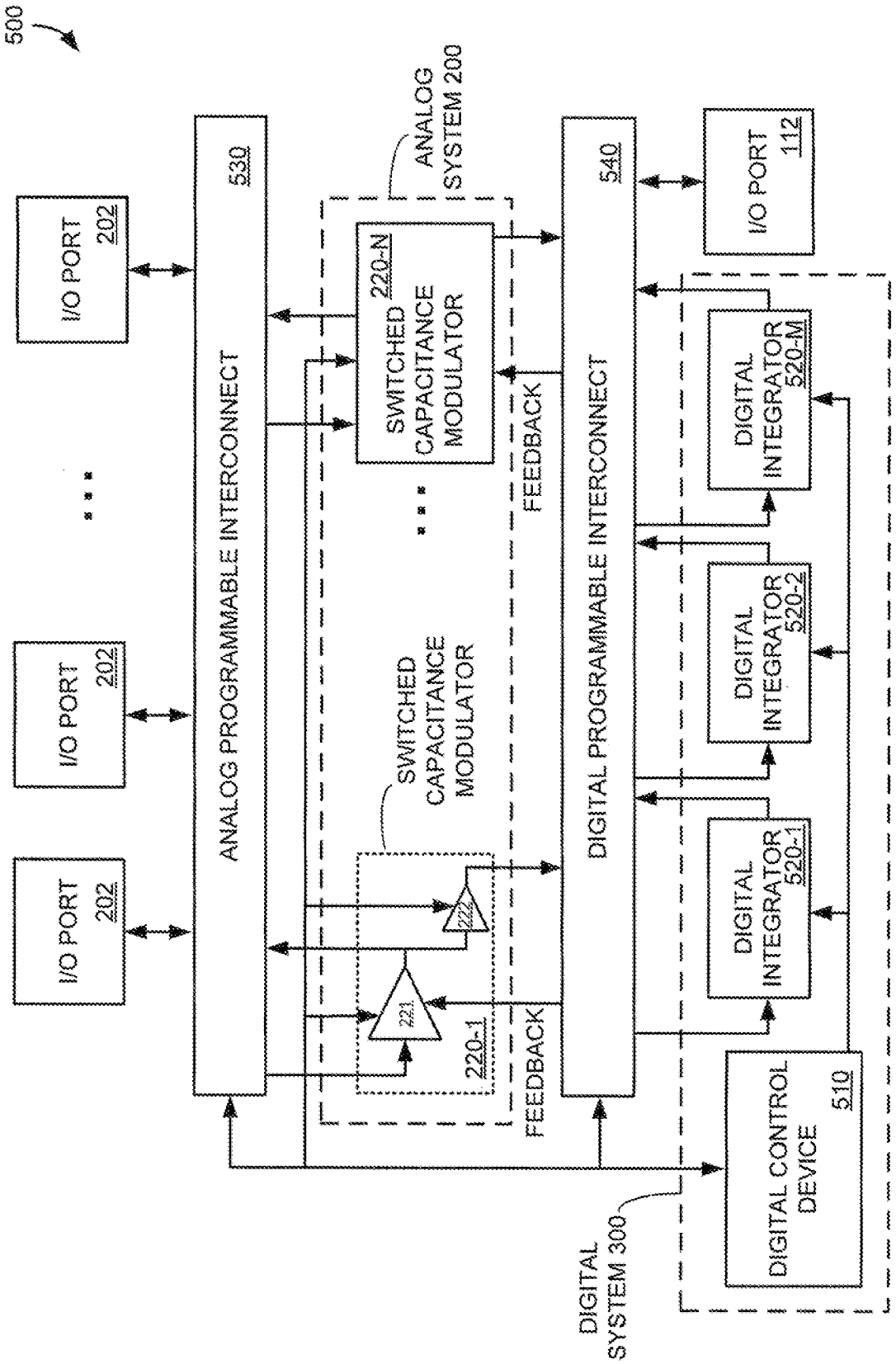
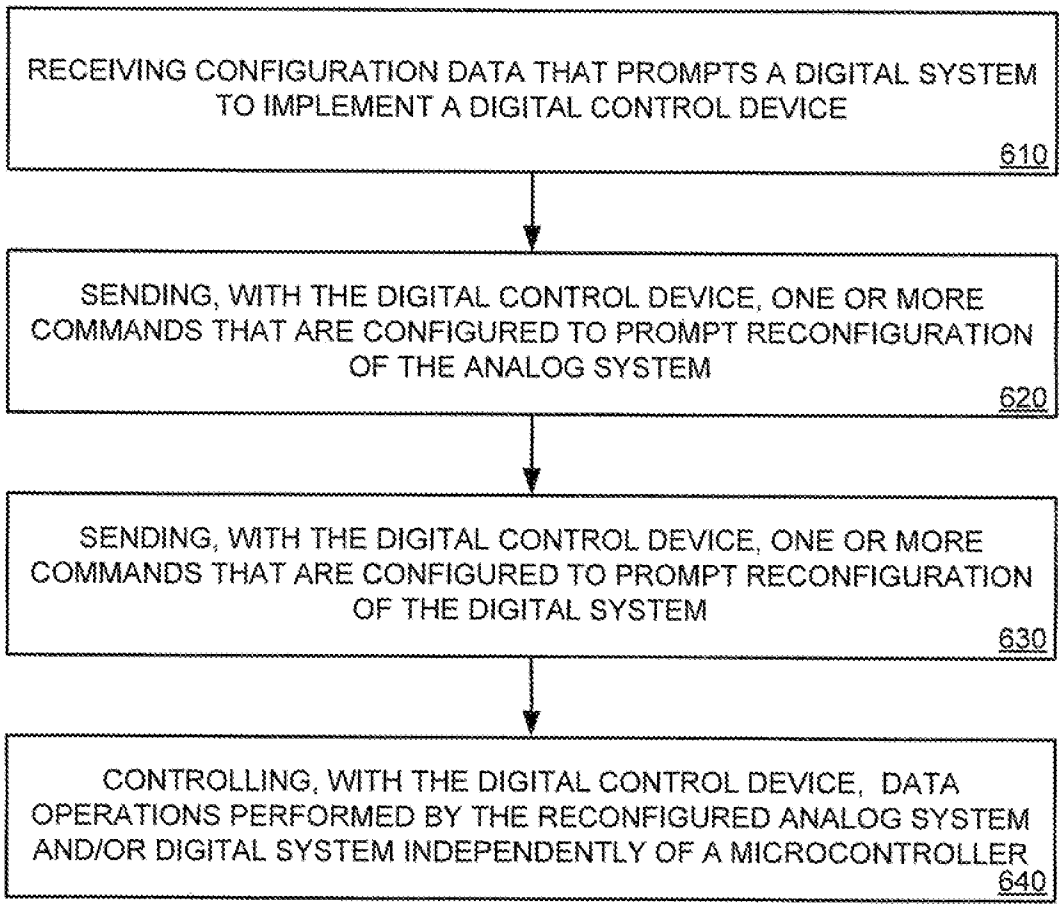

500
ANALOG-TO-DIGITAL CONVERTER IMPLEMENTATION
I/O PORT 202
I/O PORT 202
I/O PORT 202
ANALOG PROGRAMMABLE INTERCONNECT 530
ANALOG SYSTEM 200
SWITCHED CAPACITANCE MODULATOR 220-N
SWITCHED CAPACITANCE MODULATOR 220-1
221
222
FEEDBACK
FEEDBACK
DIGITAL PROGRAMMABLE INTERCONNECT 540
I/O PORT 112
DIGITAL INTEGRATOR 520-M
DIGITAL INTEGRATOR 520-2
DIGITAL INTEGRATOR 520-1
DIGITAL CONTROL DEVICE 510
DIGITAL SYSTEM 300

Figure 6


RECEIVING CONFIGURATION DATA THAT PROMPTS A DIGITAL SYSTEM TO IMPLEMENT A DIGITAL CONTROL DEVICE
610
SENDING, WITH THE DIGITAL CONTROL DEVICE, ONE OR MORE COMMANDS THAT ARE CONFIGURED TO PROMPT RECONFIGURATION OF THE ANALOG SYSTEM
620
SENDING, WITH THE DIGITAL CONTROL DEVICE, ONE OR MORE COMMANDS THAT ARE CONFIGURED TO PROMPT RECONFIGURATION OF THE DIGITAL SYSTEM
630
CONTROLLING, WITH THE DIGITAL CONTROL DEVICE, DATA OPERATIONS PERFORMED BY THE RECONFIGURED ANALOG SYSTEM AND/OR DIGITAL SYSTEM INDEPENDENTLY OF A MICROCONTROLLER
640

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 10/33626

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G05B 15/00 (2010.01)
USPC - 700/1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC - 700/1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 711/100; 326/37; 712/1, 32, 37; 700/1, 2

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Dialog Classic (Chinese Pat Abstr; Derwent Index, EPFT, French Pat, Jap Abstr, USPFT, WIPO/PCT PFT); Google Scholar; Terms searched: ACCESS, ANALOG, AUTONOMOUS, AUTONOMOUSLY, BOOT, CONFIGUR, CONTROL, DATABASE, DIGITAL, INTERCONNECT, MEMOR, MICROCONTROLLER, MIXED, MIXED-SIGNAL, MONITOR, PROGRAM, PROGRAMMABLE ANALOG...

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7,221,187 B1 (Snyder et al.) 22 May 2007 (22.05.2007); entire document, especially: col 2, ln 42-45; col 2 ln 65 to col 3, ln 31; col 3, ln 51-54; col 4, ln 45-57; col 5, ln 6-27, 63-66; col 6, ln 1-5	1-5, 7-9, 11, 13
Y		6, 10, 12, 14-20
Y	US 2008/0294806 A1 (Swindle et al.) 27 November 2008 (27.11.2008); entire document, especially: para [0016], [0020], [0024], [0030]-[0031], [0035]	6, 10, 12, 14-20
A	US 2008/0258760 A1 (Sullam et al.) 23 October 2008 (23.10.2008); entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 June 2010 (12.06.2010)	24 JUN 2010

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)