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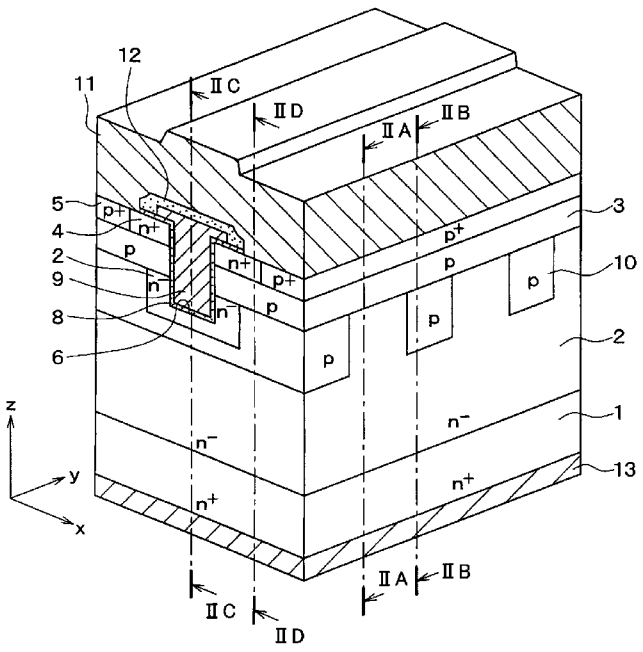
[Continued on next page]

(54) Title: SILICON CARBIDE SEMICONDUCTOR DEVICE

[Fig. 1]



(57) Abstract: A silicon carbide semiconductor device has a trench gate switching element including: a substrate (1), a drift layer (2) and a base region (3) stacked in this order; a source region (4) and a contact region (5) in upper portions of the base region (3); a trench (6) extending from the source region (4) to penetrate the base region (3); a gate electrode (9) on a gate insulating film (8) in the trench (6); a source electrode (11) coupled with the source region (4) and the base region (3); a drain electrode (13) on a back of the substrate (1); and multiple deep layers (10) in an upper portion of the drift layer (2) disposed deeper than the trench (6) and extending in a direction, which crosses the longitudinal direction of the trench. A whole of or a part of one of the deep layers (10) is spaced apart from the trench (6).

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Description

Title of Invention: SILICON CARBIDE SEMICONDUCTOR DEVICE

Cross Reference to Related Application

[0001] This application is based on Japanese Patent Application No. 2011-27996 filed on February 11, 2011, the disclosure of which is incorporated herein by reference.

Technical Field

[0002] The present disclosure relates to a silicon carbide semiconductor device having a trench gate type switching element.

Background Art

[0003] In SiC semiconductor devices, an increase in channel density is effective for providing greater electric current. A MOSFET with a trench gate structure has therefore been adopted and already been put to practical use in silicon transistors. Needless to say, this trench gate structure can be applied to a SiC semiconductor device. A serious problem however occurs when it is applied to SiC. Described specifically, SiC has breakdown field strength ten times that of silicon so that a SiC semiconductor device is used while applying a voltage about ten times that of a silicon device. As a result, an electric field ten times that of the silicon device is applied to a gate insulating film formed in a trench in SiC and the gate insulating film is easily broken at a corner of the trench.

[0004] In order to overcome this problem, Patent Document 1 proposes a SiC semiconductor device having, below a p type base region, p type deep layers which are formed in a stripe pattern and cross a trench constituting a trench gate structure. In this SiC semiconductor device, by extending a depletion layer from each of the p type deep layers toward an n^- type drift layer to prevent application of a high voltage to a gate insulating film, an electric field concentration in the gate insulating film can be mitigated and thereby the gate insulating film can be prevented from being broken.

[0005] Although the structure equipped with the p type deep layers as described in Patent Document 1 is effective for preventing an electric field concentration to the gate insulating film, a current path is narrowed by the p type deep layers and a JFET region is formed between two p type deep layers adjacent to each other, which causes an increase in on-resistance.

Citation List

Patent Literature

[0006] PTL 1: JP-A-2009-194065 corresponding to US 2009/0200559

Summary

[0007] In view of the above-described problem, it is an object of the present disclosure to provide a silicon carbide semiconductor device having a trench gate type switching element with a low on-state resistance.

[0008] According to an aspect of the present disclosure, a silicon carbide semiconductor device includes: an inversion type semiconductor switching element with a trench gate structure. The inversion type semiconductor switching element includes: a substrate having first or second conductivity type and made of silicon carbide; a drift layer disposed on the substrate, having an impurity concentration lower than the substrate, having the first conductivity type, and made of silicon carbide; a base region disposed on the drift layer, having the second conductivity type, and made of silicon carbide; a source region disposed in an upper portion of the base region, having an impurity concentration higher than the drift layer, having the first conductivity type, and made of silicon carbide; a contact region disposed in another upper portion of the base region, having an impurity concentration higher than the base layer, having the second conductivity type, and made of silicon carbide; a trench extending from a surface of the source region to penetrate the base region, and having a first direction as a longitudinal direction; a gate insulating film disposed on an inner wall of the trench; a gate electrode disposed on the gate insulating film in the trench; a source electrode electrically coupled with the source region and the base region; and a drain electrode disposed on a back side of the substrate. The inversion type semiconductor switching element is configured to flow current between the source electrode and the drain electrode via the source region, an inversion type channel region and the drift layer. The inversion type channel region is provided in a portion of the base region positioned on a side of the trench by controlling a voltage applied to the gate electrode. The inversion type semiconductor switching element further includes: a plurality of deep layers having the second conductivity type. Each deep layer is disposed in an upper portion of the drift layer below the base region, has a depth deeper than the trench, and extends along a second direction, which crosses the first direction. A whole of or a part of one of the deep layers is spaced apart from the trench.

[0009] In the above device, since the whole of or the part of one of the deep layers is spaced apart from the trench, a width of the channel is enlarged when a gate voltage is applied to the gate electrode. Thus, a width of a JFET region is sufficiently wide, compared with a case where the deep layer contacts the trench. A JFET resistance is reduced, and therefore, an on-state resistance is reduced.

Brief Description of Drawings

[0010] The above and other objects, features and advantages of the present disclosure will become more apparent from the following detailed description made with reference to

the accompanying drawings. In the drawings:

[fig.1]FIG. 1 is a perspective cross-sectional view of an inversion type MOSFET having a trench gate structure according to a first embodiment;

[fig.2A]FIG. 2A is a cross-sectional view of the MOSFET taken along the line IIA-IIA in parallel with the xz plane in FIG. 1;

[fig.2B]FIG. 2B is a cross-sectional view of the MOSFET taken along the line IIB-IIB in parallel with the xz plane in FIG. 1;

[fig.2C]FIG. 2C is a cross-sectional view of the MOSFET taken along the line IIC-IIC in parallel with the yz plane in FIG. 1;

[fig.2D]FIG. 2D is a cross-sectional view of the MOSFET taken along the line IID-IID in parallel with the yz plane in FIG. 1;

[fig.3]FIG. 3 is a partial perspective cross-sectional view of the vicinity of a trench in a trench gate structure shown while omitting therefrom a gate oxide film, a gate electrode, and the like;

[fig.4A]FIG. 4A is a cross-sectional view of the MOSFET taken along line IIB-IIB in FIG. 1 showing a manufacturing step of the MOSFET having a trench gate structure shown in FIG. 1;

[fig.4B]FIG. 4B is a cross-sectional view of the MOSFET taken along line IID-IID in FIG. 1 showing the manufacturing step of the MOSFET having a trench gate structure shown in FIG. 1;

[fig.4C]FIG. 4C is a cross-sectional view of the MOSFET taken along line IIB-IIB in FIG. 1 showing the manufacturing step of the MOSFET having a trench gate structure shown in FIG. 1;

[fig.4D]FIG. 4D is a cross-sectional view of the MOSFET taken along line IID-IID in FIG. 1 showing the manufacturing step of the MOSFET having a trench gate structure shown in FIG. 1;

[fig.4E]FIG. 4E is a cross-sectional view of the MOSFET taken along line IIB-IIB in FIG. 1 showing the manufacturing step of the MOSFET having a trench gate structure shown in FIG. 1;

[fig.4F]FIG. 4F is a cross-sectional view of the MOSFET taken along line IID-IID in FIG. 1 showing the manufacturing step of the MOSFET having a trench gate structure shown in FIG. 1;

[fig.5A]FIG. 5A is a cross-sectional view of the MOSFET taken along line IIB-IIB in FIG. 1 showing a manufacturing step of the MOSFET having a trench gate structure following those of FIGS. 4A, 4C and 4E;

[fig.5B]FIG. 5B is a cross-sectional view of the MOSFET taken along line IID-IID in FIG. 1 showing the manufacturing step of the MOSFET having a trench gate structure following those of FIGS. 4B, 4D and 4F;

[fig.5C]FIG. 5C is a cross-sectional view of the MOSFET taken along line IIB-IIB in FIG. 1 showing the manufacturing step of the MOSFET having a trench gate structure following those of FIGS. 4A, 4C and 4E;

[fig.5D]FIG. 5D is a cross-sectional view of the MOSFET taken along line IID-IID in FIG. 1 showing manufacturing steps of the MOSFET having a trench gate structure following those of FIGS. 4B, 4D and 4F;

[fig.5E]FIG. 5E is a cross-sectional view of the MOSFET taken along line IIB-IIB in FIG. 1 showing manufacturing steps of the MOSFET having a trench gate structure following those of FIGS. 4A, 4C and 4E;

[fig.5F]FIG. 5F is a cross-sectional view of the MOSFET taken along line IID-IID in FIG. 1 showing the manufacturing step of the MOSFET having a trench gate structure following those of FIGS. 4B, 4D and 4F;

[fig.6]FIG. 6 is a perspective cross-sectional view of a SiC semiconductor device according to a second embodiment;

[fig.7A]FIG. 7A is a cross-sectional view taken along the line VIIA-VIIA in parallel with the xz plane in FIG. 6;

[fig.7B]FIG. 7B is a cross-sectional view taken along the line VIIB-VIIB in parallel with the yz plane in FIG. 6;

[fig.8]FIG. 8 is a perspective cross-sectional view of a SiC semiconductor device according to a third embodiment;

[fig.9A]FIG. 9A is a cross-sectional view taken along the line IXA-IXA in parallel with the xz plane in FIG. 8;

[fig.9B]FIG. 9B is a cross-sectional view taken along the line IXB-IXB in parallel with the yz plane in FIG. 8;

[fig.10]FIG. 10 is a perspective cross-sectional view of a SiC semiconductor device according to a fourth embodiment;

[fig.11A]FIG. 11A is a cross-sectional view taken along the line XIA-XIA in parallel with the xz plane in FIG. 10;

[fig.11B]FIG. 11B is a cross-sectional view taken along the line XIB-XIB in parallel with the yz plane in FIG. 10;

[fig.12]FIG. 12 is a perspective cross-sectional view of a SiC semiconductor device according to a fifth embodiment;

[fig.13A]FIG. 13A is a cross-sectional view taken along the line XIIIA-XIIIA in parallel with the xz plane in FIG. 12;

[fig.13B]FIG. 13B is a cross-sectional view taken along the line XIIIB-XIIIB in parallel with the yz plane in FIG. 12;

[fig.14]FIG. 14 is a perspective cross-sectional view of a SiC semiconductor device according to a sixth embodiment;

[fig.15A]FIG. 15A is a cross-sectional view taken along the line XVA-XVA in parallel with the xz plane in FIG. 14; and

[fig.15B]FIG. 15B is a cross-sectional view taken along the line XVB-XVB in parallel with the yz plane in FIG. 14; and

[fig.16A]FIG. 16A is a partial perspective cross-sectional view of the vicinity of the trench in various SiC semiconductor devices described in other embodiments which are shown while omitting a gate oxide film, a gate electrode or the like in a trench gate structure;

[fig.16B]FIG. 16B is a partial perspective cross-sectional view of the vicinity of the trench in various SiC semiconductor devices described in other embodiments which are shown while omitting a gate oxide film, a gate electrode or the like in a trench gate structure; and

[fig.16C]FIG. 16C is a partial perspective cross-sectional view of the vicinity of the trench in various SiC semiconductor devices described in other embodiments which are shown while omitting a gate oxide film, a gate electrode or the like in a trench gate structure.

Description of Embodiments

[0011] (First Embodiment)

[0012] A first embodiment will next be described. Here, a description will be made on an inversion type MOSFET which is equipped in a SiC semiconductor device and serves as a semiconductor switching element having a trench gate structure.

[0013] FIG. 1 is a perspective cross-sectional view of a MOSFET having a trench gate structure according to the present embodiment. This drawing corresponds to one cell of the MOSFET. Although only one cell of the MOSFET is shown in this diagram, two or more columns of MOSFETs having a similar structure to that of the MOSFET of FIG. 1 are arranged adjacent to each other. FIGS. 2A to 2D are cross-sectional views of the MOSFET of FIG. 1. FIG. 2A is a cross-sectional view taken along the line IIA-IIA in parallel with the xz plane in FIG. 1; FIG. 2B is a cross-sectional view taken along the line IIB-IIB in parallel with the xz plane in FIG. 1, FIG. 2C is a cross-sectional view taken along the line IIC-IIC in parallel with the yz plane in FIG. 1, and FIG. 2D is a cross-sectional view taken along the line IID-IID in parallel with the yz plane in FIG. 1.

[0014] In MOSFET shown in FIG. 1 and FIGS. 2A to 2D, an n^+ type substrate 1 made of SiC is used as a semiconductor substrate. The n^+ type substrate 1 has, for example, a concentration of n type impurities, such as nitrogen, of $1.0 \times 10^{19}/cm^3$ and a thickness of about 300 micrometer. This n^+ type substrate 1 has, on the surface thereof, an n^- type drift layer 2 having, for example, a concentration of n type impurities, such as nitrogen,

of from $3.0x10^{15}/cm^3$ to $2.0x10^{16}/cm^3$ and a thickness of from about 10 to 15 micrometer and made of SiC . The impurity concentration of this n^- type drift layer 2 may be uniform in the depth direction, but preferably has a gradient concentration distribution in which the concentration of a portion of the n^- type drift layer 2 on the side of the n^+ type substrate 1 is higher than that of a portion of the n^- type drift layer 2 on the side distant from the n^+ type substrate 1. For example, it is recommended to make the impurity concentration of a portion of the n^- type drift layer 2 within a range from the surface of the n^+ type substrate 1 to about 3 to 5 micrometer therefrom higher by about $2.0x10^{15}/cm^3$ than another portion. This makes it possible to reduce the internal resistance of the n^- type drift layer 2, thereby achieving a reduction in on-resistance.

[0015] This n^- type drift layer 2 has, in the surface layer portion thereof, a p type base region 3 and the p type base region 3 has thereover an n^+ type source region 4 and p^+ type contact layer 5.

[0016] The p type base region 3 has, for example, a concentration of p type impurities, such as boron or aluminum, of from $1.0x10^{16}$ to $2.0x10^{19}$ $/cm^3$ and a thickness of about 2.0 micrometer. The n^+ type source region 4 has, in the surface layer thereof, for example, a concentration of n type impurities (surface concentration) such as nitrogen of $1.0x10^{21}$ $/cm^3$ and a thickness of about 0.3 micrometer. The p^+ type contact layer 5 has, in the surface layer thereof, for example, a concentration of p type impurities (surface concentration) such as boron or aluminum of $1.0x10^{21}$ $/cm^3$ and a thickness of about 0.3 micrometer. The n^+ type source region 4 is placed on both sides of a trench gate structure which will be described later and the p^+ type contact layer 5 is provided on the side opposite to the trench gate structure with the n^+ type source region 4 therebetween.

[0017] A trench 6 having, for example, a width of from 0.5 to 2.0 micrometer and a depth of 2.0 micrometer or greater (for example, 2.4 micrometer) is formed so as to penetrate through the p type base region 3 and the n^+ type source region 4 and reach the n^- type drift layer 2. The p type base region 3 and the n^+ type source region 4 are placed so as to be in contact with the side surface of this trench 6.

[0018] The inner wall surface of the trench 6 is covered with a gate oxide film 8 and the trench 6 is filled with a gate electrode 9 comprised of doped Poly-Si formed on the surface of the gate oxide film 8. The gate oxide film 8 is formed by thermally oxidizing the inner wall surface of the trench 6. The gate oxide film 8 has a thickness of about 100 nm both on the side surface and the bottom of the trench 6.

[0019] The trench gate structure has such a constitution. This trench gate structure extends with the direction y in FIG. 1 as a longitudinal direction. Two or more trench gate structures are arranged in parallel along the direction x in FIG. 1, thus forming a stripe pattern. The n^+ type source region 4 and the p^+ type contact layer 5 also extend along

the longitudinal direction of the trench gate structure.

[0020] Further, p type deep layers 10 extending in a direction crossing the trench gate structure are formed in the n^- type drift layer 2 below the p type base region 3. Each of the p type deep layers 10 has a certain depth. It is coupled to the p type base region 3, whereby it is fixed to a potential equal to that of the p type base region 3.

[0021] In the present embodiment, each of the p type deep layers 10 extends along the normal direction (direction x in FIG. 1) of the side surface of the trench 6 in which a channel region is formed in the trench gate structure, that is, extends in a direction perpendicular to the longitudinal direction of the trench 6. A plurality of such p type deep layers 10 is arranged in the longitudinal direction of the trench 6. These p type deep layers 10 are located deeper than the bottom portion of the trench 6. Their depth from the surface of the n^- type drift layer 2 is, for example, from about 2.6 to 3.0 micrometer (depth from the bottom portion of the p type base region 3 is, for example, from 0.6 to 1.0 micrometer). The concentration of p type impurities such as boron or aluminum is, for example, from 1.0×10^{17} to 1.0×10^{19} /cm^3. The p type deep layers 10 are in contact with the p type base region 3 so that they are fixed to a potential equal to that of the p type base region 3.

[0022] More specifically, the whole or a portion of each of the p type deep layers 10 is spaced apart from the inner wall surface of the trench 6, meaning that the p type deep layer is not in contact with at least either one of the side surface or bottom surface of the trench 6. In the present embodiment, the p type deep layers 10 are each formed at a place spaced apart from the trench gate structure so as to prevent it from contacting to both the side surface and the bottom surface of the trench gate structure. Described specifically, each of the p type deep layers 10 extends along the normal line of the side surface of the trench 6 as described above, but at a position where the trench 6 is to be formed, the p type deep layers 10 are formed neither between the trench 6 and a position spaced apart from the side surface thereof with a first predetermined distance nor between the trench and a position spaced apart from the bottom surface thereof with a second predetermined distance, meaning that each of the p type deep layers 10 has a concave form. As a result, the p type deep layers 10 are provided below the n^- type drift layer 2 on the side surface and the bottom surface of the trench 6 and the p type deep layers 10 are not exposed from the inner wall surface of the trench 6.

[0023] FIG. 3 is a partial perspective cross-sectional view of the vicinity of the trench 6 shown while omitting the gate oxide film 8 and the gate electrode 9 from the trench gate structure. As illustrated in FIG. 1, FIGS. 2A to 2D, and FIG. 3, the p type deep layers 10 of the present embodiment are each, at a site from the bottom portion thereof on the side closest to the n^+ type substrate 1 to a position having a predetermined depth from the bottom portion of the trench 6, in a linear form in a direction perpendicular to

the longitudinal direction of the trench 6 including the bottom of the trench 6. However, the p type deep layers 10 are each, at a site shallower than the position having a predetermined depth from the bottom portion of the trench 6, not in a linear form because a portion of it corresponding to a size wider than the width of the trench 6 is not formed at this site and the bottom portion of the trench 6 is surrounded at the periphery thereof with the n^- type drift layer 2. Thus, each of the p type deep layers 10 has a two-layer structure having a lower layer region which is a portion in a linear form and an upper layer region which is a portion not in a linear form, separated by the trench 6. In the upper layer region, the p type deep layers 10 are each spaced apart from the side surface of the trench 6 with a first predetermined distance.

[0024] In the present embodiment, when a gate voltage is applied to the gate electrode 9 and a channel is formed on the side surface of the trench 6, the width of the channel at the periphery of the trench 6 therefore becomes equal to that in the case where no p type deep layer 10 is formed, leading to an increase in the width of the channel. This means that in an on state, current can flow through the n^- type drift layer 2 on the side surface of the trench 6. By preventing formation of the p type deep layers 10 at the periphery of the trench 6, a JFET region can be widened and a JFET resistance can be reduced compared with a structure in which the p type deep layers 10 are formed in contact with both the side surface and the bottom surface of the trench 6.

[0025] The n^+ type source region 4, the p^+ type contact layer 5, and the gate electrode 9 have on the surfaces thereof a source electrode 11 and gate wiring (not illustrated). The source electrode 11 and the gate wiring are each comprised of a plurality of metals (for example, Ni/Al). At least a portion of them to be brought into contact with an n type SiC (more specifically, the n^+ type source region 4 and, when doped with n, the gate electrode 9) is comprised of a metal which can form an ohmic contact with the n type SiC and at least a portion of them to be brought into contact with a p type SiC (more specifically, the p^+ type contact layer 5 and, when doped with p, the gate electrode 9) is comprised of a metal which can form an ohmic contact with the p type SiC. The source electrode 11 and the gate wiring are formed on an interlayer insulating film 12 and therefore they are electrically insulated. Through a contact hole formed in the interlayer insulating film 12, the source electrode 11 is brought into electric contact with the n^+ type source region 4 and the p^+ type contact layer 5 and the gate wiring is brought into electric contact with the gate electrode 9.

[0026] The n^+ type substrate 1 has, on the back surface side thereof, a drain electrode 13 electrically coupled to the n^+ type substrate 1. Such a structure constitutes an inversion type MOSFET having a trench gate structure of an n-channel type.

[0027] Such an inversion type MOSFET having a trench gate structure operates as follows. Before a gate voltage is applied to the gate electrode 9, no inversion layer is formed in

the p type base region 3. Accordingly, even if a positive voltage is applied to the drain electrode 13, electrons from the n^+ type source region 4 cannot reach the p type base region 3 and no electric current flows between the source electrode 11 and the drain electrode 13.

[0028] In an off state (gate voltage = 0 V, drain voltage = 650 V, source voltage = 0 V), when a voltage is applied to the drain electrode 13, it becomes a reverse bias so that a depletion layer expands from between the p type base region 3 and the n^- type drift layer 2. Since the impurity concentration of the p type base region 3 is higher than that of the n^- type drift layer 2, the depletion layer expands mostly toward the n^- type drift layer 2. For example, in the case where the impurity concentration of the p type base region 3 is 10 times higher than the impurity concentration of the n^- type drift layer 2, the depletion layer expands about 0.7 micrometer toward the p type base region 3 and about 7.0 micrometer toward the n^- type drift layer 2. However, the thickness of the p type base region 3 is set to 2.0 micrometer that is greater than the expanding amount of the depletion layer so that occurrence of punching through can be prevented. Then, because the depletion layer expands more than the width with the drain voltage of 0 V and the depletion layer acts as an insulator, electric current does not flow between the source electrode 11 and the drain electrode 13.

[0029] In addition, because the gate voltage is 0 V, an electric field is applied between the drain and the gate. Therefore, a high electric field strength may occur also at the bottom of the gate oxide film 8. Since the p type deep layers 10 deeper than the trench 6 are provided, however, the depletion layer at a PN junction between the p type deep layers 10 and the n^- type drift layer 2 largely expands toward the n^- type drift layer 2 and a high voltage due to the influence of the drain voltage does not easily go into the gate oxide film 8. The width of the p type deep layers 10 is set in expectation of a breakdown voltage so that a higher voltage can be prevented from going into the gate oxide film 8. As a result, an electric field in the gate oxide film 8, especially, an electric field in the gate oxide film 8 at the bottom of the trench 6 can be mitigated, whereby breakage of the gate oxide film 8 can be prevented.

[0030] On the other hand, in an on state (gate voltage = 20V, drain voltage = 1V, and source voltage = 0V), a gate voltage of 20V is applied to the gate electrode 9 so that a channel is formed on the surface of the p type base region 3 which is in contact with the trench 6. Electrons injected from the source electrode 11 reach the n^- type drift layer 2 after passing through the n^+ type source region 4 and the channel formed on the p type base region 3. Accordingly, electric current can flow between the source electrode 11 and the drain electrode 13.

[0031] Furthermore, in the present embodiment, each of the p type deep layers 10 is not formed at the periphery of the trench 6. There are no p type deep layers 10 between the

trench 6 and a position spaced apart from the side surface thereof with a first predetermined distance and from the bottom surface thereof with a second predetermined distance. When a gate voltage is applied to the gate electrode 9 in an on state and a channel is formed, the channel can therefore have a wider width. This means that there are no p type deep layers 10 at the periphery of the trench 6 so that a current path can be widened to allow current to pass through the n^- type drift layer 2 at the periphery, that is, side surface and bottom surface of the trench 6. Compared with the case where the p type deep layers 10 are each formed in contact with the trench 6, this makes it possible to increase the width of a JFET region and achieve a reduction in JFET resistance.

[0032] Next, a manufacturing method of the MOSFET having a trench gate structure as shown in FIG. 1 will be described. FIGS. 4A to 4C and 5A to 5C are cross-sectional views showing manufacturing steps of the MOSFET having a trench gate structure as shown in FIG. 1. In each of FIGS. 4A to 4F and 5A to 5F, a cross-sectional view (area corresponding to FIG. 2B) taken along the line IIB-IIB in parallel with the xz plane in FIG. 1 is shown on the left side, while a cross-sectional views (area corresponding to FIG. 2D) taken along the line IID-IID in parallel with the yz plane in FIG. 1 is shown on the right side. The description will next be made referring to these drawings.

(Step shown in FIGS. 4A and 4B)

[0033] First, an n^+ type substrate 1 having, for example, a concentration of n type impurities, such as nitrogen, of 1.0×10^{19} /cm^3 and a thickness of about 300 micrometer is prepared. On the surface of the n^+ type substrate 1, an n^- type drift layer 2 having, for example, a concentration of n type impurities, such as nitrogen, of from 3.0×10^{15} /cm^3 to 2.0×10^{16} / cm^3 and a thickness of about 15 micrometer and made of SiC is formed by epitaxial growth. Then, after formation of a mask 20 made of LTO or the like on the surface of the n^- type drift layer 2, the mask 20 is opened at a predetermined formation region of an upper layer region of each of p type deep layers 10 through photolithography. Then, p type impurities (such as boron or aluminum) are implanted from above the mask 20. Ion implantation is performed to give a boron or aluminum concentration of, for example, from 1.0×10^{16} /cm^3 to 1.0×10^{19} /cm^3. By conducting such steps, the upper layer region of each of the p type deep layers 10 can be formed without forming the p type deep layer 10 at the periphery of a predetermined formation region of the trench 6.

(Step shown in FIGS. 4C and 4D)

[0034] After photolithography, the mask 20 is opened in a predetermined formation region of a lower layer region of each of the p type deep layers 10. Then, p type impurities (such as boron or aluminum) are implanted from above the mask 20. The concentration of ion implantation is similar to that in the step shown in FIGS. 4A and 4B. The mask 20 is then removed and ions thus implanted are activated.

[0035] In the above description, ion implantation of p type impurities for the upper layer region of each of the p type deep layers 10 is followed by ion implantation of p type impurities for the formation of the lower layer region, but they may be performed in reverse order. In this case, however, masks for the formation of the respective regions are necessary. Formation in the first mentioned order therefore enables use of a mask in common and as a result, the upper layer region and the lower layer region can be formed in self alignment without an influence of misalignment of masks.

(Step shown in FIGS. 4E and 4F)

[0036] A p type base region 3 is formed by epitaxial growth of a p type impurity layer having, for example, a concentration of p type impurities, such as boron or aluminum, of from $1.0x10^{15}$ to $2.0x10^{19}$ /cm^3 and a thickness of about 2.0 micrometer on the surface of the n^- type drift layer 2.

(Step shown in FIGS. 5A and 5B)

[0037] Then, after formation of a mask (not illustrated) made of, for example, LTO on the p type base region 3, photolithography is conducted to open the mask at a predetermined formation region of an n^+ type source region 4. After that, n type impurities (such as nitrogen) are implanted.

[0038] Then, after removal of the mask already used, another mask (not illustrated) is formed. Photolithography is performed to open the mask at a predetermined formation region of a p^+ type contact layer 5. Then, p type impurities (such as boron or aluminum) are implanted.

[0039] The ions thus implanted are then activated to form the n^+ type source region 4 having, for example, a concentration (surface concentration) of n type impurities such as nitrogen of $1.0x10^{21}$ /cm^3 and a thickness of about 0.3 micrometer and the p^+ type contact layer 5 having, for example, a concentration (surface concentration) of p type impurities such as boron or aluminum of about $1.0x10^{21}$ /cm^3 and a thickness of about 0.3 micrometer. After that, the mask is removed.

(Step shown in FIGS. 5C and 5D)

[0040] After formation of an etching mask, which is not illustrated, on the p type base region 3, the n^+ type source region 4, and the p^+ type contact layer 5, the etching mask is opened at a predetermined formation region of a trench 6. Then, etching is performed with the etching mask, followed by sacrificial oxidation if needed to form a trench 6. At this time, in the step of forming the p type deep layers 10 (steps of FIGS. 4A to 4D) performed previously, formation of the p type deep layers 10 is avoided at the periphery of the predetermined formation region of the trench 6 so that there is no p type deep layers 10 at the periphery of the trench 6, meaning they are not in contact with the trench. After this, the etching mask is removed.

(Step shown in FIGS. 5E and 5F)

[0041] A gate oxide film formation step is performed to form a gate oxide film 8 on the entire surface of the substrate including the inside of the trench 6. More specifically, the gate oxide film 8 is formed by gate oxidization (thermal oxidation) by a pyrogenic method using a wet atmosphere. Next, an about 440-nm thick polysilicon layer doped with n type impurities is formed on the surface of the gate oxide film 8 at a temperature of, for example, 600degrees C and then, an etch back step or the like is performed to make the poly silicon layer thinner.

[0042] Although steps following the above step are not illustrated because they are similar to conventional steps, after formation of an interlayer insulating film 12, the interlayer insulating film 12 is patterned to form a contact hole connected to the n^+ type source region 4 or the p^+ type contact layer 5 and at the same time, to form a contact hole connected to the gate electrode 9 on another cross section. Next, after a film of an electrode material is formed to fill the contact holes therewith, it is patterned to form a source electrode 11 and a gate wiring. In addition, a drain electrode 13 is formed on the back surface side of the n^+ type substrate 1. As a result, the MOSFET shown in FIG. 1 is completed.

[0043] As described above, in the SiC semiconductor device of the present embodiment, the whole or a portion of each of the p type deep layers 10 is spaced apart from the inner wall surface of the trench 6, meaning that the p type deep layer is not in contact with at least either one of the side surface or bottom surface of the trench 6. Described specifically, each of the p type deep layers 10 is not formed at the periphery of the trench 6. Each of the p type deep layers 10 is not formed between the trench 6 and a position spaced apart from the side surface thereof with a first predetermined distance and from the bottom surface thereof with a second predetermined distance. When a gate voltage is applied to the gate electrode 9 in an on state and a channel is formed, the channel can therefore have a wider width. Compared with the case where each of the p type deep layers 10 is formed in contact with the trench 6, this makes it possible to increase the width of a JFET region and reduce a JFET resistance. As a result, a reduction in on-resistance can be achieved.

(Second Embodiment)

[0044] A second embodiment will next be described. The SiC semiconductor device of this embodiment is different from that of the first embodiment in the structure of the p type deep layers 10. Since they are similar in the fundamental structure, only portions different from the first embodiment will next be described.

[0045] FIG. 6 is a perspective cross-sectional view of the SiC semiconductor device according to this embodiment. FIG. 7A is a cross-sectional view taken along the line VIIA-VIIA in parallel with the xz plane in FIG. 6 and FIG. 7B is a cross-sectional view taken along the line VIIB-VIIB in parallel with the yz plane in FIG. 6.

[0046] As shown in FIG. 6 and FIGS. 7A and 7B, in this embodiment different from the first embodiment, each of the p type deep layers 10 is in contact with the bottom portion of the trench 6, but similar to the first embodiment, each of the p type deep layers 10 is not in contact with a portion of the side surface of the trench 6. This means that each of the p type deep layers 10 extends along the normal line of the side surface of the trench 6, but in the upper layer region, each of the p type deep layers 10 is spaced apart from the side surface of the trench 6 with a first predetermine distance. In such a structure, when a gate voltage is applied to the gate electrode 9, it is possible to allow current to pass through a portion of the side surface of the trench 6 on which the n^- type drift layer 2 has remained and a current path can be widened. Compared with the first embodiment, the structure of the present embodiment is less effective, but a JFET resistance in a JFET region formed between two p type deep layers 10 adjacent to each other can be reduced and therefore, a reduction in on-resistance can be achieved.

[0047] A manufacturing method of the SiC semiconductor device of the present embodiment is basically similar to that of the first embodiment. It is only necessary to change the ion implantation depth employed in the first embodiment for the formation of the p type deep layers 10 shown in FIGS. 4A to 4D so that the lower layer region of each of the p type deep layers 10 extends to a position shallower than the bottom portion of the trench 6.

(Third Embodiment)

[0048] A third embodiment will next be described. The SiC semiconductor device of this embodiment is also different from that of the first embodiment in the structure of the p type deep layers 10. Since they are similar in the fundamental structure, only portions different from the first embodiment will next be described.

[0049] FIG. 8 is a perspective cross-sectional view of the SiC semiconductor device according to the present embodiment. FIG. 9A is a cross-sectional view taken along the line IXA-IXA in parallel with the xz plane in FIG. 8 and FIG. 9B is a cross-sectional view taken along the line IXB-IXB in parallel with the yz plane in FIG. 8.

[0050] As shown in FIG. 8 and FIGS. 9A and 9B, in the present embodiment, different from the first embodiment, each of the p type deep layers 10 is in contact with the side surface of the trench 6, but each of the p type deep layers 10 is not in contact with the bottom portion of the trench 6 as in the first embodiment. Described specifically, each of the p type deep layers 10 is not formed, at a position where the trench 6 is formed, between the bottom surface of the trench 6 and a position spaced apart from the bottom surface thereof with a second predetermined distance. In such a structure, when a gate voltage is applied to the gate electrode 9, it is possible to allow current to flow through the n^- type drift layer 2 which has remained on the bottom surface of the trench 6 and therefore widen a current path. The structure of the present embodiment is less

effective than that of the first embodiment but in the present embodiment, a JEFT resistance in a JEFT region formed between two adjacent p type deep layers 10 can be reduced and therefore, a reduction in on-resistance can be achieved.

[0051] A manufacturing method of the SiC semiconductor device of the present embodiment is also basically similar to that of the first embodiment. It is only necessary to change the mask pattern of the mask 20 used upon ion implantation for the formation of the upper layer region of the p type deep layers 10 shown in FIGS. 4A and 4B.

(Fourth embodiment)

[0052] A fourth embodiment will next be described. Different from the SiC semiconductor device of the second embodiment, that of the present embodiment has an increased concentration of a portion for expanding a current path. Since they are similar in the fundamental structure, only portions different from the first embodiment will next be described.

[0053] FIG. 10 is a perspective cross-sectional view of the SiC semiconductor device according to the present embodiment. FIG. 11A is a cross-sectional view taken along the line XIA-XIA in parallel with the xz plane in FIG. 10 and FIG. 11B is a cross-sectional view taken along the line XIB-XIB in parallel with the yz plane in FIG. 10.

[0054] As shown in FIG. 10 and FIGS. 11A and 11B, in the present embodiment, similar to the second embodiment, each of the p type deep layers 10 is not in contact with a portion of the side surface of the trench 6. Different from the second embodiment, however, this embodiment has a current diffusion layer 2a, which is a portion of the n^- type drift layer 2 but having an increased impurity concentration, at a least a place where each of the p type deep layers 10 is spaced apart from the trench 6. Described specifically, each of the p type deep layers 10 extends along the normal line of the side surface of the trench 6, but in the upper layer region, each of the p type deep layers 10 is spaced apart from the side surface of the trench 6 with a first predetermined distance and the current diffusion layer 2a is formed between the side surface of the trench 6 and each of the p type deep layers 10. In the present embodiment, a surface layer portion of the n^- type drift layer 2 located between two adjacent p type deep layers 10, that is, a site of the n^- type drift layer 2 having a depth equal to that of the upper layer region of the p type deep layers 10 is also the current diffusion layer 2a. In such a structure, when a gate voltage is applied to the gate electrode 9, a current flowing region can be dispersed so as to provide a width region of a current flow in a portion of the side surface of the trench 6 where the current diffusion layer 2a has been formed and therefore, a wider current path can be provided. In this embodiment, compared with the second embodiment, a JFET resistance in a JFET region formed between two adjacent p type deep layers 10 can be reduced more and therefore a further reduction in

on-resistance can be achieved.

[0055] The manufacturing method of the SiC semiconductor device having a structure of the present embodiment is basically similar to that of the first embodiment but different that it includes a step of forming a current diffusion layer 2a. The current diffusion layer 2a may be formed by either one of epitaxial growth or ion implantation. The steps of FIGS. 4A to 4D described in the first embodiment may be replaced by the following steps.

[0056] For example, after formation of a mask having an opening at a predetermined formation region of a lower layer region of p type deep layers 10 on the surface of the n^- type drift layer 2, p type impurities are implanted through the mask to form the lower layer region. After removal of the mask, a current diffusion layer 2a is formed by epitaxial growth on the surface of the n^- type drift layer 2 and the surface of the lower layer region of the p type deep layers 10. Then, a mask having an opening at a predetermined formation region of an upper layer region of the p type deep layers 10 is formed. With this mask, p type impurities are implanted to form the upper layer region. Steps after FIGS. 4E and 4F are then performed to manufacture the SiC semiconductor device of the present embodiment.

[0057] Another method can be employed for the manufacture of the SiC semiconductor device of the present embodiment. For example, after formation of a mask having an opening at a predetermined formation region of a lower layer region of the p type deep layers 10 on the surface of the n^- type drift layer 2, p type impurities are implanted through the mask to form the lower layer region. After removal of the mask, an upper layer region of the p type deep layers 10 is formed by epitaxial growth on the surface of the n^- type drift layer 2 and the surface of the lower layer region of the p type deep layers 10. Then, a mask having an opening at a region other than the predetermined formation region of the upper layer region of the p type deep layers 10 is formed. With this mask, n type impurities are implanted to form a current diffusion layer 2a. Steps after FIGS. 4E and 4F are then performed to manufacture the SiC semiconductor device of the present embodiment.

[0058] It is also possible to form a current diffusion layer 2a by forming the p type deep layers 10 as in the second embodiment and then implanting n type impurities. Described specifically, after removal of the mask 20, another mask having an opening at a predetermined formation region of the current diffusion layer 2a is placed, followed by implantation of n type impurities to form the current diffusion layer 2a. Implantation of n type impurities for the formation of the current diffusion layer 2a may be performed either before or after the formation of the p type deep layers 10. It may be performed between the formation steps of the upper layer region and the lower layer region of the p type deep layers 10.

[0059] In this embodiment, in an area having a depth equal to that of the upper layer region of the p type deep layers 10, an entire portion other than the p type deep layers 10 is the current diffusion layer 2a. Insofar as the current diffusion layer 2a is placed at least between the side surface of the trench 6 and the p type deep layers 10, a reduction in resistance of a current path and a reduction in on-resistance can be achieved.

(Fifth embodiment)

[0060] A fifth embodiment of the disclosure will next be described. The SiC semiconductor device of this embodiment has the current diffusion layer 2a of the fourth embodiment when the p type deep layers 10 have the structure of the first embodiment. Since they are similar in the fundamental structure, only portions different from the first embodiment will next be described.

[0061] FIG. 12 is a perspective cross-sectional view of the SiC semiconductor device according to the present embodiment. FIG. 13A is a cross-sectional view taken along the line XIIIA-XIIIA in parallel with the xz plane in FIG. 12 and FIG. 13B is a cross-sectional view taken along the line XIIIB-XIIIB in parallel with the yz plane in FIG. 12.

[0062] As illustrated in FIG. 12 and FIGS. 13A and 13B, in this embodiment similar to the first embodiment, each of the p type deep layers 10 is not in contact with the bottom surface and a portion of the side surface of the trench 6 as in the first embodiment. Furthermore, as in the fourth embodiment, a current diffusion layer 2a is formed between the side surface of the trench 6 and the p type deep layers 10 or in the surface layer portion of a portion of the n^- type drift layer 2 located between the p type deep layers 10 adjacent to each other.

[0063] Thus, the current diffusion layer 2a may be formed while the p type deep layers 10 are not brought into contact with the bottom surface and a portion of the side surface of the trench 6. When such a structure is employed, a current path can be made wider in the current diffusion layer 2a compared with the first embodiment, making it possible to achieve a further reduction in JFET resistance and a further reduction in on-resistance.

[0064] A manufacturing method of the SiC semiconductor device having the structure of the present embodiment is basically similar to that of the first embodiment, but different in that it includes a step of forming the current diffusion layer 2a. The current diffusion layer 2a may be formed by either one of epitaxial growth or ion implantation. After the steps of FIGS. 4A to 4D described in the first embodiment, the following steps may be performed.

[0065] For example, the current diffusion layer 2a may be formed by epitaxial growth before the formation step of the p type deep layers 10 in FIGS. 4A to 4D.

[0066] The current diffusion layer 2a may also be formed by implantation of n type im-

purities after the steps of FIGS. 4A to 4D. Described specifically, after removal of the mask 21, a mask having an opening at a predetermined formation region of the current diffusion layer 2a may be placed, followed by implantation of n type impurities to form the current diffusion layer 2a. Alternatively, implantation of n type impurities for the formation of the current diffusion layer 2a may be performed either before or after the step of FIGS. 4A and 4B.

[0067] Also in this embodiment, in an area having a depth equal to that of the upper layer region of the p type deep layers 10, an entire portion other than the p type deep layers 10 is the current diffusion layer 2a. Insofar as the current diffusion layer 2a is placed at least between the side surface of the trench 6 and the p type deep layers 10, a reduction in resistance of a current path and a reduction in on-resistance can be achieved.

(Sixth Embodiment)

[0068] A sixth embodiment will next be described. The SiC semiconductor device of this embodiment has the current diffusion layer 2a of the fourth embodiment in the case where the p type deep layers 10 have the structure of the third embodiment. Since they are similar to those of the third embodiment in the fundamental structure, only portions different from the third embodiment will next be described.

[0069] FIG. 14 is a perspective cross-sectional view of the SiC semiconductor device according to the present embodiment. FIG. 15A is a cross-sectional view taken along the line XVA-XVA in parallel with the xz plane in FIG. 14 and FIG. 15B is a cross-sectional view taken along the line XVB-XVB in parallel with the yz plane in FIG. 14.

[0070] As shown in FIG. 14 and FIGS. 15A and 15B, in the present embodiment, similar to the third embodiment, p type deep layers 10 are not in contact with the bottom surface of the trench 6 and moreover, similar to the fourth embodiment, a current diffusion layer 2a is formed, so as to be in contact with the side surface of the trench 6, between the side surface of the trench 6 and the p type deep layers 10 spaced apart from the trench 6 with a first predetermined distance.

[0071] In such a manner, the current diffusion layer 2a may be formed while the p type deep layers 10 are not brought into contact with the bottom surface of the trench 6. Such a structure makes it possible to reduce a JFET resistance further and therefore, reduce an on-resistance further because compared with the first embodiment , a current path can be widened more due to the current diffusion layer 2a thus formed.

[0072] A manufacturing method of the SiC semiconductor device having the structure of the present embodiment is basically similar to that of the fifth embodiment. It is only necessary to change the mask pattern upon formation of the lower portion of the upper layer region of the p type deep layers 10 so as to prevent contact of the p type deep layers 10 with the bottom portion of the trench 6 while not preventing the contact with the side surface of the trench 6.

(Other Embodiments)

[0073] In the above embodiments, all the p type deep layers 10 arranged in parallel with each other have the same structure, but some necessary p type deep layers may have the structure as shown in each embodiment. It is also possible to use the p type deep layers 10 having the structures shown in the embodiments in combination. FIGS. 16A to 16C are examples of such a combination and it is a partial perspective cross-sectional view showing the vicinity of the trench 6 while omitting the gate oxide film 8 or gate electrode 9 in the trench gate structure.

[0074] As shown in FIG. 16A, some of the p type deep layers 10 may selectively have the structure of the first embodiment. As shown in FIG. 16B, the p type deep layers 10 having the structure of the first embodiment may be used in combination with the p type deep layers 10 having the structure of the third embodiment. Further, as shown in FIG. 16C, the p type deep layers 10 having the structure of the first embodiment may be used in combination with the p type deep layers 10 having the structure of the second embodiment.

[0075] In the above first and second embodiments, the p type deep layers 10 extend in the direction x, but the p type deep layers 10 may be diagonally crossed with the longitudinal direction of the trench 6 or may be divided into two or more portions in the direction x. In the case where the p type deep layers 10 are diagonally crossed with the longitudinal direction of the trench 6, it is preferred, in order to prevent an uneven equipotential distribution, to arrange the p type deep layers 10 in line symmetry, with a line extending in a direction perpendicular to the longitudinal direction of the trench 6 as a symmetry line.

[0076] In the above embodiments, the description is made with, as an example, an n channel type MOSFET in which the first conductivity type is an n type and the second conductivity type is as a p type. The disclosure can also be applied to a p channel type MOSFET in which the conductivity type of each of the constituting elements have been reversed. In addition, in the above description, a MOSFET having a trench gate structure is used. The disclosure can also be applied to an IGBT having a similar trench gate structure. The structure or the manufacturing method of the IGBT is similar to that of the above embodiments except that the conductivity type of the substrate 1 is changed from n type to p type.

[0077] In the above embodiments, the gate oxide film 8 made by thermal oxidation is used as an example of a gate insulating film. The gate insulating film is not limited thereto but it may include an oxide film not formed by thermal oxidation or a nitride film.

[0078] The above disclosure has the following aspects.

[0079] According to an aspect of the present disclosure, a silicon carbide semiconductor device includes: an inversion type semiconductor switching element with a trench gate

structure. The inversion type semiconductor switching element includes: a substrate having first or second conductivity type and made of silicon carbide; a drift layer disposed on the substrate, having an impurity concentration lower than the substrate, having the first conductivity type, and made of silicon carbide; a base region disposed on the drift layer, having the second conductivity type, and made of silicon carbide; a source region disposed in an upper portion of the base region, having an impurity concentration higher than the drift layer, having the first conductivity type, and made of silicon carbide; a contact region disposed in another upper portion of the base region, having an impurity concentration higher than the base layer, having the second conductivity type, and made of silicon carbide; a trench extending from a surface of the source region to penetrate the base region, and having a first direction as a longitudinal direction; a gate insulating film disposed on an inner wall of the trench; a gate electrode disposed on the gate insulating film in the trench; a source electrode electrically coupled with the source region and the base region; and a drain electrode disposed on a back side of the substrate. The inversion type semiconductor switching element is configured to flow current between the source electrode and the drain electrode via the source region, an inversion type channel region and the drift layer. The inversion type channel region is provided in a portion of the base region positioned on a side of the trench by controlling a voltage applied to the gate electrode. The inversion type semiconductor switching element further includes: a plurality of deep layers having the second conductivity type. Each deep layer is disposed in an upper portion of the drift layer below the base region, has a depth deeper than the trench, and extends along a second direction, which crosses the first direction. A whole of or a part of one of the deep layers is spaced apart from the trench.

[0080] In the above device, since the whole of or the part of one of the deep layers is spaced apart from the trench, a width of the channel is enlarged when a gate voltage is applied to the gate electrode. Thus, a width of a JFET region is sufficiently large, compared with a case where the deep layer contacts the trench. A JFET resistance is reduced, and therefore, an on-state resistance is reduced.

[0081] Alternatively, a whole of or a part of each deep layer may be spaced apart from the trench. Further, each deep layer may be spaced apart from a sidewall of the trench by a first predetermined distance. Furthermore, each deep layer may have a lower layer region and an upper layer region. The upper layer region of each deep layer is spaced apart from the sidewall of the trench by the first predetermined distance.

[0082] Alternatively, the inversion type semiconductor switching element may further include a current diffusion layer, which is disposed between the sidewall of the trench and the deep layer. The current diffusion layer has an impurity concentration higher than the drift layer, which is located below the deeper layer. In this case, when the gate

voltage is applied to the gate electrode, the current easily flows in a large area of the current diffusion layer on the sidewall of the trench. Accordingly, the JFET region adjacent to the deep layer has a low JFET resistance, and therefore, the on-state resistance is reduced.

[0083] Alternatively, each deep layer may be spaced apart from a bottom of the trench by a second predetermined distance. Further, each deep layer may have a lower layer region and an upper layer region. The lower layer region of each deep layer is spaced apart from the bottom portion of the trench by the second predetermined distance.

[0084] Alternatively, each deep layer may be electrically coupled with the base region. In this case, an electric potential of the deep layer is fixed to an electric potential of the base region, i.e., the source potential.

[0085] Alternatively, a portion of the drift layer may be disposed between the trench and each deep layer so that the whole of or the part of the deep layer is spaced apart from the trench. Further, the portion of the drift layer may cover a sidewall and a bottom of the trench so that the whole of the deep layer is spaced apart from the trench.

[0086] While the disclosure has been described with reference to preferred embodiments thereof, it is to be understood that the disclosure is not limited to the preferred embodiments and constructions. The disclosure is intended to cover various modification and equivalent arrangements. In addition, while the various combinations and configurations, which are preferred, other combinations and configurations, including more, less or only a single element, are also within the spirit and scope of the disclosure.

Claims

[Claim 1] A silicon carbide semiconductor device comprising:
an inversion type semiconductor switching element with a trench gate structure,
wherein the inversion type semiconductor switching element includes:
a substrate (1) having first or second conductivity type and made of silicon carbide;
a drift layer (2) disposed on the substrate (1), having an impurity concentration lower than the substrate (1), having the first conductivity type, and made of silicon carbide;
a base region (3) disposed on the drift layer (2), having the second conductivity type, and made of silicon carbide;
a source region (4) disposed in an upper portion of the base region (3), having an impurity concentration higher than the drift layer (2), having the first conductivity type, and made of silicon carbide;
a contact region (5) disposed in another upper portion of the base region (3), having an impurity concentration higher than the base layer (3), having the second conductivity type, and made of silicon carbide;
a trench (6) extending from a surface of the source region (4) to penetrate the base region (3), and having a first direction as a longitudinal direction;
a gate insulating film (8) disposed on an inner wall of the trench (6);
a gate electrode (9) disposed on the gate insulating film (8) in the trench (6);
a source electrode (11) electrically coupled with the source region (4) and the base region (3); and
a drain electrode (13) disposed on a back side of the substrate (1),
wherein the inversion type semiconductor switching element is configured to flow current between the source electrode (11) and the drain electrode (13) via the source region (4), an inversion type channel region and the drift layer (2),
wherein the inversion type channel region is provided in a portion of the base region (3) positioned on a side of the trench (6) by controlling a voltage applied to the gate electrode (9),
wherein the inversion type semiconductor switching element further includes: a plurality of deep layers (10) having the second conductivity type,

wherein each deep layer (10) is disposed in an upper portion of the drift layer (2) below the base region (3), has a depth deeper than the trench (6), and extends along a second direction, which crosses the first direction, and

wherein a whole of or a part of one of the deep layers (10) is spaced apart from the trench (6).

[Claim 2] The silicon carbide semiconductor device according to claim 1, wherein a whole of or a part of each deep layer (10) is spaced apart from the trench (6).

[Claim 3] The silicon carbide semiconductor device according to claim 2, wherein each deep layer (10) is spaced apart from a sidewall of the trench (6) by a first predetermined distance.

[Claim 4] The silicon carbide semiconductor device according to claim 3, wherein each deep layers (10) has a lower layer region and an upper layer region, and

wherein the upper layer region of each deep layer (10) is spaced apart from the sidewall of the trench (6) by the first predetermined distance.

[Claim 5] The silicon carbide semiconductor device according to claim 3 or 4, wherein the inversion type semiconductor switching element further includes a current diffusion layer (2a), which is disposed between the sidewall of the trench (6) and the deep layer (10), and

wherein the current diffusion layer (2a) has an impurity concentration higher than the drift layer (2), which is located below the deeper layer (10).

[Claim 6] The silicon carbide semiconductor device according to any one of claims 2 to 5,

wherein each deep layer (10) is spaced apart from a bottom of the trench (6) by a second predetermined distance.

[Claim 7] The silicon carbide semiconductor device according to claim 6, wherein each deep layer (10) has a lower layer region and an upper layer region and,

wherein the lower layer region of each deep layer (10) is spaced apart from the bottom portion of the trench (6) by the second predetermined distance.

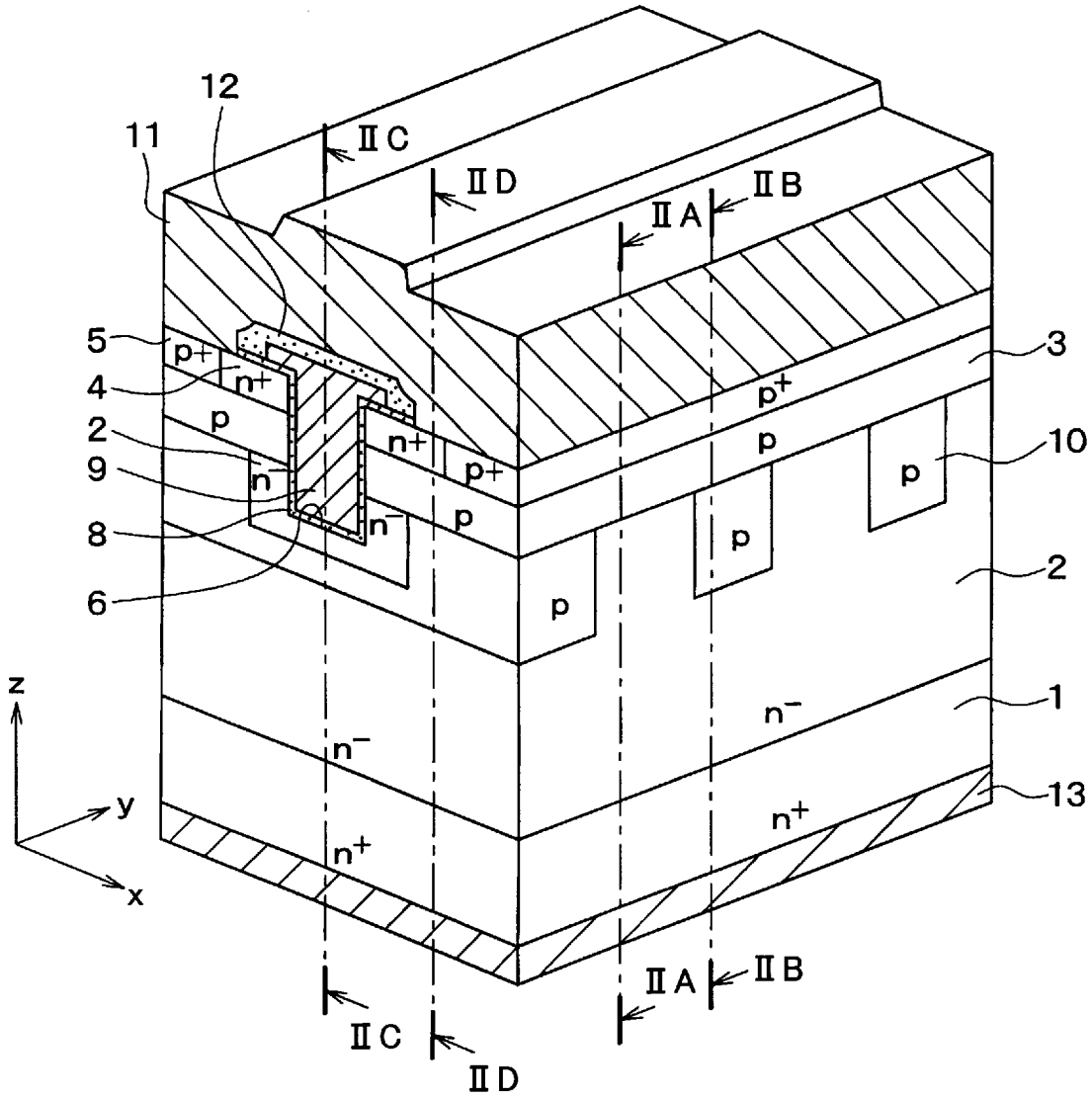
[Claim 8] The silicon carbide semiconductor device according to any one of claims 1 to 7,

wherein each deep layer (10) is electrically coupled with the base region (3).

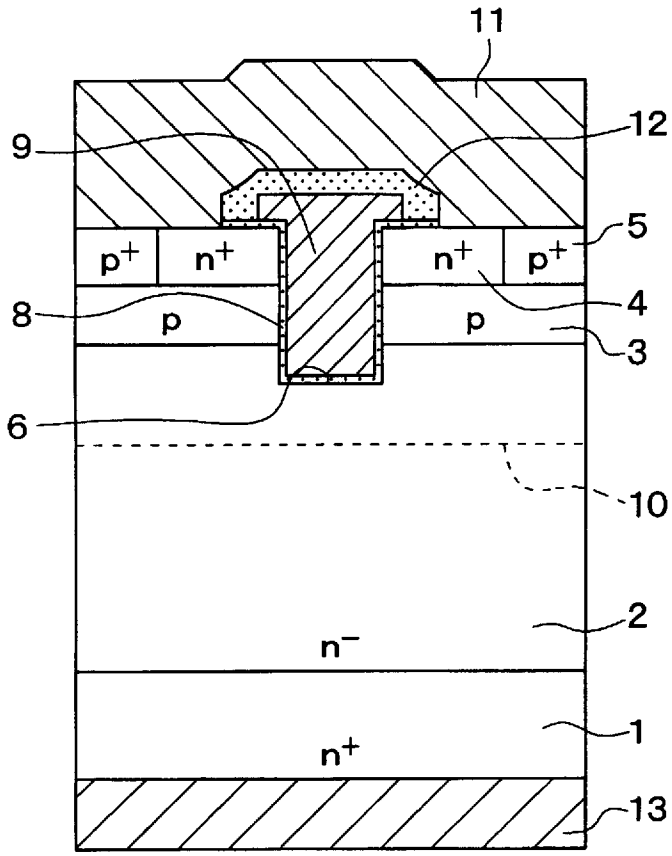
[Claim 9] The silicon carbide semiconductor device according to claim 2, wherein a portion of the drift layer (2) is disposed between the trench (6) and each deep layer (10) so that the whole of or the part of the deep layer (10) is spaced apart from the trench (6).

[Claim 10] The silicon carbide semiconductor device according to claim 9, wherein the portion of the drift layer (2) covers a sidewall and a bottom of the trench (6) so that the whole of the deep layer (10) is spaced apart from the trench (6).

[Fig. 1]


12
11
ⅡC
ⅡD
ⅡA
ⅡB
5
p+
4
n+
2
9
8
6
p
n
n+
p+
n−
p
3
p+
p
10
p
p
p
2
n−
1
n−
n+
13
n+
z
y
x
ⅡA
ⅡB
ⅡC
ⅡD

[Fig. 2A]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12
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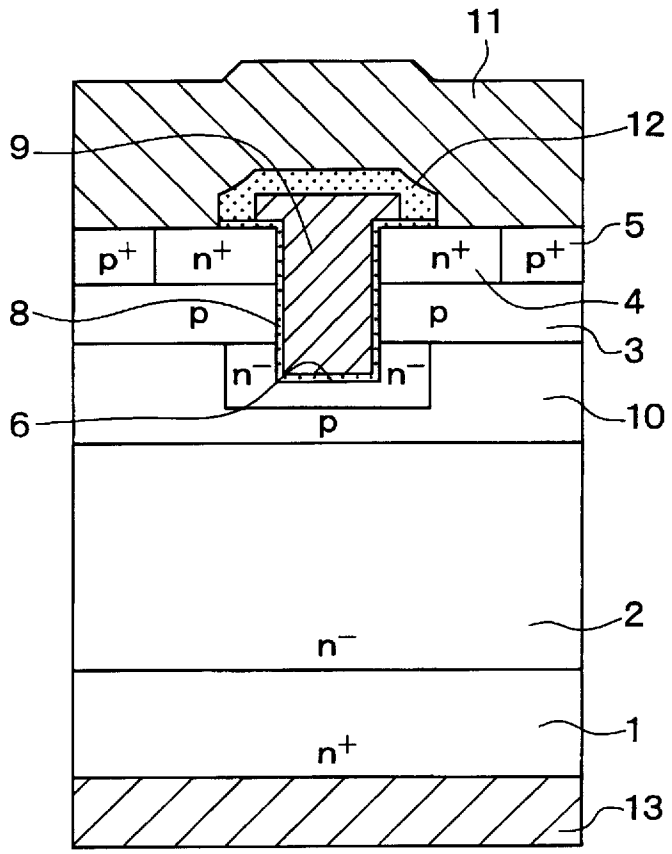
p+
n+
n+
p+
8
p
p
4
3
6
10
2
n−
1
n+
13

[Fig. 2B]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9
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5
p+
n+
n+
p+
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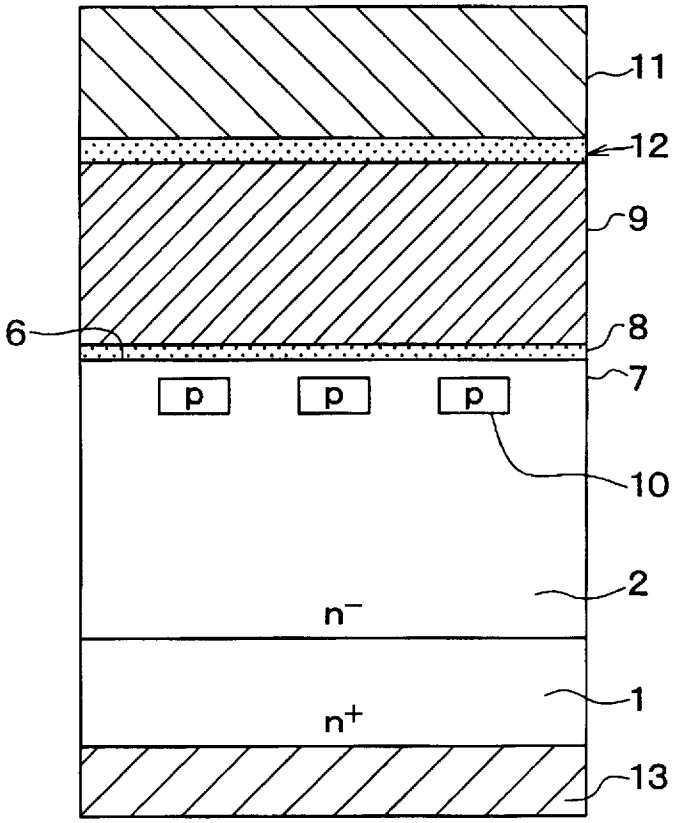
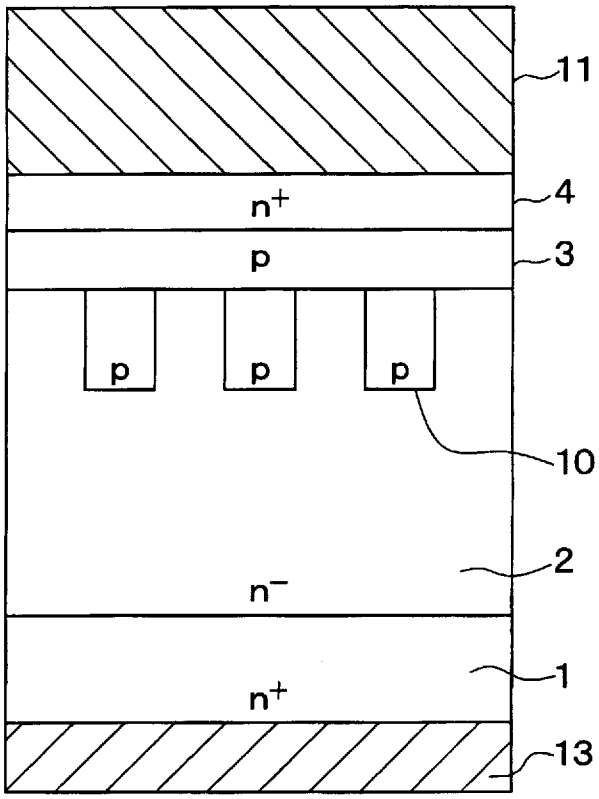
p
4
3
n−
n−
6
p
10
2
n−
1
n+
13

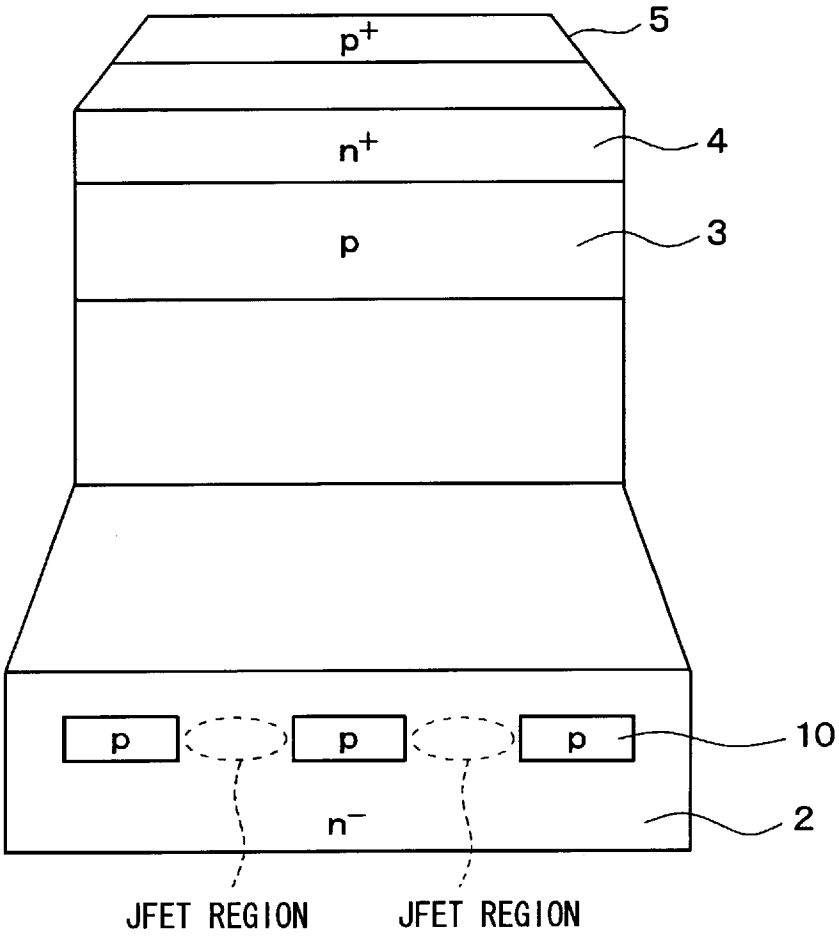
[Fig. 2C]



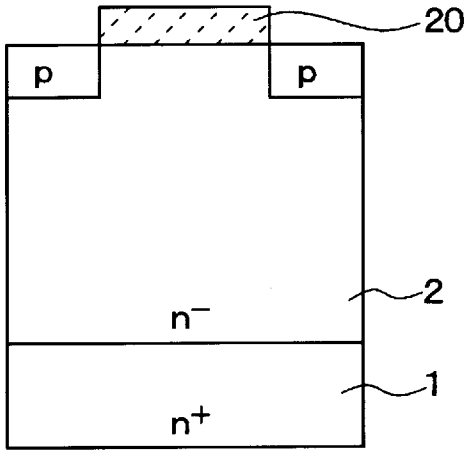
[Fig. 2D]



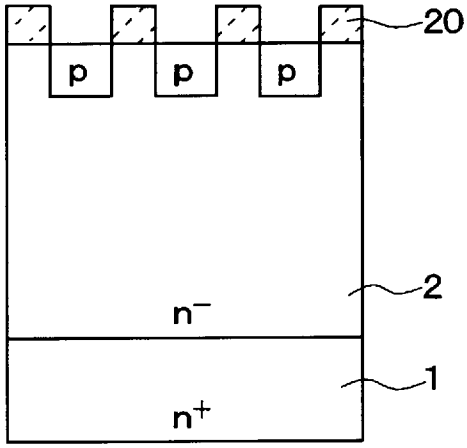
[Fig. 3]



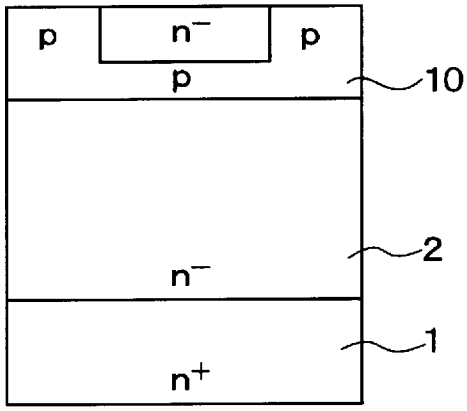
[Fig. 4A]



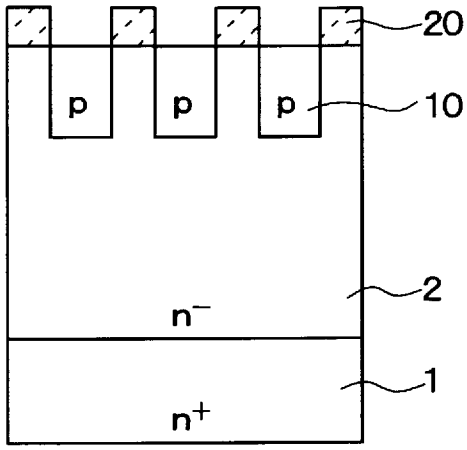
[Fig. 4B]



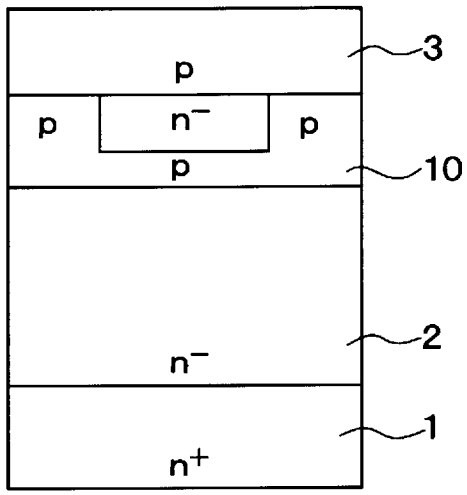
[Fig. 4C]



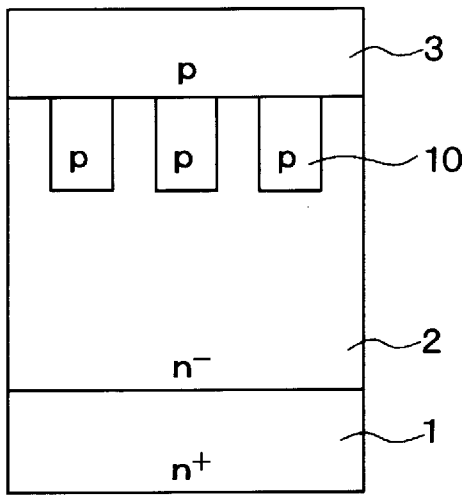
[Fig. 4D]



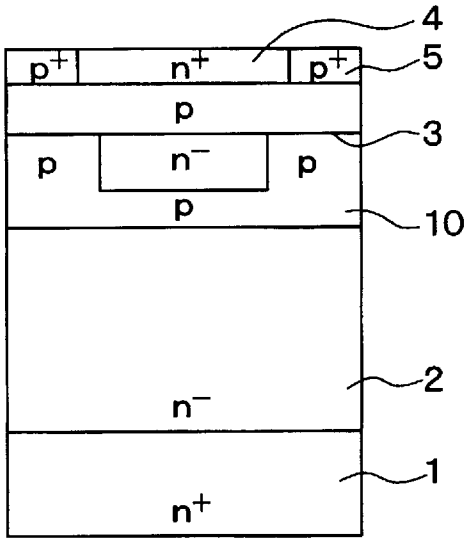
[Fig. 4E]



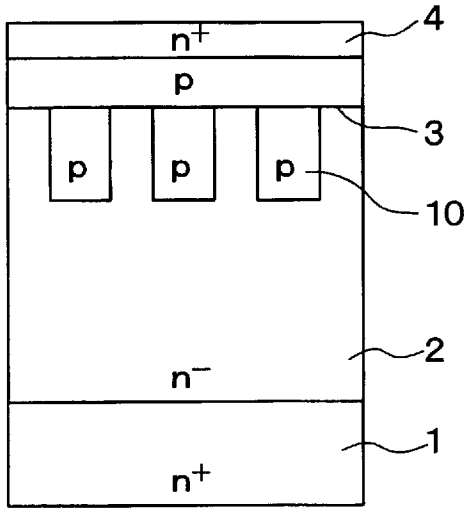
[Fig. 4F]



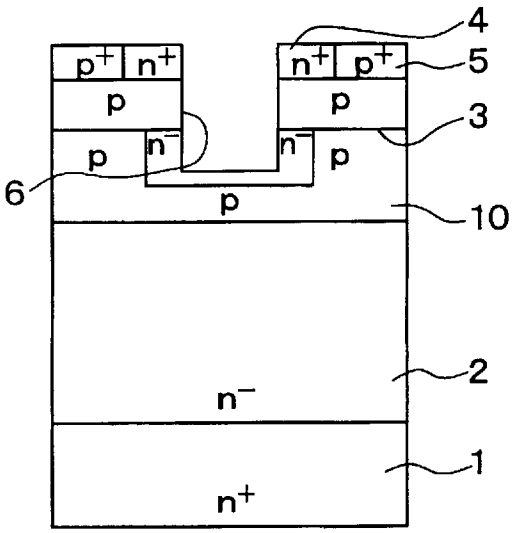
[Fig. 5A]



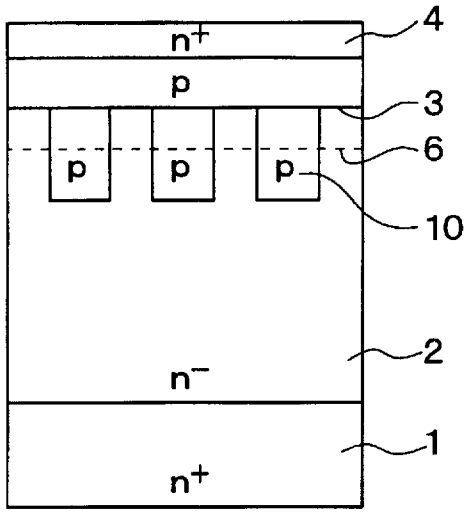
[Fig. 5B]



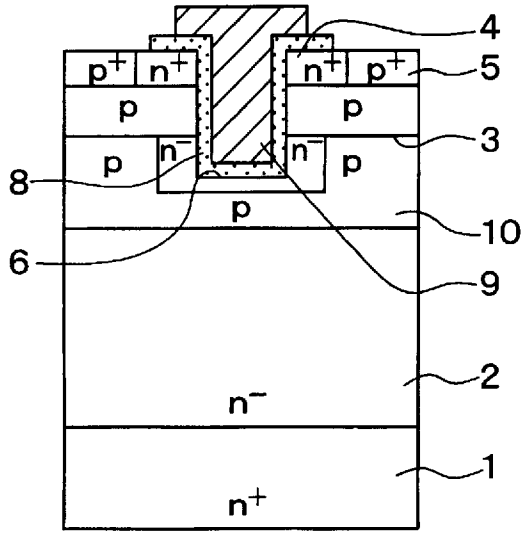
[Fig. 5C]



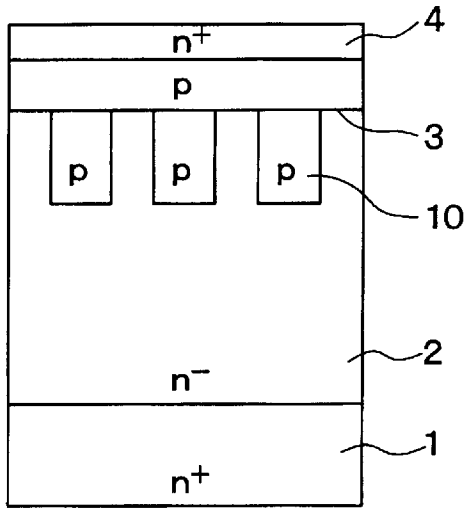
[Fig. 5D]



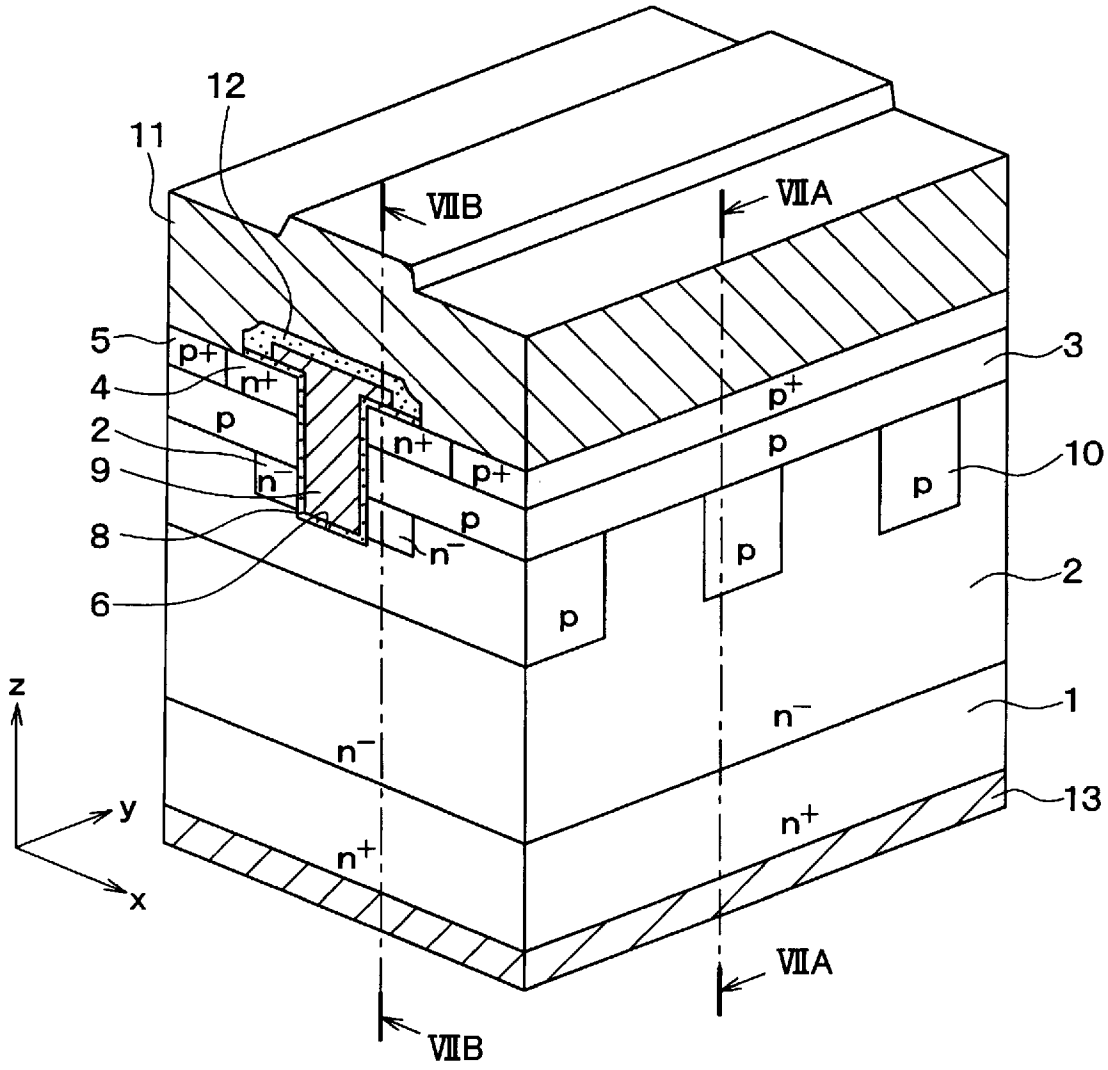
[Fig. 5E]



[Fig. 5F]



[Fig. 6]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p+
p
p
p
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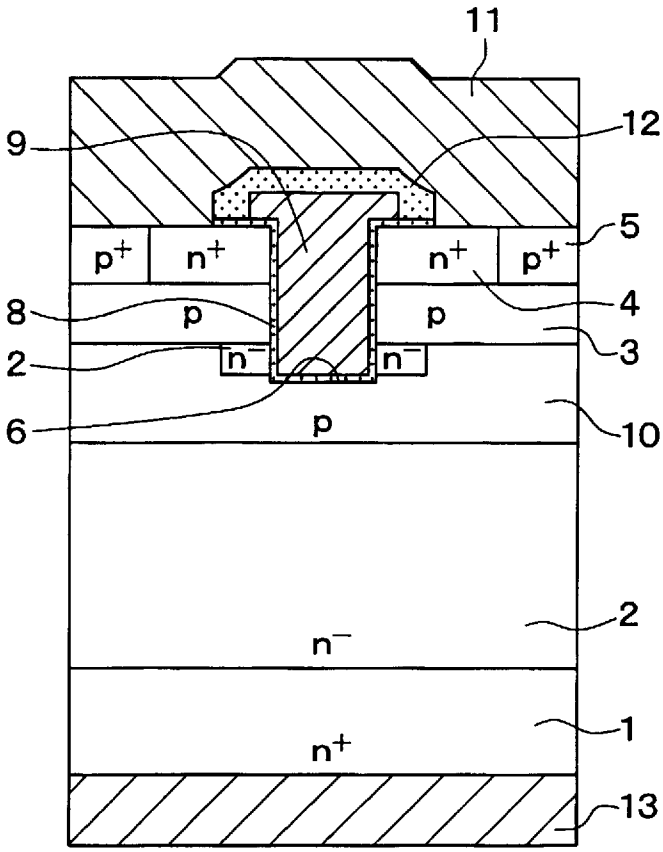
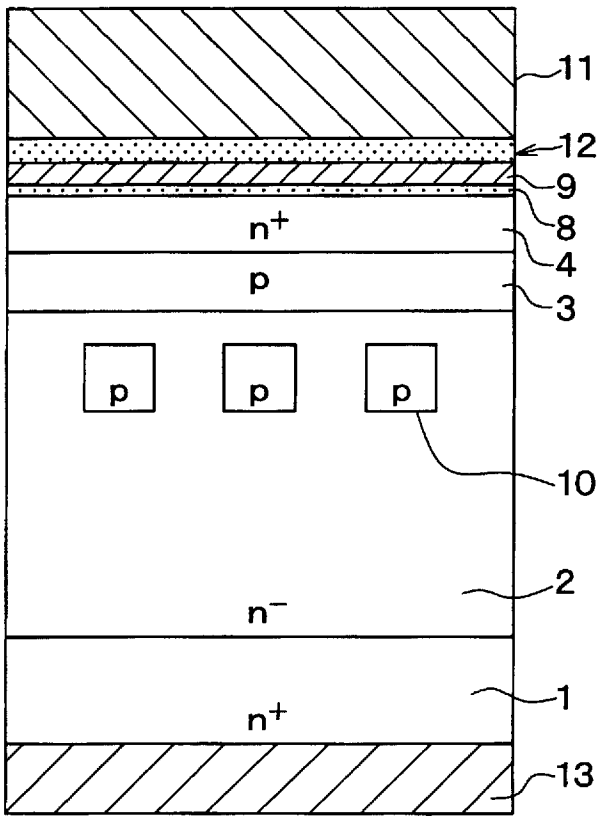
n−
n+
n+
z
y
x
VIIA
VIIB

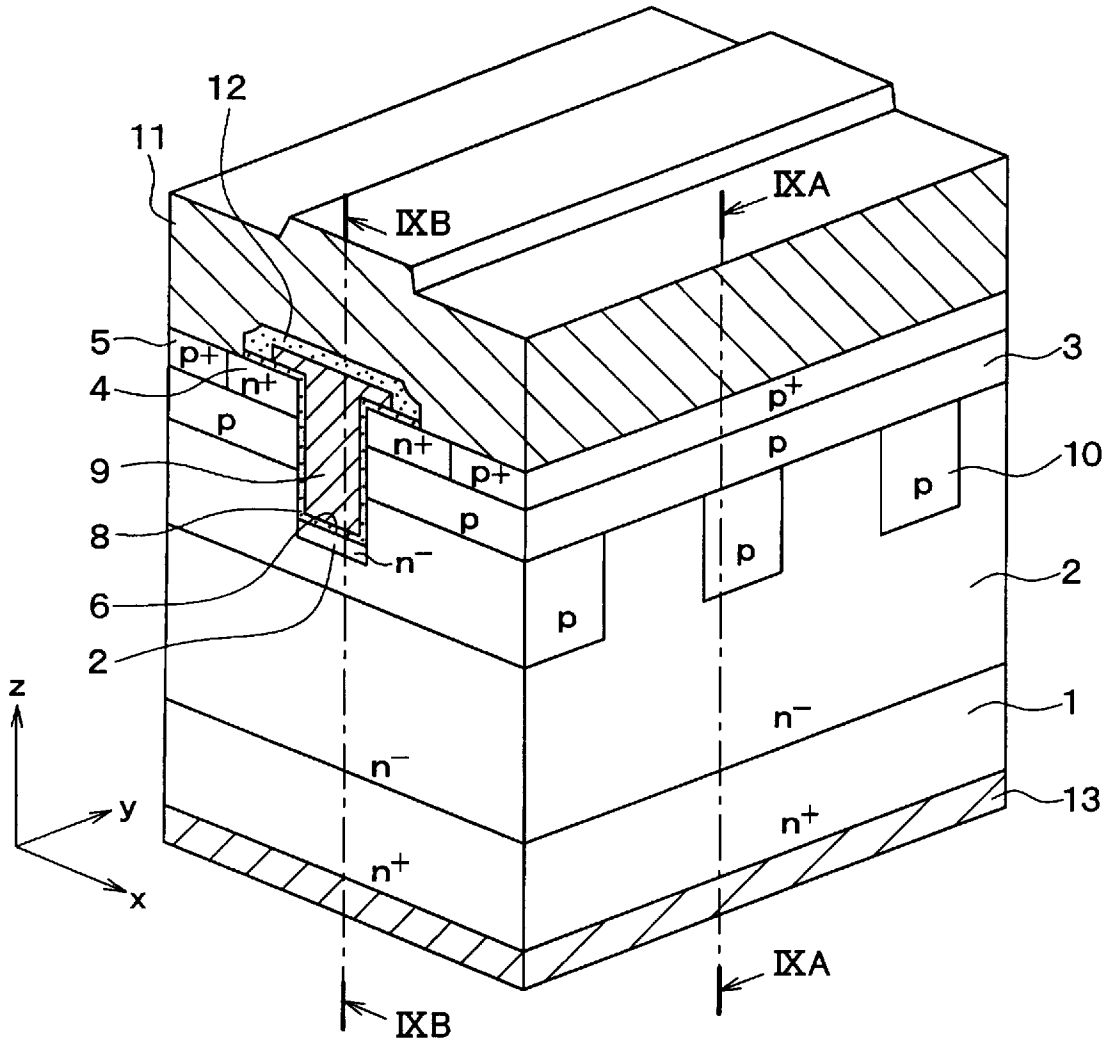
[Fig. 7A]



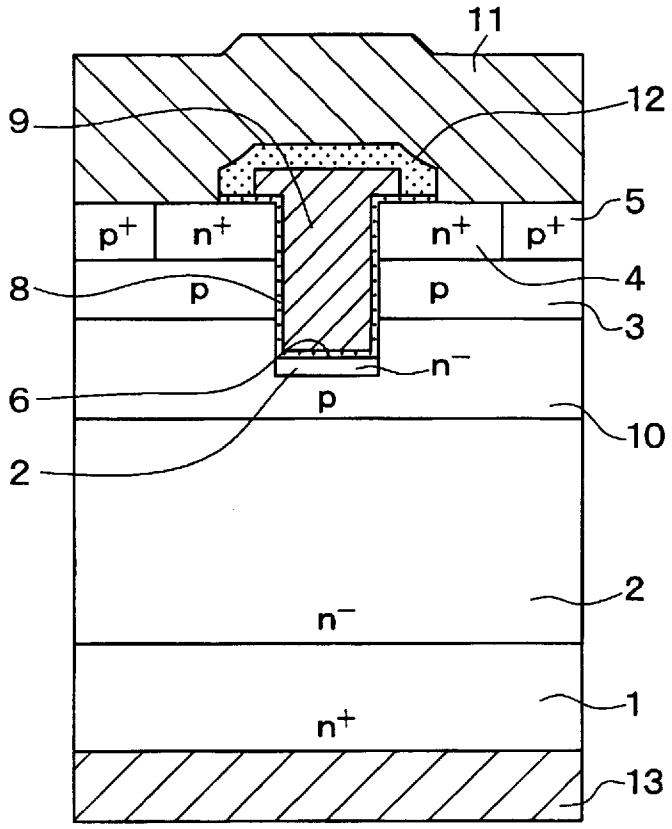
[Fig. 7B]



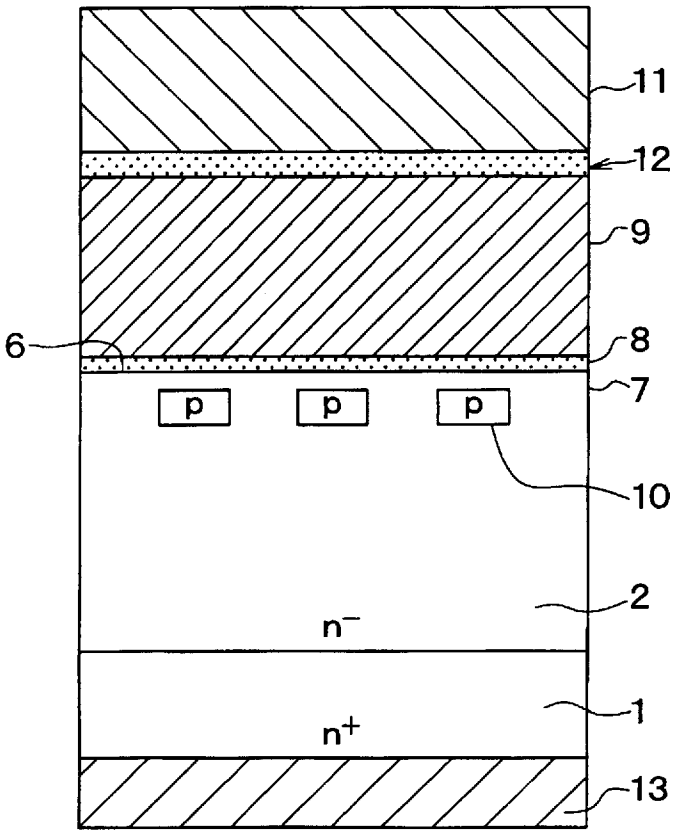
[Fig. 8]



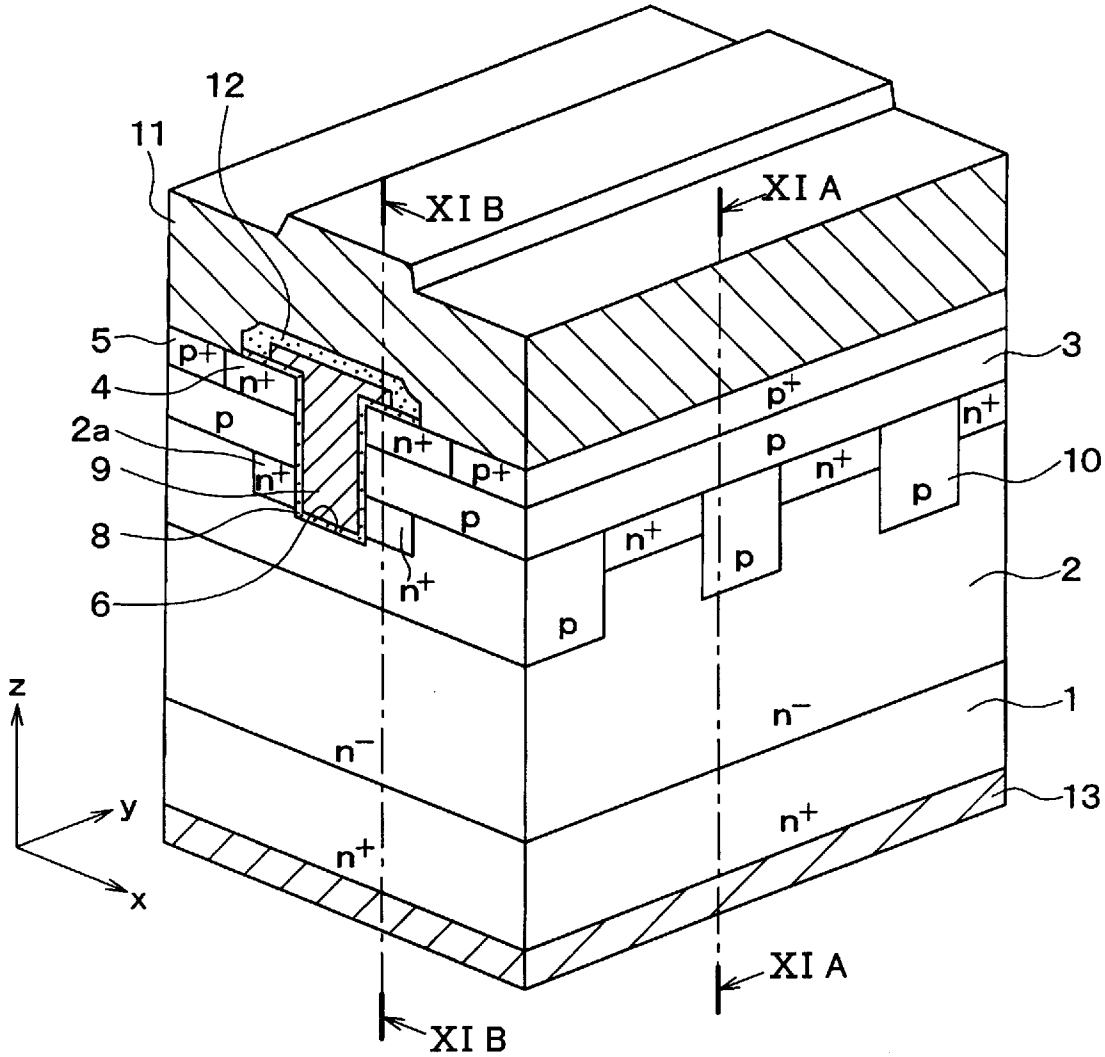
[Fig. 9A]



[Fig. 9B]



[Fig. 10]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n+
p
p+
n+
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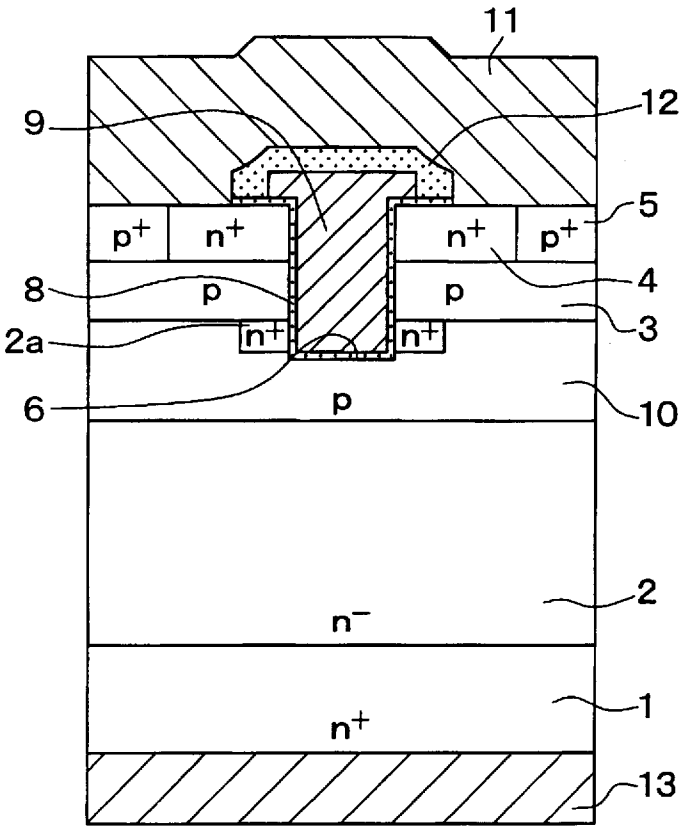
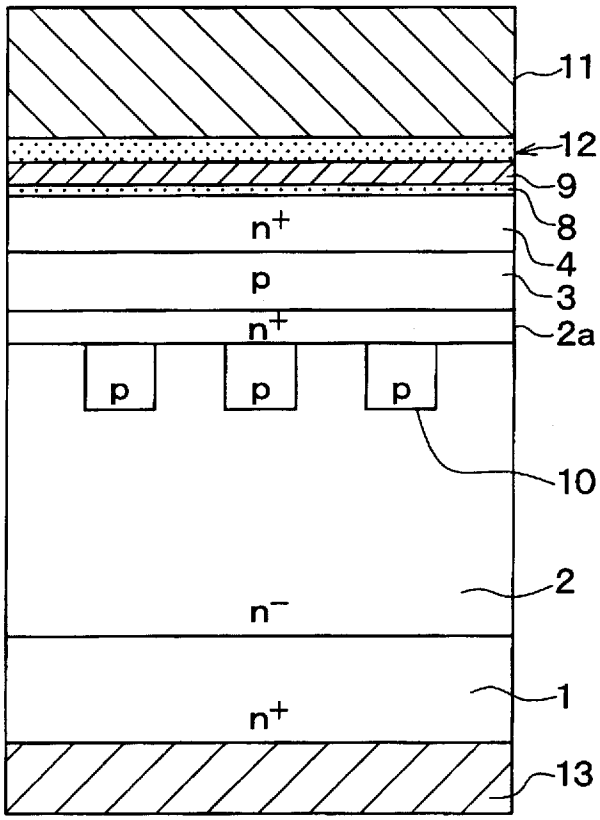
n+
z
y
x
XI A
XI B

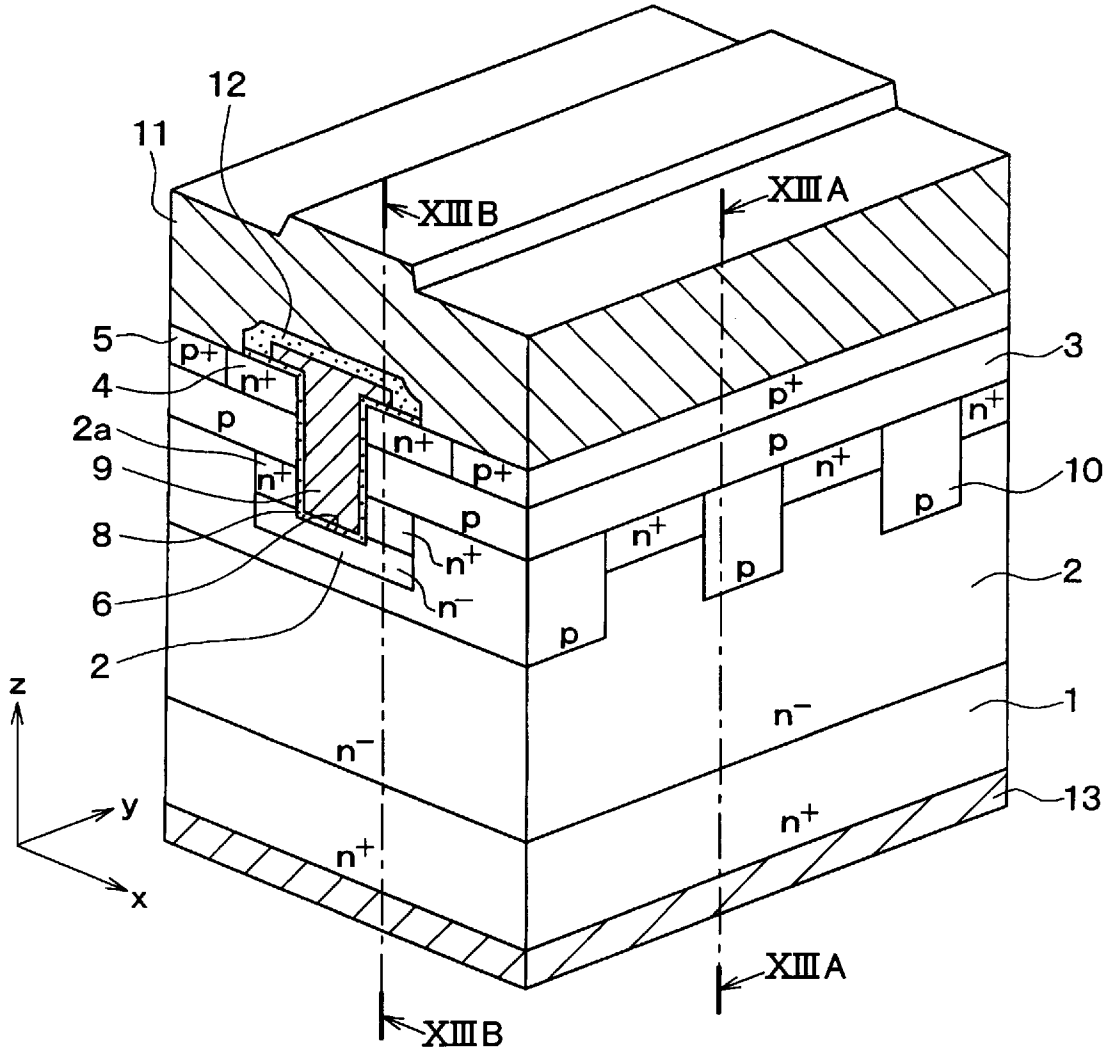
[Fig. 11A]



[Fig. 11B]



[Fig. 12]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XIIIA
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n+
2a
p
9
n+
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n+
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n+
n−
p
n+
p
n+
p
p+
n+
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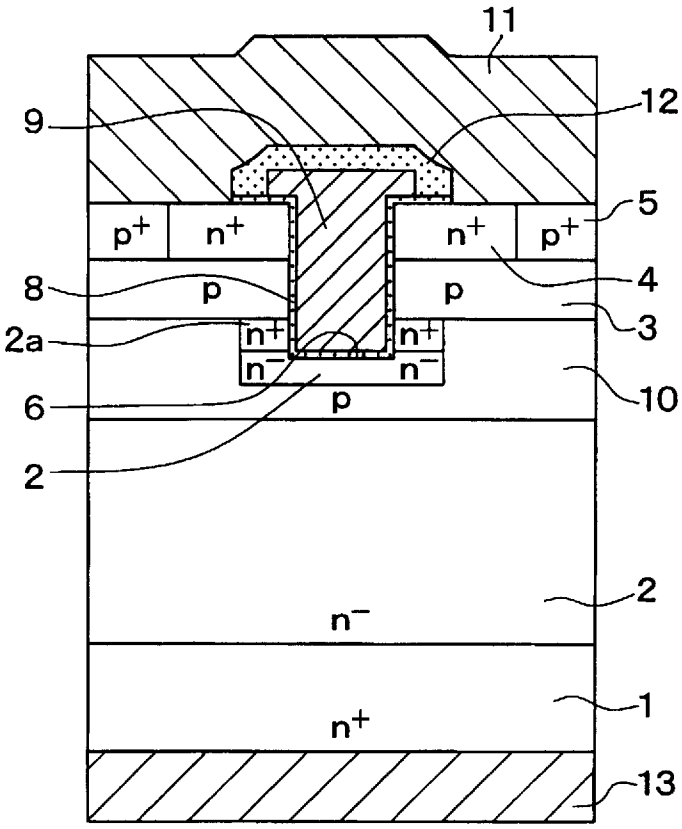
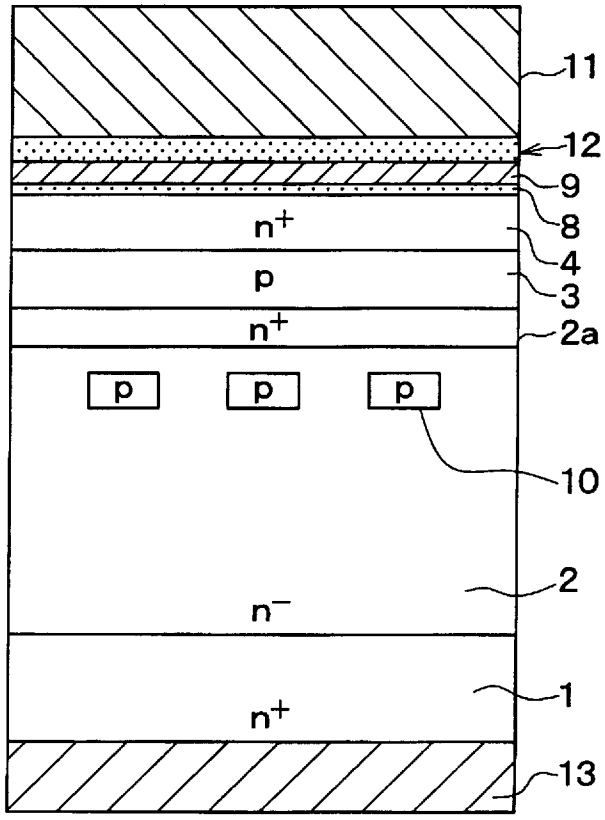
n+
n+
z
y
x
XIIIA
XIIIB

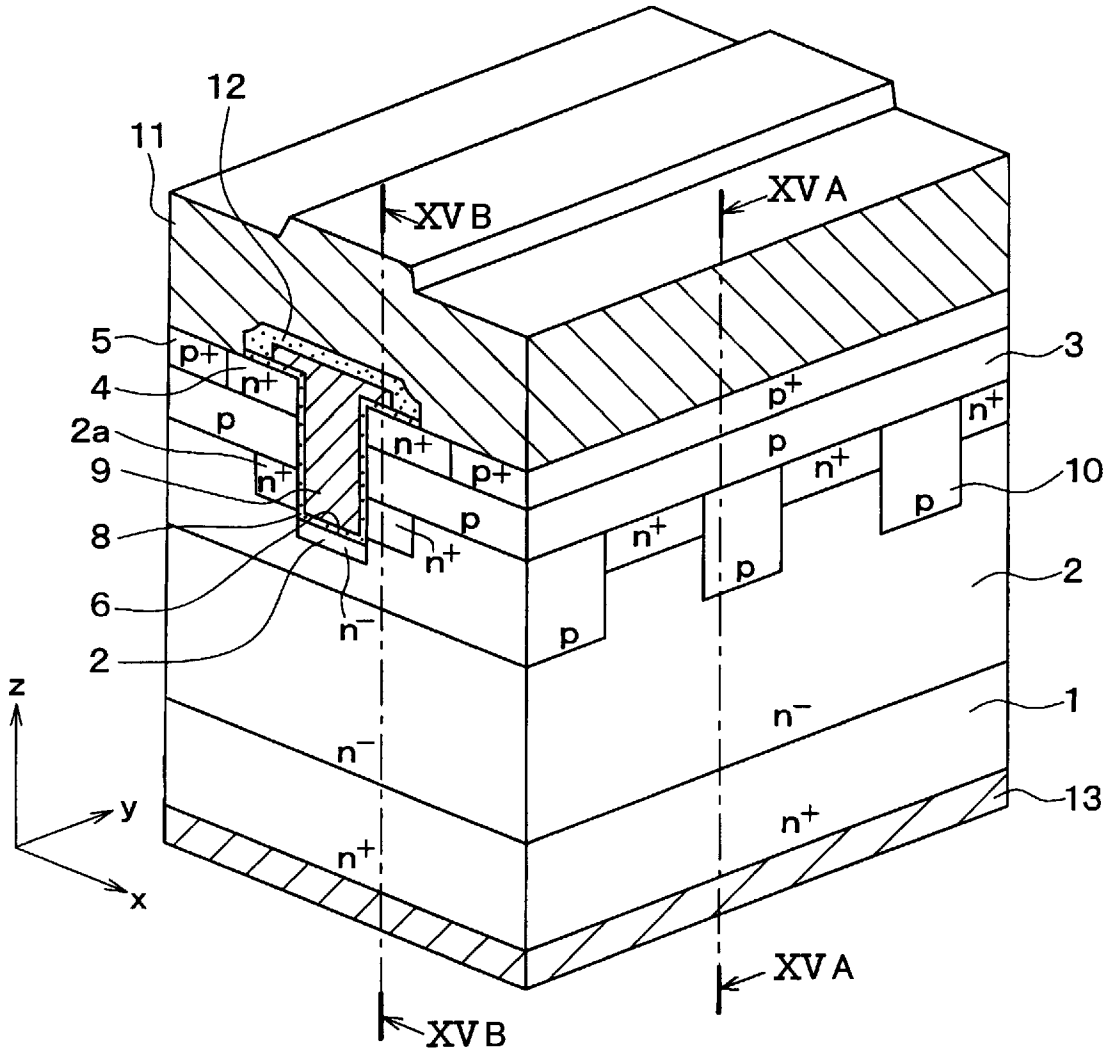
[Fig. 13A]



[Fig. 13B]



[Fig. 14]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p+
n+
p
n−
p
p+
n+
p
n+
p
n+
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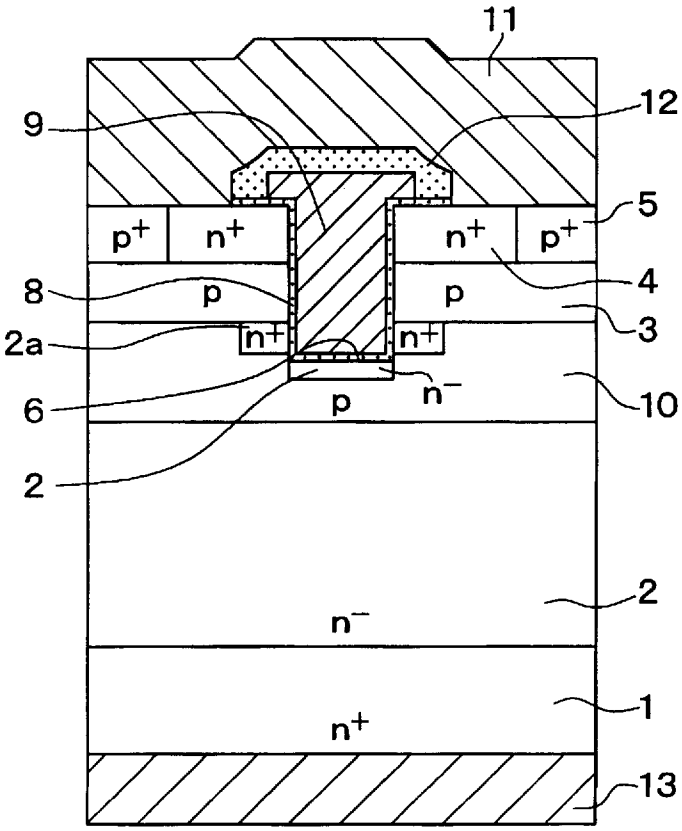
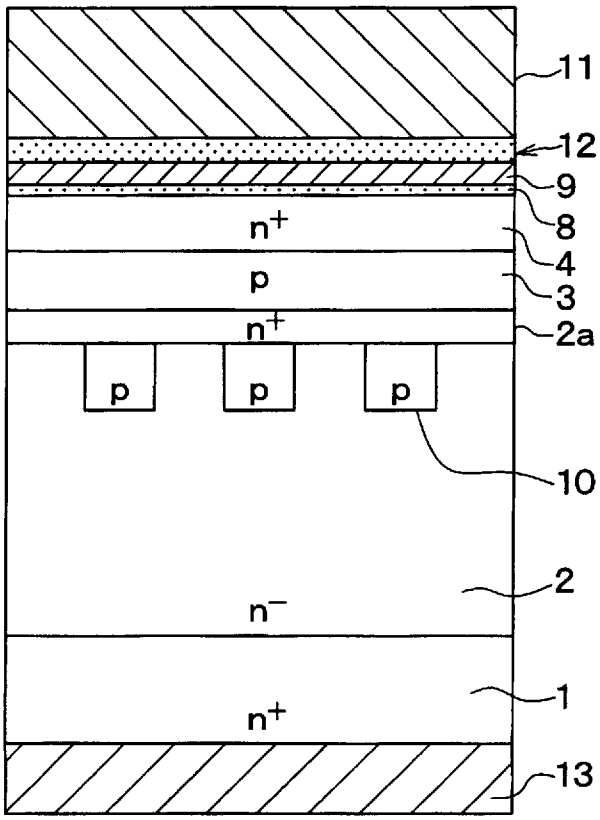
n−
n+
n+
z
y
x
XV A
XV B

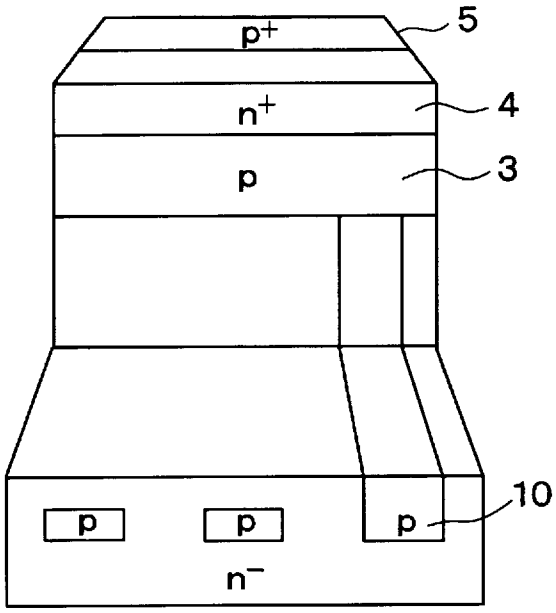
[Fig. 15A]



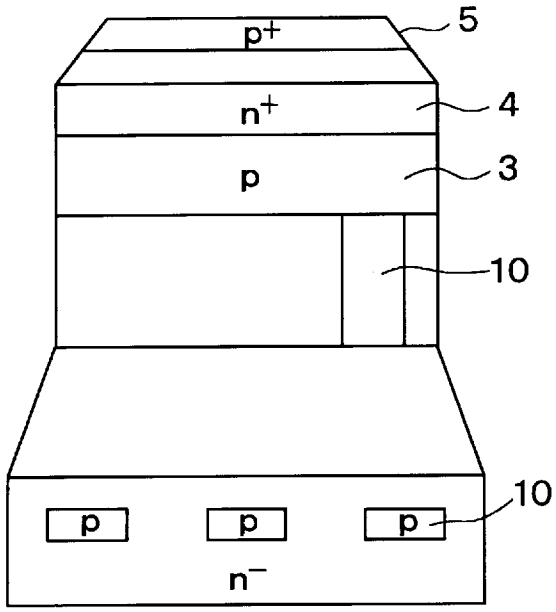
[Fig. 15B]



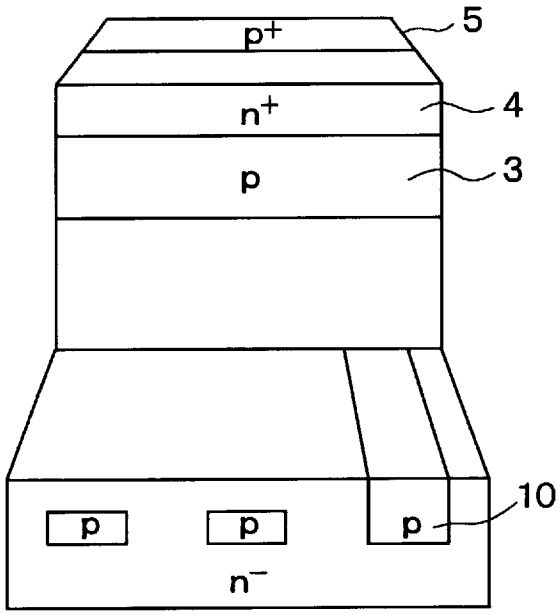
[Fig. 16A]



[Fig. 16B]



[Fig. 16C]



INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2012/000767

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/10 H01L29/16 H01L29/78 H01L29/739
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 10 2007 044209 A1 (INFINEON TECHNOLOGIES AUSTRIA [AT]) 19 March 2009 (2009-03-19) paragraph [0020] - paragraph [0033]; figures 1,2	1-4,6-10
X	JP 2004 200441 A (TOYOTA CENTRAL RES & DEV) 15 July 2004 (2004-07-15) abstract; figures 11,12,13	1-8
A	US 2008/017897 A1 (SAITO WATARU [JP] ET AL) 24 January 2008 (2008-01-24) paragraph [0041] - paragraph [0063]; figures 1A-4B paragraph [0174]	1-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 May 2012	11/05/2012

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Lantier, Roberta

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/JP2012/000767

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 102007044209 A1	19-03-2009	NONE	
JP 2004200441 A	15-07-2004	NONE	
US 2008017897 A1	24-01-2008	NONE	