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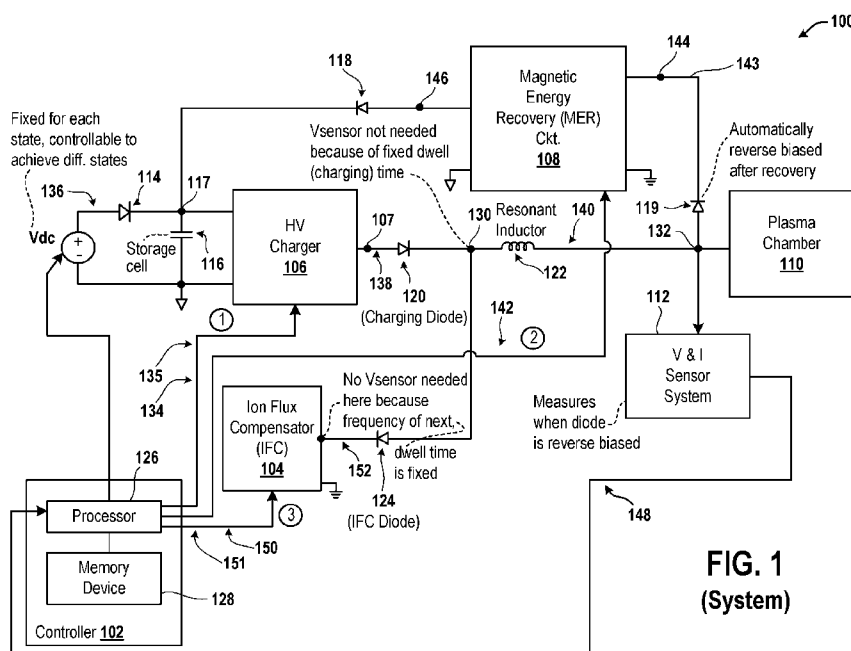


FIG. 1
(System)

(57) Abstract: Systems and methods for orthogonal control of Ion energy for High Aspect Ratio (HAR) etching are described. One of the methods includes controlling a charger circuit to provide radio frequency power to an electrode of a plasma chamber. The method further includes determining whether a predetermined charging time has passed after controlling the charger circuit and controlling a magnetic energy recovery circuit to recover radio frequency energy from the plasma chamber in response to determining that the predetermined charging time has passed. The method includes identifying whether a predetermined voltage associated with use of the magnetic energy recovery circuit is achieved after controlling the magnetic energy recovery circuit and controlling an ion flux compensation circuit to tune the ion flux within the plasma chamber in response to determining that the predetermined voltage is achieved.

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SYSTEMS AND METHODS FOR ORTHOGONAL CONTROL OF ION ENERGY FOR HAR ETCHING

Field

[0001] The present embodiments relate to systems and methods for orthogonal control of Ion energy for High Aspect Ratio (HAR) etching.

Background

[0002] The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0003] In a plasma processing system, a radio frequency (RF) generator is provided. The RF generator is coupled to a plasma chamber in which a semiconductor wafer is placed. The RF generator generates an RF signal that is provided to the plasma chamber for processing the semiconductor wafer. However, due to a change in an impedance of plasma, it is difficult to process the semiconductor wafer in a desirable manner.

Summary

[0004] Embodiments of the disclosure provide systems, apparatus, methods and computer programs for orthogonal control of Ion energy for High Aspect Ratio (HAR) etching. It should be appreciated that the present embodiments can be implemented in numerous ways, e.g., a process, an apparatus, a system, a device, or a method on a computer readable medium. Several embodiments are described below.

[0005] In an embodiment, a system for tuning ion flux is described. The system includes a bias voltage power supply and an energy storage circuit. The bias voltage power supply includes three plasma components, such as a fast high voltage (HV) charger, a magnetic energy recovery circuit, and an ion flux compensator. The fast HV charger generates a signal for charging a plasma load. After the plasma load is charged, energy from the plasma load is recovered by the magnetic energy recovery circuit to charge the energy storage circuit. Once the plasma load is discharged, the ion flux compensator compensates for ion flux to achieve a high aspect ratio (HAR) etch.

[0006] Also, in one embodiment, the fast HV charger excludes any switches.

[0007] In an embodiment, the bias voltage power supply that generates a tailored waveform to achieve desired ion energy distribution for high aspect ratio semiconductor etching

is described. The fast HV charger is a fast high voltage direct current (HVDC) charger, including HVDC power supplies, that provides resonant charging to the plasma load. After charging, the plasma load is discharged, and radio frequency (RF) energy is recovered using the magnetic energy recovery circuit. In addition to energy recovery (ER), the magnetic energy recovery circuit sets a bus to a reference potential. Subsequently, the ion flux compensator provides additional control to tune a sheath potential in a desired manner.

[0008] In an embodiment, the HV charger generates an HVDC output with fast rise time when turned on. A charging diode followed by a resonant inductor is connected in series with the HV charger to provide resonant charging to the plasma load. The system remains in this state until a specified dwell time, such as a fixed amount of dwell time. After the charging is completed, the HV charger generates a negative bias voltage to turn off the charging diode by making it reverse biased. The magnetic energy recovery circuit is turned on, which discharges the RF energy from the plasma load while recovering and feeding the RF energy to the energy storage circuit. Once the plasma load is discharged to substantially zero, such as zero, the ion flux compensator activates. The ion flux compensator includes a pulser, such as a fast HVDC source, in series with a resistor-inductor-diode (RLD) circuit. The pulser generates a high voltage to provide power for tuning the ion flux. Once the ion flux compensation is complete, the pulser generates a negative bias to make the ion flux compensator ineffective by reverse biasing an IFC diode.

[0009] In one embodiment, a method for tuning ion flux is described. The method includes controlling a charger circuit to provide radio frequency power to an electrode of a plasma chamber. The method further includes determining whether a predetermined charging time has passed after controlling the charger circuit and controlling a magnetic energy recovery circuit to recover radio frequency energy from the plasma chamber in response to determining that the predetermined charging time has passed. The method includes identifying whether a predetermined voltage associated with use of the magnetic energy recovery circuit is achieved after controlling the magnetic energy recovery circuit and controlling an ion flux compensation circuit to tune the ion flux within the plasma chamber in response to determining that the predetermined voltage is achieved.

[0010] In one embodiment, a controller for operating a plasma system to tune ion flux is described. The controller includes a processor that controls control a charger circuit to provide radio frequency power to an electrode of a plasma chamber. The processor determines whether a predetermined charging time has passed after the charger circuit is controlled. The processor controls a magnetic energy recovery circuit to recover radio frequency energy from the plasma chamber when it is determined that the predetermined charging time has passed. The

processor identifies whether a predetermined voltage associated with use of the magnetic energy recovery circuit is achieved after the magnetic energy recovery circuit is controlled. The processor controls an ion flux compensation circuit to tune the ion flux within the plasma chamber when it is determined that the predetermined voltage is achieved. The controller includes a memory device coupled to the processor.

[0011] In an embodiment, a plasma system for tuning ion flux is described. The plasma system includes a plasma chamber having an electrode and a charger circuit coupled to the plasma chamber. The charger circuit provides radio frequency power to the electrode. The plasma system also includes a magnetic energy recovery circuit coupled to the charger circuit, an ion flux compensation circuit coupled to the magnetic energy recovery circuit, and a controller. The controller is coupled to the charger circuit, the magnetic energy recovery circuit, and the ion flux compensation circuit. The controller determines whether a predetermined charging time has passed after the charger circuit provides the radio frequency power. The controller controls the magnetic energy recovery circuit to recover radio frequency energy from the plasma chamber when it is determined that the predetermined charging time has passed. The controller identifies whether a predetermined voltage associated with use of the magnetic energy recovery circuit is achieved after the magnetic energy recovery circuit is controlled. The controller controls the ion flux compensation circuit to tune the ion flux within the plasma chamber when it is determined that the predetermined voltage is achieved.

[0012] Some advantages of the herein described systems and methods include providing a combination of charging the plasma load followed by the magnetic energy recovery, which is followed by ion flux compensation to achieve a high aspect ratio etch. Charge stored within the plasma chamber is recovered by the energy recovery circuit. The recovered energy is then used during a next cycle of operation of the system. Also, after the plasma load is discharged, ion flux is tuned within the plasma chamber to achieve the high aspect ratio etch.

[0013] Other aspects will become apparent from the following detailed description, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The embodiments may best be understood by reference to the following description taken in conjunction with the accompanying drawings.

[0015] Figure 1 is a diagram of an embodiment of a system to illustrate a cycle of occurrence of charging of a plasma load followed by an occurrence of a magnetic energy recovery, which is followed by an occurrence of ion flux compensation

[0016] Figure 2 is an embodiment of a graph of a tailored waveform to illustrate an occurrence of charging of the plasma load, followed by an occurrence of the magnetic energy recovery, which is followed by an occurrence of the ion flux compensation.

[0017] Figure 3A is an embodiment of a graph to illustrate charging of the plasma load.

[0018] Figure 3B is an embodiment of a graph to illustrate multiple cycles of charging of the plasma load.

[0019] Figure 3C is an embodiment of a graph to illustrate an occurrence of the magnetic energy recovery.

[0020] Figure 3D is an embodiment of a graph to illustrate an occurrence of the ion flux compensation.

[0021] Figure 3E is an embodiment of a graph to illustrate multiple occurrences of the ion flux compensation.

[0022] Figure 4 is a diagram of an embodiment of a system to illustrate details of an ion flux compensator.

[0023] Figure 5 is a diagram of an embodiment of a system to illustrate details of a high voltage (HV) charger.

[0024] Figure 6 provides embodiments of graphs to illustrate wafer voltage, pre-blocking capacitor voltage, current output from the ion flux compensator, voltage output from the ion flux compensator, and voltage output from the HV charger versus time.

[0025] Figure 7 provides embodiments of graphs to illustrate multiple states of a voltage signal output from a direct current (DC) voltage source with respect to a voltage across a pre-blocking capacitor and a wafer potential.

DETAILED DESCRIPTION

[0026] The following embodiments describe systems and methods for orthogonal control of Ion energy for High Aspect Ratio (HAR) etching. It will be apparent that the present embodiments may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present embodiments.

[0027] Figure 1 is a diagram of an embodiment of a system 100 to illustrate a cycle of occurrence of charging of a plasma load followed by an occurrence of a magnetic energy recovery, which is followed by an occurrence of ion flux compensation. The cycle of occurrence of the charging of the plasma load, the occurrence of the magnetic energy recovery, and the occurrence of ion flux compensation repeats for multiple times.

[0028] The system 100 includes a direct current (DC) voltage source V_{DC} , a controller 102, an ion flux compensator (IFC) 104, a high-voltage (HV) charger 106, a magnetic energy recovery (MER) circuit 108, a plasma chamber 110, and a voltage and current (V&I) sensor system 112. The HV charger 106 is sometimes referred to herein as a charger circuit. The system 100 further includes a diode 114, a capacitor 116, a MER diode 119, another diode 118, a charging diode 120, a resonant inductor 122, and an IFC diode 124. The controller 102 includes a processor 126 and a memory device 128. The plasma chamber 110 is an example of the plasma load. The ion flux compensator 104 is sometimes referred to herein as an ion flux compensation circuit. The capacitor 116 is sometimes referred to herein as an energy storage circuit or a storage cell, such as a battery.

[0029] As an example, the controller 102 is a host computer, such as a desktop computer or laptop computer or a smart phone. Examples of the voltage and current sensor system 112 include one or more voltage and current sensors, and voltage sensors and current sensors. An example of the plasma chamber 110 is a capacitively coupled plasma chamber. Another example of the plasma chamber 110 is an inductively coupled plasma chamber.

[0030] The processor 126 is coupled to the memory device 128 and to the DC voltage source V_{dc} . Also, the processor 126 is coupled to the ion flux compensator 104, the HV charger 106, the MER circuit 108, and the V&I sensor system 112. The DC voltage source V_{dc} is coupled to the diode 114 to form a series circuit. The series circuit of the DC voltage source V_{dc} and the diode 114 is coupled in parallel at a point 117 to the capacitor 116. The capacitor 116 is coupled in parallel to the HV charger 106. The capacitor 116 is also coupled to the diode 118, which is coupled to an output 146 of the MER circuit 108. For example, a connection between the MER circuit 108 and the diode 118 and a connection between the diode 118 and the point 117 forms a bus. The HV charger 106 has an output 107 that is coupled in series to the charging diode 120, which is coupled to the IFC diode 124 at a point 130. The IFC diode 124 is coupled to the ion flux compensator 104.

[0031] Also, the point 130 is coupled to the resonant inductor 122, which is coupled to a point 132. The point 132 is sometimes referred to herein as an input of the plasma chamber 110. The point 132 is coupled to the MER diode 119 and to the V&I sensor system 112. The MER diode 119 is coupled to an input 144 of the MER circuit 108 via a high voltage line 143. Also, the point 132 is coupled to the plasma chamber 110. For example, the point 132 is coupled to an electrode, such as a lower electrode or an upper electrode or an RF coil, of the plasma chamber 110.

[0032] To initiate an occurrence of the charging of the plasma load, the processor 126 generates and sends a control signal 134 for a first time to the HV charger 106 to control the

HV charger 106. The control signal 134 indicates a primary amount of voltage, such as a positive voltage, to be output from the HV charger 106. The DC voltage source V_{dc} generates a voltage signal 136 that is applied via the diode 114, which is forward biased, to the HV charger 106. Upon receiving the voltage signal 136 and the control signal 134, the HV charger 106 modifies, such as increases or decreases, a voltage of the voltage signal 136 to output another voltage signal 138 having the primary amount of voltage indicated in the control signal 134. The voltage signal 138 is sent via the charging diode 120, which is forward biased, and the point 130 to the resonant inductor 122. The resonant inductor 122 modifies an impedance of the voltage signal 138 to output a voltage signal 140 having RF power and provides the voltage signal 140 to the electrode of the plasma chamber 110. The voltage signal 140 having the RF power is provided to the electrode of the plasma chamber 110 to charge the plasma load. For example, when one or more process gases, such as fluorine containing gas or an oxygen containing gas or a combination thereof, are supplied to the plasma chamber 110 in addition to the voltage signal 140, plasma is generated or stricken within the plasma chamber 110 to process a substrate placed within the plasma chamber 110. An example of the substrate includes a semiconductor wafer.

[0033] It should be noted that a charging time is fixed. For example, the plasma load is charged for a fixed amount of dwell time during each occurrence of charging. To illustrate, upon receiving the control signal 134 indicating the primary amount of voltage, the HV charger 106 outputs the voltage signal 138 having the primary amount of voltage for the fixed amount of dwell time. When the voltage signal 138 having the primary amount of voltage is generated for the fixed amount of dwell time, the plasma load 110 is charged by the voltage signal 140 for the fixed amount of dwell time during the occurrence of charging. It should be noted that until the plasma load 110 is charged, the MER diode 119 is reversed biased and the point 132 is electrically decoupled from the MER circuit 108. For example, the MER diode 119, when reverse biased, creates an open circuit between the MER circuit 108 and the point 132. Also, during the fixed amount of dwell time, the IFC diode 124 is reverse biased and there is no ion flux compensation by the ion flux compensator 104.

[0034] When the fixed amount of dwell time has passed, the MER diode 119 becomes forward biased, the charging diode 120 becomes reverse biased, and the IFC diode 124 is reverse biased. For example, after the plasma load is charged in the fixed amount of dwell time, a voltage at the point 130 is greater than a voltage at the output 107 of the HV charger 106. To illustrate, after the fixed amount of dwell time has passed, the processor 126 generates a control signal 135 indicating a secondary amount of voltage, such as a negative voltage, to be output from the HV charger 106, and sends the control signal 135 to the HV charger 106. Upon receiving the control signal 135, the HV charger 106 modifies the voltage signal 138 to have the

secondary amount of voltage from the primary amount of voltage. When the voltage signal 138 is modified to have the secondary amount of voltage, the charging diode 120 becomes reverse biased from being forward biased. When the charging diode 120 becomes reversed bias, the plasma load is no longer being charged based on the primary voltage of the voltage signal 138. Also, when the MER diode 119 becomes forward biased, recovery of RF energy stored in the plasma chamber 110 as a result of the charging initiates.

[0035] The processor 126 determines based on a clock that counts whether the fixed amount of dwell time has passed after the control signal 134 is generated. The control signal 134 is generated to control the HV charger 106 to charge the plasma load. The fixed amount of dwell time is sometimes referred to herein as a predetermined charging time. In response to determining that the fixed amount of dwell time has passed, to initiate an occurrence of the magnetic energy recovery, the processor 126 sends a control signal 142 for a first time to the MER circuit 108 to control the MER circuit 108. The MER circuit 108 is controlled to initiate recovery of the RF energy from the plasma chamber 110 via the high voltage line 143. For example, upon receiving the control signal 142, the input 144 of the MER circuit 108 receives RF energy stored within the plasma chamber 110, via the point 132, the high voltage line 143, and the MER diode 119, which is forward biased. When the MER diode 119 becomes forward biased after the fixed amount of dwell time has passed, the RF energy stored in the plasma chamber 110 is recovered by the MER circuit 108 via the point 132, the high voltage line 143, and the MER diode 119. The processor 126 controls one or more switches of the MER circuit 108 to store the RF energy in one or more inductors of the MER circuit 108. The processor 126 further controls the one or more switches of the MER circuit 108 to transfer the RF energy stored in the one or more inductors via the diode 118, which is forward biased, and the output 146 to the capacitor 116. The RF energy stored in the one or more inductors is output from the MER circuit 108 and transferred to the capacitor 116. The RF energy is transferred to the capacitor 116 for storage of the RF energy within the capacitor 116. The RF energy that is transferred via the bus to the capacitor 116 creates a reference potential at the bus. The RF energy is stored in the capacitor 116 during the occurrence of the magnetic energy recovery.

[0036] When the magnetic energy is recovered, the capacitor 116 is charged and the MER diode 119 becomes reversed biased after being forward biased. The V&I sensor system 112 measures a voltage at the point 132 to output a measurement signal 148 and sends the measurement signal 148 to the processor 126. The processor 126 determines, based on the measurement signal 148, whether the voltage at the point 132 is less than a predetermined threshold. For example, the processor 126 compares the voltage indicated by the measurement signal 148 with the predetermined threshold to determine whether the voltage is lower than the

predetermined threshold. The predetermined threshold is an example of a predetermined voltage that is associated with use of the MER circuit 108. To illustrate, the predetermined threshold is achieved after RF energy is recovered from the plasma chamber 110 by using the MER circuit 108. Upon determining that the voltage at the point 132 is less than the predetermined threshold, the processor 126 determines that the MER diode 119 is reversed biased. When it is determined that the MER diode 119 is reversed biased, the processor 126 determines to initiate an occurrence of the ion flux compensation. The occurrence of the ion flux compensation is initiated to control the ion flux of plasma within the plasma chamber 110. Also, after the magnetic energy is recovered, the charging diode 120 is still reverse biased and the IFC diode 124 becomes forward biased.

[0037] To initiate the occurrence of the ion flux compensation, the processor 126 sends a control signal 150 for a first time to the ion flux compensator 104 to control an amount of voltage that is output from the ion flux compensator 104. In response to receiving the control signal 150, the ion flux compensator 104 achieves the amount of voltage indicated within the control signal 150 to generate a current signal 152. The current signal 152 is sent from the ion flux compensator 104 via the diode 124, which is forward biased, the point 130, and the resonant inductor 122 to the plasma chamber 110.

[0038] When the current signal 152 is sent, ion flux compensation is achieved. For example, ion flux of plasma within the plasma chamber 110 is tuned, such as modified, with a change in an amount of current of the current signal 152. To illustrate, the processor 126 identifies from, within the memory device 128, that a first amount of voltage to be applied by the ion flux compensator 104 corresponds to a first amount of current of the current signal 152, a second amount of voltage to be applied by the ion flux compensator 104 corresponds to a second amount of current of the current signal 152, and a third amount of voltage to be applied by the ion flux compensator 104 corresponds to a third amount of current of the current signal 152. The second amount of voltage is greater than the first amount of voltage and the third amount of voltage is less than the first amount of voltage. Also, the second amount of current is greater than the first amount of current and the third amount of current is less than the first amount of current. The processor 126 determines that the first amount of current is to be output from the ion flux compensator 104 and indicates, within the control signal 150, the first amount of voltage, corresponding to the first amount of current, is to be applied by the ion flux compensator 104. Upon receiving the control signal 150 indicating the first amount of voltage, the ion flux compensator 104 applies the first amount of voltage to output the current signal 152 having the first amount of current. To tune, such as increase the ion flux, the processor 126 determines that the second amount of current is to be output from the ion flux compensator 104

and indicates, within the control signal 150, the second amount of voltage, corresponding to the second amount of current, is to be applied by the ion flux compensator 104. Upon receiving the control signal 150 indicating the second amount of voltage, the ion flux compensator 104 applies the second amount of voltage to output the current signal 152 having the second amount of current. Also, to tune, such as decrease the ion flux, the processor 126 determines that the third amount of current is to be output from the ion flux compensator 104 and indicates, within the control signal 150, the third amount of voltage, corresponding to the third amount of current, is to be applied by the ion flux compensator 104. Upon receiving the control signal 150 indicating the third amount of voltage, the ion flux compensator 104 applies the third amount of voltage to output the current signal 152 having the third amount of current.

[0039] The ion flux compensation occurs until a next occurrence of charging of the plasma load. For example, the ion flux compensation occurs until the processor 126 sends the control signal 134 to the DC voltage source Vdc for a second time and until the processor 126 sends another control signal 151 to the ion flux compensator 104. The control signal 151 is sent to the ion flux compensator 104 to reverse bias the IFC diode 124 to electrically decouple the ion flux compensator 104 from the plasma load. After sending the control signal 134 for the second time to charge the plasma load, the processor 126 sends the control signal 142 to the MER circuit 108 for a second time to recover RF energy from the plasma chamber 110 for the second time. It should be noted that the RF energy stored in the capacitor 116 during the first time of occurrence of the magnetic energy recovery is used to charge the plasma load for the second time. For example, the charge stored in the capacitor 116 based on the RF energy recovered from the plasma chamber 110 during the first time of occurrence of the magnetic energy recovery creates a voltage at the point 117. The voltage at the point 117 generates a voltage signal that is supplied to the HV charger 106. The HV charger 106 modifies, such as increases or decrease, the voltage at the point 117 to output a voltage signal for the second time. The voltage signal is provided via the diode 120 and the resonant inductor 122 in the same manner in which the voltage signal 138 is supplied for the first time to process the substrate in the plasma chamber 110. Also, after sending the control signal 142 for the second time, the processor 126 sends the control signal 150 for a second time to achieve ion flux compensation for the second time. In this manner, multiple occurrences, such as instances, of the charging of the plasma chamber 110, the magnetic energy recovery, and the ion flux compensation take place.

[0040] In an embodiment, the voltage and current sensor system 112 measures a peak to peak voltage and current at the point 132. A total delivered power to be provided to the plasma chamber 110 is calculated by the processor 126 based on the peak to peak voltage and current.

[0041] Figure 2 is an embodiment of a graph 200 of a tailored waveform to illustrate an occurrence of charging of the plasma load, followed by an occurrence of the magnetic energy recovery, which is followed by an occurrence of the ion flux compensation. The graph 200 plots a voltage 202 indicative of the tailored waveform on a y-axis and time t on an x-axis. Charging of the plasma load occurs from a time t_0 to a time t_3 . Once the plasma load is charged, discharging of the plasma load occurs at the time t_3 for the magnetic energy recovery to occur. After the magnetic energy recovery occurs, the ion flux compensation occurs from the time t_3 to a time t_{12} . In this manner, another cycle of an occurrence of the charging of the plasma load, an occurrence of the magnetic energy recovery, and an occurrence of the ion flux compensation repeats.

[0042] It should be noted that although a voltage of 0 volts is indicated at the time t_0 before the charging starts, in one embodiment, a positive voltage or a negative voltage occurs before the charging starts.

[0043] Figure 3A is an embodiment of a graph 300 to illustrate charging of the plasma load. The graph 300 plots a voltage on a y-axis and the time t on an x-axis. The plasma load is charged between a time t_1 and a time t_2 .

[0044] Figure 3B is an embodiment of a graph 310 to illustrate multiple cycles of charging. The graph 310 plots a voltage on a y-axis and the time t on an x-axis. The plasma load is charged, during a first cycle, between the times t_1 and t_2 and is charged again, during a second cycle, between the time t_{12} and a time t_{13} . The voltage of the graph 310 is an example of the voltage of the voltage signal 138 (Figure 1) output from the HV charger 106 (Figure 1). As an example, during each occurrence of charging of the plasma load, the voltage of the voltage signal 138 is a value between 5 volts and 15 kilovolts (kV). Also, as an example, during each occurrence of discharging of the plasma load and each occurrence of the ion flux compensation, the voltage of the voltage signal 138 is a value between 0 volts and -8 kV.

[0045] Figure 3C is an embodiment of a graph 322 to illustrate an occurrence of the magnetic energy recovery. The graph 322 plots a voltage on a y-axis and the time t on an x-axis. After charging the plasma load, magnetic energy recovery occurs from the time t_2 to the time t_3 .

[0046] Figure 3D is an embodiment of a graph 330 to illustrate an occurrence of the ion flux compensation. The graph 322 plots a voltage on a y-axis and the time t on an x-axis. After the magnetic energy recovery occurs, the ion flux compensation occurs from the time t_3 to the time t_{12} .

[0047] Figure 3E is an embodiment of a graph 340 to illustrate multiple occurrences of the ion flux compensation. The graph 340 plots a voltage on a y-axis and the time t on an x-axis. One occurrence of the ion flux compensation occurs from the time t_3 to the time t_{12} and

another occurrence of the ion flux compensation occurs from a time t_{14} to a time t_{23} . As an example, during each occurrence of the ion flux compensation, the voltage applied by the ion flux compensator 104 is a value between 5 volts and 5 kV. Also, as an example, during each occurrence of lack of the ion flux compensation, the voltage applied by the ion flux compensator 104 is a value between 0 volts and -25 kV.

[0048] It should be noted that in all the graphs 200 (Figure 2), 300, 310, 320, 330, and 340, described herein, a time $t_{(n+1)}$ is greater than a time t_n , where n is an integer greater than or equal to zero. For example, the time $t_{(n+1)}$ occurs after the time t_n .

[0049] Figure 4 is a diagram of an embodiment of a system 400 to illustrate details of the ion flux compensator 104. The system 400 includes the controller 102, the ion flux compensator 104, the HV charger 106, the charging diode 120, the resonant inductor 122, the plasma chamber 110, and the IFC diode 124.

[0050] The ion flux compensator 104 includes a pulser 402, an inductor 406, a resistor 408, and a diode 410. An example of the pulser 402 is a nanosecond pulser (nsp). An example of the pulser 402 is a DC voltage source that generates a DC signal, which pulses between two different voltage levels. The inductor 406 is coupled in series with the resistor 408 to form a series circuit. The series circuit of the inductor 406 and the resistor 408 is coupled in parallel to the diode 408 at points 412 and 414 to form a resistor-inductor-diode (RLD) circuit. The pulser 402 is coupled to the point 412 and is coupled to a ground potential. The point 414 is coupled to the IFC diode 124 and the pulser 402 is coupled to the processor 126.

[0051] During an occurrence of the ion flux compensation, the IFC diode 124 is forward biased and the diode 410 is reverse biased. Upon receiving the control signal 150, the pulser 402 generates a current signal 416 and sends the current signal 416 to the point 412. Because the current signal 416 is negative, Figure 4 illustrates the current signal 416 as flowing from the point 412 to the pulser 402. When the current signal 416 is sent via the inductor 406 and the resistor 408, an impedance of the current signal 416 is modified by the inductor 406 and the resistor 408 to output the current signal 152 at the point 414. Because the current signal 152 is negative, Figure 4 illustrates an arrow pointing from the point 130 to the point 414.

[0052] The current signal 152 is sent via the IFC diode 124, the point 130, and the resonant inductor 122 to the electrode of the plasma chamber 110 to tune the ion flux to provide ion flux compensation within the plasma chamber 110. For example, ion flux of plasma within the plasma chamber 110 is tuned, such as modified, with a change in an amount of current of the current signal 416, and the change in the amount of current of the current signal 416 changes an amount of current of the current signal 152. To illustrate, the processor 126 identifies from, within the memory device 128, that the first amount of voltage to be applied by the pulser 402

corresponds to the first amount of current of the current signal 416, the second amount of voltage to be applied by the pulser 402 corresponds to the second amount of current of the current signal 416, and the third amount of voltage to be applied by the pulser 402 corresponds to the third amount of current of the current signal 416. The processor 126 determines that the first amount of current is to be output from the pulser 402 and indicates, within the control signal 150, the first amount of voltage, corresponding to the first amount of current, is to be applied by the pulser 402. Upon receiving the control signal 150 indicating the first amount of voltage, the pulser 402 applies the first amount of voltage to output the current signal 416 having the first amount of current. To tune, such as increase the ion flux, the processor 126 determines that the second amount of current is to be output from the pulser 402 and indicates, within the control signal 150, the second amount of voltage, corresponding to the second amount of current, is to be applied by the pulser 402. Upon receiving the control signal 150 indicating the second amount of voltage, the pulser 402 applies the second amount of voltage to output the current signal 416 having the second amount of current. Also, to tune, such as decrease the ion flux, the processor 126 determines that the third amount of current is to be output from the pulser 402 and indicates, within the control signal 150, the third amount of voltage, corresponding to the third amount of current, is to be applied by the pulser 402. Upon receiving the control signal 150 indicating the third amount of voltage, the pulser 402 applies the third amount of voltage to output the current signal 416 having the third amount of current.

[0053] On the other hand, the IFC diode 124 is reverse biased to electrically disconnect the ion flux compensator 104 from the point 130. When the IFC diode 124 is reverse biased and the diode 410 is forward biased, the ion flux compensation stops. When the ion flux compensation stops, the current signal 416 is transferred via the point 412 and the diode 410 to the resistor 408 and the inductor 406. As such, the current signal 416 flows in an opposite direction when the IFC diode 424 is reverse biased and the diode 410 is forward biased compared to a direction of flow of the current signal 416 when the IFC diode 416 is forward biased and the diode 410 is reverse biased. As such, the current signal 416 is switched between the two directions, and therefore, the ion flux compensator 104 acts as a switched circuit.

[0054] The processor 126 determines, using the clock source, whether a time at which the plasma load is to be charged again, for the second time, has occurred immediately after the ion flux compensation. Upon determining so, the processor 126 generates and sends the control signal 151 to the pulser 402. For example, the ion flux compensation occurs for the first time until the processor 126 sends the control signal 134 (Figure 1) to the DC voltage source Vdc for the second time and until the processor 126 sends the control signal 151 to the pulser 402. The control signal 151 is sent to the pulser 402 to reverse bias the IFC diode 124 to

electrically decouple the ion flux compensator 104 from the plasma load. For example, the control signal 151 indicates that an amount of voltage to be applied at the pulser 402 is negative. Upon receiving the indication that the amount of voltage to be applied at the pulser 402 is negative, the pulser 402 modifies the voltage applied at its output to be of the negative amount, the diode 410 becomes forward biased, and the IFC diode 124 becomes reverse biased. When the IFC diode 124 is reverse biased, a voltage at the point 414 is greater than a voltage at the point 130 to electrically decouple the ion flux compensator 104 from the plasma chamber 110.

[0055] Figure 5 is a diagram of an embodiment of a system 500 to illustrate details of the HV charger 106. The system 500 includes the DC voltage source Vdc, the HV charger 106, the ion flux compensator 104, the diodes 116 and 118, and the controller 102. The HV charger 106 includes a combination of power supplies, such as DC power supplies or voltage power supplies, that convert, such as increase or decrease, a direct current voltage from one amount to another amount. The power supplies have inputs that are coupled in parallel and have outputs that are coupled in series. Examples of the combination of power supplies include a first power supply, a second power supply, and a third power supply coupled to each other. The point 117 is coupled to an input of the first power supply. The first input of the power supply is also an input of the HV charger 106. An output 515 of the HV charger 106 is coupled to the charging diode 120.

[0056] Enable inputs 524, 526, and 528 of the power supplies are coupled to the processor 126. For example, the enable input 524 of the first power supply is coupled via a connection 530 to the processor 126, the enable input 526 of the second power supply is coupled via a connection 532 to the processor 126, and the enable input 528 of the third power supply is coupled via a connection 534 of the processor 126.

[0057] It should be noted that the HV charger 106 excludes any switches. When switches are used, there can be a relative delay in turning off or on of the switches. For example, one of the switches is turned on before another one of the switches is turned on. As another example, one of the switches is turned off before another one of the switches is turned off. The relative delay acts as an impediment to achieving process results. When the switches are not used, any chances of occurrence of the relative delay associated with the switches are nonexistent.

[0058] The processor 126 sends the control signal 134 to control, such as enable or disable, one or more of the power supplies to modify an amount of voltage at the output 515 that is applied to the charging diode 120. For example, the processor 126 sends an enable signal ES1 via the connection 530 to the enable input 524 to turn on the first power supply, sends another enable signal ES2 via the connection 532 to the enable input 526 to turn on the second power

supply, and sends yet another enable signal ES3 via the connection 534 to the enable input 528 to turn on the third power supply. The three enable signals ES1 through ES3 are an example of the control signal 134. As another example, the first and second power supplies are turned on, and the third power supply is turned off. To illustrate, the processor 126 sends a disable signal DS3 via the connection 534 to the enable input 528 to turn off the third power supply. The two enable signals ES1 and ES2 and the third disable signal DS3 are an example of the control signal 134.

[0059] Upon receiving the voltage signal 136 via the diode 114, which is forward biased, an amount of voltage of the voltage signal 136 is modified, such as increased or decreased, by one or more of the power supplies that are turned on and remaining ones of the power supplies that are turned off to output an amount of voltage of the voltage signal 138 at the output 515. For example, when all the power supplies are turned on, the amount of voltage of the voltage signal 138 at the output 515 is greater than when the first and second power supplies are turned on and the third power supply is turned off.

[0060] In an embodiment, one or more additional HV chargers are coupled between the point 117 and the HV charger 106.

[0061] In one embodiment, to modify, such as increase or decrease, a voltage of the voltage signal 138 at the output 515, the processor 126 modifies, such as increases or decreases, a voltage applied by the DC voltage source Vdc in addition to or instead of controlling enablement or disablement of one or more of the power supplies.

[0062] Figure 6 provides embodiments of graphs 602, 604, 606, 608, and 610 to illustrate wafer voltage, pre-blocking capacitor voltage, current output from the ion flux compensator 104 (Figure 1), voltage output from the ion flux compensator 104, and voltage output from the HV charger 106 versus the time t. The graph 602 plots a voltage at a substrate support on which the substrate is placed on a y-axis and the time t on an x-axis. The substrate support includes a lower electrode. The voltage of the substrate support illustrates a wafer potential, such as a voltage at a lower sheath of plasma formed within the plasma chamber 110 (Figure 1). As illustrated in the graph 602, the wafer potential is constant between a time of 3 microseconds (μ s) and a time of 5 microseconds.

[0063] The graph 604 plots a voltage at a pre-blocking capacitor (not shown), which is located between the point 132 (Figure 1) and the plasma chamber 110. The graph 604 plots a voltage across the pre-blocking capacitor on a y-axis and the time t on an x-axis. As illustrated, the voltage across the pre-blocking capacitor has a negative slope during a time interval between 3 microseconds and 5 microseconds.

[0064] The graph 606 plots an amount of current of the current signal 152 (Figure 1) generated by the ion flux compensator 104 (Figure 1) versus the time t . The amount of current of the current signal 152 is plotted on a y-axis and the time t is plotted on an x-axis. As illustrated in the graph 606, a substantially zero current, such as an amount of current between -0.3 amperes (A) and 0 A, is generated by the ion flux compensator 104 during ion discharging and a substantially constant amount of current, such as an amount of current between 2.7 A and 3.3 A, is generated by the ion flux compensator 104 during ion charging. Because the current output from the ion flux compensator 104 switches between the substantially zero current and the substantially constant amount of current periodically, the ion flux compensator 104 is sometimes referred to herein as the switched circuit.

[0065] It should be noted that an amount of current output from the ion flux compensator 104 during each occurrence of the ion flux compensation controls an amount of slope, such as the negative slope, of the voltage across the pre-blocking capacitor. The voltage across the pre-blocking capacitor is illustrative of voltage that is applied to the plasma load 110 for processing the substrate.

[0066] The graph 608 plots an amount of voltage output from the pulser 402 (Figure 4) versus the time t . For example, the amount of voltage output from the pulser 402 is plotted on a y-axis and the time t is plotted on an x-axis. The processor 126 controls, via the control signal 150 (Figure 1), the amount of voltage output at the pulser 402. For example, the processor indicates the amount of voltage to be output at the pulser 402 within the control signal 150. Upon receiving the control signal 150, the pulser 402 generates the current signal 416 based on the amount of voltage indicated within the control signal 150. The current signal 416 has an amount of current that corresponds to the amount of voltage output at the pulser 402 to achieve and control the negative slope of voltage across the pre-blocking capacitor. The negative slope is achieved and controlled to tune the wafer potential to be constant to achieve the high aspect ratio etch.

[0067] The graph 610 plots an amount of voltage of the voltage signal 138 (Figure 1) output from the HV charger 106 (Figure 1) on a y-axis and the time t on an x-axis. The voltage signal 138 includes a charge voltage, which is an amount of voltage used to charge the plasma load. Between two consecutive cycles of applying the charge voltage, a negative bias voltage is applied from the HV charger 106 to the plasma load 110.

[0068] It should be noted that the x-axes of graphs 602, 604, 606, 608, and 610 is the same. For example, the time t progresses in the same manner along each of the x-axis of the graphs 602, 604, 606, 608, and 610.

[0069] Figure 7 provides embodiments of graphs 702, 704, and 706 to illustrate multiple states of the voltage signal 136 (Figure 1) output from the DC voltage source V_{dc} (Figure 1) with respect to the voltage across the pre-blocking capacitor and the wafer potential. The graph 702 plots a high state, such as a state 1, and a low state, such as a state 0, of the voltage signal 136 on a y-axis and the time t on an x-axis. The voltage signal 136 transitions from the state 0 to the state 1 and further transitions from the state 1 to the state 0.

[0070] The graph 704 plots the voltage across the pre-blocking capacitor on a y-axis and the time t on an x-axis. With the transition of the voltage signal 136 from the state 0 to the state 1, the voltage across the pre-blocking capacitor also transitions from a low voltage level to a high voltage level. Also, with the transition of the voltage signal 136 from the state 1 to the state 0, the voltage across the pre-blocking capacitor transitions from the high voltage level to the low voltage level.

[0071] The graph 706 plots the wafer potential on a y-axis and the time t on an x-axis. With the transition of the voltage signal 136 from the state 0 to the state 1, the wafer potential also transitions from a low voltage level to a high voltage level. Also, with the transition of the voltage signal 136 from the state 1 to the state 0, the wafer potential transitions from the high voltage level to the low voltage level.

[0072] It should be noted that the x-axes of graphs 702, 704, and 706 is the same. For example, the time t progresses in the same manner along each of the x-axis of the graphs 702, 704, and 706.

[0073] Embodiments described herein may be practiced with various computer system configurations including hand-held hardware units, microprocessor systems, microprocessor-based or programmable consumer electronics, minicomputers, mainframe computers and the like. The embodiments can also be practiced in distributed computing environments where tasks are performed by remote processing hardware units that are linked through a network.

[0074] In some embodiments, a controller, described herein, is a part of a system, which may be part of the above-described examples. Such systems include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems are integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics is referred to as the “controller,” which may control various components or subparts of the system or systems. The controller, depending on the processing requirements and/or the type of system, is programmed to control any of the processes disclosed herein, including the delivery of process

gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, RF generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks coupled to or interfaced with a system.

[0075] Broadly speaking, in a variety of embodiments, the controller is defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as Application Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). The program instructions are instructions communicated to the controller in the form of various individual settings (or program files), defining the parameters, the factors, the variables, etc., for carrying out a particular process on or for a semiconductor wafer or to a system. The program instructions are, in some embodiments, a part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0076] The controller, in some embodiments, is a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller is in a “cloud” or all or a part of a fab host computer, which allows for remote access of the wafer processing. The computer enables remote access to the system to monitor current progress of fabrication operations, examines a history of past fabrication operations, examines trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process.

[0077] In some embodiments, a remote computer (e.g. a server) provides process recipes to a system over a network, which includes a local network or the Internet. The remote computer includes a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify the parameters, factors, and/or variables for each of the processing steps to be performed during one or more operations. It should be understood that the parameters, factors, and/or variables are specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus as described above, the controller is distributed, such as by including one or more discrete controllers that are networked together and working towards a

common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes includes one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0078] Without limitation, in various embodiments, example systems to which the methods are applied include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an atomic layer deposition (ALD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that is associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0079] It is further noted that in some embodiments, the above-described operations apply to several types of plasma reactor chambers, e.g., a plasma chamber including an inductively coupled plasma (ICP) reactor, a capacitively coupled plasma (CCP) reactor, a transformer coupled plasma reactor, conductor tools, dielectric tools, a plasma chamber including an electron cyclotron resonance (ECR) reactor, etc. For example, one or more RF generators are coupled to an inductor within the ICP reactor. Examples of a shape of the inductor include a solenoid, a dome-shaped coil, a flat-shaped coil, etc.

[0080] As noted above, depending on the process step or steps to be performed by the tool, the host computer communicates with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0081] With the above embodiments in mind, it should be understood that some of the embodiments employ various computer-implemented operations involving data stored in computer systems. These operations are those physically manipulating physical quantities. Any of the operations described herein that form part of the embodiments are useful machine operations.

[0082] Some of the embodiments also relate to a hardware unit or an apparatus for performing these operations. The apparatus is specially constructed for a special purpose computer. When defined as a special purpose computer, the computer performs other

processing, program execution or routines that are not part of the special purpose, while still being capable of operating for the special purpose.

[0083] In some embodiments, the operations may be processed by a computer selectively activated or configured by one or more computer programs stored in a computer memory, cache, or obtained over the computer network. When data is obtained over the computer network, the data may be processed by other computers on the computer network, e.g., a cloud of computing resources.

[0084] One or more embodiments can also be fabricated as computer-readable code on a non-transitory computer-readable medium. The non-transitory computer-readable medium is any data storage hardware unit, e.g., a memory device, etc., that stores data, which is thereafter be read by a computer system. Examples of the non-transitory computer-readable medium include hard drives, network attached storage (NAS), read-only memory (ROM), random access memory (RAM), compact disc-ROMs (CD-ROMs), CD-recordables (CD-Rs), CD-rewritables (CD-RWs), magnetic tapes and other optical and non-optical data storage hardware units. In some embodiments, the non-transitory computer-readable medium includes a computer-readable tangible medium distributed over a network-coupled computer system so that the computer-readable code is stored and executed in a distributed fashion.

[0085] Although the method operations above were described in a specific order, it should be understood that in various embodiments, other housekeeping operations are performed in between operations, or the method operations are adjusted so that they occur at slightly different times, or are distributed in a system which allows the occurrence of the method operations at various intervals, or are performed in a different order than that described above.

[0086] It should further be noted that in an embodiment, one or more features from any embodiment described above are combined with one or more features of any other embodiment without departing from a scope described in various embodiments described in the present disclosure.

[0087] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications can be practiced within the scope of appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

IN THE CLAIMS

1. A method for tuning ion flux, comprising:
 - controlling a charger circuit to provide radio frequency power to an electrode of a plasma chamber;
 - determining whether a predetermined charging time has passed after said controlling the charger circuit;
 - controlling a magnetic energy recovery circuit to recover radio frequency energy from the plasma chamber in response to determining that the predetermined charging time has passed;
 - identifying whether a predetermined voltage associated with use of the magnetic energy recovery circuit is achieved after said controlling the magnetic energy recovery circuit; and
 - controlling an ion flux compensation circuit to tune the ion flux within the plasma chamber in response to determining that the predetermined voltage is achieved.
2. The method of claim 1, wherein said controlling the charging circuit includes generating one or more signals to control one or more power supplies.
3. The method of claim 2, wherein the one or more signals include one or more enable signals to enable the one or more power supplies.
4. The method of claim 3, wherein the one or more power supplies include a plurality of power supplies, wherein the one or more signals include a plurality of signals, wherein the plurality of signals include one or more disable signals to disable remaining ones of the plurality of power supplies.
5. The method of claim 1, wherein after the predetermined charging time has passed, a charging diode coupled to the charger circuit is reverse biased, wherein when the charging diode is reverse biased, the charger circuit does not charge the plasma chamber.
6. The method of claim 1, wherein said controlling the magnetic energy recovery circuit includes enabling a transfer of the radio frequency energy from the plasma chamber to an energy storage circuit coupled to the charger circuit.
7. The method of claim 1, comprising:
 - receiving a voltage measured at an input of the plasma chamber;
 - comparing the voltage with the predetermined voltage to determine that the voltage measured is less than the predetermined voltage, wherein the ion flux compensation circuit is controlled upon determining that the voltage measured is less than the predetermined voltage.

8. The method of claim 1, wherein said controlling the ion flux compensation circuit includes generating a control signal to modify a voltage of a pulser of the ion flux compensation circuit.
9. A controller for tuning ion flux, comprising:
 - a processor configured to:
 - control a charger circuit to provide radio frequency power to an electrode of a plasma chamber;
 - determine whether a predetermined charging time has passed after the charger circuit is controlled;
 - control a magnetic energy recovery circuit to recover radio frequency energy from the plasma chamber when it is determined that the predetermined charging time has passed;
 - identify whether a predetermined voltage associated with use of the magnetic energy recovery circuit is achieved after the magnetic energy recovery circuit is controlled; and
 - control an ion flux compensation circuit to tune the ion flux within the plasma chamber when it is determined that the predetermined voltage is achieved; and
 - a memory device coupled to the processor.
10. The controller of claim 9, wherein to control the charging circuit, the processor is configured to generate one or more signals to control one or more power supplies.
11. The controller of claim 10, wherein the one or more signals include one or more enable signals to enable the one or more power supplies.
12. The controller of claim 11, wherein the one or more power supplies include a plurality of power supplies, wherein the one or more signals include a plurality of signals, wherein the plurality of signals include one or more disable signals to disable remaining ones of the plurality of power supplies.
13. The controller of claim 9, wherein after the predetermined charging time has passed, a charging diode coupled to the charger circuit is reverse biased, wherein when the charging diode is reverse biased, the charger circuit does not charge the plasma chamber.
14. The controller of claim 9, wherein to control the magnetic energy recovery circuit, the processor is configured to enable a transfer of the radio frequency energy from the plasma chamber to an energy storage circuit coupled to the charger circuit.
15. The controller of claim 9, wherein the processor is configured to:
 - receive a voltage measured at an input of the plasma chamber;

compare the voltage with the predetermined voltage to determine that the voltage measured is less than the predetermined voltage, wherein the ion flux compensation circuit is controlled when it is determined that the voltage measured is less than the predetermined voltage.

16. The controller of claim 9, wherein to control the ion flux compensation circuit, the processor is configured to generate a control signal to modify a voltage of a pulser of the ion flux compensation circuit.

17. A plasma system for tuning ion flux, comprising:

a plasma chamber having an electrode;

a charger circuit coupled to the plasma chamber, wherein the charger circuit is configured to provide radio frequency power to the electrode;

a magnetic energy recovery circuit coupled to the charger circuit;

an ion flux compensation circuit coupled to the magnetic energy recovery circuit;

and

a controller coupled to the charger circuit, the magnetic energy recovery circuit, and the ion flux compensation circuit, wherein the controller is configured to:

determine whether a predetermined charging time has passed after the charger circuit provides the radio frequency power;

control the magnetic energy recovery circuit to recover radio frequency energy from the plasma chamber when it is determined that the predetermined charging time has passed;

identify whether a predetermined voltage associated with use of the magnetic energy recovery circuit is achieved after the magnetic energy recovery circuit is controlled; and

control the ion flux compensation circuit to tune the ion flux within the plasma chamber when it is determined that the predetermined voltage is achieved.

18. The plasma system of claim 17, wherein to control the charging circuit, the controller is configured to generate one or more signals to control one or more power supplies.

19. The plasma system of claim 18, wherein the one or more signals include one or more enable signals to enable the one or more power supplies.

20. The plasma system of claim 19, wherein the one or more power supplies include a plurality of power supplies, wherein the one or more signals include a plurality of signals, wherein the plurality of signals includes one or more disable signals to disable remaining ones of the plurality of power supplies.

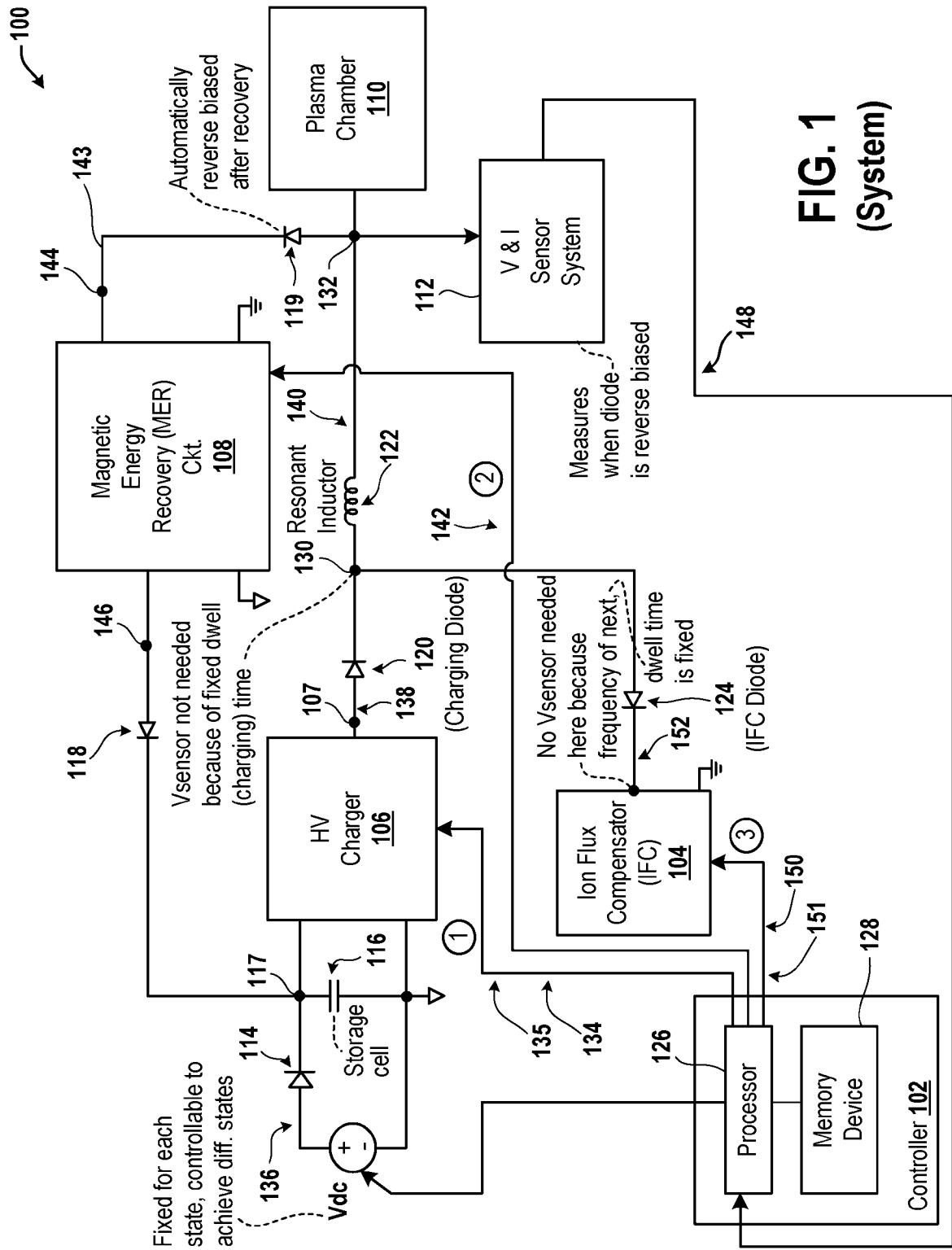


FIG. 1
(System)

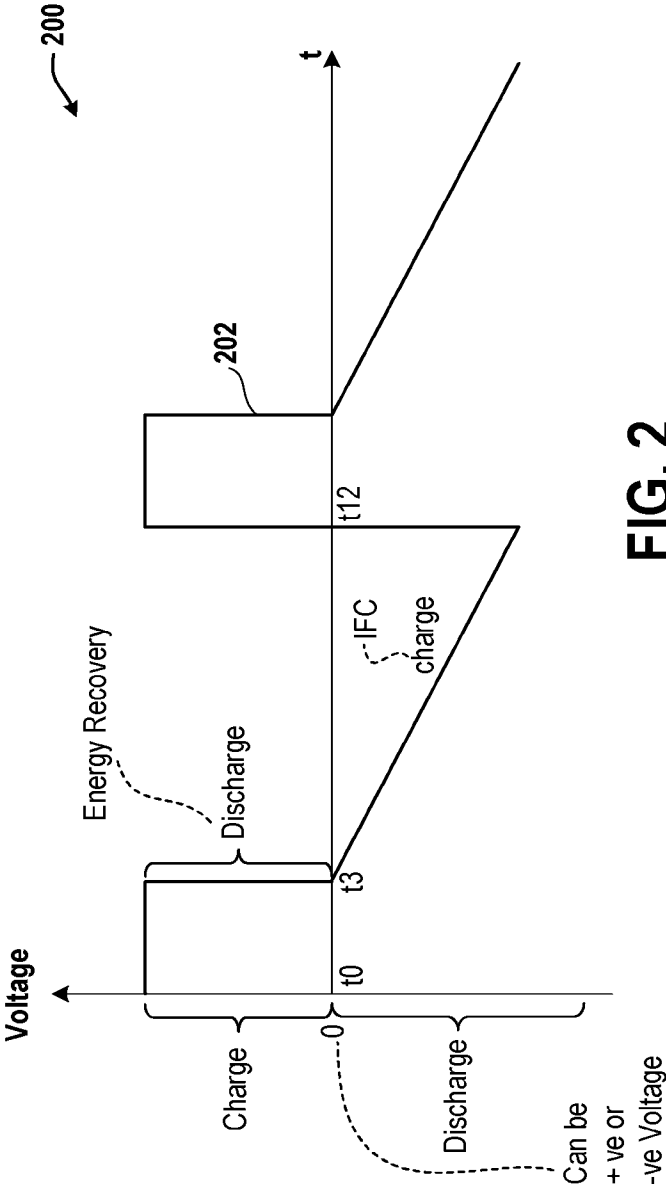
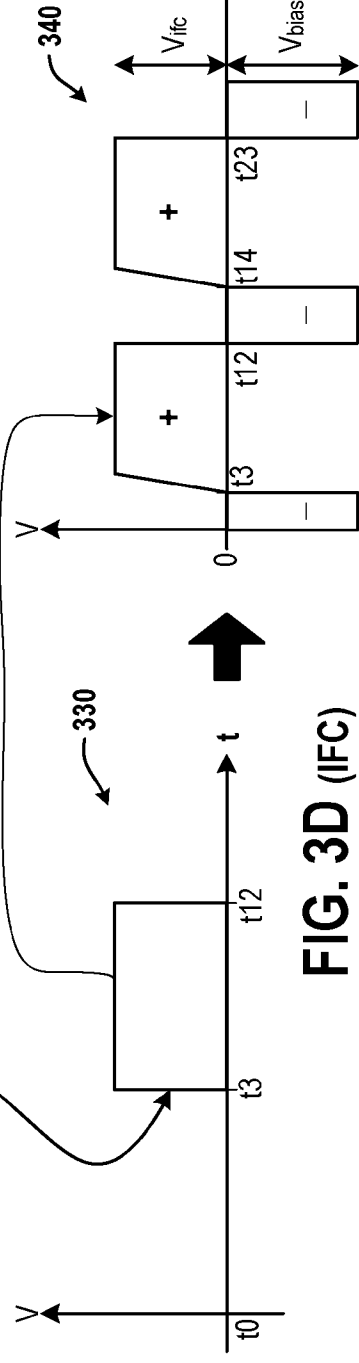
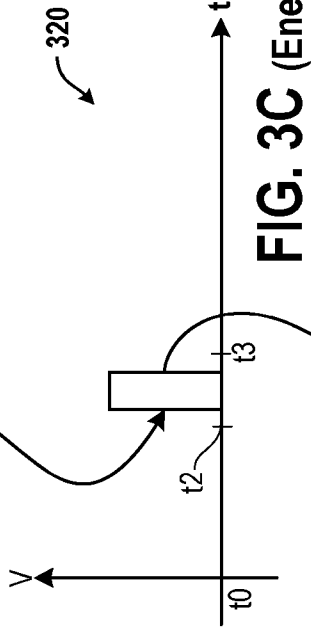
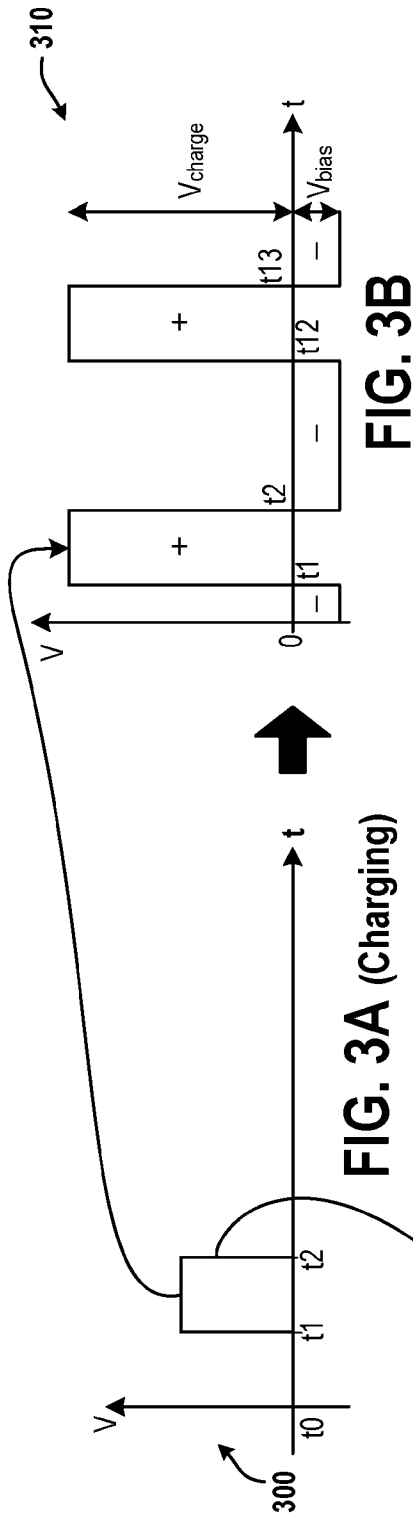


FIG. 2
(Operation)



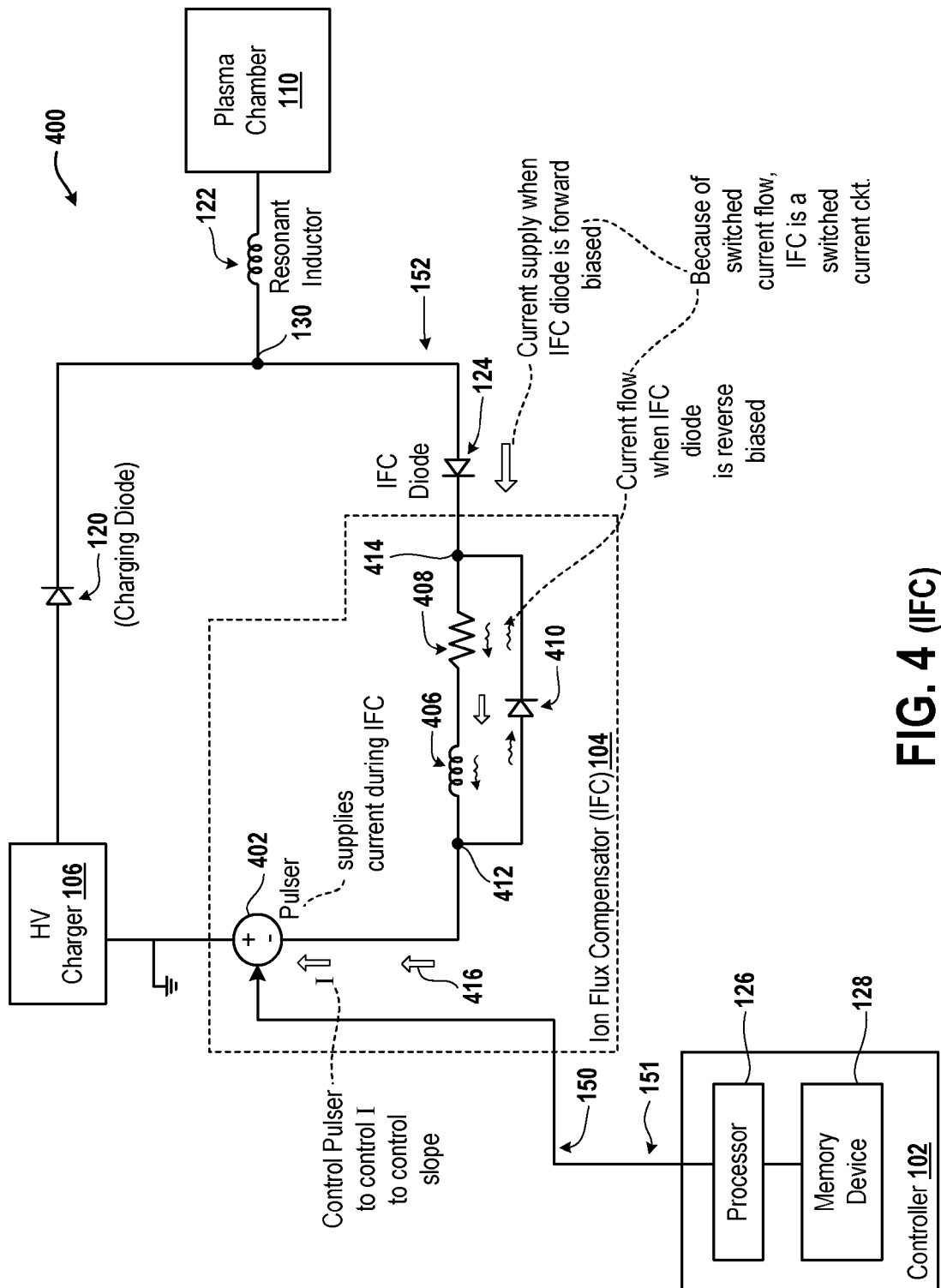


FIG. 4 (IFC)

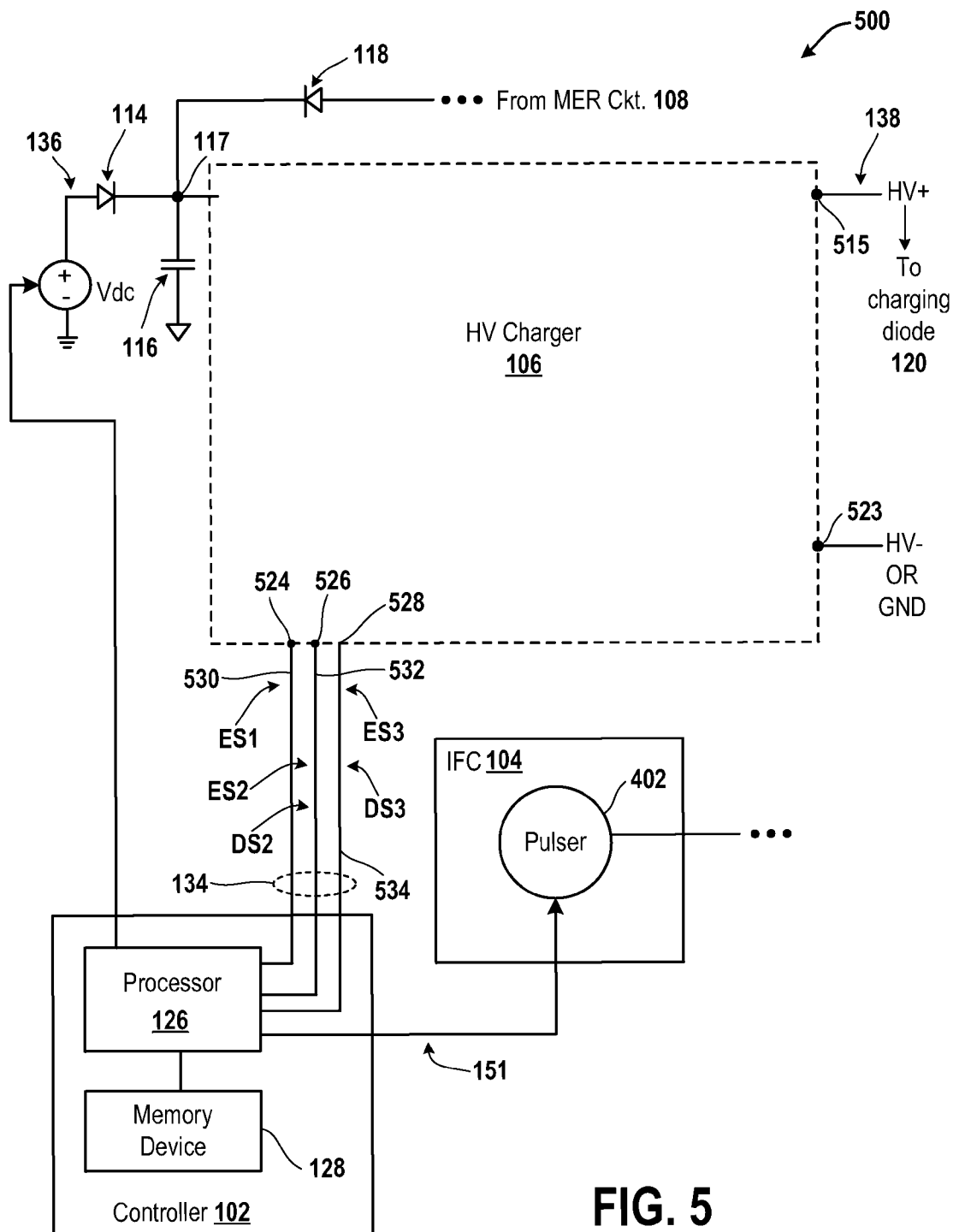


FIG. 5
(Control of HV Charge)

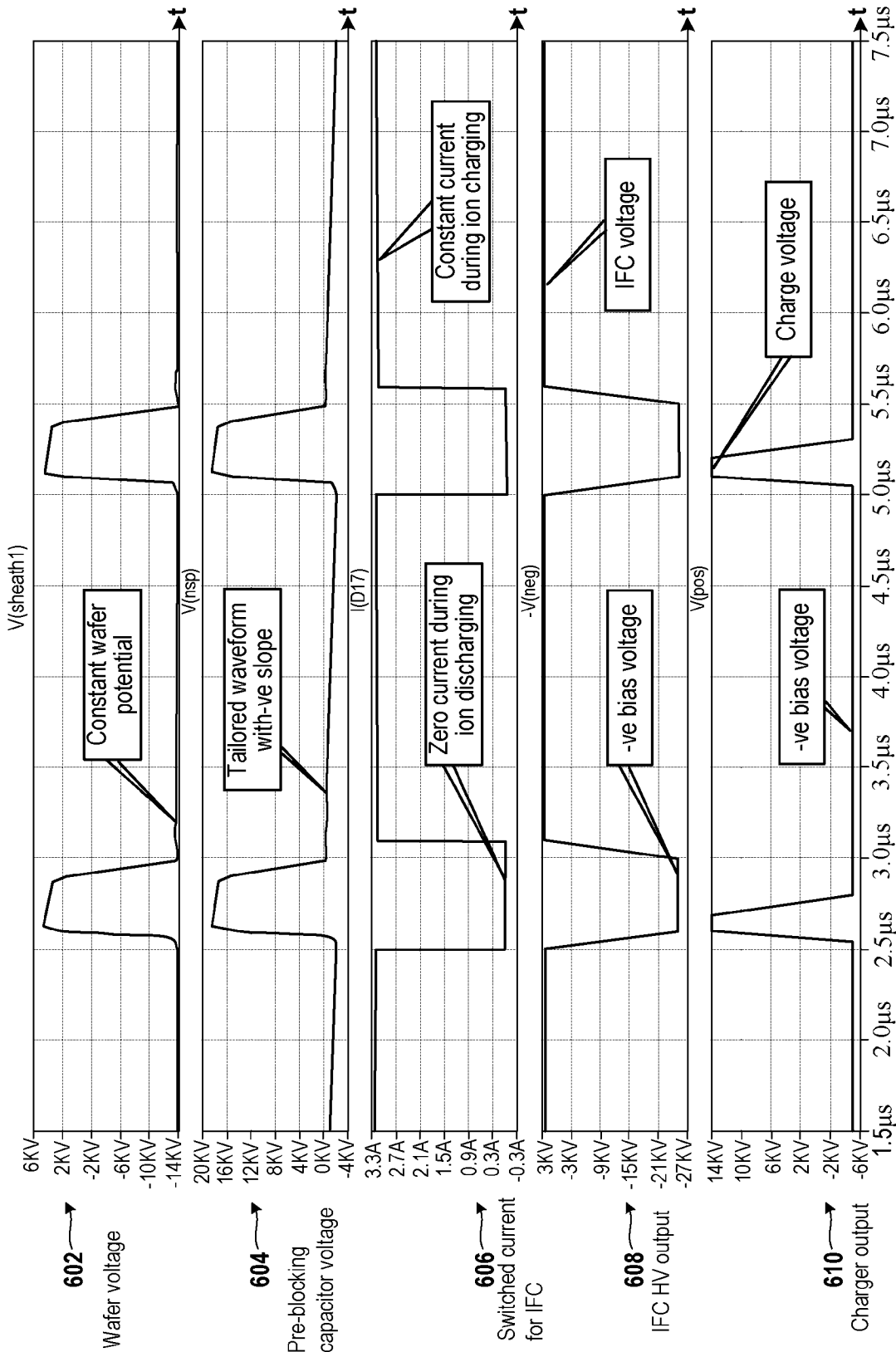


FIG. 6

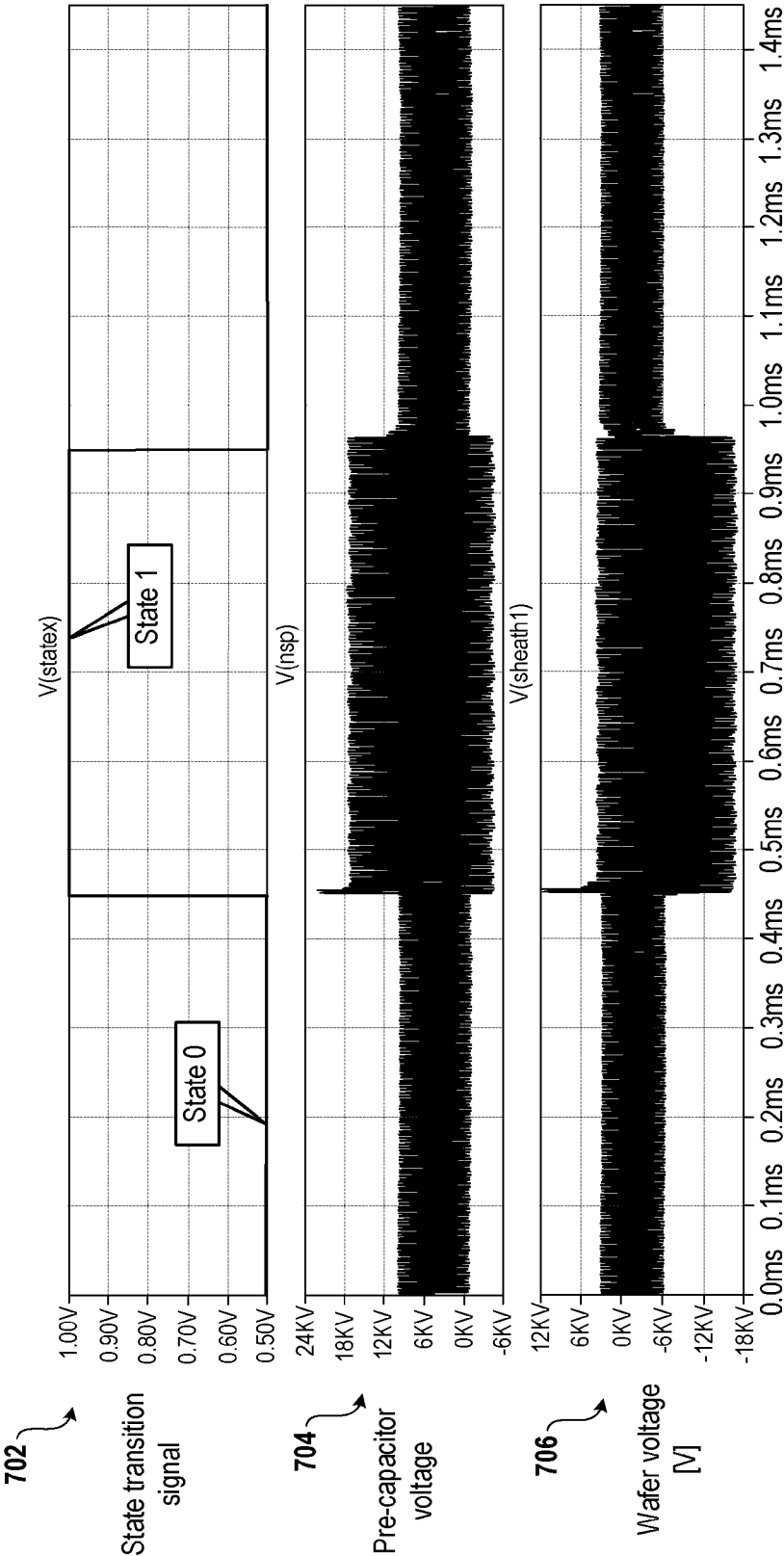


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2024/058299

A. CLASSIFICATION OF SUBJECT MATTER**H01J 37/32**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01J 37/32(2006.01); H01L 21/02(2006.01); H02M 7/5387(2007.01); H05H 1/24(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: plasma, chamber, ion, charge, compensate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0319584 A1 (VICTOR BROUK et al.) 20 December 2012 (2012-12-20) paragraphs [0207]-[0221] and figures 21-25	1-20
A	US 2011-0176343 A1 (NAOTO KOJIMA) 21 July 2011 (2011-07-21) paragraph [0103] and figure 1	1-20
A	US 2022-0108874 A1 (APPLIED MATERIALS, INC.) 07 April 2022 (2022-04-07) paragraphs [0023]-[0039] and figures 1-4	1-20
A	US 2023-0230804 A1 (LAM RESEARCH CORPORATION) 20 July 2023 (2023-07-20) paragraphs [0035]-[0121] and figures 1-8	1-20
A	KR 10-2021-0041608 A (EAGLE HARBOR TECHNOLOGIES, INC.) 15 April 2021 (2021-04-15) paragraphs [0029]-[0144] and figures 1-19	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

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“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

26 March 2025

Date of mailing of the international search report

26 March 2025

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT
nt family members

International application No.

PCT/US2024/058299

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2012-0319584	A1	20 December 2012	CN	107978506	A	01 May 2018
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