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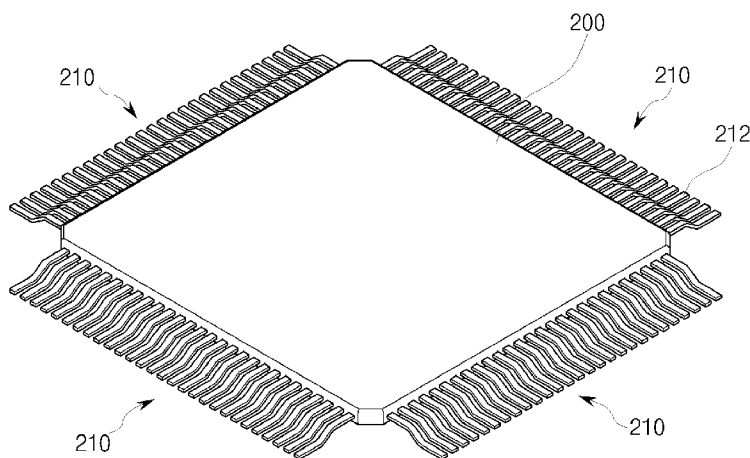
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[Continued on next page]

(54) Title: LEADFRAME AND METHOD FOR MANUFACTURING THE SAME

[Fig. 1]



(57) Abstract: Disclosed is a leadframe. The leadframe comprises a die pad part, at least one lead part, and at least one supporting part. A semiconductor chip is mounted on a first surface of the leadframe at the die pad. The at least one lead part electrically connects the semiconductor chip to at least one external circuit. The at least one supporting part is adjacent to a second surface opposite the first surface, includes an insulating material, and insulates the at least one lead part from each other.



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Description

Title of Invention: LEADFRAME AND METHOD FOR MANUFACTURING THE SAME

Technical Field

- [1] The present invention relates to a leadframe and a method for manufacturing the same, and more particularly, to a leadframe and method for manufacturing the same that makes it possible to implement a fine pattern and to decrease thickness.

Background Art

- [2] In general, as shown in FIG. 1, a semiconductor chip package 200 is manufactured by mounting a semiconductor chip on a die pad of a leadframe, performing a wire bonding electrically connecting the semiconductor chip to the leadframe and packing the mounted semiconductor chip using a sealant.
- [3] Thus, the leadframe functions to connect an inside of the semiconductor chip package 200 to an external circuit and at the same time to mount the semiconductor chip. For this purpose, the leadframe includes a die pad part on which a semiconductor chip, an inner lead of a lead part 210 electrically connected to the semiconductor chip through a wire, and an outer lead of the lead part 210 electrically connected to an external circuit.
- [4] As shown in FIG. 1, since the lead part 210 of the leadframe is formed in a lead structure having a predetermined thickness, it is difficult to realize miniaturization, slimness and formation of micropattern. Also, since the length of the wire electrically connecting the semiconductor chip to the inner lead of the lead part 210 increases, the manufacturing cost increases.

Disclosure of Invention

Technical Problem

- [5] Accordingly, embodiments of the present invention provide a leadframe and method for manufacturing the same that makes it possible to form a micropattern and to decrease the thickness of the lead part.

Solution to Problem

- [6] In an embodiment, a leadframe comprises a die pad part, at least one lead part, and at least one supporting part. A semiconductor chip is mounted on a first surface of the leadframe at the die pad. The at least one lead part electrically connects the semiconductor chip to at least one external circuit. The at least one supporting part is adjacent to a second surface opposed the first surface, includes an insulating material, and insulates the at least one lead part from each other.
- [7] Each of the at least one lead part may comprise at least one selected from the group

consisting of copper (Cu), iron (Fe), and alloys thereof.

- [8] The die pad part may include a cavity corresponding to a region where the semiconductor chip is mounted.
- [9] Each of the at least one lead part may comprise a horizontal part positioned toward the first surface, and a vertical part extending from the first surface to the second surface. The leadframe may comprises at least one inner lead and at least one outer lead. The inner lead may be formed on the first surface of the horizontal part, and the outer lead may be formed on the second surface of the vertical part.
- [10] A width of the at least one inner lead may be smaller than a width of the at least one outer lead.
- [11] In the horizontal part, a portion where the at least one inner lead is positioned may be more protruded than a portion where the at least one inner lead is not positioned.
- [12] At least one inner lead and the at least one outer lead comprises at least material selected from the group consisting of nickel (Ni), palladium (Pd), gold (Au), silver (Ag), tin (Sn), copper (Cu), chromium (Cr), and alloys thereof.
- [13] The at least one supporting part may be more protruded than the at least one outer lead.
- [14] A surface of the at least one supporting part and a surface of the at least one outer lead may be positioned on the same plane.
- [15] The ratio of a thickness of the leadframe : a depth of the at least one supporting part may be 127:65 to 127:90.
- [16] In another embodiment, a leadframe comprises a leadframe substrate and at least one supporting part. The leadframe substrate has a first surface on which a semiconductor chip is mounted, and a second surface opposite to the first surface. In the leadframe substrate, a first region comprised of at least one etched portion formed at the second surface, and a second region which is a portion other than the first region are defined. The at least one supporting part is formed in the at least one etched portion of the first region and includes an insulating material. The second region is comprised of at least one lead part connecting the semiconductor chip to at least one external circuit, and a die pad part on which the semiconductor chip is mounted.
- [17] In a further another embodiment, a method for manufacturing a leadframe comprises preparing a leadframe substrate, forming at least one etched portion, and forming at least one supporting part. The leadframe includes a first surface on which a semiconductor chip is being mounted, and a second surface opposite to the first surface. The at least one etched portion is formed by etching a first region of the second surface. The at least one supporting part is formed by filling an insulating material in the at least one etched portion.
- [18] The leadframe substrate may comprise a conductive material. The second region

other than the first region may be comprised of at least one lead part connecting the semiconductor chip to at least one external circuit, and a die pad part on which the semiconductor chip is mounted.

- [19] The method may comprise forming at least one inner lead and at least one outer lead electrically connected to the at least one lead part between the preparing of the leadframe substrate and the forming of the at least one etched portion.
- [20] The forming of the at least one inner lead and the at least one outer lead may comprise forming a photo resist pattern on the leadframe substrate, and forming a metal material in openings of the photo resist pattern.
- [21] The forming of the at least one etched portion may comprise forming a photo resist pattern on the leadframe substrate, and first etching the second surface of the leadframe substrate by using the photo resist pattern as a mask.
- [22] After the forming of the at least one supporting part, the method may comprises secondly etching the first surface of the leadframe substrate to insulate the at least one lead part from each other.
- [23] In the secondly etching, a cavity may be formed at the first surface of the leadframe substrate, corresponding to a position where the semiconductor chip is being mounted.
- [24] The method may comprise removing the photo resist pattern between the forming of the at least one etched portion and the forming of the at least one supporting part. The method may comprise secondly etching the first surface of the leadframe substrate to decrease width and thickness of the at least one lead part and to electrically insulate the at least one lead part from each other, after the forming of the at least one supporting part.
- [25] In the secondly etching, a cavity may be formed at the first surface of the leadframe substrate, corresponding to a position where the semiconductor chip is being mounted.

Advantageous Effects of Invention

- [26] According to the embodiments of the present invention, a lead part can be implemented in a fine pattern by a simple process using a supporting part insulating the lead part.
- [27] That is, by using a region except for the supporting part in a conductive leadframe substrate as a die pad part and the lead part, the process can be simplified, compared with a case of forming the lead part through a separate process, and a fine pattern can be implemented. Also, the thickness of the leadframe can be decreased. In addition, since the supporting part is formed by filling an etched portion of the leadframe substrate with an insulating material, the supporting part can insulate the lead part and at the same time support the leadframe substrate rigidly.
- [28] Moreover, since an inner lead of the lead part is formed adjacent to a semiconductor

chip, the length of a wire connecting the inner lead and the semiconductor chip can be decreased. Also, since the inner lead and an outer lead are formed in a frame of plural columns including at least one column, high integration will be possible.

[29] Further, since an upper portion of the leadframe substrate is etched to form a cavity in which a semiconductor chip is mounted, during the process of forming an etched portion, the thickness of a package in which the semiconductor chip is mounted can be decreased.

[30] Meanwhile, the leadframe is formed of a metal material and thus has a superior thermal conductivity.

Brief Description of Drawings

[31] FIG. 1 is a perspective view of a related art semiconductor chip package.

[32] FIG. 2 is a plane view of a leadframe as viewed from the front side according to an embodiment of the present invention.

[33] FIG. 3 is a plane view of the leadframe shown in FIG. 2 as viewed from the rear side.

[34] FIG. 4 is a cross-sectional view taken along line I-I' of FIG. 2 in a semiconductor chip package using the leadframe shown in FIGS. 2 and 3 according to a first embodiment.

[35] FIGS. 5 through 16 are cross-sectional views for illustrating a method for manufacturing the leadframe and the semiconductor chip package shown in FIG. 4.

[36] FIGS. 17 and 18 are plane views of masks used in the process of FIG. 6.

[37] FIG. 19 is a plane view of a mask used in the process of FIG. 9.

[38] FIGS. 20 and 21 are cross-sectional views for illustrating a method for manufacturing a supporting part according to an embodiment of the present invention.

[39] FIG. 22 is a cross-sectional view taken along line I-I' of FIG. 2 in a semiconductor chip package using the leadframe shown in FIGS. 2 and 3 according to a second embodiment.

[40] FIGS. 23 through 34 are cross-sectional views illustrating an example of a method for manufacturing the leadframe and the semiconductor chip package shown in FIG. 22.

[41] FIGS. 35 and 36 are cross-sectional views illustrating an example of a method for manufacturing a supporting part.

[42] FIGS. 37 through 49 are cross-sectional views illustrating another example of a method for manufacturing a semiconductor chip package according to a second embodiment.

Mode for the Invention

[43] Hereinafter, Hereinafter, preferred embodiments of the present invention will be described with reference to FIGS. 2 through 49.

- [44] FIG. 2 is a plane view of a leadframe as viewed from the front side according to an embodiment of the present invention, FIG. 3 is a plane view of the leadframe shown in FIG. 2 as viewed from the rear side, and FIG. 4 is a cross-sectional view taken along line I-I' of FIG. 2 in a semiconductor chip package using the leadframe shown in FIGS. 2 and 3 according to a first embodiment.
- [45] Referring to FIGS. 2 through 4, a leadframe substrate 10 includes a die pad part 116 on which a semiconductor chip 120 is mounted, at least one lead part 100 electrically connecting the semiconductor chip 120 to at least one external circuit (not shown), and at least one supporting part 110 insulating the lead parts 100.
- [46] At least one inner lead 122 may be formed at a first surface (hereinafter referred to as "upper surface") of the lead part 100, and at least one outer lead 124 may be formed at a second surface (hereinafter referred to as "lower surface") of the lead part 100. The semiconductor chip 120 may be connected to the inner lead 122 of the lead part 100 through a wire 126, and may be connected to an external circuit through the outer lead 124 of the lead part 100. Another lead 121 for supplying ground voltage to the semiconductor chip 120 may be further provided. However, it is possible that the lead 121 is not formed.
- [47] Referring to FIG. 4, a semiconductor chip package 20 including the leadframe 10 may include the semiconductor chip 120 mounted on the die pad part 116 of the leadframe 10, the wire 126 connecting the semiconductor chip 120 to the lead part 100, and a sealant 130 sealing the leadframe 10 and the semiconductor chip 120. As the sealant 130, a mold resin, epoxy mold compound (EMC) or the like may be used.
- [48] The leadframe 10 according to this embodiment will now be described in more detail.
- [49] The semiconductor chip 120 is positioned on the upper surface of the leadframe 10 and the supporting part 110 is positioned on the lower surface of the leadframe 10.
- [50] In this embodiment, an insulating material is filled in a first region comprised of at least one etched portion 112 obtained by etching a leadframe substrate (see 150 of FIG. 14) to form the supporting part 112, and a second region other than the first region is used as the die pad part 116 and the lead part 100. Thus, since the die pad part 116 and the lead part 100 are parts of the same leadframe substrate 150, the die pad part 116 and the lead part 100 may include the same conductive material. At this time, the die pad part 116 and the lead part 100 may be formed of a metal material having the conductivity, such as copper (Cu), iron (Fe), or an alloy of Cu and Fe.
- [51] The lead part 100 includes a horizontal part 102 positioned toward an upper surface of the leadframe 10, and a vertical part 104 extending from the upper surface to a lower surface. The inner lead 122 is formed at the horizontal part 102 of the lead part 100, and the outer lead 124 is formed at the lower surface of the vertical part of the

lead part 100. By adjusting the length of the horizontal part 102 of the lead part 100, semiconductor chips 120 having various sizes may be formed into semiconductor chip packages having the same size.

- [52] As viewed from the top side, by forming the inner lead 122 to be more adjacent to the semiconductor chip 120 than the outer lead 124, the length of the wire 126 may be decreased. The decrease in the length of the wire 126 can decrease the manufacturing cost. The width of the outer lead 124 may be formed greater than the width of the inner lead 122.
- [53] The inner lead 122 and the outer lead 124 electrically connected to the lead part 100 are arranged in at least one row to make it possible to achieve high integration as in region A and region B shown in FIGS. 2A and 2B. The inner lead 122 and the outer lead 124 may include at least one selected from the group consisting of nickel (Ni), palladium (Pd), gold (Au), silver (Ag), tin (Sn), copper (Cu), chromium (Cr), and alloys thereof, in consideration of an electrical characteristic, a connection characteristic to the wire or external circuit, etc.
- [54] The supporting part 110 is formed between the lead parts 100 to insulate the lead parts from one another, and to support the leadframe 10. The supporting part 110 may be formed by filling an insulating material in the etched portion 112. As the insulating material, photo soldering resist (PSR), resin coated copper (RCC), prepreg (PP), epoxy, etc., may be used. In this embodiment, the supporting part 110 and the outer lead 124 are positioned on the same plane.
- [55] A cavity 106 having a depth and corresponding to a region where the semiconductor chip 120 is mounted may be formed in the die pad part 116. Due to the cavity 106, since the semiconductor chip 120 is inserted and mounted by a thickness, the thickness of the semiconductor chip package 20 can be decreased. By doing so, the thickness of the die pad part 116 may be smaller than that of the vertical part 102 of the lead part 100.
- [56] In the horizontal part 102 according to this embodiment, a portion where the inner lead 122 is formed is protruded compared with a portion where the inner lead 122 is not formed. That is, the thickness T1 of the horizontal part 102 positioned below the inner lead 122 is thicker than thickness T2 of the horizontal part 102 of the portion where the inner lead 122 is not formed. By doing so, the thickness of the semiconductor chip package 20 including the leadframe 10 can be decreased.
- [57] This is due to the fact that in the manufacturing method, the thickness and width of the horizontal part 102 and the vertical part 104 of the portion which is not positioned below the inner lead 122 are decreased. The manufacturing method will be described in more detail with reference to FIGS. 5 through 16. In the case of the leadframe 10 manufactured by the manufacturing method, the lead part 100 may be formed in finer

pattern, and the semiconductor chip package 20 having the leadframe 10 may be formed more thinly.

[58] FIGS. 5 through 16 are cross-sectional views for illustrating a method for manufacturing the leadframe and the semiconductor chip package shown in FIG. 4.

[59] As shown in FIG. 5, a leadframe substrate 150 made of metal is prepared. Herein, the leadframe substrate 150 may be formed of a conductive material, such as Cu, Fe, and alloys thereof. The leadframe 150 may have a thickness range of 1-10 mil (1 mil = 1/1000 inch), preferably, 1-5 mil.

[60] As shown in FIG. 6, a photo resist 140 is coated on an upper surface and a lower surface of the leadframe substrate 150, and is then patterned by using masks 170 and 172. By the patterning, first photo resist patterns 142a and 142b are formed as shown in FIG. 7.

[61] Concretely, as shown in FIG. 5, the photo resist 140 is formed on the upper surface and the lower surface of the leadframe 150. At this time, the photo resist 140 may be formed by using a liquid photo resist (LPR), a dry film resist (DFE), or the like. A photolithography process using the masks 170 and 172 is performed with respect to the upper surface and the lower surface of the leadframe substrate 150 to expose and develop the photo resist 140.

[62] Each of the masks 170 and 172 includes an opaque region having a light shielding layer formed on a quartz substrate, and a transparent region composed of only the quartz substrate. FIGS. 17 and 18 are plane views of the masks used in the process of FIG. 6. For simple discrimination, the opaque region S1 is expressed by black in FIGS. 17 and 18.

[63] The transparent regions S2 of the mask 170 over the leadframe substrate 150 are positioned corresponding to portions where a lead 121 and an inner lead 122 are being formed as shown in FIG. 17, and transmit ultraviolet during the exposure process. Portions of the photo resist 140 corresponding to the transparent regions S2 are removed during the developing process, so that a first photo resist pattern 142a is formed as shown in FIG. 7.

[64] The transparent regions of the mask 172 below the leadframe substrate 150 are positioned corresponding to portions where an outer lead 124 is being formed as shown in FIG. 18, and transmit ultraviolet during the exposure process. Portions of the photo resist 140 corresponding to the transparent regions S2 are removed during the developing process, so that a first photo resist pattern 142b is formed as shown in FIG. 7.

[65] However, the embodiment is not limited thereto. That is, it will be apparent that a photo resist in which a portion which is not exposed to ultraviolet is removed may be used.

[66] Next, as shown in FIG. 8, a lead 121, an inner lead 122 and an outer lead 124 are re-

spectively formed on the upper surface and the lower surface of the leadframe substrate 150 on which the first photo resist pattern 142. The lead 121, the inner lead 122 and the outer lead 124 may be formed by plating a metal material in openings of the first photo resist pattern 142. As the metal material, nickel (Ni), palladium (Pd), gold (Au), silver (Ag), tin (Sn), copper (Cu), chromium (Cr), and alloys thereof may be used. While the current embodiment exemplarily describes the leadframe including the lead 121, it is possible that the lead 121 is not formed.

[67] Next, as shown in FIG. 9, a photo resist 140a is coated on the upper surface and the lower surface of the leadframe substrate 150 and is then patterned by using masks 174 and 176 positioned over and below the leadframe substrate 150. By the patterning, a second photoresist pattern 144a, 144b is formed as shown in FIG. 10.

[68] Concretely, the photo resist 140a is formed on the upper surface and the lower surface of the leadframe substrate 150. The photo resist 140a on the upper surface and the lower surface of the leadframe substrate 150 is exposed and developed by a photolithography process using the masks 174 and 176.

[69] FIG. 19 is a plane view of the mask 174, which is used in the process of FIG. 9 and positioned over the leadframe substrate 150. For simple discrimination, a transparent region S2 is expressed by black in FIG. 19.

[70] The mask 174 over the leadframe substrate 150 has a transparent region S2, which is positioned at a lead in-between corresponding portion (see W1 of FIGS. 10 and 11) corresponding between the lead 121 and the lead part 122 and between the lead parts 122, and at a cavity corresponding portion W3 corresponding to the cavity (see 106 of FIG. 4). The transparent region S2 transmits ultraviolet during the exposure process. After the developing process is completed, a second photo resist pattern 144a is formed at a region corresponding to the opaque region S1, as shown in FIG. 10.

[71] The mask 176 below the leadframe substrate 150 has the same shape as the mask 174 shown in FIG. 18. That is, the transparent region S2 is positioned at an etch corresponding portion (see W2 of FIGS. 10 and 11) where the etched portion is formed, and transmits ultraviolet during the exposure process. By the exposure process, after the developing process is completed, a second photo resist pattern 144b is formed at a region except for the etch corresponding portion W2, as shown in FIG. 10.

[72] However, the embodiment is not limited thereto. That is, it will be apparent that a photo resist in which a portion which is not exposed to ultraviolet is removed may be used.

[73] Next, as shown in FIG. 11, a first etching process is performed by using the photo resist pattern 144a, 144b respectively formed on the upper surface and the lower surface of the leadframe substrate 150. For reference, a dotted portion shown in FIG. 11 indicates an adjacent portion.

- [74] Concretely, the lead in-between corresponding portion W1 and the cavity corresponding portion W3 are partially etched by using the second photo resist pattern 144a as a mask. The lower surface of the leadframe substrate 150 is etched by a thickness by using the second photo resist pattern 144b as a mask to form the etched portion 112. Preferably, when the leadframe substrate 150 is 5 mil (=127 μm) thick, the etched portion 112 may have a depth of 65-90 μm . At this time, the etched portion 112 may have a depth of 70-90 μm .
- [75] That is, a ratio of the thickness of the leadframe substrate 150 (or leadframe 10) : the depth of the etched portion 112 may be 127:65-127:90. Alternatively, the ratio of the thickness of the leadframe substrate 150 (or leadframe 10) : the depth of the etched portion 112 may be 127:70-127:90. However, the embodiment is not limited thereto.
- [76] Next, as shown in FIG. 12, the second photo resist pattern 144a, 144b remaining on the upper surface and the lower surface of the leadframe substrate 150 is removed.
- [77] Next, as shown in FIG. 13, an insulating material is filled in the etched portion 112 to form a supporting part 110. As the insulating material, photo soldering resist (PSR), resin coated copper (RCC), prepreg (PP), epoxy, etc., may be used.
- [78] To form the supporting part 110 by filling the insulating material in the etched portion 112, various methods may be applied. As one example, in the case where PSR is used as the insulating material, after the PSR is deposited, the PSR on a region except for the etched portion may be removed by exposure and development. In the case where RCC, PP or epoxy is used as the insulating material, an insulating material 110a is pressed on the lower surface of the leadframe substrate 150 as shown in FIG. 20, and then the insulating material 110a is polished to expose the outer lead 124, thereby forming the supporting part 110, as shown in FIG. 21.
- [79] As shown in FIG. 14, except for regions where the lead 121 and the inner lead 122 are formed, the upper surface of the leadframe substrate 150 is secondly etched. By the second etching, the cavity corresponding portion W3 is further etched to form a cavity 106 having a predetermined depth. The lead in-between corresponding portion W1 is etched to a portion where the supporting part 110 is formed, and thus the lead 121 and the inner lead 122 are insulated from each other and the inner leads 122 are insulated from each other. Also, a region W3 of the lead part 100 where the lead 121 and the inner lead 122 are not formed may be etched to reduce the width and thickness of the lead part 100 (more precisely, some of the horizontal part 102 and the vertical part 104).
- [80] That is, in this embodiment, after the step of removing the second photo resist pattern 144a, 144b and forming the supporting part 110, secondly etching the leadframe substrate 150 is performed in order to electrically insulate the lead parts 100. Thus, the width and thickness of the lead parts 100 can be further reduced. Accordingly, a finer

pattern can be obtained.

- [81] As one example, when the leadframe substrate 150 is formed at a thickness of 5 mil, the upper surface of the leadframe substrate 150 is partially etched by 30 μm during the first etching process of FIG. 11 and the lower surface of the leadframe substrate 150 is partially etched by 65 μm , thereby capable of constituting the supporting part 110. Thereafter, in the second etching process shown in FIG. 14, the upper surface of the leadframe substrate 150 may be further etched by 30 μm . Accordingly, in the portion where the lead 121 and the inner lead 122 are not formed, the horizontal part 102 may be formed in a thin layer having a thickness of about 30 μm .
- [82] As above-described, the processes described with reference to FIGS. 5 through 14, the leadframe 10 may be formed. FIGS. 15 and 16 are cross-sectional views illustrating the semiconductor chip package using the leadframe 10.
- [83] As shown in FIG. 15, the semiconductor chip 120 is mounted in the cavity 106, and then the semiconductor chip 120 and the inner lead 122, and the semiconductor chip 120 and the lead 121 are electrically connected using wires 126. At this time, the semiconductor chip 120 may be bonded in the cavity 106 by using glue.
- [84] Next, as shown in FIG. 16, the semiconductor chip 120 and the wire 126 are sealed by using a sealant 130 to form the semiconductor chip package 20. The sealant 130 may be composed of a material including a mold resin, an epoxy mold compound (EMC), etc.
- [85] Hereinafter, a semiconductor chip package including a lead frame and a method for manufacturing the same according to a second embodiment will be described in detail. For convenience of description, description on the same constitutions as and very similar constitutions to those of the first embodiment will be omitted and only a different constitution will be described. Like or similar reference numerals refer to like elements throughout.
- [86] FIG. 22 is a cross-sectional view taken along line I-I' of FIG. 2 in a semiconductor chip package using the leadframe shown in FIGS. 2 and 3 according to a second embodiment.
- [87] Referring to FIG. 22, in this embodiment, a supporting part 110 is protruded compared with an outer lead 124. By protruding the supporting part, the protruded supporting part 110 functions as an aligning member when an external circuit is connected to the outer lead 124. Also, such a structure is formed by a manufacturing method that can prevent a lead 121 and an inner lead 122 from being damaged during a second etching process. Accordingly, according to this embodiment, a damage of the lead 121 and the inner lead 122 can be prevented.
- [88] Hereinafter, a method for manufacturing a leadframe and a semiconductor package shown in FIG. 22 will be described with reference to FIGS. 23 through 36. FIGS. 23

through 36 are cross-sectional views illustrating an example of a method for manufacturing the leadframe and the semiconductor chip package shown in FIG. 22.

[89] As shown in FIG. 23, a leadframe substrate 150 made of metal is prepared.

[90] Next, as shown in FIG. 24, a photo resist 140 is coated on an upper surface and a lower surface of the leadframe substrate 150, and is then patterned by using masks 170 and 172. By the patterning, first photo resist patterns 142a and 142b are formed as shown in FIG. 25.

[91] Next, as shown in FIG. 26, a lead 121 and an inner lead 122 are formed on the upper surface of the leadframe substrate 150, and an outer lead 124 is formed on the lower surface of the leadframe substrate 150.

[92] Next, as shown in FIG. 27, a photo resist 140a is coated on the upper surface and the lower surface of the leadframe substrate 150 and is then patterned by using masks 174 and 176 to form a second photoresist pattern 144a, 144b as shown in FIG. 28.

[93] Next, as shown in FIG. 29, a first etching process is performed by using the photo resist pattern 144a, 144b respectively formed on the upper surface and the lower surface of the leadframe substrate 150. By the first etching process, a cavity corresponding portion W3 of the upper surface of the leadframe substrate 150 is partially etched, and a lead in-between corresponding portion W1 is partially etched. Also, an etched portion 112 is formed at an etch corresponding portion W2 of the lower surface of the leadframe substrate 150.

[94] Next, as shown in FIG. 30, an insulating material is filled in the etched portion 112 to form a supporting part 110. To form the supporting part 110 by filling the insulating material in the etched portion 112, various methods may be applied. As one example, in the case where PSR is used as the insulating material, after the PSR is deposited, the PSR on a region except for the etched portion may be removed by exposure and development. In the case where RCC, PP or epoxy is used as the insulating material, an insulating material 110a is pressed on the lower surface of the leadframe substrate 150 as shown in FIG. 35, and then the insulating material 110a is polished to expose the outer lead 124, thereby forming the supporting part 110, as shown in FIG. 36.

[95] Next, as shown in FIG. 31, a second etching process using the second photo resist pattern formed on the upper surface of the leadframe substrate 150 as a mask is performed. By the second etching process, the upper surface of the leadframe substrate 150 is etched. Accordingly, the cavity corresponding portion W3 is further etched to form a cavity 106 having a predetermined depth. The lead in-between corresponding portion W1 is etched to a portion where the supporting part 110 is formed, and thus the lead 121 and the inner lead 122 are insulated from each other and the inner leads 122 are insulated from each other.

[96] Next, as shown in FIG. 32, the second photo resist pattern 144a, 144b remaining on

the upper surface and the lower surface of the leadframe substrate 150 is removed to form a leadframe 10.

[97] The second embodiment has a difference from the first embodiment in that in the second embodiment, the second photo resist pattern 144a, 144b is removed after the second etching process (FIG. 31) of the leadframe substrate 150, but in the first embodiment, the second photo resist pattern 144a, 144b is removed before the second etching process (FIG. 14) of the leadframe substrate 150. Herein, since the second photo resist pattern 144a, 144b is removed after the supporting part 110 is formed, the supporting part 110 is protruded compared with the outer lead 124. In the second embodiment, since the second etching process is performed in a state that the second photo resist pattern 144a covers the lead 121 and the inner lead 122, the lead 121 and the inner lead 122 can be prevented from being damaged during the second etching process.

[98] Next, the processes shown in FIGS. 33 and 34 are performed to form a semiconductor chip package 20. That is, as shown in FIG. 33, the semiconductor chip 120 is mounted in the cavity 106, and then the semiconductor chip 120 and the lead 121, and the semiconductor chip 120 and the inner lead 122 are electrically connected using a wire 126. Next, as shown in FIG. 34, the leadframe 10, the semiconductor chip 120 and the wire 126 are sealed together by using a sealant 130 to form the semiconductor chip package 20.

[99] Hereinafter, another example of a method for manufacturing a leadframe and a semiconductor chip package according to a second embodiment will be described with reference to FIGS. 37 through 49. FIGS. 37 through 49 are cross-sectional views illustrating another example of a method for manufacturing a semiconductor chip package according to a second embodiment.

[100] As shown in FIG. 37, a leadframe substrate 150 made of metal is prepared.

[101] As shown in FIG. 38, a photo resist 140 is coated on an upper surface and a lower surface of the leadframe substrate 150, and is then patterned by using masks 170 and 172. By the patterning, a first photo resist pattern 142 is formed as shown in FIG. 39.

[102] As shown in FIG. 40, a lead 121 and an inner lead 122 are formed on the upper surface of the leadframe substrate 150, and an outer lead 124 is formed on the lower surface of the leadframe substrate 150.

[103] Next, as shown in FIG. 41, a photo resist 140b is coated on the upper surface and the lower surface of the leadframe substrate 150 and is then patterned by using masks 174 and 176 to form a second photoresist pattern 144b, 144c, as shown in FIG. 42. In this embodiment, a dry film resist (DFR) is used as the photo resist 140b. At this time, the DFR may be formed in a stack structure including a photosensitive material layer 242 and a protective film 240 stacked on the photosensitive material layer 242.

- [104] Referring to FIG. 42, the second photo resist pattern 144c on the upper surface of the leadframe substrate 150 is used in a state that the protective film 240 is removed, and the photo resist pattern 144b on the lower surface of the leadframe substrate 150 is used in a state that the protective film 240 is removed. The photosensitive material layer 242 of the second photoresist pattern 144c on the upper surface of the leadframe substrate 150 includes a pattern 242a reacted with ultraviolet, and a pattern 242b not reacted with ultraviolet.
- [105] As shown in FIG. 43, the lower surface of the leadframe substrate 150 is first etched by using the second photo resist pattern 144b on the lower surface of the leadframe substrate 150 as a mask, to form an etched portion 112. The present embodiment has a difference from the previous embodiment in that the upper surface of the leadframe substrate 150 is not etched during the first etching process.
- [106] As shown in FIG. 44, an insulating material is filled in the etched portion 112 to form a supporting part 110.
- [107] As shown in FIG. 45, the protective film 240 over the upper surface of the leadframe substrate 150 is removed and then the photosensitive material layer 242 is developed. By the developing, only the pattern 242b which is not reacted with ultraviolet is left.
- [108] As shown in FIG. 46, the upper surface of the leadframe substrate 150 is etched by a second etching process using the pattern 242b which is not reacted with ultraviolet, as a mask. By the second etching process, a cavity corresponding portion W3 is etched, so that a cavity 106 is formed. Also, a lead in-between corresponding portion W1 is etched to the supporting part 110, so that the lead 121 and the inner lead 122 are insulated from each other and the inner leads 122 are insulated from each other.
- [109] As shown in FIG. 47, the second photo resist pattern 144b and the pattern 242b not reacted with ultraviolet, which remain on the upper surface and lower surface of the leadframe substrate 150, are removed, thereby forming a leadframe 10.
- [110] As shown in FIGS. 48 and 49, the semiconductor chip 120 is mounted and then bonded using a wire 126. Thereafter, the semiconductor chip 120 is sealed by using a sealant 130 to form the semiconductor chip package 20.
- [111] While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. Therefore, the scope of the invention is defined not by the detailed description of the invention but by the appended claims.

Claims

- [Claim 1] A leadframe comprising:
a die pad part where a semiconductor chip is mounted on a first surface of the leadframe;
at least one lead part electrically connecting the semiconductor chip to at least one external circuit; and
at least one supporting part adjacent to a second surface opposited the first surface, the at least one supporting part including an insulating material and insulating the at least one lead part from each other.
- [Claim 2] The leadframe of claim 1, wherein each of the at least one lead part comprises at least one selected from the group consisting of copper (Cu), iron (Fe), and alloys thereof.
- [Claim 3] The leadframe of claim 1, wherein the die pad part includes a cavity corresponding to a region where the semiconductor chip is mounted.
- [Claim 4] The leadframe of claim 1, wherein each of the at least one lead part comprises a horizontal part positioned toward the first surface, and a vertical part extending from the first surface to the second surface, and wherein the leadframe comprises at least one inner lead and at least one outer lead, and
wherein the inner lead is formed on the first surface of the horizontal part, and the outer lead is formed on the second surface of the vertical part.
- [Claim 5] The leadframe of claim 4, wherein a width of the at least one inner lead is smaller than a width of the at least one outer lead.
- [Claim 6] The leadframe of claim 4, wherein in the horizontal part, a portion where the at least one inner lead is positioned is more protruded than a portion where the at least one inner lead is not positioned.
- [Claim 7] The leadframe of claim 4, wherein the at least one inner lead and the at least one outer lead comprises at least material selected from the group consisting of nickel (Ni), palladium (Pd), gold (Au), silver (Ag), tin (Sn), copper (Cu), chromium (Cr), and alloys thereof.
- [Claim 8] The leadframe of claim 5, wherein the at least one supporting part is more protruded than the at least one outer lead.
- [Claim 9] The leadframe of claim 5, wherein a surface of the at least one supporting part and a surface of the at least one outer lead are positioned on the same plane.
- [Claim 10] The leadframe of claim 1, wherein the ratio of a thickness of the

leadframe : a depth of the at least one supporting part is 127:65 to 127:90.

[Claim 11]

A leadframe comprising:

a leadframe substrate having a first surface on which a semiconductor chip is mounted, and a second surface opposite to the first surface, in which a first region comprised of at least one etched portion formed at the second surface, and a second region which is a portion other than the first region are defined; and

at least one supporting part formed in the at least one etched portion of the first region and including an insulating material,

wherein the second region is comprised of at least one lead part connecting the semiconductor chip to at least one external circuit, and a die pad part on which the semiconductor chip is mounted.

[Claim 12]

A method for manufacturing a leadframe, comprising:

preparing a leadframe substrate including a first surface on which a semiconductor chip is being mounted, and a second surface opposite to the first surface;

forming at least one etched portion at a first region of the second surface by etching the leadframe substrate to ; and

forming at least one supporting part by filling an insulating material in the at least one etched portion.

[Claim 13]

The method of claim 12, wherein the leadframe substrate comprises a conductive material, and

a second region other than the first region is comprised of at least one lead part connecting the semiconductor chip to at least one external circuit, and a die pad part on which the semiconductor chip is mounted.

[Claim 14]

The method of claim 13, comprising forming at least one inner lead and at least one outer lead electrically connected to the at least one lead part between the preparing of the leadframe substrate and the forming of the at least one etched portion.

[Claim 15]

The method of claim 14, wherein the forming of the at least one inner lead and the at least one outer lead comprises:

forming a photo resist pattern on the leadframe substrate; and

forming a metal material in openings of the photo resist pattern.

[Claim 16]

The method of claim 13, wherein the forming of the at least one etched portion comprises:

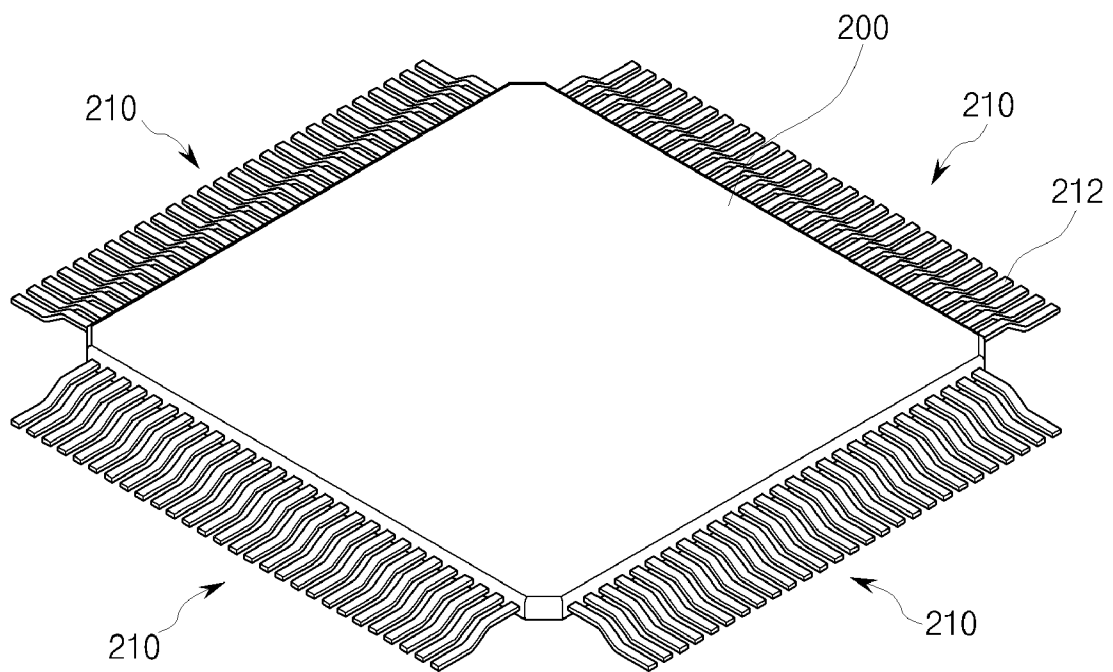
forming a photo resist pattern on the leadframe substrate; and

first etching the second surface of the leadframe substrate by using the

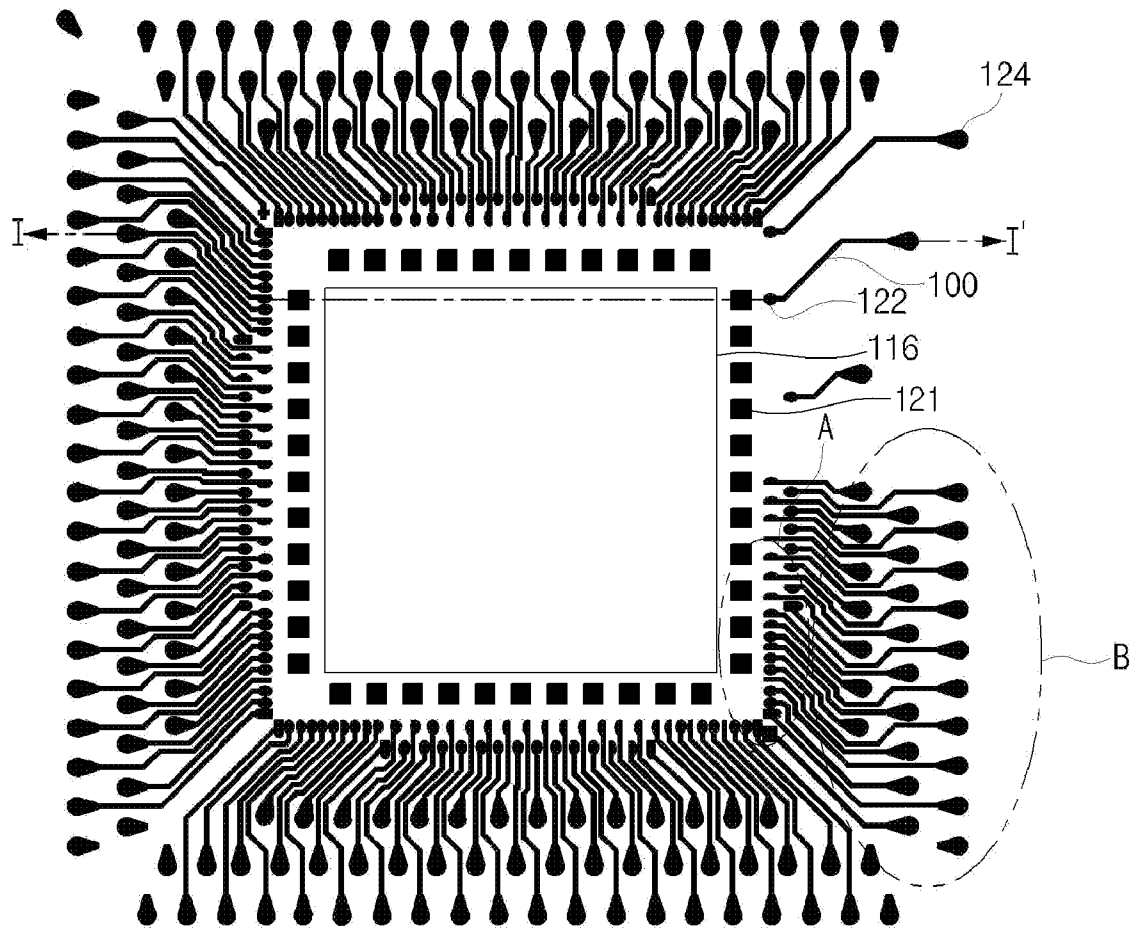
photo resist pattern as a mask.

- [Claim 17] The method of claim 16, after the forming of the at least one supporting part, comprising secondly etching the first surface of the leadframe substrate to insulate the at least one lead part from each other.
- [Claim 18] The method of claim 17, wherein in the secondly etching, a cavity is formed at the first surface of the leadframe substrate, corresponding to a position where the semiconductor chip is being mounted.
- [Claim 19] The method of claim 16, comprising removing the photo resist pattern between the forming of the at least one etched portion and the forming of the at least one supporting part, and comprising secondly etching the first surface of the leadframe substrate to decrease width and thickness of the at least one lead part and to electrically insulate the at least one lead part from each other, after the forming of the at least one supporting part.
- [Claim 20] The method of claim 19, wherein in the secondly etching, a cavity is formed at the first surface of the leadframe substrate, corresponding to a position where the semiconductor chip is being mounted.

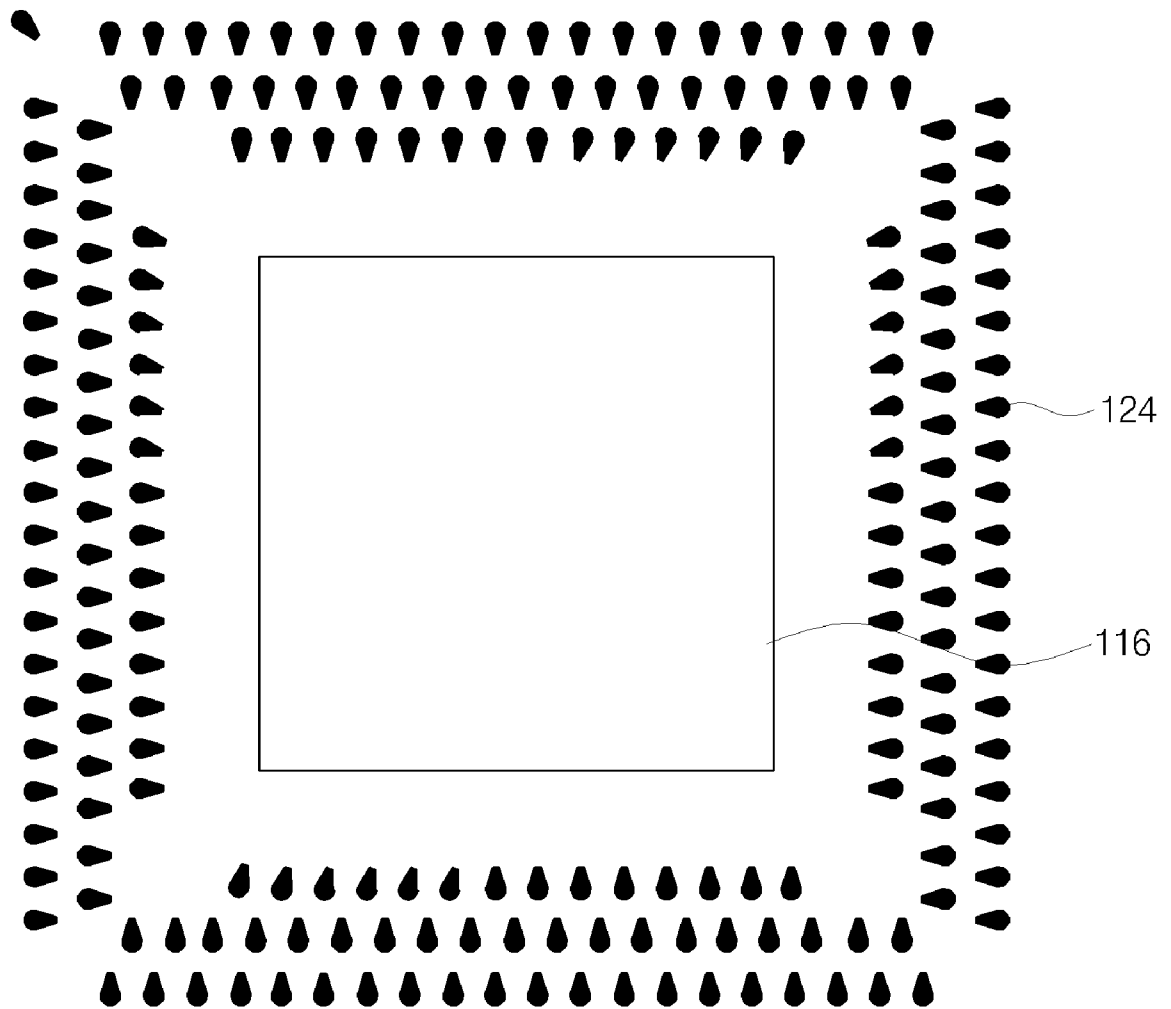
[Fig. 1]



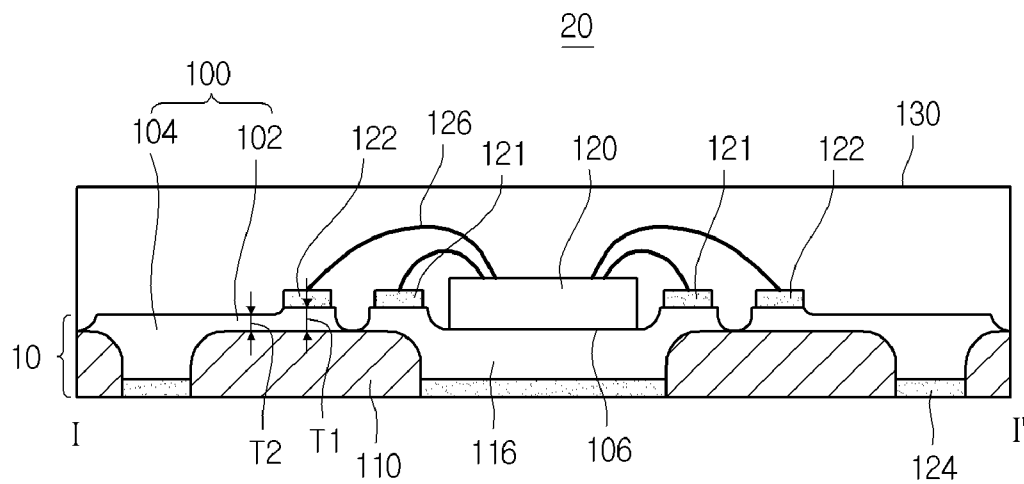
[Fig. 2]



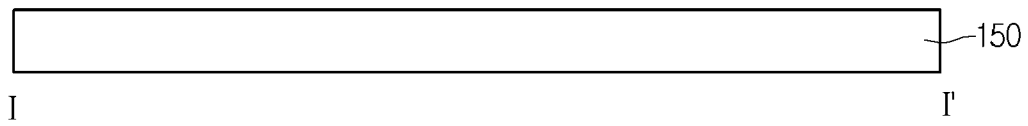
[Fig. 3]



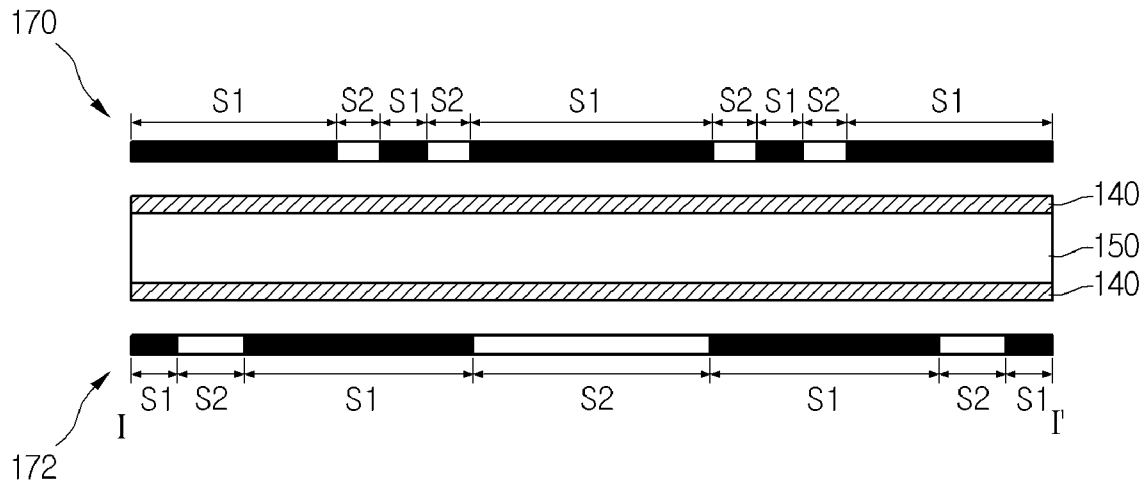
[Fig. 4]



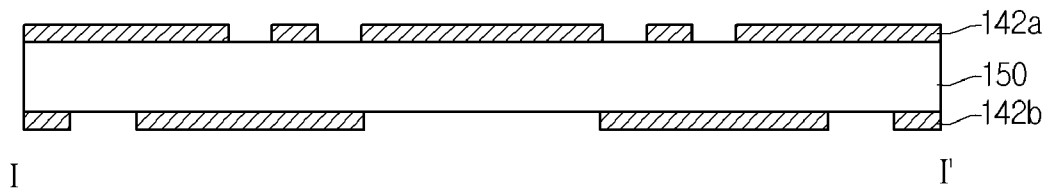
[Fig. 5]



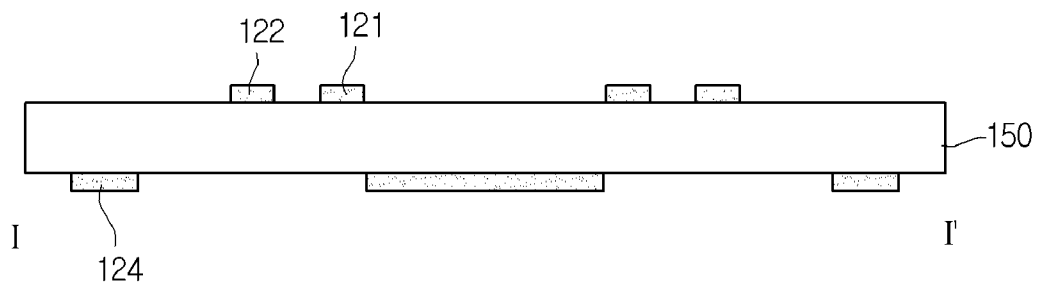
[Fig. 6]



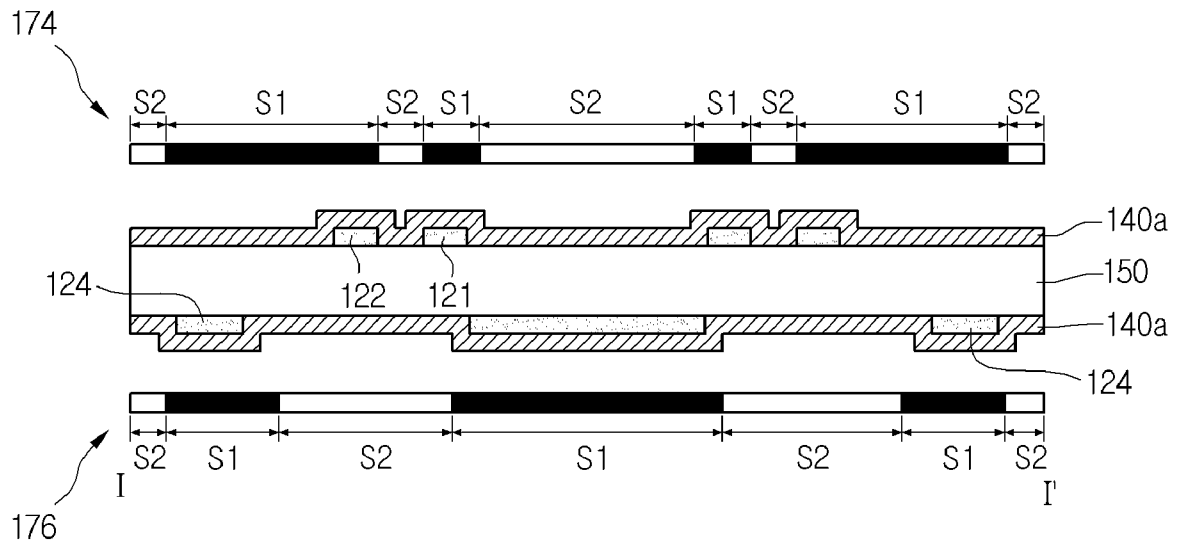
[Fig. 7]



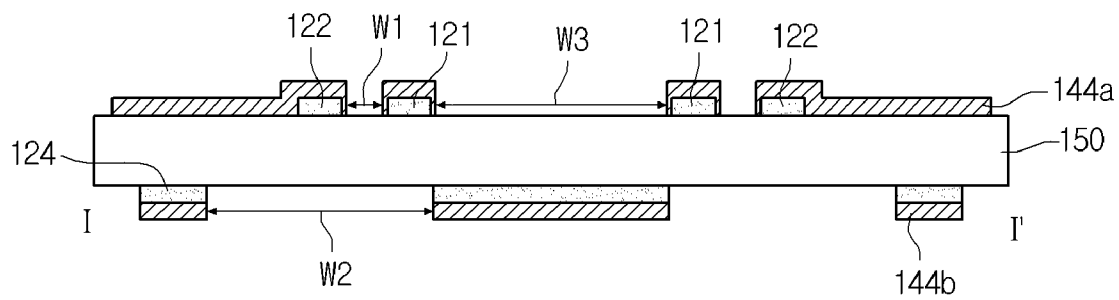
[Fig. 8]



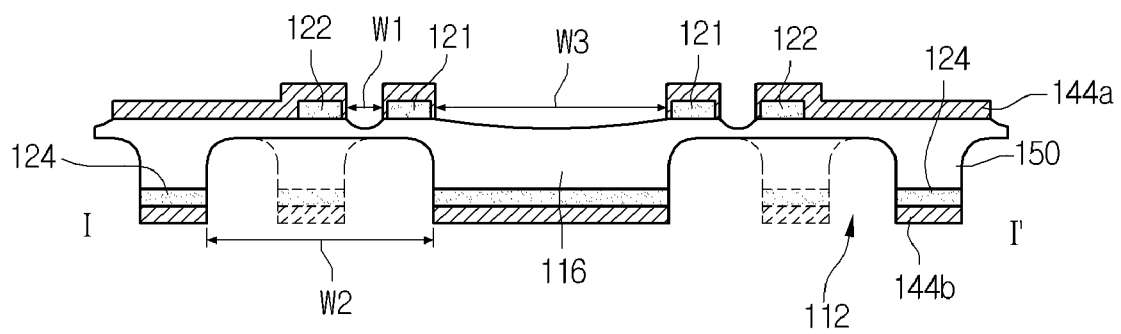
[Fig. 9]



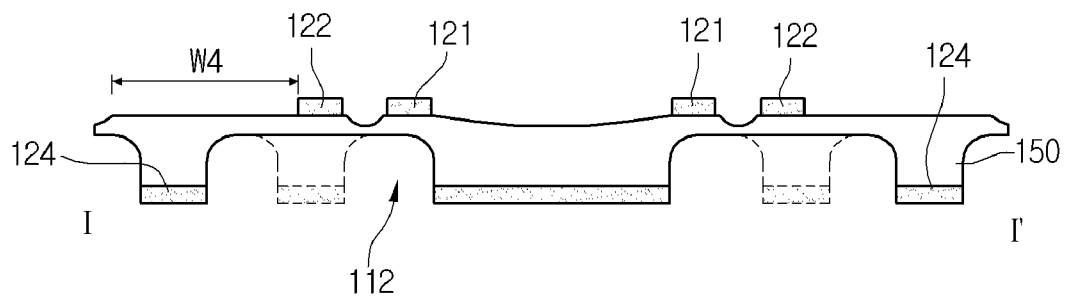
[Fig. 10]



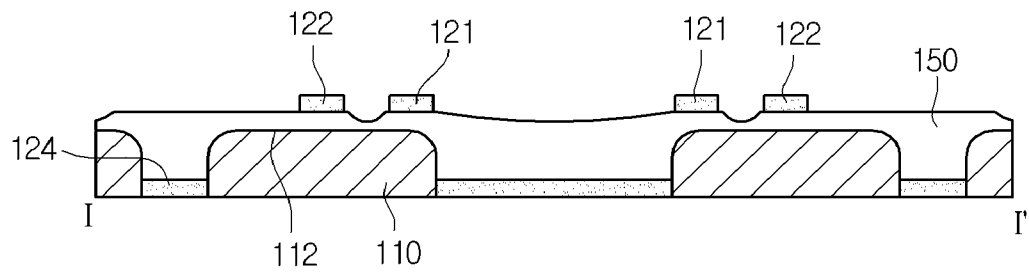
[Fig. 11]



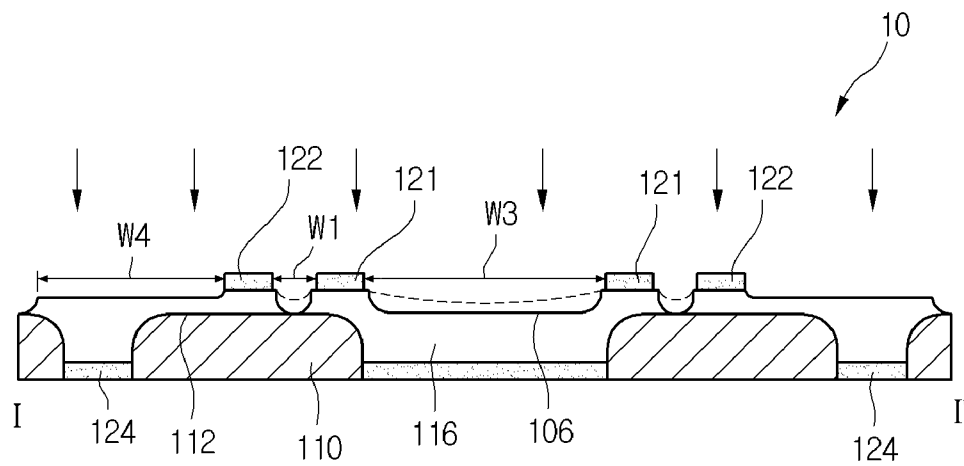
[Fig. 12]



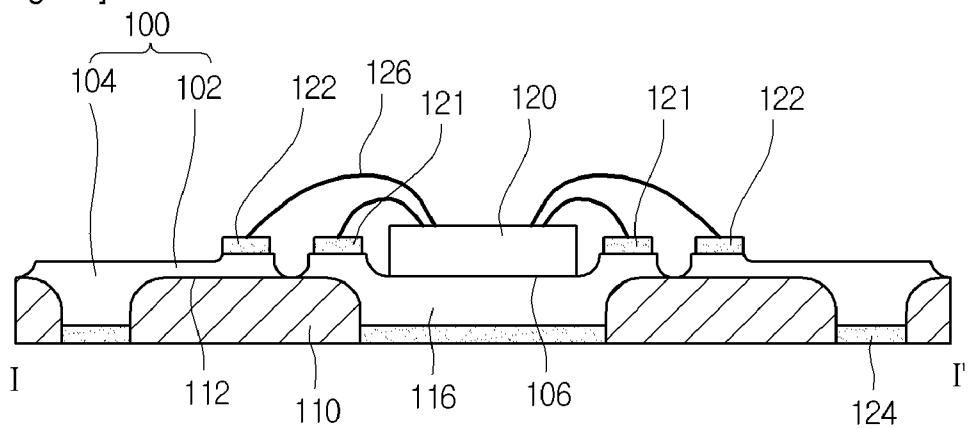
[Fig. 13]



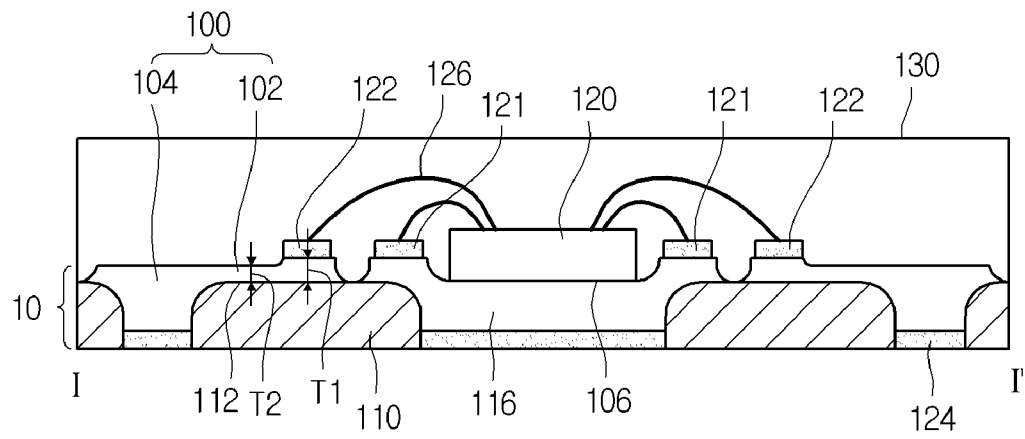
[Fig. 14]



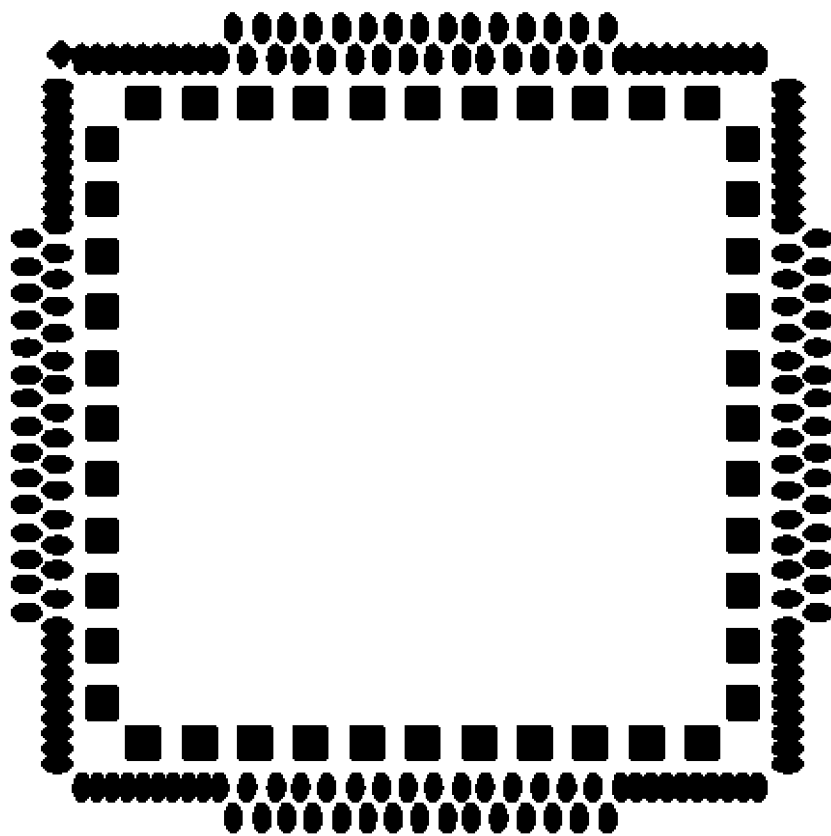
[Fig. 15]



[Fig. 16]

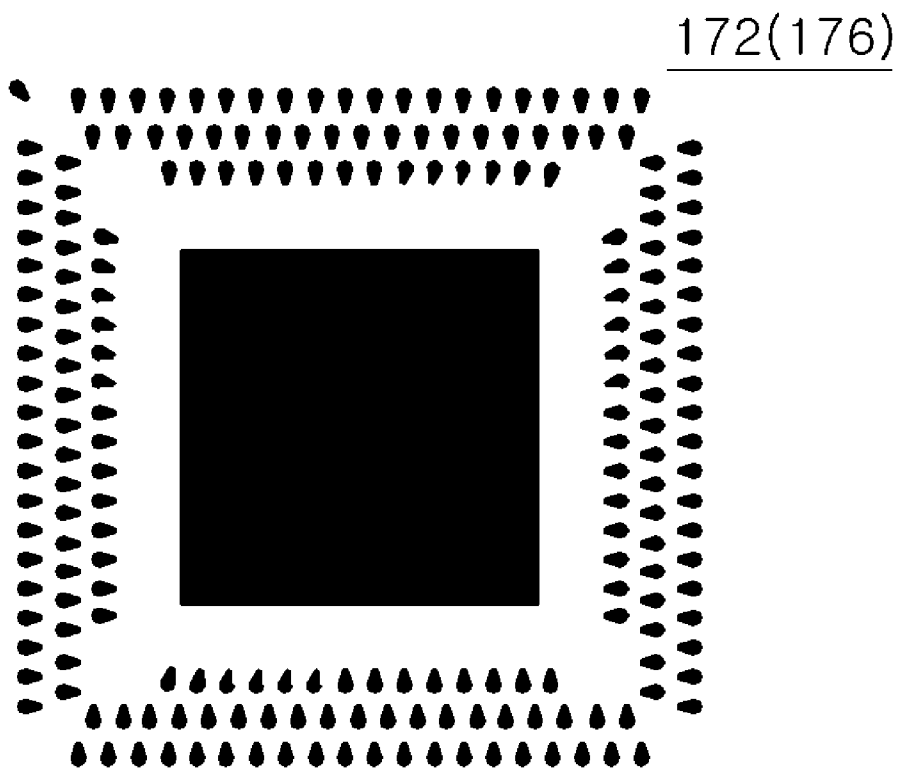


[Fig. 17]

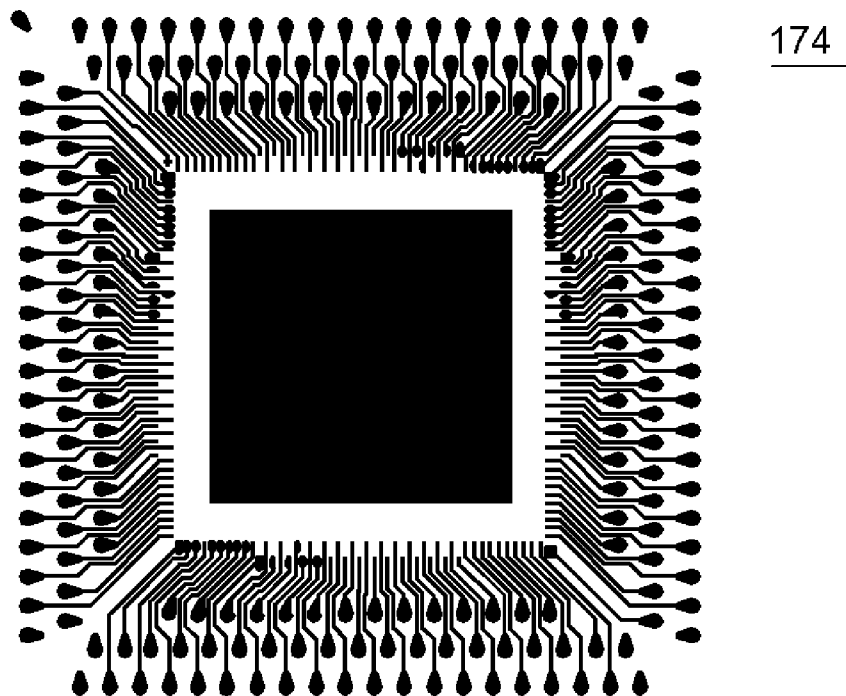


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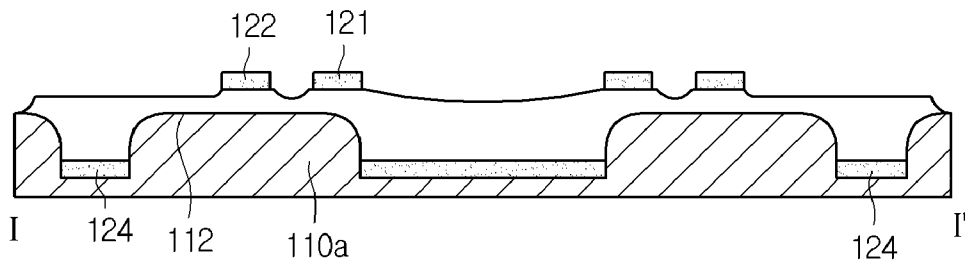
[Fig. 18]



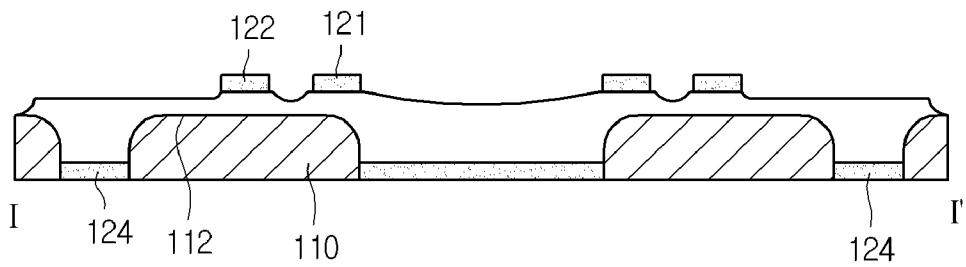
[Fig. 19]



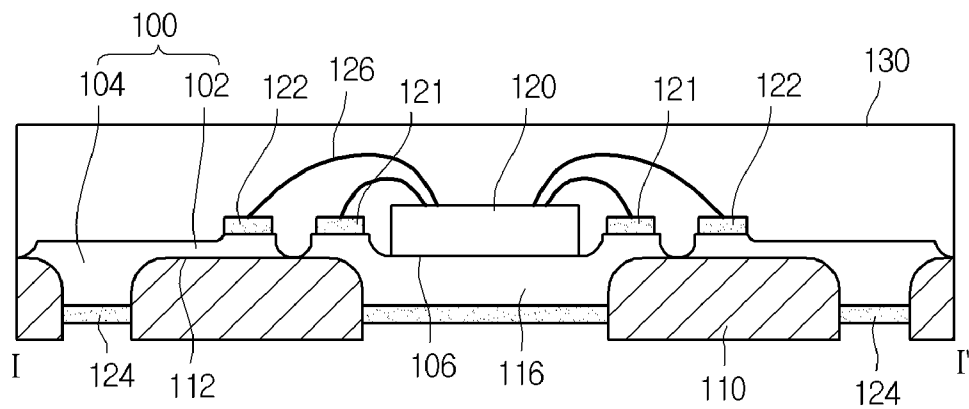
[Fig. 20]



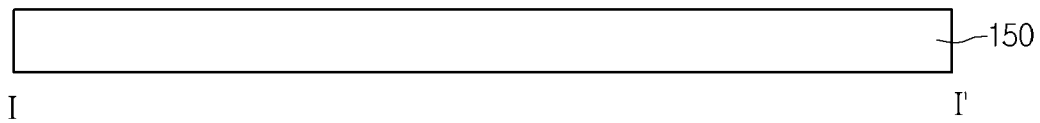
[Fig. 21]



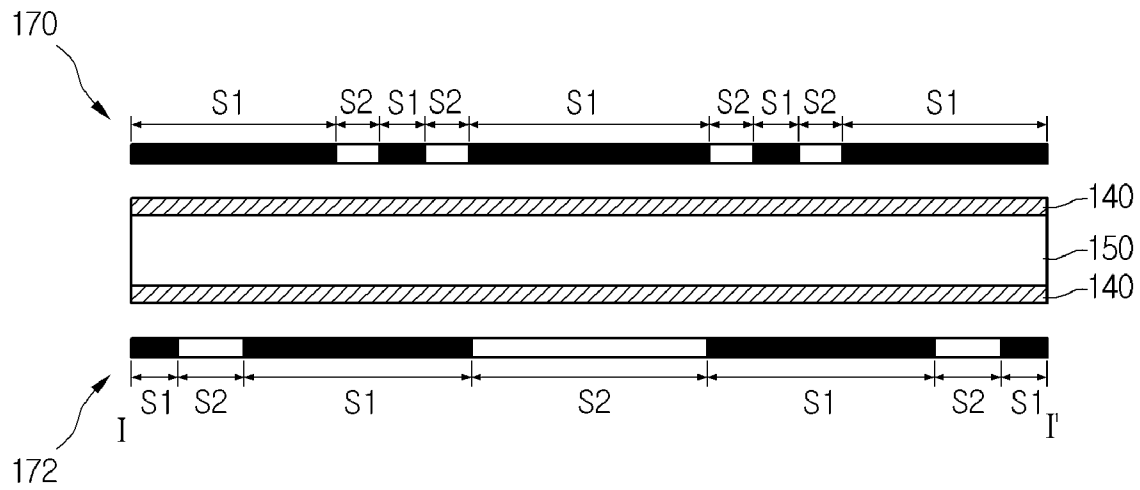
[Fig. 22]



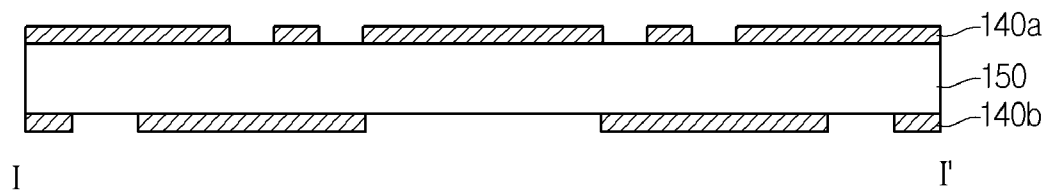
[Fig. 23]



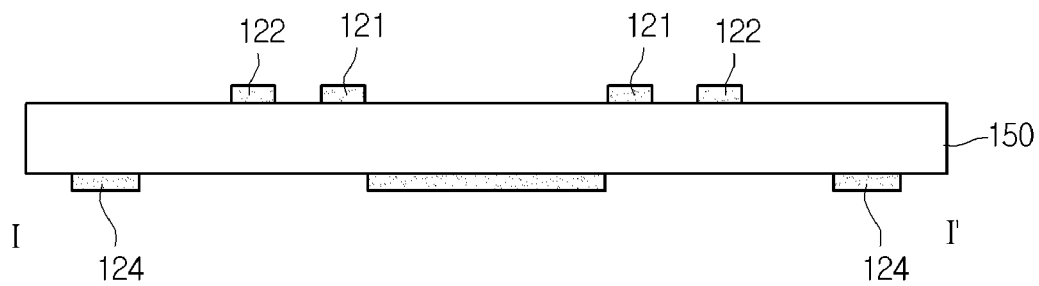
[Fig. 24]



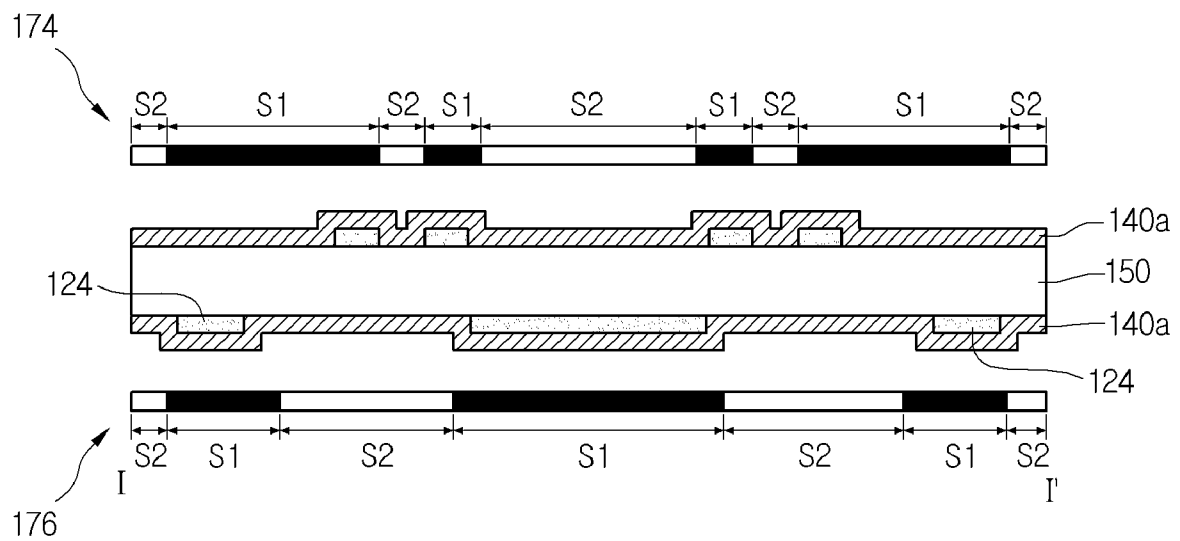
[Fig. 25]



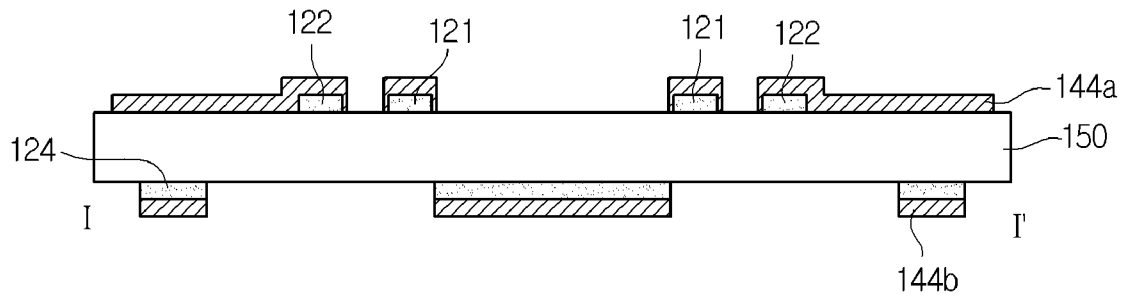
[Fig. 26]



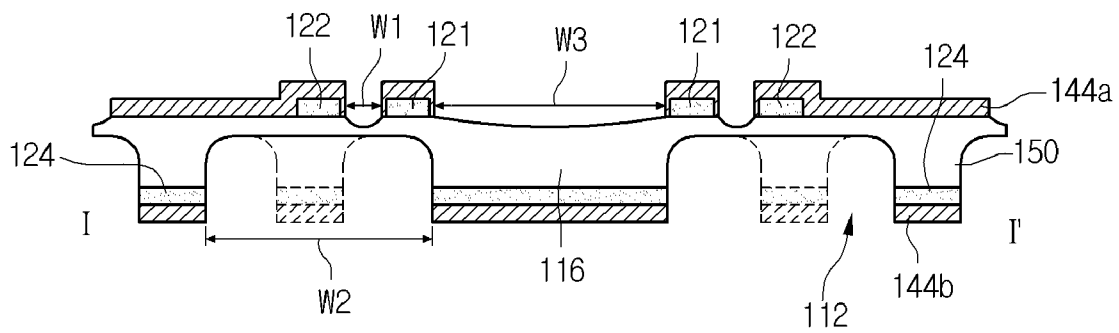
[Fig. 27]



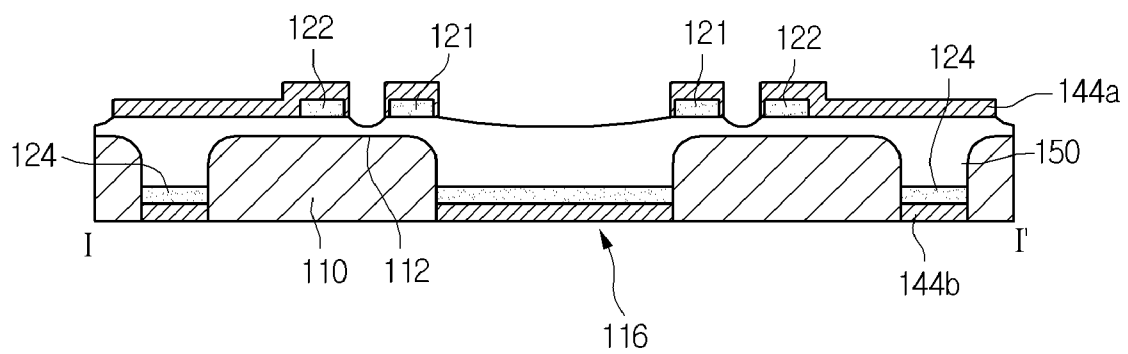
[Fig. 28]



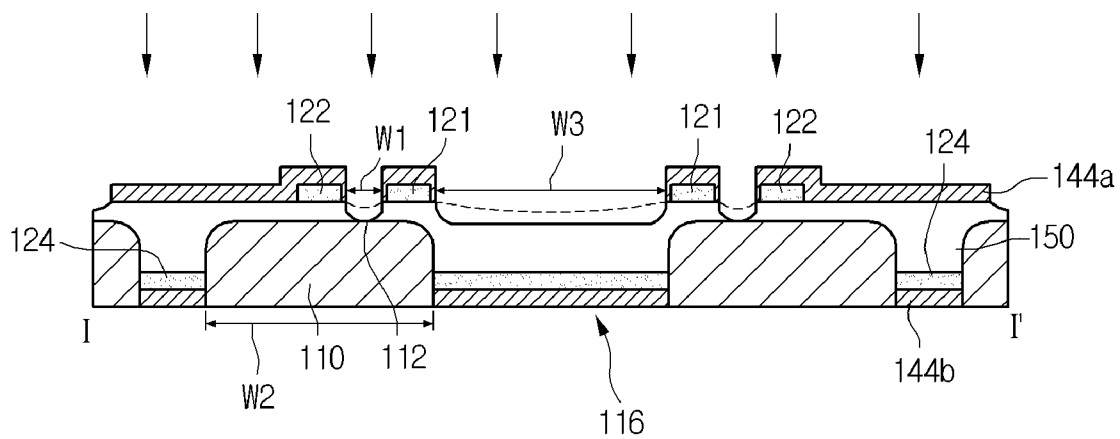
[Fig. 29]



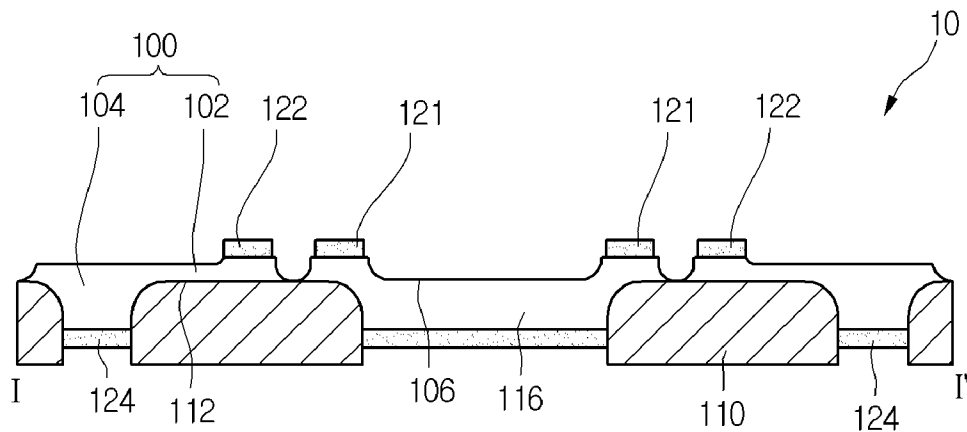
[Fig. 30]



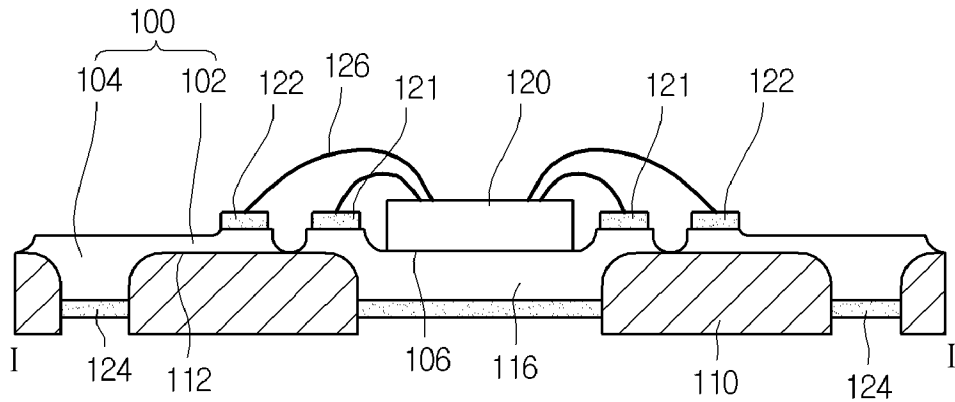
[Fig. 31]



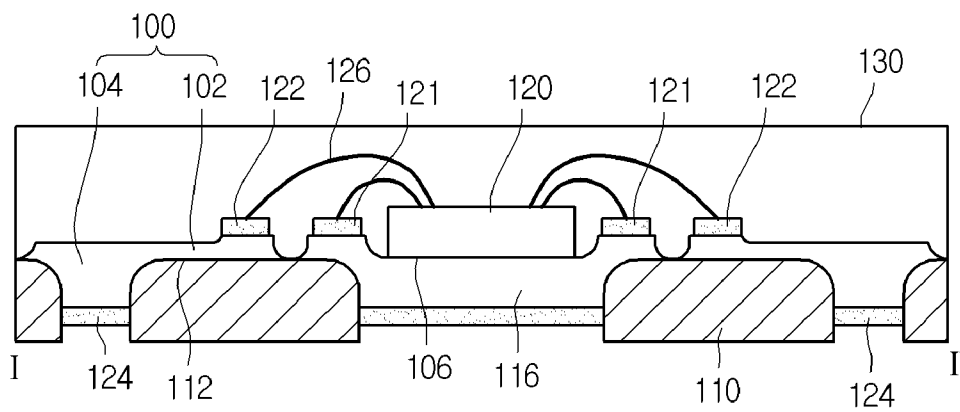
[Fig. 32]



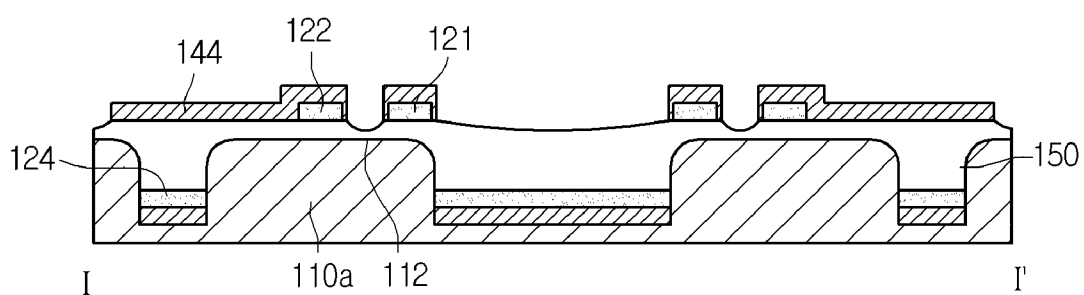
[Fig. 33]



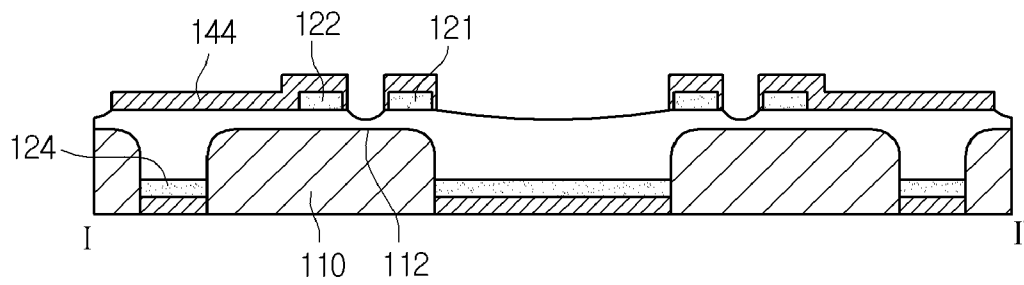
[Fig. 34]



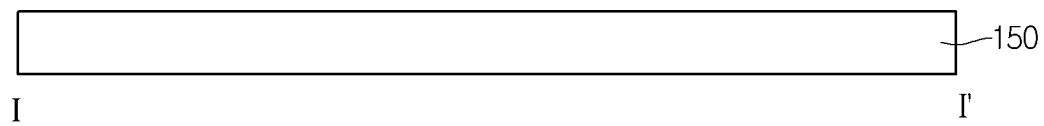
[Fig. 35]



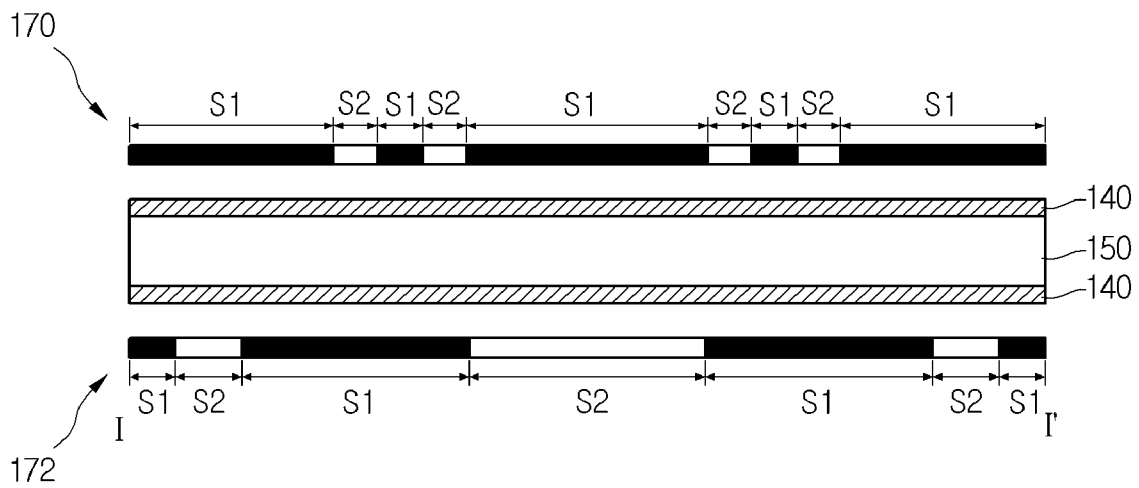
[Fig. 36]



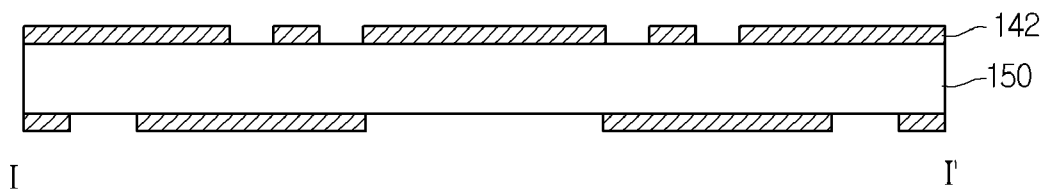
[Fig. 37]



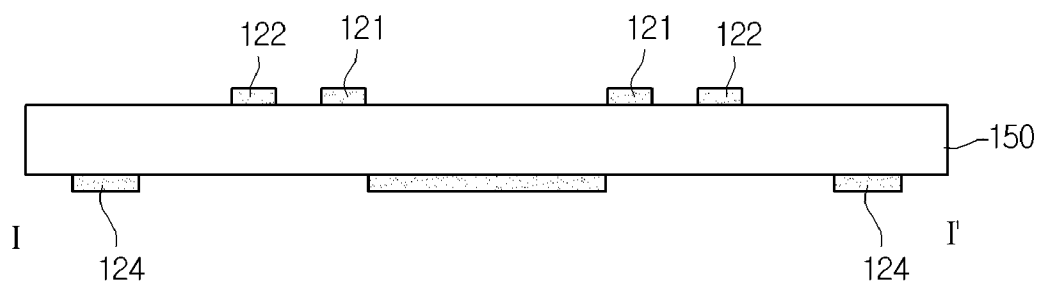
[Fig. 38]



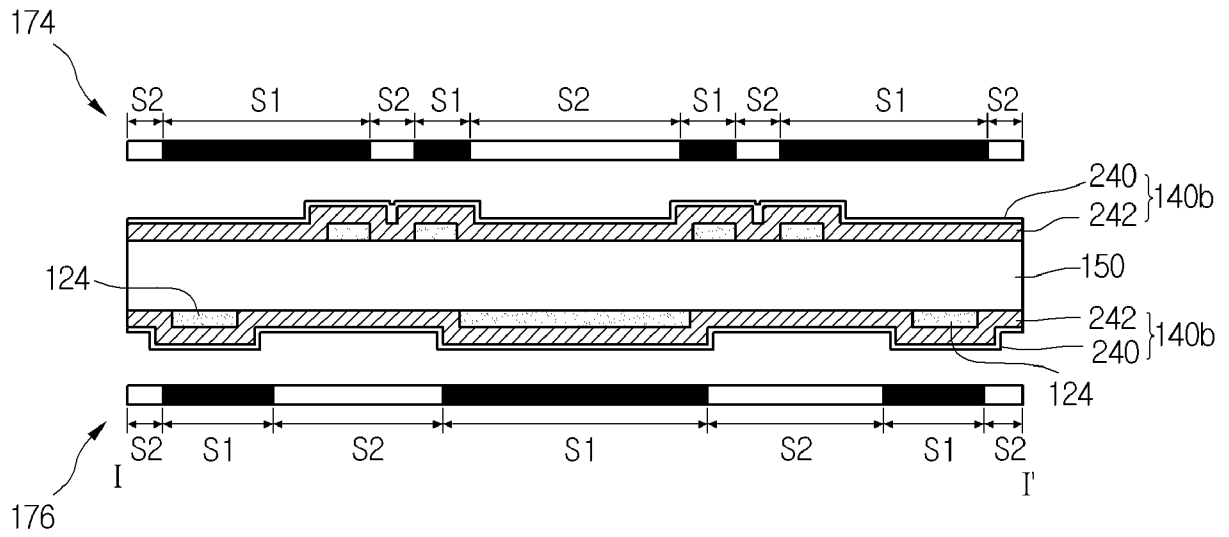
[Fig. 39]



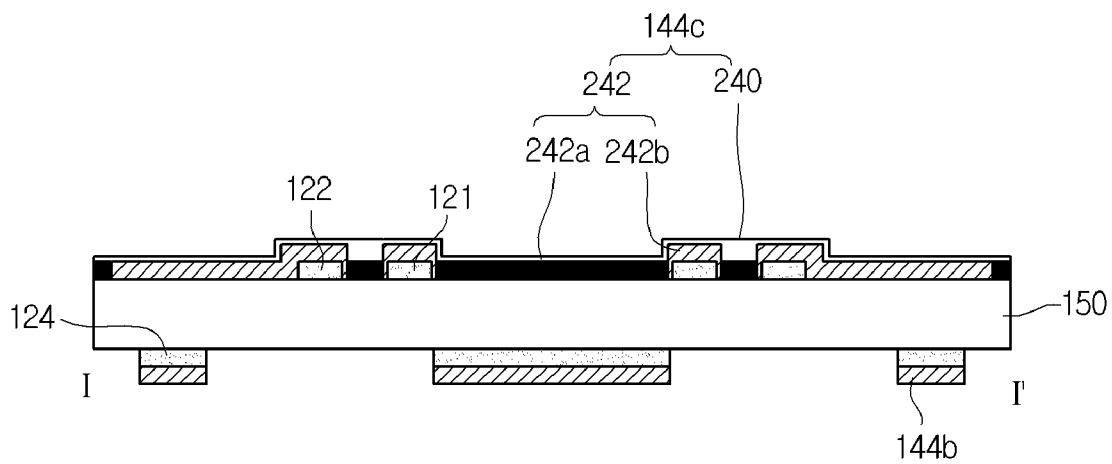
[Fig. 40]



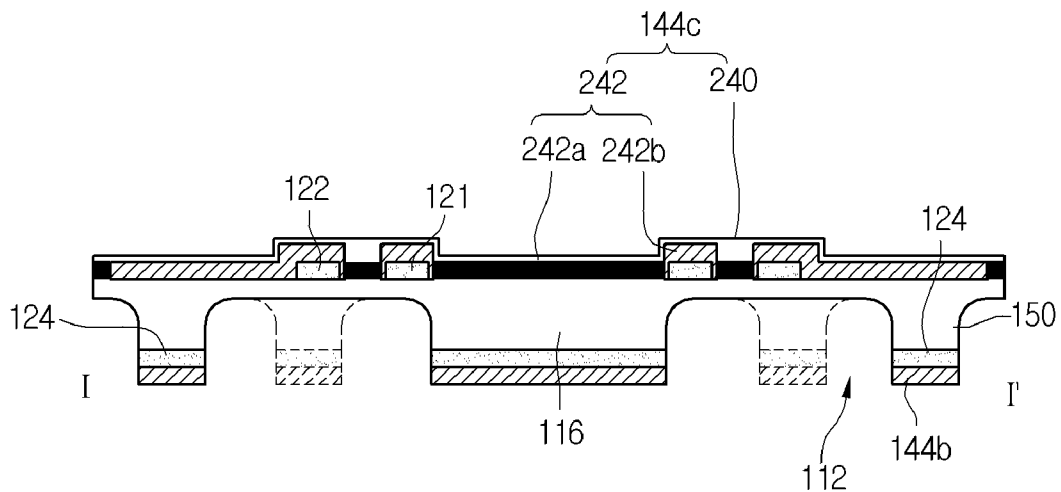
[Fig. 41]



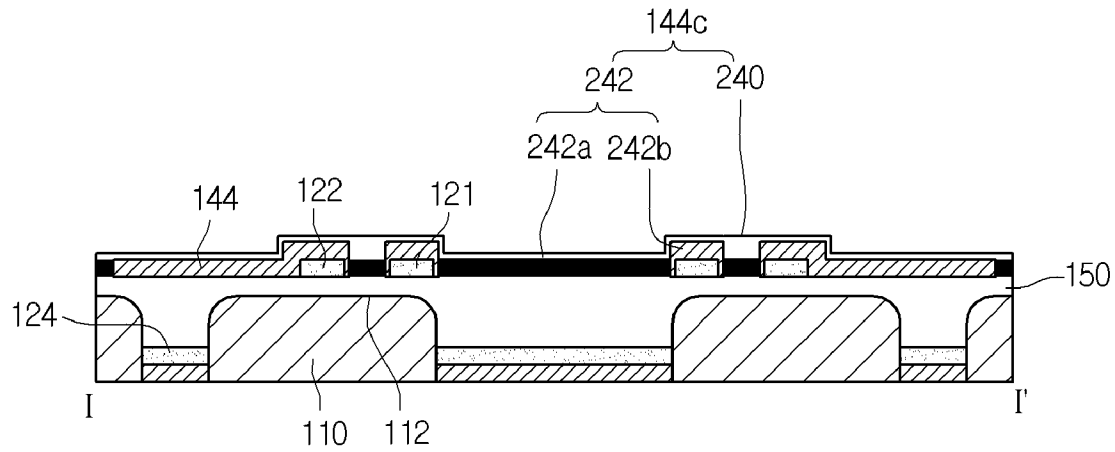
[Fig. 42]



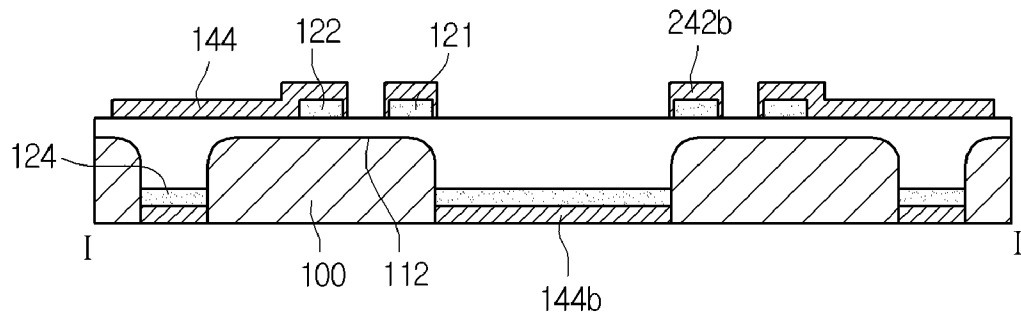
[Fig. 43]



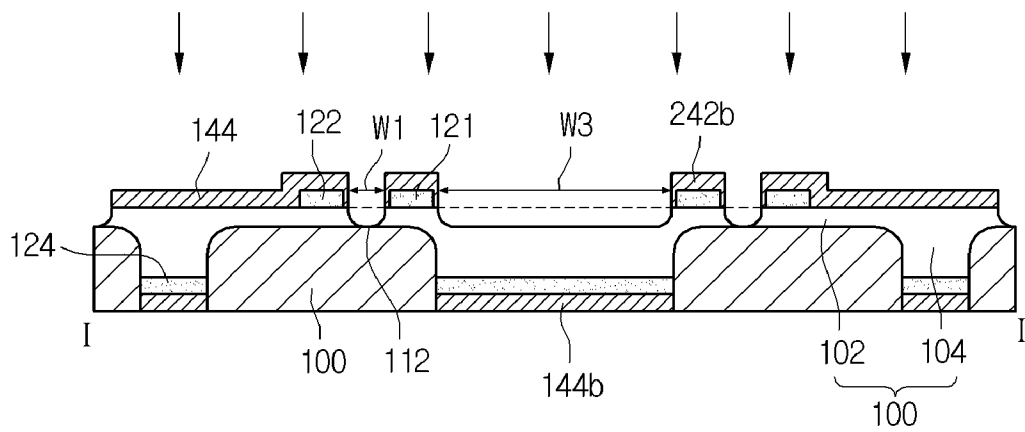
[Fig. 44]



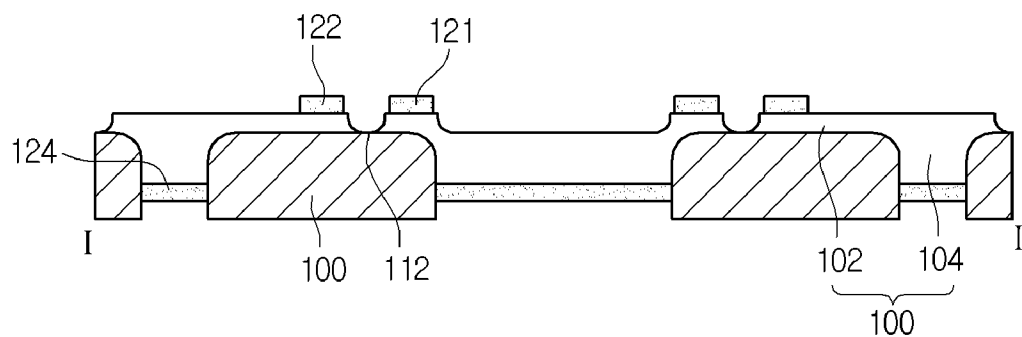
[Fig. 45]



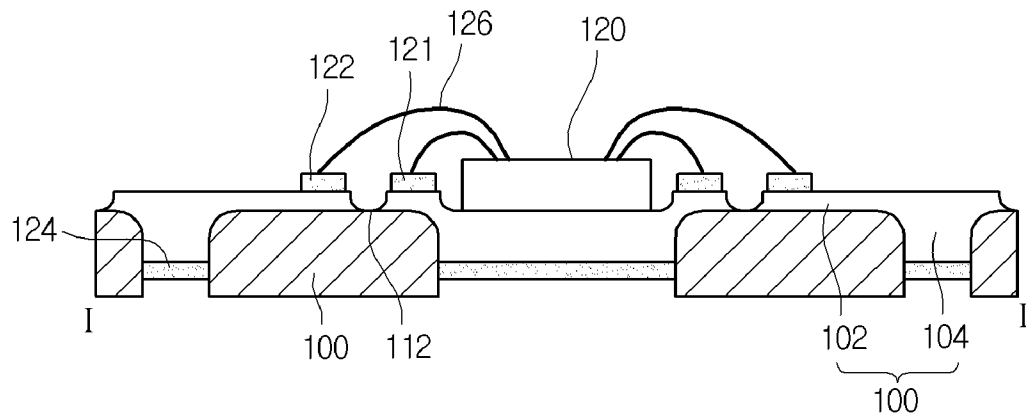
[Fig. 46]



[Fig. 47]



[Fig. 48]



[Fig. 49]

