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(54) **Title:** TEMPERATURE-CONTROLLED WAFER SUPPORT PEDESTAL WITH VACUUM CLAMPING FEATURES

(57) **Abstract:** Pedestals, apparatuses, systems and methods for semiconductor processing are provided. An apparatus may have a pedestal body having a first side and a second side facing in an opposite direction from the first side, a plurality of vacuum clamping channels located on the first side, the vacuum clamping channels fluidically connected with a vacuum passage extending through the pedestal body, the plurality of vacuum clamping channels is configured for vacuum clamping a wafer to the first side of the pedestal body, and a first channel positioned on the second side of the pedestal body, the first channel is configured to receive a first temperature control element that is configured to control a temperature of the pedestal body by actively cooling the pedestal body.

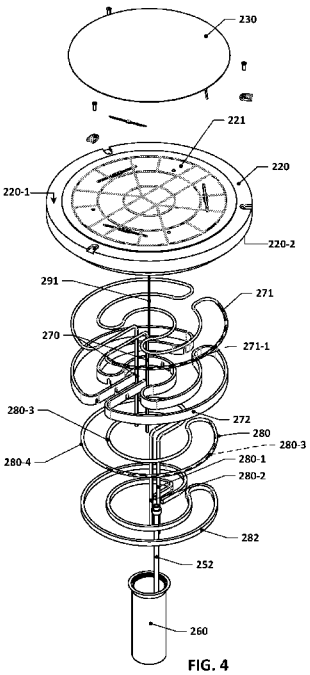

FIG. 4

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TEMPERATURE-CONTROLLED WAFER SUPPORT PEDESTAL WITH VACUUM CLAMPING FEATURES

INCORPORATION BY REFERENCE

[0000] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in their entireties and for all purposes.

BACKGROUND

[0001] Semiconductor manufacturing processes often occur within a chamber in which a semiconductor wafer or semiconductor wafers are supported on pedestals during wafer processing operations. Such a pedestal may be positioned underneath a corresponding gas distribution system, e.g., a showerhead, that may be used to distribute process gases across the exposed side of a semiconductor wafer supported by the pedestal. Disclosed herein are new pedestal designs for use in such processing chambers.

[0002] The background provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent that it is described in this background, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the disclosure.

SUMMARY

[0003] Details of one or more implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings, and the claims.

[0004] In some implementations, an apparatus may include a pedestal body having a first side and a second side facing in an opposite direction from the first side. The apparatus may also include a plurality of vacuum clamping channels located on the first side. The vacuum clamping channels may be fluidically connected with a vacuum passage extending through the pedestal body. The plurality of vacuum clamping channels may be configured for vacuum clamping a wafer to the first side of the pedestal body. The apparatus may further include a

first channel positioned on the second side of the pedestal body. The first channel may be configured to receive a first temperature control element that is configured to control a temperature of the pedestal body by actively cooling the pedestal body.

[0005] In some implementations, the apparatus may further include the first temperature control element. The first channel may have a cross-sectional profile that may include a semicircular segment that contacts at least 50% of an exterior of the first temperature control element.

[0006] In some implementations, the apparatus may further include a second channel positioned on the second side of the pedestal body. The second channel may be configured to receive a second temperature control element that is configured to control a temperature of the pedestal body by heating the pedestal body.

[0007] In some implementations, a bottom of the first channel may be closer in distance to the second side than a bottom of the second channel.

[0008] In some implementations, the apparatus may further include a first insert corresponding to the first channel and configured to compress the first temperature control element into the first channel. The apparatus may further include a second insert corresponding to the second channel and configured to compress the second temperature control element into the second channel.

[0009] In some implementations, the first insert may include a concave surface that faces towards a bottom of the first channel, and the second insert may include a concave surface that faces towards a bottom of the second channel.

[0010] In some implementations, the first channel may follow a first path, the first insert may follow the first path for at least 90% of a length of the first path, and the first insert may be friction stir-welded along the first path to opposing edges of the first channel.

[0011] In some implementations, the first path may encircle at least 60% of a circumference of the pedestal body.

[0012] In some implementations, the second channel may follow a second path, the second insert may follow the second path for at least 90% of a length of the second path, and the second insert may be friction stir-welded along the second path to opposing edges of the second channel.

[0013] In some implementations, the first path may encircle at least 60% of a circumference of the pedestal body.

[0014] In some implementations, the second path may include a C-shaped segment.

[0015] In some implementations, the pedestal body may be connected with a support column that houses: a vacuum port fluidically connected with the plurality of vacuum clamping channels; a coolant passage inlet and a coolant passage outlet that are both fluidically connected with the first temperature control element such that a coolant passage of the first temperature control element is fluidically interposed between the coolant passage inlet and the coolant passage outlet; and resistive heater cables electrically connected with the second temperature control element.

[0016] In some implementations, the coolant passage may have an inner portion and an outer portion radially outwards from the inner portion, the inner portion may be fluidically interposed between the outer portion and the coolant passage outlet, and the outer portion may be fluidically interposed between the inner portion and the coolant passage inlet.

[0017] In some implementations, the coolant passage may have an inner portion and an outer portion radially outwards from the inner portion, the inner portion may be fluidically interposed between the outer portion and the coolant passage inlet, and the outer portion may be fluidically interposed between the inner portion and the coolant passage outlet.

[0018] In some implementations, the apparatus may further include a temperature sensor receiving hole configured to receive a temperature sensor that is configured to monitor a temperature of the pedestal body.

[0019] In some implementations, the plurality of vacuum clamping channels may include concentric vacuum channels, radial vacuum channels, parallel vacuum channels, or any combination thereof.

[0020] In some implementations, wherein when viewing along a direction perpendicular to the first side of the pedestal, the vacuum clamping channels may be positioned entirely within a circular region encircled by an annular seal region. The circular region may be smaller than 300mm in diameter.

[0021] In some implementations, the apparatus may further include a plurality of flexure springs configured to control a clamping force applied to the wafer.

[0022] In some implementations, each flexure spring in the plurality of flexure springs may include a ceramic flexure spring.

[0023] In some implementations, wherein the pedestal body may be made of a metal or a metal alloy.

[0024] In some implementations, wherein the pedestal body may be made of aluminum.

[0025] In some implementations, wherein pedestal body may be made of a single piece of metal.

[0026] In some implementations, the first temperature control element may have a coolant passage configured to flow a coolant therein, and the coolant may be clear dry air.

[0027] In some implementations, the coolant may be flowed through the coolant passage at a flow rate of about 50 slm to about 150 slm.

[0028] In some implementations, the system further has a controller having one or more processors and one or more memories that store instructions that are configured to cause the one or more processors to cause material to be deposited on a wafer on the pedestal body, coolant to flow through the coolant passage at a first flow rate for a first time period during material deposition on the wafer, and coolant to flow through the coolant passage at a second flow rate for a second time period during material deposition on the wafer.

[0029] In some implementations, the first flow rate may be different than the second flow rate.

[0030] In some implementations, the first time period may be the same as the second time period.

[0031] In some implementations, the first time period may be different than the second time period.

[0032] In some implementations, the apparatus may further include a showerhead for distributing gases over a surface of a wafer and a processing chamber. The pedestal body may be positioned within the processing chamber and beneath the showerhead.

[0033] In some implementations, a multi-station semiconductor processing system may be provided. The system may have a processing chamber, a plurality of processing stations in the processing chamber, each processing station has a pedestal configured to support a wafer, each pedestal has a pedestal body having a first side and a second side facing in an opposite direction from the first side, a plurality of vacuum clamping channels located on the first side, the vacuum clamping channels fluidically connected with a vacuum passage extending through the pedestal body, the plurality of vacuum clamping channels is configured for vacuum clamping a wafer to the first side of the pedestal body, and a first channel positioned on the second side of the pedestal body, the first channel is configured to receive a first temperature control element having a coolant passage and that is configured to control a temperature of the pedestal body by actively cooling the pedestal body, a showerhead positioned above a respective pedestal, and a controller having one or more processors and one or more memories

that store instructions for controlling the system, the instructions are configured to cause the one or more processors to cause material to be deposited at the same time on a first wafer positioned on a first pedestal in a first processing station and a second wafer positioned on a second pedestal in a second station, each pedestal to vacuum clamp the respective wafer positioned thereon, coolant to flow in the coolant passage of the first pedestal at a first flow rate during material deposition on the first wafer, and coolant to flow through the coolant passage of the second pedestal at a second flow rate during material deposition on the second wafer.

[0034] In some implementations, the first flow rate may be different than the second flow rate.

[0035] In some implementations, the first flow rate may be the same as the second flow rate, the instructions may be further configured to cause the one or more processors to cause coolant to flow in the coolant passage of the first pedestal at a third flow rate during material deposition of the first wafer, and the third flow rate may be different than the second flow rate.

[0036] In some implementations, the third flow rate may be greater than the second flow rate.

[0037] In some implementations, the third flow rate may be less than the second flow rate.

[0038] In some implementations, the system further has a coolant source fluidically connected to each respective pedestal and configured to flow coolant to each respective pedestal.

[0039] In some implementations, flowing coolant in the coolant passage of the first pedestal at the first flow rate and flowing coolant in the coolant passage of the second pedestal at the second flow rate may reduce nonuniformity of the deposited material between the first wafer and the second wafer.

[0040] In some implementations, a method of semiconductor processing may be provided. The method may have providing a first wafer to a first pedestal in a first processing station in a processing chamber, heating the first wafer to a first temperature with a second temperature control element in the first pedestal, actively cooling the first pedestal during the heating by flowing a coolant through a coolant passage of the first pedestal, vacuum clamping the first wafer to the first pedestal during the heating and the active cooling, and depositing a material on the first wafer while, at the same time, heating the first wafer to the first temperature, actively cooling the first pedestal, and vacuum clamping the first wafer.

[0041] In some implementations, the actively cooling may comprise flowing the coolant through the coolant passage at a first flow rate, and flowing the coolant through the coolant passage at a second flow rate different than the first flow rate.

[0042] In some implementations, the first flow rate may be less than the second flow rate.

[0043] In some implementations, flowing coolant in the coolant passage at the first flow rate and the second flow rate may reduce nonuniformity of the deposited material on the first wafer.

[0044] In some implementations, the method may further have providing a second wafer to a second pedestal in a second processing station in the processing chamber, heating the second wafer to the first temperature with a third temperature control element in the second pedestal, actively cooling the second pedestal during the heating by flowing a coolant through a coolant passage of the second pedestal, vacuum clamping the second wafer to the second pedestal during the heating and the active cooling, and depositing, while depositing the material on the first wafer, a material on the second wafer while, at the same time, heating the second wafer to the first temperature, actively cooling the second pedestal, and vacuum clamping the second wafer.

[0045] In some implementations, actively cooling the first pedestal may comprise flowing the coolant through the coolant passage of the first pedestal at a first flow rate, and actively cooling the second pedestal may comprise flowing the coolant through the coolant passage of the second pedestal at a second flow rate.

[0046] In some implementations, the first flow rate may be different than the second flow rate.

[0047] In some implementations, the first flow rate may be the same as the second flow rate.

[0048] In some implementations, actively cooling the first pedestal may further comprises adjusting the first flow rate to a third flow rate, and flowing the coolant through the coolant passage of the first pedestal.

[0049] In some implementations, the first flow rate may be less than the second flow rate, and the third flow rate may be greater than the second flow rate.

[0050] In some implementations, the first flow rate may be greater than the second flow rate, and the third flow rate may be less than the second flow rate.

[0051] In some implementations, the first flow rate may be the same as the second flow rate, and the third flow rate is different than the second flow rate.

[0052] In some implementations, flowing the coolant through the coolant passage of the first pedestal at the first flow rate and flowing the coolant through the coolant passage of the second pedestal at the second flow rate may reduce nonuniformity of the deposited material between the first wafer and the second wafer.

[0053] In some implementations, actively cooling the first wafer and the second wafer may reduce nonuniformity of the deposited material between the first wafer and the second wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0054] Reference to the following Figures is made in the discussion below; the Figures are not intended to be limiting in scope and are simply provided to facilitate the discussion below.

[0055] FIG. 1 depicts a schematic of an example semiconductor processing tool in which the pedestals disclosed herein may be used, according to some implementations.

[0056] FIG. 2 depicts an example pedestal assembly with a wafer positioned atop it, according to some implementations.

[0057] FIG. 3 depicts the example pedestal of FIG. 2 with the wafer removed, according to some implementations.

[0058] FIG. 4 depicts an exploded view of the example pedestal of FIG. 2, according to some implementations.

[0059] FIG. 5 depicts a top view of the example pedestal of FIG. 2, according to some implementations.

[0060] FIG. 6 depicts a section view along section line 6-6 in FIG. 5, according to some implementations.

[0061] FIG. 7 depicts a section view along section line 7-7 in FIG. 5, according to some implementations.

[0062] FIG. 8 depicts a section view along section line 8-8 in FIG. 5, according to some implementations.

[0063] FIG. 9 is an isometric view of the insert system of the example pedestal of FIG. 2, according to some implementations.

[0064] FIG. 10 depicts a first technique for wafer processing.

[0065] FIG. 11 depicts a second technique for wafer processing.

[0066] FIG. 12 schematically illustrates a multi-station processing tool according to some implementations.

[0067] The above-described Figures are provided to facilitate understanding of the concepts discussed in this disclosure and are intended to be illustrative of some implementations that fall within the scope of this disclosure but are not intended to be limiting—implementations consistent with this disclosure and which are not depicted in the Figures are still considered to be within the scope of this disclosure.

DETAILED DESCRIPTION

[0068] As discussed above, semiconductor wafer processing operations are often performed on semiconductor wafers while such wafers are supported within a processing chamber on a pedestal or wafer support, e.g., a structure typically designed to support a semiconductor wafer from below in an evenly distributed manner. Process gases are usually flowed through ports on an underside of a showerhead and then distributed across a semiconductor wafer supported on the pedestal via gas distribution ports distributed across an underside of the showerhead, in some instances.

[0069] Disclosed herein are new pedestal designs configured to receive bowed wafers in plasma-enhanced chemical vapor deposition (PECVD) processing tools and other contexts. These pedestal designs may incorporate vacuum clamping features, allowing a bowed wafer to be drawn flat against the pedestal's wafer clamping region.

[0070] In PECVD processes, radio frequency (RF) power may be applied for generating the plasma used to deposit layers onto the wafer. The pedestal may serve as an RF electrode, for instance, as the ground electrode, during the application of RF power. A high frequency (e.g., higher than approximately 13.56 megahertz) and high RF power (e.g., exceeding 1500 watts) may be applied to the RF electrodes in order to generate a plasma within the process chamber, thereby facilitating one or more process operations, e.g., film deposition. In some semiconductor processes, it may be desirable to also actively heat the pedestal, e.g., to ensure that the wafer being processed is kept at a particular temperature that enables certain process operations. However, due to the heat generated by using the pedestal as such an RF electrode and the active heating of such a pedestal, the pedestal may be at a risk of thermal runaway. A pedestal temperature exceeding, e.g., 400°C may, for example, compromise wafer integrity and/or damage components connected with the pedestal, such as seals that maybe used to seal a support column that supports the pedestal to the pedestal. The present inventors determined that an actively heated pedestal that was able to be used as an RF electrode while being able to keep the temperature of the pedestal within an optimal range (e.g., between

200°C to 300°C) under high-frequency and high-power conditions would beneficially enable certain semiconductor manufacturing processes that require plasma generation coupled with active wafer heating via the pedestal.

[0071] To address these needs, the pedestal designs disclosed herein may incorporate active cooling and heating features, allowing the temperature of the pedestal to be controlled during wafer processing operations. Specifically, the active cooling features can be employed to cool the pedestal during use (e.g., to keep the pedestal temperature within the optimal range), thereby enabling its use as an RF electrode, such as the ground electrode, without risking thermal runaway due to the heat generated by the pedestal's role as an RF electrode and the active heating of the pedestal.

[0072] FIG. 1 depicts a schematic of an example semiconductor processing tool 100 in which the pedestals disclosed herein may be used, according to some implementations. The semiconductor processing tool 100 may include a semiconductor processing chamber 110 that includes an interior volume that houses one or more semiconductor processing stations 115. Each semiconductor processing station 115 may include a pedestal 120 that may be used to support a wafer 130 (e.g., a semiconductor wafer or wafer that is to be processed). The wafer 130 may be processed within the semiconductor processing chamber 110 underneath a showerhead assembly 140.

[0073] In some implementations, the showerhead assembly 140 may be configured to distribute gases over the surface of the wafer 130. The showerhead assembly 140 may include an inlet configured to connect to a gas source or gas sources, a stem with an interior gas passage, and a showerhead plenum configured to evenly distribute the gases.

[0074] In some implementations, the semiconductor processing chamber 110 may also include one or more slit valves (not shown), and each slit valve may be configured to allow the semiconductor wafer 130 to be inserted into or withdrawn from the semiconductor processing chamber 110. In some implementations, the slit valves may be located in a wall of the semiconductor processing chamber 110.

[0075] In some implementations of the semiconductor processing tool 100, the pedestal 120 may have an outer diameter of at least a diameter of the wafer 130 (e.g., 300 mm), and the showerhead assembly 140 may have an outer diameter of at least 50% of the pedestal 120 outer diameter.

[0076] In some implementations, the semiconductor processing chamber 110 may further include a rotational indexer shaft and a rotational indexer. The rotational indexer shaft may be configured to rotate the rotational indexer within the semiconductor processing chamber 110, thereby allowing the semiconductor wafer(s) 130 to be transferred from station to station within the semiconductor processing chamber 110.

[0077] FIG. 2 depicts an example pedestal 220 assembly with a wafer 230 positioned atop it (e.g., on a first side 220-1 of the pedestal 220), according to some implementations. The pedestal 220 may correspond to the pedestal 120 in FIG. 1 and the wafer 230 may correspond to the wafer 130 in FIG. 1. FIG. 2 depicts the pedestal 220 in FIG. 2 with the wafer 230 removed, according to some implementations. As shown in FIG. 3, the pedestal 220 is generally round in shape and may support the wafer 230 within a vacuum clamping region 221. The vacuum clamping region 221 may include a plurality of vacuum channels 250, including, for example, multiple concentric vacuum channels 250-1 extending along circular paths, as well as other vacuum channels, such as radial vacuum channels 250-2 and/or parallel vacuum channels 250-3. The vacuum channels 250 may, as can be seen, not extend beyond a circular region 223 that is entirely covered by the wafer 230 when the wafer 230 is placed upon the pedestal 220. For example, as shown in FIG. 2, when the wafer 230 is placed upon the pedestal 220, the circular region 223 may not be visible when viewing along a direction perpendicular to the first side 220-1 of the pedestal 220. In some implementations, the outer perimeter of the wafer 230 may lie within an annular seal region 224. When the wafer 230 is placed on the pedestal 220, the outer perimeter of the wafer 230 is positioned within the annular seal region 224.

[0078] As shown in FIG. 3, when clamping the wafer 230 to the first side 220-1 of the pedestal 220, a vacuum may be drawn on the vacuum channels 250 via one or more vacuum ports 251. For example, the vacuum port(s) 251 may be in fluidic communication with (e.g., fluidically connected with) one or more of the vacuum channels 250 (e.g., through a vacuum passage extending through the body of the pedestal 220) and may act to draw the wafer 230 flat against the vacuum clamping region 221 of the pedestal 220. As can be seen in FIG. 2, in particular, an outer annular region of the wafer 230 may be drawn into close contact with the annular seal region 224, thereby creating a seal that allows the vacuum to be maintained (e.g., vacuum clamping the wafer 230 to the first side 220-1 of the body of the pedestal 220). The pressure differential between the side of the wafer 230 that faces the first side 220-1 of the pedestal 220 and the side of the wafer 230 that faces the showerhead (not shown) may cause the wafer 230 to be pressed flat against the pedestal 220.

[0079] The pedestal 220 may be supported within the processing chamber (e.g., 110 in FIG. 1) using a support column 260, which may, for example, extend through a floor of the processing chamber in some cases. In other cases, the support column 260 may connect with, or be part of, a support arm that then extends horizontally and out through a side wall of the processing chamber.

[0080] The support column 260 may, for example, be hollow and may serve as a conduit for routing multiple different types of components to or from the pedestal 220. For example, in the depicted pedestal 220, the support column 260 houses a vacuum inlet 252 that leads directly upward to the vacuum port 251 (shown in FIG. 3) and which may be used to draw a vacuum on the vacuum channels 250 during vacuum clamping operations.

[0081] The support column 260 may also house a pair of resistive heater cables 270 (e.g., resistive heater cables 270-1 and resistive heater cables 270-2) that may be connected in series (e.g., electrically connected) with a resistive heater element (not shown but discussed in detail below) that may be located within the pedestal 220. The support column 260 may also house a coolant passage inlet 280-1 and a coolant passage outlet 280-2, which may be fluidically connected with a coolant passage loop (not shown but discussed in detail below) located within the pedestal 220. The coolant passage loop is fluidically interposed between the coolant passage inlet 280-1 and the coolant passage outlet 280-2. The coolant passage loop 280 may also be referred to herein as a coolant passage. The coolant passage loop has an inner portion 280-3 and an outer portion 280-4 radially outwards of the inner portion 280-3.

[0082] The support column 260 may also have one or more sensor cables 291 routed through it. The one or more sensor cables 291 may include a temperature sensor cable that leads to a temperature sensor (not shown but discussed in more detail below), which is embedded within the pedestal 220. For example, the pedestal 220 may include a temperature sensor receiving hole (not shown but discussed in detail below) configured to receive the temperature sensor. The temperature sensor may be configured to monitor a temperature of the pedestal 220.

[0083] As can be seen in FIG. 3, in some implementations, the pedestal 220 may further include a plurality of flexure springs 290 configured to control a clamping force applied to the wafer 230 when the wafer 230 needs to be lifted off the pedestal 220. For example, the plurality of flexure springs 290 may include ceramic flexure springs that help lift the wafer 230 to release the seal caused by the vacuum clamping when lifting the wafer 230 off the pedestal 220. The pedestal 220 may additionally have a series of (e.g., three as shown in FIGS. 2 and 3) recessed slots 295 or other locator features configured to center focus ring(s) or carrier ring(s)

(not shown) that may be placed on the pedestal as well and in a location centered on the wafer 230. It is noted that the plurality of flexure springs 290 may be optional and can be omitted in some implementations.

[0084] FIG. 4 depicts an exploded view of the example pedestal of FIGS. 2 and 3 (e.g., the pedestal 220), according to some implementations. As discussed above, to have active control of the pedestal temperature during PECVD processes, the pedestal 220 may include a first temperature control element that is configured to control a temperature of the pedestal 220 by actively cooling the pedestal 220 and a second temperature control element that is configured to control a temperature of the pedestal 220 by actively heating the pedestal 220. Specifically, as can be seen in FIG. 4, the pedestal 220 in this example includes a resistive heater element 271 configured to control a temperature of the pedestal 220 by heating the pedestal 220. The resistive heater element 271 may feature multiple, nested C-shaped segments (e.g., C-shaped segments 271-1) that are joined at their ends by smaller connecting segments such that the C-shaped segments are electrically connected together in series. Also, the pedestal 220 in this example includes a coolant passage loop 280 configured to control a temperature of the pedestal 220 by actively cooling the pedestal 220 (e.g., by circulating a coolant such as clean dry air (CDA) in the coolant passage). In this example, the coolant passage loop 280 features multiple, nested C-shaped segments (e.g., C-shaped segments 280-5) that are joined at their ends by smaller connecting segments such that the C-shaped segments encircles at least 60% of a center region of the pedestal 220. It is understood that the arrangement of C-shaped segments may be feature any suitable symmetrical or non-symmetrical paths.

[0085] The pedestal 220 may, it will be understood, include first and second channels (e.g., discussed in detail below) that are milled into the side of the pedestal (e.g., a second side 220-2) opposite the side thereof that faces the wafer 230 (e.g., the first side 220-1). The first and second channels may each be sized to snugly receive the first or second temperature control element they are receiving, e.g., the resistive heater element 271 or the coolant passage loop 280. The first and second channels may, for example, have bottoms (the surfaces closest to the vacuum clamping region 221) that are semicircular in cross-sectional profile, thereby allowing a circular cross-section resistive heater element 271 or coolant passage loop 280 to be placed into such corresponding channels such that at least 30%, e.g., approximately 50% in some implementations of the exterior of the corresponding temperature control element (e.g., resistive heater element 271 or the coolant passage loop 280) is in close physical conduct with

the pedestal 220, thereby increasing the amount of heat transfer/reducing the thermal resistance between the corresponding temperature control element and the pedestal 220.

[0086] As can be seen in FIG. 4, the pedestal 220 may also include a heater retention insert 272 and a coolant passage retention insert 282. The heater retention insert 272 may, for example, be a wall-like element that follows the same path followed by the resistive heater element 271 within the pedestal 220. For example, the channel configured for receiving the resistive heater element 271 may follow a first path that defines the entire length of the corresponding channel and the heater retention insert 272 may follow the first path for at least 90% of the length of the first path. The channel configured for receiving the coolant passage loop 280 may follow a second path that defines the entire length of the corresponding channel and the coolant passage retention insert 282 may follow the second path for at least 90% of the length of the second path.

[0087] The heater retention insert 272 may, for example, have a width that is generally the same as, or nearly the same as, the width of the channel that receives the resistive heater element 271 (e.g., the first channel of the pedestal 220), thereby allowing the heater retention insert 272 to be inserted into the receiving channel with little or no gap between the heater retention insert 272 and the side walls of the receiving channel. In some instances, the heater retention insert 272 may be interference fit or press fit into the first channel (e.g., the channels that receive the resistive heater element 271) and would thus, compress the resistive heater element 271 into the bottom of the first channel. As discussed in detail below, in some implementations, the heater retention insert 272 may be friction stir-welded along the first path to opposing edges of the first channel.

[0088] In some implementations, the coolant passage retention insert 282 may be similarly configured and may be designed to fit within the channel that is provided in the pedestal 220 to receive the coolant passage loop 280 (e.g., the second channel). The coolant passage retention insert 282 may be sized so as to have little or no gap between the coolant passage retention insert 282 and the channel that receives the coolant passage retention insert 282. In some instances, the coolant passage retention insert 282 may be interference fit or press fit into the second channel (e.g., the channels that receive the coolant passage loop 280) and would thus, compress the coolant passage loop 280 into the bottom of the second channel. As discussed in detail below, in some implementations, the coolant passage retention insert 282 may be friction stir-welded along the second path to opposing edges of the second channel.

[0089] As can be seen, the resistive heater element 271 is positioned closer to the side of the pedestal 220 that supports the semiconductor wafer 230 (e.g., first side 220-1), while the coolant passage loop 280 is positioned further from the side of the pedestal 220 that supports the semiconductor wafer 230. Thus, the resistive heater element 271 is interposed between the vacuum clamping region 221 and the coolant passage loop 280. Positioning the coolant passage loop 280 further from the side of the pedestal 220 that supports the semiconductor wafer 230 than the resistive heater element 271 (e.g., the bottom of the first channel receiving the resistive heater element 271 is closer in distance to the first side 220-1 than the bottom of the second channel receiving the coolant passage loop 280) allows the resistive heater element 271 to be used to heat the pedestal 220, or at least the vacuum clamping region 221 thereof while cooling the underside of the pedestal 220 using the coolant passage loop 280 to reduce the temperature that the support column 260 (and the components housed within it) may experience during wafer processing operations.

[0090] In the depicted example, the coolant passage loop 280 crosses over (or under, depending on one's perspective) the resistive heater element 271 at several locations. Accordingly, the heater retention insert 272 includes several locations where there are notches (shown and discussed in later Figures) in the wall-like structure of the heater retention insert 272. Such notches allow the coolant passage loop 280 to pass through the heater retention insert 272 and may each line up with a corresponding pair of coolant passage loop 280 segments. The coolant passage retention insert 282 may similarly pass through the same notches as the coolant passage loop 280.

[0091] In some implementations, one or both of the coolant passage retention insert 282 and the heater retention insert 272 may feature surfaces that face towards the side of the pedestal 220 that has the vacuum clamping region 221 that have curved, e.g., semicircular, cross-sectional profiles. For example, the coolant passage retention insert 282 may include a concave surface that faces toward the bottom of the second channel (e.g., the channels configured for receiving the coolant passage loop 280), and the heater retention insert 272 may include a concave surface that faces towards the bottom of the first channel (e.g., the channels configured for receiving the resistive heater element 271). Accordingly, when the corresponding temperature control elements are installed (e.g., the resistive heater element 271 being compressed into the corresponding channels by the heater retention insert 272 and the coolant passage loop 280 being compressed into the corresponding channels by the coolant passage retention insert 282) in such an implementation, the coolant passage retention insert

282 comes into physical contact with approximately 50% of the exterior surface area of the coolant passage loop 280, and the heater retention insert 272 comes into physical contact with approximately 50% of the exterior of the resistive heater element 271. The surface configurations of the inserts, channels, and the temperature control elements may further increase the amount of heat transfer that may occur via conduction between the pedestal 220 and temperature control elements (e.g., the resistive heater element 271 and/or the coolant passage loop 280).

[0092] In some implementations, the pedestal 220 may be made of an aluminum alloy and the heater retention insert 272 and the coolant passage retention insert 282 may also be made of an aluminum alloy. In instances where the pedestal 220, the heater retention insert 272, and the coolant passage retention insert 282 are made of metal alloys, a technique such as friction stir welding may be used to weld the seams between the heater retention insert 272 and the pedestal 220 (e.g., the first channel) and then the coolant passage retention insert 282 and the pedestal 220 (e.g., the second channel). For example, as noted above, the heater retention insert 272 may be friction stir-welded to the opposing edges of the first channel along the first path, and the coolant passage retention insert 282 may be friction stir-welded to the opposing edges of the second channel along the second path.

[0093] Friction stir welding may be particularly well-suited for such an application since the process of performing a friction stir weld involves pushing a rotating friction stir welding head or tool against the components to be welded. In this particular instance, this results in the heater retention insert 272 and the coolant passage retention insert 282 both being pushed into the channels in the pedestal 220 (e.g., the first channel and the second channel, respectively) during such a welding process, thereby compressing the resistive heater element 271 and the coolant passage loop 280 into their respective channels and further enhancing the heat transfer across the interface between the pedestal 220 and the resistive heater element 271 and/or the coolant passage loop 280. The use of friction stir welding may also allow the heater retention insert 272 and/or the coolant passage retention insert 282 to be made of metals that are dissimilar to that used for the pedestal 220 if desired.

[0094] FIG. 5 depicts a top view of the example pedestal of FIG. 2, according to some implementations. FIG. 6 depicts a section view along section line 6-6 in FIG. 5, according to some implementations. As can be seen in FIG. 6, the channel that receives the resistive heater element 271 is clearly visible, as is the channel that receives the coolant passage loop 280. The curved or arcuate bottoms of such channels, which are in conformal contact with the resistive

heater element 271 and the coolant passage loop 280, respectively, are clearly visible. The concave curved or arcuate tops of the heater retention insert 272 and the coolant passage retention insert 282 are also clearly visible—as can be seen, there is little or no gap between the resistive heater element 271 and the pedestal 220 or the coolant passage loop 280 and the pedestal 220.

[0095] As can also be seen in FIG. 6, the pedestal 220 may include, for example, a temperature sensor 292 that may be inserted into a hole in the pedestal 220, e.g., near the center of the pedestal 220. As noted, the temperature sensor 292 may be used to monitor the temperature of the pedestal 220. Such temperature data may be used to guide control of the amount of heat that is to be generated by the resistive heater element 271 or the amount of cooling that is to be provided by the coolant passage loop 280.

[0096] FIG. 7 depicts a section view along section line 7-7 in FIG. 5. FIG. 8 depicts a section view along section line 8-8 in FIG. 5. FIG. 9 is an isometric view of the insert system (e.g., including the heater retention insert 272 and the coolant passage retention insert 282) of the example pedestal of FIG. 2. Visible in all FIGS. 7, 8, and 9 are notches 241 that may be included in the heater retention insert 272 in order to allow the coolant passage insert 282 and the coolant passage loop 280 to pass through the heater retention insert 272. For example, as shown in FIGS. 8 and 9, at the notches 241 may be formed in the wall-like structure of the heater retention insert 272. The notches 241 allow the coolant passage loop 280 to pass through the heater retention insert 272 (e.g., at an angle as shown in FIG. 8) and may each line up with a corresponding coolant passage loop 280 segment. The coolant passage retention insert 282 may similarly pass through the notches 241 as the coolant passage loop 280.

[0097] In some implementations, the active cooling may be adjusted in various manners for numerous benefits. For example, the cooling provided by flowing the coolant through the coolant passage may be adjusted by changing the flow rate of the coolant through the coolant passage. Increasing the flow rate of the coolant through the coolant passage may increase the cooling provided, while decreasing the flow rate may decrease the cooling provided. For instance, it was discovered that increasing the flow rate of the coolant affected the material deposition at the edge of the wafer. By controlling, such as by adjusting, the flow rate of the coolant through the coolant passage, the nonuniformity at the edge of the wafer can be reduced, such as reducing or increasing the amount of material deposited at the edge of the wafer to this material has a closer height or profile to the deposited material on the inner portion of the wafer. Under some process conditions, coolant flow rates of about 50 standard

liter per minute (slm) to about 150 slm were found to affect the characteristics, such as shape or thickness, of the material deposited at the edge of the wafer. By using these flow rates, the material deposited at the edge of the wafer may be more uniform with the material deposited on the central portion of the wafer. In some such instances, the heater (e.g., the second control element) may remain at a constant, or substantially constant, level.

[0098] In some implementations, the coolant flow rate may remain at a constant, or substantially constant, level during processing a wafer. As mentioned above, the flow rates may be about 50 slm to about 150 slm and the temperature of the pedestal may range between about 200°C to 300°C, for example. In some other implementations, the coolant flow rate may be adjusted to at least two different flow rates during the processing of the wafer. The various adjustments may be based on the numerous factors, such as the material being deposited and the process being utilized (e.g., PECVD). FIG. 10 depicts a first technique for wafer processing. Here, in block 1001, a wafer 230 may be positioned on the pedestal 220 for processing, such as material deposition. During this processing, the pedestal may be actively cooled by flowing the coolant through the coolant passage loop 280 at a first flow rate for a first time period, as indicated by block 1003. Also during this processing after the first time period, in block 1005, the pedestal may be actively cooled by flowing the coolant through the coolant passage loop 280 at a second flow rate different than the first flow rate for a second time period. In some instances, the first flow rate may be higher than the second flow rate while in other instances, the first flow rate may be lower than the second flow rate. In some instances, the first time period may be the same as the second time period, while in other instances, it may be shorter or longer than the second time period.

[0099] In some implementations, during the processing of blocks 1003 and/or 1005, the pedestal is configured to apply a vacuum through the vacuum clamping channels and vacuum clamp the wafer to the respective pedestal. In some implementations, during the processing of blocks 1003 and/or 1005, the pedestal is configured to actively heat the wafer using the second temperature control element. Accordingly, block 1003 may involve actively cooling the pedestal by flowing the coolant through the coolant passage at the first flow rate, actively heating the wafer on the pedestal, and vacuum clamping the wafer. Similarly, block 1005 may involve actively cooling the pedestal by flowing the coolant through the coolant passage at the second flow rate, actively heating the wafer on the pedestal, and vacuum clamping the wafer.

[0100] In some implementations, the direction of the coolant flow through the coolant passage may be reversed. As provided herein, the coolant may flow through the coolant

passage inlet 280-1 and out the coolant passage outlet 280-2. The coolant initially flows through the outer portion of the coolant flow loop, then to the inner portion of the coolant flow loop, and out the outlet 280-2. This direction of flow through the coolant passage loop causes the outer portion to be cooler than the inner portion due to the heat transfer to the coolant as it traverses through the coolant passage loop. By reversing the coolant flow direction and flowing the coolant into the pedestal through the outlet 280-2, through the inner portion, then the outer portion, and out the inlet 280-1, the inner portion may be cooler than the outer portion. This coolant flow direction may also provide advantageous affects, such as reducing nonuniformity of the deposited material and/or tuning various characteristics of the deposited material, such as material thickness or refractive index.

[0101] In some implementations, the pedestal provided herein is used in multi-station processing chambers. Despite efforts to design and control multi-station chambers to reduce nonuniformity between stations, some such nonuniformity may nevertheless exist and it is desirable to reduce such nonuniformity. For instance, as material is simultaneously deposited on a set of wafers at different stations in the same multi-station chamber, process conditions at one of the stations may not be equal to the other stations, which may be caused by a drifting processing condition, and thereby result in different station-to-station material properties, such as different thicknesses, and result in station-to-station nonuniformity. Controlling and adjusting the flow rate of the coolant through the pedestals in a multi-station processing chamber may provide additional controls that can reduce station-to-station nonuniformity. In another instance, process conditions may tend to drift throughout a batch of substrates (e.g., 200 or 500 substrates) and these drifting conditions may result in nonuniformity or increased nonuniformity of material properties. Controlling and adjusting the flow rate of the coolant through the pedestals in a multi-station processing chamber during the processing of a batch of wafers may again reduce station-to-station nonuniformity.

[0102] Some implementations may therefore utilize techniques that can reduce station-to-station nonuniformity. In some instances, the flow rate of coolant through two pedestals in a multi-station processing chamber may be the same, or substantially the same. As provided above, the flow rate may be about 50 slm to about 150 slm, in some examples. In some other instances, the flow rate of coolant through two pedestals in a multi-station processing chamber may be different which in turn reduces the nonuniformity between these two pedestals. Figure 11 provides another example technique for wafer processing. Here, in block 1101 a first wafer is provided to a first pedestal in a multi-station chamber and a second wafer is provided to a

second pedestal in the same multi-station chamber. The first and second pedestals are the same as provided herein. The material processing may be depositing material onto the wafers, such as with PECVD or CVD. During this processing, coolant is flowed through by the first and second pedestals to actively cool the pedestals.

[0103] In block 1103, the first pedestal is actively cooled by flowing coolant, such as CDA, through the coolant passage loop of the first pedestal at a first flow rate. In block 1105, the second pedestal is actively cooled by flowing coolant, such as CDA, through the coolant passage loop of the second pedestal at a second flow rate. As mentioned above, in some instances, the first and second flow rates may be the same. In some other instances, the first and second flow rates may be different. In some implementations, for all the processing of the first and second wafers, blocks 1103 and 1105 may be performed at the same time, and the first and second flow rates may be different. Using the different flow rates may result in reduced nonuniformity between the first and second wafers.

[0104] In some implementations, during the processing of blocks 1103 and/or 1105, the first and second pedestals are each configured to apply a vacuum through the vacuum clamping channels and vacuum clamp the respective wafer to the respective pedestal. In some implementations, during the processing of blocks 1103 and/or 1105, the first and second pedestals are configured to actively heat the respective wafer using the second temperature control element in the respective pedestal. Accordingly, block 1103 may involve actively cooling the first pedestal by flowing the coolant through the coolant passage at the first flow rate, actively heating the first wafer on the first pedestal, and vacuum clamping the first wafer all at the same time. In other words, material may be deposited on the first wafer at the first station while the first wafer is heated and vacuum clamped to the first pedestal, and while the first pedestal is actively cooled, all at the same time. Similarly, block 1005 may involve actively cooling the second pedestal by flowing the coolant through the coolant passage, actively heating the second wafer on the second pedestal, and vacuum clamping the second wafer to the second pedestal.

[0105] Block 1105 may also involve actively heating the first pedestal and vacuum clamping the first wafer to the first pedestal. In other words, material may be deposited on the second wafer at the second station while the second wafer is heated and vacuum clamped to the second pedestal, and while the second pedestal is actively cooled, all at the same time. Here, blocks 1103 and 1105 may be performed at the same time, or concurrently, such that material may be deposited at the same time on the first wafer and the second wafer while the first

wafer is heated and vacuum clamped to the first pedestal, and while the first pedestal is actively cooled, and while the second wafer is heated and vacuum clamped to the second pedestal, and while the second pedestal is actively cooled.

[0106] In some implementations, the first and second flow rates may be the same for a first portion of processing the first and second wafers, and may be different during another portion of the processing the first and second wafers. For instance, as provided in optional block 1107, the first flow rate may be adjusted to a third flow rate during the processing. The third flow rate may be greater than or less than the first flow rate, and greater than, equal to, or less than the second flow rate. In one example, the first and second flow rates may start the same during the first portion of processing the wafers, which may be the concurrent performance of blocks 1103 and 1105. After the first portion of processing, optional block 1107 may be performed and the first flow rate may be raised or lowered to the third flow rate. In another example, the first and second flow rates may start different than each other during the first portion of processing the wafers, which may be the concurrent performance of blocks 1103 and 1105. After the first portion of processing, optional block 1107 may be performed and the first flow rate may be raised or lowered to the third flow rate. This third flow rate may be less than, greater than, or equal to the second flow rate, depending on the implementation. Adjusting the flow rates as provided herein may result in reduced nonuniformity between the first and second wafers.

[0107] In some implementations, a controller having one or more processors and one or more memories storing instructions configured to cause the one or more processors to control various aspects of a semiconductor processing tool may be provided. The controller, such as controller 1223 described below, is configured to control aspects of the pedestal operation which may include the coolant flow through the pedestal. For instance, the controller is configured to perform any of the techniques provided herein, such as the techniques of Figures 10 and 11.

[0108] Pedestals such as the above may be made of a metal, such as a metal alloy. In some implementations, the pedestal may be made from a single piece of machined metal (although the retention inserts would be formed separately), such as a single piece of aluminum, and may be used to provide an electrode in a processing tool that is configured to generate a plasma above the wafer using the showerhead and the pedestal as opposing electrodes that may be used to generate an electromagnetic field in order to spark and maintain such a plasma. By including the coolant passage(s) within the pedestal, such pedestals are able to not only provide RF power without overheating when used as electrodes but may also be able to

support higher power throughput without overheating when used in such contexts. Such coolant passages are, in fact, sufficiently effective that they allow the use of clean dry air, e.g., from a pressurized source, to be used to cool the pedestal, thereby avoiding the need to resort to more costly and potentially problematic coolants such as perfluorinated coolants (such as Galden heat transfer fluids). Moreover, by having the annular seal region of such pedestals be sized larger in outer diameter than the diameter of the wafer, the underside of the wafer may be minimally exposed to the process gases used during wafer processing operations, thereby reducing the potential for undesirable backside deposition (or etching in the context of an etching tool).

[0109] Such pedestals may also be very economical to produce compared to other pedestals. For example, a pedestal design such as that discussed above may cost less than half of what an electrostatic chuck pedestal might cost.

[0110] Without limitation, example pedestal assemblies according to the present disclosure may be mounted in or part of semiconductor processing tools with a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an ALD chamber or module, an ALE chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0111] FIG. 12 schematically illustrates a multi-station processing tool according to some embodiments.

[0112] In some implementations, multi-station processing tool 1200, which may also be considered a multi-station semiconductor processing system 1200, can include an inbound load lock 1203 and an outbound load lock 1205, either or both of which may include a plasma source and/or an ultraviolet (UV) source. Robot 1237, at atmospheric pressure, is configured to move wafers from a cassette loaded through pod 1209 into inbound load lock 1203 via an atmospheric port 1211. Wafer 1207 is placed by robot 1237 on pedestal 1213 in inbound load lock 1203, atmospheric port 1211 is closed, and inbound load lock 1203 is pumped down. In instances in which inbound load lock 1203 includes a remote plasma source, wafer 1207 may be exposed to a remote plasma treatment in inbound load lock 1203 prior to being introduced into

processing chamber 1215. Further, wafer 1207 may be heated in inbound load lock 1203 to, for example, remove moisture and/or adsorbed gases. Next, chamber transport port 1217 to processing chamber 1215 is opened, and another robot 1219 places wafer 1207 into the reactor on a pedestal of a first station shown in the reactor for processing. While the implementation depicted in FIG. 12 includes load locks, it will be appreciated that, in some implementations, direct entry of wafer 1207 into a processing station may be provided.

[0113] As seen in FIG. 12, processing chamber 1215 includes four process stations, numbered 1 to 4. Each process station may be considered a process module provided above. Each station has a temperature-controlled pedestal (such as temperature-controlled pedestal 1221 of station 1), and gas line inlets, one or more of which may include a corresponding flow adjuster (such as flow adjuster 151) configured to match (or substantially match) flow conditions (e.g., flow conductance, flow velocity, etc.) to the gas line inlets. The pedestal 1221 may be the pedestal provided above and illustrated in Figures 1–9. It will be appreciated that, in some cases, each process station may have different or multiple purposes. For example, in some embodiments, a process station may be switchable between a chemical vapor deposition (CVD) and PECVD process mode. In another example, deposition operations, e.g., PECVD operations, may be performed in one station, while exposure to UV radiation for UV curing may be performed in another station. In some cases, deposition and UV curing may be performed in the same station. Further, although processing chamber 1215 shown as including four stations, embodiments are not limited thereto. For example, processing chamber 1215 may have any suitable number of stations, such as five or more stations, or three or less stations.

[0114] As previously mentioned, multi-station processing tool 1200 may include a wafer handling system (e.g., robot 1219 including spider forks 1201) for transferring and/or positioning wafers within processing chamber 1215. In some embodiments, the wafer handling system may transfer wafers between various process stations and/or between a process station and a load lock. It is contemplated, however, that any suitable wafer handling system may be employed, such as, for example, wafer carousels, other wafer handling robots, etc. Further, multi-station processing tool 1200 may include (or otherwise be coupled to) a system controller 1223 employed to control process conditions and hardware states of multi-station processing tool 1200. System controller 1223 may include one or more memory devices 1225, one or more mass storage devices 1227, and one or more processors 1229. Each processor 1229 may include a central processing unit (CPU) or computer, analog, and/or digital input/output

connections, stepper motor controller boards, etc.

[0115] In some embodiments, system controller 1223 controls each of the activities of multi-station processing tool 1200. For instance, system controller 1223 may execute system control software 1231 stored in mass storage device 1227, loaded into memory device 1225, and executed by processor 1229. Alternatively, control logic may be hard coded in system controller 1223. Application specific integrated circuits (ASIC), programmable logic devices (e.g., field-programmable gate arrays (FPGAs)) and/or the like may be used for these purposes. In the following discussion, wherever "software" or "code" is used, functionally comparable hard coded logic may be used in its place. System control software 1231 may include instructions for controlling the timing, mixture of gases, gas flow rates, flow conductance, chamber and/or station pressure, chamber and/or station temperature, wafer temperature, target power levels, RF power levels, substrate pedestal, chuck and/or susceptor position, and other parameters of a particular process performed by multi-station processing tool 1200. Further, system control software 1231 may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operation of the process tool components used to carry out various process tool processes. System control software 1231 may be coded in any suitable computer readable programming language.

[0116] In some embodiments, system control software 1231 may include input/output control (IOC) sequencing instructions for controlling the various parameters described above. Other computer software and/or programs stored on mass storage device 1227 and/or memory device 1225 associated with system controller 1223 may be employed in some embodiments. Examples of programs or sections of programs for this purpose include a substrate positioning program, a process gas control program, a pressure control program, a heater control program, a cooler control program, and a plasma control program.

[0117] A substrate positioning program may include program code for process tool components that are used to load and orientate wafer 1207 on pedestal 1221 and to control the spacing between wafer 1207 and other parts of multi-station processing tool 1200.

[0118] A process gas control program may include code for controlling gas composition (e.g., silicon-containing gases, oxygen-containing gases, nitrogen-containing gases, dilution (or inert) gases, etc.) flow rates, flow conductances, and optionally for flowing gas into one or more process stations prior to deposition to stabilize the pressure in the process station. A pressure

control program may include code for controlling the pressure in the process station by regulating, for example, a throttle valve in an exhaust system of the process station or the like.

[0119] A heater control program may include code for controlling current to one or more heating units used to heat a pedestal (e.g., pedestal 1221) and/or a showerhead of processing chamber 1215. Additionally or alternatively, the heater control program may control delivery of a heat transfer gas (such as helium) to a gas distributor, and, thereby, to wafer 1207.

[0120] A cooling control program may include code for controlling a flow rate of conductive cooling fluid, e.g., clean dry air or CDA, through a cooling unit used to extract heat from a pedestal (e.g., pedestal 1221) and/or a showerhead of processing chamber 1215, and, thereby, transfer such thermal energy to, for instance, a waste heat capturing, storage, recycling, and/or disposing system. The flow of the cooling fluid through the cooling unit may also extract heat from wafer 1207. The tool, or system, 1200 also has a representational coolant source 1255 which may be a source of clean dry air (CDA) that is fluidically connected to each pedestal in stations 1–4. In some implementations, the coolant source 1255 may be a common source for multiple pedestals. In some such instances, the flow rate of the coolant may be individually controlled for each respective pedestal. This provides for independent coolant flow rate control for each pedestal. The controller 1223 is configured to control the coolant flow, such as the CDA flow, from the coolant source 1255 to each individual pedestal.

[0121] A plasma control program may include code for setting RF power levels applied to the process electrodes in one or more process stations in accordance with various embodiments.

[0122] A pressure control program may include code for maintaining pressure in a reaction chamber in accordance with various embodiments.

[0123] In some embodiments, a user interface may be provided in association with system controller 1223. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices, such as pointing devices, keyboards, touch screens, microphones, etc.

[0124] In some embodiments, parameters adjusted by system controller 1223 may relate to process conditions. Non-limiting examples include process gas composition and flow rates, temperature, pressure, plasma conditions (such as RF bias power levels), pressure, temperature, etc. These parameters may be provided to the user in the form of a recipe, which may be entered utilizing the user interface.

[0125] Signals for monitoring the process may be provided by analog and/or digital input connections of system controller 1223 from various process tool sensors. The signals for controlling the process may be output on analog and/or digital output connections of multi-station process tool 1200. Non-limiting examples of process tool sensors that may be monitored include mass flow controllers, pressure sensors (such as manometers), thermocouples, etc. Appropriately programmed feedback and control algorithms may be used with data from the sensors to maintain process conditions.

[0126] System controller 1223 may provide program instructions for implementing one or more of the above-described processes. The program instructions may control a variety of process parameters, such as direct current (DC) power level, RF bias power level, pressure, temperature, etc. The instructions may control the parameters to operate deposition of film stacks of a stress compensation layer according to various embodiments.

[0127] System controller 1223 will typically include one or more memory devices and one or more processors configured to execute the instructions so that the apparatus will perform a method in accordance with some embodiments. In some instances, machine-readable media containing instructions for controlling process operations in accordance with various embodiments may be coupled to system controller 1223.

[0128] In some embodiments, system controller 1223 may be part of a system, which may be part of at least one of the above-described examples. Such systems may include semiconductor processing equipment, including a processing tool or tools, a chamber or chambers, a platform or platforms for processing, and/or specific processing components (e.g., a wafer pedestal, a gas flow system, a thermal management system, etc.). The systems discussed above may be integrated with electronics for controlling their operation before, during, and/or after processing of a semiconductor wafer or substrate. The electronics may be referred to as the "controller," which may control various components or subparts of the system or systems. For instance, system controller 1223, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), valve operation, flow adjuster operation, light source control for radiative heating, pressure settings, vacuum settings, power settings, RF generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operational settings, wafer transfers into and out of a tool or chamber and other transfer tools and/or load locks

connected to or interfaced with a specific system. In this manner, system controller 1223 may be configured to control, among other systems, the various actuators and motors of a wafer processing system and flow adjusters of a fluid delivery system.

[0129] Broadly speaking, system controller 1223 may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and/or the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to system controller 1223 in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon oxide, surfaces, circuits, dies of a wafer, etc.

[0130] System controller 1223, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, system controller 1223 may be in the "cloud" or all or a part of a fab host computer system, which can allow for remote access of wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g., a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It is to be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as

described above, system controller 1223 may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0131] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an atomic layer deposition (ALD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and/or any other semiconductor processing system that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0132] As noted above, depending on the process step or steps to be performed by the tool, system controller 1223 might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, and/or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0133] The use, if any, of ordinal indicators, e.g., (a), (b), (c)... or (1), (2), (3)... or the like, in this disclosure and claims is to be understood as not conveying any particular order or sequence, except to the extent that such an order or sequence is explicitly indicated. For example, if there are three steps labeled (i), (ii), and (iii), it is to be understood that these steps may be performed in any order (or even concurrently, if not otherwise contraindicated) unless indicated otherwise. For example, if step (ii) involves the handling of an element that is created in step (i), then step (ii) may be viewed as happening at some point after step (i). Similarly, if step (i) involves the handling of an element that is created in step (ii), the reverse is to be understood. It is also to be understood that use of the ordinal indicator "first" herein, e.g., "a first item," should not be read as suggesting, implicitly or inherently, that there is necessarily a "second" instance, e.g., "a second item."

[0134] It is to be understood that the phrases "for each <item> of the one or more <items>," "each <item> of the one or more <items>," or the like, if used herein, are inclusive of both a single-item group and multiple-item groups, i.e., the phrase "for ... each" is used in the sense that it is used in programming languages to refer to each item of whatever population of items is referenced. For example, if the population of items referenced is a single item, then "each" would refer to only that single item (despite the fact that dictionary definitions of "each" frequently define the term to refer to "every one of two or more things") and would not imply that there must be at least two of those items. Similarly, the term "set" or "subset" should not be viewed, in itself, as necessarily encompassing a plurality of items—it will be understood that a set or a subset can encompass only one member or multiple members (unless the context indicates otherwise).

[0135] The term "between," as used herein and when used with a range of values, is to be understood, unless otherwise indicated, as being inclusive of the start and end values of that range. For example, between 1 and 5 is to be understood to be inclusive of the numbers 1, 2, 3, 4, and 5, not just the numbers 2, 3, and 4.

[0136] The term "operatively connected" is to be understood to refer to a state in which two components and/or systems are connected, either directly or indirectly, such that, for example, at least one component or system can control the other. For example, a controller may be described as being operatively connected with a resistive heating unit, which is inclusive of the controller being connected with a sub-controller of the resistive heating unit that is electrically connected with a relay that is configured to controllably connect or disconnect the resistive heating unit with a power source that is capable of providing an amount of power that is able to power the resistive heating unit so as to generate a desired degree of heating. The controller itself likely cannot supply such power directly to the resistive heating unit due to the currents involved, but it will be understood that the controller is nonetheless operatively connected with the resistive heating unit.

[0137] For the purposes of this disclosure, the term "fluidically connected" is used with respect to volumes, plenums, holes, etc., that may be connected with one another, either directly or via one or more intervening components or volumes, in order to form a fluidic connection, similar to how the term "electrically connected" is used with respect to components that are connected together to form an electric connection. In the context of the first and second passage segments discussed in this application, however, it will be understood that when reference is made to such a passage segment fluidically connecting with other

passage segments, such fluidic connections are to be understood to be direct couplings between such passage segments, e.g., the end of such a passage segment is directly connected to the ends of the other passage segments (as opposed to being connected with such other passage segments via one or more other intervening passage segments). The term "fluidically interposed," if used, may be used to refer to a component, volume, plenum, or hole that is fluidically connected with at least two other components, volumes, plenums, or holes such that fluid flowing from one of those other components, volumes, plenums, or holes to the other or another of those components, volumes, plenums, or holes would first flow through the "fluidically interposed" component before reaching that other or another of those components, volumes, plenums, or holes. For example, if a pump is fluidically interposed between a reservoir and an outlet, fluid that flowed from the reservoir to the outlet would first flow through the pump before reaching the outlet. The term "fluidically adjacent," if used, refers to placement of a fluidic element relative to another fluidic element such that there are no potential structures fluidically interposed between the two elements that might potentially interrupt fluid flow between the two fluidic elements. For example, in a flow path having a first valve, a second valve, and a third valve placed sequentially therealong, the first valve would be fluidically adjacent to the second valve, the second valve fluidically adjacent to both the first and third valves, and the third valve fluidically adjacent to the second valve.

[0138] It is understood that the examples and implementations described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art. Although various details have been omitted for clarity's sake, various design alternatives may be implemented. Therefore, the present examples are to be considered as illustrative and not restrictive, and the disclosure is not to be limited to the details given herein but may be modified within the scope of the disclosure.

[0139] It is to be understood that the above disclosure, while focusing on a particular example implementation or implementations, is not limited to only the discussed example, but may also apply to similar variants and mechanisms as well, and such similar variants and mechanisms are also considered to be within the scope of this disclosure.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a pedestal body having a first side and a second side facing in an opposite direction from the first side;

a plurality of vacuum clamping channels located on the first side, the vacuum clamping channels fluidically connected with a vacuum passage extending through the pedestal body, wherein the plurality of vacuum clamping channels is configured for vacuum clamping a wafer to the first side of the pedestal body; and

a first channel positioned on the second side of the pedestal body, wherein the first channel is configured to receive a first temperature control element that is configured to control a temperature of the pedestal body by actively cooling the pedestal body.

2. The apparatus of claim 1, further comprising the first temperature control element, wherein the first channel has a cross-sectional profile that includes a semicircular segment that contacts at least 50% of an exterior of the first temperature control element.

3. The apparatus of claim 2, further comprising a second channel positioned on the second side of the pedestal body, wherein the second channel is configured to receive a second temperature control element that is configured to control a temperature of the pedestal body by heating the pedestal body.

4. The apparatus of claim 3, wherein a bottom of the first channel is closer in distance to the second side than a bottom of the second channel.

5. The apparatus of claim 3, further comprising:

a first insert corresponding to the first channel and configured to compress the first temperature control element into the first channel; and

a second insert corresponding to the second channel and configured to compress the second temperature control element into the second channel.

6. The apparatus of claim 5, wherein the first insert includes a concave surface that faces towards a bottom of the first channel, and wherein the second insert includes a concave surface that faces towards a bottom of the second channel.

7. The apparatus of claim 5, wherein

the first channel follows a first path,

the first insert follows the first path for at least 90% of a length of the first path, and

the first insert is friction stir-welded along the first path to opposing edges of the first channel.

8. The apparatus of claim 7, wherein the first path encircles at least 60% of a circumference of the pedestal body.

9. The apparatus of claim 5, wherein

the second channel follows a second path,

the second insert follows the second path for at least 90% of a length of the second path, and

the second insert is friction stir-welded along the second path to opposing edges of the second channel.

10. The apparatus of claim 9, wherein the second path comprises a C-shaped segment.

11. The apparatus of claim 3, wherein the pedestal body is connected with a support column that houses:

a vacuum port fluidically connected with the plurality of vacuum clamping channels;

a coolant passage inlet and a coolant passage outlet that are both fluidically connected with the first temperature control element such that a coolant passage of the first temperature control element is fluidically interposed between the coolant passage inlet and the coolant passage outlet; and

resistive heater cables electrically connected with the second temperature control element.

12. The apparatus of claim 11, wherein:

the coolant passage has an inner portion and an outer portion radially outwards from the inner portion,

the inner portion is fluidically interposed between the outer portion and the coolant passage outlet, and

the outer portion is fluidically interposed between the inner portion and the coolant passage inlet.

13. The apparatus of claim 11, wherein:

the coolant passage has an inner portion and an outer portion radially outwards from the inner portion,

the inner portion is fluidically interposed between the outer portion and the coolant passage inlet, and

the outer portion is fluidically interposed between the inner portion and the coolant passage outlet.

14. The apparatus of claim 1, further comprising:

a temperature sensor receiving hole configured to receive a temperature sensor that is configured to monitor a temperature of the pedestal body.

15. The apparatus of claim 1, wherein the plurality of vacuum clamping channels comprises concentric vacuum channels, radial vacuum channels, parallel vacuum channels, or any combination thereof.

16. The apparatus of claim 1, wherein when viewing along a direction perpendicular to the first side of the pedestal body, the vacuum clamping channels are positioned entirely within a circular region encircled by an annular seal region, wherein the circular region is smaller than 300mm in diameter.

17. The apparatus of claim 1, further comprising a plurality of flexure springs configured to control a clamping force applied to the wafer.

18. The apparatus of claim 17, wherein each flexure spring in the plurality of flexure springs comprises a ceramic flexure spring.

19. The apparatus of claim 1, wherein the pedestal body is made of a metal or a metal alloy.

20. The apparatus of claim 19, wherein the pedestal body is made of aluminum.

21. The apparatus of claim 1, wherein pedestal body is made of a single piece of metal.

22. The apparatus of claim 1, wherein:

the first temperature control element comprises a coolant passage configured to flow a coolant therein, and

the coolant is clear dry air.

23. The apparatus of claim 22, wherein the coolant is flowed through the coolant passage at a flow rate of about 50 slm to about 150 slm.

24. The apparatus of claim 22, further comprising a controller having one or more processors and one or more memories that store instructions that are configured to cause the one or more processors to cause:

material to be deposited on a wafer on the pedestal body,

coolant to flow through the coolant passage at a first flow rate for a first time period during material deposition on the wafer, and

coolant to flow through the coolant passage at a second flow rate for a second time period during material deposition on the wafer.

25. The apparatus of claim 24, wherein the first flow rate is different than the second flow rate.

26. The apparatus of claim 24, wherein the first time period is the same as the second time period.

27. The apparatus of claim 24, wherein the first time period is different than the second time period.

28. The apparatus of any one of claims 1 through 27, further comprising:
a showerhead for distributing gases over a surface of a wafer; and
a processing chamber, wherein the pedestal body is positioned within the processing chamber and beneath the showerhead.

29. A multi-station semiconductor processing system, comprising:
a processing chamber;
a plurality of processing stations in the processing chamber, wherein each processing station has:
a pedestal configured to support a wafer, wherein each pedestal has:
a pedestal body having a first side and a second side facing in an opposite direction from the first side,
a plurality of vacuum clamping channels located on the first side, the vacuum clamping channels fluidically connected with a vacuum passage extending through the pedestal body, wherein the plurality of vacuum clamping channels is configured for vacuum clamping a wafer to the first side of the pedestal body, and
a first channel positioned on the second side of the pedestal body, wherein the first channel is configured to receive a first temperature control element having a coolant passage and that is configured to control a temperature of the pedestal body by actively cooling the pedestal body;
a showerhead positioned above a respective pedestal; and
a controller having one or more processors and one or more memories that store instructions for controlling the system, the instructions are configured to cause the one or more processors to cause:
material to be deposited at the same time on a first wafer positioned on a first pedestal in a first processing station and a second wafer positioned on a second pedestal in a second station,
each pedestal to vacuum clamp the respective wafer positioned thereon,
coolant to flow in the coolant passage of the first pedestal at a first flow rate during material deposition on the first wafer, and
coolant to flow through the coolant passage of the second pedestal at a second flow rate during material deposition on the second wafer.

30. The system of claim 29, wherein the first flow rate is different than the second flow rate.

31. The system of claim 29, wherein:

the first flow rate is the same as the second flow rate,

the instructions are further configured to cause the one or more processors to cause coolant to flow in the coolant passage of the first pedestal at a third flow rate during material deposition of the first wafer, and

the third flow rate is different than the second flow rate.

32. The system of claim 31, wherein the third flow rate is greater than the second flow rate.

33. The system of claim 31, wherein the third flow rate is less than the second flow rate.

34. The system of claim 31, further comprising a coolant source fluidically connected to each respective pedestal and configured to flow coolant to each respective pedestal.

35. The system of claim 31, wherein flowing coolant in the coolant passage of the first pedestal at the first flow rate and flowing coolant in the coolant passage of the second pedestal at the second flow rate reduces nonuniformity of the deposited material between the first wafer and the second wafer.

36. A method of semiconductor processing, the method comprising:

providing a first wafer to a first pedestal in a first processing station in a processing chamber;

heating the first wafer to a first temperature with a second temperature control element in the first pedestal;

actively cooling the first pedestal during the heating by flowing a coolant through a coolant passage of the first pedestal;

vacuum clamping the first wafer to the first pedestal during the heating and the active cooling; and

depositing a material on the first wafer while, at the same time, heating the first wafer to the first temperature, actively cooling the first pedestal, and vacuum clamping the first wafer.

37. The method of claim 36, wherein the actively cooling comprises:

flowing the coolant through the coolant passage at a first flow rate, and

flowing the coolant through the coolant passage at a second flow rate different than the first flow rate.

38. The method of claim 37, wherein the first flow rate is less than the second flow rate.

39. The method of claim 37, wherein flowing coolant in the coolant passage at the first flow rate and the second flow rate reduces nonuniformity of the deposited material on the first wafer.

40. The method of claim 36, further comprising:

providing a second wafer to a second pedestal in a second processing station in the processing chamber;

heating the second wafer to the first temperature with a third temperature control element in the second pedestal;

actively cooling the second pedestal during the heating by flowing a coolant through a coolant passage of the second pedestal;

vacuum clamping the second wafer to the second pedestal during the heating and the active cooling; and

depositing, while depositing the material on the first wafer, a material on the second wafer while, at the same time, heating the second wafer to the first temperature, actively cooling the second pedestal, and vacuum clamping the second wafer.

41. The method of claim 40, wherein:

actively cooling the first pedestal comprises flowing the coolant through the coolant passage of the first pedestal at a first flow rate, and

actively cooling the second pedestal comprises flowing the coolant through the coolant passage of the second pedestal at a second flow rate.

42. The method of claim 41, wherein the first flow rate is different than the second flow rate.

43. The method of claim 41, wherein the first flow rate is the same as the second flow rate.

44. The method of claim 41, wherein actively cooling the first pedestal further comprises:

adjusting the first flow rate to a third flow rate, and

flowing the coolant through the coolant passage of the first pedestal.

45. The method of claim 44, wherein:

the first flow rate is less than the second flow rate, and

the third flow rate is greater than the second flow rate.

46. The method of claim 44, wherein:

the first flow rate is greater than the second flow rate, and

the third flow rate is less than the second flow rate.

47. The method of claim 44, wherein:

the first flow rate is the same as the second flow rate, and

the third flow rate is different than the second flow rate.

48. The method of claim 41, wherein flowing the coolant through the coolant passage of the first pedestal at the first flow rate and flowing the coolant through the coolant passage of the second pedestal at the second flow rate reduces nonuniformity of the deposited material between the first wafer and the second wafer.

49. The method of claim 40, wherein actively cooling the first wafer and the second wafer reduces nonuniformity of the deposited material between the first wafer and the second wafer.

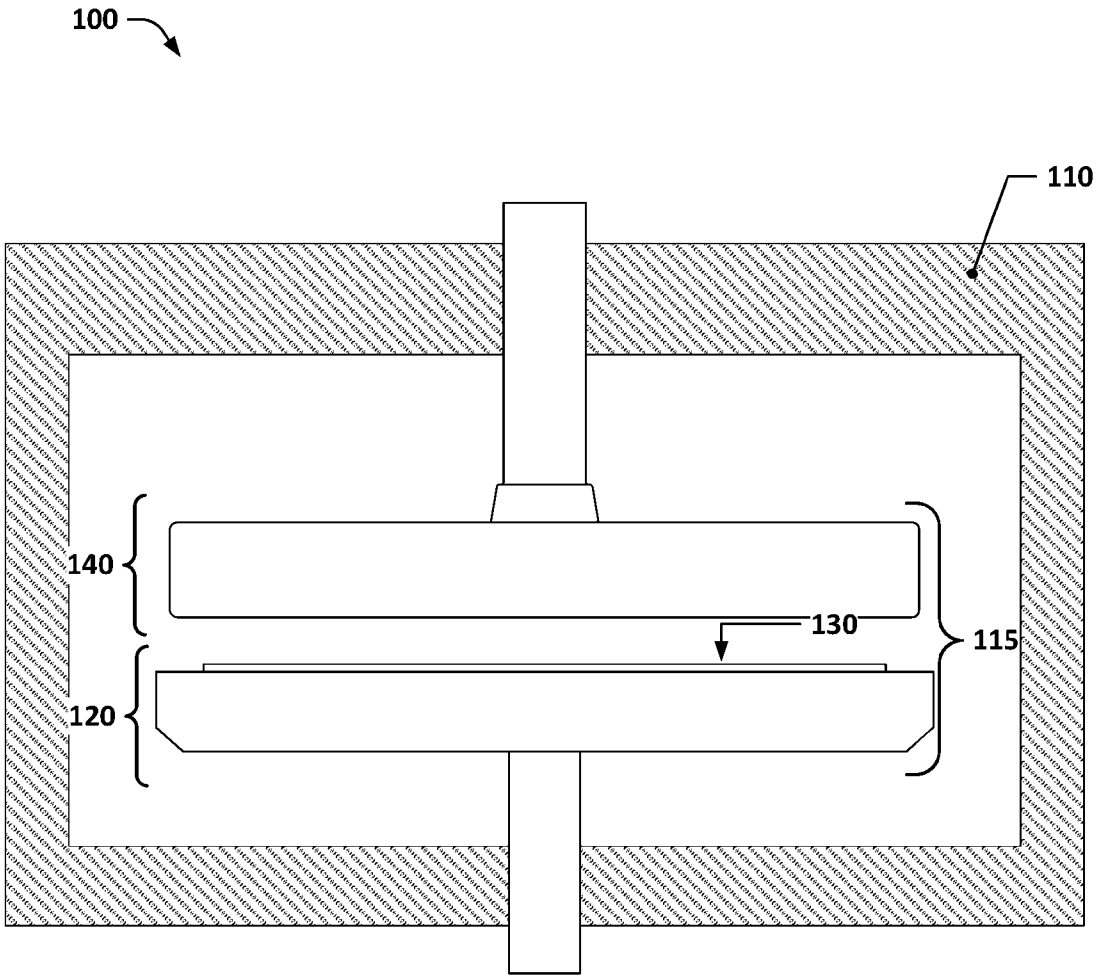

FIG. 1

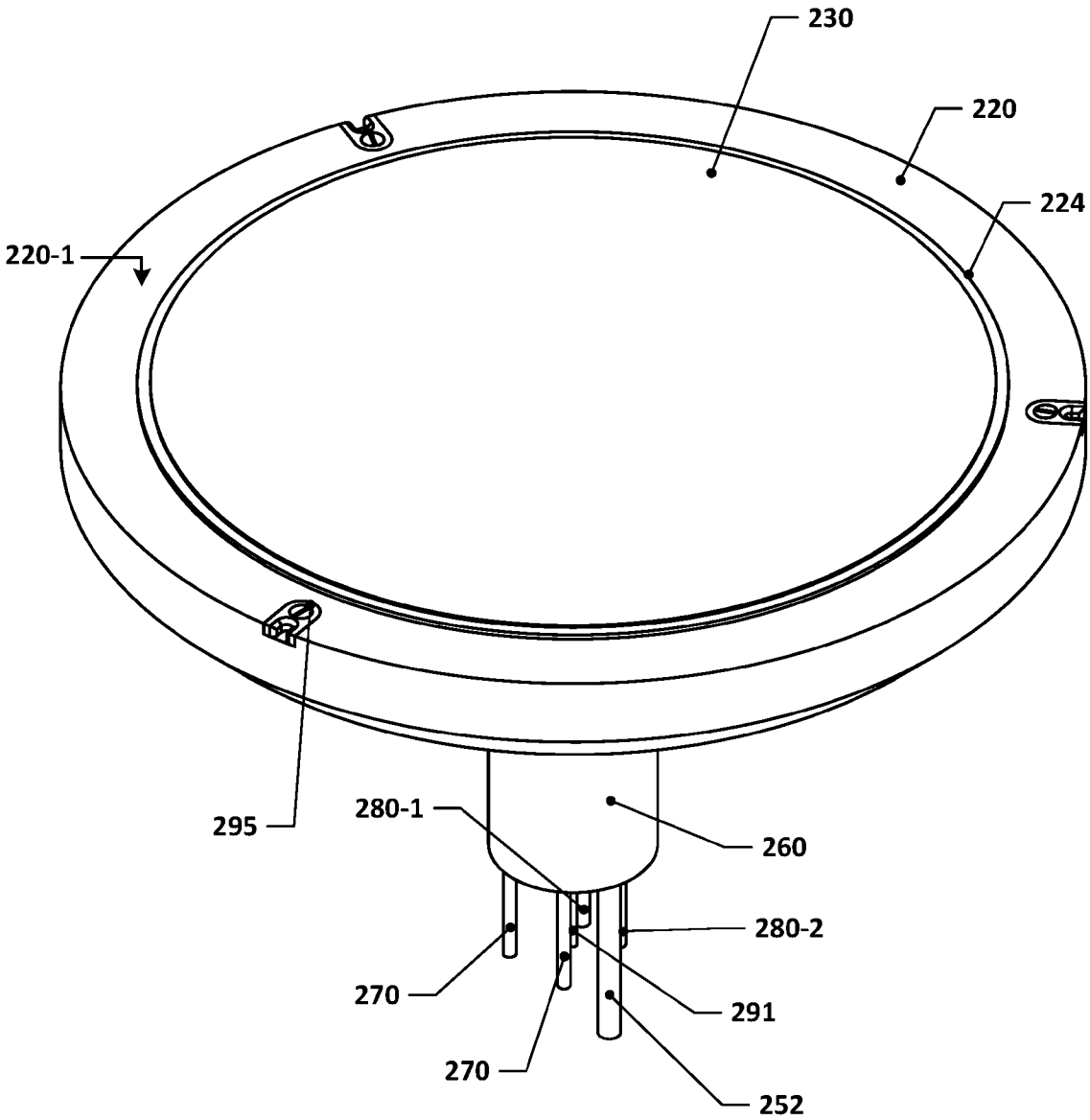

FIG. 2

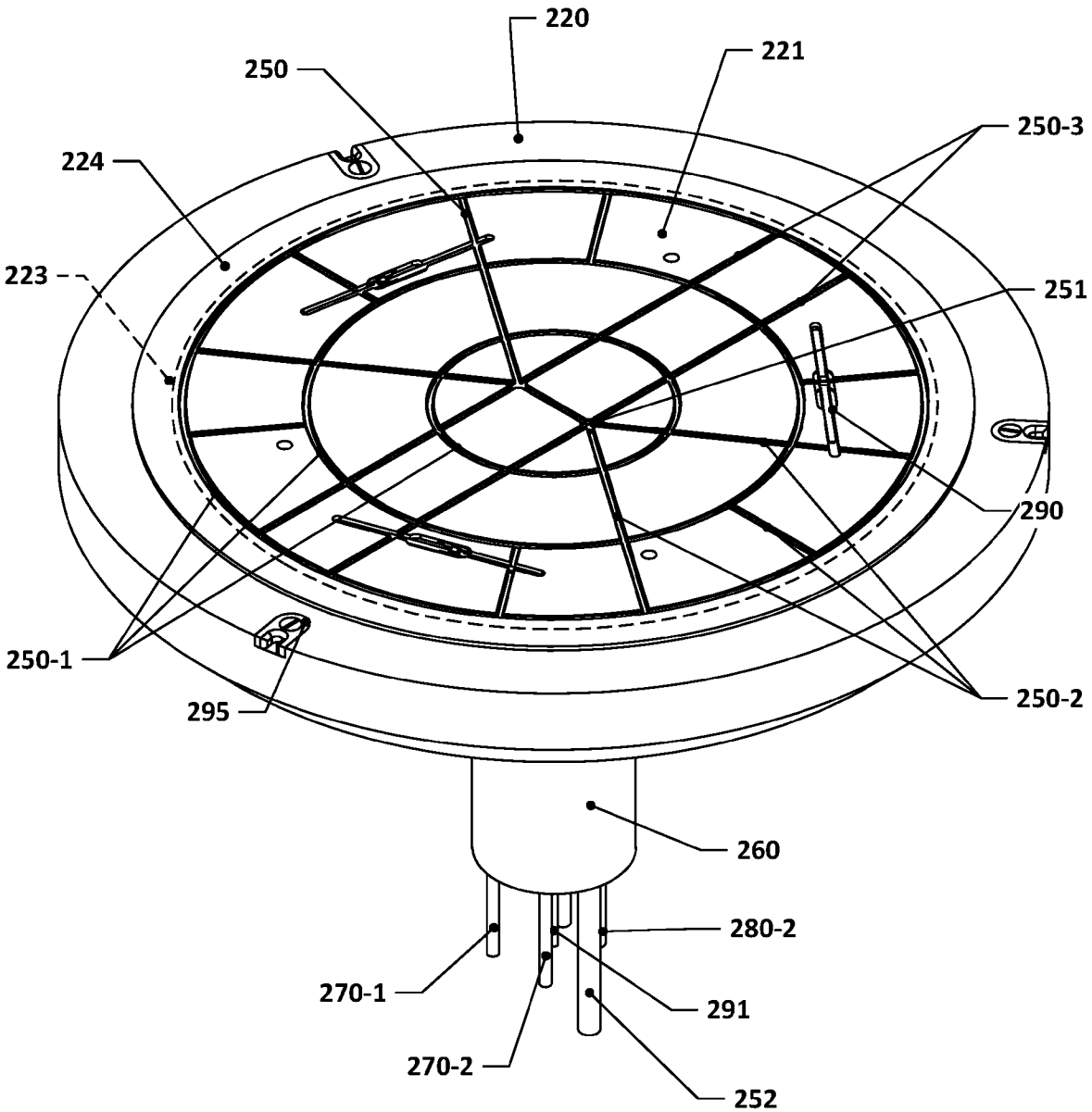
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FIG. 3

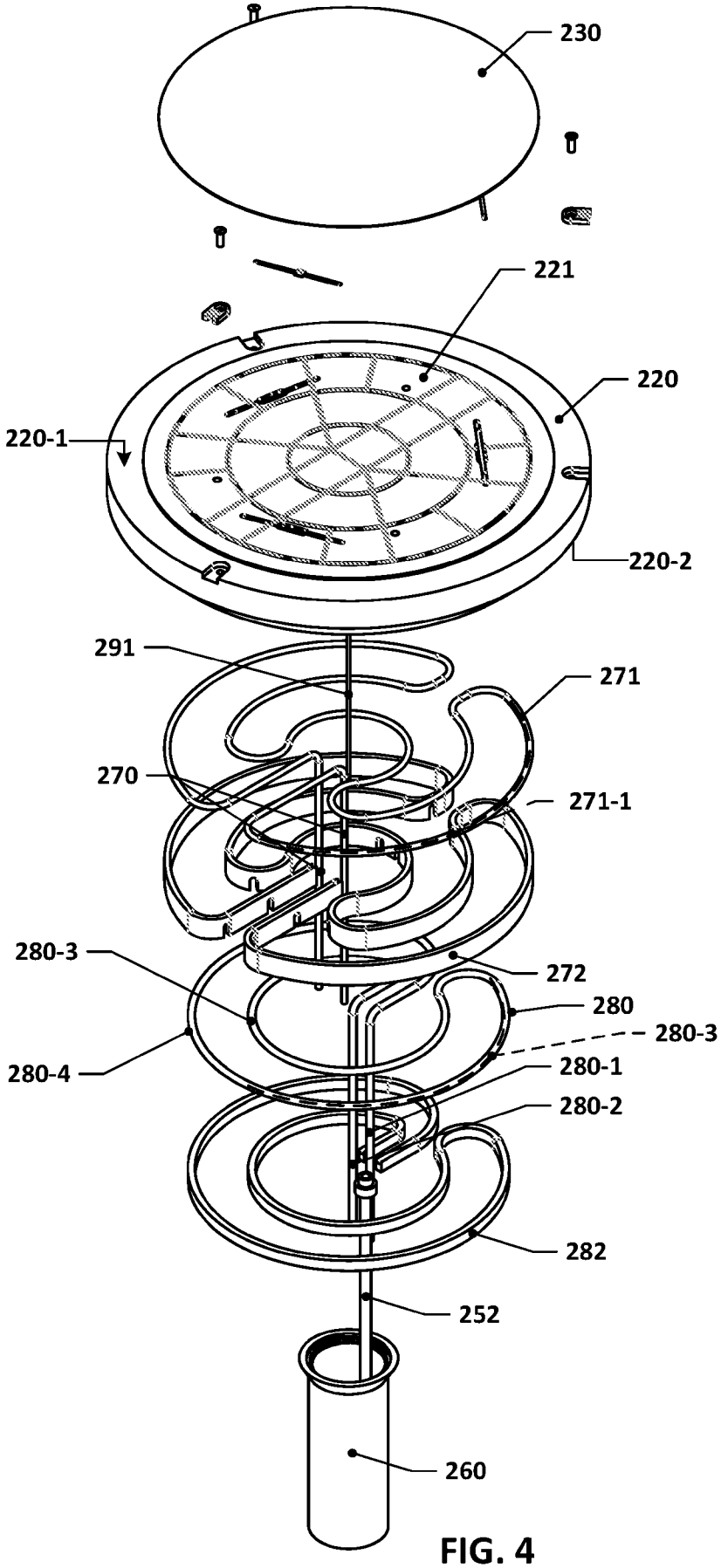
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FIG. 4

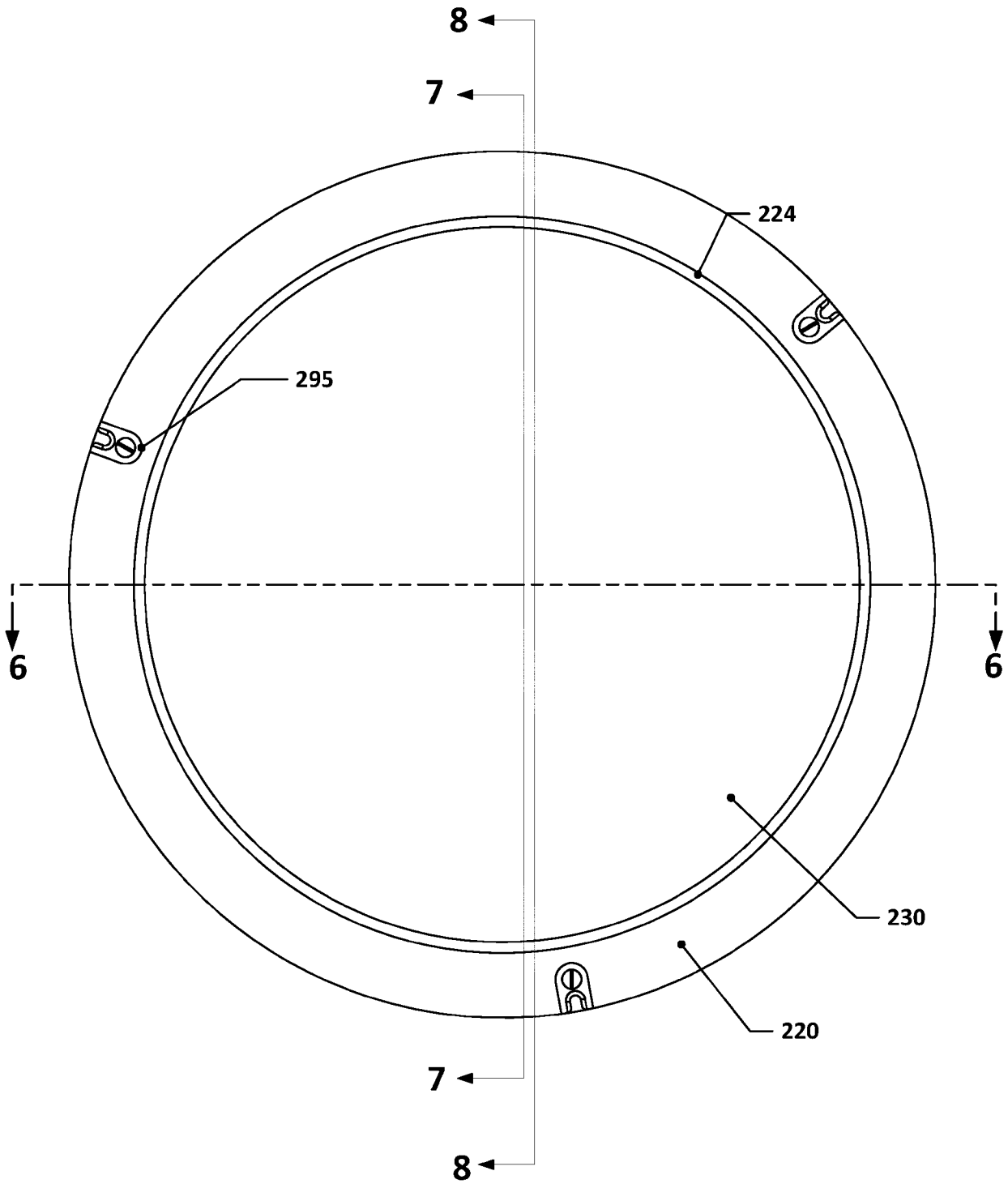

FIG. 5

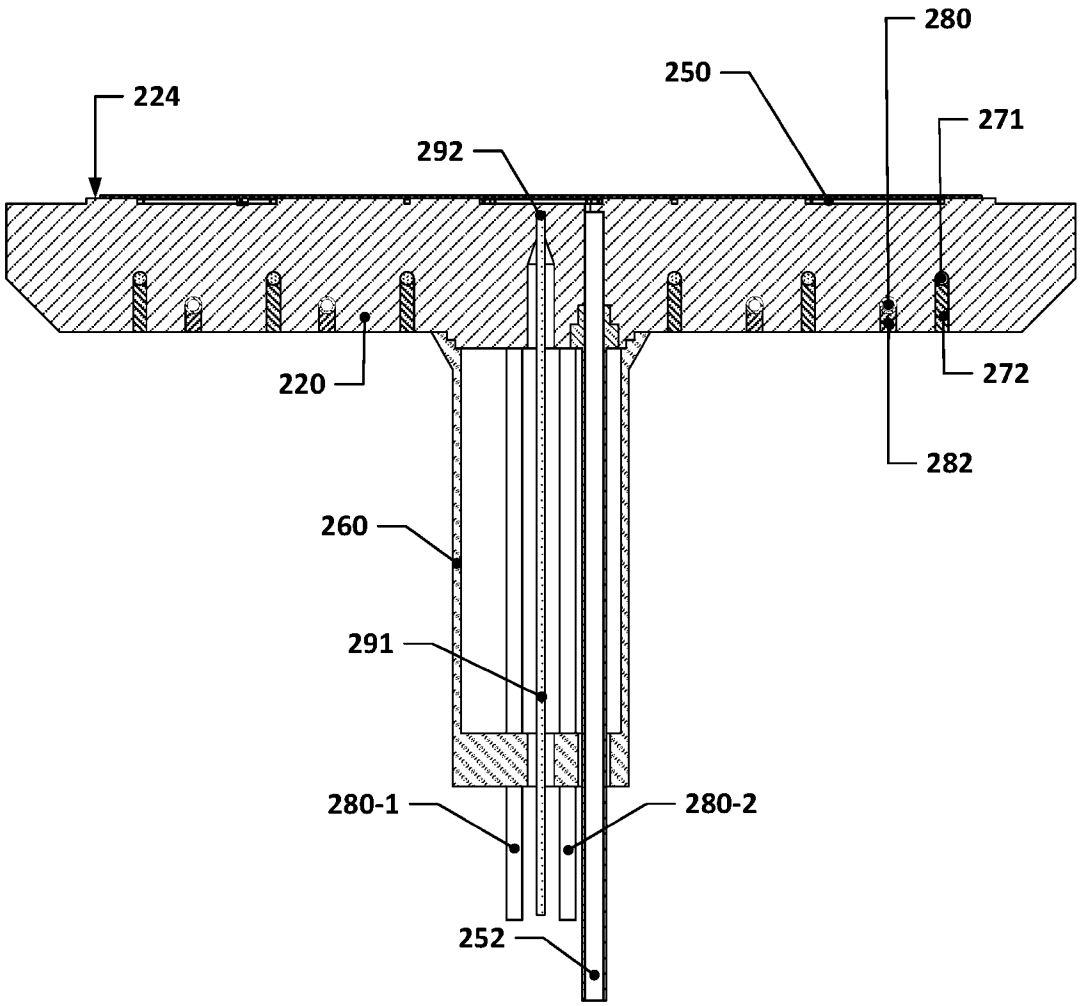

FIG. 6

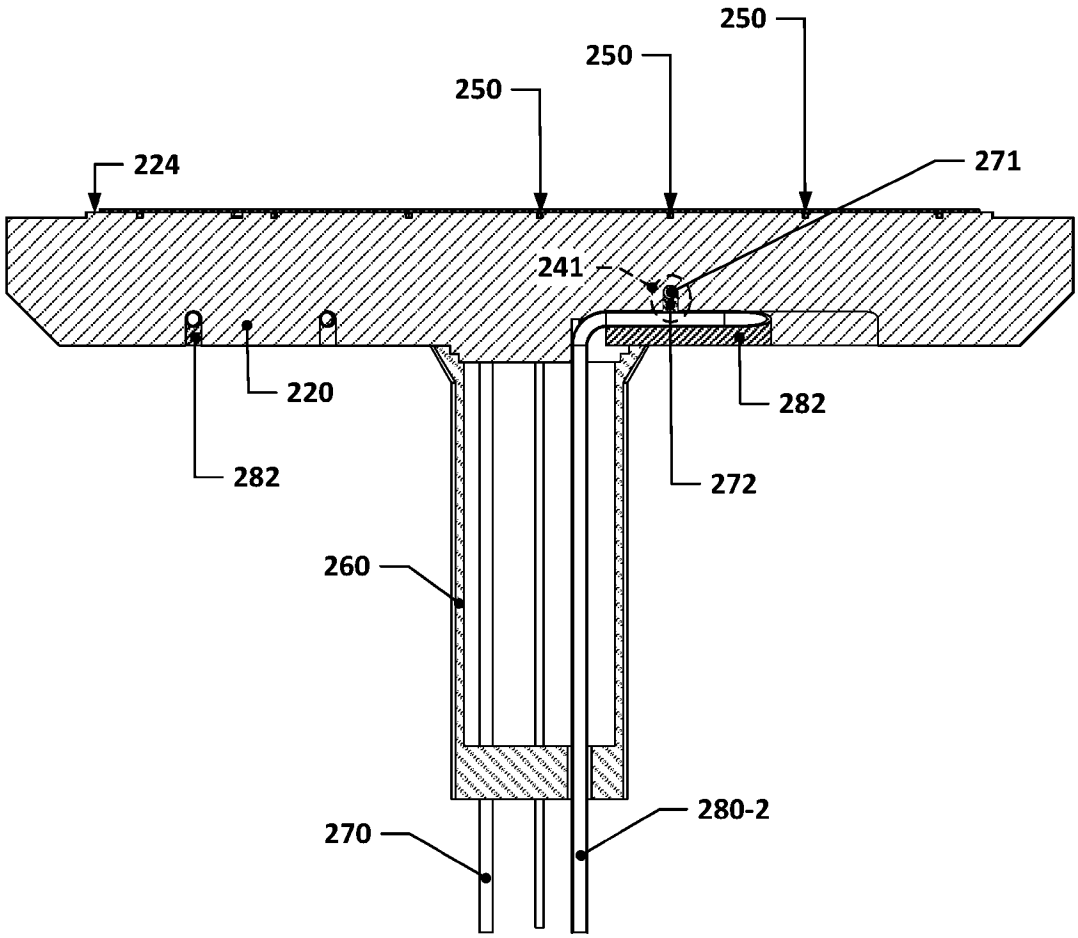

FIG. 7

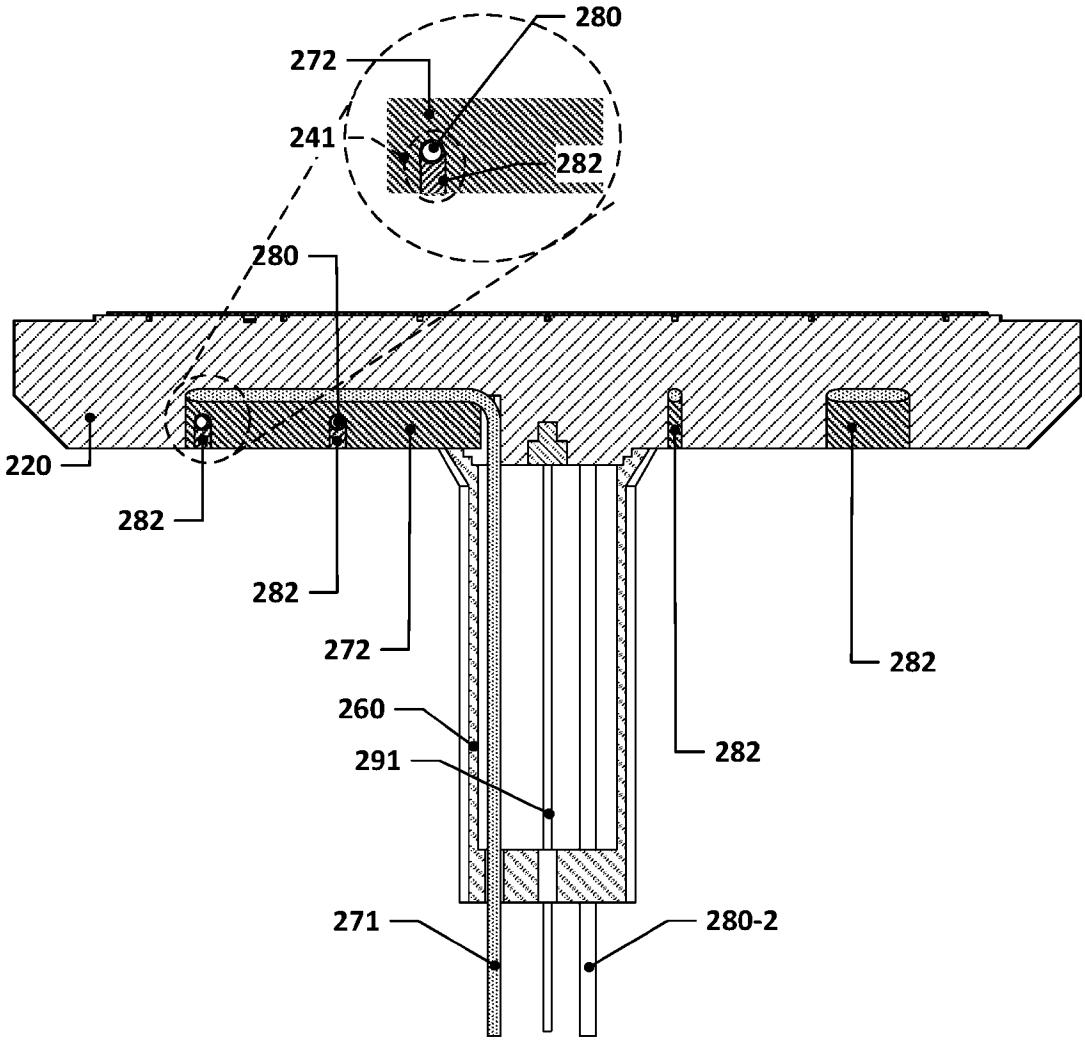

FIG. 8

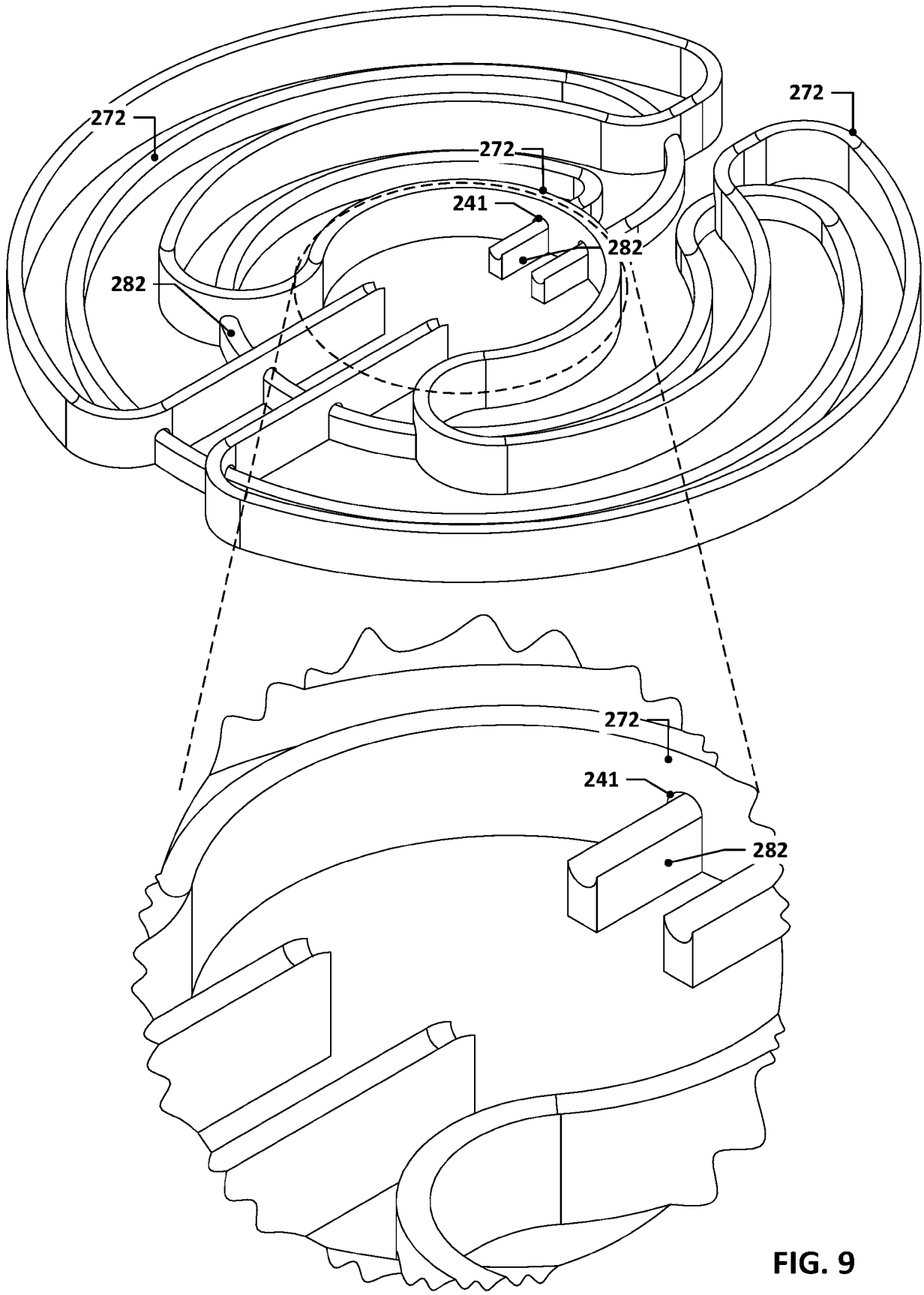

FIG. 9

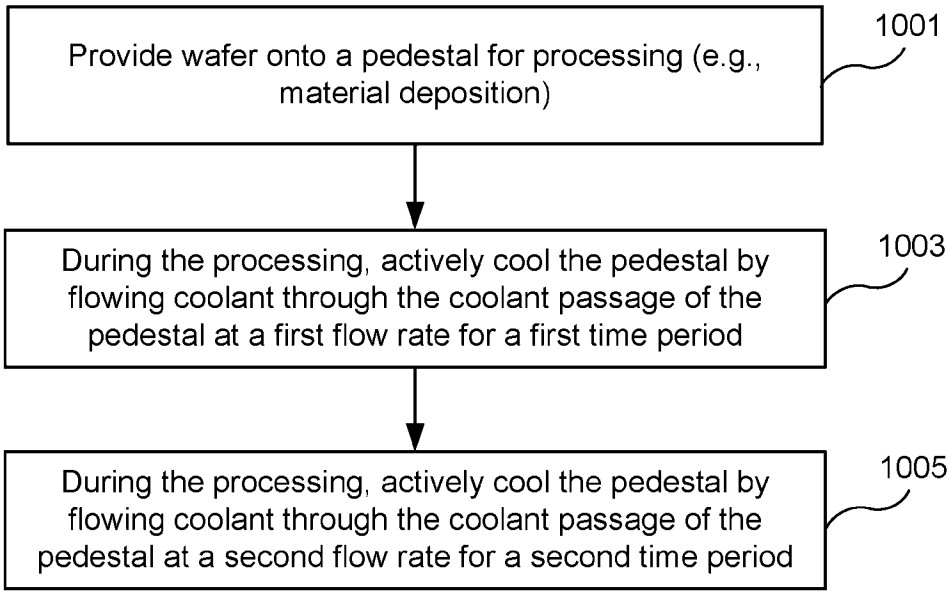
Provide wafer onto a pedestal for processing (e.g., material deposition)
1001
During the processing, actively cool the pedestal by flowing coolant through the coolant passage of the pedestal at a first flow rate for a first time period
1003
During the processing, actively cool the pedestal by flowing coolant through the coolant passage of the pedestal at a second flow rate for a second time period
1005

FIG. 10

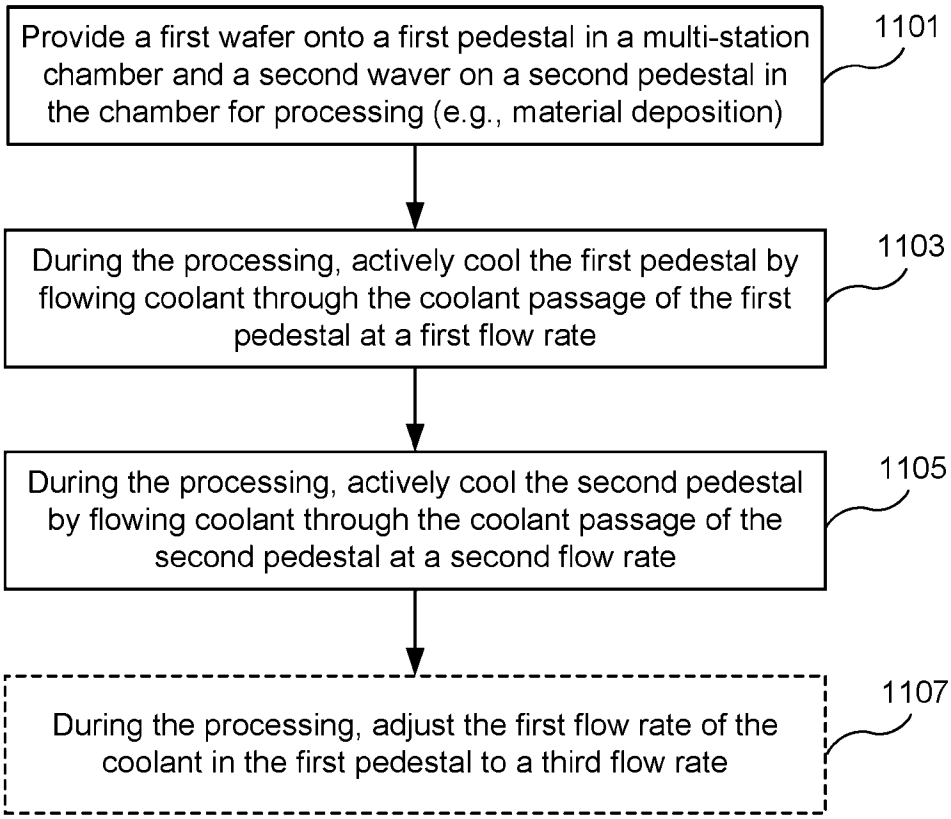
Provide a first wafer onto a first pedestal in a multi-station chamber and a second waver on a second pedestal in the chamber for processing (e.g., material deposition)
1101
During the processing, actively cool the first pedestal by flowing coolant through the coolant passage of the first pedestal at a first flow rate
1103
During the processing, actively cool the second pedestal by flowing coolant through the coolant passage of the second pedestal at a second flow rate
1105
During the processing, adjust the first flow rate of the coolant in the first pedestal to a third flow rate
1107

FIG. 11

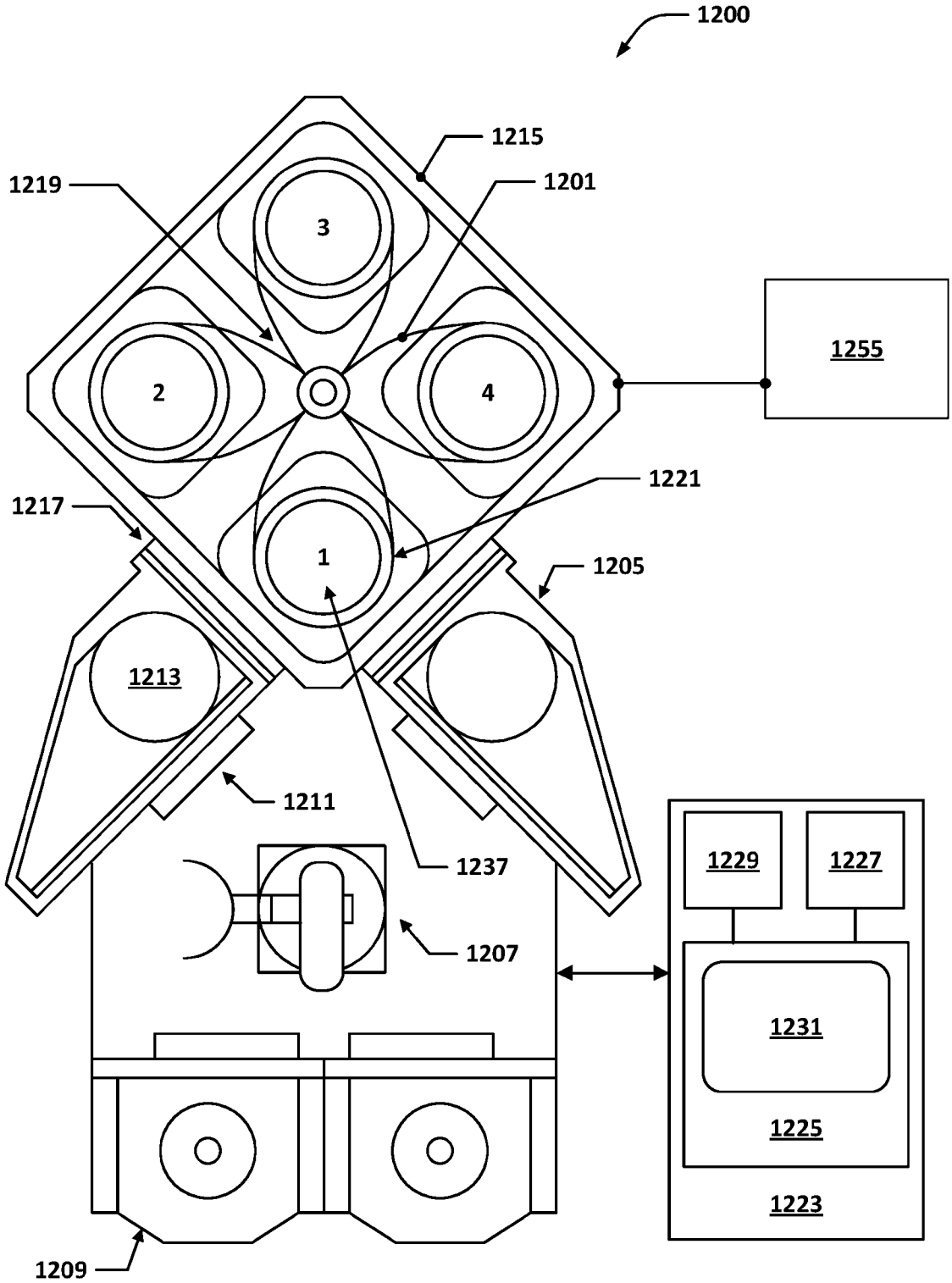
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FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2024/053641

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/683(2006.01)i; **H01L 21/67**(2006.01)i; **H01L 21/687**(2006.01)i; **C23C 16/458**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/683(2006.01); B23B 31/30(2006.01); B25B 11/00(2006.01); H01L 21/67(2006.01); H01L 21/687(2006.01); H02N 13/00(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: pedestal, vacuum, clamping, channel, passage, temperature, cooling

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2017-0221734 A1 (WATLOW ELECTRIC MANUFACTURING COMPANY) 03 August 2017 (2017-08-03) paragraphs [0002]-[0008], [0024]-[0031] and figures 1-5	1-4,14-23,28
A		5-13,24-27,29-49
Y	US 6605955 B1 (SIMON COSTELLO et al.) 12 August 2003 (2003-08-12) column 3, line 49 - column 17, line 4 and claim 1	1-4,14-23,28
Y	US 2009-0179365 A1 (ALEXANDER N. LERNER et al.) 16 July 2009 (2009-07-16) paragraph [0035]	16-18
A	US 2016-0148828 A1 (VARIAN SEMICONDUCTOR EQUIPMENT ASSOCIATES, INC.) 26 May 2016 (2016-05-26) claims 1-23 and figure 1	1-49

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 February 2025	**11 February 2025**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office **189 Cheongsa-ro, Seo-gu, Daejeon** **35208, Republic of Korea**	**LEE, Kang Ha**
Facsimile No. **+82-42-481-8578**	Telephone No. **+82-42-481-5687**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2024/053641

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2017-0256431 A1 (APPLIED MATERIALS, INC.) 07 September 2017 (2017-09-07) claims 1-20 and figure 1	1-49

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2024/053641

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2017-0221734 A1	03 August 2017	CA 2878338 A1	09 January 2014
		CA 2878338 C	24 October 2017
		CA 2902220 A1	04 September 2014
		CA 2902220 C	06 November 2018
		CN 104488074 A	01 April 2015
		CN 104488074 B	11 July 2017
		CN 105009686 A	28 October 2015
		CN 105009686 B	05 May 2020
		EP 2870622 A1	13 May 2015
		EP 2870622 B1	27 February 2019
		EP 2962524 A2	06 January 2016
		EP 2962524 B1	25 December 2019
		EP 3327758 A1	30 May 2018
		JP 2015-523732 A	13 August 2015
		JP 2016-508676 A	22 March 2016
		JP 6127137 B2	10 May 2017
		JP 6322656 B2	09 May 2018
		KR 10-1812510 B1	30 January 2018
		KR 10-2015-0036331 A	07 April 2015
		KR 10-2015-0122699 A	02 November 2015
		KR 10-2213060 B1	05 February 2021
		MX 2015000004 A	14 August 2015
		MX 2015011285 A	03 February 2016
		MX 341488 B	23 August 2016
		MX 350960 B	27 September 2017
		US 10395953 B2	27 August 2019
		US 10658206 B2	19 May 2020
		US 2014-0007416 A1	09 January 2014
		US 2014-0011153 A1	09 January 2014
		US 2015-0351158 A1	03 December 2015
		US 2016-0035602 A1	04 February 2016
		US 9224626 B2	29 December 2015
		US 9673077 B2	06 June 2017
		WO 2014-008241 A1	09 January 2014
		WO 2014-134507 A2	04 September 2014
		WO 2014-134507 A3	23 October 2014
US 6605955 B1	12 August 2003	AU 2743300 A	31 January 2001
		US 2002-0017916 A1	14 February 2002
		US 6583638 B2	24 June 2003
		WO 01-01460 A2	04 January 2001
		WO 01-01460 A3	03 May 2001
		WO 01-01460 A9	06 September 2002
US 2009-0179365 A1	16 July 2009	EP 2235748 A2	06 October 2010
		EP 2235748 B1	06 September 2017
		JP 2011-510488 A	31 March 2011
		JP 5481390 B2	23 April 2014
		TW 200940246 A	01 October 2009
		TW I454336 B	01 October 2014
		US 2012-0205878 A1	16 August 2012
		US 8198567 B2	12 June 2012

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2024/053641

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
		US 8698048 B2	15 April 2014
		WO 2009-091640 A2	23 July 2009
		WO 2009-091640 A3	08 October 2009
US 2016-0148828 A1	26 May 2016	US 9666467 B2	30 May 2017
US 2017-0256431 A1	07 September 2017	CN 108701642 A	23 October 2018
		CN 108701642 B	14 July 2023
		CN 116741696 A	12 September 2023
		JP 2019-508898 A	28 March 2019
		JP 2022-043180 A	15 March 2022
		JP 7026052 B2	25 February 2022
		JP 7232892 B2	03 March 2023
		KR 10-2018-0113221 A	15 October 2018
		KR 10-2023-0124097 A	24 August 2023
		KR 10-2567808 B1	16 August 2023
		TW 201803005 A	16 January 2018
		TW 202114041 A	01 April 2021
		TW I705520 B	21 September 2020
		TW I755817 B	21 February 2022
		US 10249526 B2	02 April 2019
		US 11527429 B2	13 December 2022
		US 2019-0189492 A1	20 June 2019
		WO 2017-151238 A1	08 September 2017