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**Declaration under Rule 4.17:**

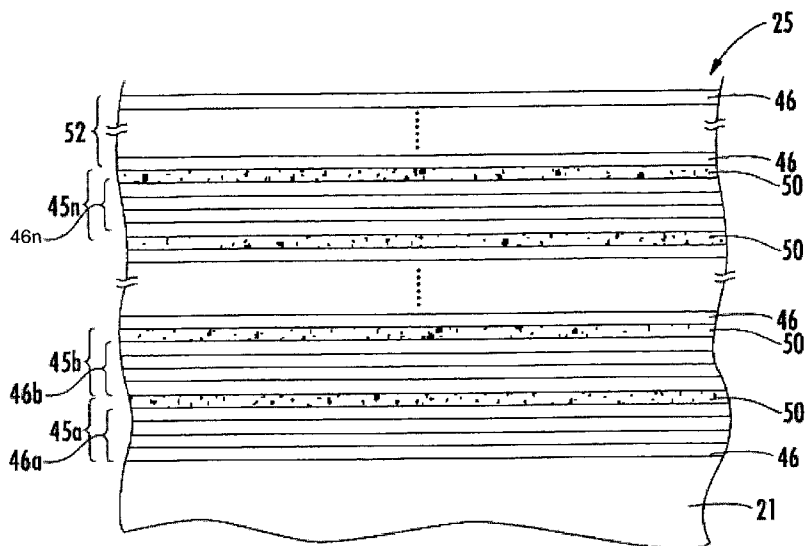
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(54) Title: METHOD FOR MAKING A SEMICONDUCTOR DEVICE INCLUDING BAND-ENGINEERED SUPERLATTICE USING INTERMEDIATE ANNEALING



**FIG. 3**

(57) Abstract: A method for making a semiconductor device includes forming a superlattice including a plurality of stacked groups of layers, with each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. The method also includes performing at least one anneal prior to completing forming of the superlattice.

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# INTERNATIONAL SEARCH REPORT

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PCT/US2006/019290

**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. H01L21/20 H01L21/205

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2005/018005 A (RJ MEARS LLC [US]; MEARS ROBERT J [US]; YIPTONG JEAN AUGUSTIN CHAN SOW) 24 February 2005 (2005-02-24) the whole document	1-31
Y	US 5 216 262 A (TSU RAPHAEL [US]) 1 June 1993 (1993-06-01) cited in the application column 5, lines 39-45; example 3	1-31
Y	US 6 117 750 A (BENSAHEL DANIEL [FR] ET AL) 12 September 2000 (2000-09-12) column 1, line 64 - column 2, line 15	1-31

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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# INTERNATIONAL SEARCH REPORT

Information on patent family members

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