United States Patent [19]

Hoffman et al.

[11] **3,857,471**

[45] **Dec. 31, 1974**

[54] **TAPELESS PAPER MOTION CONTROL SYSTEM PROVIDING SENSING CIRCUITS TO GOVERN MOTOR INCREMENTING**

[75] Inventors: **Paul R. Hoffman,** Farmington; **Roger S. Naeyaert,** Warren, both of Mich.

[73] Assignee: **Burroughs Corporation,** Detroit, Mich.

[22] Filed: **Sept. 12, 1973**

[21] Appl. No.: **396,353**

[52] **U.S. Cl.** ..... **197/133 R,** 74/348

[51] **Int. Cl.** **B41j 15/04**

[58] **Field of Search** ..... 197/84, 133 R, 127; 74/337, 337.5, 341, 348

[56] **References Cited**

UNITED STATES PATENTS

774,910	11/1904	Crawford	74/348 X
1,206,043	11/1916	Slonecker	74/348
2,842,246	7/1958	Furman et al.	197/133 R
3,123,195	3/1964	Hewitt et al.	197/133 R
3,499,516	3/1970	Schaaf	197/133 R
3,502,190	3/1970	Smith	197/133 R
3,557,929	1/1971	Schaaf	197/133 R
3,643,039	2/1972	Barcomb et al.	197/133 R
3,656,041	4/1972	Bonzano	197/133 R
3,761,000	9/1973	Hagstrom	197/133 R X

OTHER PUBLICATIONS

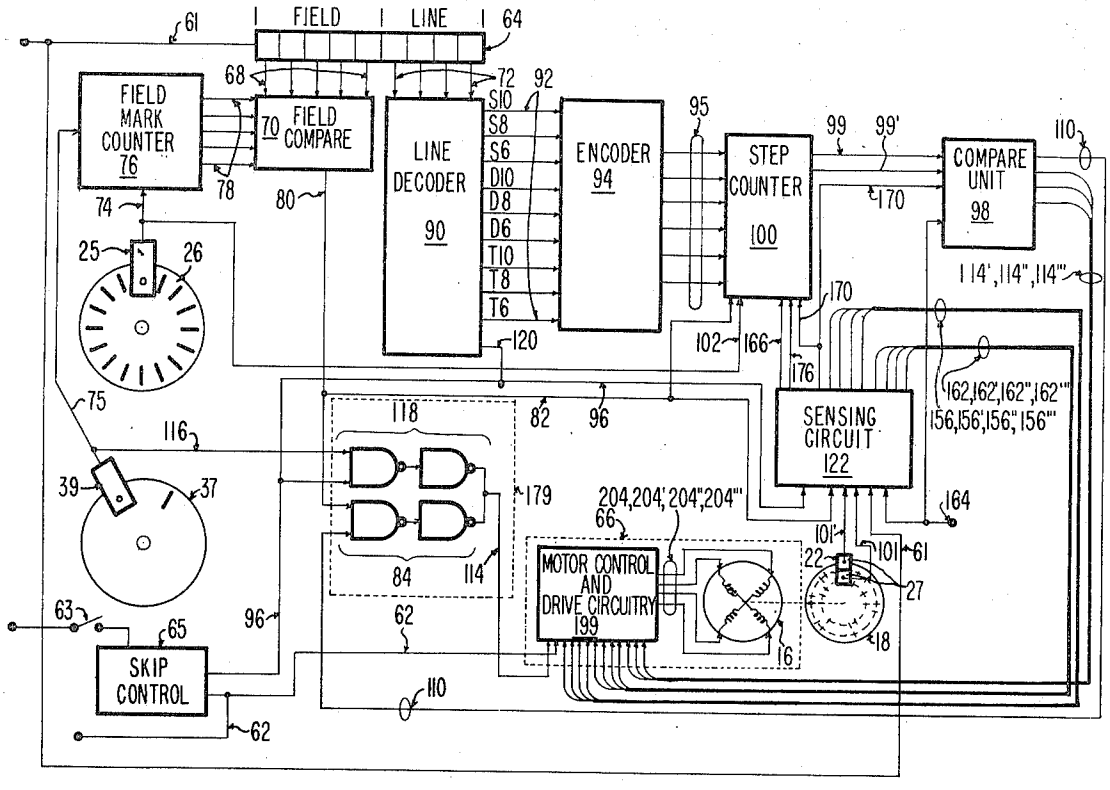
IBM Technical Disclosure Bulletin, "Tapeless Carriage Control," Kerr et al., Vol. 13, No. 3, August, 1970, pp. 657–658.

Primary Examiner—Robert E. Pulfrey
Assistant Examiner—Edward M. Coven
Attorney, Agent, or Firm—Edwin W. Uren; Edward G. Fiorito; Paul W. Fish

[57] **ABSTRACT**

An improved tapeless format control system for a line printer is provided which will control the pitch between printed lines on various length web paper forms. The system includes a stepping motor for driving a paper advance mechanism, a manually operated shift mechanism for selecting the desired one of a plurality of form lengths, and a plurality of photo cells and light sensing devices associated with the stepping motor, the paper advance mechanism and the form length selecting mechanism, the photo cells and sensing devices cooperating with logic circuitry in response to two different types of spacing instructions to provide a wide variety of printing formats on a variety of form sizes to thereby assure optimized flexibility in printing with the line printer, the logic circuitry including a speed retarding device for the stepping motor and a device for checking forward incrementing of the motor using gray code.

42 Claims, 13 Drawing Figures



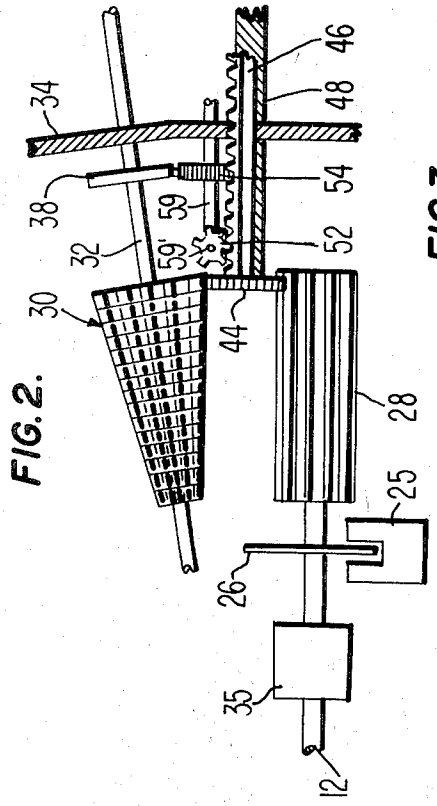


FIG. 2.

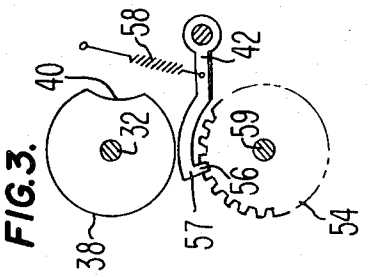


FIG. 3.

FIG. 1.

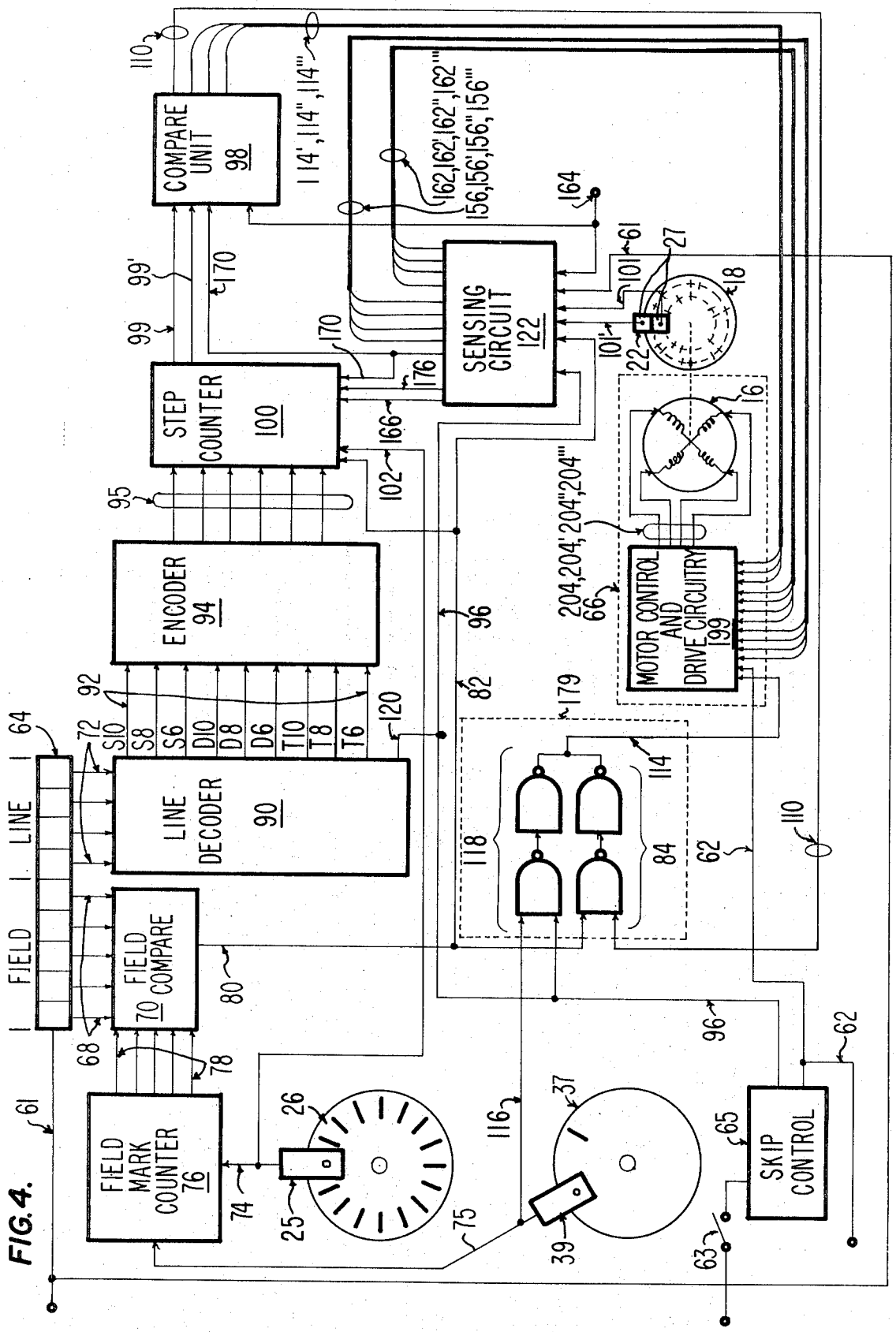

COMPARE UNIT 98
STEP COUNTER 100
ENCODER 94
LINE DECODER 90
FIELD COMPARE 70
FIELD MARK COUNTER 76
SENSING CIRCUIT 122
MOTOR CONTROL AND DRIVE CIRCUITRY 199
SKIP CONTROL
FIELD
LINE
S10
S8
S6
D10
D8
D6
T10
T8
T6
114',114",114'''
162,162',162",162'''
156,156',156",156'''
204,204',204",204'''

FIG. 4.

FIG. 6.

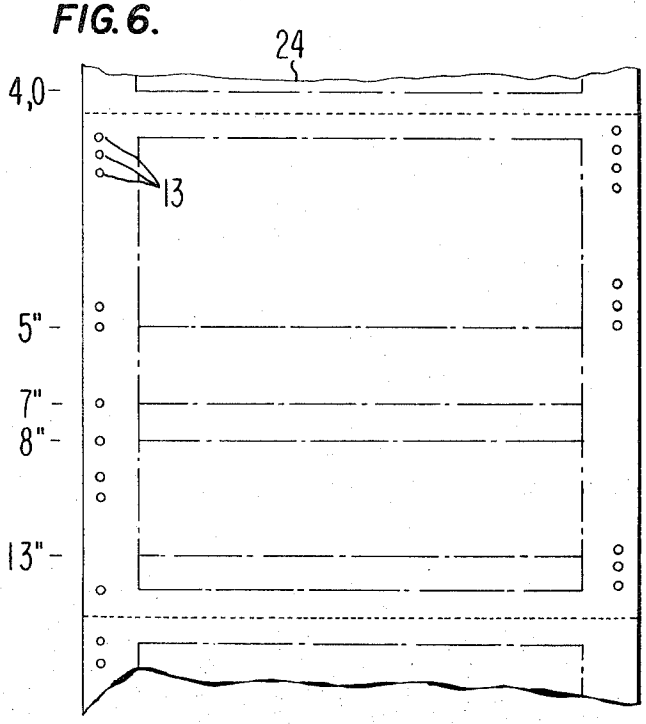


FIG. 8A.

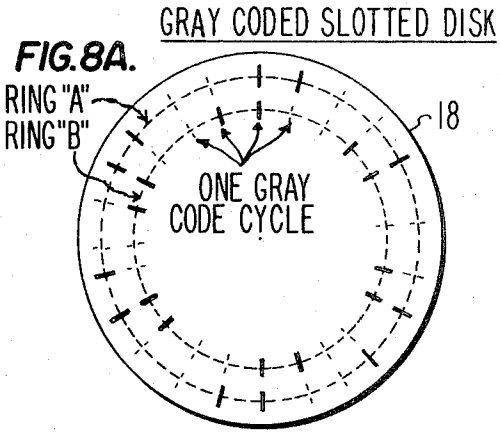


FIG. 8B.

GRAY CODE TABLE

A	B	
0	0	ONE GRAY CODE CYCLE
0	1	
1	1	
1	0	
0	0	ONE DISK REVOLUTION
0	1	
0	1	
0	0	
1	0	
1	0	
1	1	
1	1	
1	0	
1	0	
1	1	
1	1	
0	1	
0	1	
0	0	
0	0	
1	0	
1	0	
1	1	
1	1	
0	1	
0	1	
0	0	
0	0	
1	0	
1	0	
1	1	
1	1	
0	1	
0	1	
0	0	
0	0	
1	0	
1	0	
1	1	
1	1	
0	1	

FIG. 5

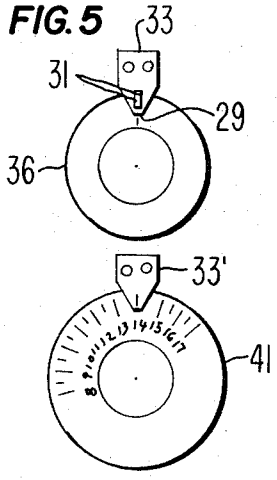


FIG.7A.

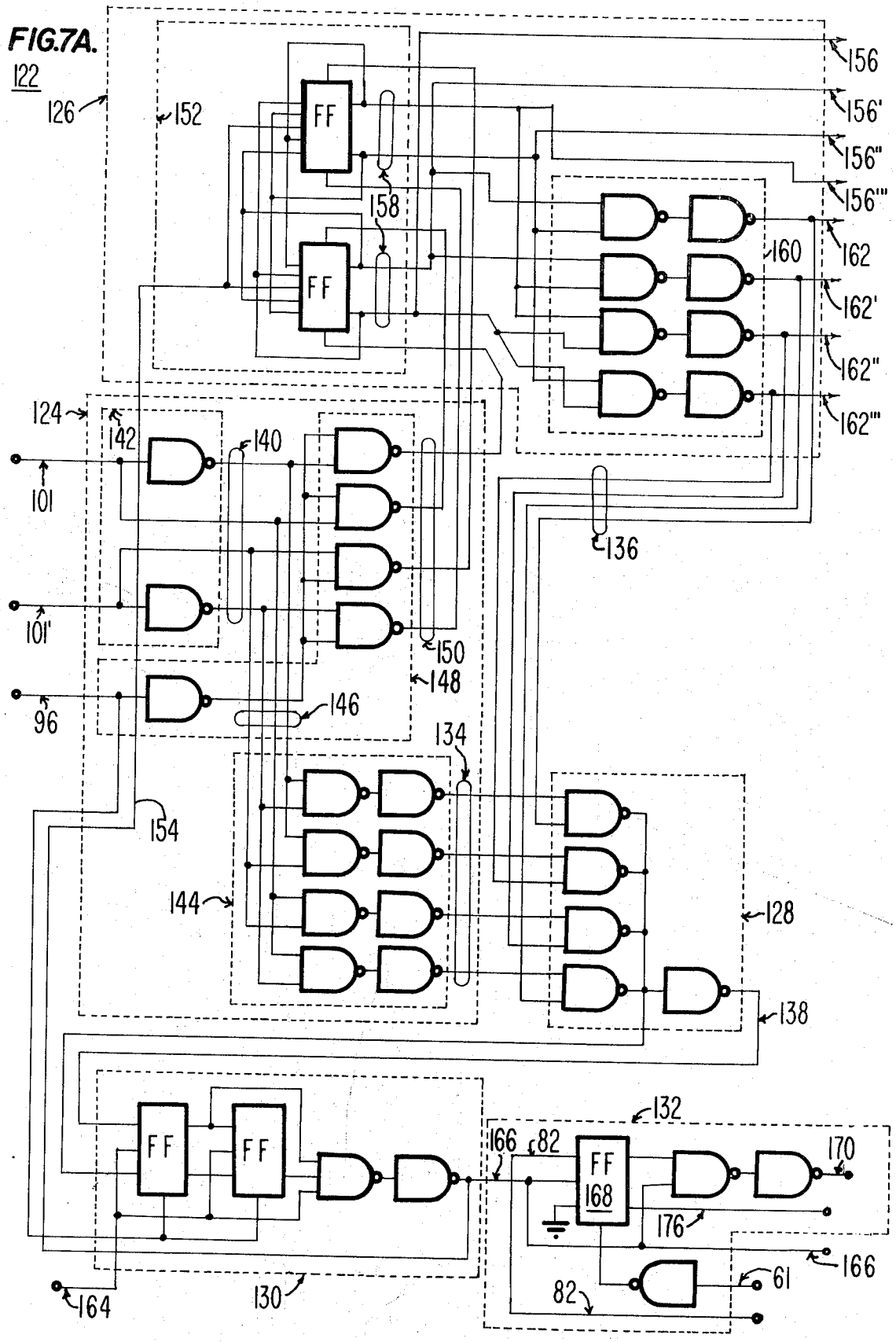

122
126
152
FF
FF
158
156
156'
156"
156'"
160
162
162'
162"
162'"
124
142
140
101
101'
96
150
148
146
136
134
154
144
128
138
FF
FF
132
166
82
FF
168
170
176
166
61
82
164
130

FIG.7B.

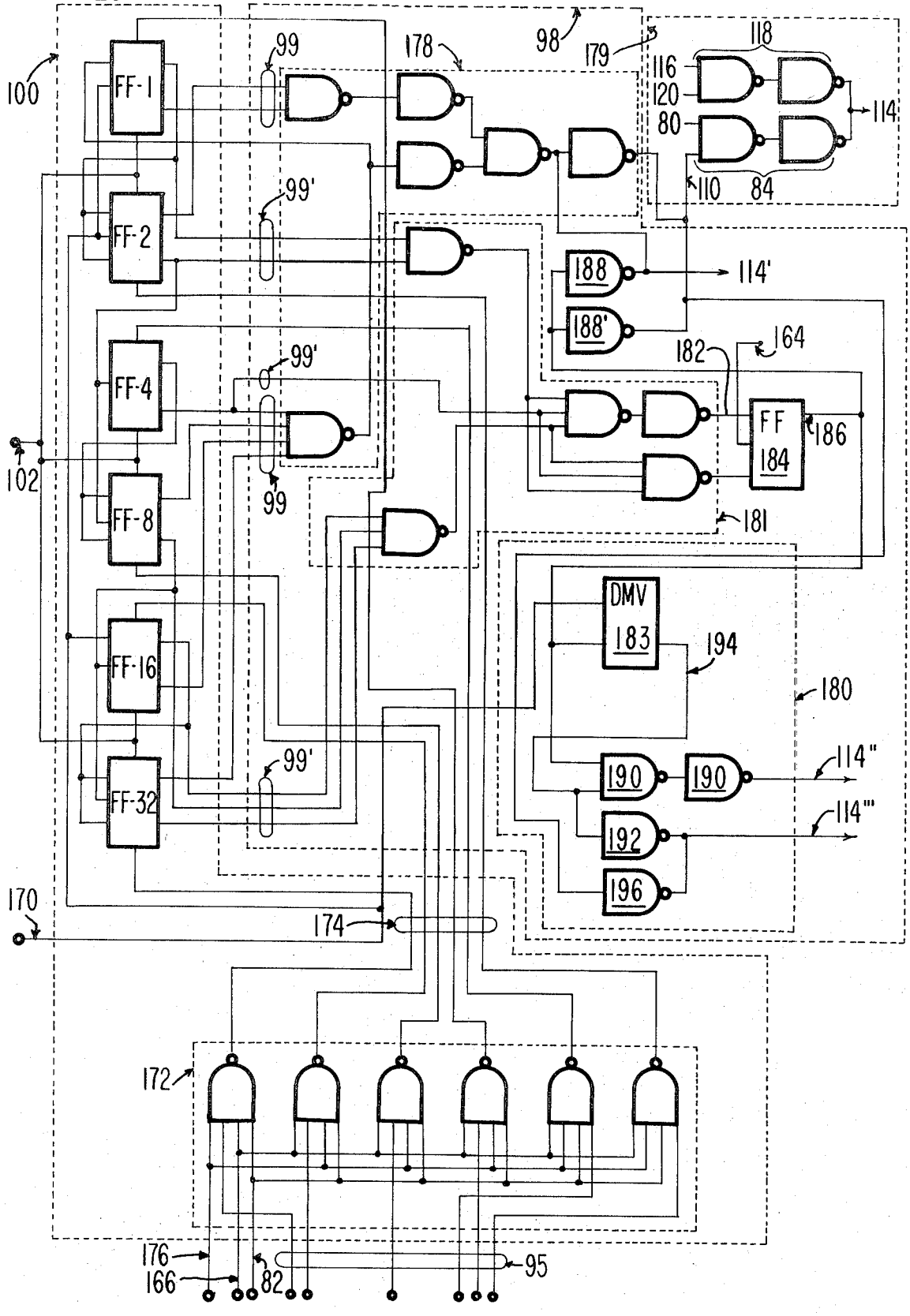

100
FF-1
FF-2
FF-4
FF-8
FF-16
FF-32
99
99'
99'
99'
99
102
178
98
179
118
116
120
80
114
110
84
188
188'
114'
164
182
FF
184
186
181
DMV
183
194
180
190
190
114"
192
114'''
196
170
174
172
176
166
82
95

FIG. 7C.

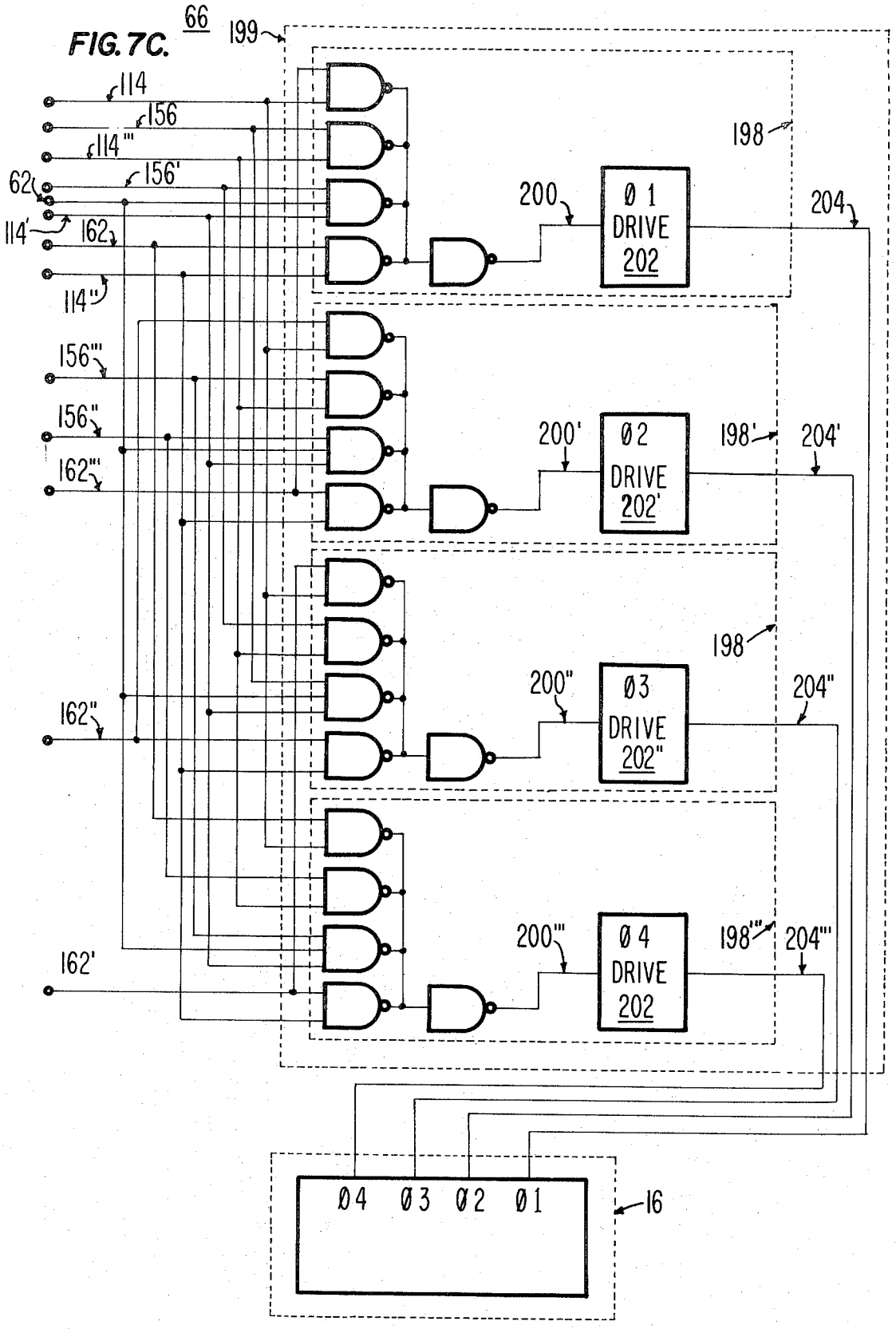

66
199
114
156
114'''
156'
62
114'
162
114''
156'''
156''
162'''
162''
162'
198
200
Ø 1
DRIVE
202
204
200'
Ø 2
DRIVE
202'
198'
204'
198
200''
Ø 3
DRIVE
202''
204''
200'''
Ø 4
DRIVE
202
198'''
204'''
Ø4 Ø3 Ø2 Ø1
16

FIG. 9A.

STEP COUNTER TABLE

LINE INSTRUCTION	STEP COUNTER STATE AT ANY GIVEN STEP FF-32	FF-16	FF-8	FF-4	FF-2	FF-1	STEPS REQUIRED TO REACH HOME POSITION	
TS-6	1	0	1	1	1	0	60	A~171
	1	0	1	1	1	1	59	
	1	0	1	1	0	0	58	
	1	0	1	1	0	1	57	
	1	0	0	0	1	0	56	
	1	0	0	0	1	1	55	
	1	0	0	0	0	0	54	
	1	0	0	0	0	1	53	
	1	0	0	1	1	0	52	
	1	0	0	1	1	1	51	
	1	0	0	1	0	0	50	
	1	0	0	1	0	1	49	
	1	1	1	0	1	0	48	
	1	1	1	0	1	1	47	
	1	1	1	0	0	0	46	
TS-8	1	1	1	0	0	1	45	A~171
	1	1	1	1	1	0	44	
	1	1	1	1	1	1	43	
	1	1	1	1	0	0	42	
	1	1	1	1	0	1	41	
DS-6	1	1	0	0	1	0	40	A~171
	1	1	0	0	1	1	39	
	1	1	0	0	0	0	38	
	1	1	0	0	0	1	37	
TS-10	1	1	0	1	1	0	36	A~171
	1	1	0	1	1	1	35	
	1	1	0	1	0	0	34	
	1	1	0	1	0	1	33	
	0	0	1	0	1	0	32	
	0	0	1	0	1	1	31	
DS-8	0	0	1	0	0	0	30	A~171
	0	0	1	0	0	1	29	
	0	0	1	1	1	0	28	
	0	0	1	1	1	1	27	
	0	0	1	1	0	0	26	
	0	0	1	1	0	1	25	
DS-10							24	A~171
							23	

FIG. 9B.

DS-10	0 0 0 0 1 0	24	A. 171
	0 0 0 0 1 1	23	
	0 0 0 0 0 0	22	
	0 0 0 0 0 1	21	
SS-6	0 0 0 1 1 0	20	A. 171
	0 0 0 1 1 1	19	
	0 0 0 1 0 0	18	
	0 0 0 1 0 1	17	
	0 1 1 0 1 0	16	
SS-8	0 1 1 0 1 1	15	A. 171
	0 1 1 0 0 0	14	
	0 1 1 0 0 1	13	
SS-10	0 1 1 1 1 0	12	A. 171
	0 1 1 1 1 1	11	
	0 1 1 1 0 0	10	
	0 1 1 1 0 1	9	
	0 1 0 0 1 0	8	
	0 1 0 0 1 1	7	
	0 1 0 0 0 0	6	
	0 1 0 0 0 1	5	B. 177
	0 1 0 1 1 0	4	
	0 1 0 1 1 1	3	
	0 1 0 1 0 0	2	
	0 1 0 1 0 1	1	
	1 0 1 0 1 0	0	C. 173

A. 60, 45, 40, 36, 30, 24, 20, 15 AND 12 (171) = LINE INSTRUCTION INITIALIZATION POINTS FOR THE STEP COUNTER 175.

B. 5 = BRAKING CIRCUIT ACTIVATION POINT 177.

C. COMMON HOME POSITION 173.

TAPELESS PAPER MOTION CONTROL SYSTEM PROVIDING SENSING CIRCUITS TO GOVERN MOTOR INCREMENTING

CROSS REFERENCE TO A RELATED APPLICATION

The present invention related to and represents an improvement over the tapeless format control apparatus described and claimed in a patent application entitled "A Tapeless Format Control System" by Paul R. Hoffman, such application, also assigned to the assignee of the present invention, having been filed on June 1, 1973 and assigned Ser. No. 366,122.

FIELD OF THE INVENTION

The invention relates generally to a format control system for line printers and more particularly to a tapeless format control system for controlling the advancement of web paper in a line printer.

BACKGROUND OF THE INVENTION

As pointed out in connection with the disclosure of the above-referenced patent application, Ser. No. 366,122, many prior art printing systems make use of prepunched paper tape loops to control the spacing and arrangement of printed information on paper forms. Such loops are generally provided with rows and columns of machine readable apertures which represent spacing and formatting control instructions, the tapes being selectively and individually installable in tape sensing devices in the printer where they are advanced in synchronism with the advancement of the web paper. During this synchronized advancement of the tape loops, the apertures therein are sensed by sensing means, whereupon pulses resulting therefrom are transmitted through appropriate circuitry to the web paper advancing means of the printer, the web paper advancing means being thereby controlled from a starting and stopping standpoint to produce the desired arrangement of the printed information on the web paper forms. The control instructions represented by the apertures in the tape loops are generally combined with line selection instructions transmitted to the printer from a central processor or other extraneous control device.

Format control tapes of the kind commonly used in prior art line printers, and in format control apparatus forming a part thereof, have generally been characterized by two different categories of problems, a first category involving the operational characteristics of the apparatus used for sensing and advancing the tapes, and the second category involving the condition and storage requirements of the tapes themselves. Prominent among the first category of problems are the inertial tendencies of prior art tape advancing apparatus, such tendencies frequently causing the start-up or stopping motion of the tape to either lag behind or to run ahead of the starting or stopping of web paper motion, thereby giving rise to the disruption of the required synchronization between the tape and the web paper. Included in the second category of problems, involving the tapes themselves, are the need of maintaining space-taking files for storing a plurality of tapes that are not in active usage, the tendency of the tapes to become worn and dilapidated through excessive use or misuse, and the likelihood of error in either punchably

producing the tapes or in effecting installation thereof in the tape sensing and advancing apparatus.

An additional problem common both to line printers using and those not using carriage control tapes is that of oscillatory motion of the web paper about the area of the new line position. The closer the line advancing mechanism is to running in a "slew" condition before it is stopped at the new line position, the more pronounced the problem of oscillatory motion becomes.

A further problem particularly relevant to line printers using stepping motors as paper advancement drive units is that of knowing whether the required forward incrementing of the paper has been experienced, according to instruction, or whether single increments of back stepping have occurred. Here again, the tendency to back step or to non-step is aggravated when the paper advancement mechanism approaches a "slew" condition.

SUMMARY OF THE INVENTION

It is accordingly an object of the present invention to provide a tapeless format control system for use in high speed line printers, such system being completely reliable in operation and ideally flexible in its ability to produce the desired formatting of printed information on any desired form length.

It is another object of the present invention to provide an improved tapeless format control system that will facilitate bringing the web paper advancement mechanism of the line printer from a high speed condition to a controlled stop at a new line position.

Still another object of the present invention is to provide an improved tapeless format control system wherein incrementing of a stepping motor is fully controlled and wherein precise execution of a previous spacing instruction is a prerequisite to the execution of a new spacing instruction.

The present invention is directed to a tapeless format control system for use in line printers, such system including a stepping motor for incrementally advancing the web paper, means for selectively determining the length of the paper form upon which the printed information is to be arranged, means for controllably retarding the web paper's advancement as it approaches a new line position, a plurality of pulse generating means for identifying each increment of motion of the stepping motor, each increment of advancement of the web paper, and the passage of each unit of selected form length past the print station, means for comparing the previous position of the stepping motor with its present position so as to allow further incrementing of the stepping motor only when the preceding incrementing step has been successfully completed, means also being provided for receiving and storing skip and line advance spacing instructions from a central processor, and for controllably coordinating such extraneous instructions with said plurality of identifying pulses such that each line of information printed on the selected form length is properly spaced from the preceding lines and all of the lines of printed information conform to the preselected format represented by the extraneous instructions.

BRIEF DESCRIPTION OF THE DRAWING

These and other objects and advantages of the invention will become apparent from the following description when read in conjunction with the accompanying drawing figures, in which:

FIG. 1 is a partial perspective view showing various of the elements of the inventive format control system in association with web paper advancing means in a line printer;

FIG. 2 an elevational view of various of the elements shown in FIG. 1;

FIG. 3 is a view taken in the direction of the arrow 3 of FIG. 2;

FIG. 4 is a schematic block diagram illustrating the logic circuitry of the inventive format control system;

FIG. 5 is a plan view of the adjustable dials shown in FIG. 1;

FIG. 6 is a view of a portion of the continuous web paper used in the line printer, separable form sheets thereof being represented by perforated lines and representative printing lines thereon being identified by a plurality of broken lines;

FIG. 7A is a schematic component diagram illustrating the sensing circuit of the inventive format control system;

FIG. 7B is a schematic component diagram illustrating the step counter and compare unit circuits of the inventive format control system;

FIG. 7C is a schematic component diagram illustrating the motor control unit of the inventive format control system;

FIG. 8A illustrates the gray code as it appears on the slotted motor step disk;

FIG. 8B is a table of the gray codes in binary form for one revolution of the slotted motor step disk;

FIGS. 9A and 9B represent a table of the coded counting sequence for the step counter as it counts down from a given initialized position, representing a line instruction, to a common home position.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The inventive tapeless format control system is comprised of a stepping motor for incrementally advancing the web paper, means for selectively determining the length of the paper form upon which the printed information is to be arranged, a plurality of pulse generating means for identifying each increment of rotational motion of the stepping motor, each increment of advancement of the web paper, and the passage of eah unit of selected form length past the print station, means for receiving and storing externally originated skip and line advance spacing instructions, and means for controllably coordinating the skip and line advance instructions with the plurality of identifying pulses such that each line of information printed on the selected form length is properly spaced from the preceding lines, the latter coordinating means including means for controlling the incrementing of the stepping motor such that each forward step is dependent upon the successful completion of the preceding step, and means for retarding the speed of the stepping motor as it approaches a selected print position such that paper advancement is brought to a precise stop. Each of these broadly defined elements of the inventive format control system will be hereinafter described from a structural and functional standpoint, with reference to the accompanying drawing figures.

As illustrated in FIGS. 1 and 4, a stepping motor 16 fixed to the framework (not shown) of a line printer is provided with an incrementally rotatable motor shaft 20 to the outermost extremities of which are fixed a photocommutator disk 18 disposed in cooperating relationship with a sensing device 22, and a toothed pulley 21 which is coupled to a predeterminately larger toothed pulley 23 by means of a belt 14. The pulley 23 is fixed to an extremity of a paper advance shaft 12 which is provided with fixed and spaced-apart sprockets 10, the extending teeth of the sprockets being cooperably engageable with perforations 13 arranged along the outermost edges of the web paper 24.

The previously mentioned means for selectively determining the length of the paper form upon which the printed information is to be arranged is comprised of a conically configured stack of variously diametered gears generally indicated at 30 in FIGS. 1 and 2, such gears being fixed to a shaft 32 that is journaled in a frame member 34 (FIG. 2). In the preferred embodiment of the invention, the conical stack of gears 30 is comprised of a total of eighteen gears ranging in toothed circumference from 17 to 34 teeth, each gear having one additional peripheral tooth over its smaller diametered adjoining gear, the smallest diametered 17-toothed gear representing an 8½ inch form length and the largest diametered 34-toothed gear representing at 17 inches form length, each of the gears therebetween representing different form lengths of half inch differential. The conical stack of variously diametered gears 30 is operatively coupled to the paper advance shaft 12 by means of an elongated wide-faced gear 28 fixed to the rightmost extremity of the shaft 12, and a rotatably and translatably supported idler gear 44, rotation of the paper advance shaft 12 by the stepping motor 16 thereby providing rotational movement to the idler gear 44 and to the conical gear stack 30. Selection of a given form length within the previously defined range of from 8½ inch to 17 inches is accomplished by manually rotating a dial 41 to bring the indication mark corresponding to the given form length (FIG. 5) into alignment with a single mark on a cursor 33', rotation of the dial 41 being effective to rotate a supporting shaft 59 and a pair of bevel gears 55, 53 (FIG. 1), the bevel gear 53 being fixed to a suitably supported and normally disposed short shaft 59' to the other extremity of which is fixed a pinion gear 52. It can be seen from FIG. 1 that the pinion gear 52 is engaged with the linearly arranged teeth of a rack 46, the rack 46 being translatable on a supporting and retaining base member 48. The rack 46 is provided on its innermost extremity with a short mounting shaft (not shown) upon which the idler gear 44 is rotatably mounted. It can thus be seen that rotation of the dial 41 will serve to effectuate a corresponding translation of the rack 46, by means of the shafts 59 and 59', the fixed gears 55—53 and the pinion gear 52, to thereby engage the coupling gear 44 with the individual gear of the stack 30 that corresponds to the indexed form length.

As may be suggested by the hereinafter described detenting means illustrated in FIGS. 2 and 3, the form selection dial 41 may be manually rotated only after the conical gear stack 30 has been returned to a home position wherein corresponding peripheral teeth of the various gears in the stack are aligned to enable translation

of the coupling gear 44. This home position of the gear stack 30 is defined by the central coincidence of a line mark 29 on a home positioning dial 36 relative to a pair of marks 31 on a cursor 33, as best shown in FIG. 5. FIGS. 1 and 3 are illustrative of the detenting means effective for preventing manual rotation of the form selection dial 41 when the gear stack 30 is displaced from its above defined home position. This detenting means is comprised of a locking wheel 38 fixed to the shaft 32, a peripherally notched or toothed detent wheel 54 fixed to the shaft 59, and a rockably supported and biased detent arm 42 interposed between the wheels 38 and 54. The locking wheel 38 is provided with a concave recess 40 which is conformably aligned with a curved portion 57 of the detent arm 42 only when the dial 36 and gear stack 30 are located in their home positions, such conformable alignment of the recess 40 permitting a spring 58 to rock the detent arm 42 such that a projection 56 thereof is displaced from its engageable locking relationship with the wheel 54. When the dial 36 and gear stack 30 are displaced from their home positions, as when operatively rotated by the wide-faced gear 28 and idler gear 44, the raised concentric surface of the locking wheel 38 serves to depressably hold the detent arm 42 and the projection 56 thereof in engageable locking relationship relative to the notches or teeth in the detent wheel 54, against the bias of the spring 58.

In accordance with the above description, the selection of a given form length may be accomplished by first rotating the dial 36 to its home position, to thereby align corresponding peripheral teeth of the individual gears of the gear stack 30 and to enable the spring 58 to disengage the detent arm 42 from the wheel 54, and by then rotating the form selection dial 41 to a position corresponding to the desired form length, the idler gear 44 being thereby translated into engaged relationship with the individual gear of the stack 30 that corresponds to the desired form length. It is to be noted that a disconnect clutch 35 (FIG. 1) is provided intermediate the paper advance shaft 12 and the wide-faced gear 28 to permit rotation of the dial 36 and gear stack 30 without disturbing the position of the shaft 12 or the web paper 24.

The aforementioned plurality of pulse generating means forming a part of the present invention includes a double ringed multi-slotted photocommutator disk 18 fixed to the motor shaft 20 and its associated sensing device 22, a single-slotted disk 37 fixed to the innermost extremity of the shaft 32 of the previously defined form length selecting means, along with its associated sensing device 39, and a multi-slotted disk 26 fixed to the paper advance shaft 12 intermediate the disconnect clutch 35 and the wide-faced gear 28, the disk 26 being associated with a sensing device 25. Each of the sensing devices 22, 25 and 39 is provided with a well-known light emitting element or photo cell disposed on one side of its associated slotted disk, and a light sensitive switch disposed on the other side of the disk, such elements being effective for pulsably sensing the passage of a slot therebetween. As best shown in FIG. 8A, the double ringed multi-slotted photocommutator disk 18, identified hereinafter as the motor step disk, is provided with 24 equally spaced-apart coded positions in gray code per ring where the coded positions contain up to 12 slots per ring and the multi-slotted disk 26, identified hereinafter as the field mark disk, is provided with 16 equally spaced-apart radial slots. In the preferred embodiment of the invention, each ring of coded positions of the motor step disk 18 is operatively sensed by its own photo cell and associated light sensing switch or sensor 27 of the sensing device 22, thereby providing for the generation of up to 24 codes per ring for each revolution of the motor shaft 20, each of such codes (resulting from the presence or absence of a slot) representing an incremental step of motor shaft movement equal to a 15° angular displacement thereof. The predetermined relative diameters of the motor shaft pulley 21 and the pulley 23 of the shaft 12 are such that each 15° increment or step of motor shaft movement will produce 1/120 inch of web paper advancing movement, a complete revolution of the motor shaft thereby producing 1/5 inch of paper advancement. In the preferred embodiment, also, the diameters of the sprockets 10 on the paper advance shaft 12 have been so predetermined that one revolution of the shaft 12 will produce 8 inches of paper advancement. It can thus be seen that each of the 16 pulses generated during each revolution of the paper advance shaft 12, by a reason of the 16-slotted field mark disk 26 fixed thereto, will serve to represent and to identify a one-half inch incremental advancement of the web paper. It will also be apparent from FIG. 1 that the single-slotted forms index disk 37 will generate a pulse upon each occurrence of the gear stack 30's advanceable return to its home position, such pulse accordingly representing and identifying the advancement of each unit of the selected form length.

The previously mentioned means for receiving and storing skip and line advance spacing instructions from a central processor is comprised of the shift register 64 shown in FIG. 4, such register consisting of a five-digit field advance instruction portion and a four-digit line advance instruction portion, the five digits of the field instruction portion representing the binary decimal digits 1, 2, 4, 8 and 16, and the four digits of the line instruction portion representing the binary decimal digits 1, 2, 4 and 8. It will thus be seen that the field instruction portion of the register 64 will be effective to receive and store 32 separate codes to provide for one-half inch incremental advancements of the web paper, and that the line instruction portion will be effective to receive and store 16 separate codes to provide for various one one-hundred-twentieths inch incremental advancements of the paper, the latter incremental advancements being explained hereinafter in connection with the previously mentioned broadly defined means for controllably coordinating the skip and line advance instructions with the plurality of identifying pulses.

FIG. 4 is illustrative of the means for controllably coordinating the skip and line advance instructions stored in the register 64 with the plurality of identifying pulses generated by the forms index disk 37, the field mark disk 26 and the motor step disk 18. A line decoder 90 is coupled to the line instruction portion of the register 64 by lines 72, and coupled also to an encoder 94 by a plurality of lines 92. It is the function of the line decoder 90 to interpret and give meaning to the 16 possible codes received and stored in the line instruction portion of the register 64. The following table is suggestive of how these 16 codes might be interpreted:

Code		Decoded Instruction
0000	No advance	
0001	Single space 10-per-inch	(S10)
0010	Single space 8-per-inch	(S8)
0011	Single space 6-per-inch	(S6)
0100	Double space 10-per-inch	(D10)
0101	Double space 8-per-inch	(D8)
0110	Double space 6-per-inch	(D6)
0111	Triple space 10-per-inch	(T10)
1000	Triple space 8-per-inch	(T8)
1001	Triple space 6-per-inch	(T6)
1010	Skip to Heading	
1011	Skip to Bottom	
1100, 1101, 1110, 1111	Remaining codes may be utilized for other desired line spacing instructions, such as four spaces at 6-per-inch, and six spaces at 8-per-inch, etc.	

The encoder **94**, which as previously mentioned is coupled to the line decoder **90** by a plurality of lines **92**, functions to compute the number of **one one-hundred-twentieths inch steps of the stepping motor** 16 **that will be required to produce the desired line spacing represented by the particular code stored in the line instruction portion of the register** 64 **and interpreted by the line decoder** 90, **the computed value being then entered in a step counter** 100. **The following table will serve to reflect the number of** 1/120 inch steps of the stepping motor that will be required to satisfy the various line spacing instructions interpreted by the line decoder **90.**

Decoded Instruction	Computation	Value in Terms of Motor Steps Required
S10	1/10" ÷ 1/120"	12
S8	1/8" ÷ 1/120"	15
S6	1/6" ÷ 1/120"	20
D10	2/10" ÷ 1/120"	24
D8	2/8" ÷ 1/120"	30
D6	2/6" ÷ 1/120"	40
T10	3/10" ÷ 1/120"	36
T8	3/8" ÷ 1/120"	45
T6	3/6" ÷ 1/120"	60

In addition to the register **64**, the line decoder **90**, the encoder **94**, and the step counter **100**, the previously mentioned means for controllably coordinating the skip and line instructions with the plurality of identifying pulses also includes a field mark counter **76**, a field compare unit **70**, a compare unit **98**, a motor control unit **66**, and a sensing circuit **122** the function of which will be hereinafter described. It is to be noted from FIG. **4** that the field mark counter **76** is coupled to the forms index disk **37** and its associated sensing device **39** by a line **75**, and to the field mark disk **26** and its associated sensing device **25** by a line **74**, and that the field compare unit **70** is coupled to the field instruction portion of the register **64** by a plurality of lines **68**, and coupled also to the field mark counter **76** by lines **78**.

The field compare unit **70** is coupled to a motor stop and detent control **114** by a line **80**, through a pair of NAND gates **84**. The field compare unit **70**, in addition to being coupled to the motor stop and detent control **114**, is also coupled to a flip flop **168** (FIG. 7A) of a Sensor Sensing Circuit **122** and the step counter **100** by a line **82**. It can be seen from the above described couplings of the various elements that the field mark counter **76** is reset by each pulse generated by the forms index disk **37** and transmitted along the line **75**, and is countably advanced by each pulse generated by the field mark disk **26** and transmitted along the line **74**. It will be apparent that the field compare unit **70** will function to continuously compare the accumulated count in the field mark counter **76** with the binary coded instruction stored in the field instruction portion of the register **64**, and will transmit a signal indicating a true state along the line **80** to the NAND gates **84**, and along the line **82** to the flip flop **168** of a Sensing Circuit **122**, whenever an equals or true state is detected therein.

The step counter **100** is coupled to the motor step disk **18** and its associated sensing device **22** through the sensing circuit **122**. The sensing circuit **122** as shown in FIG. 7A is comprised of a sensor gating circuit **124**, a sensor storage circuit **126**, a sensor compare circuit **128**, and a pulse generator circuit **130–132**. The purpose of the sensing circuit **122** is to allow the stepping motor **16** to increment only after successfully completing the previous increment of one forward step. Using signals on line **134** of the gating circuit **124** gained by sensing of the gray-coded slots on the motor step disk **18**, combined with the stored signals on line **136** from the storage circuit **126**, resulting from the previously sensed gray coded slots, will give a comparison signal on line **138** indicating a correct increment that will be unique to 60° of rotation of the motor step disk **18** in either direction. If there is an error condition, the sensing circuit **122** will not allow the stepping motor **16** to continue to rotate until a correct sensor comparison is made by the sensor compare circuit **128**.

The sensor gating circuit **124** receives the separate gray coded signals generated by the sensing device **22** from the slotted rings "A" and "B" of the motor step disk **18**. FIGS. 8A and 8B show the gray coded slit arrangement of disk **18**, and a table of the gray codes, respectively, in the sequential order in which they will cyclically appear on the disk **18**. These "A" and "B" signals on lines **101** and **101'** respectively (FIGS. 4 and 7A) are further subdivided into lines **140** (FIG. 7A) for signal A "on", signal A "off", signal B "on", and signal B "off" by means of the lines and NAND gates of circuit **142**. An additional plurality of NAND gates **144** are included using signals on lines **146** from the above subdividing circuit **142** as inputs to provide a unique signal on lines **134** for any combination of the "A" and "B" gray coded signals being sensed.

Another function of the sensor gating circuit **124** is to allow the subdivided signals on line **140**, before printing is to begin, to initialized on lines **150** the flip flops **152** of a sensor storage circuit **126** through a series of NAND gates **148**, whenever the skip control circuit is enabled on line **96**. Thus the electronics of the format control system will start out in sync with the stepping motor **16**. Whatever gray coded position the motor step disk **18** is in at system start up time will be recorded in the sensor storage circuit **126**.

The flip flops **152** of the sensor storage circuit **126** will be triggered by a signal on a line **154** from the pulse generator circuit **130–132** every time a correct increment of the stepping motor **16** has been made and are so interconnected so as to have the immediately previously sensed gray coded signals as their respective states. The direct outputs on lines **156**, **156'**, **156''**, **156'''** from these flip flops **152** are used as bias signals for the "run" and "full-brake" functions of the motor

drive unit 66 to be explained hereinafter. Also, the outputs on lines 158 from flip flops 152 are gated in circuit 160 so that all possible combinations of two of their outputs may be represented by one unique signal on lines 162, 162', 162'', 162''', corresponding to previously sensed "A" and "B" gray coded signals as placed in the sensor storage circuit 126. Thus only one of these four sets of gates in circuit 160 will output at any given time on lines 162, 162', 162'', 162'''. These combined signals on lines 162, 162', 162'', 162''' are used in the motor control unit 66 for "stop" and "brake-step" biasing and additionally as inputs to the sensor compare circuit 128 as will be later explained.

The sensor compare circuit 128 functions to compare the sensor gating circuit signal on lines 134 representing the presently sensed gray coded signal with the sensor storage signal on lines 162, 162', 162'', 162''' representing the immediately previously sensed gray coded signal. As an example of such comparison, with reference to FIGS. 8A, 8B and 7A, if the sensor storage circuit 126 has a signal A of "O" and a signal B of "O" stored in it representing the immediately previously executed slot position, then the sensor gating circuit 124 should presently be receiving a signal A of "O" and a signal B of "1" on lines 101 and 101' respectively in order for the sensor compare circuit 128 to output a signal on line 138. When the presently sensed signal is one step forward of the previously sensed signal then the sensor compare circuit 128 will output a signal indicating a good compare.

The pulse generator circuit 130–132 (FIG. 7A) serves as the source of trigger pulses for the flip flops 152 of sensor storage circuit 126 (along the line 154), and for the step counter 100 and the compare unit 98 (along line 170). The triggering input for the first stage 130 of the pulse generator circuits 130–132 itself is the clock of the central computer processor coming in on line 164 in the preferred embodiment. The bias for the first stage 130 of the pulse generator circuit 130–132 is received from the sensor compare circuit 128 on line 138. Since the trigger rate of the central processor clock is very much higher than the sensor compare circuit bias rate, as it is applied, the sensor compare circuit 128 bias application rate becomes defacto the pulse generator 130–132 circuit output trigger rate. The flip flops and associated NAND gates of the first stage 130 of the pulse generator circuit 130–132 will thus output trigger pulses to the second stage 132 of this circuit 130–132 on line 166, and also to the sensor storage circuit 126 on line 154, whenever a correct increment of the stepping motor 16 has been made, whether in execution of a field or line instruction. It will be noted that the flip flops of this first stage 130 may be reset by a skip control signal on line 96. A flip flop 168 and associated NAND gates of a second stage 132 of the pulse generator circuit 130–132, on the other hand, will only begin outputting triggering pulses upon receipt of a trigger pulse on line 166 from the first stage 130 and also of an initializing signal from the field compare 70 on line 82. It will be noted that the flip flop 168 is always grounded to its low state except when a line instruction is to be executed, at which point it is triggered by the first stage 130 and biased by a signal on line 82 to its high state to thereby output a signal on line 170. It will be noted that a signal on line 82 will only be present upon completion of a field instruction. The flip flop 168 will be reset back to its low state everytime a new signal is sent on line 61 to the register 64. The signal appearing on line 82 indicates completion of a field instruction and the permissive beginning of a line instruction. The pulse outputted on line 170 by the second stage is used to trigger the step counter 100 and also the braking circuit 180 of the compare unit 98 as will be explained hereinafter.

The step counter 100 of this system, as illustrated in FIG. 7B, is a six stage binary counter consisting of flip flops FF-1, FF-2, FF-4, FF-8, FF-16 and FF-32 going from low to high stages respectively, such counter having been designed to count down to a home position 173 in a binary manner as shown in the table in FIGS. 9A and 9B. At the beginning of a line instruction, the step counter 10 will be set by the encoder 94 on line 95 to whatever number of steps are required to accomplish the line instruction given in the register 64. Thus if SS-10 is desired as a line instruction, the step counter 100 will be set to (011110) which is equivalent to 12 steps as shown at 171. As the stepping motor 16 begins incrementing for the line instruction, the step counter 100 will begin counting down at one count per completed step until the counter 100 reaches (101010) which is the common home position shown at 173 for all line settings of the counter 100, at which point the stepping motor 16 will lock into its stop position. The step counter 100 is reset to a zero state every time a signal appears on line 102, which is every ½ inch of paper advance as recorded by the sensing device 25. The encoder 94, on the other hand, is always outputting a setting signal on line 95. Thus at the beginning of an execution of a line instruction, the stepping counter 100 will be reset to zero by a signal on line 102. Next, initializing NAND gates 172 coupled to the line 95 will output control signals on lines 174 for the brief instant when an input signal is received on line 82 from the field compare 70, an input signal from the first stage 130 is received on line 166, a low state signal from flip flop 168 is received on line 176, and encoder 94 signals are received on lines 95 such signals being received simultaneously to thus initialize on line 174 the step counter 100 to a value corresponding to the desired current line instruction as represented at 175 in FIGS. 9A and 9B.

As the step counter 100 is triggered by the pulse generator circuit 130–132 from its initialized line position to its home position, the compare unit 98 continuously samples the state of the step counter 100 on lines 99 and 99' and outputs function signals on lines 114, 114', 114'', 114''' to the motor control unit 66 reflecting the current step being processed. The step counter 100 outputs are NAND gated up through two distinct NAND trees 178 and 180 of the compare unit 98, the first tree 178 for controlling the "stop and run" functions through stop and run control signals on output lines 114 and 114' respectively of the stepping motor 16, and a second tree 181 for controlling the braking circuit 180 of the stepping motor 16. At the top or output point of the first NAND tree 178, there are two separate output lines, one for stop on lines 110 and 114, and one for run on line 114' (FIG. 7C). In the time interval between the time the step counter 100 is initialized and the time at which the step counter 100 reaches its home position, the "run" signal along line 114' may be activated to merely indicate an absence of a stop signal on line 110, which in turn means that the home position has not yet been reached by the step counter 100,

thereby allowing the stepping motor **16** to continue to increment. Once the step counter **100** has reached its home position (101010) in FIGS. **9A** and **9B**, the "stop" signal on line **114** will be outputted to disallow any incrementing by the stepping motor **16.** The "stop" signal on line **110** will continue to be outputted until the step counter **100** is reset to zero by a signal on line **102.** The stop signal on line **110** is inputted into gating circuitry **179** (FIGS. **4** and **7B**) where the stop signal on line **110** is inputted to NAND gates **84** as is the field compare completion signal on line **80.** Concurrent receipt of these signals will cause NAND gates **84** to output a motor stop and detent control signal on line **114** to the motor control unit **66.**

At the top or output point of the second NAND tree **181** (FIG. **7B**), a signal outputted on line **182** by the final NAND gate in the tree will indicate that the stepping motor **16** is five steps away (010001) from its home position (101010) as determined from the outputs of the step counter **100.** The signal outputted by the second tree line **182** is used for biasing the high input side of its associated flip flop **184.** As this flip flop **184** is triggered by the high frequency central processor clock signal on line **164** (as was the first stage **130** of pulse generator circuit **130–132**), application of bias by line **182** to the flip flop **184** will cause it to be almost immediately switched to its high state. As the low input side of the flip flop must receive a signal through an associated NAND gate that is the complete truth negation of the high input side signal in order to change its state, the flip flop then will only be triggered back to its low side upon a zero reset signal on line **102** as used by the step counter **100.** The net result of this is that once the flip flop **184** has been set to its high side, it will stay there for the last five steps leading to the home position of the stepping motor. Once the flip flop outputs a signal on line **186** from its high side, a connected NAND gate **188** will deliver this signal to a point having a common terminal with the "run" signal line **114'**, thereby effectively cancelling the "run" signal when both are preset, the significance of which will be described more fully hereinafter. An additional NAND gate **188'** is supplied with an input common to NAND gate **188** and whose inverted output is used to cancel any premature lock or stop signals on line **110** as a result of residue currents in the first NAND tree **178.** Five steps away (**177** in FIGS. **9A** and **9B**) from the home position was chosen as the maximum number of steps that the braking circuit **180** requires to controllably retard the speed of the stepping motor **16** to prevent any overshoot or oscillation over or about the home position respectively. The braking circuit **180** in this embodiment comprises a delayed multivibrator (DMV) **183** and associated NAND gates for outputting a brake step function signal on line **114''** and a full brake function signal on line **114'''**. The DMV **183** is biased by a signal on line **186** from the high side of flip flop **184.** Once so biased, the DMV **183** will output a signal on line **194** upon receipt of a triggering pulse on line **170** from the second stage **132** of the pulse generating circuit **130–132** which corresponds to the beginning of each of the last five steps mentioned above. The adjustable period of the output signal on line **194** from the delayed multivibrator **183** will never be any longer than the shortest anticipated interval between increments of the stepping motor **16,** or in other words, the fastest expected speed of the motor **16.**

The output signal on line **194** from the DMV **183** will be inverted and shaped by an operatively coupled NAND gate **192** to become what is called a Full Brake Signal on line **114'''** (FIG. **7C**) which is actually a reverse run signal in that the windings of the stepping motor **16** are excited in a mode reverse to that of the normal run mode, thereby giving a braking effect to a forward moving stepping motor **16** when activated. As the stepping motor **16** begins to slow down as a result of the cancelling of the "run" signal on line **114'**, and application of the "full brake" signal on line **114'''**, the DMV **183** for a given adjustable output period, will begin to "time out" or be off for increasingly longer periods near the end of each step as the stepping motor **16** increments closer to the home position. This effect is taken advantage of by also feeding the output of the DMV **183** into its second series of associated NAND gates **190.** These NAND gates **190** will be activated to output a signal on line **114''** whenever concurrently the DMV **183** is not outputting a signal on line **194** and the flip flop **184** is outputting a signal on line **186.** The signal outputting outputted by NAND gates **190** on line **114''** is called a brake step and is used to power the stepping motor **16** in a manner similar to the "run" signal on line **114'** except that only one of the four motor windings of the stepping motor **16** are excited at any given time. The purpose of this being to power the stepping motor **16** forward at a relatively low speed for increasingly longer periods as home position is approached, so that the stepping motor **16** is neither over or undershooting its home position. Once the home position is reached by the stepping motor **16,** the first NAND tree **178** will become true and a stop signal on line **110** will output to stop and lock the motor **16** in place, that is, the stator and rotor windings of the stepping motor **16** having like phases will line up with each other. The stop signal on line **110** through a NAND gate **196** will also cancel the full-brake signal on line **114'''** if there happens to be any residue left as outputted by the DMV **183** on line **194** when home position is reached, thereby preventing the stepping motor from backing away from home position. As can be seen from the above, the full-brake signal on line **114'''** will pre-empt the run signal on line **114'**, likewise the step-brake signal on line **114''** will pre-empt the full-brake signal on line **114'''**, and finally the "stop" signal on line **110** will pre-empt the brake-step signal on line **114''**. In effect, the above function signals are exclusive ORed in that only one of them may be present at any given time.

The motor control unit **66** illustrated in FIG. **7C** and consisting of gating and drive circuitry **199** will receive the function signals **114, 114', 114'', 114'''** from the compare unit **98** and gate them with bias signals from the sensing circuitry **122.** The result being that the direct bias signals on lines **156, 156', 156'', 156'''**, and combination bias signals on lines **162, 162', 162'', 162'''** will indicate which phases of the four phase stepping motor **16** are available for performing the desired function at that point in time. The gating and drive circuitry **199** will allow only those phase windings having a concurrence of bias and function signals to be energized. Specifically, the gating and drive circuitry **199** is subdivided into four identical sets of NAND gates and drive units **198, 198', 198'', 198'''**, corresponding to the first, second, third and fourth phases respectively of the motor. Each of the sets of gates and drive units **198,**

198', 198'', 198''', in turn, is provided with four identical NAND gates ORed together and corresponding to the four possible function signals outputted by the compare unit 98, namely, "run", "stop", "full brake" and "step brake". Each of the NAND gates of a set, if it is to output, must have a function signal from the compare unit 98 and a biasing signal from the sensing circuit 122. Thus, if the function desired is "run" or "full-brake", then two different direct biasing signals on line 156, 156', 156'', or 156''' must be gated with the run or full-brake signal on lines 114' or 114''' respectively in two different sets consisting of 198, 198',198'' or 198''' because the stepping motor 16 is designed to run or full-brake in a two phase mode. Additionally, the run signal on line 114', must be gated with a signal on line 62 indicating the presence of an instruction in order for the gate to be enabled. Likewise, if the function desired is step brake or stop, then one combination biasing signal on lines 162, 162', 162'', or 162''' from the flip flops 152 must be gated with the step-brake or stop signals on lines 114'' or 114 respectively in one of the sets consisting of 198, 198', 198'' or 198''' because the stepping motor 16 may only step-brake or stop in a one phase mode. Once a function NAND gate in a set has been activated, in a set consisting of 198, 198', 198'' or 198''', it will output a control signal on line 200, 200', 200'' or 200''' to its associated drive unit consisting of 202, 202', 202'', or 202''' respectively for that phase depending on the phase it is in. A drive unit consisting of 202, 202', 202'' or 202''' upon being switched on by such a control signal on line 200, 200', 200'' or 200''' will energize an associated winding of the stepping motor 16 through line 204, 204', 204'', or 204''' respectively to perform the desired function, be it run, stop, full brake or step brake.

A skip control unit 65 also shown in FIG. 4 is provided to enable slewing or skipping of the web paper in the absence of a field or line instruction code from the central processor along the line 61. A push button switch 63 coupled to the skip control unit 65 is manually operable to activate the stepping motor 16 along the line 62, an input being coincidentally transmitted along the line 96 to the NAND gates 118 and the step counter 100 to thereby reset the step counter and to initialize the circuitry 172 thereof. This manually initiated slewing will terminate when an enabling input signal is transmitted to the NAND gates 118 along the line 116, as generated by the forms index disk 37 upon arrival of the gear stack 30 at its home position, a stop pulse being thus passes and ORed to the motor stop and detent control 114. The NAND gates 118 also serve to activate the motor stop and detent control 114 in the normal execution of a Skip to Heading instruction (binary code 1010 stored in the line instruction portion of the register 64), the line decoder 90 in such instance transmitting an input along the line 120 to the NAND gates 118, such gate being enabled upon receipt of an input along the line 116 upon arrival of gear stack 30 in its home position, it being apparent that the home positions of the gear stack 30 and the forms index 37 would represent the heading of the succeeding form.

Operation

A full understanding of the operation of the inventive format control system is hereinafter conveyed with reference to FIG. 4, an initial phase of such explanation being of a generalized nature not involving the use of specific skip and line instruction codes, and a subsequent phase thereof describing how representative instruction codes would be utilized to effectuate printing on specified print lines.

It is to be noted before proceeding with this explanation that the field mark counter 76 is reset only at the beginning of each unit of selected form length, when the forms index disk 37 transmits a pulse thereto along the line 75, and that the step counter 100 is reset at the beginning of each one-half inch increment of paper advancement, when the field mark disk 26 transmits a pulse thereto along the line 102. It is accordingly also to be noted that the field mark counter 76 will accumulatively count a pulse from the disk 26 for the passage of each ½ inch vertical printing area on the selected form length, and that the step counter 100, when enabled by the flip flop 168, will count up to 60 one one-hundred-twentieths inch increments of paper advancement between said ½ inch printing areas.

Upon setting the dials 36 and 41 (FIG. 1) to select a desired form length (between 8½ inches and 17 inches in the preferred embodiment), a pulse is generated by the home positioned form index disk 37 to thereby reset the field mark counter 76, and to transmit an input pulse along the line 116 to the NAND gates 118, the step counter 100 having already been reset by the preceding pulse from the field mark disk 36. Upon receipt of a field instruction code (other than 00000) in the five-digit field instruction portion of the register 64, along the line 61, (and with a 0000 code in the line instruction portion of the register) the motor 16 is activated to rotate the motor step disk 18 and the paper advance shaft 12, rotation of the shaft 12 being effective also for rotating the field mark disk 26 and the forms index disk 37. As the field mark disk 26 rotates, the pulses generated by the radial slots therein will be counted by the field mark counter 76, each pulse representing and identifying a one-half inch increment of paper advancement. It is to be noted that during this advancement of the web paper, and counting of the field mark pulses by the counter 76, the pulses generated by the motor step disk 18 will not be counted by the step counter 100, since the flip flop 168 (FIG. 7A), which was de-enabled by the new instruction signal on line 61, has not again been enabled by an input from the field compare unit 7Q along the line 82. When the accumulated count in the field mark counter 76 is equal to the five-digit field instruction code in the register 64, the field compare unit 70 will transmit an input pulse along the line 80 to the NAND gates 84, such gate also having an input from the compare unit 98 along the line 110, by reason of the 0-equals state of the step counter 100. Upon thus enabling the NAND gates 84, a stop pulse is transmitted and ORed to the motor stop and detent control 114 of the motor control 66, the motor being accordingly stopped for printing a line of information on the print line represented by the field instruction code stored in the register 64.

In the event printing is to occur in the first half inch of the selected form length, a line instruction code other than 0000 would be transmitted along the line 61 to the line instruction portion of the register 64 (with a 00000 in the field instruction portion of the register), whereupon the line decoder 90 would serve to activate the selected line 92 corresponding to such line instruction code, the encoder 94 thereupon computing the number of motor steps of one one-hundred-twentieth inch each that are required to provide the desired line

spacing, the value computed being entered in the step counter **100.** Upon rotational activation of the motor **16,** the motor step pulses generated by the disk **18** and the photo cells **22** would be transmitted along the lines **101** and **101'** through the sensing circuit **122,** along the line **170,** if it is ascertained that a correct step has been made, to the step counter **100,** the flip flop **168** having been enabled by an input along the line **82** from the field compare unit **70** by reason of the 0-equals state of the field mark counter **76** and the field instruction portion of the register **64.** When the count of the step counter **100** is equal to zero (or binary code 101010) representing the home position of the stepping motor **16,** compare unit **98** would transmit an input stop pulse along the line **110** through the NAND gates **84** to the motor step and detent control **114,** the NAND gates **84** being enabled by the presence of an input along line **80** from the field compare unit **70,** also by reason of the 0-equals state of the field mark counter **76** and the field instruction portion of the register **64.** Upon activation of the motor stop and detent control **114,** the motor **16** would be stopped for the printing of the line of information on a print line corresponding to the line instruction code.

To effectuate printing beyond the first half inch of space on a selected form length, and on a print line not corresponding to a one-half inch increment of paper advancement, a field instruction code (other than 00000) and line instruction code (other than 0000) would be transmitted along the line **61** to the register **64,** the field instruction code being initially operative to advance the paper to the print line corresponding to the one-half inch increment next preceding the desired print line, and the line instruction code being thereafter effective, without stopping the motor, to advance the paper from such preceding ½ inch increment line to the desired print line. Upon receipt of the spacing codes in the register **64,** the line decoder **90** would be responsive to the line instruction code to activate a selected line **92** to the encoder **94,** the encoder **94** thereupon computing the number of 1/120 inch motor steps required to advance the paper from the ½ inch increment line corresponding to the entered field instruction code to the desired print line, such value being entered in the step counter **100.** At the outset of motor activation, the step counter **100** would be in a reset state by reason of the preceding pulse generated by the field mark disk **26,** and the field mark counter **76** would contain an accumulated count corresponding to the recorded one-half inch increments of previous paper advancement. Since the field instruction code stored in the five-digit field instruction portion of the register **64** would be of higher value than the accumulated count in the field mark counter **76,** the flip flop **168** would not initially be provided with an input along the lines **80** and **82** from the field compare unit **70,** and the motor step pulses generated by the disk **18** would initially be blocked from the step counter **100.** It can thus be seen that during the early stage of motor activation, only the pulses generated by the field mark disk **26** would be counted (by the field mark counter **76**), an enabling pulse being transmitted by the field compare unit **70** along the line **82** to the flip flop **168** when an equals state is detected therein, the flip flop **168** being thus enabled to pass the subsequently generated pulses representative of those generated from the motor step disk **18** to the step counter **100** where they would then be counted. When the count of the motor step pulses equals zero (or binary code 101010), to represent the arrival of the desired print line, the compare unit **98** would transmit a pulse along the line **110** through the NAND gates **84** to the motor stop and detent control **114,** the NAND gates **84** having also been enabled by the previously mentioned pulse from the field compare unit **70,** along line **80.** The motor would accordingly be stopped at the desired print line for the printing of a line of information.

The following explanation is set forth to illustrate how various field instruction codes and line instruction codes would be utilized in the inventive tapeless format control system to effectuate printing on desired print lines on a selected form length. With the form select dial **41** set on the 14 inch mark as shown in FIG. **5,** printing on various lines on a 14 inch form may be explained with reference to FIGS. **4** and **6.** If after setting the dial **41** on the 14 inch mark, it is then desired to print a first line of information on the 5 inch line of the form, the field instruction code 01010 would be entered in the five-digit field instruction portion of the register **64,** and the code 0000 entered in the line instruction portion of the register. During the resultant activation of the motor **16,** the field instruction portion of the register being greater than the count in the field mark counter **76,** the flip flop **168** would not be enabled by an input along the line **82** to permit the step counter **100** to count the motor step pulses generated by the disk **18,** paper advancement continuing until the count in the field mark counter **76** is equal to the field instruction code (in this case both equaling **10**), whereupon the field compare unit **70** would transmit a stop pulse along the line **80** through the NAND gates **84** to the motor control unit **66,** the NAND gates **84** being enabled by an input from the compare unit **98** along the line **110** by reason of the zero (or binary code 101010) state of the step counter **100.** Paper advancement would accordingly terminate with the 5 inch line of the form in printing position.

If after printing the line of information on the 5 inch line, it were then desired to print four lines of information in **S10** spacing immediately following the 5 inch line, the codes 01010 and 0001 would be entered in the field instruction and line instruction portions, respectively, of the register **64** for each of the desired four lines of printing. With the 0001 code in the line instruction portion of the register **64,** the line decoder **90** would activate the **S10** line **92** to the encoder **94,** whereupon the encoder **94** would compute and transmit to step counter **100** a unique value for each of the four lines of printing, such values, representing the separately accumulated number of 1/120 inch motor steps required to produce each of the four lines of **S10** spacing, being **12** steps for each line in this case. With the field mark counter **76** and the field instruction portion of the register **64** both being in a 10-equals state, the flip flop **168** would be enabled for each line of printing by an input from the field compare unit **70** along the lines **80** and **82,** to thereby enable the passage of the motor step pulses from the disk **18** through the sensing circuit **122,** assuming correct steps have been made, to the step counter **100.** Upon the counting of **12** motor step pulses for each of the four respective lines of printing, the compare unit **98** would transmit a pulse along the line **110** through the NAND gates **84** to the motor stop and detent control **114,** the NAND gates **84** also

having been enabled by the previously mentioned pulse from the field compare unit **70**.

If after printing the four lines of information in **S10** spacing immediately following the 5 inch line, it were then desired to print two lines of information in **D10** spacing immediately following the 7 inch line on the form, the codes 01110 and 0100 would be entered in the field instruction and line instruction portions, respectively, of the register **64** for each of the desired two lines of printing, entry of the 01110 code for the first line of printing creating an unequal state between the field mark counter **76** and the field instruction portion of the register, and entry of the code 0100 for each of the two lines causing the line decoder **90** to activate the D10 line **92** to the encoder **94**, the encoder **94** thereupon computing and entering in the step counter **100** a value of **24** for the first line of printing and a value of **24** for the second line, such values representing the separately accumulated number of motor steps required to produce each of the two lines of printing. In view of the unequal state of the field mark counter **76** and the field instruction portion of the register **64** during spacing for the first line, the motor step pulses from the disk **18** would initially be blocked from the step counter **100** by the flip flop **168** and four pulses generated by the field mark disk **26** would be counted by the field mark counter **76** (corresponding to the 5½ inch, **6** inch, 6½ inch and 7 inch lines on the form). Upon the occurrence of a 14-equals state of the field mark counter **76** and the field instruction portion of the register **64** a pulse would be transmitted from the field compare unit **70** along the line **80** to the NAND gates **84**, and along the line **82** to the flip flop **168**, the NAND gates **84** not being enabled by an input from the compare unit **98** due to the non-zero state of the step counter **100**, the flip flop **168**, however, being enabled by such pulse to permit the passage of motor step pulses from the disk **18** through the sensing circuit **122**, assuming correct steps have been made, to the step counter **100**. Upon the counting of **24** motor step pulses by the counter **100**, the compare unit **98** would transmit a stop pulse along the line **110** through the NAND gates **84** to the motor stop and detent control **114**, the NAND gates **84** being enabled by the previously mentioned input from the field compare unit **70**. Advancement of the paper would accordingly be terminated for the printing of the first line of information following the 7 inch line. The codes 01110 and 0100 would then be entered in the field instruction and line instruction portions, respectively, of the register **64** for the printing of the second line of information in **D10** spacing, an enabling pulse from the field compare unit **70** being immediately transmitted to the NAND gates **84** and flip flop **168**, by reason of the 14-equals state of the field mark counter and the field instruction portion of the register **64**, the motor step pulses from the disk **18** being accordingly passed through the sensing circuit **122**, then to the flip flop **168**, assuming a correct step has been made, and finally inputted to and counted by the step counter **100**. Upon the occurrence of a zero-equals state in the step counter **100** representing **24** steps completed, the compare unit **98** would transmit a stop pulse along the line **110** through the enabled NAND gates **84** to the motor stop and detent control **114**, to thereby terminate paper advancement for the printing of the second line of information in **D10** spacing.

If after printing the two lines of information in **D10** spacing immediately following the 7 inch line on the form, it were then desired to print two lines of information in **S8** spacing immediately following the 8 inch line, the coes 10000 and 0010 would be entered in the field instruction and line instruction portions, respectively, of the register **64** for each of the two lines of printing, spacing for the first line of printing involving the initial counting of two pulses from the field mark disk **26** by the counter **76** (corresponding to the 7½inch and 3 inch lines), and the subsequent counting of **15** motor step pulses from the disk **18** by the step counter **100** (to create a zero-equals state in the step counter **100** representing 15 steps completed), when a 16-equals state occurs in the field mark counter **76** and the field instruction portion of the reegister **64**, as previously described. Upon entering the codes 10000 and 0010 for the second lines of **S8** printing, the flip flop **168** would be enabled immediately by an input along the line **82** resulting from the 16-equals state of the field mark counter **76** and the field instruction portion of the register **64**, the step counter **100** proceeding to count the motor step pulses from the disk **18**. Upon the counting of **15** additional motor step pulses by the counter **100** therein (such being the value computed by the encoder **94** and stored in the step counter **100** upon entry of the code 0010 for the second line of printing), a pulse would be transmitted from the compare unit **98** along the line **110** through the enabled NAND gates **84** to the motor stop and detent control **114**, to thereby terminate paper advancement for the printing of the second line of information in **S8** spacing.

If after printing the two lines of information in **S8** spacing immediately following the **8** inch line on the form, it were then desired to print one line of information on the 13 inch line and one line of information in **T6** spacing immediately following the 13 inch line, the codes 11010 and 0000 would be entered in the field instruction and line instruction portions, respectively, of the register **64** for printing on the 13 inch line, and the codes 11010 and 1001 would be entered in the respective portions of the register **64** for the printing of the second line in **T6** spacing. Entry of the 11010 and 0000 codes would result immediately in the transmission of an input pulse from the compare unit **98** to the NAND gates **84**, by reason of the 0-equals state of the step counter **100**, the field mark counter **76** proceeding to count 10 pulses from the field mark disk **26** (corresponding to the 8½ inches, 9 inches, 9½ inches, 10 inches, 10½ inches, 11 inches, 11½ inches, 12 inches, 12½ inches and 13 inches lines on the form), and the field compare unit **70** serving to transmit a pulse to the NAND gates **84** upon the occurrence of a 26-equals state in the field mark counter **76** and the field instruction portion of the register **64**, the NAND gates **84** being thereby enabled to pass a pulse to the motor stop and detent control **114** to terminate paper advancement for the printing of the line of information on the 13 inches line of the form. Upon the entry of the 11010 and 1001 codes in the respective portions of the register **64**, for the printing of the second line of information in **T6** spacing, the flip flop **168** would immediately receive an input along the line **82** from the field compare unit **70**, due to the 26-equals state of the field mark counter **76** and the field instruction portion of the register **64**, the step counter **100** being thereby rendered enabled to count the motor step pulses from the disk

18. Upon the counting of 60 motor step pulses by the counter 100, such being the value computed by the encoder 94 and entered in the step counter 100 upon activation of the T6 line 92 by the line decoder 90, a stop pulse would be generated by the compare unit 98 and transmitted along the line 110 through the enabled NAND gates 84 to the motor stop and detent control 114, to thereby terminate paper advancement for the printing of the second line in T6 spacing.

While a preferred embodiment of the tapeless format control system has been described herein in considerable detail, it will be appreciated that various modifications and alterations therein may be conceived by persons skilled in the art without departing from the true spirit and scope of the invention.

What is claimed is:

1. A tapeless format control apparatus for use in a line printer for printing on web paper, said printer having web paper handling and positioning means associated with a printing position thereof, said apparatus comprising:

a. a stepping motor for operatively advancing said web paper relative to said printing position, said motor being coupled to said web paper handling and positioning means,

b. motor control means associated with said stepping motor and effective for stopping and detenting said stepping motor,

c. means for selectively determining the length of the web paper upon which lines of information are to be printed, such selected web paper length constituting a selected form length,

d. means for receiving and storing externally originated print spacing instructions,

e. a plurality of pulse generating means effective for identifying each increment of rotational motion of said stepping motor according to a gray coded scheme, each increment of advancement of said web paper, and the passage of each unit of selected form length, and

f. means cooperating with said motor control means and responsive to said print spacing instructions for controllably coordinating said plurality of identifying pulses such that each line of information printed on said selected form length is properly spaced from the preceding line and all of the lines of printed information conform to a preselected format represented by said externally originated print spacing instructions wherein said controllably coordinating means includes:

sensing means responsive to said pulse generating means effective for identifying each increment of rotational motion of said stepping motor and cooperating with said motor control means for allowing said stepping motor to increment only upon ascertaining that its preceding increment was properly executed, and

first comparator means responsive to said print spacing instructions and interacting with said motor control means for controllably retarding the speed of said stepping motor as a print line on said web paper corresponding to said print spacing instructions approaches said printing position.

2. The format control apparatus defined in claim 1 wherein said selective form length determining means comprises:

a. a plurality of gears of varying diameters fixed to a rotatable first shaft in coaxial relationship to form a conical gear stack, each of said gears of said stack representing a different form length,

b. an elongated cylindrical gear coupled to said web paper handling and positioning means of said line printer, and

c. adjustable means for coupling said elongated cylindrical gear with a selected one of said plurality of gears forming said conical gear stack.

3. The format control apparatus defined in claim 2 wherein said adjustable coupling means comprises:

a. a translatably supported toothed rack disposed intermediate and in parallel relationship relative to said elongated cylindrical gear and said conical gear stack,

b. an idling coupling gear rotatably mounted on the innermost extremity of said toothed rack, said coupling gear being engageably disposed relative to said elongated gear and individual ones of said gears forming said conical gear stack, and

c. means responsive to manual manipulation for selectively translating said rack and said coupling gear relative to said elongated gear so as to cooperably couple a selected gear of said conical gear stack with said elongated gear.

4. The format control apparatus defined in claim 3 wherein said means for selectively translating said rack and said coupling gear comprises:

a. a pinion gear rotatably mounted on a rotatably second shaft in engaged relationship with the teeth of said toothed rack,

b. a third shaft gearably coupled to said second shaft, and

c. a manually manipulatable dial member fixed to said third shaft at the end thereof opposite the end gearably coupled to said second shaft.

5. The format control apparatus defined in claim 1 wherein said means for receiving and storing said print spacing instructions comprises: a shift register having a field skip portion for temporarily storing a binary decimal code indicative of the number of increments of web paper advancement that are required in an initial skipping phase thereof, and a line advance portion for storing a binary decimal code indicative of the number of increments of rotational motion of the stepping motor that are required in a line advance phase of said web paper advancement.

6. The format control apparatus defined in claim 5 wherein said pulse generating means effective for identifying each increment of advancement of said web paper during said initial skipping phase thereof comprises:

a. a first multi-slotted disk coupled to said web paper handling and positioning means in contiguous relationship with said elongated cylindrical gear, and

b. a first sensing device comprised of a light emitting member and a light sensitive switch, said device being coupled to said pulse coordinating means and disposed in cooperating relationship with said first disk.

7. The format control apparatus defined in claim 6 wherein said pulse generating means effective for identifying each increment of rotational motion of said stepping motor according to said gray coded scheme comprises:

a. a second disk of two rings of multi-slots coupled to a motor shaft of said stepping motor, and

b. a second sensing device comprised of at least two light emitting members and at least two light sensitive switches in parallel, said device being coupled to said pulse coordinating means and disposed in cooperating relationship with said second disk.

8. The format control apparatus defined in claim **7** wherein said pulse generating means effective for identifying the passage of each unit of selected form length comprises:

a. a third slotted disk coupled to said first shaft at an extremity thereof adjacent said conical gear stack, and

a third sensing device comprised of a light emitting member and a light sensitive switch, said device being coupled to said pulse coordinating means and disposed in cooperating relationship with said third disk.

9. The format control apparatus defined in claim **6** wherein said disk is provided with sixteen radially disposed and equally spaced-apart slots, the movement of each slot into cooperating relationship with said first sensing device representing a one-half inch increment of web paper advancement.

10. The format control apparatus defined in claim **7** wherein said second disk is provided with **24** radially disposed and equally spaced-apart coded positions per ring in gray code and said second sensing device is provided with two parallelly arranged light emitting members and light sensitive switches, the movement of each of said coded positions into cooperating relationship with each of said light emitting members and light sensitive switches representing a 15° angular displacement of said stepping motor as translated into a 1/120 inch increments of web paper advancement.

11. The format control apparatus defined in claim **8** wherein said third disk is provided with a single radially disposed slot the movement thereof into cooperating relationship with said third sensing device representing the passage of each unit of selected form length as delineated by said adjustable means of said selective form length determining means.

12. The format control apparatus defined in claim **8** wherein said means for controllably coordinating said plurality of identifying pulses comprises:

a. first counter means associated with said first and third slotted disks and with said first and second sensing devices,

b. second comparator means operatively coupled to said first counter means and to said field skip portion of said register,

c. value determining means associated with and coupled to said line advance portion of said register,

d. second counter means associated with said first slotted disk, said first sensing device, said sensing means, and said value determining means, and

e. first gating means coupled to said first and said second comparator means and effective for outputting a pulse to said motor control means to thereby stop said stepping motor when both said comparator means output a pulse concurrently.

13. The format control apparatus defined in claim **12** wherein said first counter means is resettably responsive to pulses generated by said third slotted disk and said third sensing device, and advanceably responsive to pulses generated by said first slotted disk and said first sensing device.

14. The format control apparatus defined in claim **12** wherein said second counter means is resettably responsive to pulses generated by said first slotted disk and said first sensing device and advanceably responsive in a count down sequence to pulses generated by said sensing means after having been initialized by a pulse from said value determining means, said count down sequence starting at a selected initialization point and reduceably advancing from said selected point to zero.

15. The format control apparatus defined in claim **14** wherein said second counter means is provided with initializing means respnsive to said value determining means and effective for setting said second counter means upon the concurrent receipt of pulses from said sensing means and from said second comparator means.

16. The format control apparatus defined in claim **14** wherein said sensing means comprises:

a. sensor gating means coupled to said second sensing device and effective for decoding gray coded signals received therefrom,

b. sensor storage means responsive to initialization by said sensor gating means and effective for storing a pulse representative of the preceding increment of advancement of said stepping motor,

c. sensor compare means coupled to said sensor gating means and said sensor storage means and effective for outputting a pulse whenever the gray coded signal received by said sensor gating means and representing the present step is the next correct step when compared with the preceding step as indicated by said sensor storage means, and

d. pulse triggering means biased by said sensor compare means and effective upon receipt of a pulse therefrom for triggering said sensor storage means, said second counter means and said first comparator means.

17. The format control system defined by claim **16** wherein said sensor gating means and said sensor compare means are NAND gates.

18. The format control system defined by claim **16** wherein said sensor storage means and said pulse triggering means are gated flip flops.

19. The format control apparatus defined in claim **12** wherein said value determining means comprises:

a. a decoder coupled to said line advance portion of said register and effective for decoding a binary coded signal stored therein to thereby activate a selected one of a plurality of output channels corresponding to said binary coded signal, said binary coded signal being representative of a predetermined line advance instruction, and

b. an encoder coupled to said decoder by means of said plurality of output channels and coupled also to said second counter means, said encoder being effective for computing a value representative of the number of incremental motor steps required to execute said predetermined line advance instruction and to initialize said value in said second counter means upon the receipt of concurrent signals from said first comparator means and from said sensing means.

20. The format control apparatus defined in claim **19** wherein said first comparator means comprises:

a. second gating means coupled to receive signals from said second counter means and effective for outputting a plurality of unique signals to said motor control means to thereby initiate or terminate stepping motor incrementing,

b. third gating means coupled to receive signals from said second counter means and effective for outputting a signal when said second counter means has reached a predetermined point in its down-counting to zero,

c. latching means coupled to said third gating means and effective for outputting a signal upon receipt of a signal therefrom, and

d. braking means coupled to said latching means and to said sensing means and effective upon receiving concurrent signals therefrom to output fixed and variable period signals to said motor control means to thereby enable braking and reduced speed powering of the stepping motor, respectively.

21. The format control system defined in claim **20** wherein said second gating means and said third gating means are NAND gates.

22. The format control system defined in claim **20** wherein said latching means is a flip flop.

23. The format control system defined in claim **20** wherein said braking means is a gated delayed multivibrator.

24. The format control apparatus defined in claim **20** wherein said motor control means comprises sets of gating circuits equal in number to the number of phases of said stepping motor, each of said sets being comprised of a plurality of gates according to the number of functions that are to be performed by said stepping motor, the outputs of said gating sets being ORed together to output a control pulse upon the concurrent receipt of input pulses from said first comparator means and said sensing means, said output pulses serving to activate corresponding motor drive means to thereby energize the desired phase windings of said stepping motor.

25. The format control system defined in claim **24** wherein said function gates are NAND gates.

26. The format control apparatus defined in claim **19** wherein said means for controllably coordinating said plurality of identifying pulses additionally comprises: fourth gating means coupled to said third sensing device and to said decoder by means of a predetermined one of said output channels thereof, said fourth gating means being coupled also to a manually operable skip control unit effective for advancing said web paper in the absence of a binary coded signal in either said field skip or line advance portions of said register, the enabling of said fourth gating means by a pulse generated by said third slotted disk and said third sensing device and a pulse from either said skip control unit or said decoder being effective to output a signal to said motor control means to thereby terminate said incremented movement of said stepping motor.

27. The format control apparatus defined in claim **26** wherein said fourth gating means is comprised of NAND gates.

28. In a web medium control system for use in a line printer having a stepping motor and associated web medium advancing means, said control system including a shift register for storing field skip and line advance spacing instructions and a plurality of pulse generating means including first means for outputting a signal when a predetermined length of the web medium has been advanced by said advancing means, said predetermined length representing a selected form length, second means for outputting a signal upon sensing each increment of web medium advancement according to said stored field skip spacing instruction, and third means for outputting a signal upon sensing each increment of rotational motion of said stepping motor according to said stored line advance spacing instruction, improved means for controllably coordinating and checking said plurality of pulse generating means such that each line of information printed on each predetermined form length is properly spaced from the preceding line and all of the lines of printed information conform to a preselected format represented by said print spacing instructions, said improved coordinating and checking means comprising:

a. a sensing circuit responsive to said third pulse generating means and cooperating with said stepping motor to permit incrementing thereof only upon ascertaining that the preceding increment was properly effectuated, and

b. a first comparator activated by said print spacing instructions so as to interact with said stepping motor to controllably retard the speed thereof as a print line on said web medium corresponding to said instructions approaches a printing position of said line printer.

29. The improved means for controllably coordinating and checking said plurality of pulse generating means defined in claim **28** and additionally comprising:

a. a first counter associated with said first and said second pulse generating means,

b. a second comparator operatively coupled to said first counter and to a portion of said shift register effective for storing said field skip spacing instruction,

c. value determining means associated with and coupled to a portion of said shift register effective for storing said line advance spacing instruction,

d. a second counter associated with said second and said third pulse generating means, with said value determining means, and with said sensing circuit and said first comparator, and

e. first gating means coupled to said first ad said second comparators and effective for outputting a signal to said stepping motor to thereby stop said motor when an equals state is detected in said first and said second comparators.

30. The improved coordinating means defined in claim **29** wherein said first counter is resettably responsive to pulses generated by said first pulse generating means, and advanceably responsive to pulses generated by said second pulse generating means.

31. The improved coordinating means defined in claim **29** wherein said second counter is resettably responsive to pulses generated by said second pulse generating means and advanceably responsive to pulses generated by said sensing circuit after having been initialized by a pulse from said value determining means to thereby count down from a selected initialization point to zero.

32. The improved coordiating means defined in claim **29** wherein said second counter further includes an intialization circuit responsive to said value determining means to set said second counter upon simultaneous

receipt of pulses from said sensing circuit and said second comparator.

33. The improved coordinating means defined in claim **29** wherein said value determining means comprises:

a. a decoder coupled to said line advance portion of said register and effective for decoding a binary coded signal stored therein to thereby activate a selected one of a plurality of output channels corresponding to said binary coded signal, said binary coded signal being representative of a predetermined line advance spacing instruction, and

b. an encoder coupled to said decoder by means of said plurality of output channels and coupled also to said second counter, said encoder being effective for computing a value representative of the number of incremental motor steps required to execute said predetermined line advance instruction and to enter said value in said second counter.

34. The improved coordinating means defined in claim **29** wherein said sensing circuit additionally comprises:

a. a sensor gating unit coupled to said third pulse generating means and effective for decoding signals received therefrom, said signals being coded in incremental steps according to a gray coded scheme,

b. storage means coupled to said sensor gating unit and effective for indicating the preceding increment position of said stepping motor,

c. a sensor compare unit coupled to said sensor gating unit and to said storage means and effective for outputting a pulse whenever the incremental step indicated by said sensor gating unit is one step forward of the incremental position indicated by said storage means, and

d. triggering means coupled to receive pulses from said sensor compare unit and effective for clock pulsing said storage means, said second counter and said first comparator.

35. The improved coordinating means defined in claim **34** wherein said sensor gating unit and said sensor compare unit are NAND gates.

36. The improved coordinating means defined in claim **34** wherein said storage means and said triggering means are gated flip flops.

37. The improved coordinating means defined in claim **29** wherein said first comparator additionally comprises:

a. second gating means coupled to receive signals from said second counter and effective for outputting unique signals to said stepping motor when said second counter has or has not counted down from its initialization point to zero, to thereby prevent or enable incrementing of the stepping motor, respectively,

b. third gating means coupled to receive signals from said second counter and effective for outputting a signal when said second counter has counted down to within a fixed number of steps from its zero point,

c. bistable means couplled to said third gatingmeans and effective for outputting a signal upon receipt of a signal from said third gating means, and

d. stepping motor braking means coupled to said bistable means, to said sensing circuit and to said stepping motor and effective upon receiving concurrent signals from said bistable means and said sensing circuit to output fixed and variable period signals to said stepping motor for retarding the speed thereof and for alternately powering and braking said stepping motor.

38. The improved coordinating means defined in claim **37** wherein said second gating means and said third gating means are NAND gates.

39. The improved coordinating means defined in claim **37** wherein said bistable means is a flip flop.

40. The improved coordinating means defined in claim **37** wherein said stepping motor braking means is a gated delayed multivibrator.

41. The improved means for controllably coordinating and checking said plurality of pulse generating means defined in claim **37** and additionally comprising: fourth gating means coupled to said first pulse generating means, to said decoder, and to a manually operable skip control unit effective for advancing said web medium in the absence of a print spacing instruction stored in said shift register, the enabling of said fourth gating means by a pulse generated by said first pulse generating means a pulse from either said skip control unit or from said decoder being effective to output a signal to said stepping motor to thereby terminate the incrementing thereof.

42. The improved coordinating means defined in claim **41** wherein said fourth gating means are NAND gates.

* * * * *

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,857,471 Dated December 31, 1974

Inventor(s) Paul R. Hoffman and Roger S. Naeyaert

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 10, line 15, change "counter 10" to read --counter 100--.
Col. 14, line 26, change "disk 36" to read --disk 26--.
Col. 18, line 11, change "3" lines" to read --8" lines--.
Col. 24, line 46, change "add said" to read --and said--.

Signed and sealed this 11th day of March 1975.

(SEAL)
Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents
and Trademarks