Title: ANCHORED THROUGH-SILICON VIAS

Abstract: Anchored through-silicon vias (TSVs), and related devices and methods, are disclosed herein. In some embodiments, an anchored TSV may include a first copper portion having a first width; a second copper portion having a second width greater than the first width; and a third copper portion having a third width less than the second width; wherein the second copper portion is disposed between the first copper portion and the third copper portion.

Diagram: FIG. 1A
ANCHORED THROUGH-SILICON VIAS

Technical Field

[0001] The present disclosure relates generally to the field of integrated circuit devices, and more particularly, to anchored through-silicon vias.

Background

[0002] Through-silicon vias (TSVs) are used to provide a conductive pathway between the front and back sides of a silicon substrate. Components on either side of the silicon substrate may use the TSV for electrical communication, or the routing of power and ground signals.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIGS. 1A-B are cross-sectional side views of an anchored through-silicon via (TSV), in accordance with various embodiments.

[0005] FIGS. 2, 3A-3B and 4-15 are cross-sectional side views of assemblies at various stages in the manufacture of an integrated circuit (IC) device including the anchored TSV of FIG. 1, in accordance with various embodiments.

[0006] FIG. 16 is a flow diagram of a method of manufacturing an anchored TSV, in accordance with various embodiments.

[0007] FIGS. 17A-B are top views of a wafer and dies that may include an anchored TSV in accordance with any of the embodiments disclosed herein.

[0008] FIG. 18 is a cross-sectional side view of an IC device that may include an anchored TSV in accordance with any of the embodiments disclosed herein.

[0009] FIG. 19 is a cross-sectional side view of an IC device assembly that may include an anchored TSV in accordance with any of the embodiments disclosed herein.

[0010] FIG. 20 is a block diagram of an example computing device that may include an anchored TSV in accordance with the teachings of the present disclosure.

Detailed Description

[0011] Anchored through-silicon vias (TSVs), and related devices and methods, are disclosed herein. In some embodiments, an anchored TSV may include a first copper portion having a first width; a second copper portion having a second width greater than the first width; and a third copper portion having a third width less than the second width; wherein the second copper portion is disposed between the first copper portion and the third copper portion.
[0012] Relative to conventional TSV technology, the anchored TSVs disclosed herein may exhibit improved reliability and mechanical integrity. In particular, conventional TSVs may fail during stress testing or in the field when the TSV delaminates from its surrounding components (e.g., an oxide liner or inter-layer dielectric). Delamination may occur, for example, when the TSV has a different coefficient of thermal expansion than the surrounding components (e.g., the inter-layer dielectric), causing the TSV to expand or contract to a different degree than the surrounding components as the temperature changes. The crack formed by this delamination may interrupt the conductive pathway of which the TSV is a part, preventing the desired electrical flow.

[0013] Various embodiments of the anchored TSVs disclosed herein may provide a "flare" that anchors the TSVs in the silicon substrate, providing more surface area over which stress (e.g., caused by heat or material mismatches due to contamination) can be distributed, reducing the likelihood of delamination.

[0014] In the following detailed description, reference is made to the accompanying drawings that form a part hereof wherein like numerals designate like parts throughout, and in which are shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0015] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0016] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C).

[0017] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale.
FIGS. 1A-B are cross-sectional side views of an anchored through-silicon via (TSV) 100, in accordance with various embodiments. In particular, FIG. 1B is a detailed view of the indicated portion of FIG. 1A. The TSV 100 may include a first copper portion 102 having a first width 112, a second copper portion 104 having a second width 114, and a third copper portion 106 having a third width 116. The second width 114 may be greater than the first width 112, and the third width 116 may be less than the second width 114. As shown in FIG. 1, the second copper portion 104 may be disposed between the first copper portion 102 and the third copper portion 106. As used herein, the "width" of an element may refer to the largest extent of that element in the indicated direction.

In some embodiments, as illustrated in FIG. 1, the first copper portion 102 may be proximate to the backside 142 of a silicon substrate 138 through which the TSV 100 extends. The third copper portion 106 may be proximate to the front side 140 of the silicon substrate 138, and to a front metal layer 144 disposed at the front side 140 of the silicon substrate 138. The front metal layer 144 may include metal interconnect structures and an inter-layer dielectric (ILD), and may be coupled with transistor devices included in a device layer (not shown). For example, the front metal layer 144 may be the M1 layer discussed below with reference to FIG. 18. The side surfaces 150 of the first copper portion 102 may be substantially parallel, as illustrated, or may be slightly tapered (forming an angle slightly greater or slightly less than 90° with the backside 142 of the silicon substrate 138). When a deep-reactive ion etching (DRIE) process is used in the manufacture of the TSV 100 (e.g., as discussed below with reference to FIGS. 2-4), the side surfaces 150 of the first copper portion 102 may be scalloped with a depth between approximately 100 and 500 nm.

The cross section of the TSV 100 may include a body 108 and two first projections 110 extending away from the body 108. For example, as illustrated in FIG. 1, the first projections 110 may extend laterally away from the body 108, in a direction substantially perpendicular to the side surfaces 150 of the first copper portion 102. The first projections 110 may be included in the second copper portion 104, and may have tips 118, such that the second width 114 of the second copper portion 104 is the distance between the tips 118.

The first projections 110 may have a first surface 120 proximate to the first copper portion 102, and a second surface 122 proximate to the third copper portion 106. The first surface 120 and the second surface 122 may meet at the tip 118. In some embodiments, as illustrated in FIG. 1, the first surface 120 may include a second projection 124 having its own tip 126. Additionally, in some embodiments, the first surface 120 may include a third projection 128 having its own tip 130. In some embodiments, the "height" of the second projection 124 may be greater than the "height" of the third projection 128, as illustrated in FIG. 1. Although the tips 118, 126, and 130 are illustrated as sharp angles, the tips 118, 126, and/or 130 may be rounded. In some embodiments, the first surface 120 may not include a second projection 124 and/or a third projection 128.
[0022] The first surface 120 and/or the second surface 122 may include portions with convex curvature. For example, the portion 132 of the first surface 120, and substantially all of the second surface 122, is illustrated in FIG. 1 as having convex curvature. In some embodiments, the second copper portion 104 may be flared between the first width 112 of the first copper portion 102 and the second width 114 of the second copper portion 104, with the first projections 110 gradually extending away from the side surfaces 150 of the first copper portion 102. Similarly, the second copper portion 104 may be flared between the third width 116 of the third copper portion 106 and the second width 114 of the second copper portion 104 (e.g., rather than the second copper portion 104 forming a sharp angle with the third copper portion 106).

[0023] In some embodiments, the third width 116 may be the same as the first width 112 (e.g., when the over etch process discussed below with reference to FIGS. 2-4 is used to form an opening in the silicon substrate 138 filled at least in part by the TSV 100). In other embodiments, the first width 112 and the third width 116 may be different, but both may be less than the second width 114.

[0024] Suitable dimensions for the TSV 100 may depend on the setting in which the TSV 100 will be used. In some embodiments, the first width 112 may be at least 4 \( \mu \text{m} \) (e.g., between 4 \( \mu \text{m} \) and 8 \( \mu \text{m} \)). For example, the first width 112 may be 6-7 \( \mu \text{m} \). In some embodiments, the third width 116 may be at least 4 \( \mu \text{m} \) (e.g., between 4 \( \mu \text{m} \) and 8 \( \mu \text{m} \)). For example, the third width 116 may be 6-7 \( \mu \text{m} \). In some embodiments, the second width 114 may be at least 3 \( \mu \text{m} \) greater than the first width 112 and/or the third width 116, or at least 4 \( \mu \text{m} \) greater than the first width 112 and/or the third width 116. For example, the second width 114 may be 4-5 \( \mu \text{m} \) greater than the first width 112 and/or the third width 116 (e.g., when each of the first projections 110 has its own "width" that is 2-2.5 \( \mu \text{m} \)). Thus, the second width 114, in some embodiments, may be at least 7 \( \mu \text{m} \) (e.g., between 7 and 13 \( \mu \text{m} \), or between 9 and 11 \( \mu \text{m} \)). The height 136 of the TSV 100 (measured between the backside 142 and the front side 140 of the silicon substrate 138) may depend on the thickness of the silicon substrate 138; in some embodiments, the height 136 may be at least 50 \( \mu \text{m} \), or at least 100 \( \mu \text{m} \). For example, the height 136 may be 80-120 \( \mu \text{m} \).

[0025] In FIG. 1, a layer of titanium 148 is illustrated as contacting the side surfaces 135 and the bottom surface 134 of the TSV 100, and in particular, as disposed between the bottom surface 134 of the TSV 100 and the front metal layer 144. A layer of silicon oxide 146 is illustrated as contacting the side surfaces 158 of the silicon substrate 138 such that the silicon oxide 146 is disposed between the side surfaces 158 of the silicon substrate 138 and the side surfaces 135 of the TSV 100 (with the titanium 148 at least partially disposed between the silicon oxide 146 and the side surfaces 135 of the TSV 100).
FIGS. 2-15 are cross-sectional side views of assemblies at various stages in the manufacture of an IC device 1800 including the TSV 100 of FIG. 1, in accordance with various embodiments. Although specific operations and assemblies are illustrated in FIGS. 2-15 to illustrate an embodiment of a technique for manufacturing a particular TSV 100, other manufacturing techniques may be used, and other assemblies may be formed, in accordance with the teachings of the present disclosure and as known by one of ordinary skill in the art.

FIG. 2 illustrates an assembly 200 including a silicon substrate 138 having a front metal layer 144 disposed at the front side 140 of the silicon substrate 138. A nitride layer 152, patterned by a hardmask 154, may be disposed at the backside 142 of the silicon substrate 138.

FIGS. 3A and 3B illustrate an assembly 300 subsequent to performing a DRIE process in the silicon substrate 138 of the assembly 200 (FIG. 2) to form an opening 156 between the backside 142 of the silicon substrate 138 and the front metal layer 144 disposed at the front side 140 of the silicon substrate 138. As known in the art, a DRIE process (also referred to as a Bosch process, or time-multiplexed etching) may include multiple iterations of two stages: etching the silicon substrate 138 with sulfur hexafluoride (SF6) plasma and coating the exposed surface with a passivation layer using an octafluorocyclobutane (C8F8) source gas. Fluorine ions in the SF6 plasma may etch the passivation layer at the bottom of the opening before fluorine radicals commence a generally isotropic etch; after a short etch period, the passivation layer is replaced, and the cycle begins again. Any suitable number of iterations (e.g., 100 or more) may be performed to achieve an opening 156 with the desired geometries. As known in the art (and as illustrated in FIG. 3B), the side surfaces 158 of the opening 156 may be scalloped, with the scallops having a depth 160 typically in the range of 100-500 nm. The depth 160, spacing, and other aspects of the geometry of the scalloped side surfaces 158 may be controlled by varying the parameters of the DRIE process, as known in the art. As discussed above with reference to FIG. 1, in some embodiments, the side surfaces 158 of the opening 156 may be substantially parallel, while in other embodiments, the opening 156 may have a slight taper.

FIG. 4 illustrates an assembly 400 subsequent to continuing the DRIE process upon reaching the front metal layer 144 of the assembly 300 (FIG. 3) to "over etch" the opening 156 such that the cross section of the opening 156 includes lateral recesses 162 in the silicon substrate 138. The lateral recesses 162 may be formed when the DRIE process reaches the front metal layer 144, and the front metal layer 144 is not grounded; fluorine radicals generated during the DRIE process may "bounce" off the front metal layer 144 and continue etching the silicon substrate 138 laterally (rather than being discharged through an electrical pathway, as would occur if the front metal layer 144 were grounded). Conventional approaches to DRIE have attempted to avoid the formation of the lateral recesses 162 during a TSV manufacturing process; however, the anchored TSVs 100 disclosed herein take advantage of this conventional "defect" to improve the mechanical coupling.
between the TSVs 100 and the silicon substrate 138, and thus reduce the mechanical failure rate of TSVs, as discussed in further detail herein. The amount of over etch performed to form the lateral recesses 162 may depend on the geometry and materials of the assembly 300. For example, in some embodiments, 10% over etch may be performed.

[0030] The opening 156 of the assembly 400 may include features substantially complementary to those of the TSV 100 discussed above with reference to FIG. 1. In particular, the opening 156 may include a first portion 172 having a first width 182, a second portion 174 having a second width 184, and a third portion 176 having a third width 186. The second portion 174 may be disposed between the first portion 172 and the third portion 176, and the second width 184 may be greater than the first width 182 and greater than the third width 186. As evident from a comparison between FIGS. 1 and 4, the first portion 172 of the opening 156 may correspond to the first copper portion 102 of the TSV 100, the second portion 172 of the opening 156 may correspond to the second copper portion 104 of the TSV 100, and the third portion 176 of the opening 156 may correspond to the third copper portion 106 of the TSV 100 (as illustrated with reference to FIG. 9 and discussed further below). In particular, the lateral recesses 162 may include first surfaces 188 proximate to the first portion 172 of the opening 156, and second surfaces 190 proximate to the third portion 176 of the opening 156. The first surface 188 may correspond to the first surface 120 of the TSV 100, and the second surface 190 may correspond to the second surface 122 of the TSV 100 (as illustrated with reference to FIG. 9 and discussed further below).

[0031] FIG. 5 illustrates an assembly 500 subsequent to providing a layer of silicon oxide 146 to the surfaces of the opening 156 (e.g., the side surfaces 158 and the bottom surface 164) of the assembly 400 (FIG. 4). In some embodiments, the layer of silicon oxide 146 may cover both the first surfaces 188 and the second surfaces 190 of the lateral recesses 162. The silicon oxide 146 may be provided using a conventional chemical vapor deposition (CVD) process, for example.

[0032] FIG. 6 illustrates an assembly 600 subsequent to removing the silicon oxide 146 at the bottom surface 164 of the opening 156 so that the front metal layer 144 is exposed to the opening 156. The silicon oxide 146 may remain on the side surfaces 158 of the opening 156 (including the first surface 188 and the second surface 190 of the lateral recesses 162). The silicon oxide 146 may be removed to make an opening with the front metal layer 144 using a “break-through etch” process as part of conventional DRIE (e.g., using Ar chemistry).

[0033] FIG. 7 illustrates an assembly 700 subsequent to providing a layer of titanium 148 to the surfaces of the opening 156 of the assembly 600 (FIG. 6). The titanium 148 may provide a surface on which a copper seed layer may adhere, as discussed below with reference to FIG. 8, and thus may substantially “seal” the silicon oxide 146. As discussed above with reference to FIG. 1, the titanium 148 may be in contact with the front metal layer 144 and the silicon oxide 146 may be disposed
between the titanium 148 and the silicon substrate 138. In some embodiments, the titanium 148 may not cover the first surface 188 and/or the second surface 190 of the lateral recesses 162; for example, in some embodiments, the titanium 148 may not reach the first surface 188 and/or may not fully coat the first surface 188. The titanium 148 may be provided using a conventional sputtering process, for example.

[0034] FIG. 8 illustrates an assembly 800 subsequent to providing a copper seed layer 168 to the surfaces of the opening 156 of the assembly 700 (FIG. 7). The copper seed layer 168 may substantially cover the side surfaces 158 and the bottom surface 164 of the opening 156. In some embodiments, the copper seed layer 168 may not cover both the first surface 188 and/or the second surface 190 of the lateral recesses 162; for example, in some embodiments, the copper seed layer 168 may not reach the first surface 188 and/or may not fully coat the first surface 188. The copper seed layer 168 may be provided using a conventional sputtering process, for example.

[0035] FIG. 9 illustrates an assembly 900 subsequent to filling the opening 156 of the assembly 800 (FIG. 8) with copper to form a TSV 100. As discussed above with reference to FIG. 1, the TSV 100 of FIG. 9 may have a first copper portion 102, a second copper portion 104, and a third copper portion 106; the second copper portion 104 may be disposed between the first copper portion 102 and the third copper portion 106, and may have a width greater than the widths of the first copper portion 102 and the third copper portion 106. The opening 156 of the assembly 800 may be filled with copper by electroplating the copper onto the copper seed layer 168. The opening 156 may fill with copper even in embodiments in which no copper seed layer 168 is present on the first surface 188 of the lateral recesses 162.

[0036] FIG. 10 illustrates an assembly 1000 subsequent to performing chemical mechanical polish (CMP) proximate to the backside 142 of the silicon substrate 138 of the assembly 900 (FIG. 9) to remove the hardmask 154 and some of the nitride 152 (e.g., leaving a layer of nitride 152 approximately 2 μm thick), and to form a flat backside surface 192 of the TSV 100.

[0037] FIG. 11 illustrates an assembly 1100 subsequent to providing a patterned photoresist 194 at the backside 142 of the silicon substrate 138 (e.g., by depositing a photoresist and patterning it using any suitable method). The patterned photoresist 194 may include an opening 196 proximate to the backside surface 192 of the TSV 100.

[0038] FIG. 12 illustrates an assembly 1200 subsequent to providing a copper fill 198 in the opening 196 of the assembly 1100 (FIG. 11). The copper fill 198 may be provided by, for example, depositing a copper seed layer and electroplating copper onto the seed layer, as known in the art.

[0039] FIG. 13 illustrates an assembly 1300 subsequent to performing a wet etch to remove the copper fill 198 above the photoresist 194 of the assembly 1200 (FIG. 12), leaving a copper contact 199 in contact with the backside surface 192 of the TSV 100. The copper contact 199 may be part of
a back metal layer 197. In some embodiments, the back metal layer 197 may be a redistribution layer, for example.

[0040] FIG. 14 illustrates an assembly 1400 subsequent to depositing a layer of nitride 195 on the back metal layer 197 of the assembly 1300 (FIG. 13), patterning the nitride 195 to form an opening 191 above the copper contact 199, and forming a metal pad 193 in the opening 191. The metal pad 193 may be in conductive contact with the copper contact 199, which may be an electrical contact with the TSV 100, which may be an electrical contact with the front metal layer 144, as discussed above. In some embodiments, the nitride 195 may be deposited using a CVD process, and the opening 191 may be formed using any suitable lithography techniques. In some embodiments, the metal pad 193 may be formed from a non-copper material (e.g., cobalt or gold), and may be formed via electroless plating.

[0041] FIG. 15 illustrates an IC device 1800 subsequent to coupling a conductive contact 187 of an IC package 189 to the back metal layer 197 of the assembly 1400 (FIG. 14) via the metal pad 193. A conductive pathway from the IC package 189 to the front metal layer 144 may include the conductive contact 187, the metal pad 193, the copper contact 199, the TSV 100, and the titanium 148. The IC package may include any suitable circuitry for performing any desired function. For example, in some embodiments, the IC package 189 may be a memory device.

[0042] FIG. 16 is a flow diagram of a method 1600 of manufacturing an anchored TSV, in accordance with various embodiments. While the operations of the method 1600 are arranged in a particular order in FIG. 16 and illustrated once each, in various embodiments, one or more of the operations may be repeated (e.g., when multiple TSVs are formed). Operations discussed below with reference to the method 1600 may be illustrated with reference to the TSV 100 of FIGS. 2-15, but this is simply for ease of discussion, and the method 1600 may be used to form any appropriate anchored TSV. The various operations discussed below with reference to the method 1600 may be performed in accordance with any of the embodiments of the TSV 100 disclosed herein, for example.

[0043] At 1602, a DRIE process may be performed in a silicon substrate to form an opening between a backside of the silicon substrate and a front metal layer disposed at the front side of the silicon substrate. For example, as discussed above with reference to FIG. 3, a DRIE process may be performed in a silicon substrate 138 to form an opening 156 between a backside 142 of the silicon substrate 138 and a front metal layer 144 disposed at the front side 140 of the silicon substrate 138. In some embodiments, the front metal layer may not be grounded during the DRIE process of 1602.

[0044] At 1604, the DRIE process may be continued upon reaching the front metal layer such that a cross section of the opening includes lateral recesses in the silicon substrate, wherein the lateral recesses are proximate to the front metal layer. For example, as discussed above with reference to FIG. 4, a DRIE process may be continued upon reaching the front metal layer 144 such that a cross
section of the opening 156 includes lateral recesses 162 and the silicon substrate 138. The lateral recesses 162 of FIG. 4 are proximate to the front metal layer 144. In some embodiments, the front metal layer may not be grounded during the DRIE process of 1604.

[0045] At 1606, the DRIE process may be terminated subsequent to forming the lateral recesses such that the opening includes a first portion having a first width, a second portion having a second width greater than the first width, and a third portion having a third width less than the second width, wherein the second portion is disposed between the first and third portions, and the second portion includes lateral recesses. For example, as illustrated in FIG. 4, the opening 156 includes a first portion 172 having a first width 182, a second portion 174 having a second width 184 greater than the first width 182, and a third portion 176 having a third width 186 less than the second width 184. The second portion 174 of FIG. 4 is disposed between the first portion 172 and the third portion 176, and includes the lateral recesses 162.

[0046] The TSVs disclosed herein may be included in any suitable IC device, which may in turn be included in any suitable computing device. FIGS. 17-20 illustrate various examples of apparatuses that may include any of the TSVs disclosed herein. Similarly, the methods disclosed herein may be used in any suitable stage in the manufacture of any of the apparatuses discussed below with reference to FIGS. 17-20.

[0047] FIGS. 17A-B are top views of a wafer 1700 and dies 1702 that may include the TSV 100 (not shown) in accordance with any of the embodiments disclosed herein. The TSV 100 may be included in any of multiple IC structures formed on the wafer 1700. The wafer 1700 may be composed of semiconductor material and may include one or more dies 1702 having IC structures formed on a surface of the wafer 1700. In particular, the wafer 1700 may provide the silicon substrate 138 in which the TSV 100 is disposed. Each of the dies 1702 may be a repeating unit of a semiconductor product that includes one or more of the TSVs 100. After the fabrication of the semiconductor product is complete (e.g., including the operations discussed above with reference to FIGS. 2-14), the wafer 1700 may undergo a singulation process in which each of the dies 1702 is separated from one another to provide discrete “chips” of the semiconductor product. Thus, the TSV 100 may be present in the wafer 1700 due to its presence in the dies 1702. In particular, the TSV 100 may take the form of the wafer 1700 (e.g., not singulated) or the form of the die 1702 (e.g., singulated). In addition to the TSV 100, the die 1702 may include one or more transistors (e.g., transistor(s) 1840 of FIG. 18, discussed below) and/or supporting circuitry to route electrical signals to the one or more transistors, as well as any other IC components.

[0048] In some embodiments, the TSV 100 may be included in memory and logic devices combined on a single die 1702. For example, a memory array may be formed on a same die 1702 as a processing device (e.g., the processing device 2002 of FIG. 20) or other logic that is configured to
store information in the memory array or execute instructions stored in the memory array. For example, a processing device and a cache may be formed on the same die.

[0049] FIG. 18 is a cross-sectional side view of an IC device 1800 that may include a TSV 100 in accordance with any of the embodiments disclosed herein. The IC device 1800 may be formed on a substrate 1802 (e.g., the wafer 1700 of FIG. 17A, and the silicon substrate 138 of the TSV 100) and may be included in a die (e.g., the die 1702 of FIG. 17B). The substrate 1802 may be a semiconductor substrate composed of semiconductor material systems including, for example, N-type or P-type materials systems. In particular, the substrate 1802 may include silicon to provide the silicon substrate 138 of the TSV 100. The substrate 1802 may include, for example, a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In some embodiments, the semiconductor substrate 1802, or substrates for other IC devices included in a common computing device with the TSV 100, may be formed using alternative materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V, or IV materials may also be used to form a substrate for an IC device. Although a few examples of materials from which a substrate may be formed are described here, any material that may serve as a foundation for an IC device 1800 may be used as suitable. The substrate 1802 may be part of a singulated die (e.g., the dies 1702 of FIG. 17B) or a wafer (e.g., the wafer 1700 of FIG. 17A). The substrate 1802 may have a front side 1850 (e.g., corresponding to the front side 140 of the silicon substrate 138 of FIG. 1) and a back side 1854 (e.g., corresponding to the back side 142 of the silicon substrate 138 of FIG. 1).

[0050] The IC device 1800 may include one or more device layers 1804 disposed on the substrate 1802. The device layer 1804 may include features of one or more transistors 1840 (e.g., metal-oxide semiconductor field-effect transistors (MOSFETs)) formed on the substrate 1802. The device layer 1804 may include, for example, one or more source and/or drain (S/D) regions 1820, a gate 1822 to control current flow in transistors 1840 between the S/D regions 1820, and one or more S/D contacts 1824 to route electrical signals to/from the S/D regions 1820. The transistors 1840 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 1840 are not limited to the type and configuration depicted in FIG. 18 and may include a wide variety of other types and configurations, such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors, such as double-gate transistors or tri-gate transistors, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors.

[0051] Each transistor 1840 may include a gate 1822 formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers.
The one or more layers may include silicon oxide, silicon dioxide, and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0052] The gate electrode layer may be formed on the gate dielectric layer and may include at least one P-type work function metal or N-type work function metal, depending on whether the transistor 1840 is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer. For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides (e.g., ruthenium oxide). For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide.

[0053] In some embodiments, when viewed as a cross section of the transistor 1840 along the source-channel-drain direction, the gate electrode may consist of a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In other embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0054] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack to bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used; for
instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of
the gate stack.

[0055] The S/D regions 1820 may be formed within the substrate 1802 adjacent to the gate 1822 of
each transistor 1840. The S/D regions 1820 may be formed using either an implantation/diffusion
process or an etching/deposition process. In the former process, dopants such as boron, aluminum,
antimony, phosphorous, or arsenic may be ion-implanted into the substrate 1802 to form the S/D
regions 1820. An annealing process that activates the dopants and causes them to diffuse further
into the substrate 1802 may follow the ion implantation process. In the latter process, the substrate
1802 may first be etched to form recesses at the locations of the S/D regions 1820. An epitaxial
deposition process may then be carried out to fill the recesses with material that is used to fabricate
the S/D regions 1820. In some implementations, the S/D regions 1820 may be fabricated using a
silicon alloy such as silicon germanium or silicon carbide. In some embodiments, the epitaxially
deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In
some embodiments, the S/D regions 1820 may be formed using one or more alternate
semiconductor materials such as germanium or a group III-V material or alloy. In further
embodiments, one or more layers of metal and/or metal alloys may be used to form the S/D regions
1820.

[0056] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or
from the transistors 1840 of the device layer 1804 through one or more interconnect layers disposed
on the device layer 1804 (illustrated in FIG. 18 as interconnect layers 1806-1810). For example,
electrically conductive features of the device layer 1804 (e.g., the gate 1822 and the S/D contacts
1824) may be electrically coupled with interconnect structures 1828 of the interconnect layers 1806-
1810. The one or more interconnect layers 1806-1810 may form an interlayer dielectric (ILD) stack
1819 of the IC device 1800. In some embodiments, an interconnect layer may be referred to as a
"metal layer" or a "metallization stack."

[0057] The interconnect structures 1828 may be arranged within the interconnect layers 1806-1810
to route electrical signals according to a wide variety of designs (in particular, the arrangement is not
limited to the particular configuration of interconnect structures 1828 depicted in FIG. 18). Although
a particular number of interconnect layers 1806-1810 is depicted in FIG. 18, embodiments of the
present disclosure include IC devices having more or fewer interconnect layers than depicted by
interconnect layers 1806-1810.

[0058] In some embodiments, the interconnect structures 1828 may include trench structures
1828a (sometimes referred to as "lines") and/or via structures 1828b (sometimes referred to as
"holes") filled with an electrically conductive material such as a metal. The trench structures 1828a
may be arranged to route electrical signals in a direction of a plane that is substantially parallel with
a surface of the substrate 1802 upon which the device layer 1804 is formed. For example, the trench structures 1828a may route electrical signals in a direction in and out of the page from the perspective of FIG. 18. The via structures 1828b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 1802 upon which the device layer 1804 is formed. In some embodiments, the via structures 1828b may electrically couple trench structures 1828a of different interconnect layers 1806-1810 together.

The interconnect layers 1806-1810 may include a dielectric material 1826 disposed between the interconnect structures 1828, as shown in FIG. 18. In some embodiments, the dielectric material 1826 disposed between the interconnect structures 1828 in different ones of the interconnect layers 1806-1810 may have different compositions; in other embodiments, the composition of the dielectric material 1826 between different interconnect layers 1806-1810 may be the same.

A first interconnect layer 1806 (referred to as Metal 1 or "M1") may be formed directly on the device layer 1804. In some embodiments, the first interconnect layer 1806 may include trench structures 1828a and/or via structures 1828b, as shown. Trench structures 1828a of the first interconnect layer 1806 may be coupled with contacts (e.g., S/D contacts 1824) of the device layer 1804. In some embodiments, the first interconnect layer 1806 may provide the front metal layer 144 discussed above with reference to FIGS. 1-16. As illustrated in FIG. 18, a TSV 100 may be in conductive contact with the front metal layer 144, and may be part of a conductive pathway between the front metal layer 144 and the IC package 189, as discussed above with reference to FIG. 15. Only one TSV 100 is shown in FIG. 18 for ease of illustration, and multiple TSVs 100 may be included in an IC device 1800.

A second interconnect layer 1808 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 1806. In some embodiments, the second interconnect layer 1808 may include via structures 1828b to couple the trench structures 1828a of the second interconnect layer 1808 with the trench structures 1828a of the first interconnect layer 1806. Although the trench structures 1828a and the via structures 1828b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 1808) for the sake of clarity, the trench structures 1828a and the via structures 1828b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

A third interconnect layer 1810 (referred to as Metal 3 or "M3") (and additional interconnect layers, as desired) may be formed in succession on the second interconnect layer 1808 according to similar techniques and configurations described in connection with the second interconnect layer 1808 on the first interconnect layer 1806.

The IC device 1800 may include a solder resist material 1834 (e.g., polyimide or similar material) and one or more bond pads 1836 formed on the interconnect layers 1806-1810. The bond
pads 1836 may be electrically coupled with the interconnect structures 1828 and configured to route the electrical signals of transistor(s) 1840 (and any devices coupled to the back side of the semiconductor substrate 1802 and in conductive contact with the TSV 100, such as the IC package 189) to other external devices. For example, solder bonds may be formed on the one or more bond pads 1836 to mechanically and/or electrically couple a chip including the IC device 1800 with another component (e.g., a circuit board). The IC device 1800 may have other alternative configurations to route the electrical signals from the interconnect layers 1806-1810 than depicted in other embodiments. For example, the bond pads 1836 may be replaced by or may further include other analogous features (e.g., posts) that route the electrical signals to external components.

[0064] FIG. 19 is a cross-sectional side view of an IC device assembly 1900 that may include a TSV 100 in accordance with any of the embodiments disclosed herein. The IC device assembly 1900 includes a number of components disposed on a circuit board 1902 (which may be, for example, a motherboard). The IC device assembly 1900 includes components disposed on a first face 1940 of the circuit board 1902 and an opposing second face 1942 of the circuit board 1902; generally, components may be disposed on one or both faces 1940 and 1942.

[0065] In some embodiments, the circuit board 1902 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 1902. In other embodiments, the circuit board 1902 may be a non-PCB substrate.

[0066] The IC device assembly 1900 illustrated in FIG. 19 includes a package-on-interposer structure 1936 coupled to the first face 1940 of the circuit board 1902 by coupling components 1916. The coupling components 1916 may electrically and mechanically couple the package-on-interposer structure 1936 to the circuit board 1902, and may include solder balls (as shown in FIG. 19), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0067] The package-on-interposer structure 1936 may include an IC package 1920 coupled to an interposer 1904 by coupling components 1918. The coupling components 1918 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 1916. Although a single IC package 1920 is shown in FIG. 19, multiple IC packages may be coupled to the interposer 1904; indeed, additional interposers may be coupled to the interposer 1904. The interposer 1904 may provide an intervening substrate used to bridge the circuit board 1902 and the IC package 1920. The IC package 1920 may be or include, for example, a die (the die 1702 of FIG. 17B), an IC device (e.g., the IC device 1800 of FIG. 18), or any other suitable component.
Generally, the interposer 1904 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 1904 may couple the IC package 1920 (e.g., a die) to a ball grid array (BGA) of the coupling components 1916 for coupling to the circuit board 1902. In the embodiment illustrated in FIG. 19, the IC package 1920 and the circuit board 1902 are attached to opposing sides of the interposer 1904; in other embodiments, the IC package 1920 and the circuit board 1902 may be attached to a same side of the interposer 1904. In some embodiments, three or more components may be interconnected by way of the interposer 1904.

[0068] The interposer 1904 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 1904 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 1904 may include metal interconnects 1908 and vias 1910, including but not limited to TSVs 1906 (which may include one or more of the TSVs 100). The interposer 1904 may further include embedded devices 1914, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 1904. The package-on-interposer structure 1936 may take the form of any of the package-on-interposer structures known in the art.

[0069] The IC device assembly 1900 may include an IC package 1924 coupled to the first face 1940 of the circuit board 1902 by coupling components 1922. The coupling components 1922 may take the form of any of the embodiments discussed above with reference to the coupling components 1916, and the IC package 1924 may take the form of any of the embodiments discussed above with reference to the IC package 1920.

[0070] The IC device assembly 1900 illustrated in FIG. 19 includes a package-on-package structure 1934 coupled to the second face 1942 of the circuit board 1902 by coupling components 1928. The package-on-package structure 1934 may include an IC package 1926 and an IC package 1932 coupled together by coupling components 1930 such that the IC package 1926 is disposed between the circuit board 1902 and the IC package 1932. The coupling components 1928 and 1930 may take the form of any of the embodiments of the coupling components 1916 discussed above, and the IC packages 1926 and 1932 may take the form of any of the embodiments of the IC package 1920 discussed above. The package-on-package structure 1934 may be configured in accordance with any of the package-on-package structures known in the art.
FIG. 20 is a block diagram of an example computing device 2000 that may include a TSV 100 in accordance with the teachings of the present disclosure. In particular, any of the components of the computing device 2000 that may include TSVs may include the TSV 100 (e.g., in the form of an IC device 1800 (FIG. 18), and/or in a die 1702 (FIG. 17B)). A number of components are illustrated in FIG. 20 as included in the computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the computing device 2000 may be attached to one or more motherboards. In some embodiments, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die.

Additionally, in various embodiments, the computing device 2000 may not include one or more of the components illustrated in FIG. 20, but the computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the computing device 2000 may not include an audio input device 2024 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2024 or audio output device 2008 may be coupled. Any one or more of the components of the computing device 2000 may be included in one or more IC devices that may include an embodiment of the TSV 100 disclosed herein.

The computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices. The computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), non-volatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the memory 2004 may include memory that shares a die with the processing device 2002. This memory may be used as cache memory and may include embedded DRAM (eDRAM) or spin-transfer torque magnetic random-access memory (STT-MRAM). The processing device 2002 and/or the memory 2004 may include one or more of the TSVs 100.
In some embodiments, the computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the computing device 2000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

The communication chip 2012 may implement any of a number of wireless standards or protocols, including, but not limited to, Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultra mobile broadband (UMB) project (also referred to as “3GPP2”), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE.
EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications. The communication chip 2012 may include one or more of the TSVs 100.

[0077] The computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the computing device 2000 to an energy source separate from the computing device 2000 (e.g., AC line power).

[0078] The computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0079] The computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0080] The computing device 2000 may include an audio input device 2024 (or corresponding interface circuitry, as discussed above). The audio input device 2024 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0081] The computing device 2000 may include a global positioning system (GPS) device 2018 (or corresponding interface circuitry, as discussed above). The GPS device 2018 may be in communication with a satellite-based system and may receive a location of the computing device 2000, as known in the art.

[0082] The computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0083] The computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0084] The computing device 2000 may have any desired form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultra-mobile personal computer, etc.), a desktop computing device, a server or
other networked computing component, a printer, a scanner, a monitor, a set-top box, an
entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a
wearable computing device. In some embodiments, the computing device 2000 may be any other
electronic device that processes data.

[0085] The following paragraphs provide various examples of the embodiments disclosed herein.

[0086] Example 1 is a through-silicon via (TSV), including: a first copper portion having a first width;
a second copper portion having a second width greater than the first width; and a third copper
portion having a third width less than the second width; wherein the second copper portion is
disposed between the first copper portion and the third copper portion.

[0087] Example 2 may include the subject matter of Example 1, and may further specify that the
third width is the same as the first width.

[0088] Example 3 may include the subject matter of any of Examples 1-2, and may further specify
that a cross section of the second copper portion includes two projections extending away from a
body of the TSV.

[0089] Example 4 may include the subject matter of Example 3, and may further specify that the
second width is a distance between tips of the two projections.

[0090] Example 5 may include the subject matter of any of Examples 3-4, and may further specify
that each projection has a first surface proximate to the first copper portion and a second surface
proximate to the second copper portion.

[0091] Example 6 may include the subject matter of Example 5, and may further specify that the
projections are first projections, and each first surface of the first projections includes a second
projection.

[0092] Example 7 may include the subject matter of Example 6, and may further specify that each
second projection has a tip.

[0093] Example 8 may include the subject matter of any of Examples 6-7, and may further specify
that each first surface has a portion with convex curvature.

[0094] Example 9 may include the subject matter of any of Examples 5-8, and may further specify
that each second surface has a portion with convex curvature.

[0095] Example 10 may include the subject matter of any of Examples 1-9, and may further specify
that the first width is at least 4 µm.

[0096] Example 11 may include the subject matter of any of Examples 1-10, and may further specify
that the third width is at least 4 µm.

[0097] Example 12 may include the subject matter of any of Examples 1-11, and may further specify
that the second width is at least 7 µm.
Example 13 may include the subject matter of any of Examples 1-12, and may further specify that the second width is at least 10 µm.

Example 14 may include the subject matter of any of Examples 1-13, and may further specify that the TSV has a height greater than 50 µm.

Example 15 may include the subject matter of any of Examples 1-14, and may further specify that the TSV has a height greater than 100 µm.

Example 16 may include the subject matter of any of Examples 1-15, and may further specify that the second copper portion is flared between the first width and the second width.

Example 17 may include the subject matter of any of Examples 1-16, and may further specify that the second copper portion is flared between the first width and the third width.

Example 18 may include the subject matter of any of Examples 1-17, and may further specify that side surfaces of the first copper portion are scalloped.

Example 19 is an integrated circuit (IC) device, including: a silicon substrate having a front side and a back side; a front metal layer disposed at the front side of the silicon substrate; and a through-silicon via (TSV) extending from the front metal layer to the back side, wherein the TSV includes: a first copper portion having a first width, a second copper portion having a second width greater than the first width, and a third copper portion having a third width less than the second width, wherein the second copper portion is disposed between the first copper portion and the third copper portion.

Example 20 may include the subject matter of Example 19, and may further specify that the third copper portion is disposed between the second copper portion and the front metal layer.

Example 21 may include the subject matter of any of Examples 19-20, and may further specify that the first copper portion has side surfaces, and the IC device further includes silicon oxide disposed between the side surfaces and the silicon substrate.

Example 22 may include the subject matter of Example 21, and may further include titanium disposed between the side surfaces and the silicon oxide.

Example 23 may include the subject matter of any of Examples 19-22, and may further specify that a surface of the TSV at the back side is chemically mechanically polished.

Example 24 may include the subject matter of any of Examples 19-23, and may further include a back metal layer disposed at the back side, wherein the TSV extends to the back metal layer.

Example 25 may include the subject matter of any of Examples 19-24, and may further include a memory device disposed at the back side and coupled to the TSV.

Example 26 is a method of manufacturing a through-silicon via (TSV), including: performing a deep-reactive ion etching (DRIE) process in a silicon substrate to form an opening between a back
side of the silicon substrate and a front metal layer disposed at a front side of the silicon substrate; continuing the DRIE process upon reaching the front metal layer such that a cross section of the opening includes lateral recesses in the silicon substrate, wherein the lateral recesses are proximate to the front metal layer; and terminating the DRIE process subsequent to forming the lateral recesses such that the opening includes: a first portion having a first width, a second portion having a second width greater than the first width, and a third portion having a third width less than the second width, wherein the second portion is disposed between the first and third portions, and the second portion includes the lateral recesses.

Example 27 may include the subject matter of Example 26, and may further specify that the front metal layer is not grounded during the DRIE process.

Example 28 may include the subject matter of any of Examples 26-27, and may further include: providing a silicon oxide layer to the surfaces of the opening; removing the silicon oxide layer at a bottom surface of the opening, wherein the bottom surface is proximate to the front metal layer; and after removing the silicon oxide layer at the bottom surface of the opening, providing a titanium layer to the surfaces of the opening.

Example 29 may include the subject matter of Example 28, and may further include: subsequent to providing the titanium layer, providing a copper seed layer to the surfaces of the opening; and subsequent to providing the copper seed layer, filling the opening with copper to form the TSV.

Example 30 may include the subject matter of Example 29, and may further specify that the lateral recesses have a first surface proximate to the first portion, a second surface proximate to the second portion, and no copper seed layer is present on the first surface.

Example 31 may include the subject matter of any of Examples 29-30, and may further include forming a back metal layer on the back side of the silicon substrate, the back metal layer coupled to the TSV.

Example 32 may include the subject matter of Example 31, and may further include coupling an integrated circuit (IC) package to the back metal layer.

Example 33 is a computing device, including: a memory device; and a processing device, coupled to the memory device, wherein the processing device includes: a silicon substrate having a front side and a back side, a front metal layer disposed at the front side of the silicon substrate, and a through-silicon via (TSV) extending from the front metal layer to the back side, wherein the TSV includes a first copper portion having a first width, a second copper portion having a second width greater than the first width, and a third copper portion having a third width less than the second width, wherein the second copper portion is disposed between the first copper portion and the third copper portion.
Example 34 may include the subject matter of Example 33, and may further include: an antenna; a communication chip; a display; and a battery.

Example 35 may include the subject matter of any of Examples 33-34, and may further include a graphics processing unit, a power amplifier, a global positioning system receiver, or a voltage regulator.

Example 36 may include the subject matter of any of Examples 33-35, and may further specify that a cross section of the second copper portion includes two projections extending away from a body of the TSV.

Example 37 may include the subject matter of Example 36, and may further specify that each projection has a first surface proximate to the first copper portion and a second surface proximate to the second copper portion.

Example 38 may include the subject matter of Example 37, and may further specify that the projections are first projections, and each first surface of the first projections includes a second projection.

Example 39 may include the subject matter of Example 38, and may further specify that each second projection has a tip.

Example 40 may include the subject matter of any of Examples 37-39, and may further specify that each second surface has convex curvature.

Example 41 may include the subject matter of any of Examples 37-40, and may further specify that each first surface has convex curvature.
Claims:
1. A through-silicon via (TSV), comprising:
   a first copper portion having a first width;
   a second copper portion having a second width greater than the first width; and
   a third copper portion having a third width less than the second width;
   wherein the second copper portion is disposed between the first copper portion and the
   third copper portion.
2. The TSV of claim 1, wherein the third width is the same as the first width.
3. The TSV of claim 1, wherein a cross section of the second copper portion includes two projections extending away from a body of the TSV.
4. The TSV of claim 3, wherein the second width is a distance between tips of the two projections.
5. The TSV of claim 3, wherein each projection has a first surface proximate to the first copper portion and a second surface proximate to the second copper portion.
6. The TSV of claim 5, wherein the projections are first projections, and each first surface of the first projections includes a second projection.
7. The TSV of claim 6, wherein each second projection has a tip.
8. The TSV of any of claims 1-7, wherein the first width is at least 4 µm.
9. The TSV of any of claims 1-7, wherein the third width is at least 4 µm.
10. The TSV of any of claims 1-7, wherein the second width is at least 7 µm.
11. The TSV of any of claims 1-7, wherein the second width is at least 10 µm.
12. The TSV of any of claims 1-7, wherein the TSV has a height greater than 50 µm.
13. The TSV of any of claims 1-7, wherein side surfaces of the first copper portion are scalloped.
14. An integrated circuit (IC) device, comprising:
   a silicon substrate having a front side and a back side;
   a front metal layer disposed at the front side of the silicon substrate; and
   a through-silicon via (TSV) extending from the front metal layer to the back side, wherein the TSV includes:
   a first copper portion having a first width,
   a second copper portion having a second width greater than the first width, and
   a third copper portion having a third width less than the second width,
   wherein the second copper portion is disposed between the first copper portion and the
   third copper portion.
15. The IC device of claim 14, wherein the third copper portion is disposed between the second copper portion and the front metal layer.
16. The IC device of claim 14, wherein the first copper portion has side surfaces, and the IC device further comprises:

   silicon oxide disposed between the side surfaces and the silicon substrate.

17. The IC device of claim 16, further comprising:

   titanium disposed between the side surfaces and the silicon oxide.

18. The IC device of any of claims 14-17, wherein a surface of the TSV at the back side is chemically mechanically polished.

19. The IC device of any of claims 14-17, further comprising:

   a back metal layer disposed at the back side, wherein the TSV extends to the back metal layer.

20. The IC device of any of claims 14-17, further comprising:

   a memory device disposed at the back side and coupled to the TSV.

21. A method of manufacturing a through-silicon via (TSV), comprising:

   performing a deep-reactive ion etching (DRIE) process in a silicon substrate to form an opening between a back side of the silicon substrate and a front metal layer disposed at a front side of the silicon substrate;

   continuing the DRIE process upon reaching the front metal layer such that a cross section of the opening includes lateral recesses in the silicon substrate, wherein the lateral recesses are proximate to the front metal layer; and

   terminating the DRIE process subsequent to forming the lateral recesses such that the opening includes:

   a first portion having a first width,

   a second portion having a second width greater than the first width, and

   a third portion having a third width less than the second width,

   wherein the second portion is disposed between the first and third portions, and the second portion includes the lateral recesses.

22. The method of claim 21, wherein the front metal layer is not grounded during the DRIE process.

23. A computing device, comprising:

   a memory device; and

   a processing device, coupled to the memory device, wherein the processing device includes:

   a silicon substrate having a front side and a back side,

   a front metal layer disposed at the front side of the silicon substrate, and

   a through-silicon via (TSV) extending from the front metal layer to the back side,

   wherein the TSV includes a first copper portion having a first width, a second copper portion having a second width greater than the first width, and a third copper portion having a third width less than
the second width, wherein the second copper portion is disposed between the first copper portion and the third copper portion.

24. The computing device of claim 23, further comprising:
   
   an antenna;
   
   a communication chip;
   
   a display; and
   
   a battery.

25. The computing device of any of claims 23-24, wherein a cross section of the second copper portion includes two projections extending away from a body of the TSV.
PERFORM A DEEP-REACTIVE (OR ETCHING DRIE) PROCESS IN A SILICON SUBSTRATE TO FORM AN OPENING BETWEEN A BACK SIDE OF THE SILICON SUBSTRATE AND A FRONT METAL LAYER DISPOSED AT A FRONT SIDE OF THE SILICON SUBSTRATE.

CONTINUE THE DRIE PROCESS UNTIL REACHING THE FRONT METAL LAYER SUCH THAT A CROSS SECTION OF THE OPENING INCLUDES LATERAL RECEESSES IN THE SILICON SUBSTRATE, WHEREIN THE LATERAL RECEESSES ARE PROXIMATE TO THE FRONT METAL LAYER.

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/60(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/60; H01L 21/768; H01L 21/20; H01L 23/48; H01L 29/06; H01L 21/265

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: hole, trench, TSV, width, substrate, metal, side, semiconductor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US 2004-0140563 A1 (JONG-HYON AHN) 22 July 2004 See abstract, paragraphs [0049], [0054]-[0055], claims 1-2 and figures 1, 10A-10D.</td>
<td>1-4,8-12</td>
</tr>
<tr>
<td>Y</td>
<td>US 2015-0069581 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 12 March 2015 See abstract, paragraphs [0016]-[0021], claim 1 and figures 3-7.</td>
<td>13</td>
</tr>
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Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

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<tr>
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<th>Publication date</th>
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<th>Publication date</th>
</tr>
</thead>
<tbody>
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<td></td>
<td></td>
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<tr>
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</tr>
</tbody>
</table>