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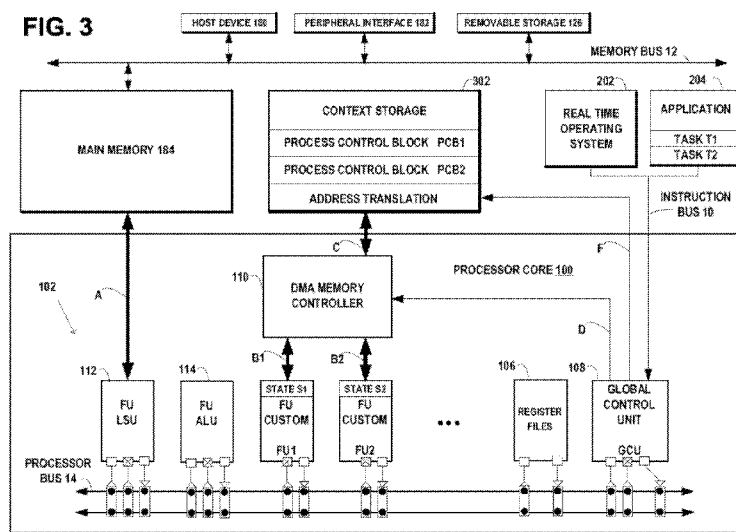
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(54) Title: METHOD, APPARATUS, AND COMPUTER PROGRAM PRODUCT FOR FAST CONTEXT SWITCHING OF APPLICATION SPECIFIC PROCESSORS



(57) Abstract: Embodiments of the invention enable fast context switching of application specific processors having functional units with an architecturally visible state. In example embodiments, a processor allocates memory space to store two process control blocks for two active tasks to be performed by the processor comprising one or more custom functional units having a respective processing state not accessible by the processor. A memory controller stores the processing state of the custom functional units currently running a first active task, in a first process control block, in response to a preemptive task switch requirement. The memory controller loads a second processing state of the custom functional units for a second active task, from a second process control block in the memory, in response to the preemptive task switch requirement. The processor may then perform the second active task, based on the second processing state loaded into the custom functional units.

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI2013/050555

A. CLASSIFICATION OF SUBJECT MATTER See extra sheet According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC: G06F, G06T Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched FI, SE, NO, DK Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI, XPESP, XPI3E, COMPDX, INSPEC, Internet		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7420572 B1 (YUE LORDSON L [US] et al.) 02 September 2008 (02.09.2008) abstract; column 4, line 17 - column 5, line 10; column 6, lines 2-17; figures 1 and 2	1-2, 4-5, 7-8, 10, 14-15, 17-18, 21-24, 26-27, 29-30, 33-34
X	WO 9411816 A1 (S MOS SYSTEMS INC [US]) 26 May 1994 (26.05.1994) abstract; page 3, lines 26-38; page 4, lines 21-30; page 5, lines 8-15; figures 1 and 4	1, 14, 22, 26, 33
A	CORPORAAL, H. TTAs: Missing the ILP Complexity Wall. Journal of Systems Architecture. June 1999, Vol. 45, No. 12-13, pages 949-973. DOI: 10.1016/S1383-7621(98)00046-0. the whole document	1-34
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
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INTERNATIONAL SEARCH REPORT
Information on patent family members

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Patent document cited in search report	Publication date	Patent family members(s)	Publication date
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WO 9411816 A1	26/05/1994	JP H08505965 A	25/06/1996
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