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[Continued on next page]

(54) Title: BARRIER LAYER ON POLYMER PASSIVATION FOR INTEGRATED CIRCUIT PACKAGING

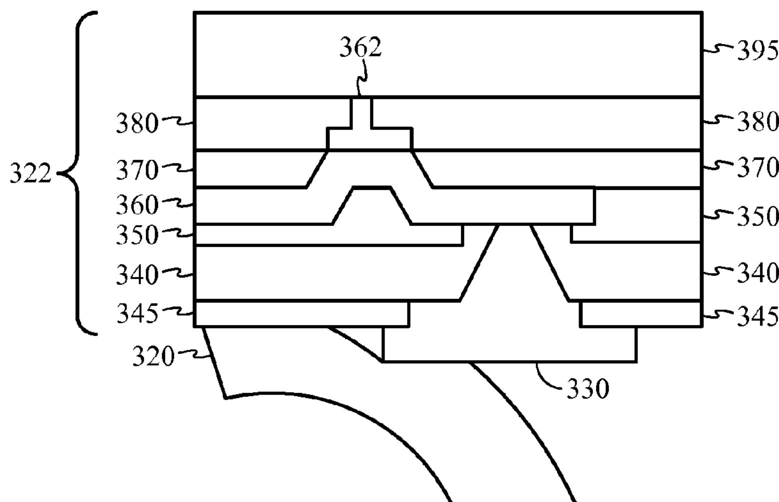

FIG. 3B

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(57) Abstract: A barrier layer deposited on the passivation layer of a semiconductor die decreases adhesion of glue used during stacking of semiconductor dies by altering chemical or structural properties of the passivation layer. During detachment of a carrier wafer from a wafer, the barrier layer reduces glue residue on the wafer by modifying the surface of the passivation layer. The barrier layer may be insulating films such as silicon dioxide, silicon nitride, silicon carbide, polytetrafluoroethylene, organic layers, or epoxy and may be less than two micrometers in thickness. Additionally, the barrier layer may be used to reduce topography of the semiconductor die to decrease adhesion of glues.

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BARRIER LAYER ON POLYMER PASSIVATION FOR INTEGRATED CIRCUIT PACKAGING

TECHNICAL FIELD

[0001] The present disclosure generally relates to integrated circuits. More specifically, the present disclosure relates to packaging integrated circuits.

BACKGROUND

[0002] Passivation of an integrated circuit (IC) during fabrication is conventionally accomplished by depositing a polymer such as polyimide over the IC. The passivation layer provides compliance and acts as a mechanical cushion for the IC. Polymers have several characteristics that may cause problems during later steps in packaging. For example, polymers have high moisture absorption rates, which reduce reliability of the IC after packaging. Additionally, polymers have strong adhesion to glues temporarily applied during packaging, which increases the difficulty of removing the glue. One example of when glues are applied is during manufacturing of stacked ICs.

[0003] Recently, desire for stacked ICs has increased as stacked ICs allow manufacturing of higher density ICs through 3D stacking than could be achieved on a 2D IC. For example, DRAM may be stacked above a microprocessor to increase the number of transistors and functionality of an IC without increasing the die size. A block diagram illustrating a conventional stacked IC is shown in FIGURE 1A. A stacked IC 100 includes a packaging substrate 110. The packaging substrate 110 is coupled to a first tier die 120 through a packaging connection 112 such as bumps in a ball grid array. A second tier die 130 is coupled to the first tier die 120 through a packaging connection 122. The first tier die 120 includes through silicon vias 124, which couple the packaging substrate 110 to the packaging connection 122 to allow communication with the second tier die 130.

[0004] Manufacturing through silicon vias 124 in the first tier die 120 includes thinning the first tier die 120. To improve stability of the first tier die 120 during thinning, the first tier die 120 is attached to a carrier wafer by glue. A flow chart illustrating a conventional process flow for manufacturing a stacked IC is shown in FIGURE 1B. At block 150 a wafer is received and attached to a carrier wafer at block

155. The wafer is thinned at block 160 and processed at block 165. Processing at block 165 may include, for example, attaching a second tier wafer. At block 170 the wafer is detached from the carrier wafer.

[0005] Glue applied during carrier wafer attachment at block 155 attaches to the final passivation layer of integrated circuits on the first tier wafer. Adhesion between glue and the final passivation layer causes difficulty in completely removing the glue during detachment from the carrier wafer at block 170. Additionally, plasma processing of the passivation layer roughens the passivation layer, further increasing adhesion. The adhesion problem is demonstrated with reference to FIGURES 2A-B.

[0006] FIGURE 2A is a block diagram illustrating a conventional wafer attached to a carrier wafer. A carrier wafer 210 is attached to a wafer 222 by a glue 220. The wafer 222 includes a semiconductor layer 295. A flip chip bump 230 provides an electrical contact to a metal layer 260 (e.g., redistribution layer) and a top metal 262. Insulating layers 250, 270, 280 separate the metal layer 260 from other layers in the wafer 222. The insulating layer 280 may be, for example, a low-k (LK), an extra low-k (ELK), or an ultra low-k (ULK) dielectric layer. A passivation layer 240 on the wafer 222 provides the final separation between outside elements and the wafer 222. Adhesion between the glue 220 and the passivation layer 240 makes removal of the glue 220 after detachment of the carrier wafer 210 difficult as illustrated in FIGURE 2B.

[0007] FIGURE 2B is a block diagram illustrating a conventional wafer after detachment from a carrier wafer. The carrier wafer 210 is detached from the glue 220, and the glue 220 is removed from wafer 222. However, strong adhesion between the glue 220 and the passivation layer 240 results in residue left behind. Additionally, strong adhesion results in delamination 282 of the LK, ELK, and/or ULK dielectrics in the insulating layer 280. Reduced mass of LK, ELK, and ULK dielectric materials increases susceptibility of the insulating layer 280 to delamination 282. Damage to the insulating layer 280 may change operating characteristics of ICs in the wafer 222.

[0008] Thus, there is a need for an improved process and structure for passivation of integrated circuits.

BRIEF SUMMARY

[0009] According to one aspect of the disclosure, a layer structure for a semiconductor die includes an insulating layer of the semiconductor die. The layer structure also includes a passivation layer on the insulating layer that provides compliance for the semiconductor die. The layer structure further includes a barrier layer on the passivation layer that reduces adhesion of glues applied during semiconductor manufacturing to the passivation layer.

[0010] According to another aspect of the disclosure, a semiconductor manufacturing process includes patterning a passivation layer of a semiconductor die. The semiconductor manufacturing process also includes depositing a barrier layer on the passivation layer that reduces adhesion of glues applied during the semiconductor manufacturing process to the passivation layer. The semiconductor manufacturing process further includes patterning the barrier layer.

[0011] According to yet another aspect of the disclosure, a semiconductor manufacturing process includes building up a flip chip bump. The semiconductor manufacturing process also includes depositing a barrier layer after building up the flip chip bump. The semiconductor manufacturing process further includes patterning the barrier layer to expose the flip chip bump.

[0012] According to another aspect of the disclosure, a layer structure for a semiconductor die includes an insulator layer of the semiconductor die. The layer structure also includes a passivation layer on the insulator layer. The layer structure further includes means for modifying a surface to decrease adhesion, the surface modifying means disposed on the passivation layer.

[0013] According to yet another aspect of the disclosure, a semiconductor manufacturing process includes depositing a barrier layer on a semiconductor die to substantially cover an interface structure of the semiconductor die and to substantially cover a passivation layer of the semiconductor die. The semiconductor manufacturing process also includes etching the barrier layer to create a surface having reduced topography.

[0014] According to a further aspect of the disclosure, a semiconductor manufacturing process includes patterning a passivation layer of a semiconductor die. The semiconductor manufacturing process also includes depositing a barrier layer on the passivation layer that reduces adhesion of glues applied during the semiconductor

manufacturing process to the passivation layer. The semiconductor manufacturing process further includes patterning the barrier layer.

[0015] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description that follows may be better understood. Additional features and advantages will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the technology of the invention as set forth in the appended claims. The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] For a more complete understanding of the present invention, reference is now made to the following description taken in conjunction with the accompanying drawings.

[0017] FIGURE 1A is a block diagram illustrating a conventional stacked IC.

[0018] FIGURE 1B is a flow chart illustrating a conventional process flow for manufacturing a stacked IC.

[0019] FIGURE 2A is a block diagram illustrating a conventional wafer attached to a carrier wafer.

[0020] FIGURE 2B is a block diagram illustrating a conventional wafer after detachment from a carrier wafer.

[0021] FIGURE 3A is a block diagram illustrating a wafer having an exemplary barrier layer attached to a carrier wafer according to one embodiment.

[0022] FIGURE 3B is a block diagram illustrating a wafer having an exemplary barrier layer after detachment from a carrier wafer according to one embodiment.

[0023] FIGURE 4 is a flow chart illustrating an exemplary process flow for forming the barrier layer according to a first embodiment.

[0024] FIGURES 5A-F are block diagrams illustrating a die during an exemplary process for forming the barrier layer according to the first embodiment.

[0025] FIGURE 6 is a flow chart illustrating an exemplary process flow for forming the barrier layer according to a second embodiment.

[0026] FIGURES 7A-F are block diagrams illustrating a die during an exemplary process for forming the barrier layer according to the second embodiment.

[0027] FIGURE 8 is a block diagram illustrating an exemplary stacked IC having a barrier layer according to one embodiment.

[0028] FIGURES 9A-C are cross-sectional views illustrating a die during an exemplary process for forming the barrier layer according to a third embodiment.

[0029] FIGURE 10 is a flow chart illustrating an exemplary process flow for forming the barrier layer according to the third embodiment.

[0030] FIGURE 11 is a block diagram showing an exemplary wireless communication system in which an embodiment may be advantageously employed.

[0031] FIGURE 12 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component according to one embodiment.

DETAILED DESCRIPTION

[0032] A barrier layer may be deposited on the passivation layer of an integrated circuit (IC) to improve detachment of the carrier wafer after wafer thinning and to reduce glue residue remaining on the wafer after detachment. The barrier may be, for example, an inorganic film such as silicon nitride, silicon oxide, or an organic material such as polytetrafluoroethylene. The barrier layer may alter either the chemical or structural properties of the passivation layer to reduce adhesion.

[0033] FIGURE 3A is a block diagram illustrating a wafer having an exemplary barrier layer attached to a carrier wafer according to one embodiment. A

carrier wafer 310 is attached to a wafer 322 by a glue 320. The wafer 322 includes semiconductor layer 395 which may have front end of line (FEOL) layers and low metal layers. A bump 330 provides connection to a metal layer 360 such as, for example, a redistribution layer. The metal layer 360 couples to a top metal 362 for communication with devices and/or back-end-of-line (BEOL) layers in a semiconductor layer 395. The wafer 322 also includes insulating layers 350, 370, 380. A passivation layer 340 deposited on the wafer 322 protects the wafer 322 from outside elements and provides compliance.

[0034] Additionally, a barrier layer 345 deposited on the passivation layer 340 reduces adhesion between the glue 320 and the passivation layer 340. The barrier layer 345 modifies the surface of the passivation layer 340 to reduce moisture absorption and decrease adhesion to the glue 320. That is, the barrier layer 345 alters the chemical properties of the passivation layer 340. Stress and thickness of the barrier layer 345 are selected to preserve the low stress of the passivation layer 340. According to one embodiment, the barrier layer 345 is less than two micrometers in thickness and is either silicon dioxide, silicon nitride, silicon carbide, aluminum oxide, polytetrafluoroethylene, or other insulating materials. According to another embodiment, the thickness of the barrier layer 345 is 0.05 – 1.0 micrometers.

[0035] FIGURE 3B is a block diagram illustrating a wafer having an exemplary barrier layer after detachment from a carrier wafer according to one embodiment. After detaching the carrier wafer 310, the glue 320 is removed. The barrier layer 345 decreases adhesion of the glue 320 to the passivation layer 340 allowing removal of the glue 320 with reduced residue remaining on the wafer 322.

[0036] A process for depositing the barrier layer on the passivation layer is illustrated with reference to FIGURE 4 and FIGURES 5A-F. FIGURE 4 is a flow chart illustrating an exemplary process flow for forming the barrier layer according to a first embodiment. At block 410 a passivation layer is patterned. FIGURE 5A is a block diagram illustrating a wafer after patterning of the passivation layer according to the first embodiment. Insulating layers 510, 520, 540 surround a metal layer 530. According to one embodiment, the insulating layer 510 is SiO_2, fluorosilicate glass (FSG), LK, ELK, or ULK, the insulating layer 520 is silicon dioxide or fluorine doped silicon dioxide, and the insulating layer 540 is silicon dioxide or silicon nitride. The metal layer 530 couples through a top metal 506 to, for example, devices and back-end-of-line (BEOL) layers on a semiconductor layer 595. A passivation layer 550 on the

insulating layer 540 is patterned to create an opening 502. The opening 502 may be formed by, for example, depositing a photoresist layer (not shown), patterning the photoresist layer, wet or dry etching the passivation layer 550, and stripping the photoresist layer.

[0037] At block 415 a barrier layer is deposited. FIGURE 5B is a block diagram illustrating a wafer after deposition of a barrier layer according to the first embodiment. A barrier layer 560 is deposited on the passivation layer 550 and may be, for example, silicon dioxide, silicon nitride, silicon carbide, aluminum oxide, polytetrafluoroethylene, or other insulating materials. According to one embodiment, the barrier layer 560 is less than two micrometers in thickness.

[0038] At block 420 the barrier layer is patterned. The barrier layer may be patterned, for example, using a photoresist as a hard mark for etching. FIGURE 5C is a block diagram illustrating a wafer after deposition of a photoresist according to the first embodiment. A photoresist 570 is deposited on the barrier layer 560 and patterned to substantially align with the opening 502.

[0039] FIGURE 5D is a block diagram illustrating a wafer after etching of the barrier layer according to the first embodiment. A photoresist 570 acts as a hard mask during etching of the barrier layer 560 from the opening 502. The barrier layer 560 may be etched, for example, by wet or dry etching processes.

[0040] FIGURE 5E is a block diagram illustrating a wafer after stripping the photoresist according to the first embodiment. After etching the barrier layer 560 from the opening 502, the photoresist 570 is stripped from the remainder of the barrier layer 560.

[0041] At block 425 flip chip build up occurs to connect with the top metal layer. FIGURE 5F is a block diagram illustrating a wafer after flip chip build up according to the first embodiment. A bump 580 is deposited in the opening 502 for external connections to the metal layer 530. For example, the bump 580 may be used to couple external components to the metal layer 530.

[0042] An alternative process flow for depositing the passivation layer is illustrated with reference to FIGURE 6 and FIGURES 7A-F. FIGURE 6 is a flow chart illustrating an exemplary process flow for forming the barrier layer according to a second embodiment. At block 610 flip chip bump build up occurs. FIGURE 7A is a block diagram illustrating a wafer after flip chip bump build up according to the second embodiment. Insulating layers 710, 720, 740 surround a metal layer 730. A top metal

706 couples to the metal layer 730 to provide communication to, for example, vias, other metal layers and devices on a semiconductor layer 795. A passivation layer 750 on the insulating layer 740 provides compliance and may be, for example, polyimide or another polymer. A bump 760 connects through the passivation layer 750 to the metal layer 730 for coupling external components to the top metal 706. An under bump metallurgy (UBM) (not shown) may be deposited before the bump 760 to facilitate building of the bump 760.

[0043] At block 615 a barrier layer is deposited. FIGURE 7B is a block diagram illustrating a wafer after deposition of a barrier layer according to the second embodiment. A barrier layer 770 is deposited on the passivation layer 750 and the bump 760. The barrier layer 770 may be, for example, silicon dioxide, silicon nitride, silicon carbide, aluminum oxide, polytetrafluoroethylene, or other insulating materials. According to one embodiment, the barrier layer 770 is less than two micrometers in thickness.

[0044] At block 620 a sacrificial layer is deposited. FIGURE 7C is a block diagram illustrating a wafer after deposition of a sacrificial layer according to the second embodiment. A sacrificial layer 780, such as a photoresist, is deposited on the barrier layer 770. The sacrificial layer 780 may be spray coated such that the thickness of the sacrificial layer 780 on the bump 760 is thinner than the thickness of the sacrificial layer 780 is other regions.

[0045] At block 625 the sacrificial layer is etched back. FIGURE 7D is a block diagram illustrating a wafer after etch back of the sacrificial layer according to the second embodiment. The sacrificial layer 780 is etched back by, for example, wet or dry etching. After etch back, the barrier layer 770 is exposed on the bump 760. The sacrificial layer 780 remains in regions around the bump 760 because of a greater thickness.

[0046] At block 630 the barrier layer is patterned. FIGURE 7E is a block diagram illustrating a wafer after patterning of the barrier layer according to the second embodiment. The barrier layer 770 is patterned using, for example, dry or wet etch processes with the sacrificial layer 780 acting as a hard mask. In regions where the sacrificial layer 780 remains intact, the barrier layer 770 is left relatively unchanged. In regions where the sacrificial layer 780 was removed, the barrier layer 770 is etched away to expose the bump 760.

[0047] At block 635 the sacrificial layer is removed. FIGURE 7F is a block diagram illustrating a wafer after removal of the sacrificial layer according to the second embodiment. The sacrificial layer 780 is removed through, for example, wet or dry etch processes exposing the barrier layer 770. Substantially all of the passivation layer 750 is covered by the barrier layer 770. Thus, any glue attached to the passivation layer 750 is easier to remove due to modifications to the surface of the passivation layer 750 by the barrier layer 770, resulting in reduced adhesion.

[0048] A barrier layer as described above may be implemented in construction of a stacked IC. FIGURE 8 is a block diagram illustrating an exemplary stacked IC having a barrier layer according to one embodiment. A first tier die 850 is coupled to a second tier die 860 through an interconnect 862. Devices in the first tier die 850 include, for example, a transistor 842. The interconnect 862 couples to a through silicon via 846 in the first tier die 850 and interconnects 844. The interconnects 844 are surrounded by an insulating layer 840 such as, for example, LK, HLK, or ULK dielectrics. The interconnects 844 couple to a bump 824 to allow communication between the first tier die 850, the second tier die 860, and external components.

[0049] Deposited on the insulating layer 840 is a first passivation layer 830 and a second passivation layer 826. According to one embodiment, the first passivation layer 830 is silicon nitride, and the second passivation layer 826 is polyimide. A barrier layer 820 covers substantially all of the second passivation layer 826 to reduce residue left by a glue 816 after detachment of a carrier wafer 810. The carrier wafer 810 provides support for the first tier die 850 during processing, such as thinning the first tier die 850, to reduce fragility of the first tier die 850.

[0050] According to a third embodiment, a barrier layer is deposited and etched to reduce topography of a layer structure of a semiconductor wafer to reduce glue adhesion. Glue adhesion may be reduced through altering of structural properties. FIGURES 9A-9C are cross-sectional views illustrating barrier layer deposition and etching according to the third embodiment. FIGURE 10 is a flow chart illustrating an exemplary process flow for forming the barrier layer according to the third embodiment.

[0051] Referring to FIGURE 9A, film layers 904 of a layer structure 900 are located on a semiconductor layer 902. The film layers may include metal layers, top metal interconnects, insulating layers, vias, and passivation layers. On the film layers 904 is a passivation layer 906. Under bump metallurgy (UBM) 908 on the passivation layer 906 couples an interface structure 910 (e.g., bumps) to devices (not shown) on the

semiconductor layer 902 through vias and metal layers in the film layers 904. Large topography differences (e.g., height variation between the top of the bump 910 and a surface of the passivation layer 906) and access to locking regions 920 allow adhesives (not shown) deposited on the layer structure 900 to lock into the layer structure 900 increasing difficulty of removing the adhesive.

[0052] At block 1010 a barrier layer 912 is deposited on the layer structure 900 to substantially cover the bumps 910 and the passivation layer 906 as shown in FIGURE 9B. The barrier layer 912 may be, for example, silicon nitride, an organic film, or an epoxy.

[0053] At block 1020, the barrier layer 912 is etched back as shown in FIGURE 9C. The etching may include a photoresist deposition and patterning process. The barrier layer 912 is etched back and results in a reduced topography and reduced exposure of locking regions 920 of the layer structure 900. After etching, the barrier layer 912 has a substantially flat surface. The reduced topography prevents an adhesive deposited on the layer structure 900 from locking into the bumps 910. That is, adhesion is reduced through altering of structural properties of the layer structure 900.

[0054] The layer structure 900 of FIGURE 9C may be stacked with other semiconductor wafers by depositing an adhesive, attaching a carrier wafer, thinning the layer structure 900, processing the layer structure 900, attaching a second tier die, and detaching the carrier wafer by dissolving the adhesive. The barrier layer 912 reduces adhesion of the adhesive layer to the layer structure 900 allowing removal of the adhesive without any residue remaining on the layer structure 900. The barrier layer 912 may be removed through wet and/or dry etching after the adhesive is dissolved.

[0055] According to one embodiment, an additional barrier layer (not shown) may be deposited between the barrier layer 912 and the passivation layer 906. The additional barrier layer may be deposited according to the first and/or second embodiments described above.

[0056] A barrier layer deposited over a passivation layer decreases residue of glues attached to the passivation layer by decreasing adhesion of glue to the passivation layer. Inorganic materials may be chosen for the barrier layer because inorganic materials have increased resistance to plasma and chemical processes, which increase surface roughness of other materials. Decreased surface roughness further reduces adhesion of glues to the passivation layer. The barrier layer is used in one

embodiment during construction of stacked ICs to reduce glue residue remaining after detachment of a carrier wafer.

[0057] FIGURE 11 shows an exemplary wireless communication system 1100 in which an embodiment of the disclosure may be advantageously employed. For purposes of illustration, FIGURE 11 shows three remote units 1120, 1130, and 1150 and two base stations 1140. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 1120, 1130, and 1150 include improved packaged ICs 1125A, 1125C, and 1125B, respectively, which are embodiments as discussed above. FIGURE 10 shows forward link signals 1180 from the base stations 1140 and the remote units 1120, 1130, and 1150 and reverse link signals 1190 from the remote units 1120, 1130, and 1150 to base stations 1140.

[0058] In FIGURE 11, remote unit 1120 is shown as a mobile telephone, remote unit 1130 is shown as a portable computer, and remote unit 1150 is shown as a computer in a wireless local loop system. For example, the remote units may be cell phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, fixed location data units such as meter reading equipment, set top boxes, music players, video players, entertainment units, navigation devices, or computers. Although FIGURE 11 illustrates remote units according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. The disclosure may be suitably employed in any device which includes packaged ICs.

[0059] FIGURE 12 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component as disclosed below. A design workstation 1200 includes a hard disk 1201 containing operating system software, support files, and design software such as Cadence or OrCAD. The design workstation 1200 also includes a display to facilitate design of a circuit 1210 or a semiconductor component 1212 such as a wafer or die. A storage medium 1204 is provided for tangibly storing the circuit design 1210 or the semiconductor component 1212. The circuit design 1210 or the semiconductor component 1212 may be stored on the storage medium 1204 in a file format such as GDSII or GERBER. The storage medium 1204 may be a CD-ROM, DVD, hard disk, flash memory, or other appropriate device. Furthermore, the design workstation 1200 includes a drive apparatus 1203 for accepting input from or writing output to the storage medium 1204.

[0060] Data recorded on the storage medium 1204 may specify logic circuit configurations, pattern data for photolithography masks, or mask pattern data for serial write tools such as electron beam lithography. The data may further include logic verification data such as timing diagrams or net circuits associated with logic simulations. Providing data on the storage medium 1204 facilitates the design of the circuit design 1210 or the semiconductor component 1212 by decreasing the number of processes for designing semiconductor wafers.

[0061] The methodologies described herein may be implemented by various components depending upon the application. For example, these methodologies may be implemented in hardware, firmware, software, or any combination thereof. For a hardware implementation, the processing units may be implemented within one or more application specific integrated circuits (ASICs), digital signal processors (DSPs), digital signal processing devices (DSPDs), programmable logic devices (PLDs), field programmable gate arrays (FPGAs), processors, controllers, micro-controllers, microprocessors, electronic devices, other electronic units designed to perform the functions described herein, or a combination thereof.

[0062] For a firmware and/or software implementation, the methodologies may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. Any machine-readable medium tangibly embodying instructions may be used in implementing the methodologies described herein. For example, software codes may be stored in a memory and executed by a processor unit. Memory may be implemented within the processor unit or external to the processor unit. As used herein the term "memory" refers to any type of long term, short term, volatile, nonvolatile, or other memory and is not to be limited to any particular type of memory or number of memories, or type of media upon which memory is stored.

[0063] If implemented in firmware and/or software, the functions may be stored as one or more instructions or code on a computer-readable medium. Examples include computer-readable media encoded with a data structure and computer-readable media encoded with a computer program. Computer-readable media includes physical computer storage media. A storage medium may be any available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium

that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer; disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0064] In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.

[0065] Although the terminology "through silicon via" includes the word silicon, it is noted that through silicon vias are not necessarily constructed in silicon. Rather, the material can be any device substrate material.

[0066] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the technology of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. A layer structure for a semiconductor die, comprising:

an insulating layer of the semiconductor die;

a passivation layer on the insulating layer that provides compliance for the semiconductor die; and

a barrier layer on the passivation layer that reduces adhesion of glues applied during semiconductor manufacturing to the passivation layer.

2. The layer structure of claim 1, in which the barrier layer is at least one of silicon dioxide, silicon nitride, silicon carbide, polytetrafluoroethylene, organic materials, and epoxy.

3. The layer structure of claim 1, in which the barrier layer modifies chemical properties of the passivation layer to reduce adhesion.

4. The layer structure of claim 1, in which the barrier layer modifies structural properties of the passivation layer

5. The layer structure of claim 1, integrated into a stacked integrated circuit.

6. The layer structure of claim 1, integrated into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

7. A semiconductor manufacturing process, comprising:

patterning a passivation layer of a semiconductor die;

depositing a barrier layer on the passivation layer that reduces adhesion of glues applied during the semiconductor manufacturing process to the passivation layer; and

patterning the barrier layer.

8. The semiconductor manufacturing process of claim 7, further comprising building up an interconnect after patterning the barrier layer.

9. The semiconductor manufacturing process of claim 7, in which depositing the barrier layer comprises depositing at least one of silicon dioxide, silicon nitride, silicon carbide, and polytetrafluoroethylene.

10. The semiconductor manufacturing process of claim 7, in which depositing the barrier layer comprises depositing less than two micrometers of the barrier layer.

11. The semiconductor manufacturing process of claim 7, in which patterning the barrier layer comprises:

depositing a photoresist;

patterning the photoresist;

etching the barrier layer after patterning the photoresist; and

removing the photoresist after etching the barrier layer.

12. The semiconductor manufacturing process of claim 7, in which the semiconductor manufacturing process is integrated into the manufacturing of stacked integrated circuits.

13. A semiconductor manufacturing process, comprising:

building up a flip chip bump;

depositing a barrier layer after building up the flip chip bump; and

patterning the barrier layer to expose the flip chip bump.

14. The semiconductor manufacturing process of claim 13, in which patterning the barrier layer comprises:

depositing a sacrificial layer;

etching back the sacrificial layer;

etching the barrier layer after etching back the sacrificial layer; and

removing the sacrificial layer after etching the barrier layer.

15. The semiconductor manufacturing process of claim 13, in which depositing the barrier layer comprises depositing at least one of silicon dioxide, silicon nitride, silicon carbide, and polytetrafluoroethylene.

16. The semiconductor manufacturing process of claim 13, in which depositing the barrier layer comprises depositing less than two micrometers of the barrier layer.

17. A layer structure for a semiconductor die, comprising:

an insulator layer of the semiconductor die;

a passivation layer on the insulator layer; and

means for modifying a surface to decrease adhesion, the surface modifying means disposed on the passivation layer.

18. The layer structure of claim 17, in which the surface modifying means comprises means for altering structural properties of the passivation layer.

19. The layer structure of claim 17, in which the surface modifying means comprises means for altering chemical properties of the passivation layer.

20. The layer structure of claim 17, further comprising an integrated circuit, the insulator layer disposed on the integrated circuit.

21. The layer structure of claim 20, integrated into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

22. A semiconductor manufacturing process, comprising:

depositing a barrier layer on a semiconductor die to substantially cover an interface structure of the semiconductor die and to substantially cover a passivation layer of the semiconductor die; and

etching the barrier layer to create a surface having reduced topography.

23. The semiconductor manufacturing process of claim 22, further comprising integrated the semiconductor die into the manufacturing of stacked integrated circuits.

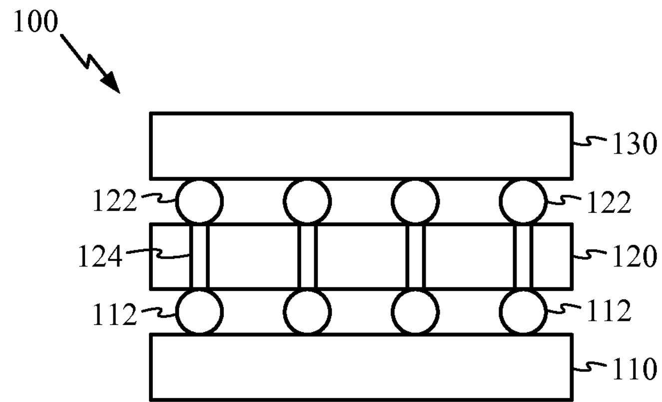
24. A semiconductor manufacturing process, comprising the steps of:

patterning a passivation layer of a semiconductor die;

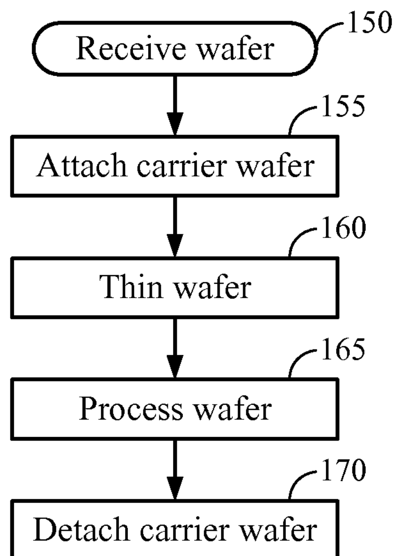
depositing a barrier layer on the passivation layer that reduces adhesion of glues applied during the semiconductor manufacturing process to the passivation layer; and

patterning the barrier layer.

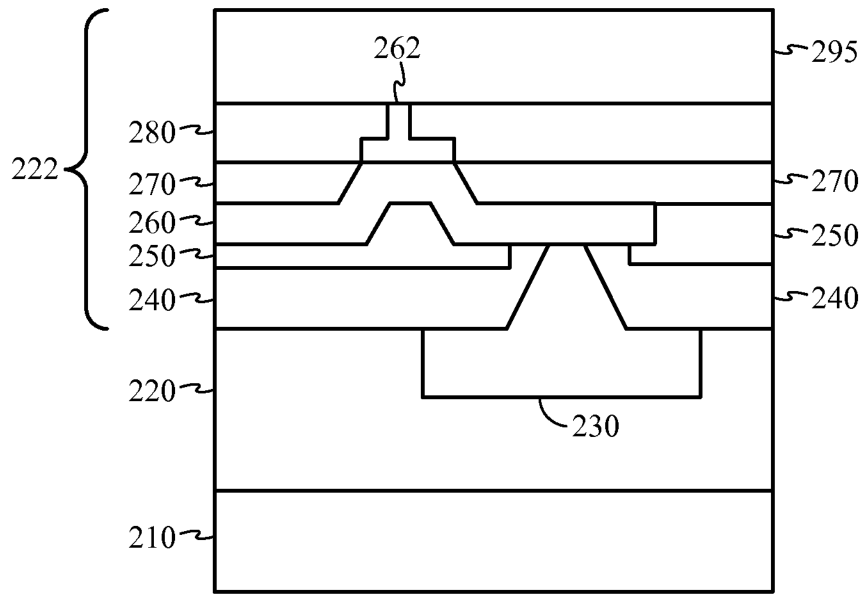
25. The semiconductor manufacturing process of claim 24, further comprising integrated the semiconductor die into the manufacturing of stacked integrated circuits.



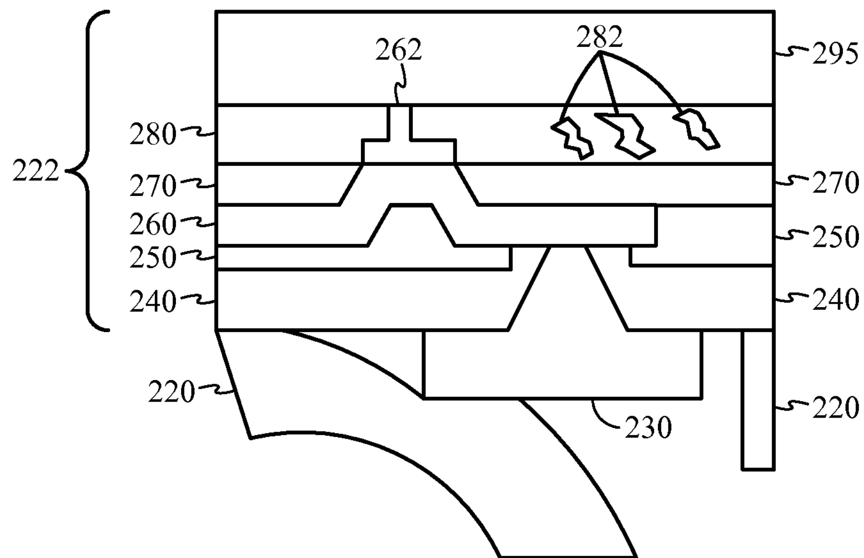
(PRIOR ART)
FIG. 1A



(PRIOR ART)
FIG. 1B



(PRIOR ART)
FIG. 2A



(PRIOR ART)
FIG. 2B

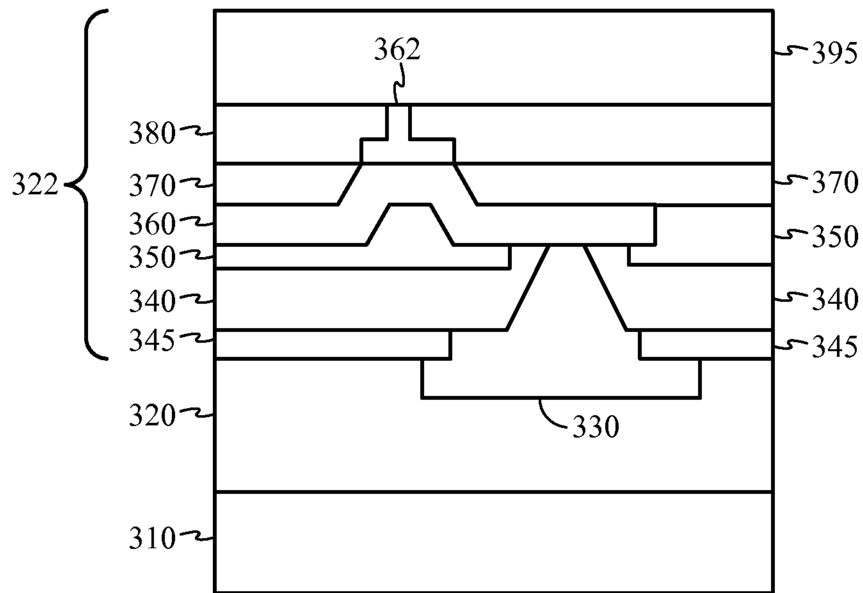


FIG. 3A

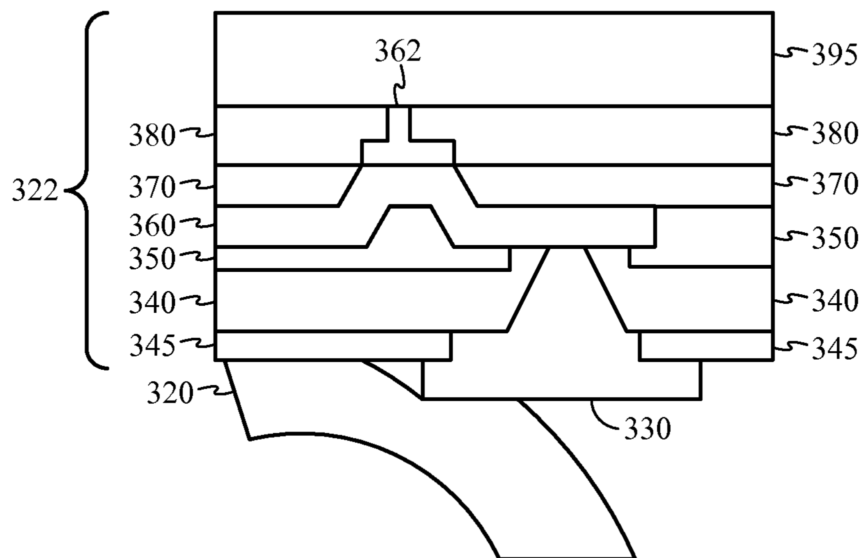


FIG. 3B

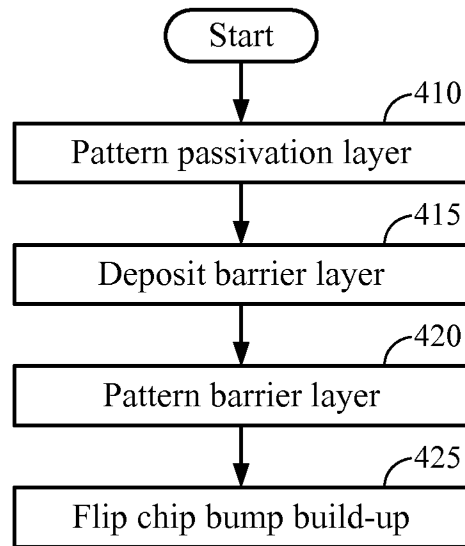


FIG. 4

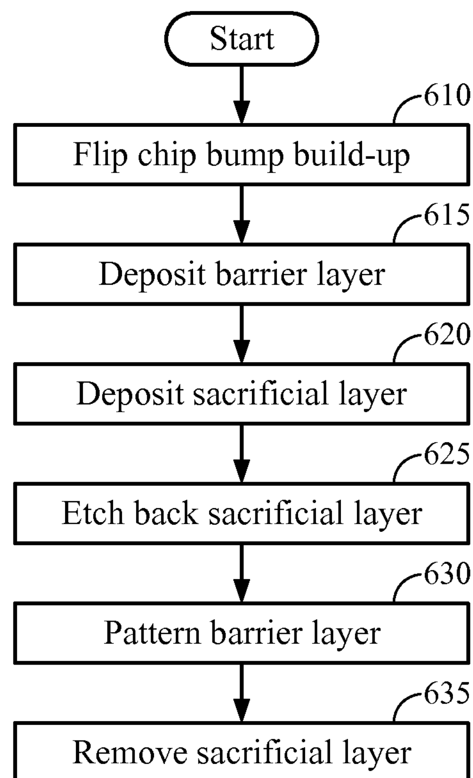


FIG. 6

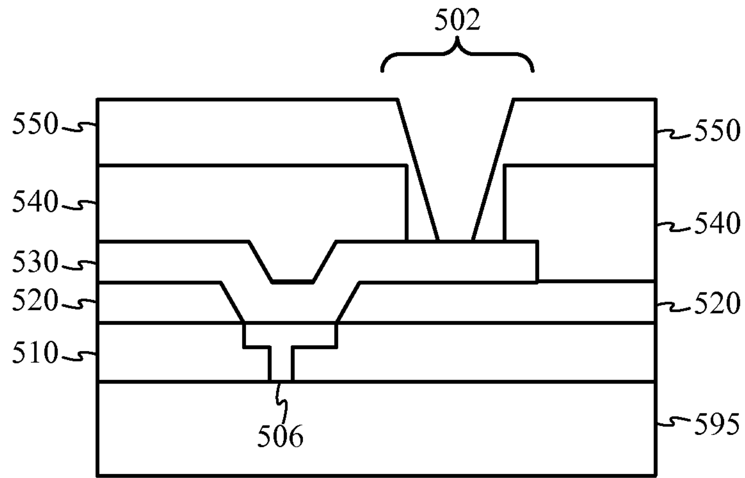


FIG. 5A

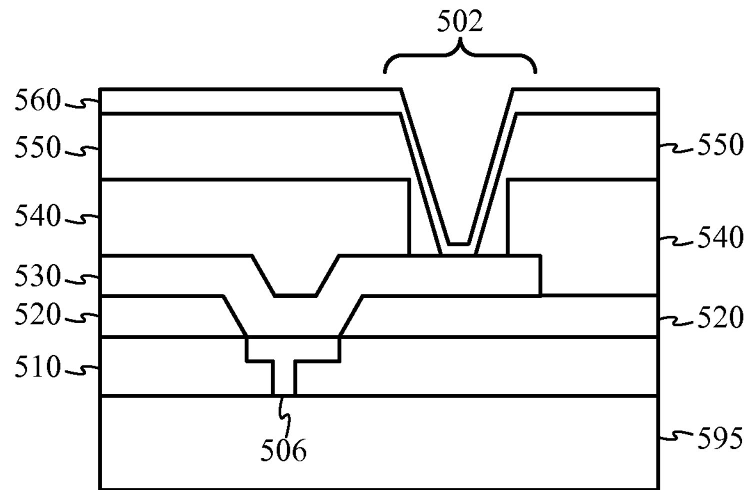


FIG. 5B

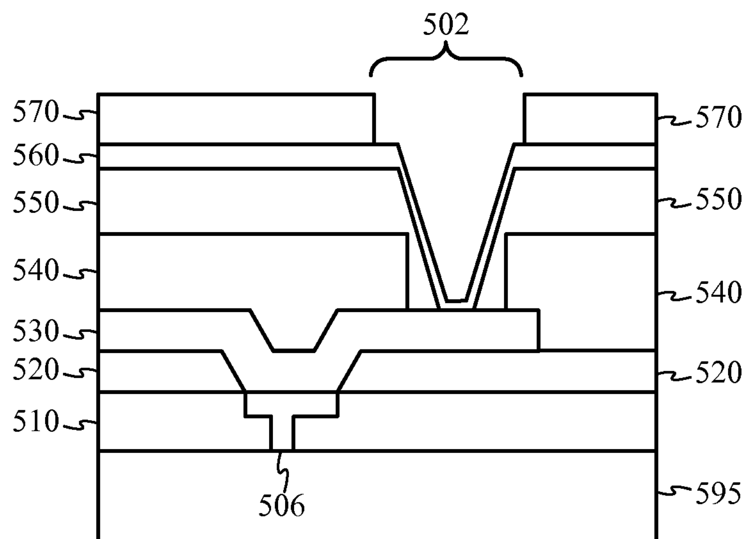


FIG. 5C

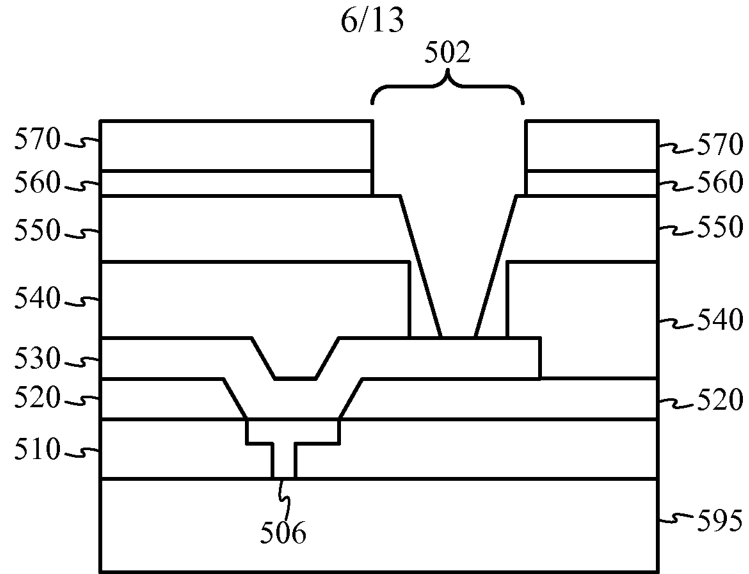


FIG. 5D

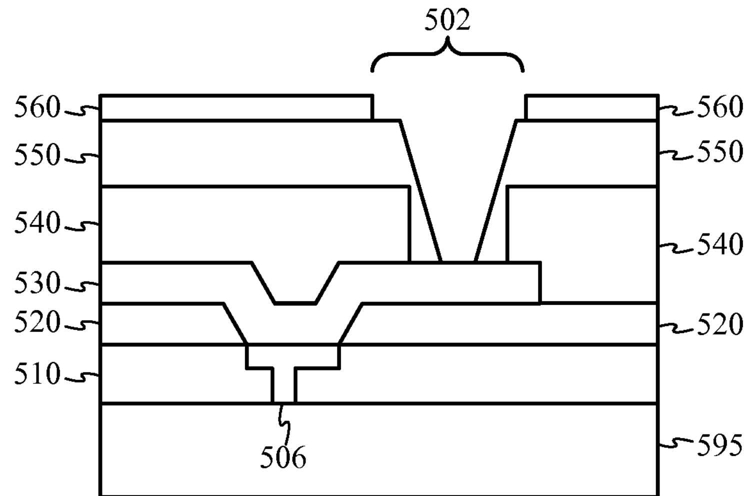


FIG. 5E

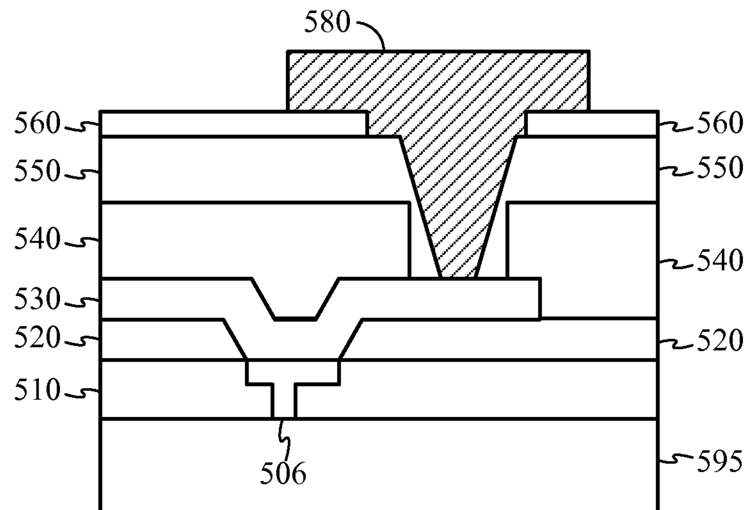


FIG. 5F

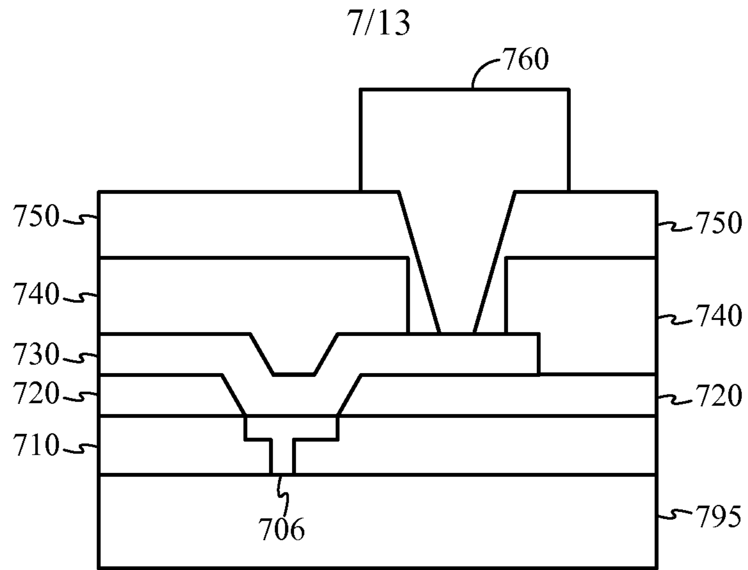


FIG. 7A

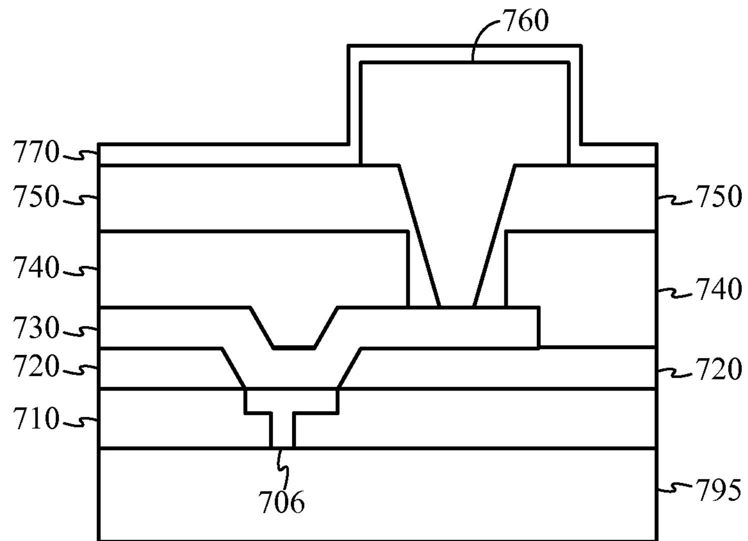


FIG. 7B

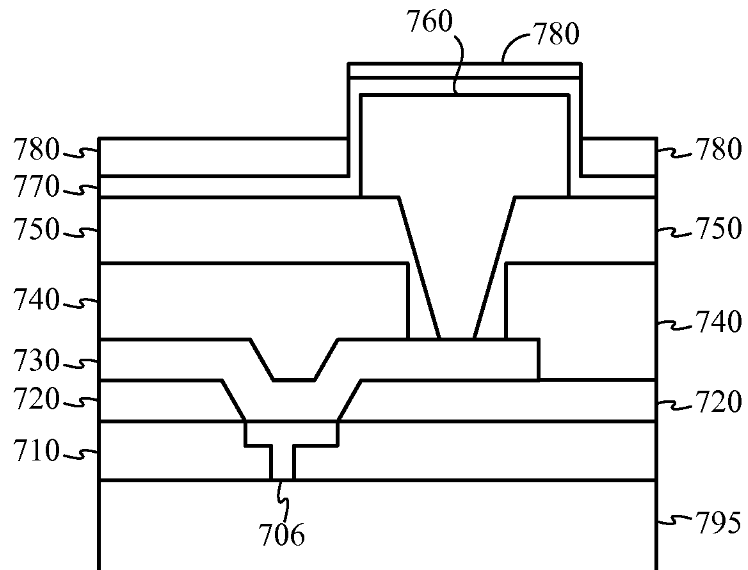


FIG. 7C

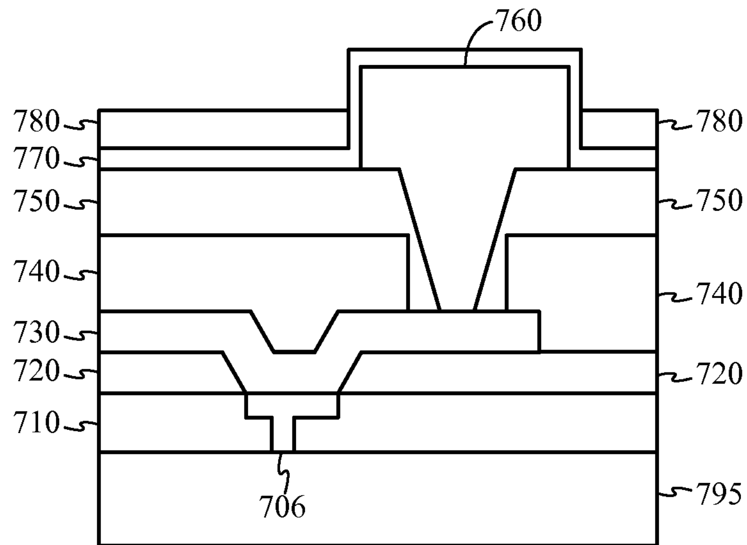


FIG. 7D

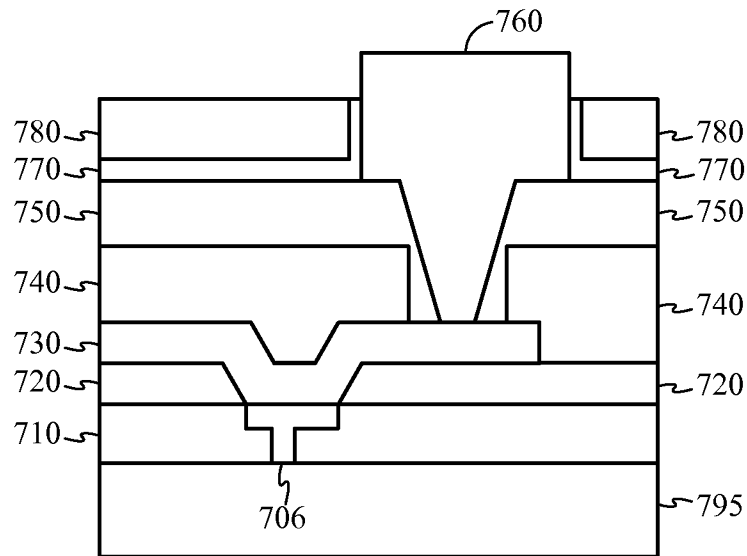


FIG. 7E

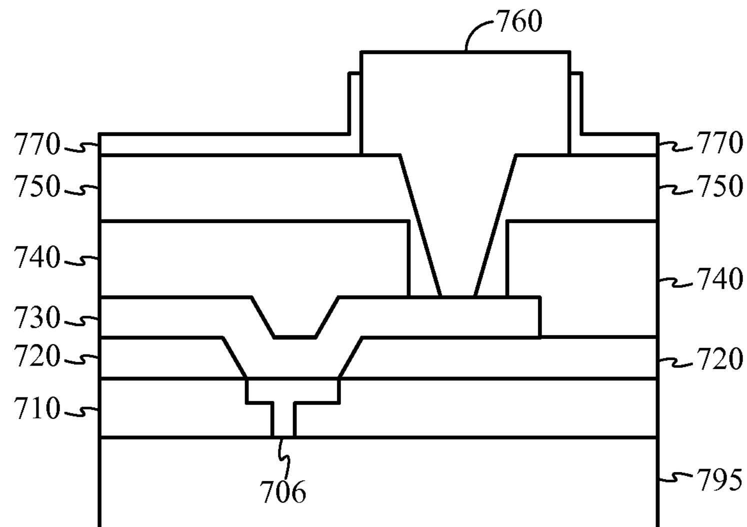


FIG. 7F

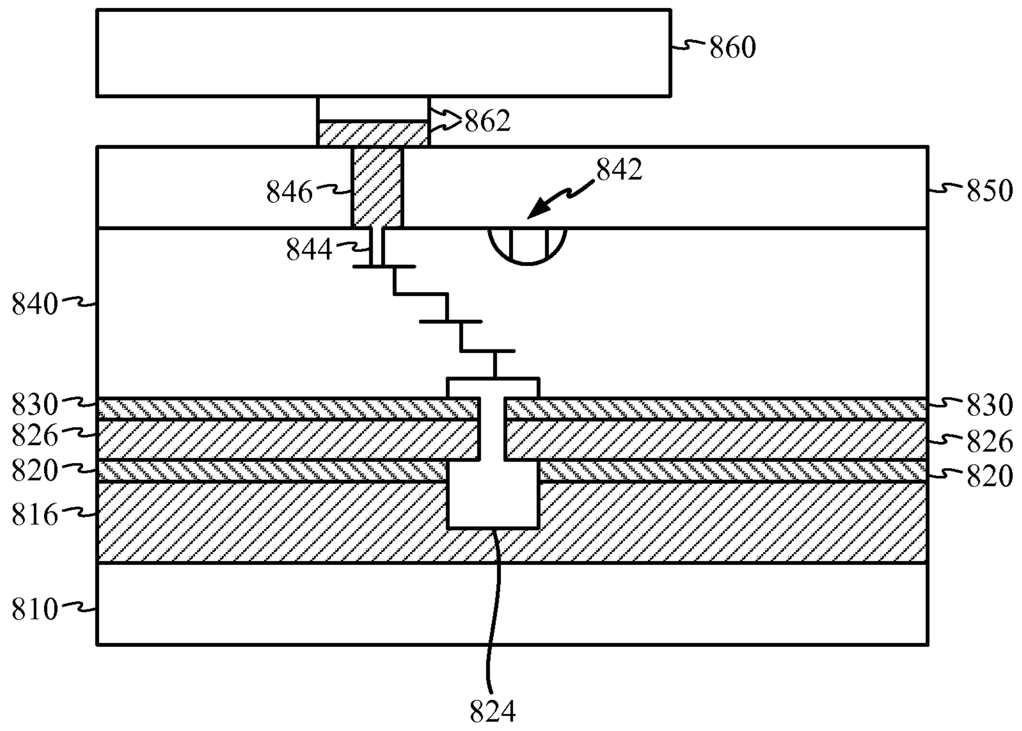


FIG. 8

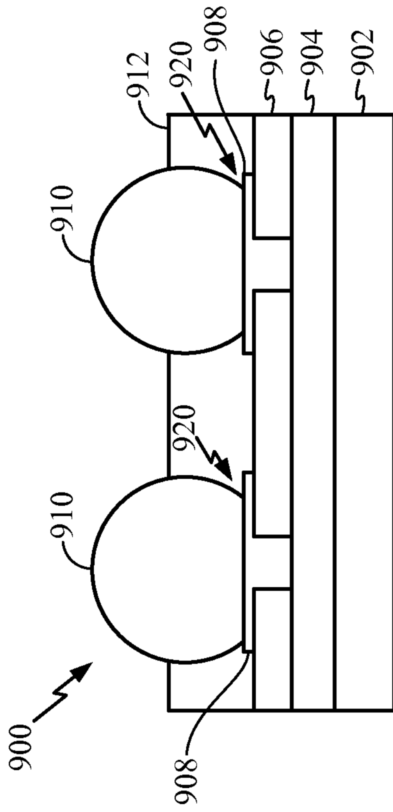


FIG. 9C

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FIG. 9A

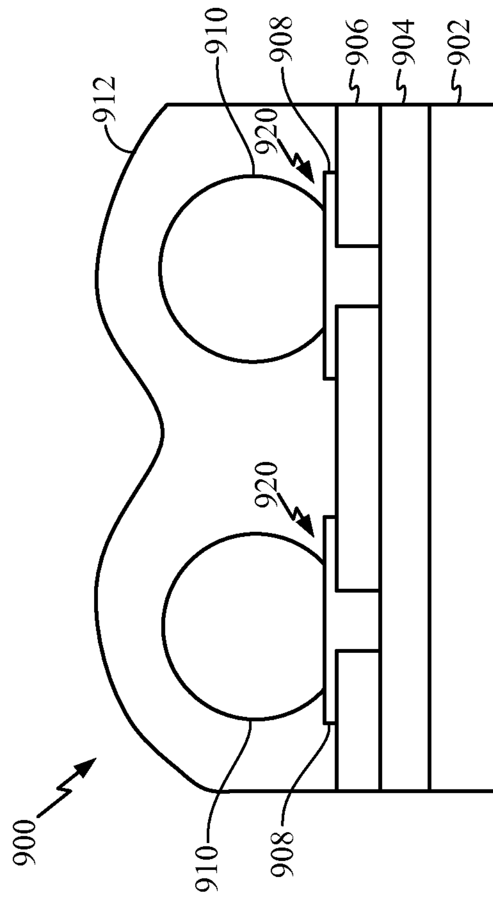

FIG. 9B

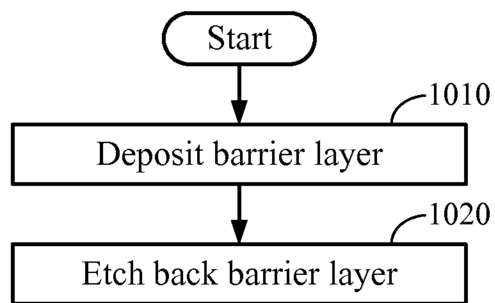

FIG. 10

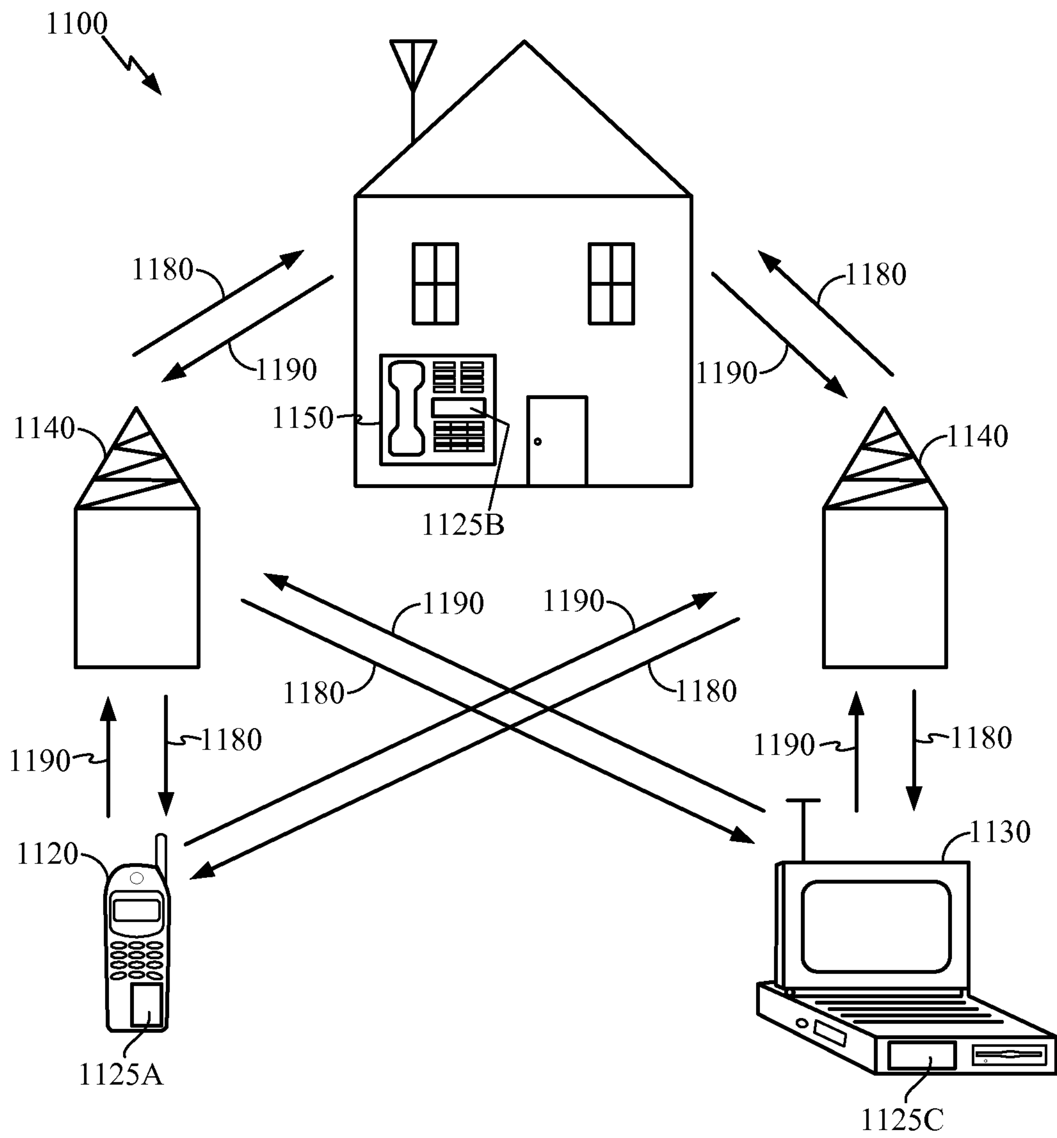

FIG. 11

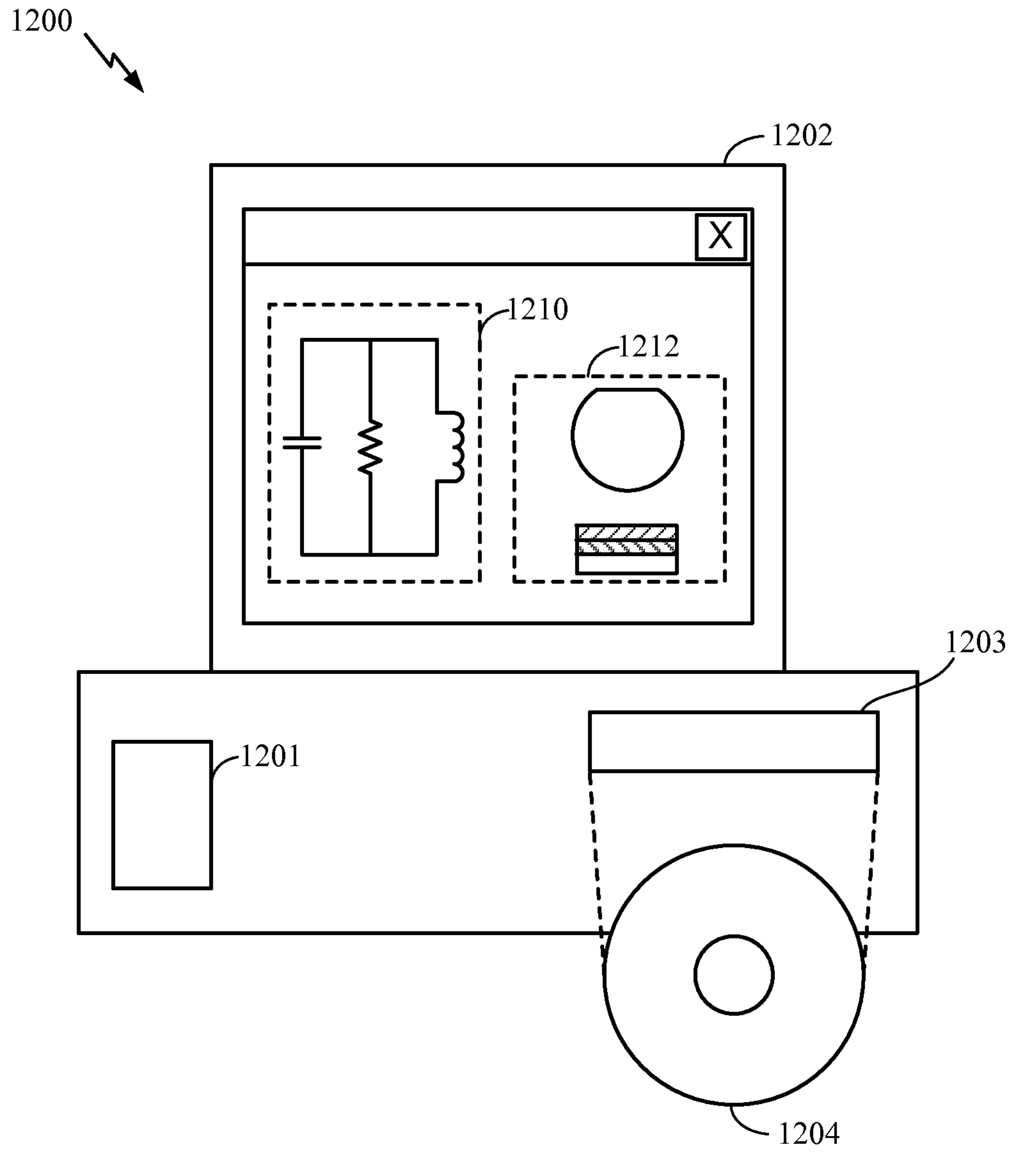

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/042310

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/31 H01L21/68
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/166464 A1 (JAKOB ANDREAS [DE] ET AL) 27 July 2006 (2006-07-27)	1-3,5,6, 17,19-21
Y	paragraphs [0013], [125] - [0130]; figures 1-4 paragraphs [0187] - [0191]; figures 16,17	7-12,24, 25
Y	US 2006/284285 A1 (FUKAZAWA MOTOHIKO [JP]) 21 December 2006 (2006-12-21) paragraphs [0119] - [0157]; figures 2A-C	7-12,24, 25
X	US 2005/221598 A1 (LU DAOQIANG [US] ET AL LU DAOQIANG [US] ET AL) 6 October 2005 (2005-10-06) paragraphs [0016] - [0036]; figures 1-9	1-3,5-7, 17, 19-21,24
A	US 4 907 039 A (CHIKAKI SHINICHI [JP]) 6 March 1990 (1990-03-06) the whole document	1,2,7,9

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 December 2010	27/12/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Edmeades, Michael

Form PCT/ISA/210 (second sheet) (April 2005)

International application No
PCT/US2010/042310

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/166525 A1 (SWINNEN BART [BE] ET AL) 10 July 2008 (2008-07-10) paragraphs [0025] - [0062]; figures 4A,B	1,7,17
A	US 5 851 664 A (BENNETT RICHARD E [US] ET AL) 22 December 1998 (1998-12-22) the whole document	1,7,17
X	US 6 338 980 B1 (SATOH TETSUO [JP]) 15 January 2002 (2002-01-15) column 6, line 50 - column 8, line 14; figures 2-10	4,18,22, 23
A	US 2004/104272 A1 (FIGUET CHRISTOPHE [FR] ET AL) 3 June 2004 (2004-06-03) paragraphs [0034], [0055] - [0064]; figures 1a-D	4,18,22, 23
X	US 5 956 605 A (AKRAM SALMAN [US] ET AL) 21 September 1999 (1999-09-21) column 6, lines 19-67; figures 1-3	13-16
X	US 2007/090156 A1 (RAMANATHAN LAKSHMI N [US] ET AL) 26 April 2007 (2007-04-26) paragraphs [0031] - [0039]; figures 14-17	13-16
X	US 2005/167799 A1 (DOAN TRUNG T [US]) 4 August 2005 (2005-08-04) paragraphs [0032] - [0046]; figures 2-10	13
A	US 2007/293033 A1 (HILL DARRELL G [US] ET AL) 20 December 2007 (2007-12-20) columns 30-33; figures 7-11	13-16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/042310

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. [ ] Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. [ ] Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. [ ] Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. [X] As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. [ ] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

[ ] The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

[ ] The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

[X] No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/042310

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
US 2006166464	A1	27-07-2006	AU	2003299296	A1	23-06-2004
			WO	2004051708	A2	17-06-2004
			EP	1568071	A2	31-08-2005
			JP	2006508540	T	09-03-2006
			KR	20050075037	A	19-07-2005
			US	2009176349	A1	09-07-2009
US 2006284285	A1	21-12-2006	JP	4544143	B2	15-09-2010
			JP	2007027675	A	01-02-2007
			KR	20060132450	A	21-12-2006
US 2005221598	A1	06-10-2005	NONE			
US 4907039	A	06-03-1990	JP	1004050	A	09-01-1989
			JP	1963487	C	25-08-1995
			JP	6095517	B	24-11-1994
US 2008166525	A1	10-07-2008	NONE			
US 5851664	A	22-12-1998	AU	703233	B2	18-03-1999
			AU	6177596	A	10-02-1997
			CA	2224774	A1	30-01-1997
			CN	1195424	A	07-10-1998
			DE	69601942	D1	06-05-1999
			DE	69601942	T2	11-11-1999
			EP	0838086	A1	29-04-1998
			JP	3643600	B2	27-04-2005
			JP	11508924	T	03-08-1999
			WO	9703461	A1	30-01-1997
US 6338980	B1	15-01-2002	TW	510030	B	11-11-2002
US 2004104272	A1	03-06-2004	AT	301332	T	15-08-2005
			CN	1513204	A	14-07-2004
			DE	60205358	D1	08-09-2005
			DE	60205358	T2	06-07-2006
			EP	1386346	A2	04-02-2004
			FR	2823012	A1	04-10-2002
			WO	02082502	A2	17-10-2002
			JP	4249490	B2	02-04-2009
			JP	2004526323	T	26-08-2004
			TW	255486	B	21-05-2006
US 5956605	A	21-09-1999	US	6528894	B1	04-03-2003
US 2007090156	A1	26-04-2007	CN	101356634	A	28-01-2009
US 2007090156	A1		JP	2009514228	T	02-04-2009
			KR	20080059590	A	30-06-2008
			WO	2007050471	A2	03-05-2007
US 2005167799	A1	04-08-2005	US	2006197190	A1	07-09-2006
			US	2010102433	A1	29-04-2010
US 2007293033	A1	20-12-2007	WO	2007146478	A1	21-12-2007

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-3, 5-12, 17, 19-21, 24, 25

   Device and corresponding method in which the choice of material of the barrier layer above a semiconductor die having a passivation layer modifies the adhesion properties of an (unspecified) glue that is to be provided to adhesively bond the die to a (unspecified) temporary substrate

   ---

2. claims: 4, 18, 22, 23

   Device and corresponding method in which the surface topography of the barrier layer above a semiconductor die having a passivation layer modifies the adhesion properties of an (unspecified) glue that is to be provided to adhesively bond the die to a (unspecified) temporary substrate

   ---

3. claims: 13-16

   Method of forming a flip-chip device with bump with the step of patterning a barrier layer

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