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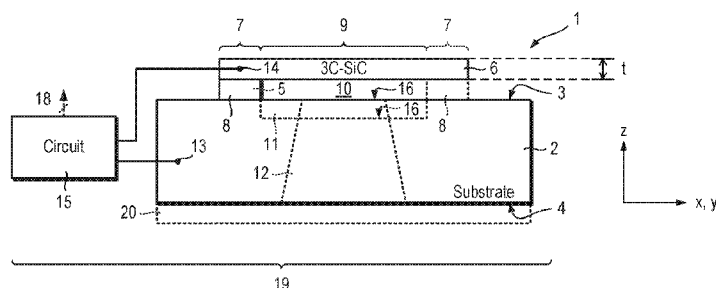


Fig. 1

(57) Abstract: A sensor is disclosed. The sensor comprises a substrate (2) and a layer (6) of monocrystalline 3C-SiC supported by the substrate. The substrate may consist of silicon SiC. The monocrystalline 3C-SiC layer may comprise at least one fixed region (7), for example which is directly supported by the substrate, and at least one suspended region (9).

3C-SiC based sensor

Field of the Invention

The present invention relates to a 3C-SiC based sensor, such as a pressure sensor, and
5 to a monolithic integrated sensor including a 3C-SiC based sensor.

Background

Silicon carbide is wide-bandgap compound semiconductor material which is well suited
to being used in high-power and high-frequency electronic devices on account of having
10 high values of thermal conductivity, breakdown field and saturation velocity.

Silicon carbide exists in several different crystal forms (or “polytypes”) depending on
the sequence in which bi-layers of silicon and carbon stack. Of these polytypes, 3C-
silicon carbide (3C-SiC), 4H-silicon carbide (4H-SiC) and 6H-silicon carbide (6H-SiC)
15 are most commonly used in electronic devices.

4H- and 6H-SiC substrates are commercially available and high-quality homoepitaxial
layers of 4H- and 6H-SiC can be grown on these types of substrates. However, 4H- and
6H-SiC substrates are much more expensive to produce than silicon substrates and are
20 much smaller.

Although 3C-SiC substrates are not available, heteroepitaxial 3C-SiC can be grown on
silicon. This allows larger, cheaper silicon wafers to be used. Currently, however, hot-
wall chemical vapour deposition (CVD) reactors are used to grow 3C-SiC epitaxial
25 layers on silicon. High-temperature cold-wall CVD reactors have purportedly been
used to grow 3C-SiC epitaxial layers on silicon, although it is unclear how temperatures
exceeding 1,300°C can be achieved in such reactors without damaging the reactor or
component lying inside the reactor.

Moreover, most, if not all, of the research into 3C-SiC/Si heteroepitaxy tends to be
conducted on small substrates, such as 50 mm-diameter wafers or 10 mm dies. This
can give a misleading impression of whether or not a given heteroepitaxial process has
been successful and suitable for production since it is easier to achieve a uniform
temperature across a small substrate. Thus, small heterostructures may not reveal
35 problems regarding lack of uniformity across the wafer, voiding, and wafer bow.

For example, R. Anzalone *et al.*: “Heteroepitaxy of 3C-SiC on different on-axis oriented silicon substrates”, Journal of Applied Physics, volume 105, page 084910 (2009) describes growing epitaxial films on 2-inch silicon wafers in a hot-wall, low-pressure chemical vapour (LPCVD) reactor using trichlorosilane (SiHCl_3) as a silicon supply, ethylene (C_2H_4) as a carbon supply and hydrogen (H_2) as a carrier gas at a growth temperature of 1350 °C. A hot-wall CVD reactor tends to have a low throughput and requires regular, costly maintenance.

Wei-Yu Chen *et al.*: “Crystal Quality of 3C-SiC Influenced by the Diffusion Step in the Modified Four-Step Method”, Journal of The Electrochemical Society, volume 157, pages H377-H380 (2010) describes growing epitaxial films on 1 cm × cm substrate in a horizontal, cold-wall-type LPCVD system using silane (SiH_4) as a silicon supply, propane (C_3H_8) as a carbon supply and hydrogen (H_2) as a carrier gas at a growth temperature of 1420 °C. Although a cold-wall reactor is used, a complex 3- or 4-step deposition process is used, employing temperatures which are close to melting point of silicon. However, it is unclear if the process is repeatable, can be achieved without damaging the chamber and components inside the chamber, and can be used to produce high volumes of large-diameter wafers.

Y. Gao *et al.*: “Low-temperature chemical-vapor deposition of 3C-SiC films on Si(100) using SiH_4 - C_2H_4 - HCl - H_2 ”, Journal of Crystal Growth, volume 191, pages 439 to 445 (1998) describes deposition of 3C-SiC films on silicon using HCl to suppress pure silicon nucleation. The paper, however, omits several details, such as wafer offcut and size, and does not mention whether the substrate suffers from warp or bow after deposition. Furthermore, the SiC films appear to be very rough. From micrographs shown in the paper, RMS surface roughness values of SiC films appear to be several hundreds of nanometres. Moreover, although using a higher concentration of HCl appears to improve crystal quality, it reduces growth rate and if HCl is omitted, then the SiC films are polycrystalline.

Summary

The present invention seeks to provide a 3C-SiC based sensor.

According to a first aspect of the present invention there is provided a sensor
5 comprising a substrate and a 3C-SiC layer which is monocrystalline which is supported
by the substrate. The 3C-SiC layer may comprise at least one fixed region and at least
one fixed suspended region.

The substrate may be a silicon or silicon-on-insulator substrate. The substrate may be
10 a silicon carbide substrate.

A first fixed region of the 3C-SiC layer may be directly supported by the substrate. The
sensor may further comprise an intermediate layer, which is supported by the
substrate, and a second fixed region of the 3C-SiC layer may be directly supported by
15 the intermediate layer.

The second may further comprise an intermediate layer which is supported by the
substrate and a first fixed region of the 3C-SiC layer may be directly supported by the
intermediate layer.

20 The substrate has first and second opposite surfaces and the 3C-SiC layer may be
supported on the first surface. The sensor may comprise another 3C-SiC layer
supported on the second surface. This can be used to help avoid substrate bow and
warp. The sensor may comprise a window passing through the substrate between the
25 first and second opposite surfaces of the substrate.

The sensor may comprise a housing forming a sealed cavity and a first unsupported
region of the 3C-SiC layer may form a deformable portion of the housing. This type of
sensor can be used as a pressure sensor.

30 A first unsupported region of the 3C-SiC layer may comprise a wire or mesh. A first
unsupported region of the 3C-Si layer or the first unsupported region of the 3C-Si layer
may comprise a cantilever.

35 The sensor preferably comprises a first electrode supported by the substrate. The first
electrode is preferably fixed, i.e. does not move. The first electrode may comprise a

conductive layer or region. The conductive layer or region may comprise a doped layer or region of semiconductor material. The conductive layer or region may comprise a metallization layer or region.

- 5 The sensor preferably comprises a second electrode supported by the SiC layer. The second electrode may be displaceable with respect to the substrate. The second electrode may comprise a conductive layer or region. The conductive layer or region may comprise a doped layer or region of semiconductor material. The conductive layer or region may comprise a metallization layer or region.

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The sensor may include one or more dielectric layers comprising, for example, AlN or Al₂O₃.

The sensor is preferably a pressure sensor.

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The sensor may further comprise a dielectric layer disposed on the SiC layer and a conductive layer disposed on the dielectric layer. The sensor may further comprise a functional layer overlying the conductive layer or the conductive layer may be functionalised, e.g. so as to selectively absorb a particular gas species.

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The sensor may be a gas sensor.

- According to a second aspect of the present invention there is provided a sensor comprising a 3C-SiC substrate and a Si layer which is monocrystalline and which is supported by the substrate. The Si layer may comprise at least one fixed region and at least one fixed suspended region.

25

- According to a third aspect of the present invention there is provided a monolithic integrated sensor comprising a sensor according to first or second aspect and a circuit which is coupled to the sensor and which is formed (i.e. disposed) in and/or the substrate.

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- According to a fourth aspect of the present invention there is provided a method of fabricating a sensor. The method comprises providing a sensor substrate and providing a monocrystalline 3C-SiC layer on the substrate. Providing the 3C-SiC layer comprises forming the 3C-SiC layer by growing epitaxial 3C-SiC on single-crystal silicon. The

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method comprises providing a single-crystal substrate (such as single-crystal silicon wafer or a silicon-on-insulator wafer) in a cold-wall chemical vapour deposition reactor. The method comprises heating the substrate to a temperature equal to or greater than 700 °C and equal to or less than 1200 °C and introducing a gas mixture
5 into the reactor, while the substrate is at the temperature, so as to deposit an epitaxial layer of 3C-SiC on the single-crystal silicon. The gas mixture comprises a silicon source precursor, a carbon source precursor and a carrier gas. The method may further comprise processing the substrate, layers on the substrate and/or the 3C-SiC layer (for example, by forming mask(s) and etching) such that the 3C-SiC layer comprises at least
10 one fixed region and at least one suspended region.

The monocrystalline silicon substrate may be the sensor substrate. Alternatively, the monocrystalline silicon substrate may be a handle substrate and providing the 3C-SiC layer on the substrate may comprise bonding the 3C-SiC layer and the sensor substrate
15 and. The method may comprise, thereafter, removing the handle substrate, for example, by etching.

The method may comprise providing more than one 3C-SiC layer. The method may comprise providing electrode regions.
20

The method may further comprise providing transistors in and/or on the sensor substrate so as to form a monolithic integrated circuit.

The 3C-SiC growth rate may be at least 1 µm/h. The growth rate may be at least 10
25 µm/h. The growth rate may be up to 20 µm/h or more. However, lower growth rates can be used, for example, to grow thin layers (e.g. < 100 nm) of 3C-SiC.

The carbon source precursor may be an organosilicon compound. The carbon source precursor may be a methyl-containing silane. Preferably, the carbon source precursor
30 is trimethylsilane (C₃H₉Si).

The silicon source precursor and carbon source precursor are preferably different, i.e. a single precursor serving as both silicon and carbon sources is not used.

35 The carbon source precursor may have a flow rate of at least 1 sccm or at least 10 sccm.

The silicon source precursor may be a silane, or a chlorine-containing silane.

Preferably, the silicon source precursor is dichlorosilane (SiH_2Cl_2). The silicon source precursor may be trichlorosilane. The silicon source precursor may comprise first and second precursor components. For example, the silicon source precursor may comprise
5 a mixture of gases, such as silane or disilane and hydrogen chloride (HCl).

The silicon source precursor may have a flow rate of at least 1 sccm or at least 10 sccm.

The carrier gas is preferably hydrogen (H_2).

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The carrier gas may have a flow rate of at least 1 sccm or at least 10 sccm.

The ratio of the flow rate of the carbon source precursor and the silicon source precursor may be less than 3 and greater than 0.33. The ratio of the flow rate of the
15 carbon source precursor and the silicon source precursor may be less than 2 and greater than 0.5. The flow rates of the carbon source precursor and the silicon source precursor may be the same or substantially the same (e.g. ratio of the flow rate of the carbon source precursor and the silicon source precursor is less than 1.2 and greater than 0.8).

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The gas mixture preferably consists of a silicon source precursor, a carbon source precursor and a carrier gas or a silicon source precursor, a carbon source precursor, a carrier gas and a dopant source precursor.

25 The gas mixture preferably excludes (i.e. does not include or consist of) hydrogen chloride (HCl) gas.

The temperature may be equal to or greater than 900 °C, equal to or greater than 900 °C, or equal to or greater than 1000 °C. The temperature is preferably equal to or
30 greater than 1100 °C.

Pressure in the reactor during deposition may be equal to or greater than 66.7 Pa (0.5 Torr) and equal to or less than 26.7 kPa (200 Torr) or equal to or less than 80 kPa (600 Torr), i.e. sub-atmospheric chemical vapour deposition. Pressure in the reactor during
35 deposition is equal to or greater than 13.3 kPa (100 Torr) and equal to or less than 13.3 kPa (760 Torr).

The single-crystal silicon has an (001) surface orientation. The single-crystal silicon may have a (110) orientation. The single-crystal silicon may have a (111) orientation. An epilayer of 3C-SiC having (111) orientation (i.e. grown on (111) Si) can used as a
5 substrate for gallium nitride (GaN) overgrowth.

Preferably, the surface of the single-crystal silicon is flat, i.e. unpatterned. The single-crystal silicon may be on-axis. The single-crystal silicon may be off-axis.

10 For a heterostructure having a diameter of at least 100 mm, there is substantially no wafer bow. The surface of the epitaxial 3C-SiC may have an RMS surface roughness, measured by AFM, equal to or less than 20 nm and preferably equal to or less than 10 nm.

15 The substrate may be a wafer and may have a diameter which is at least 100 mm, at least 200 mm or at least 450 mm or more. The wafer is preferably a single-crystal wafer. However, the wafer may be silicon-on-insulator (SOI) wafer or a silicon-on-sapphire (SoS) wafer or other, similar type of substrates.

Brief Description of the Drawings

Certain embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic side view of a 3C-SiC based sensor having a 3C-SiC membrane;

5 Figure 2 is a schematic side view of a first type of 3C-SiC based pressure sensor;

Figure 3 illustrates some of the steps taken during fabrication of the first type of pressure sensor shown in Figure 3; and

Figure 4 is a schematic side view of a second type of 3C-SiC based pressure sensor.

10 **Detail Description of Certain Embodiments**

3C-SiC-based sensor 1 having a 3-C SiC membrane

Referring to Figure 1, a 3C-SiC based sensor 1 is shown.

The sensor 1 comprises a substrate 2 having first and second faces 3, 4 (herein referred to as “upper” and “lower” faces or surfaces). The sensor 1 may include a stack of one or more intermediate layers 5 supported on the first face 3 of the substrate 2. The intermediate layers 5 may include a conductive layer (such as a metal layer) and/or a dielectric layer. The sensor 1 includes a layer 6 of monocrystalline 3C-SiC (hereinafter simply referred to as a 3C-SiC layer) supported directly and/or indirectly on the first face 3 of the substrate 2. As will be explained in more detail layer, the 3C-SiC layer 6 is grown by a low-temperature (i.e. below 1200 °C) deposition process in a cold-wall chemical vapour deposition (CVD) reactor of a type normally used in silicon processing.

The 3C-SiC layer 6 has a thickness, t , which can lie in a range from just a couple of nanometres to several micrometres. For example, the 3C-SiC layer 6 can be ultra-thin, for instance lying in a range between 2 nm and 10 nm, or can be thick, for instance, having an order of magnitude of 1 μm or 10 μm . As will be explained in more detail later, the deposition process can adapted to alter the growth rate by several orders of magnitude.

30 The substrate 2 has a surface region at the top surface 3 which preferably consists of a semiconductor material and which is preferably monocrystalline. The semiconductor material may be silicon and so the substrate 2 can take the form of a silicon substrate or silicon-on-insulator substrate. The silicon may be on-axis and have (001) orientation.

35 The semiconductor material may be SiC and may be 3C-SiC, 4H-SiC, 6H-SiC or other SiC polytype.

The 3C-SiC layer 6 includes at least one first region 7 (hereinafter referred to as “fixed region”) which is directly supported by corresponding underlying region(s) 8, which may be provided by portion(s) of the one or more of the optional intermediate layer(s) 5 and/or the substrate 2.

The 3C-SiC layer 6 also includes at least one second region 9 (hereinafter referred to as “free region” or “suspended region”) which is suspended over a cavity 10. The free region(s) 9 is (are) free to deflect or deform, for example, by bending. A free region 9 is preferably unsupported by an underlying region. However, a free region 9 may move and come into contact with another layer, which may be underlying layer.

The free region(s) 9 of the 3C-SiC layer 6 may be, or may be part of, a sheet or plate (herein referred to as a “membrane”). As will be explained in more detail later, the membrane 9 may deform due to a difference in pressure on either side of (i.e. above and below) the membrane 9 and so the sensor 1 can be used as a pressure sensor. The free region(s) 9 may, however, take the form of a wire or mesh and can be used as, for example, an accelerometer. The free region(s) 9 may be cantilevered, for example, by supporting a first end or edge of free region 9 and leaving a second end or other edges unsupported.

The cavity 10 can take the form of, for example, a trench, blind hole or other form of recess. For example, a cavity 10 may be formed by a recess resulting, at least in part, from etching a part 11 of the substrate 2 at its surface 3. The cavity 10 can take the form of a through-hole resulting from etching a portion 12 of the substrate 2 between the upper and lower surfaces 3, 4 of the substrate 2.

The cavity 10 can be different shapes (in plan view), e.g. circular or rectangular. The cavity 10 can be multi-level, that is, can have two or more parts having different depths.

The sensor 1 preferably includes first and second electrodes 13, 14 for providing electrical signals to a circuit or module 15. For example, the first electrode 13 may be disposed on or in a bottom surface 16 of the cavity 10 and the second electrode 14 is disposed on, in or under the second region 8 of the 3C-SiC layer 6. If the second region 8 is able to deflect or deform towards or away from the bottom 16 of the cavity 10, then the circuit 15 can measure capacitance of the two electrodes 13, 14. Other forms of

electrical measurements, for example using the piezoresistive or piezoelectric effect, can be used.

5 A module 15 may comprise an analogue front end (not shown), which may include amplifiers and filters, and a digital back end (not shown) for providing a digital output 18 via a wire or wireless interface (not shown). The digital output 18 may be compliant with serial bus protocol, such as, for example, I²C/SPI.

10 Preferably, the sensor 1 and the circuit 15 are monolithically integrated using the same substrate, i.e. substrate 2, to provide an integrated sensor 19 suitable for use in harsh environments, for example, at a temperature exceeding 200 °C and up to 400 °C, 500 °C or more. Transistors (not shown) can be implemented using Si-CMOS or SiC-based CMOS and the transistors and other circuit elements can be fabricated in the substrate 2. The digital output 18 may be supplied to a remotely-located module, microcontroller or
15 other computing device (not shown) which is in a less harsh environment.

The back surface 4 of the substrate 2 can support another layer 20 of SiC. This can be used to help ensure that the substrate 2 does not bow or warp.

20 Growing 3C-SiC on Si

In the sensors herein described, crystalline 3C-SiC can be grown on silicon at a temperature below 1200 °C using a cold-wall, reduced-pressure, sub-atmospheric-pressure or atmospheric pressure CVD reactor of a type normally used in silicon processing. An example of a suitable reactor system is the ASM Epsilon 2000 RP-CVD
25 system.

Deposition is carried out using a gas mixture consisting of a silicon source precursor, a carbon source precursor, an optional dopant precursor and a carrier gas. A single silicon/carbon precursor is not used. Hydrogen chloride is not included in the gas
30 mixture.

The silicon source precursor takes the form of dichlorosilane (which may be referred to as “DCS”) having a chemical formula SiH_2Cl_2 and the silicon source precursor takes the form of trimethylsilane (which may be referred to as “TMS”) having a chemical formula
35 $\text{C}_3\text{H}_{10}\text{Si}$. An n-type dopant precursor may take the form of arsine (AsH_3) or phosphine

(PH₃) and a p-type dopant precursor may take the form diborane (B₂H₆). Hydrogen gas is used as a carrier gas.

5 Using these or other similar precursors, crystalline 3C-SiC epilayers can be grown on blank (i.e. unpatterned) silicon substrates, such as on-axis (001)-orientated silicon wafers, at a deposition temperature, T_{EPI} , at or below 1,200 °C and growth rates above 10 µm/h can be achieved. If required, lower growth rates can be used.

10 Examples of other silicon source precursors include other silanes, such as silane (SiH₄) or chlorine-containing silanes, such as trichlorosilane (SiHCl₃). Examples of other carbon source precursors include methyl-containing silanes, such as methylsilane (CH₃SiH₃) or penta-methylene methyl silane (C₆H₁₄Si).

15 The on-axis (001)-orientated silicon wafer is cleaned and its native surface oxide (not shown) is removed using a hydrofluoric (HF) acid dip. The wafer is loaded into the reactor (not shown) at a standby temperature, T_{SB} , via the load lock at atmospheric pressure. The standby temperature, T_{SB} , is 900 °C. However, the standby temperature, T_{SB} , can take a value between room temperature and 1,200 °C.

20 Carrier gas, in this case hydrogen, is introduced into the reactor at a flow rate of 10 slm at a pressure 13.3 kPa (100 Torr). The heaters are switched on and are controlled so that the temperature of the wafer reaches and is maintained at a set-point temperature, which in this case is 1,190 °C.

25 A mixture of dichlorosilane, trimethylsilane and hydrogen is introduced into the reactor (not shown) having flow rates of 10 sccm, 10 sccm and 10,000 sccm respectively, while temperature is maintained at 1,190 °C and pressure is maintained at 13.3 kPa (100 Torr). Thus, the partial pressures of the dichlorosilane and trimethylsilane are 13.3 Pa, 13.3 Pa respectively. The growth rate for this gas mixture and gas flow rates, and at this
30 temperature and pressure is about 20 µm/h.

The gas mixture continues to flow until the desired thickness of 3C-SiC is grown. Once the desired thickness has been reached, the flow of dichlorosilane and trimethylsilane is stopped, but the carrier gas continues to flow. The heaters are switched off and the 3C-SiC/Si wafer is allowed to cool. This can take about 5 to 10 minutes. Once the wafer
35

has cooled, carrier gas flow is stopped and the reactor purged. The 3C-SiC/Si wafer is then removed from the reactor.

The process can be modified by forming *in-situ* a thin seed layer (not shown) prior to epitaxy. The seed layer (not shown) comprises a layer of silicon-carbon ($\text{Si}_{1-x}\text{C}_x$ where x is about 0.01) having a thickness of up to 10 nm.

After loading the wafer into the reactor at a standby temperature, T_{SB} , via the load lock at atmospheric pressure, the wafer is cooled to about 600 °C. A short deposition cycle (e.g. lasting a few minutes) using the same precursors, same flow rates and same pressure is carried out. Due to the lower temperature, however, the process does not result in epitaxy.

Without wishing to be bound by theory, the seed layer (not shown) is thought to help prevent the formation of voids at the surface of the silicon during epitaxy.

No wafer bow can be observed in a 3C-SiC/Si heterostructure 1 comprising a 3C-SiC epilayer grown on a 100 mm-diameter (100) orientation, on-axis single-crystal silicon wafer at 1,190 °C using dichlorosilane and trimethylsilane using the process hereinbefore described. Furthermore, the 3C-SiC/Si heterostructure has an RMS surface roughness of (10 ± 1) nm as measured using an atomic force microscope.

First type of 3C-SiC-based pressure sensor

Referring to Figure 2, a first type of 3C-SiC based pressure sensor 21 is shown. The pressure sensor 21 can operate at high temperatures, for example, up to 500 °C and higher. Reference is made to Haojie Lv *et al.*: “A SiC High-temperature Pressure Sensor Operating in Severe Condition”, TELKOMNIKA, volume 10, pages 2247 to 2252 (2012).

The sensor 21 comprises a monocrystalline 6H-SiC substrate 22 having a stepped upper face 23 and a lower face 24. The sensor 1 includes a conformal layer 25 of dielectric material, which may be aluminium nitride (AlN), supported directly on the stepped face 23 of the substrate 22.

The dielectric layer 25 supports a layer 26 of monocrystalline 3C-SiC comprising an outer fixed region 27 supported by an uppermost part 25₁ of the dielectric layer 25,

which provides a region 28 of attachment for the 3C-SiC layer 26, and an inner, circular membrane 29. A sealed cavity 30 is formed between the dielectric layer 25 and the 3C-SiC layer 26. First and second electrodes 33, 34 are provided by first and second doped regions in substrate 22 and 3C-SiC layer 26 respectively.

5

Referring also to Figure 3, a method of fabricating the first type of 3C-SiC-based pressure sensor 21 will now be described.

10 A 6H-SiC substrate 22' is patterned using photolithography and by reactive ion etching to form the etched substrate 22 (step S1). The first electrode 13 is formed by photolithography and by implanting ions of a dopant species, such as aluminium, into the bottom of the recessed portion of the substrate 22 (step S2). A layer of dielectric material, such as AlN is deposited, for example, using CVD or molecular beam epitaxy (step S3).

15

A layer 26 of monocrystalline SiC is deposited on monocrystalline silicon handle substrate using the process hereinbefore described (step S4). The thickness of the 3C-SiC may have a thickness of about 2 μm . The 3C-SiC layer 26 is wafer bonded to the dielectric layer 25 (step S5) and the silicon handle wafer 29 is removed by wet etching using tetramethyl ammonium hydroxide (TMAH) (step S6). A protective capping layer (not shown) of dielectric material, such as AlN, can be deposited on the exposed surface 20 40 of the 3C-SiC layer 26.

Second type of 3C-SiC-based pressure sensor

25 Referring to Figure 4, a second type of 3C-SiC-based pressure sensor 41 is shown. The pressure sensor 41 can operate at high temperatures, for example, up to 500 °C and higher. Reference is made to N G Wright and A B Horsfall: "SiC sensors: a review", Journal of Physics D: Applied Physics, volume 40, pages 6345 to 6354 (2007).

30 The sensor 41 comprises a monocrystalline silicon substrate 42 having upper and lower faces 43, 44.

The supports a first layer 46 of monocrystalline 3C-SiC comprising an outer fixed region 47 directly supported by the substrate 42 and an inner, elevated membrane 49.

35 A sealed cavity 50 is formed between the substrate 42 and the 3C-SiC layer 46.

A first electrode 53 is supported on the upper surface 43 of the substrate. A second electrode 54 is supported on an upper surface 61 of the 3C-SiC layer 46. A second layer 62 of monocrystalline 3C-SiC overlies the second electrode 54. A third layer 63 of monocrystalline 3C-SiC overlies the second 3C-SiC layer 62. A via 64 passing through
5 the first and second 3C-SiC layers 46, 62 and provides a connection between the third 3C-SiC layer 63 and the substrate 42. Fewer 3C-SiC layers can be used. For example, a single 3C-SiC layer similar to the first type of pressure sensor can be used.

The monocrystalline SiC layers can be deposited using the process hereinbefore
10 described. The layers can be patterned using photolithography and using deep reactive ion etching (DRIE) employing inductively coupled plasma (ISP) advanced silicon etch (ASE) using SF₆/O₂ and/or reactive ion etching (RIE) using SF₆/He.

Gas sensor

15 In some types of sensors, a suspended region of 3C-SiC need not be used. For example, a gas sensor (not shown) comprises a layer of 3C-SiC, an overlying layer of dielectric and a functionalised electrode disposed on the dielectric layer. Reference is made to N G Wright and A B Horsfall: "SiC sensors: a review" *ibid*.

20 Large-scale fabrication

The sensors herein described can be fabricated by depositing crystalline 3C-SiC on a silicon wafer having a diameter, d, equal to or greater than 100 mm without causing bow or warp. This can allow sensors to be fabricated more cheaply. However, even for such large wafers, the 3C-SiC process does not result in bow or warp.

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SiC-based sensor having a Si membrane

In the sensors hereinbefore described, the 3C-SiC membranes are fabricated by depositing 3C-SiC on monocrystalline silicon.

30 The deposition method can be used to deposit a sufficiently thick layer of 3C-SiC at high deposition rates which can be used as a substrate. Thus, the silicon or silicon-on-insulator wafer can be processed, e.g. by thinning the silicon wafer or etching the buried oxide layer, to leave a thin (e.g. less than 100 nm) layer of silicon.

The sensor having a Si membrane has a similar structure to that shown in Figure 1 except that the substrate consists of 3C-SiC and the membrane is provided in a layer of silicon.

5 Modifications

It will be appreciated that many modifications may be made to the embodiments hereinbefore described.

Other forms of electronic device can be formed in and/or on a membrane. Integrated
10 circuits comprising a plurality of devices can be formed in and/or on a membrane.
Additionally or alternatively, other forms of device can be used. For example, optical
devices (such as a laser, light emitting diode or modulator), photonic devices,
spintronic devices and/or microelectromechanical (MEMS) or nanoelectromechanical
(NEMS) devices may be formed.

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Claims

1. A sensor comprising:
a substrate; and
5 a 3C-SiC layer which is monocrystalline and which is supported by the substrate.
2. A sensor according to claim 1, wherein the 3C-SiC layer comprises at least one fixed region and at least one suspended region.
- 10 3. A sensor according to claim 1 or 2, wherein the substrate is a silicon or silicon-on-insulator substrate.
4. A sensor according to claim 1 or 2, wherein the substrate is a silicon carbide substrate.
- 15 5. A sensor according to any one of claims 1 to 4, wherein a first fixed region of the 3C-SiC layer is directly supported by the substrate.
6. A sensor according to claim 5, further comprising:
20 an intermediate layer which is supported by the substrate.,
wherein a second fixed region of the 3C-SiC layer is directly supported by the intermediate layer.
7. A sensor according to any one of claims 1 to 4, further comprising:
25 an intermediate layer which is supported by the substrate,
wherein a first fixed region of the 3C-SiC layer is directly supported by the intermediate layer.
8. A sensor according to any one of claims 1 to 7, wherein the substrate has first and
30 second opposite surfaces and the 3C-SiC layer is supported on the first surface, and
wherein the sensor comprises another 3C-SiC layer which is supported on the second surface.
9. A sensor according to any one of claims 1 to 8, wherein the substrate has first and
35 second opposite surfaces and the sensor comprises a window passing through the substrate between the first and second opposite surfaces of the substrate.

10. A sensor according to any one of claims 1 to 9, comprising:
a housing forming a sealed cavity;
wherein a first suspended region of the 3C-SiC layer forms a deformable portion of the
5 housing.
11. A sensor according to any one of claims 1 to 9, wherein a first suspended region of
the 3C-SiC layer comprises a wire or mesh.
- 10 12. A sensor according to any one of claims 1 to 9, wherein a first suspended region of
the 3C-SiC layer comprises a cantilever.
13. A sensor according to any one of claims 1 to 12, which is a pressure sensor.
- 15 14. A sensor according to any one of claims 1 to 10, further comprising:
a dielectric layer disposed on the SiC layer; and
a conductive layer disposed on the dielectric layer.
15. A sensor according to claim 14, further comprising a functional layer overlying
20 the conductive layer or the conductive layer is functionalised.
16. A sensor according to any one of claims 1 to 10, 14 or 15, which is a gas sensor.
17. A sensor comprising:
25 a 3C-SiC substrate; and
a Si layer which is monocrystalline and which is supported by the substrate.
18. A sensor according to claim 17, wherein the Si layer comprises at least one fixed
region and at least one suspended region.
30
19. A monolithic integrated sensor comprising:
a sensor according to any preceding claim; and
a circuit which is coupled to the sensor and which is disposed in and/or the
substrate.
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20. A method of fabricating a sensor, the method comprising:

providing a sensor substrate; and
providing a monocrystalline 3C-SiC layer on the substrate, wherein providing the 3C-SiC layer comprises forming the 3C-SiC layer by:

5 providing a monocrystalline silicon substrate in a cold-wall chemical vapour deposition reactor;

heating the substrate to a temperature equal to or greater than 700 °C and equal to or less than 1200 °C; and

10 introducing a gas mixture into the reactor while the substrate is at the temperature, the gas mixture comprising a silicon source precursor, a carbon source precursor and a carrier gas so as to deposit an epitaxial layer of 3C-SiC on the monocrystalline silicon.

21. A method according to claim 20, further comprising:

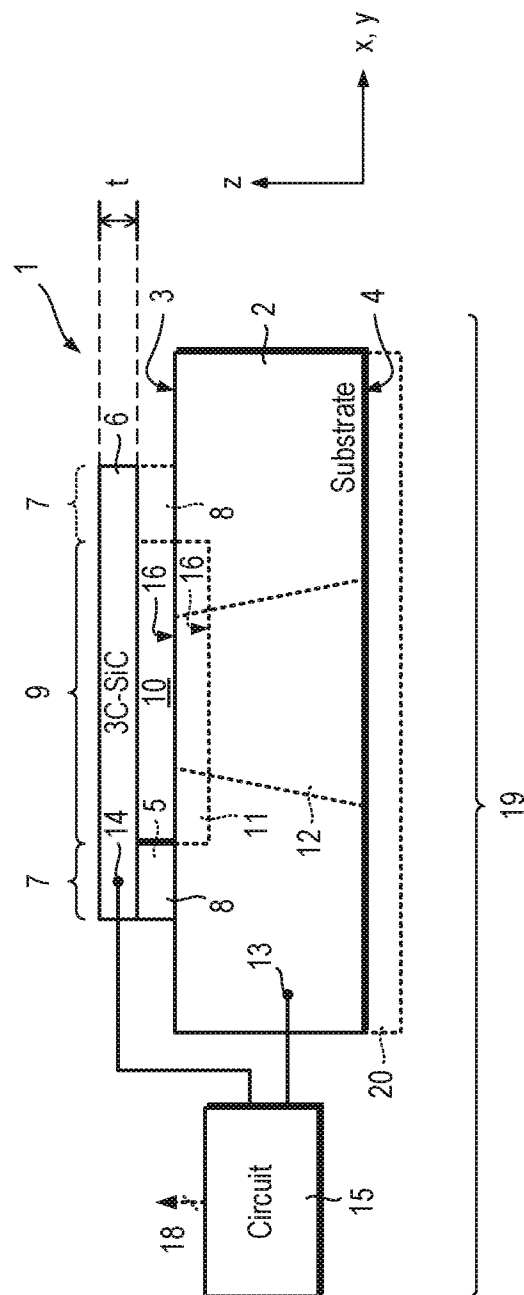
15 processing the substrate, layers on the substrate and/or the 3C-SiC layer such that the 3C-SiC layer comprises at least one fixed region and at least one suspended region.

22. A method according to claim 20 or 21, wherein the monocrystalline silicon substrate is the sensor substrate.

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23. A method according to claim 20 or 21, wherein the monocrystalline silicon substrate is a handle substrate and wherein providing the 3C-SiC layer on the substrate comprises bonding the 3C-SiC layer and the sensor substrate and, optionally, removing the handle substrate.

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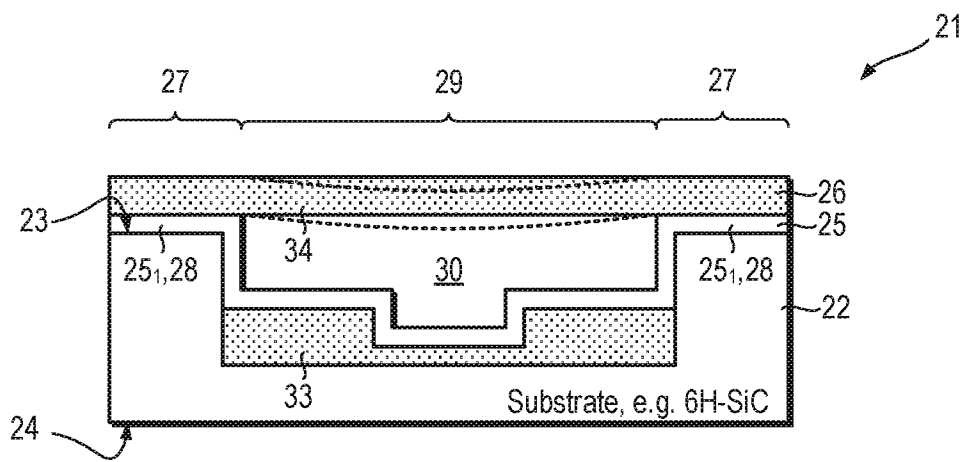


Fig. 2

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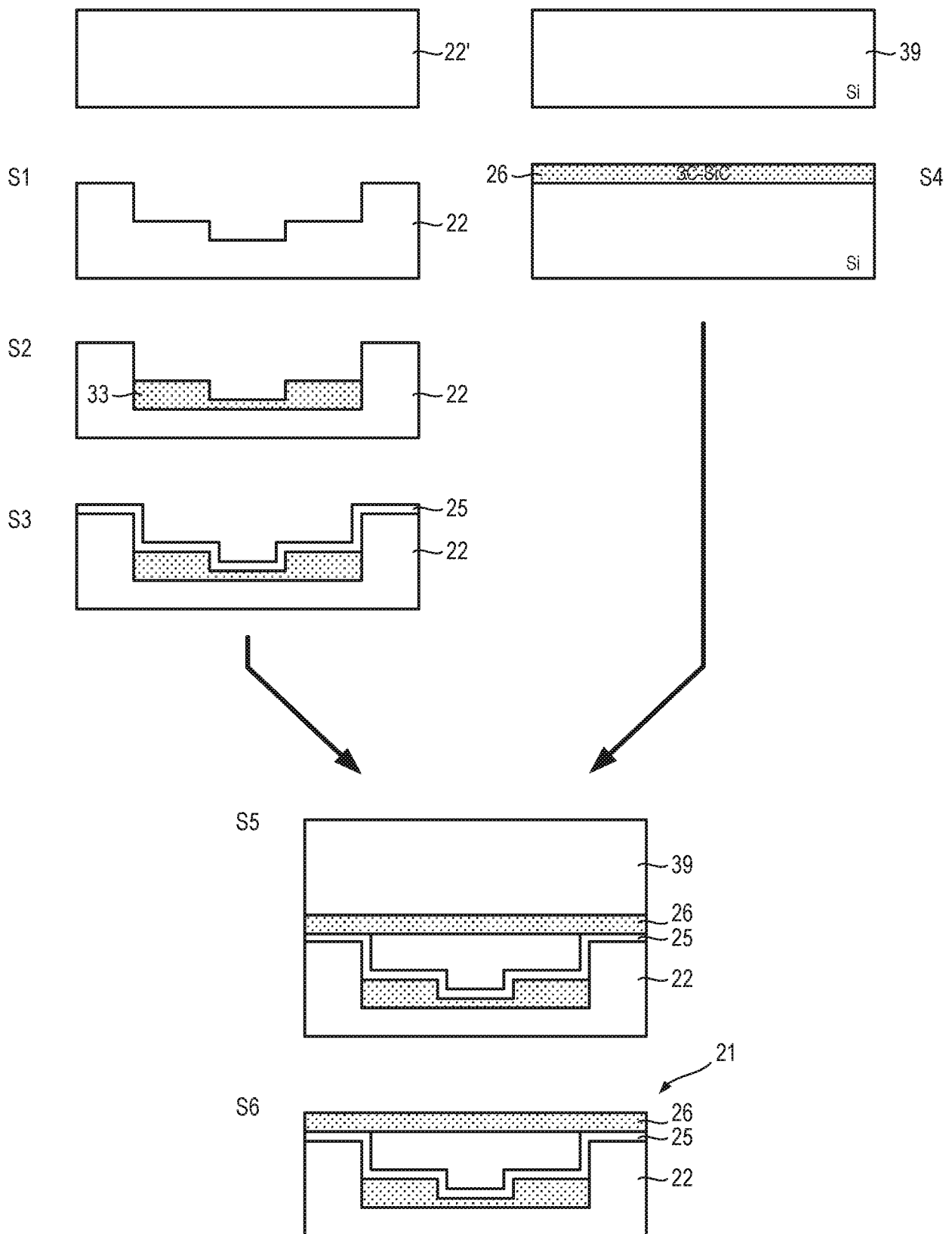


Fig. 3

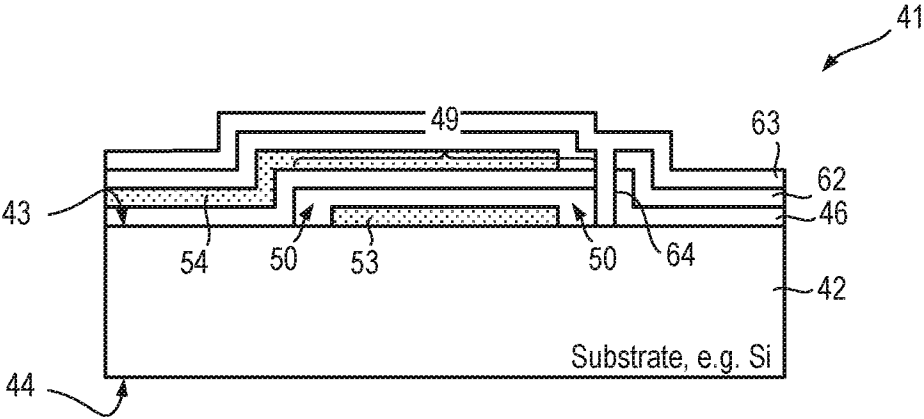


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2016/052992

A. CLASSIFICATION OF SUBJECT MATTER
INV. B81C1/00 G01L9/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B81C B81B G01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/085175 A1 (JOHANSSON HAKAN [SE]) 12 April 2012 (2012-04-12) figure 2	1-23
X	US 5 303 594 A (KURTZ ANTHONY D [US] ET AL) 19 April 1994 (1994-04-19) figure 6	1-23
X	US 2003/036247 A1 (ERIKSEN ODD HARALD STEEN [US] ET AL) 20 February 2003 (2003-02-20) figures 3A-3K paragraphs [0022], [0023]	1,17,19, 20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2016/052992

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