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Fletcher et al.

[15] **3,700,961**

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[54] **PHOTOTRANSISTOR IMAGING SYSTEM**

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[52] **U.S. Cl.**.....**315/169 TV,** 315/169 R, 317/101 A

[51] **Int. Cl.**.....**H05b 37/00,** H02b 1/04

[58] **Field of Search**.....307/303; 315/169 R, 169 TV; 317/101 A

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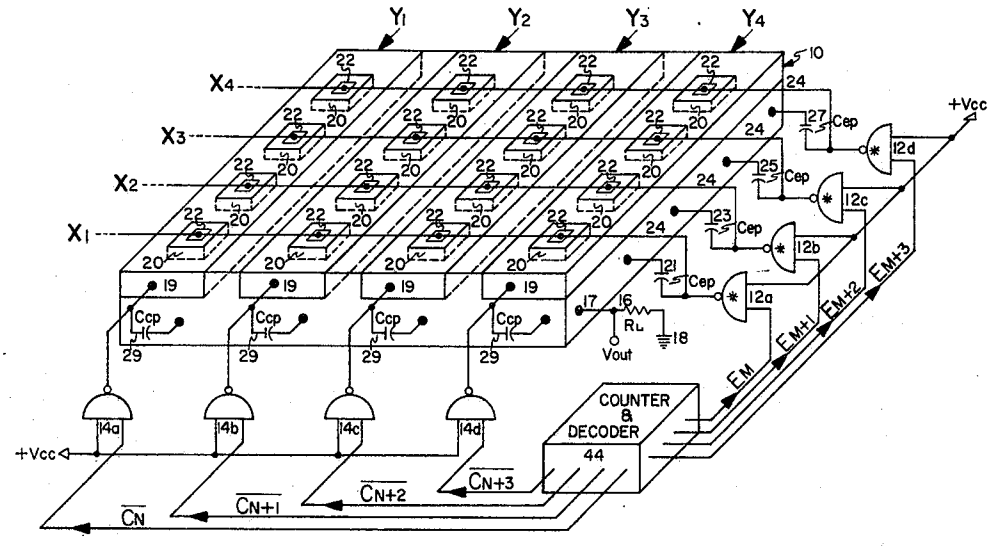
[57] **ABSTRACT**

A phototransistor Imaging system employing a mosaic of phototransistors formed on a semiconductor substrate and operated in a charge-storage mode and in which a charge-storage effect occurring between the substrate and an electrical conductor interconnecting emitters of the phototransistors is used to provide a system output across a load circuit connected between the substrate and a system ground.

7 Claims, 6 Drawing Figures



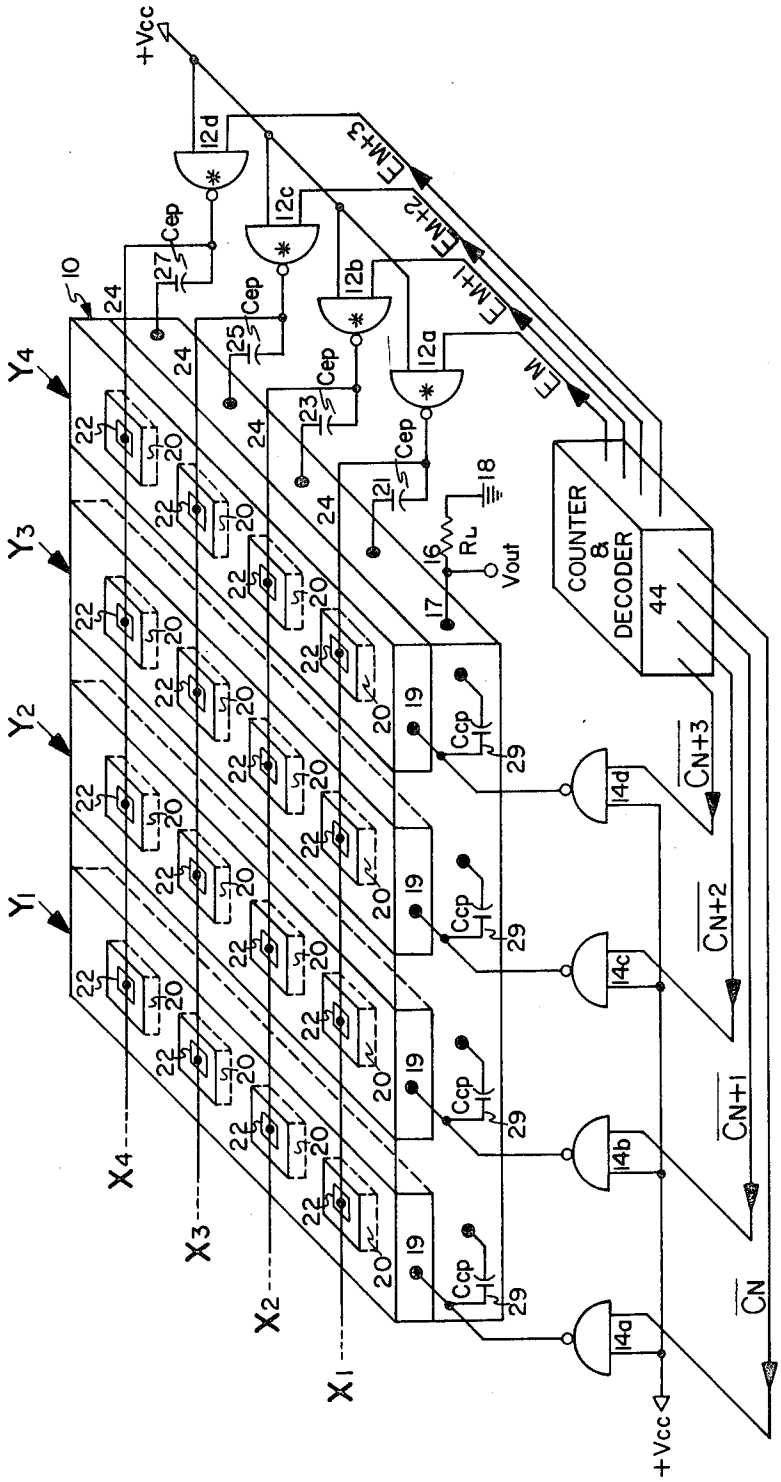


FIG. 1

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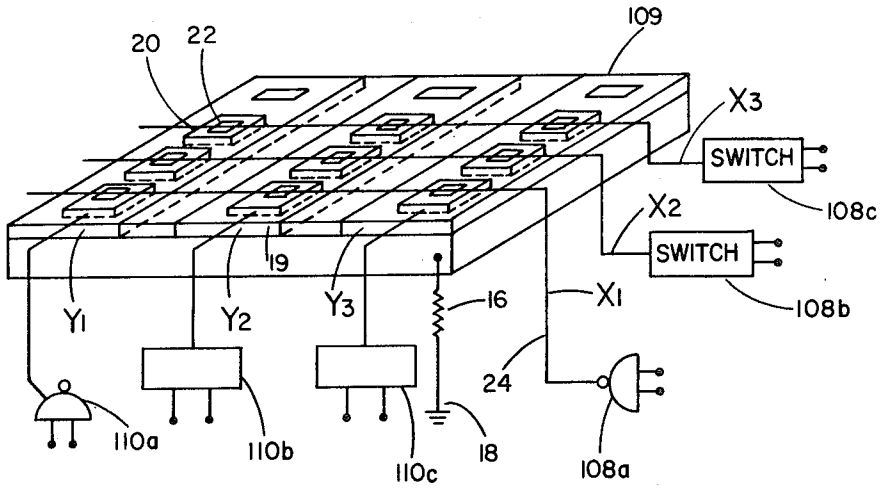

FIG. 2.

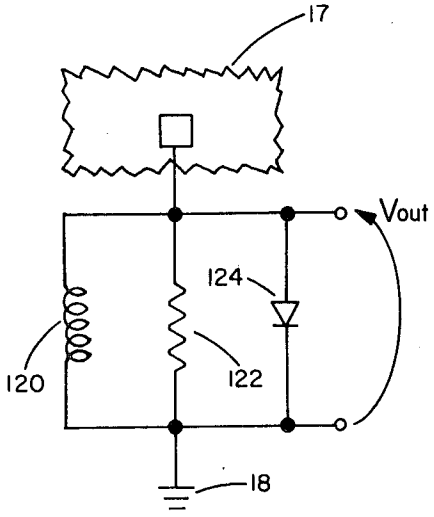

FIG. 5.

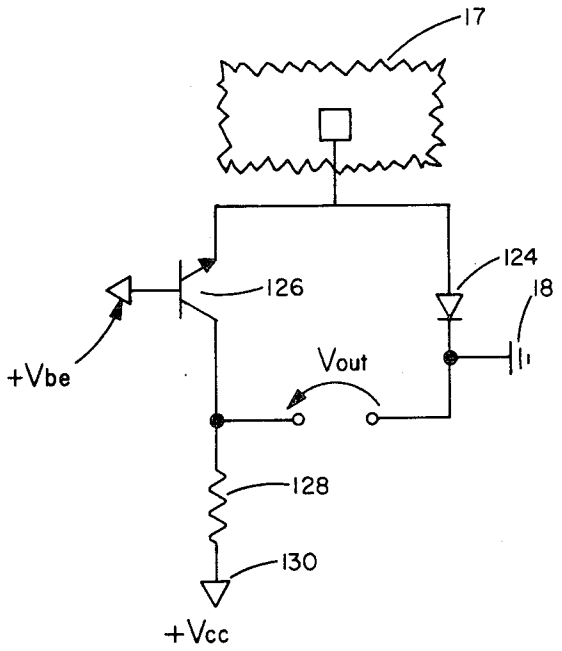

FIG. 6

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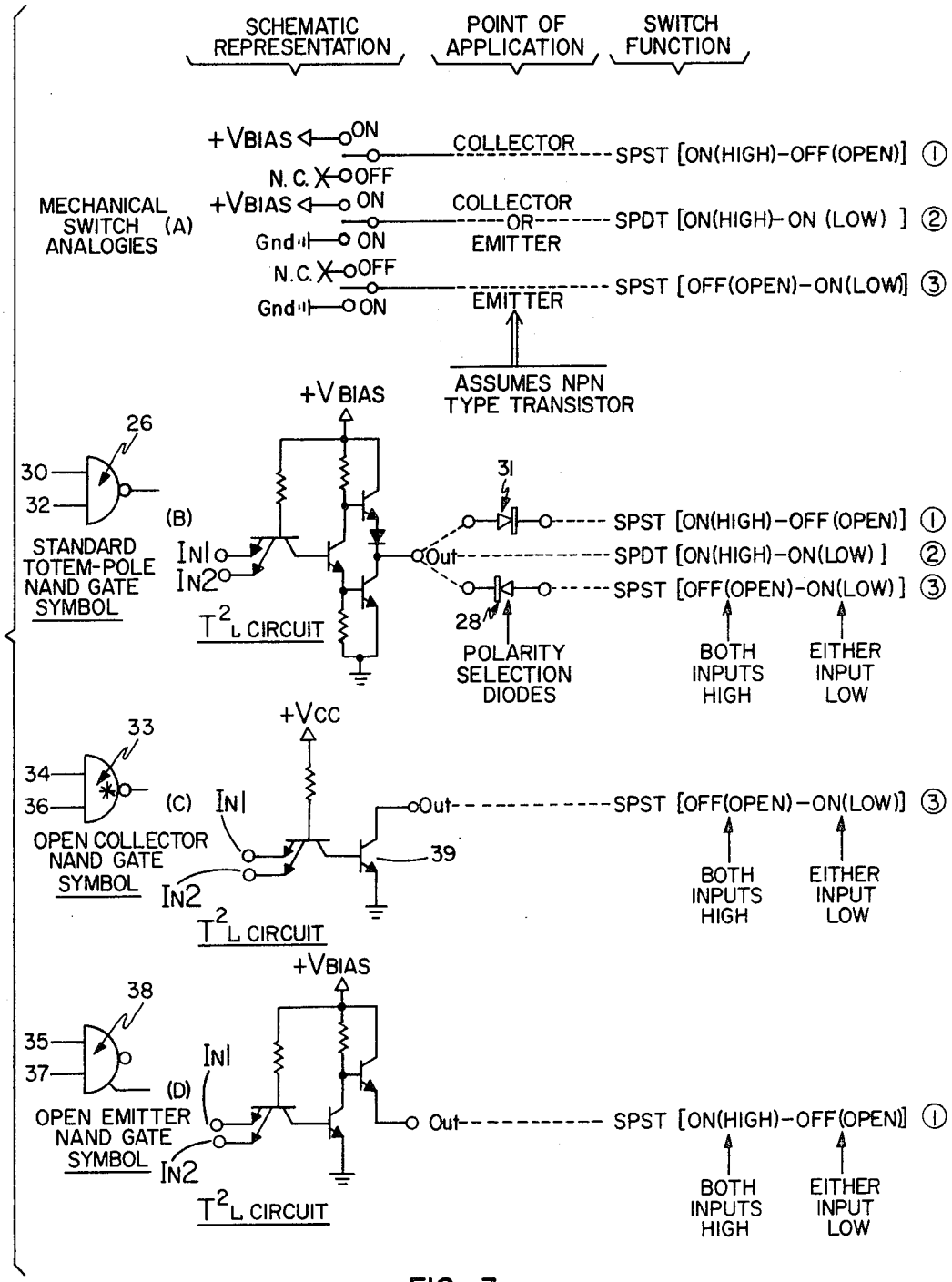

FIG. 3

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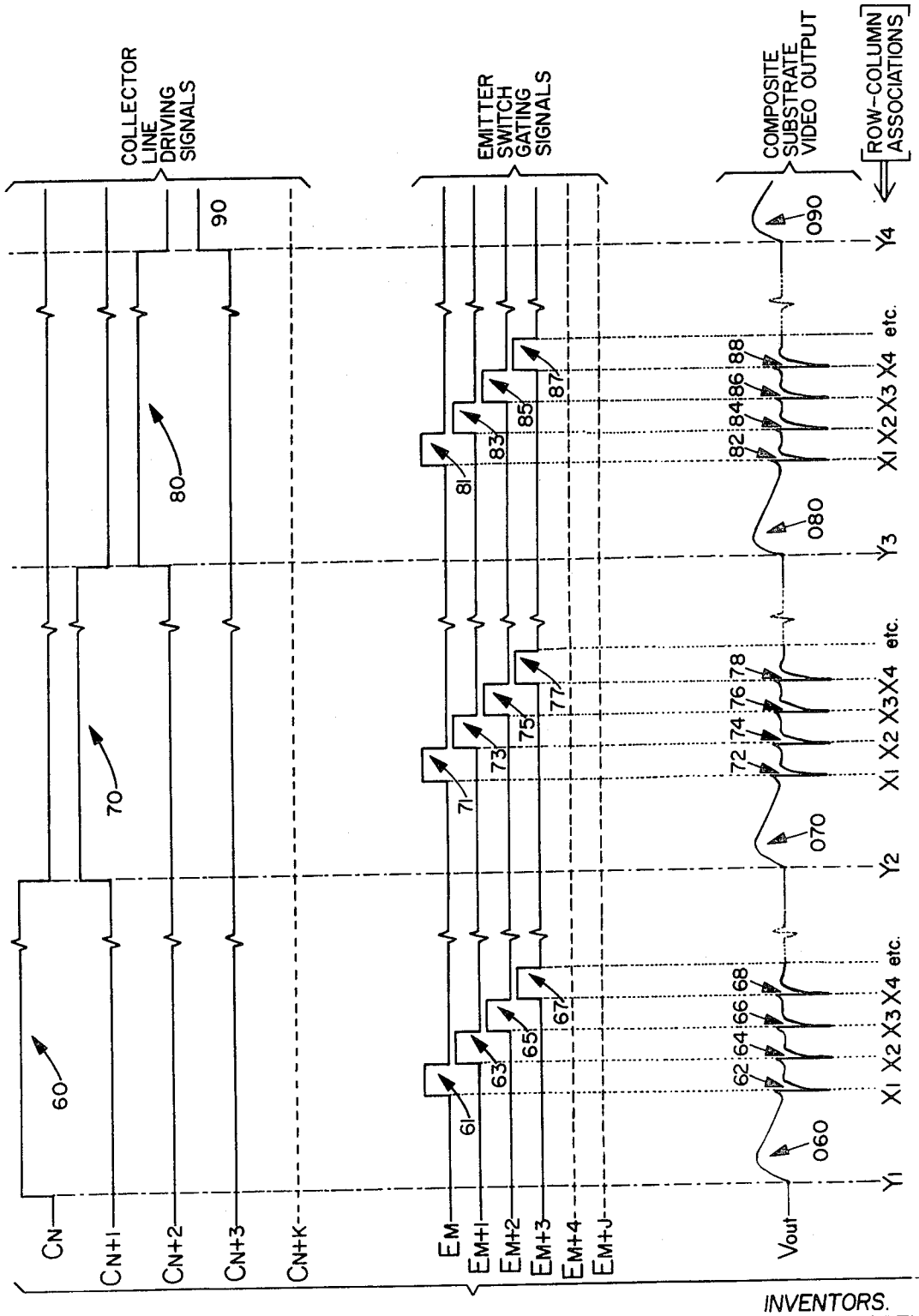

FIG. 4

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PHOTOTRANSISTOR IMAGING SYSTEM

ORIGIN OF THE INVENTION

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958, Public Law 85-568 (72 Stat. 435; 42 U.S.C. 2457).

BACKGROUND OF THE INVENTION

This invention relates to monolithic solid-state photon sensor array systems and particularly to an improved television type imaging system employing phototransistors connected for operation in a charge-storage mode.

GENERAL DESCRIPTION OF THE PRIOR ART

Imaging systems utilizing a large number of phototransistors operated in a charge-storage mode have heretofore been proposed as a substitute for tube type scanning devices commonly employed in television systems (U.S. Pat. No. 3,470,318 to James E. Webb, Administrator of the National Aeronautics and Space Administration, and "Transfer Functions of Imaging Mosaics Utilizing the Charge-Storage Phenomena of Transistor Structures" by Irwin Tepper, Roland A. Anders, and David H. McCann, IEEE Transactions on Electron Devices, Vol. Ed.-15, No. 4, April, 1968).

Basically, phototransistor operation in the charge-storage mode is a dynamic mode of operation in which transient output pulses are obtained. Each pulse is a measure of the total number of photons incident upon the light sensitive region of a particular phototransistor between pulse samplings. Between samplings, light continuously generates carriers which cancel excess carriers stored on the junction capacitance of the phototransistor. Sampling, typically and in accordance with the prior art, consists of detecting the recharge of the collector-base junction capacitance of each transistor through a load resistance. The magnitude of the output, in the form of pulses, depends upon the total amount of light generated charge introduced since the previous sampling and greatly exceeds that which can be obtained by reading out static instantaneous light generated photon current during a period of sampling. This follows since sampling periods, particularly in large scale arrays where thousands of phototransistors are sampled per frame or picture, typically 30 or more frames per second, are very short.

The basic problem in the perfection of large scale phototransistor arrays has been the development of compatible switching systems capable of powering and reading out data from the arrays with sufficient speed. In general this has involved the placement and operation of analog commutating switches in either the collector or emitter leads of the phototransistors and in series with the output load of the array while simultaneously driving the opposing type leads with digital addressing switches. One previous attempt involved the use of bipolar commutating switches, but it was learned that the offset voltage introduced by base injection current made them unacceptable. Another approach has involved using FET switching devices and these have

been successfully used in switching commutators in small and medium size arrays up to approximately 256 lines. Unfortunately, however, an extension of their use to larger arrays has been exceedingly difficult because of the switching speed and "on" resistance tradeoff limitations inherent in unipolar devices. The problem specifically is that the non-zero resistance and turn-on delay time of the commutating devices increases the time constant of the circuit sufficiently to restrict high speed signal read-out. One proposed way of circumventing these characteristic limitations of FET's is to time-share multiplex the per-element selection intervals so that the RC time constant associated with such devices will be sufficient to allow completion of the sensor element recharge cycle. While this approach can be used to some advantage, it requires highly complex logic in the gating circuitry. As a result interest has turned to finding some way of employing saturated bipolar switches, which possess essentially zero "on" resistance. An examination has revealed that in readout signal processing, a charge equal to the leakage in photon generated current during the integration period is fed initially into the parasitic capacitance existing between the emitter bus, that is the conductor interconnecting contiguous phototransistor emitters in an emitter column, and the substrate upon which the phototransistors are formed. This occurs when the collector row of the accessed phototransistor is first activated. The sequential signal selection process then senses or samples in some fashion this charge, after which the potential on the emitter bus capacitance is reset to zero. The usual type of signal output is a voltage developed across a load resistor placed directly in the recharge path of a phototransistor element, that is in series with the emitter-collector circuit of the phototransistor. This means, of course, that in order to achieve fast sampling rates that the time constant of the interface output circuit must be kept low.

While it might seem that a sufficiently low time constant could be obtained by simply reducing either the load resistance or the "on" resistance of the accessing switch, typically a unipolar device, unfortunately the "on" resistance of such devices cannot be made less than about 1000 ohms while still maintaining adequate switching speed in the size device demanded by packaging requirements of large scale arrays. This dictates that the load resistance be kept greater than this value, normally at least 2000 ohms, to prevent excessive voltage division of the output signal.

The result is that neither of these critical parameters, load resistance nor switch resistance, can be effectively reduced sufficiently to provide a circuit time constant low enough to achieve desired high accessing rates of photosensor arrays when interconnected in accordance with prior concepts of accessing circuitry.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a new approach to accessing circuitry which will permit substantially higher rates of readout of photosensor devices and thus make feasible high speed, large scale, photosensor arrays.

These and other objects are embodied in the invention in which a photosensor array is constructed in mosaic form with a plurality of rows of phototransistors

mounted on a common substrate. The collectors of all phototransistors in a particular row are formed of a single common strip on the substrate. Discrete phototransistors are fabricated by forming individual base regions on the collector strip and then introducing an emitter region into each base region. Individual emitters of the phototransistors are subsequently cross-coupled in orthoganal columns, that is the emitters of side-by-side phototransistors are interconnected by a common electrical bus with the result that they are connected in columns perpendicular to the collector rows. Thus a particular phototransistor may be individually energized or accessed by activating the appropriate combination of emitter column and collector row terminals. The sequence and mechanism of operation is as follows: a collector switch applies a charging bias across a series circuit consisting of the collector-emitter circuit of a phototransistor and the parasitic capacitance between the emitter bus associated with that phototransistor and the substrate of the array. Assume that from a previous application of bias to this phototransistor that there remains a residual charge on the base-collector junction of the phototransistor which is equal to the original charge applied less the decrease in potential caused by leakage current across this junction as the result of light received by the phototransistor in the interval since the previous charge was applied. Thus now there will be applied a net charging potential to the parasitic capacitance, and base-collector junction, representative of the difference between applied bias potential and residual base collector potential or charge which is proportional to light sensed by the phototransistor between charging events. Following the parasitic capacitance being so charged, the next thing that occurs is accessing of the emitter, that is connection of the emitter to the return lead of the collector biasing source. The load impedence is not directly in this series circuit however. Instead, by thus closing the emitter circuit the load impedence is connected in an alternate series path which consists of the load impedence, the substrate-emitter stray capacitance and the closed emitter switch. Two things occur as a direct consequence: one, the charge on the substrate-emitter stray capacitance discharges across the load impedence giving rise to an output which is representative of light received by the phototransistor in the interval between successive events of charging or accessing; and, two, the base-collector junction of the phototransistor is again recharged to its full bias potential to ready it for another integration interval. This same process follows for the remaining phototransistors along the given collector row, and thereafter to each of the other phototransistors in the array as it is sequentially scanned row by row and column by column.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a perspective view of a four-by-four section of a phototransistor array and an electrical schematic diagram of the associated circuitry which, together, illustrate an embodiment of the invention;

FIG. **2** is a like type view of an alternate embodiment of the invention;

FIG. **3** is an electrical schematic illustration of the switching functions provided by the matrix per line switches in FIGS. **1** and **2** and the corresponding TTL logic family mechanization forms of each switching function;

FIG. **4** is a graphic illustration of the electrical waveforms secured in the operation of a phototransistor array as shown in FIGS. **1** and **2**;

FIG. **5** is an electrical schematic diagram of an alternate form of load circuit to that shown in FIGS. **1** and **2**; and

FIG. **6** is an electrical schematic diagram of an alternate load circuit to that shown in FIGS. **1**, **2** and **5**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. **1** illustrates a phototransistor imaging system consisting basically of mosaic sensor **10**, emitter switches **12***a*–**12***d*, collector switches **14***a*–**14***d*, and output load resistor (RL) **16**. Significantly, load resistor **16** is connected between substrate **17** of mosaic sensor **10** and system ground **18**. For purposes of illustration only, mosaic sensor **10** is shown with only four strip collector regions **19**, also designated Y_1, Y_2, Y_3 and Y_4 indicative of their row position, and four emitter interconnecting buses **24**, also designated X_1, X_2, X_3 and X_4 indicative of their column position in the array. Actually such a mosaic sensor would typically consist of a row-column matrix of 100 by 100 or more phototransistors. The strip collectors are created or formed in N-type doped epitaxial layer on a P-type silicon substrate **17** by P-type isolation diffusions. Discrete base regions **20** are spaced along each collector strip, each being formed of a layer of P doped silicon. In turn, each emitter region **22** is formed by an N-doped layer on the surface of a base region. Particular phototransistors will be referred to in terms of their matrix position such as X_1- Y_1. While, as illustrated, the phototransistors are of the NPN type it is to be understood that they may be of the reverse, PNP type, in which case the doped regions would be doped with opposite polarity materials. Since there is in effect a junction between each collector row and the substrate, there will exist collector strip junction capacities (Ccp) **29** and the resistance between collector rows will be high providing substantial isolation of rows in this area. In addition, these areas of the substrate between rows contribute small segments to the emitter bus-substrate parasitic capacitance (Cep) **21**, **23**, **25** and **27** which will be further discussed below.

Matrix sensor **10** is energized and outputs obtained by means of the selective operation of emitter column switches **12***a*–**12***d* and collector row switches **14***a*–**14***d* in response to switching control pulses determined and supplied by the system counter and decoder matrix **44**. Counter and decoder matrix **44** is a pulse generator of conventional construction, including a counter and decoder to provide the pulse outputs shown in FIG. **4**. Functionally, the powering of matrix sensor **10** follows, as illustrated in FIG. **4**, a pattern of composite cross-correlation pulses applied through the respective digitally activated line switches.

The individual drive pulses from collector switches **14***a*, **14***b*, **14***c* and **14***d*, are shown as waveforms Cn, Cn+1, Cn+2 and Cn+3, respectively in FIG. **1**. They are produced by like timed pulses from counter and decoder matrix **44**. The fully decoded gating inputs to

emitter switches 12*a*, 12*b*, 12*c* and 12*d* are shown as waveform Em, Em+1, Em+2 and Em+ 3 in the same figure.

Emitter column switches 12*a*–12*d* in FIG. 1 each function as a pull-down type SPST digital switch, the mechanical analogy for which is shown in Configuration A of FIG. 3. Implementation of these addressing units is readily made using commercial TTL devices in the form of either configuration B or C of FIG. 3. These switches are operated in sequence each time and during the powering of every collector row so as to enable the readout of signals from successive phototransistors of that collector row. Emitter accessing occurs when coincident positive inputs are applied to either terminals 30 and 32 of NAND gate 26 or terminals 34 and 36 of NAND gate 33, depending on which is used for a switch 12*a*–12*d* causing it to switch to a zero output. The resulting zero output pulls the emitters to which it is connected down to near zero through either a saturated bipolar transistor (Configuration C of FIG. 3) or a combination saturated transistor and diode (Configuration B of FIG. 3). In the latter case, in the absence of such a pair of accessing pulses, the positive output from NAND gate 26 reverse biases blocking diode 28, or, alternately, the output transistor 39 of NAND gate 33 (Configuration C) is deactivated, either of which condition effectively opens the emitter line and disables the phototransistors to which it is connected. Thus an emitter is enabled or accessed when either a type 26 gate (along with diode 28) or a type 33 gate is gated by coincident positive inputs to terminals 30 and 32, or 34 and 36, respectively, and disabled in between such gating pulses.

Collector row switches 14*a*–14*d* in FIG. 1 each function as an active pull-up and pull-down spot switch, the analogy of which is shown as Configuration A of FIG. 3. One of the many forms in which these switching units can be implemented is shown in Configuration B FIG. 3 using four commercial TTL type NAND logic gates. In operation these row switches each provide, selectively, first a collector biasing potential to a collector row just prior to and during the reading out or accessing of the emitters of that row and then second a hard ground potential to that collector row during those intervals when other collector rows are energized and being accessed. High output, collector line activation using NAND gate 26 (Configuration B of FIG. 3) occurs when non-coincidence exists between positive pulses applied to its inputs, that is when either of the inputs 30 or 32 is placed in the low binary state. In this case the function performed by the NAND gate is simply that of a line controlling switch. Simultaneous incorporation of a basic coincidence requirement in the switch unit can be made by substituting either an AND gate or a NOR gate, assuming conventional positive logic convention, in place of the NAND gate.

Here it should be understood that the TTL logic family, NAND gate switch mechanizations presented in FIG. 3 are merely representative of a number of arrangements possible using any of the various standard logic families, such as DCL, RTL, DTL, TTL, ECL, etc., or any equivalent non-standard binary electronics having sufficient state change, speed and output drive capability. The exact number and polarity of control pulses applied to an emitter or collector switch is thus seen to be governed both by the particular logic design employed in the matrix counter and decoder 44 and by the nature of the input circuitry of the collector and emitter switches 14*a*–14*d* and 12*a*–12*d*, respectively.

Activation of collector switch 14*a*, implemented in the form of NAND gate 26, causes a positive operating bias potential "V" to be applied to collector row Y_1 through the upper pull-up transistor in the "totem-pole" output stage of the gate. The initial result of this process is that the parasitic capacitance 29 or Ccp associated with strip 19 of collector row Y_1 is charged to the "V" bias level, but, since an adjacent collector row capacitance Ccp is simultaneously discharged when it is deactivated, the net result felt at the substrate node 17 and thence across the load resistor 16 is essentially zero. Following this exchange of charge between successive Ccp's, the base-collector junction capacitances of all transistors having their collectors common with collector row Y_1 will be recharged through their individual parasitic emitter bus 24 to substrate 17 capacitances (Cep) 21, 23, 25 and 27 in series with the common output load resistor 16 to ground 18, provided their emitter bus lines are unterminated so that their emitter potentials can "float."

The corresponding charging current pulse at this point in time is illustrated in the V out waveform of FIG. 4 as it appears across substrate load resistor 16. The magnitude of pulse 060 depends upon the pre-existing charge on the base-collector junctions of phototransistors X_1- Y_1,X_2- Y_1, X_3- Y_1,etc., and specifically represents the cumulative electronic charge necessary to re-establish the potential of all these junctions at the level of the bias source. It is to be noted that the charging current represented by pulse 060 is not utilized directly as an output; but rather, as will be further discussed, steps are taken to eliminate its presence in the output.

Following the charging of the elemental capacitances associated with collector row Y_1, the next thing that occurs is that the counter and decoder matrix 44 provides a composite gating pulse to switch 12*a*, shown as pulse 61 in waveform Em on FIG. 4. Propogation of this gating pulse results in switch 12*a*, implemented in the form of either Configuration B or 3 of FIG. 3, pulling the emitter bus 24 for column X_1 to near ground potential for the duration of pulse 61 and thus effecting the discharge of the parasitic capacitance (Cep) 21 associated with emitter column X_1. This is brought about by placing in series a circuit consisting of load resistor 16, substrate-emitter bus X_1 parasitic capacitance 21, and activated emitter switch 12*a*, and results in the development of output pulse 62 in the V out waveform of FIG. 4. The amplitude of this negative output pulse is proportional to the quantity of charge which was pumped into capacitance 21 during and as a part of the charging current indicated by pulse 060. This in turn is dependent upon the preexisting charge on the junction capacitance of phototransistor X_1-Y_1 at the time of charging, and, assuming a previous charging, the loss of charge between chargings. This loss of charge will have been proportional to the light impinging predominently on the base region of the phototransistor between chargings, so output pulse 62 signifies the replacement charge necessary to make up the lost charge, and thereby represents the light incident on phototransistor

X_1-Y_1 between chargings. Once the parasitic emitter bus capacitance **21** has been discharged it will remain in an uncharged state until the next phototransistor along column X_1 is accessed; which, following a normal progression, will occur when collector row Y_2 is addressed.

Next, contiguous emitter switch **12***b* is operated by coincident gating pulses, represented by pulse **63** in FIG. **4**, and as a result parasitic capacitance (Cep) **23** between substrate **17** and emitter bus X_2 is discharged through load resistor **16** producing the output pulse **64** in the V out waveform of FIG. **4**. Again, the resulting negative output pulse across load resistor **16** is proportional to the state of discharge, and thus light received by, the associated phototransistor, in this instance phototransistor X_2- Y_1. Likewise the charge on the base-collector junction capacitance of phototransistor X_2-Y_1 is re-established at full bias value for the next light sensing interval.

Next, switch **12**c is gated by a selection pulse input, represented by pulse **65** in FIG. **4**, which effects the discharge of parasitic capacitance (Cep) **25** and results in the production of output signal pulse **66** which represents the total photons collected by phototransistor X_3-Y_1 since it was last read out. Gating pulse **67** is then processed through switch **12***d* to discharge capacitance (Cep) **27** associated with sensor X_4-Y_1 and yields output signal pulse **68**. This process subsequently is continued for all other emitter columns in the row-column sensor matrix with cross activated collector row Y_1.

The next event is that drive pulse **60** is terminated by deactivating switch **14***a* while a like pulse **70** is simultaneously initiated by activating switch **14***b* as shown by waveforms Cn and Cn+**1** in FIG. **4**. The events described with respect to collector row Y_1 are thus repeated with respect to collector row Y_2, and transistors X_1-Y_2, X_2-Y_2, X_3-Y_2 and X_4-Y_2 are correspondingly accessed by selection pulses **71**, **73**, **75** and **77** of waveforms Em, Em+**1**, Em+**2** and Em+**3** with the resulting production of charging pulse **070** and discharging pulses represented by signal output pulses **72**, **74**, **76** and **78** (waveform V out of FIG. **4**). Finally the sequence described above with respect to collector row Y_1 and Y_2 is repeated for collector rows Y_3, Y_4 and all others remaining in the sensor array. Collector bias is thus applied sequentially according to waveforms Cn through Cn+ k (FIG. **4**) for all of collector switches **14** (FIG. **1**) and emitter pull-down is accomplished contiguously following the Em through Em +j sequence of gating pulse waveforms applied to all of emitter switches **12**. This aggregate, repetitive accessing process results in the development, across substrate load resistor **16**, of composite video signal V out.

As stated above, after a given phototransistor is accessed with the grounding of its emitter the junction capacitance of that transistor is fully charged to the applied bias value enabling it to immediately commence its light sensing interval. During the interim until it is again accessed this phototransistor receives light which, by virtue of recombination action in the base region, causes the excess charge stored on the collector-base junction capacitance to be reduced in proportion to the quantity of light received. Thus, the replenishing current pulse which occurs during operation of the associated emitter switch the next time that sensor is accessed is representative of the loss of charge caused by received light, and thus is an indication of the light which the sensor has received.

Operation of the systems shown in FIG. **2** is similar to the system shown in FIG. **1** except that in this embodiment of the invention provision is made for the collector circuits to float during the periods they are not energized rather than being grounded as in the case of the sensor matrix shown in FIG. **1**. Thus, as shown in FIG. **2**, switches **108***a*, **108***b* and **108***c*, consist simply of a NAND gate **26** (Configuration B of FIG. **3**) which upon application of a positive gating pulse (e.g., waveform Em of FIG. **4**) pulls down its associated emitter bus to ground and in the absence of such a pulse applies a positive and thus inoperative potential to the N-type emitter of mosaic sensor **108**. Collector switches **110***a*, **110***b* and **110***c*, each consist of either NAND gate **38**, with inputs **35** and **37** or NAND gate **26**, with inputs **30** and **32** (Configuration D or B of FIG. **3**). The application of a decoder selection gating pulse to the input of either of these type gates causes an operating bias voltage (e.g., waveform Cn of FIG. **4**) to be applied to the appropriate collector row of matrix sensor **109**. In the absence of such a pulse the pull-up device in the NAND gate turns "off" and thus opens the circuit to the associated collector row of matrix sensor **109** permitting it to float. Actually, during the "off" state of the emitter and collector switches either the emitter or the collector lead may be opened permitting the associated element to float.

FIG. **5** illustrates a modified form of load circuit which could replace load resistor **16** in either FIGS. **1** or **2**. Thus, as shown there is connected between substrate **17** and ground **18**, inductor **120**, resistor **122**, and diode **124**, all in parallel, with diode **124** being polarized for the same direction of flow as the emitter of matrix sensor **10**. Resistor **122** functions to lower the Q of inductor **120**, and the value inductance of inductor **120** is chosen so that it resonates with the substrate-emitter bus parasitic capacitance at a frequency F_e which satisfies the relation of $F_{clock} > F_o > \frac{1}{2} F_{clock}$ where F_{clock} is the rate of accessing of the phototransistors in the array. The diode is included to indicate, in idealized, simplex form, the functioning of a high gain, feedback controlled threshold clamp or clipper which expedites the development of only negative transition signals while positive transitions are rapidly damped out. This thus enables the production of only minor positive excursions and will consequently affect removal of the positive pulses **060**, **070**, **080** and **090** in FIG. **4** which occur at the beginning of each collector address period, and do not represent useful output. This modification also facilitates the introduction of a higher signal developing impedance than normally available, because the DC resistance is very small while the AC impedance is unilateral. This also permits mutually inductive as well as capacitive coupling of the output signal.

FIG. **6** shows still another version of output load circuit. In it there is employed NPN transistor **126** with a fixed operating bias supplied to its base, its emitter being connected to substrate **17** and its collector connected through load resistor **128** to a source of collector bias **130**. As in the case of the circuit shown in FIG.

5, diode **124** is connected between substrate **17** and ground **18** to dampen the effects of initial collector row activation charging pulses **060**, **070**, **080** and **090** on the output. The output signal is subsequently taken off at the collector of transistor **126** where the impedance level transformation introduced into the signal path by the series-pass device allows the use of a much higher signal developing resistance **128** than is possible with the more basic arrangements of FIGS. **1** and **2**. A very high frequency, fast response, operational amplifier could also be used in place of the NPN pass transistor to process the substrate node video.

It is believed that the foregoing invention provides, for the first time, workable means of securing an all bipolar, element-sequencing commutator, for X-Y addressed area arrays of phototransistors and that the phototransistor imaging system of this invention facilitates the handling of photon converted image video date at a much higher rate than has been possible in previous systems.

What is claimed is:

1. A photo imaging system including:

A. a wafer of semiconductor material including a substrate region;

B. a plurality of phototransistors formed in contiguous rows on the surface of said substrate region of said wafer;

C. a said row of phototransistors comprising;

1. a semiconductor strip disposed on said wafer, said strip being a common collector row,

2. a plurality of discrete, light receiving, base regions formed in the surface of said semiconductor strip,

3. a plurality of discrete emitter regions, each emitter region being formed in a surface of a said base region,

D. portions of said wafer lying adjacent to said strips comprising electrical isolation areas whereby very low leakage-conductances are effected between said collector rows;

E. a plurality of emitter connecting conductors for electrically tying a plurality of said discrete emitter regions to form emitter columns, said emitter columns running perpendicular to said common collector rows whereby actuation of a selected discrete combination of a said emitter column and a said common collector row provides unique access to one of said transistors;

F. an output terminal connected to said substrate region;

G. a system reference terminal;

H. an output load connected between said output terminal and said reference terminal;

I. a collector row control switch associated with each said common collector row for selectively applying a first or second electrical condition to a said common collector row;

J. an emitter column control switch associated with each emitter column for selectively applying a first or second electrical condition to a said emitter connecting conductor; and wherein the combination of a said first electrical condition applied to a particular said common collector row and a said first electrical condition applied to a particular said emitter connecting conductor are polarized to apply a reverse bias to the base-collector junction of the intercepted phototransistor and one of said second applied electrical conditions is an open circuit.

2. A phototransistor imaging system as set forth in claim **1** wherein said condition of open circuit is applied to a said emitter connecting conductor.

3. A phototransistor imaging system as set forth in claim **1** wherein said open circuit condition is applied to a said common collector row.

4. A phototransistor imaging system as set forth in claim **1** wherein said open circuit condition is applied to both a said emitter connecting conductor and a said common collector row.

5. A phototransistor imaging system as set forth in claim **1** further comprising switching control means for controlling said collector row control switches and said emitter column control switches and comprising means for sequentially applying operating signals to said collector row control switch for sequentially producing said first electrical condition ad sequentially applying signals to each of said emitter column control switches timed whereby all of said emitter column control switches are discretely operated to provide a first said electrical condition during each period of application by a said collector row control switch of a said first condition to a said collector row, whereby scanning of said phototransistor imaging system is accomplished on a row by row and column by column basis.

6. A phototransistor imaging system as set forth in claim **1** wherein said load device comprises a resistor, an inductor, and diode in parallel, and wherein the inductive reactance of said inductor is substantially equal to the capacitive reactance of the capacitance between said emitter connecting conductors and said semiconductor wafer at a resonant frequency of between one and one-half the frequency of operation of said emitter control switches.

7. A phototransistor imaging system as set forth in claim **1** wherein said load device comprises active device network means configured for providing both direct level conversion and signal amplification.

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