PATENT SPECIFICATION (11) 1 576 734

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(21) Application No. 15691/77 (22) Filed 15 Apr. 1977 (19)
(31) Convention Application No. 678431 (32) Filed 19 Apr. 1976 in
(33) United States of America (US)
(44) Complete Specification Published 15 Oct. 1980
(51) INT. CL.[3] H03L 7/08
H04L 27/06
(52) Index at Acceptance
H3A D LX P T
H4P AA

(72) Inventor: STEVEN A. TRETTER

(54) QAM PHASE JITTER AND FREQUENCY OFFSET CORRECTION SYSTEM

(71) We, RIXON INC., a corporation organised and existing under the laws of the State of Delaware, United States of America, of 2120 Industrial Parkway, Silver Spring, Maryland 20904, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The present invention relates to QAM modems and, more particularly, to a phase jitter and frequency offset correction system for QAM modems.

Two common forms of distortion in digital data transmission systems are phase jitter and frequency offset. Phase jitter is a time-varying shift in the instantaneous phase of a modulated signal and is usually repetitive in some systematic manner. Frequency offset occurs when the modulating and demodulating carriers differ in frequency.

A number of techniques have been developed for combatting phase jitter and frequency offset. For example, where the demodulating carrier is derived from a pilot frequency transmitted over the transmission line, no frequency offset occurs, although the received waveform may be quite different from the transmitted waveform since the phase of the carrier is not adjusted. The reader is referred to U.S. Patent No. 3,813,598 (Stuart) which discloses a carrier recovery system which utilizes a single pilot tone. Reference is also made to U.S. Patent No. 3,849,730 (Ho) which likewise deals with the problems of phase jitter and frequency offset in a vestigial sideband amplitude modulation system. The Ho system employs a quadrature pilot tone added to the transmitted data signal. At the receiver, the carrier frequency, frequency offsets and phase jitter are estimated from the pilot tone which is separated from the data signal using a quadrature demodulator and associated circuitry. The requirement of a pilot tone has obvious disadvantages.

According to the present invention, there is provided a QAM receiver system for correcting phase jitter and frequency offsets in a transmitted QAM signal, said system comprising a decision directed phase-locked loop for receiving the transmitted signal and for generating a phase error signal based on estimates of the transmitted symbols, said phase error signal being used in said phase-locked loop to correct for said frequency offsets, and phase jitter correction means located outside said phase-locked loop and including a low pass filter for passing the expected jitter frequencies, for receiving the inphase and quadrature components of the transmitted signal and said phase error signal, and for correcting said inphase and quadrature components for phase jitter.

The invention will now be described, by way of example only, with reference to the accompanying drawings, of which:

Figure 1 is a schematic circuit diagram, in block form, of a preferred embodiment of a system for correcting phase jitter and frequency offsets in QAM modems in accordance with the invention; and

Figure 2 is a schematic circuit diagram of a phase shifter forming part of the system of Figure 1.

Before discussing the system shown in the drawings, the nature of the transmitted and received signals will be considered. The transmitted signal in a QAM system can be expressed as:

$$s(t) = \Sigma_n a_n h(t-nT) \cos \omega_o t - \Sigma_n b_n h(t-nT) \sin \omega_o t$$

where T is the baud duration, ω_o is the carrier frequency, and h(t) is the impulse response of the transmitter shaping filter. The signal

$a(t) = \Sigma_n a_n H(t-nT)$

is normally referred to as the inphase component of s(t) and

$b(t) = \Sigma_n b_n h(t-nT)$

is normally referred to as the quadrature component of s(t). The pairs (a_n, b_n) can take on 2^k discrete values where k is the number of data bits transmitted per baud. Any two-dimensional signal sets can be generated by QAM modulation. Typical examples are phase modulation, combined amplitude and phase modulation, and signal points at the vertices of rectangular grids.

The equivalent low-pass complex representation for s(t) is

$c(t) = a(t) + jb(t)$

By direct computation it can be seen that

$s(t) = \mathrm{Re}\{c(t)\, e^{j\omega_0 t}\}$

Assuming that the transmitter shaping filter causes no inter-symbol interference, the samples of c(t) are

$c(nT) = a(nT) + jb(nT) = a_n + jb_n$

The complex representation will be used in the remainder of this disclosure.

Assuming that the channel has no amplitude or delay distortion, the received signal can be represented as

$r(t) = c(t)\, e^{jp(t)} + w(t)$

where p(t) is the sum of the channel frequency offset and phase jitter, and w(t) represents additive noise.

Referring now to the drawings, the system illustrated basically comprises a decision directed phase-locked loop indicated within dashed line block A and a jitter corrector indicated within dashed line block B. The line signal enters the system at an input terminal 10 which is connected to first and second balanced mixers 12 and 14. Balanced mixer 12 is directly connected to a voltage controlled oscillator (VCO) 16 while mixer 14 is connected to VCO 16 through a 90° phase shift network 18. The outputs of mixers 12 and 14 are passed through corresponding low pass filters 20 and 22 so as to obtain the inphase component x(t) and the quadrature component y(t) of the received signal, respectively. In complex notation this demodulation process can be expressed by the relationships:

$v(t) = x(t) + jy(t) = r(t)e^{-jB(t)}$

where B is the phase of the output of VCO.

The output signals x(t) and y(t) from low pass filters 20 and 22 are sampled at the time nT and a symbol decision circuit 24 connected to filters 20, 22 selects the most likely transmitted symbol. The output of symbol decision circuit 24 is a pair of signals $\hat{a}_n$ and $\hat{b}_n$. The output of symbol decision network 24, along with the outputs of filters 20 and 22, are connected to a phase error generator 26 which generates a phase error signal f_n of the form

$f_n = \mathrm{Im}\{(\hat{a}_n + j\hat{b}_n)\, \overline{v(nT)} / |(\hat{a}_n + j\hat{b}_n)\, v(nT)|\}$

$= \sin \Delta_n$

where Δ_n is the noise corrupted phase error at the time nT. When the loop is tracking well, the value of Δ_n is small and

$f_n = \sin \Delta_n = \Delta_n$

The output of phase error generator 26 is passed through a low pass loop filter 28 and applied to VCO 16. The bandwidth of loop filter 28 is made small so that the loop including VCO 16 tracks the average phase offset but does not respond to the channel phase jitter. The loop filter 28 is also chosen so that the frequency offsets are tracked. Under these conditions, the output f_n of phase error generator 26 is a noisy estimate of the channel phase jitter.

At this point, it should be noted that decision directed phase-locked loops are conventional and are described in a number of journal articles and textbooks. Reference is made, for example, to U.S. Patent No. 3,806,815 (Fletcher et al) for an example decision directed feedback loop.

Turning now to a consideration of the jitter corrector portion of the system illustrated, the output of phase error generator 26 is connected to a low pass digital filter 30 to eliminate noise. The bandwidth of digital filter 30 is chosen such that the expected phase jitter frequencies are passed thereby. Suitable digital filters are described in the patent and non-patent literature. The outputs of low pass filters 20 and 22 are connected to delay networks 32 and 34, respectively, which delay the inphase samples x(nT) and quadrature samples y(nT) so as to match the delay of digital filter 30.

The outputs of delay networks 32, 34 are connected to a phase shifter 36 which corrects the phase error by performing the computation

$\tilde{a}(n) + j\tilde{b}(n) = [x(nT - NT) + j\, y(nT-NT)]e^{j\hat{f}_n}$

where $\tilde{a}(n)$ and $\tilde{b}(n)$ are the corrected inphase and quadrature components. Expanding the right hand sides yields

$\tilde{a}(n) = x(nT-NT) \cos \hat{f}_n - y(nT-NT) \sin \hat{f}_n$

These are the well known equations for rotating a point in two-dimensional space through an angle $\hat{f}_n$.

Referring to Figure 2, a schematic circuit diagram of an exemplary embodiment of the phase shifter 36 of Figure 1 is illustrated. The phase error signal $\tilde{f}_n$ is applied to a pair of digital table "look-ups" 40 and 42 which produce outputs corresponding to $\cos(\tilde{f}_n)$ and $\sin(\tilde{f}_n)$, respectively, these circuits functioning simply to "look up" in a memory the cosine or sine of the phase error angle $\tilde{f}_n$. The output of digital table look-up 40 is connected to a first pair of multipliers 44 and 46 which receives as a second input the x(nT-NT) and y(nT-NT) input signals, respectively. Similarly, the output of digital table look-up 42 is connected to a second pair of multipliers 48 and 50 which are respectively connected to receive the x(nT-NT) and y(nT-NT) inputs to phase shifter 36. The outputs of multipliers 46 and 48 are connected to the inputs of a first adder 54 while the outputs of multipliers 44 and 50 are connected to the inputs of a second adder 52. It will be appreciated that the circuitry illustrated performs the required mathematical manipulations and thus that the outputs of adders 52 and 54 are desired signals $\tilde{a}(n)$ and $\tilde{b}(n)$ as defined hereinabove.

It will be seen that if no additive noise were present in the channel, the bandwidth of the decision directed phase-locked loop, indicated within the dashed lines block A, could be increased so that the jitter corrector, indicated within dashed line block B, would not be required. However, in the presence of noise, the loop performs poorly because of the relatively wide bandwidth thereof. Thus, as stated hereinbefore, and as will be evident from the foregoing, the present invention concerns the use of a narrow band loop, as provided by loop filter 28, which is not affected by noise, in combination with the provision of jitter correction outside of the loop.

Although the invention has been described relative to examplary embodiments thereof, it will be understood that other variations and modifications can be effected in these embodiments without department from the scope of the invention.

WHAT WE CLAIM IS:

1. A QAM receiver system for correcting phase jitter and frequency offsets in a transmitted QAM signal, said system comprising a decision directed phase-locked loop for receiving the transmitted signal and for generating a phase error signal based on estimates of the transmitted symbols, said phase error signal being used in said phase-locked loop to correct for said frequency offsets, and phase jitter correction means, located outside said phase-locked loop and including a low pass filter for passing the expected jitter frequencies, for receiving the inphase and quadrature components of the transmitted signal and said phase error signal, and for correcting said inphase and quadrature components for phase jitter.

2. A system as claimed in Claim 1, wherein said low pass filter comprises a low pass digital filter connected to receive said phase error signal, and wherein said phase jitter correction means further includes delay means for delaying the phase of the inphase and quadrature components to match the delay of the digital filter, and phase shifter means connected to the outputs of said digital filter and said delay means for correcting the phase of said inphase and quadrature components by a rotational transformation.

3. A system as claimed in Claim 2, wherein said phase shifter means comprises means for performing the computation $\tilde{a}(n) + j\tilde{b}(n) = [x(nt\text{-}NT) + j\, y\, (nT\text{-}NT)]\, e^{j\tilde{f}n}$, where $\tilde{a}(n)$ and $\tilde{b}(n)$ are the corrected inphase and quadrature components, x(nT-NT) and y(nT-NT) are the values of the inphase and quadrature components at the sample time nT, as delayed by said delay means, and f_n is the phase error signal after processing by said low pass digital filter.

4. A system as claimed in any preceding Claim, wherein said phase-locked loop includes symbol decision means for selecting the most likely transmitted symbol and generating corresponding inphase and quadrature signals $\hat{a}_n$ and $\hat{b}_n$, and a phase error generator for generating said phase error signal, said phase error generator receiving said $\hat{a}_n$ and $\hat{b}_n$ signals together with the inphase and quadrature signals sampled at the time nT, and computing an error signal

$$\hat{f}_n = \mathrm{Im}\left\{\frac{(\hat{a}_n + j\hat{b}_n)\,\overline{v(nT)}}{\left|(\hat{a}_n + j\hat{b}_n)\,\overline{v(nT)}\right|}\right\}$$

5. A QAM receiver system for correcting phase jitter and frequency offsets in a transmitted QAM signal, the system being substantially as herein described with reference to the accompanying drawings.

B.D. STOOLE
Chartered Patent Agent
Agent for the Applicants

Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1980.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1576734 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

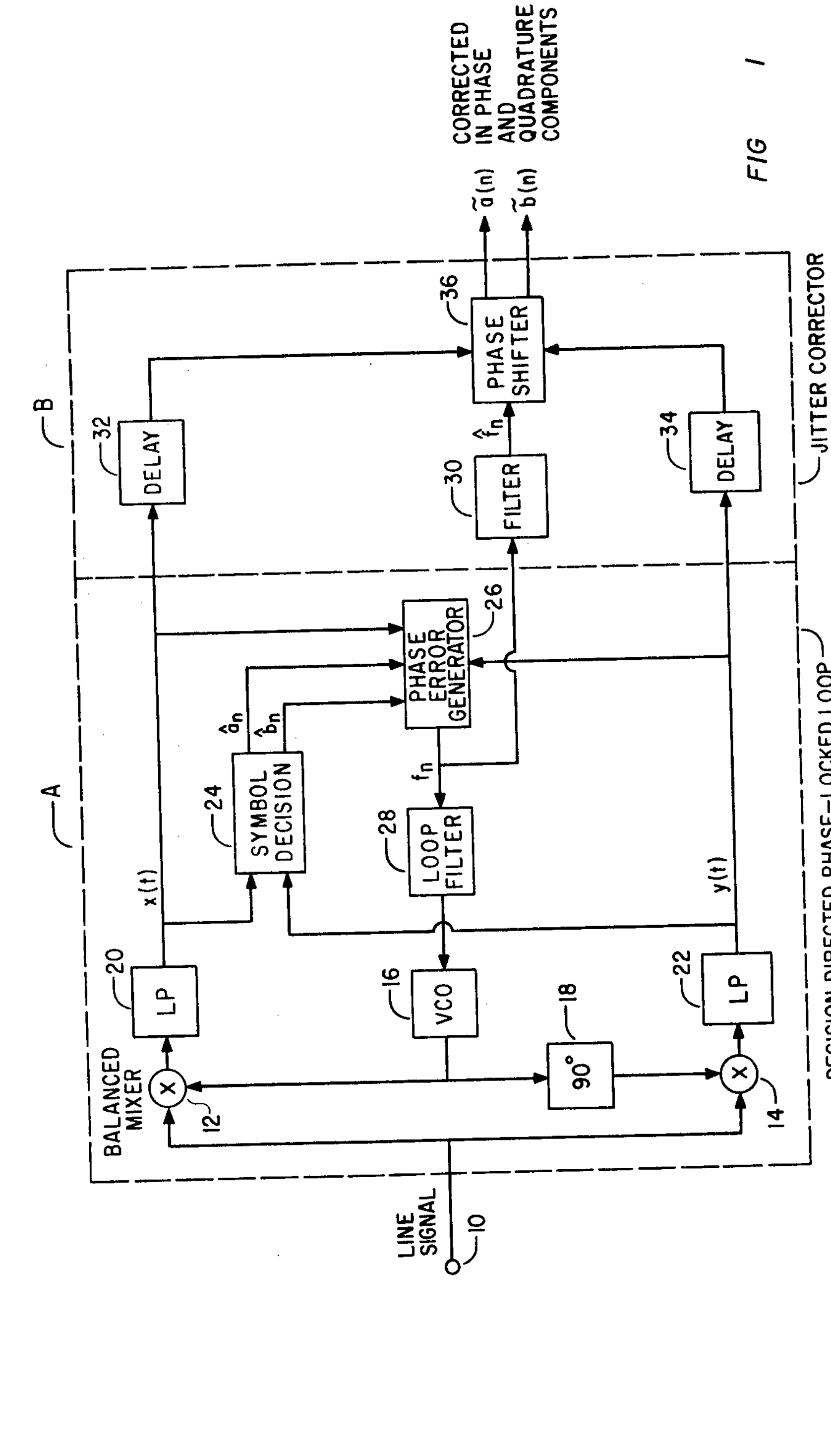

FIG 1

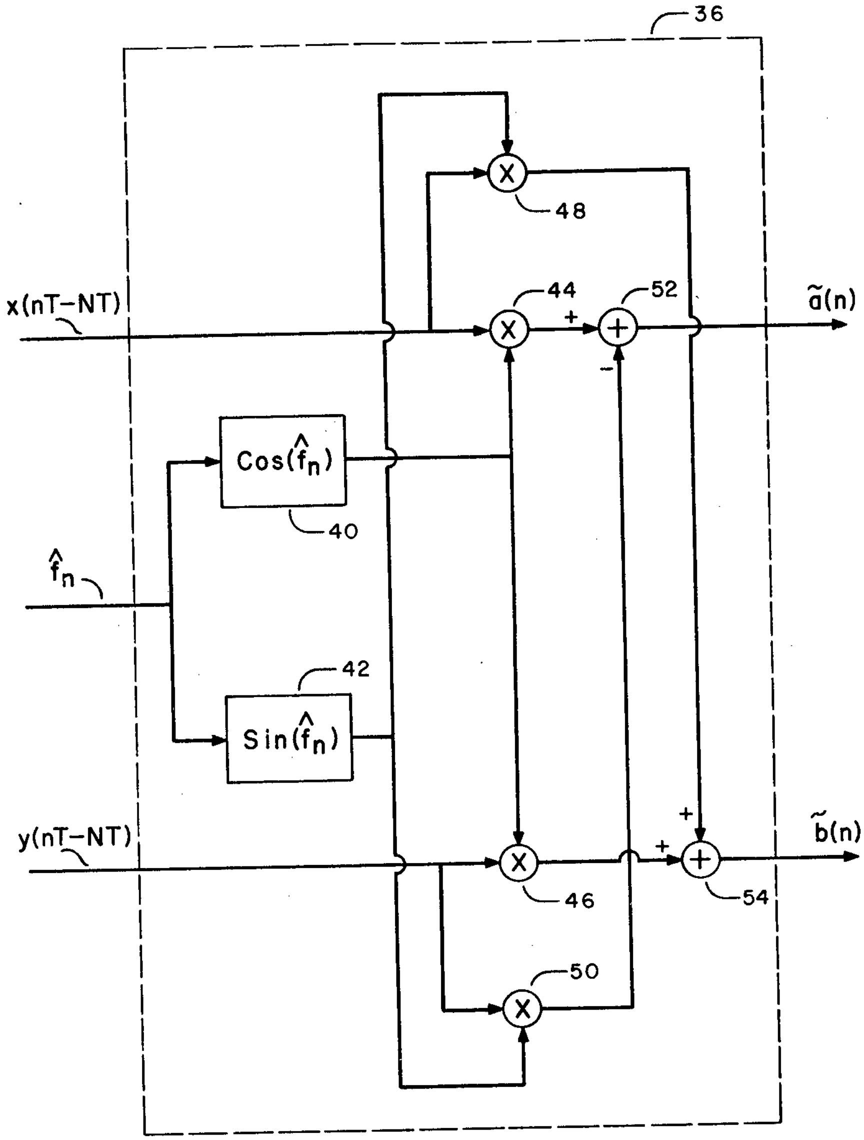

FIG 2