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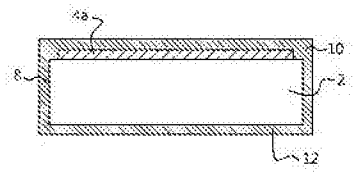
(54) **Method for manufacturing photovoltaic cells with a rear side polysiliconpassivating contact**

(57) A method for manufacturing a photovoltaic cell from a substrate (2) having a front side (4), a back side (6) and an edge (8). A carrier selective contact structure (4a) of a first type is provided on at least a part of the front side (4). A stack (10) having a thin oxide layer covered by a polysilicon layer is applied, wherein the stack (10) is applied to the back side (6) and the front side (4) of the substrate (2), and possibly also on edge (8). The stack (10) of thin oxide layer and polysilicon layer on the front side (4) is then removed.



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Method for manufacturing photovoltaic cells with a rear side polysilicon passivating contact

Field of the invention

The present invention relates to a method of manufacturing a solar cell, in particular a solar cell having a rear side polysilicon passivating contact.

Background art

US patent publication US-B-7,633,006 discloses a method for manufacturing a photovoltaic cell, wherein atmospheric pressure chemical vapour deposition (APCVD) is used to deposit various layers on top of a tunnel oxide layer on a back side of a silicon substrate. The tunnel oxide layer is deposited on both sides of the substrate (using e.g. an ozone oxidation process), and the front side tunnel oxide layer is removed in a later process step. The various layers include a polysilicon layer on top of a tunnel oxide layer, followed by a layer of p-type dopant and a layer of undoped silicon oxide. Such APCVD depositions are advantageous when only applying layers to one side of the substrate, such as in manufacturing back side contact solar cells.

Summary of the invention

The present invention seeks to provide an improved method for manufacturing photovoltaic cells comprising rear side polysilicon passivating contacts. The method allows efficient use of manufacturing steps for protecting sides of the solar cell during various treatment steps.

According to the present invention, a method is provided for manufacturing a photovoltaic cell from a substrate having a front side, a back side and an edge (i.e. the circumferential side between front and back side). The method comprises providing a carrier selective contact structure of a first type (i.e. an electron or hole contact structure) on at least a part of the front side, and applying a stack having a thin oxide layer covered by a polysilicon layer. The stack is applied to the back side and the front side of the substrate, e.g. using a non-single sided process, and thus possibly also on the edge. At the back side the stack may be forming a rear side passivating contact structure of a second type (electron/hole). The method then further comprises removing (e.g. etching) the stack of thin oxide layer and polysilicon layer on the front side. It is noted that the term polysilicon as used herein encompasses amorphous silicon or polycrystalline silicon.

Through application of the thin oxide layer and polysilicon layer to the back side, edge as well as the front side of the substrate, a simplified manufacturing process is obtained wherein the applied stack acts as an effective barrier for subsequent treatment steps, in particular diffusion steps. Providing the stack of the present invention allows for a convenient "all side" manufacturing process, wherein an unwanted part of the stack on the front side of the substrate can be easily

removed. It is noted that other elements, e.g. carbon, may be admixed to the polysilicon. The oxide layer may be a silicon oxide layer. Other elements, e.g. nitrogen, may be admixed to the oxide layer.

Another advantage of the method is that removal of the stack from the front side of the substrate allows to provide a good edge isolation, which in its turn minimizes reverse currents through the photovoltaic cell when in operation.

Short description of drawings

The present invention will be discussed in more detail below, with reference to the attached drawings, in which

Figure 1A to 1F depicts a schematic overview of the consecutive process steps for manufacturing a photovoltaic cell with a rear side polysilicon passivating contact in accordance with an embodiment of the present invention;

Figure 2A to 2E depict a schematic overview of the consecutive process steps for manufacturing a photovoltaic cell with a rear side polysilicon passivating contact in accordance with a further embodiment of the present invention; and

Figure 3A to 3E depict a schematic overview of the consecutive process steps for manufacturing a photovoltaic cell with a rear side polysilicon passivating contact in accordance with an even further embodiment of the present invention.

Description of embodiments

When manufacturing a solar cell from a substrate through single sided processing steps, the manufacturing process must ensure that exposure of the other sides to the single sided processing step is minimized. In light of this there is a need for a method of manufacturing a solar cell that reduces the number of single sided processing steps and as such reduces the manufacturing complexity and associate costs for the solar cell.

The method of the present invention fulfils the above need by providing a method of manufacturing a solar cell by allowing for convenient "all side" processing steps whereby all sides of the substrate are subjected to the same treatment.

A doped polysilicon layer on top of a tunnel oxide layer forms a passivating contact on a silicon wafer, also known as a passivated contact or a carrier-selective contact. As is known in the art, contacts to crystalline silicon solar cells have to extract one type of carrier (electron or hole) and to at least a certain extent prevent the other type of carrier from entering the contact or recombining in the contact region (this prevention means there is some degree of passivation). That means that all contacts to solar cells advantageously are passivating or carrier-selective to some degree. The quality of a contact in preventing the other type of carrier from entering the contact and from recombining in the contact region is typically represented by the prefactor of the recombination current contributed by that contact $J_{o,c}$. A highly doped surface region of a wafer, that can e.g. be created by diffusion or implantation and anneal, and on which a metal contact is disposed, is one way of creating a contact for a solar cell that has some degree of carrier

selectivity and passivation. This is the dominant way of creating contacts to crystalline silicon solar cells in the present industrial manufacturing of solar cells. A typical $J_{o,c}$ of such a contact ranges from several hundred fA/cm^2 to several thousand fA/cm^2. Much better $J_{o,c}$ of typically between one and several tens fA/cm^2 can be obtained by disposing on a crystalline silicon wafer a highly doped polysilicon layer on top of a tunnel oxide layer (the tunnel oxide layer being between the wafer and the doped polysilicon). On the polysilicon a metallic contact can be disposed while retaining such a low $J_{o,c}$. In the following description the terminology passivating contact as well as carrier selective contact is used, both describing such and other variations for creating a contact for a crystalline silicon solar cell.

Figure 1A to 1F each show consecutive steps of an embodiment of the method according to the present invention. In the embodiment step shown in Figure 1A there is provided a substrate or wafer 2, e.g. a silicon substrate/wafer, having a front side 4, a back side 6 and an edge 8. In an embodiment, the edge 8 may be seen as a circumferential edge of the (semi-square) substrate 2, i.e. the edge 8 is the surface part of the substrate 2 connecting the front side 4 and back side 6.

As depicted in Figure 1A, the substrate 2 may be a substrate or wafer 2 suitable for production of solar cells (e.g. having a textured front side or a textured front and back side). In one embodiment a carrier selective contact structure 4a of a first type is provided as a first polarity diffusion layer 4a on at least part of the front side 4, e.g. on both front side 4 and back side 6, before applying a stack 10 as described below with reference to Fig. 1C. The first polarity diffusion layer 4a may also be provided on (or into) all sides of the substrate/wafer 2, i.e. on the back side 6, edge 8, and front side 4, as shown in Figure 1A (note that diffusion layer 4a would be within a surface layer part of the front side 4, back side 6, and edge 8) thereby allowing for all side treatment of the substrate 2. The carrier selective contact structure 4a may also be formed by or comprise an implanted layer, an implanted and annealed layer, deposition of BSG, or a thin oxide/doped polysilicon stack, as well as other carrier-selective contact layers which are known as such in the art, e.g. a metal oxide or metal oxide/oxide stack.

In an exemplary embodiment, the first polarity diffusion layer 4a may be a *p*+ diffusion layer. The *p*+ diffusion layer 4a may be envisaged as providing a *p*+ type front contact layer on the front side 4 of the substrate 2 as shown in Figure 1a. The p+ diffusion may be applied through an all side treatment step and as such the *p*+ diffusion layer 4a will enclose the undiffused body of the substrate 2 as depicted. In an embodiment, the first polarity diffusion layer 4a may be obtained by depositing borosilicate glass (BSG) followed by an annealing step. E.g., the sheet resistance of the layer 4a may between about 50 and 500 Ohm/square, e.g. about 100 Ohm/square, with a surface dopant concentration above about 1E19 cm^{-3}. For example the thickness of layer 4a may be between about 50 nm and 5 µm, e.g. about 1 µm.

As mentioned, the method embodiments of the present invention allow for a first polarity diffusion layer 4a to be provided to the substrate 2 before the stack 10 of a thin oxide layer and polysilicon layer is applied. In an embodiment, providing such a first polarity diffusion layer 4a may be accomplished in an all side treatment step so that the first polarity diffusion layer 4a is provided on the back side 6, edge 8 as well on the front side 4. In case the first diffusion layer 4a is to be

used as a front contact layer, for example, an embodiment is provided wherein the first polarity diffusion layer 4a on the back side 6 and the edge 8 of the substrate 2 is removed using a single side etching step. The result of this step is clearly depicted in Figure 1B, wherein only the front side 4 comprises the first polarity diffusion layer 4a. It is noted that this etching step is performed before the stack 10 is applied, again see the description with reference to Figure 1C below.

In an advantageous embodiment, the first polarity diffusion layer 4a is further removed from a rim surface part 5 of the front side 4 of the substrate 2 using a single side etching step. The rim surface part 5 may be seen as a circumferential edge of the front side 4. The main reason for also removing the rim surface part 5 of the front side 4 (e.g. with a (circumferential) width of at most 2 mm) is to provide an improved edge isolation with respect to a doped layer 12 which is provided later in the manufacturing process (see description of Figure 1C below). This method embodiment step is also depicted in Figure 1B and also performed before the stack 10 is applied to the substrate 2.

The rim surface part 5 may further be passivated with a passivating coating such as a silicon oxide/silicon nitride stack or an aluminium oxide/silicon nitride stack.

According to the present invention, the method for manufacturing the solar cell comprises, as depicted in Figure 1C, the step of applying or depositing a stack 10 of a thin oxide layer covered by a polysilicon layer on all sides of the substrate 2. That is, the stack 10 is deposited on the back side 6, the edge 8 as well as the front side 4 of the substrate 2. In an embodiment, the thin oxide is a thin silicon oxide layer providing excellent passivating properties. In a further embodiment the thin oxide layer has a thickness between 0.5 nm and 3 nm. The stack 10 may furthermore comprise amorphous silicon which crystallizes into polysilicon during subsequent processing. E.g., the thickness of the polysilicon may be between about 5 nm and 500nm, e.g. about 100nm.

Through the above method step an "all-side" treatment step is provided whereby all sides of the substrate 2 are subjected to the same treatment. Such an all-side treatment step may be performed in e.g. a single processing chamber for the substrate 2, so that manufacturing complexity is reduced as masking equipment or use of barriers for the substrate 2 are not needed.

Once the stack 10 of the thin oxide layer and polysilicon layer is deposited on all sides 4, 6, 8 of the substrate 2, the method according to this embodiment further comprises the step of subsequently providing a doped layer 12 on the back side 6, the (circumferential) edge 8 and the front side 4 of the substrate 2 through diffusion. The doped layer 12 may be formed by a doped polysilicon layer part of the stack 10. Instead of subsequently doping the polysilicon layer part of the stack 10, the polysilicon layer may also be doped in-situ during deposition of the entire stack 10. Instead of doping by diffusion or in-situ doping, also other doping methods such as implantation may be used (in case of implantation, for reasons of cost-effectiveness only the rear side part of stack 10 would be implanted).

In an embodiment the doped layer 12 may be a $p+$ or an $n+$ type doped layer 12. For example, in an embodiment a $p+$ doped layer 12 may be provided through boron diffusion. In a further embodiment an $n+$ doped layer 12 may be provided through phosphorous diffusion (e.g.

using POCl3). The active dopant concentration of the doped polysilicon layer is in advantageous embodiments above 1E19 cm^{-3}, more preferably about 1E20 cm^{-3} or higher, to obtain suitable carrier selective properties.

The method then proceeds with the step of removing the stack 10 of the thin oxide layer and polysilicon layer on the front side 4 (e.g. by an etching step). This step allows the front side of the substrate 2 to be exposed again and ready for further processing, e.g. making front contacts.

According to the present invention, the stack 10 of the thin oxide layer and polysilicon layer provides an excellent barrier so that one or more sides 4, 6, 8 of the substrate 2 can be subjected to one or more all side treatment steps such as an all side diffusion step after which unwanted parts of the resulting stack 10 can be removed at will.

As depicted in Figure 1C, when the stack 10 is deposited on the back side 6, edge 8, and/or front side 4 of the substrate 2, the applied stack 10 covers (at least in part) the first polarity diffusion layer 4a and prevents degradation thereof during subsequently applied diffusion steps. For example, in case a p+ diffusion layer 4a is present on the front side 4 of the substrate 2, as shown in Figure 1a and 1b, the applied stack 10 covers this p+ diffusion layer 4a so that when a doped layer 12 on the front side 4 (and back side 6 and edge 8) is obtained through an all side treatment step, the p+ diffusion layer is preserved and protected against further diffusion. In particular, the front side 4 may comprise a p+ diffusion layer 4a covered by the stack 10, where an n+ diffusion layer (n+ doped layer 12) can be provided in the stack 10 on the back side 6, edge 8 and the front side 4 whilst not affecting the p+ diffusion layer 4a.

Figure 1D depicts a further step in this exemplary embodiment of the present invention method wherein removing the stack 10 of the thin oxide layer and polysilicon layer on the front side 4 comprises a selective etching step that is preceded by applying an etch barrier 14 to the back side 6 of the substrate 2, e.g. using a plasma enhanced chemical vapour deposition (PECVD) step. The term selective etching step is to be understood that the etching step has different process parameters, such as etching speed or material etching capability, depending of the material encountered. This embodiment provides optional protection for further treatments steps of the doped layer 12 at the back side 6, so that doping and passivation quality of the doped layer 12 at the back side 6 is retained during further processing. E.g., the thickness of the etch barrier 14, in case deposited by PECVD, may be between about 5 nm and 500nm, e.g. about 100nm. When the etch barrier is deposited by other means, e.g. a screen printing of a barrier paste, its thickness may be much higher, e.g. several μm.

As a further embodiment (shown in Figure 1D), the method may further comprise applying an etch barrier 14 to the back side 6 followed by a removal of parasitic etch barrier material from the front side 4. Here the etch barrier 14 applied to the back side 6 may leave parasitic traces on the front side 4, (indicated as barrier part 14a of the etch barrier 14) which in this embodiment may be removed, e.g. using a (short) HF dip step.

Referring to Figure 1E, in this figure an exemplary embodiment is shown wherein the stack 10 is removed from the front side 4 of the substrate 2. In Figure 1E it is clearly shown that the earlier removal of the rim surface part 5 of the front side 4 (see the step of Figure 1B), now

prevents immediate electrical connection between the first polarity diffusion layer 4a on the front side 4 and the remaining part of the stack 10, in particular the doped layer 12 applied thereto. As there is no electrical connection between the first polarity diffusion layer 4a and the stack 10, it is possible to obtain a good edge isolation and as a result obtain minimized reverse currents in the solar cell (increasing performance thereof).

In an advantageous embodiment the method step of removing the stack 10 of the thin oxide layer and the polysilicon layer on the front side 4 may further comprise one or more selective etching steps. The selective etching steps will first etch the doped layer 12 and furthermore the polysilicon part of stack 10 and finally the thin oxide layer of the stack 10, at appropriate etching rates matching the material being etched. This method step allows efficient and complete removal of the stack 10 on the front side 4 whilst preserving quality of the first polarity diffusion layer 4a. The selective etching of an n-type doped layer 12 may for example be performed by an etchant comprising diluted TMAH (tetra methyl ammonium hydroxide), which etches a p-type doped layer 4a much more slowly, and also etches the thin oxide of stack 10 much more slowly.

During the step of providing the doped layer 12 to the stack 10 on the back side 6, edge 8 and the front side 4 through diffusion, it may happen that some diffusion occurs through the stack 10 into the first polarity diffusion layer 4a. For example, should the substrate 2 be provided with a p+ diffusion layer 4a, it may be possible that when applying an n+ doped layer 12 to the stack 10 some n+ diffusion or leakage occurs into the p+ diffusion layer 4a. In the event that some contamination occurs of the first polarity diffusion layer 4a, an embodiment is provided wherein the first polarity diffusion layer 4a remaining on the front side 4 after removal of the stack 10 of thin oxide layer and polysilicon layer on the front side 4, is subjected to a further etching step as shown in Figure 1F. This method step thus allows for further etching of the first polarity diffusion layer 4a once the stack 10 has been removed. Such further etching step removes any leaked doping into the first polarity diffusion layer 4a that can happen e.g. when applying the doped layer 12 to the stack 10. Such further etching step may for example be performed with an acid etching step with an etching solution comprising nitric acid and hydrofluoric acid. The depth of etching in this further etching step is e.g. between 5 nm and 200 nm.

Figures 2A to 2E depict a schematic overview of consecutive steps of a further method embodiment. The figures 2A to 2C and the associated method steps are similar to the method steps performed as depicted in the embodiment described above with reference to Figure 1A to 1C. Figure 2A shows an embodiment wherein the substrate 2 may be a textured substrate or textured wafer 2. The substrate 2 may be provided with a first polarity diffusion layer 4a on the front side 4 of the substrate 2. In an embodiment the first polarity diffusion layer 4a may be a p+ or n+ type diffusion layer. As depicted the first polarity diffusion layer 4a may be provided to all sides of the substrate 2, i.e. the back side 6, edge 8, and the front side 4, to allow for all side treatment of the substrate 2 to reduce manufacturing complexity.

All method steps prior to applying the stack 10 to the back side 6, edge 8 and front side 4 of the substrate 2 associated with Figures 2A and 2B are similar to the method steps as disclosed

for Figures 1A and 1B. For example, in Figure 2B an embodiment step is shown similar to Figure 1B wherein the first polarity diffusion layer 4a is also removed from a rim surface part 5 of the front side 4 of the substrate 6 (again, e.g. with a width of at most 2 mm).

In the further embodiment step as shown in Figure 2D, the method may comprise a step wherein the stack 10 of the thin oxide layer and the polysilicon layer is further removed from the edge 8 of the substrate. This embodiment provides further electrical isolation or separation between the first polarity diffusion layer 4a and the stack 10, in particular between the first polarity diffusion layer 4a and the stack 10 on the back side 6 of the substrate 2.

Figure 2E also shows that in this embodiment of the method an additional step is executed wherein the stack 10 of the thin oxide layer and the polysilicon layer is further removed from a rim surface part 7 of the back side 6 of the substrate 2. This removal from the rim surface part 7 of the back side 6 can be accomplished by a controlled creep of the single side etchant onto the back side 6 of the substrate 2, e.g. by adjusting the speed of the movement of the substrate 2 in the single etch tool, by adjusting the liquid level in the single side etch tool, and/or by adjusting the viscosity and surface tension of the etchant. This step may also be performed through e.g. a selective etching procedure after applying an etch barrier 14 (see similar step of Figure 1D) and yields even further electrical isolation of the first polarity diffusion layer 4a and the stack 10 with respect to the back side 6.

The rim surface part 7 at the back side 6 of the substrate 2 may furthermore be passivated with a passivating coating such as a silicon oxide/silicon nitride stack or an aluminium oxide/silicon nitride stack.

Utilizing a rim surface part 7 of the back side 6 for electrical isolation (for which a width of at most 2 mm is sufficient) may also be possible for the embodiments as shown in e.g. Figures 1D to 1F. For example, an embodiment is provided wherein the etch barrier 14 is applied to a part of the back side 6 of the substrate 2. In this embodiment a rim surface part 7 of the back side 6 may be left open from the etch barrier 14 for etching so that the rim surface part 7 may be selectively removed by an etching procedure while shielding the stack 10 applied to the part of the back side 6.

Figures 3A to 3E depict a schematic overview of consecutive steps of an even further embodiment of the method according to the present invention. Figure 3A is associated with method steps that are similar to those used for Figure 1A and Figure 2A. That is, Figure 3A shows an embodiment wherein the substrate 2 may be a textured substrate or textured wafer 2. The substrate 2 may be provided with a first polarity diffusion layer 4a on the front side 4 of the substrate 2. Furthermore, the first polarity diffusion layer 4a may be provided to all sides of the substrate 2, i.e. the back side 6, edge 8, and the front side 4, to allow for all side treatment of the substrate 2 to reduce manufacturing complexity. In an embodiment the first polarity diffusion layer 4a may be a p+ or n+ diffusion layer.

Figure 3B shows a further possible processing step for an alternative embodiment of the present invention method wherein a barrier layer 9 is provided on the first polarity diffusion layer 4a on the front side 4 before applying the stack 10 of the thin oxide layer and the polysilicon layer.

The deposited barrier layer 9 shields the first polarity diffusion layer 4a from removal steps (e.g. etchings steps) during subsequent manufacturing. Note that in Figure 3B an embodiment is shown similar to Figure 1B and 2B wherein the first polarity diffusion layer 4a may also be removed from a rim surface part 5 of the front side 4 (and also the corresponding part of the barrier layer 9 is then removed as shown).

The barrier layer 9 may be obtained in a variety of ways. For example, in case a p+ type diffusion layer 4a is to be provided to the substrate 2 (see Figure 3A) then a BSG doping layer may be used in conjunction with an annealing step for obtaining a p+ diffusion layer 4a. However, the BSG doping layer need not be removed when the first polarity diffusion layer 4a on the back side 6 and the edge 8 of the substrate 2 is removed, e.g. using a single side etching step. Then as shown in Figure 3B, a substrate 2 is obtained having a first polarity diffusion layer 4a, i.e. a p+ diffusion layer, covered by the barrier layer 9 comprising the remaining part of the BSG doping layer. Alternatively, the barrier layer 9 can of course be deposited separately before applying the stack 10. The barrier layer 9 enhances the protection of first polarity diffusion layer 4a against indiffusion of dopant from the doping process of stack 10. Further, the barrier layer 9 allows a reduced selectivity of the etching chemistry used for removing stack 10 from the front side 4. In a further embodiment, the barrier layer 9 comprises dopant silicate glass. In an alternative embodiment, the barrier layer 9 comprises a surface passivating layer for the carrier selective contact structure 4a of the first type, such as a layer or layer stack based on thin silicon oxide, aluminium oxide or silicon nitride. In a further advantageous embodiment, the barrier layer 9 is used as a passivating layer and as a base layer of an antireflection coating of the solar cell.

Similar to the method steps associated with Figures 1D, 1E and 2D, in Figure 3D an embodiment step is shown wherein the method step is provided which comprises removal of the stack 10 of the thin oxide layer and the polysilicon layer on the front side 4. A single side etching procedure may be used for this embodiment (similar to the step in Figure 2D), or a selective etching step with provision of an etch barrier (similar to the steps in Figure 1D and 1E).

In a further embodiment, the stack 10 of the thin oxide layer and the polysilicon layer may also be removed from the edge 8 of the substrate 2. In an alternative embodiment, an etch barrier (not shown) may be provided to the back side 6 and optionally to the edge 8, thereby preventing removal of the stack 10 from the back side 6 and edge 8, or only the back side 6, during e.g. an etching procedure. The etch barrier in this embodiment is similarly arranged on the back side 6 and edge 8 as depicted in Figure 1D before removing the stack 10 from the front side 4. Figure 3D shows an embodiment where parts 10a of the stack 10 are indicated which may be removed in this etch step. It is noted that here the parts 10a of the stack 10 are on the edges 8, and on the rim surfaces 7 of the back side 6 (see embodiment of Fig. 2E). As a final processing step in this embodiment, the barrier layer 9 on the front side may be removed as shown in Figure 3E (and in this specific case, the stack 10 is left on the edges 8, providing only the rim surface parts 5 for edge isolation).

The processing steps resulting in the rim surface part 5 on the front side 4 and/or the rim surface part 7 on the back side 6, could be applied in further embodiments for processing a

substrate 2, especially for solar cell applications, as the rim surface parts 5, 7 can advantageously provide a very good edge isolation. To this end, the method steps may comprise providing a stack 10 of a thin dielectric material layer and a polysilicon layer (amorphous or polycrystalline silicon) on (at least a part of) the front side 4 and (at least a part of) the back side 6, subsequently removing the polysilicon layer from the front side (and optionally including removing the polysilicon layer from a rim surface part 7 of the back side 6 to enhance isolation in the final device structure), and subsequently creating a selective carrier contact on the front side 4. The selective carrier contact on the front side 4 and the polysilicon layer on the back side 6 can have opposite polarities. One embodiment for the creation of the selective carrier contact on the front side 4 is by implantation of dopants. Another embodiment is to apply a diffusion barrier on the rear side 6, optionally including a rim surface part 5 on the front side 4, followed by diffusion of a dopant into at least the exposed part of the front side 4. Yet another embodiment comprises deposition of a material known for its selective carrier contacting properties on the front side 4, such as titanium oxide, molybdenum oxide, etc. Applying a material on the back side 6 as well as a rim surface part 5 of the front side 4 which masks or inhibits deposition of the front side selective carrier contact, e.g. applying a silylated surface to inhibit ALD, can be used to enhance isolation in an even further embodiment.

After the processing steps as described in this invention, the solar cells may be finished with passivation and anti-reflection coating layers, and metallisation layers and grids, as known in the art.

The above described exemplary embodiments may be summarized as the following interrelated embodiment descriptions:

Embodiment 1. Method for manufacturing a photovoltaic cell from a substrate (2) having a front side (4), a back side (6) and an edge (8), the method comprising:

providing a carrier selective contact structure (4a) of a first type on at least a part of the front side (4);

applying a stack (10) having a thin oxide layer covered by a polysilicon layer, wherein the stack (10) is applied to the back side (6) and the front side (4) of the substrate (2);

removing the stack (10) of thin oxide layer and polysilicon layer on the front side (4).

Embodiment 2. Method according to embodiment 1, further comprising providing a doped layer (12) on the back side (6), edge (8) and front side (4) of the substrate (2), e.g. by diffusion.

Embodiment 3. Method according to embodiment 1, further comprising providing a doped layer (12) on the back side (6) of the substrate (2).

Embodiment 4. Method according to any one of embodiments 1-3, wherein removing the stack (10) of thin oxide layer and polysilicon layer on the front side (4) comprises a selective etching step preceded by applying an etch barrier (14) to the back side (6) of the substrate (2).

Embodiment 5. Method according to embodiment 4, wherein the etch barrier (14) is applied to a part of the back side (6) of the substrate (2).

Embodiment 6. Method according to embodiment 4 or 5, wherein applying an etch barrier to the back side (6) is followed by a removal of parasitic barrier material from the front side (4).

Embodiment 7. Method according to any one of embodiments 1-3, wherein removing the stack (10) of thin oxide layer and polysilicon layer on the front side (4) comprises a single side etching step.

Embodiment 8. Method according to embodiment 7, wherein the stack (10) of thin oxide layer and polysilicon layer is further removed from the edge (8) of the substrate (2).

Embodiment 9. Method according to embodiment 8, wherein the stack (10) of thin oxide layer and polysilicon layer is further removed from a rim surface part (7) of the back side (6) of the substrate (2).

Embodiment 10. Method according to any one of embodiments 1-9, wherein the thin oxide layer is a thin silicon oxide layer.

Embodiment 11. Method according to any one of embodiments 1-10, wherein the carrier selective contact structure (4a) of the first type is a first polarity diffusion layer (4a) on at least part of the front side (4), e.g. on all sides (4, 6, 8), before applying the stack (10).

Embodiment 12. Method according to embodiment 11, wherein the first polarity diffusion layer (4a) is a p+ diffusion layer.

Embodiment 13. Method according to embodiment 11 or 12, wherein the first polarity diffusion layer (4a) on the back side (6) and the edge (8) of the substrate (2) is removed using a single side etching step.

Embodiment 14. Method according to embodiment 13, wherein the first polarity diffusion layer (4a) is also removed using the single side etching step from a rim surface part (5) of the front side of the substrate (2).

Embodiment 15. Method according to any one of embodiments 11-14, wherein a barrier layer (9) is provided on the first polarity diffusion layer (4a) on the front side (4) before applying the stack (10).

Embodiment 16. Method according to any one of embodiments 11-15, wherein the first polarity diffusion layer (4a) remaining on the front side (4) after removing the stack (10) of thin oxide layer and polysilicon layer on the front side (4), is subjected to a further etching step.

The present invention has been described above with reference to a number of exemplary embodiments as shown in the drawings. Modifications and alternative implementations of some parts or elements are possible, and are included in the scope of protection as defined in the appended claims.

CONCLUSIES

1. Werkwijze voor het vervaardigen van een fotovoltaïsche cel vanuit een substraat (2) met een voorzijde (4), een achterzijde (6) en een zijkant (8), waarbij de werkwijze omvat:

verschaffen van een ladingdrager-selectieve contactstructuur (4a) van een eerste type op ten minste een deel van de voorzijde (4);

aanbrengen van een stapellaag (10) met een dunne oxidelaag die bedekt is door een polysiliciumlaag, waarbij de stapellaag (10) wordt aangebracht op de achterzijde (6) en de voorzijde (4) van het substraat (2);

verwijderen van de stapellaag (10) met dunne oxidelaag en polysiliciumlaag aan de voorzijde (4).

2. Werkwijze volgens conclusie 1, verder omvattende verschaffen van een gedoteerde laag (12) op de achterzijde (6), zijkant (8) en voorzijde (4) van het substraat (2), bijvoorbeeld door diffusie.

3. Werkwijze volgens conclusie 1, verder omvattende verschaffen van een gedoteerde laag (12) op de achterzijde (6) van het substraat (2).

4. Werkwijze volgens één van de conclusies 1-3, waarbij verwijderen van de stapellaag (10) met dunne oxidelaag en polysiliciumlaag op de voorzijde (4) een selectieve etsstap omvat die vooraf gegaan wordt door het aanbrengen van een etsbarrière (14) op de achterzijde (6) van het substraat (2).

5. Werkwijze volgens conclusie 4, waarbij de etsbarrière (14) wordt aangebracht op een deel van de achterzijde (6) van het substraat (2).

6. Werkwijze volgens conclusie 4 of 5, waarbij aanbrengen van een etsbarrière op de achterzijde (6) wordt gevolgd door een verwijdering van parasitair barrièremateriaal aan de voorzijde (4).

7. Werkwijze volgens één van de conclusies 1-3, waarbij verwijderen van de stapellaag(10) met dunne oxidelaag en polysiliciumlaag op de voorzijde (4) een enkele zij-etsstap omvat.

8. Werkwijze volgens conclusie 7, waarbij de stapellaag(10) met dunne oxidelaag en polysiliciumlaag verder wordt verwijderd van de zijkant (8) van het substraat (2).

9. Werkwijze volgens conclusie 8, waarbij de stapellaag(10) met dunne oxidelaag en polysiliciumlaag verder wordt verwijderd van een randoppervlaktedeel (7) van de achterzijde (6) van het substraat (2).

10. Werkwijze volgens één van de conclusies 1-9, waarbij de dunne oxidelaag een dunne siliciumoxidelaag is.

11. Werkwijze volgens één van de conclusies 1-10, waarbij de ladingdrager-selectieve contactstructuur (4a) van het eerste type een diffusielaag van eerste polariteit (4a) is op ten minste een deel van de voorzijde (4), bijvoorbeeld op alle zijden (4, 6, 8), vóór het aanbrengen van de stapellaag(10).

12. Werkwijze volgens conclusie 11, waarbij de diffusielaag van eerste polariteit (4a) een p+ diffusielaag is.

13. Werkwijze volgens conclusie 11 of 12, waarbij de diffusielaag van eerste polariteit (4a) op de achterzijde (6) en de zijkant (8) van het substraat (2) wordt verwijderd met een enkele zij-etsstap.

14. Werkwijze volgens conclusie 13, waarbij de diffusielaag van eerste polariteit (4a) ook met gebruik van de enkele zij-etsstap wordt verwijderd van een randoppervlaktedeel (5) van de voorzijde van het substraat (2).

15. Werkwijze volgens één van de conclusies 11-14, waarbij een barrièrelaag (9) wordt verschaft op de diffusielaag van eerste polariteit (4a) op de voorzijde (4) vóór het aanbrengen van de stapellaag(10).

16. Werkwijze volgens één van de conclusies 11-15, waarbij de diffusielaag van eerste polariteit (4a) die op de voorzijde (4) over blijft na verwijderen van de stapellaag(10) met dunne oxidelaag en polysiliciumlaag op de voorzijde (4), wordt onderworpen aan een verdere etsstap.

******

Fig. 1A

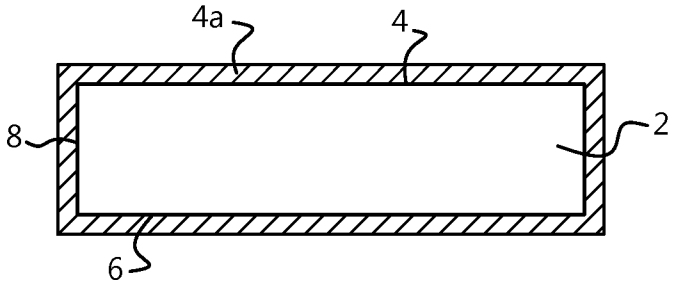


Fig. 1B

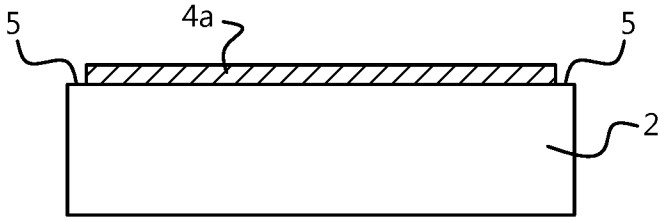


Fig. 1C

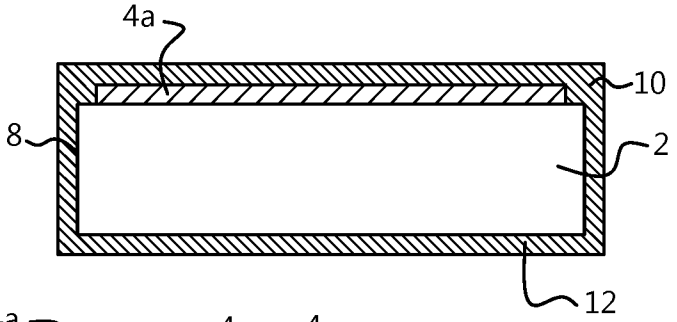


Fig. 1D

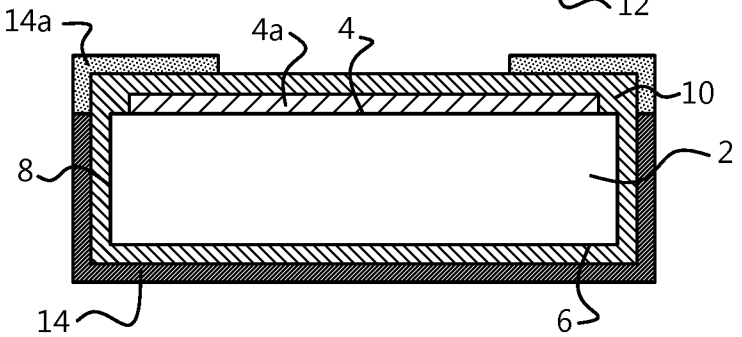


Fig. 1E

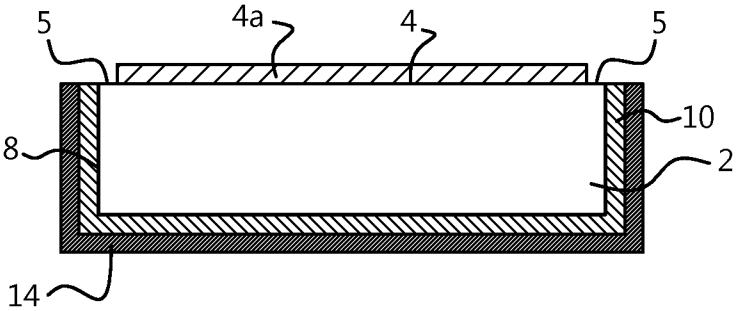


Fig. 1F

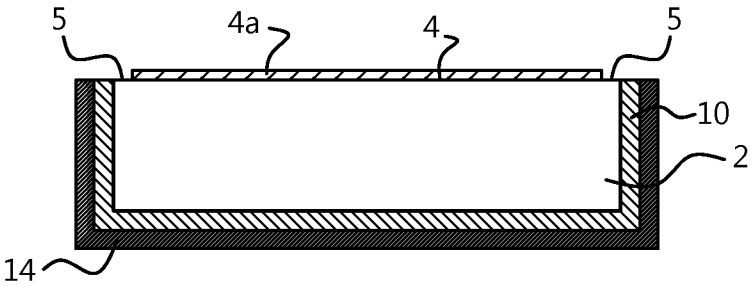


Fig. 2A

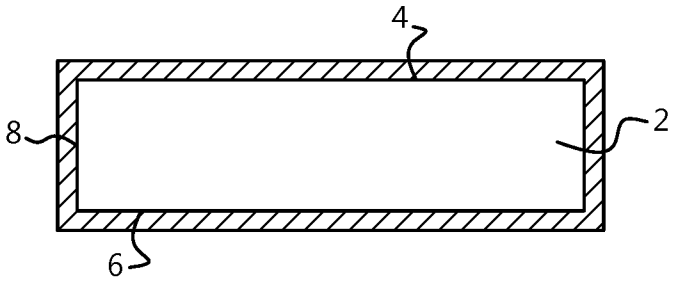


Fig. 2B

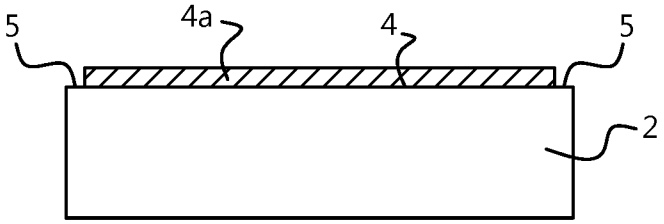


Fig. 2C

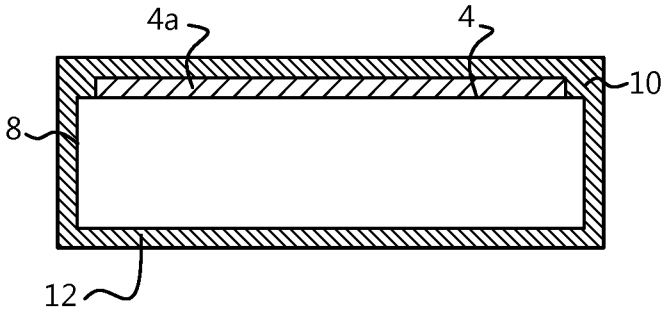


Fig. 2D

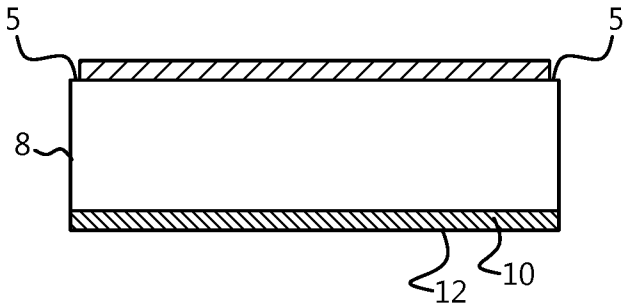


Fig. 2E

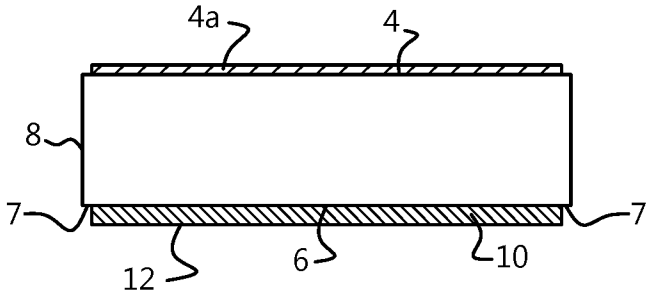


Fig. 3A

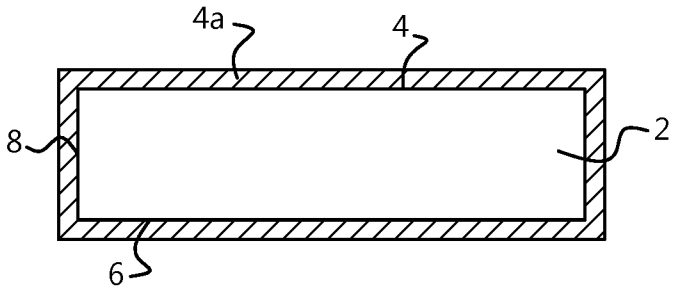


Fig. 3B

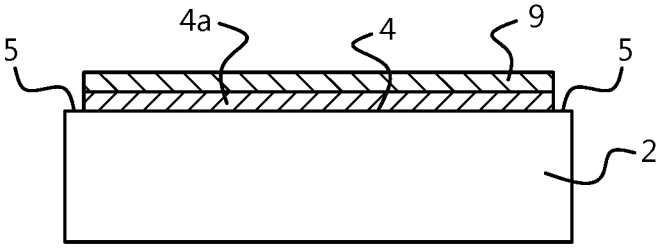


Fig. 3C

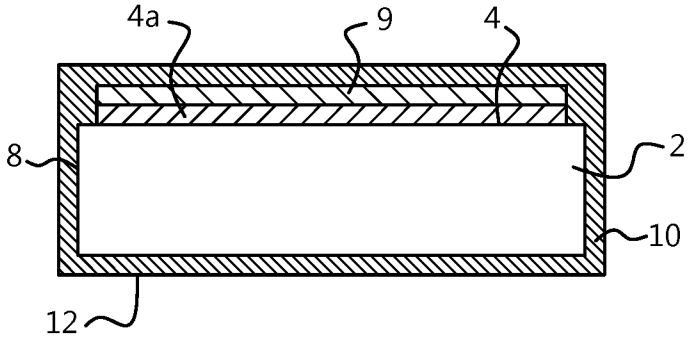


Fig. 3D

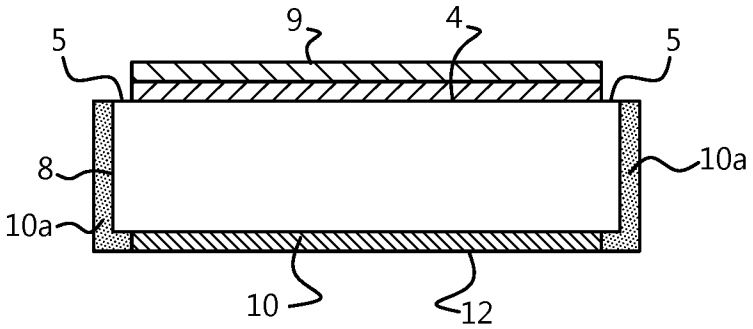
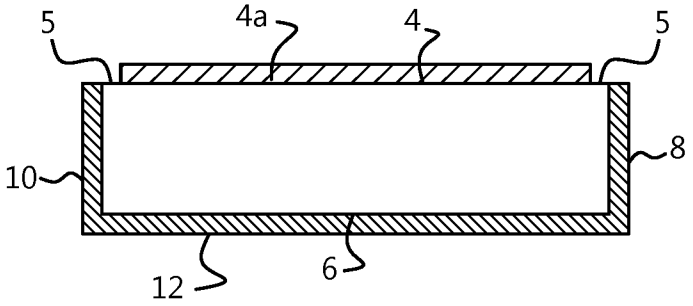


Fig. 3E



ABSTRACT

A method for manufacturing a photovoltaic cell from a substrate (2) having a front side (4), a back side (6) and an edge (8). A carrier selective contact structure (4a) of a first type is provided on at least a part of the front side (4). A stack (10) having a thin oxide layer covered by a polysilicon layer is applied, wherein the stack (10) is applied to the back side (6) and the front side (4) of the substrate (2), and possibly also on edge (8). The stack (10) of thin oxide layer and polysilicon layer on the front side (4) is then removed.

[Fig 1C]

SAMENWERKINGSVERDRAG (PCT)

RAPPORT BETREFFENDE NIEUWHEIDSONDERZOEK VAN INTERNATIONAAL TYPE

IDENTIFICATIE VAN DE NATIONALE AANVRAGE	KENMERK VAN DE AANVRAGER OF VAN DE GEMACHTIGDE
	P6063321NL
Nederlands aanvraag nr. **2018042**	Indieningsdatum **22-12-2016**
	Ingeroepen voorrangsdatum
Aanvrager (Naam) **Stichting Energieonderzoek Centrum Nederland**	
Datum van het verzoek voor een onderzoek van internationaal type **04-02-2017**	Door de Instantie voor Internationaal Onderzoek aan het verzoek voor een onderzoek van internationaal type toegekend nr. **SN68315**

I. CLASSIFICATIE VAN HET ONDERWERP (bij toepassing van verschillende classificaties, alle classificatiesymbolen opgeven)

Volgens de internationale classificatie (IPC)

H01L31/0368;H01L31/068;H01L31/18;H01L31/0745

II. ONDERZOCHTE GEBIEDEN VAN DE TECHNIEK

Onderzochte minimumdocumentatie

Classificatiesysteem	Classificatiesymbolen
IPC	**H01L**

Onderzochte andere documentatie dan de minimum documentatie, voor zover dergelijke documenten in de onderzochte gebieden zijn opgenomen

III.	☐ **GEEN ONDERZOEK MOGELIJK VOOR BEPAALDE CONCLUSIES**	(opmerkingen op aanvullingsblad)
IV.	☐ **GEBREK AAN EENHEID VAN UITVINDING**	(opmerkingen op aanvullingsblad)

ONDERZOEKSRAPPORT BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK VAN HET INTERNATIONALE TYPE

Nummer van het verzoek om een onderzoek naar de stand van de techniek
NL 2018042

A. CLASSIFICATIE VAN HET ONDERWERP
INV. H01L31/0368 H01L31/068 H01L31/18 H01L31/0745
ADD.

Volgens de Internationale Classificatie van octrooien (IPC) of zowel volgens de nationale classificatie als volgens de IPC.

B. ONDERZOCHTE GEBIEDEN VAN DE TECHNIEK

Onderzochte minimum documentatie (classificatie gevolgd door classificatiesymbolen)
H01L

Onderzochte andere documentatie dan de minimum documentatie, voor dergelijke documenten, voor zover dergelijke documenten in de onderzochte gebieden zijn opgenomen

Tijdens het onderzoek geraadpleegde elektronische gegevensbestanden (naam van de gegevensbestanden en, waar uitvoerbaar, gebruikte trefwoorden)
EPO-Internal, WPI Data

C. VAN BELANG GEACHTE DOCUMENTEN

Categorie *	Geciteerde documenten, eventueel met aanduiding van speciaal van belang zijnde passages	Van belang voor conclusie nr.
A	US 2012/073650 A1 (SMITH DAVID [US] ET AL) 29 maart 2012 (2012-03-29) * alineas [0003], [0017] - alinea [0019] * * alinea [0030] - alinea [0039]; figuren 4,5 * -----	1-16
A,D	US 7 633 006 B1 (SWANSON RICHARD M [US]) 15 december 2009 (2009-12-15) in de aanvraag genoemd * kolom 2, regel 63 - kolom 6, regel 54; figuren 1-13 * -----	1-16

-/--

[X] Verdere documenten worden vermeld in het vervolg van vak C.

[X] Leden van dezelfde octrooifamilie zijn vermeld in een bijlage

* Speciale categorieën van aangehaalde documenten

"A" niet tot de categorie X of Y behorende literatuur die de stand van de techniek beschrijft

"D" in de octrooiaanvrage vermeld

"E" eerdere octrooi(aanvrage), gepubliceerd op of na de indieningsdatum, waarin dezelfde uitvinding wordt beschreven

"L" om andere redenen vermelde literatuur

"O" niet-schriftelijke stand van de techniek

"P" tussen de voorrangsdatum en de indieningsdatum gepubliceerde literatuur

"T" na de indieningsdatum of de voorrangsdatum gepubliceerde literatuur die niet bezwarend is voor de octrooiaanvrage, maar wordt vermeld ter verheldering van de theorie of het principe dat ten grondslag ligt aan de uitvinding

"X" de conclusie wordt als niet nieuw of niet inventief beschouwd ten opzichte van deze literatuur

"Y" de conclusie wordt als niet inventief beschouwd ten opzichte van de combinatie van deze literatuur met andere geciteerde literatuur van dezelfde categorie, waarbij de combinatie voor de vakman voor de hand liggend wordt geacht

"&" lid van dezelfde octrooifamilie of overeenkomstige octrooipublicatie

Datum waarop het onderzoek naar de stand van de techniek van internationaal type werd voltooid	Verzenddatum van het rapport van het onderzoek naar de stand van de techniek van internationaal type
3 augustus 2017	

Naam en adres van de instantie	De bevoegde ambtenaar
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hofmann, Kerrin

1

ONDERZOEKSRAPPORT BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK VAN HET INTERNATIONALE TYPE

Nummer van het verzoek om een onderzoek naar de stand van de techniek
NL 2018042

C.(Vervolg). VAN BELANG GEACHTE DOCUMENTEN

Categorie *	Geciteerde documenten, eventueel met aanduiding van speciaal van belang zijnde passages	Van belang voor conclusie nr.
A	REICHEL CHRISTIAN ET AL: "Tunnel oxide passivated contacts formed by ion implantation for applications in silicon solar cells", JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS, US, deel 118, nr. 20, 28 november 2015 (2015-11-28), XP012202759, ISSN: 0021-8979, DOI: 10.1063/1.4936223 [gevonden op 1901-01-01] * samenvatting * * bladzijde 1, linker kolom - bladzijde 3, linker kolom *	1-16
A	EP 2 703 368 A1 (DU PONT [US]) 5 maart 2014 (2014-03-05) * alinea [0081] - alinea [0091]; figuren 1A-1F *	1-16
A	US 2014/352769 A1 (BATEMAN NICHOLAS P T [US]) 4 december 2014 (2014-12-04) * alinea [0018] - alinea [0033]; figuren 1,2 *	1-16

ONDERZOEKSRAPPORT BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK VAN HET INTERNATIONALE TYPE

Informatie over leden van dezelfde octrooifamilie

Nummer van het verzoek om een onderzoek naar de stand van de techniek: NL 2018042

In het rapport genoemd octrooigeschrift	Datum van publicatie	Overeenkomend(e) geschrift(en)	Datum van publicatie
US 2012073650 A1	29-03-2012	AU 2011306011 A1	10-01-2013
		CN 102959738 A	06-03-2013
		CN 105789375 A	20-07-2016
		EP 2619806 A1	31-07-2013
		JP 5837600 B2	24-12-2015
		JP 2013538009 A	07-10-2013
		JP 2016076709 A	12-05-2016
		KR 20130109992 A	08-10-2013
		US 2012073650 A1	29-03-2012
		WO 2012039831 A1	29-03-2012
US 7633006 B1	15-12-2009	US 7468485 B1	23-12-2008
		US 7633006 B1	15-12-2009
EP 2703368 A1	05-03-2014	CN 103681949 A	26-03-2014
		EP 2703368 A1	05-03-2014
		JP 2014049743 A	17-03-2014
		KR 20140030009 A	11-03-2014
		US 2014060632 A1	06-03-2014
US 2014352769 A1	04-12-2014	GEEN	

WRITTEN OPINION

File No.	Filing date *(day/month/year)*	Priority date *(day/month/year)*	Application No.
SN68315	22.12.2016		NL2018042

International Patent Classification (IPC)
INV. H01L31/0368 H01L31/068 H01L31/18 H01L31/0745

Applicant
Stichting Energieonderzoek Centrum Nederland

This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the application
- ☐ Box No. VIII Certain observations on the application

	Examiner
	Hofmann, Kerrin

Application number

WRITTEN OPINION

NL2018042

Box No. I Basis of this opinion

1. This opinion has been established on the basis of the latest set of claims filed before the start of the search.
2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material:

   ☐ on paper

   ☐ in electronic form

   c. time of filing/furnishing:

   ☐ contained in the application as filed.

   ☐ filed together with the application in electronic form.

   ☐ furnished subsequently for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
4. Additional comments:

Box No. V Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty	Yes:	Claims	1-16
	No:	Claims	
Inventive step	Yes:	Claims	1-16
	No:	Claims	
Industrial applicability	Yes:	Claims	1-16
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following documents:

D1 US 2012/073650 A1 (SMITH DAVID [US] ET AL) 29 maart 2012 (2012-03-29)

D2 US 7 633 006 B1 (SWANSON RICHARD M [US]) 15 december 2009 (2009-12-15) in de aanvraag genoemd

D3 REICHEL CHRISTIAN ET AL: "Tunnel oxide passivated contacts formed by ion implantation for applications in silicon solar cells", JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS, US, deel 118, nr. 20, 28 november 2015 (2015-11-28), XP012202759, ISSN: 0021-8979, DOI: 10.1063/1.4936223 [gevonden op 1901-01-01]

D4 EP 2 703 368 A1 (DU PONT [US]) 5 maart 2014 (2014-03-05)

D5 US 2014/352769 A1 (BATEMAN NICHOLAS P T [US]) 4 december 2014 (2014-12-04)

2 INDEPENDENT CLAIM 1

2.1 D1 is regarded as being the prior art closest to the subject-matter of claim 1, and discloses (see references in parentheses):

Werkwijze voor het vervaardigen van een fotovoltaische cel vanuit een substraat (wafer 404, 406, 408; fig. 4; 502, fig. 5) *met een voorzijde* (see par. 31; wafers 406, 408 are positioned back-to-back, fig. 4B; upper side, fig. 5), *een achterzijde* (see par. 31; lower side, fig. 5) *en een zijkant* (see par. 31; left and right side, fig. 5), *waarbij de werkwijze omvat:*
verschaffen van een ladingdrager-selectieve contactstructuur (n- or p-type doped region in layer 506, fig. 5; par. 39) *van een eerste type op ten minste een deel van de voorzijde* (upper side, fig. 5);
aanbrengen van een stapellaag (504, 506) *met een dunne oxidelaag* (410, fig. 4C; 504, fig. 5; par. 32, 37) *die bedekt is door een polysiliciumlaag* (506, fig. 5; par. 37), ...

2.2 The subject-matter of claim 1 therefore differs from this known D1 in that the stack is applied to the **back side** and the **front side** of the substrate; and in that the stack of the thin oxide layer and the polysilicon layer is **removed** on the **front side**.

2.3 The subject-matter of claim 1 is therefore new.

2.4 The problem to be solved by the present invention may be regarded as providing an improved manufacturing method for solar cells comprising rear side polysilicon passivating contacts. The method allows efficient use of manufacturing steps for protecting sides of the solar cell during various treatment steps.

2.5 The solution to this problem proposed in claim 1 of the present application is considered as involving an inventive step for the following reasons:

2.5.1 None of the available **prior art** documents discloses the above difference or anything within an obvious modification of the above difference.

2.5.1.1 **D1** itself prevents a deposition on all layers of the stack on both front and rear side due to the wafer back-to-back position in a furnace. Therefore there is no need to remove the stack from an unwanted side.

2.5.1.2 In **D2** APCVD is used to deposit various layers on top of a tunnel oxide layer on a back side of a silicon substrate. The tunnel oxide is deposited on both sides and the front side tunnel oxide is removed in a later process step. The various layers include a poly-Si layer on top of the tunnel oxide layer, followed by a layer of p-type dopant and a layer of undoped silicon oxide. In an optional later process step an additional tunnel oxide layer and poly-Si layer is applied to the front side. The poly-Si layer not applied on back and front side during the same processing step.

2.5.1.3 In **D3**, passivated contacts (poly-Si/SiO_x/c-Si) are formed by dry-chemically growing a tunnel oxide layer and depositing intrinsic or in-situ doped a-Si layers, followed by overcompensation doping of the opposite dopant. Photoresist masks are used to protect undoped areas. As usual, a-Si becomes poly-Si after high-temperature anneal. D2 does not disclose any removal of the stack from a front surface.

2.5.1.4 **D4** and **D5** do not relate to passivated poly-Si contacts but provide methods where an n-type emitter layer is deposited on all sides of a wafer and subsequently removed from all sides but the front side (D3) or implanted on the backside and the edges of the wafer (D4). No tunnel oxide layer is present.

2.6 Claims 2-16 are dependent on claim 1 and as such also meet the requirements of novelty and inventive step.