(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 4 403 364 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
24.07.2024 Bulletin 2024/30

(21) Application number: **23205891.7**

(22) Date of filing: **25.10.2023**

(51) International Patent Classification (IPC):
B41J 2/045 *(2006.01)*

(52) Cooperative Patent Classification (CPC):
B41J 2/04541; B41J 2/04548; B41J 2/0455; B41J 2/04581

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC ME MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA
Designated Validation States:
KH MA MD TN

(30) Priority: **19.01.2023 JP 2023006653**

(71) Applicant: **Toshiba Tec Kabushiki Kaisha**
Shinagawa-ku
Tokyo 141-8562 (JP)

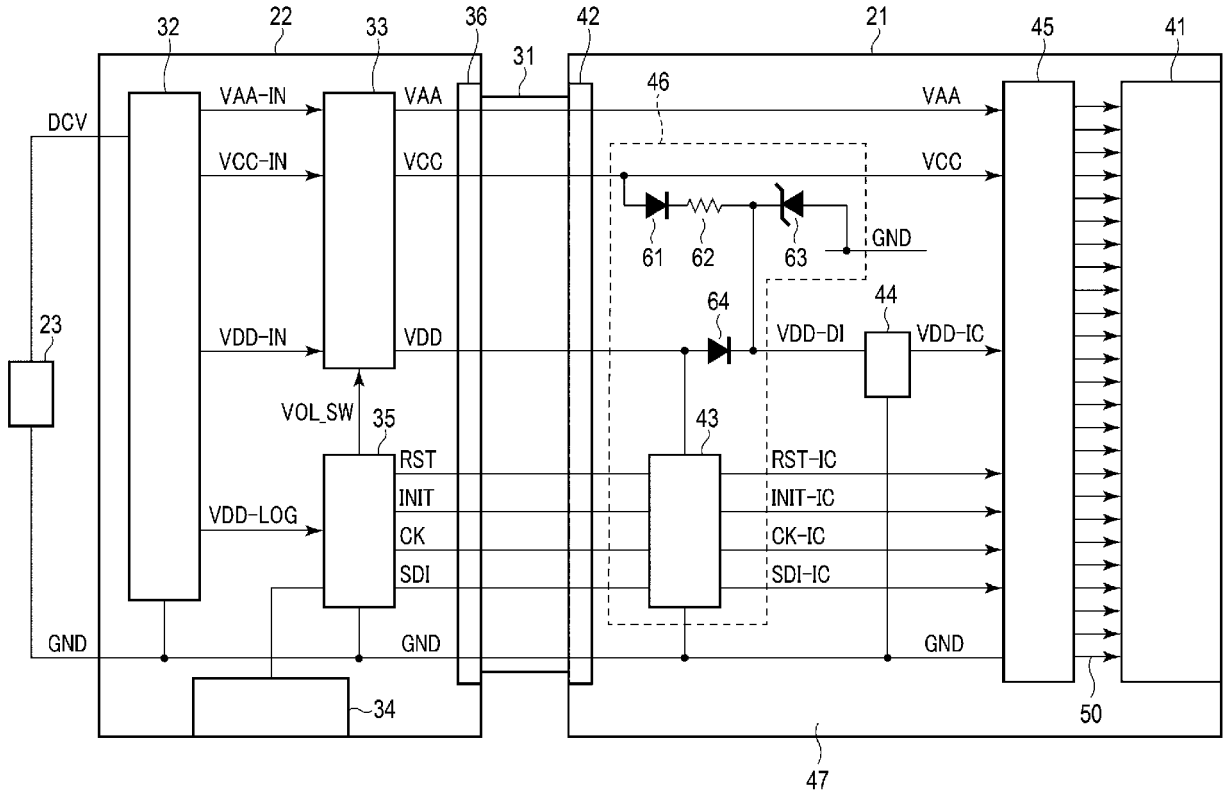
(72) Inventor: **Hiyoshi, Teruyuki**
141-8562 Tokyo (JP)

(74) Representative: **Bandpay & Greuter**
11 rue Christophe Colomb
75008 Paris (FR)

(54) **INKJET HEAD AND INKJET PRINTER**

(57) According to one embodiment, there is provided an inkjet head including a driver IC, a logic power supply circuit, and a first diode. The driver IC includes a logic circuit and a level shifter. The logic power supply circuit inputs a first voltage to a power supply input terminal thereof and supplies a voltage to the logic circuit. The first diode is provided with an anode connected to a second voltage input to the level shifter and a cathode connected to the power supply input terminal of the logic power supply circuit.

FIG. 2



EP 4 403 364 A1

Description

FIELD

[0001] Embodiments described herein relate generally to an inkjet head and an inkjet printer.

BACKGROUND

[0002] An inkjet printer that forms an image on a print medium in accordance with print data is put into practical use. The inkjet printer includes, for example, an inkjet head and a head controller that controls the inkjet head.

[0003] The inkjet head includes an actuator for ejecting ink and a driver IC for driving the actuator under the control of the head controller.

[0004] The head controller supplies a plurality of power supply voltages to the driver IC of the inkjet head. The head controller inputs and interrupts the plurality of power supply voltages based on a predetermined order. With this configuration, the head controller prevents a through-current from flowing in the driver IC.

[0005] However, even if the head controller inputs and interrupts the plurality of power supply voltages in the predetermined order, if a connection failure exists in a wiring that connects the head controller and the driver IC, the order of inputting the power supply voltage supplied to the driver IC does not correspond to the predetermined order.

[0006] In order to cope with such an event, a technique for supplying power by connecting a signal line for supplying a control signal to the driver IC is provided.

[0007] In the related art, if the control signal is not in a high level state, the power supply voltage supplied to the driver IC may not be ensured.

DISCLOSURE OF INVENTION

[0008] To this end, there is provided an inkjet head comprising: a driver IC that includes a logic circuit and a level shifter; a logic power supply circuit that inputs a first voltage to a power supply input terminal thereof and supplies a voltage to the logic circuit; and a first diode that is provided with an anode connected to a second voltage input to the level shifter and a cathode connected to the power supply input terminal of the logic power supply circuit.

[0009] Preferred embodiments of the inkjet head are set out in dependent claims.

[0010] There is also provided an inkjet printer comprising: an inkjet head that ejects ink onto a print medium; and a head controller that supplies a first voltage and a second voltage to the inkjet head, wherein the inkjet head includes a driver IC that includes a logic circuit and a level shifter, a logic power supply circuit that inputs the first voltage to a power supply input terminal thereof and supplies a voltage to the logic circuit, and a first diode that is provided with an anode connected to the second voltage input to the level shifter and a cathode connected to the power supply input terminal of the logic power supply circuit.

DESCRIPTION OF THE DRAWINGS

[0011]

FIG. 1 is a block diagram illustrating a configuration example of an inkjet printer according to an embodiment;
FIG. 2 is a circuit diagram conceptually illustrating a configuration example of an inkjet head and a head controller;
FIG. 3 is a circuit diagram illustrating a configuration example of a recovery circuit;
FIG. 4 is a diagram illustrating a configuration example of a driver IC;
FIG. 5 is a timing chart illustrating an operation of the head controller and the inkjet head during normality;
FIG. 6 is a timing chart illustrating the operation of the head controller and the inkjet head during normality;
FIG. 7 is a timing chart illustrating an operation of the head controller and the inkjet head during abnormality; and
FIG. 8 is a timing chart illustrating the operation of the head controller and the inkjet head during abnormality.

DETAILED DESCRIPTION

[0012] Embodiments provide an inkjet head and an inkjet printer having high safety.

[0013] In general, according to one embodiment, there is provided an inkjet head including a driver IC, a logic power supply circuit, and a first diode. The driver IC includes a logic circuit and a level shifter. The logic power supply circuit inputs a first voltage to a power supply input terminal thereof and supplies a voltage to the logic circuit. The first diode is provided with an anode connected to a second voltage input to the level shifter and a cathode connected to the power supply input terminal of the logic power supply circuit.

[0014] Hereinafter, embodiments will be described with reference to the drawings.

[0015] An inkjet printer and an inkjet head according to an embodiment will be described below with reference to the drawings.

[0016] First, an inkjet printer 1 according to an embodiment will be described. FIG. 1 is a block diagram illustrating a configuration example of the inkjet printer 1 according to the embodiment.

[0017] The inkjet printer 1 is an example of an inkjet recording apparatus. The inkjet recording apparatus is not limited to the inkjet printer 1, and may be another apparatus such as a copying machine.

[0018] The inkjet printer 1, for example, performs various kinds of processing such as image formation while conveying a print medium, which is a recording medium. The inkjet printer 1 includes a central processing unit (CPU) 11, a read only memory (ROM) 12, a random access memory (RAM) 13, a communication interface 14, a display 15, an operation unit 16, a conveyance motor 17, a motor drive circuit 18, a pump 19, a pump drive circuit 20, an inkjet head 21, a head controller 22, and a power supply circuit 23. Furthermore, the inkjet printer 1 includes a paper feed cassette and a paper discharge tray (not illustrated).

[0019] The CPU 11 is an operation element (for example, a processor) that executes operation processing. The CPU 11 performs various kinds of processing based on data such as a program stored in the ROM 12. The CPU 11 functions as a control unit capable of executing various operations by executing the program stored in the ROM 12.

[0020] The ROM 12 is a read-only non-volatile memory. The ROM 12 stores a program, data used in the program, and the like.

[0021] The RAM 13 is a volatile memory that functions as a working memory. The RAM 13 temporarily stores data being processed by the CPU 11. The RAM 13 also temporarily stores the program executed by the CPU 11.

[0022] The communication interface 14 is an interface for communicating with other devices. The communication interface 14 is used, for example, for communication with a host device that transmits a print command to the inkjet printer 1. The communication interface 14 may perform wireless communication with other devices according to standards such as Bluetooth (registered trademark) or Wi-fi (registered trademark).

[0023] The display 15 is a display device that displays a screen according to a video signal input from the CPU 11 or a display control unit such as a graphic controller (not illustrated). For example, the display 15 displays a screen for setting the inkjet printer 1.

[0024] The operation unit 16 generates an operation signal based on the operation. The operation unit 16 is, for example, a touch sensor, ten keys, a power key, a paper feed key, various function keys, or a keyboard. The touch sensor is, for example, a resistance film type touch sensor, or a capacitance type touch sensor. The touch sensor acquires information indicating a designated position within a certain area. The touch sensor is configured as a touch panel integrated with the display 15 to generate a signal indicating a touched position on the screen displayed on the display 15.

[0025] The conveyance motor 17 rotates to operate conveyance members of a conveyance path (not illustrated) for conveying the print medium. The conveyance members are a belt, a roller, a guide, and the like for conveying the print medium. The conveyance motor 17 conveys the print medium along the guide by driving the roller that operates in interlocking with the belt that holds the print medium.

[0026] The motor drive circuit 18 is a circuit that drives the conveyance motor 17. The motor drive circuit 18 conveys the print medium in the paper feed cassette to the paper discharge tray via the inkjet head 21 by driving the conveyance motor 17 according to a conveyance control signal input from the CPU 11. The paper feed cassette is a cassette that accommodates a plurality of print media. The paper discharge tray accommodates the print medium on which an image is formed by the inkjet printer 1 and discharged.

[0027] The pump 19 includes, for example, a tube that communicates an ink tank (not illustrated) that stores ink with the inkjet head 21. Specifically, the tube communicates with a common ink chamber (not illustrated) of the inkjet head 21.

[0028] The pump drive circuit 20 drives the pump 19 according to an ink supply control signal input from the CPU 11 to supply the ink in the ink tank to the common ink chamber of the inkjet head 21.

[0029] The inkjet head 21 is an image forming unit that forms an image on the print medium. The inkjet head 21 forms an image by ejecting ink onto the print medium conveyed by the conveyance motor 17 and a holding roller (not illustrated) based on a power supply voltage and a control signal supplied from the head controller 22. The inkjet printer 1 may include a plurality of inkjet heads 21 corresponding to respective colors such as cyan, magenta, yellow, and black.

[0030] The head controller 22 is a circuit that controls the inkjet head 21. The head controller 22 causes ink to be ejected from the inkjet head 21 by operating the inkjet head 21. The head controller 22 supplies a plurality of power supply voltages to the inkjet head 21. The head controller 22 generates the control signal based on the print command input via the communication interface 14. The head controller 22 causes the inkjet head 21 to form an image on the print medium by supplying the power supply voltage and the control signal.

[0031] The power supply circuit 23 converts AC power supplied from a commercial power source into DC power. The power supply circuit 23 supplies the DC power to each component in the inkjet printer 1.

[0032] FIG. 2 is a circuit diagram illustrating a detailed configuration of the inkjet head 21 and the head controller 22. The inkjet head 21 and the head controller 22 are connected to each other via a transmission flexible printed circuit (FPC) board (hereinafter referred to as a transmission FPC 31). With this configuration, the head controller 22 can supply the power supply voltage and the control signal to the inkjet head 21.

[0033] First, the head controller 22 will be described.

[0034] The head controller 22 includes a power supply voltage generator 32, a power supply sequence circuit 33, a first communication interface 34, a control IC 35, and a second communication interface 36.

[0035] The power supply voltage generator 32 generates the plurality of power supply voltages necessary for the operation of the inkjet head 21 and a power supply

voltage necessary for the operation of the control IC 35 using a DC voltage DCV supplied from the power supply circuit 23. The DC voltage DCV is, for example, 39 V.

[0036] For example, the power supply voltage generator 32 generates a power supply voltage VAA-IN, a power supply voltage VCC-IN, a power supply voltage VDD-IN, and a power supply voltage VDD-LOG using the DC voltage DCV. The power supply voltage VAA-IN is a power supply voltage for generating a power supply voltage VAA used in the inkjet head 21. The power supply voltage VAA-IN is, for example, 20 V The power supply voltage VCC-IN is a power supply voltage for generating a power supply voltage VCC used in the inkjet head 21. The power supply voltage VCC-IN is, for example, 39 V. The power supply voltage VDD-IN is a power supply voltage for generating a power supply voltage VDD used in the inkjet head 21. The power supply voltage VDD-IN is, for example, 5 V The power supply voltage VDD-LOG is a power supply voltage for operating the control IC 35. The power supply voltage VDD-LOG is, for example, 5 V.

[0037] The power supply voltage generator 32 supplies the power supply voltage VAA-IN, the power supply voltage VCC-IN, and the power supply voltage VDD-IN to the power supply sequence circuit 33. The power supply voltage generator 32 supplies the power supply voltage VDD-LOG to the control IC 35.

[0038] The power supply sequence circuit 33 inputs and interrupts each power supply voltage to the inkjet head 21. The power supply sequence circuit 33 inputs and interrupts each power supply voltage to the inkjet head 21 if the power supply sequence circuit 33 is in an enabled state. Further, if the power supply sequence circuit 33 is in a disabled state, the power supply sequence circuit 33 does not input and interrupt each power supply voltage. The power supply sequence circuit 33 switches between the enabled state and the disabled state under the control of the control IC 35.

[0039] The power supply sequence circuit 33 outputs the power supply voltage VAA, the power supply voltage VCC (second voltage), and the power supply voltage VDD (first voltage) to the inkjet head 21 based on the power supply voltage VAA-IN, the power supply voltage VCC-IN, and the power supply voltage VDD-IN supplied from the power supply voltage generator 32.

[0040] The power supply sequence circuit 33 starts (input) the output of each power supply voltage based on a preset order (sequence). The power supply sequence circuit 33 stops (interrupts) the output of each power supply voltage based on a preset order (sequence). The power supply sequence circuit 33 inputs the power supply voltages in the order of the power supply voltage VDD, the power supply voltage VCC, and the power supply voltage VAA if the power is input. The power supply sequence circuit 33 interrupts the power supply voltages in the order of the power supply voltage VAA, the power supply voltage VCC, and the power supply voltage VDD if the power is interrupted.

[0041] The first communication interface 34 is an interface that connects the CPU 11 or communication interface 14 and the control IC 35. The print command input to the first communication interface 34 from the host device connected via the communication interface 14 or from the CPU 11 is supplied to the control IC 35.

[0042] The control IC 35 operates with the power supply voltage VDD-LOG. The control IC 35 generates the control signal based on the print command input via the first communication interface 34. The control signal includes a clock signal CK, a reset signal RST, an initialization signal INIT, print data SDI, and the like. The control IC 35 outputs the control signals to the inkjet head 21 via the transmission FPC 31.

[0043] The control IC 35 also generates a switching signal VOL-SW for switching the operation of the power supply sequence circuit 33 between the enabled state and the disabled state. The control IC 35 switches the operation of the power supply sequence circuit 33 between the enabled state and the disabled state by inputting the switching signal VOL-SW to the power supply sequence circuit 33. For example, if the control IC 35 is started up by being supplied with the power supply voltage VDD-LOG, the control IC 35 switches the operation of the power supply sequence circuit 33 to the enabled state. The control IC 35 switches the operation of the power supply sequence circuit 33 to the disabled state if a predetermined signal is received from the CPU 11.

[0044] The second communication interface 36 is an interface that connects the inkjet head 21 and the head controller 22. The second communication interface 36 is provided with various terminals to which the transmission FPC 31 is connected.

[0045] For example, the second communication interface 36 is provided with four terminals connected to an output terminal for the power supply voltage VAA of the power supply sequence circuit 33, two terminals connected to an output terminal for the power supply voltage VCC of the power supply sequence circuit 33, and one terminal connected to an output terminal for the power supply voltage VDD of the power supply sequence circuit 33. The second communication interface 36 is also provided with one terminal connected to an output terminal for the clock signal CK of the control IC 35, one terminal connected to an output terminal for the reset signal RST of the control IC 35, one terminal connected to an output terminal for the initialization signal INIT of the control IC 35, and one terminal connected to an output terminal for the print data SDI of the control IC 35. In addition, the second communication interface 36 is provided with seven terminals that are grounded. The transmission FPC 31 is also provided with a plurality of wirings connected to respective terminals of the second communication interface 36.

[0046] The power supply voltage VAA, the power supply voltage VCC, and the power supply voltage VDD output from the power supply sequence circuit 33, and the clock signal CK, the reset signal RST, the initialization signal INIT, and the print data SDI output from the control

IC 35 are supplied to the inkjet head 21 connected via the second communication interface 36 and the transmission FPC 31.

[0047] The number of terminals provided in the second communication interface 36 and the number of wirings (number of cores) in the transmission FPC 31 can be determined based on the current consumption in the inkjet head 21, and are not limited to the numbers described above. That is, the number of terminals and wirings may be changed as appropriate according to the specifications of the inkjet head 21 and the head controller 22.

[0048] Next, the inkjet head 21 will be described.

[0049] The inkjet head 21 includes a channel group 41, a communication interface 42, a logic power supply voltage generator 44, a driver IC 45, a recovery circuit 46, a head substrate 47, and an electrode group 50. The channel group 41, the communication interface 42, the logic power supply voltage generator 44, the driver IC 45, the recovery circuit 46, and the electrode group 50 are mounted on the head substrate 47.

[0050] FIG. 3 is a circuit diagram illustrating a configuration example of the recovery circuit 46. As illustrated in FIG. 3, the recovery circuit 46 includes a buffer IC 43, a first diode 61, a resistor 62, a Zener diode 63, and a second diode 64.

[0051] The channel group 41 is a member that ejects ink. The channel group 41 is configured by arranging a plurality of channels for ejecting ink according to an applied voltage. The channel group 41 includes a first piezoelectric member joined to the head substrate 47, a second piezoelectric member joined to the first piezoelectric member, a plurality of electrodes, and a nozzle plate.

[0052] The first piezoelectric member and the second piezoelectric member are joined such that polarization directions thereof are opposite to each other. A plurality of parallel grooves extending from a side of the second piezoelectric member to the first piezoelectric member are formed in the first piezoelectric member and the second piezoelectric member. The electrode is formed in each groove. The first piezoelectric member and the second piezoelectric member sandwiched between two electrodes formed in two grooves are configured as actuators that are deformed by a potential difference between the two electrodes.

[0053] The nozzle plate is the member that seals the grooves. In the nozzle plate, a plurality of ejection nozzles for communicating the groove with the outside of the inkjet head 21 are formed in each groove. The groove sealed by the nozzle plate is filled with ink by the pump 19 and functions as a pressure chamber whose walls are configured with a pair of actuators.

[0054] If a drive waveform is input from the driver IC 45 to the electrode of the actuator that configures the wall of the pressure chamber, the actuator is deformed and the volume of the pressure chamber changes. With this configuration, pressure in the pressure chamber changes, and ink in the pressure chamber is ejected from the ejection nozzle. In this example, a combination of the pressure chamber and the ejection nozzle is referred to as a channel. That is, the channel group 41 is provided with channels corresponding to the number of grooves.

[0055] The communication interface 42 is an interface for connecting the inkjet head 21 and the head controller 22. The communication interface 42 is provided with various terminals to which the transmission FPC 31 is connected.

[0056] The communication interface 42 is provided with a plurality of power supply voltage input terminals to which the power supply voltage is supplied from the head controller 22 and a plurality of control signal input terminals to which the control signal is supplied from the head controller 22. For example, the communication interface 42 is provided with four VAA input terminals respectively connected to a plurality of wirings for transmitting the power supply voltage VAA in the transmission FPC 31. The VAA input terminals are respectively connected to the power supply input terminals of the driver IC 45 for the power supply voltage VAA. The communication interface 42 is also provided with two VCC input terminals respectively connected to a plurality of wirings for transmitting the power supply voltage VCC in the transmission FPC 31. The VCC input terminals are respectively connected to power supply input terminals of the driver IC 45 for the power supply voltage VCC. At least one of the VCC input terminals is connected in parallel to an anode of the first diode 61 and the power supply input terminal of the driver IC 45 for the power supply voltage VCC. With this configuration, the power supply voltage VAA and the power supply voltage VCC are supplied from the head controller 22 to the recovery circuit 46 and the driver IC 45 via the transmission FPC 31 and the communication interface 42.

[0057] The communication interface 42 is also provided with one VDD input terminal connected to the wiring for transmission of the power supply voltage VDD in the transmission FPC 31. The VDD input terminal is connected in parallel to an anode of the second diode 64 and a power supply input terminal of the buffer IC 43. A cathode of the second diode 64 is connected to a power supply input terminal of the logic power supply voltage generator 44 of the driver IC 45. With this configuration, the power supply voltage VDD is supplied from the head controller 22 to the logic power supply voltage generator 44 and the buffer IC 43 via the transmission FPC 31 and the communication interface 42.

[0058] The communication interface 42 is also provided with one CK input terminal connected to the wiring for transmission of the clock signal CK in the transmission FPC 31 and connected to the signal input terminal for the clock signal CK of the buffer IC 43. The communication interface 42 is also provided with one RST input terminal connected to the wiring for transmission of the reset signal RST in the transmission FPC 31 and connected to the signal input terminal for the reset signal RST of the buffer IC 43. The communication interface 42 is also pro-

vided with one INIT input terminal connected to the wiring for transmission of the initialization signal INIT in the transmission FPC 31 and connected to the signal input terminal for the initialization signal INIT of the buffer IC 43. The communication interface 42 is also provided with one SDI input terminal connected to the wiring for transmission of the print data SDI in the transmission FPC 31 and connected to the signal input terminal for the print data SDI of the buffer IC 43. The communication interface 42 is also provided with seven GND terminals that are grounded. With this configuration, the clock signal CK, the reset signal RST, the initialization signal INIT, and the print data SDI are supplied from the head controller 22 to the buffer IC 43 via the transmission FPC 31 and the communication interface 42.

[0059] The buffer IC 43 is connected to the VDD input terminal of the communication interface 42 and operates with the power supply voltage VDD. The buffer IC 43 has an input-tolerant function. The buffer IC 43 changes (normalizes) a voltage level of the control signal supplied from the head controller 22 via the transmission FPC 31 and the communication interface 42, generates a control signal for controlling the driver IC 45, and supplies the control signal to the driver IC 45. For example, the buffer IC 43 normalizes the clock signal CK input to the signal input terminal for the clock signal CK and converts the clock signal CK into a clock signal CK-IC. The buffer IC 43 normalizes the reset signal RST input to the signal input terminal for the reset signal RST and converts the reset signal RST into a reset signal RST-IC. The buffer IC 43 normalizes the initialization signal INIT input to the signal input terminal for the initialization signal INIT and converts the initialization signal INIT into an initialization signal INIT-IC. The buffer IC 43 normalizes the print data SDI input to the signal input terminal for the print data SDI and converts the print data SDI into print data SDI-IC. The buffer IC 43 inputs the clock signal CK-IC, the reset signal RST-IC, the initialization signal INIT-IC, and the print data SDI-IC to the driver IC 45.

[0060] Each signal input terminal of the buffer IC 43 is configured as an input protection circuit. That is, the buffer IC 43 is an IC having a configuration with the input-tolerant function, in which each of the signal input terminal for the clock signal CK, the signal input terminal for the reset signal RST, the signal input terminal for the initialization signal INIT, and the signal input terminal for the print data SDI is not connected to a diode on a positive side (forward direction from signal input terminal to power supply input terminal). With this configuration, even if the voltage of the signal input to the signal input terminal becomes higher than the power supply voltage VDD, the current can be prevented from flowing from the signal input terminal to the power supply input terminal.

[0061] The logic power supply voltage generator 44 (logic power supply circuit) converts the power supply voltage VDD into a power supply voltage VDD-IC according to the specifications of the driver IC 45. The logic power supply voltage generator 44 inputs the power supply voltage VDD-IC to the driver IC 45.

[0062] The driver IC 45 is connected to the power supply voltage input terminals such as the VAA input terminal, the VCC input terminal, the VDD input terminal, and the like of the communication interface 42, the logic power supply voltage generator 44, the buffer IC 43, and the like. The driver IC 45 drives the channel group 41 based on the control signals output from the buffer IC 43.

[0063] The driver IC 45 generates a drive waveform based on the control signals such as the clock signal CK-IC, the reset signal RST-IC, the initialization signal INIT-IC, and the print data SDI-IC input from the buffer IC 43 with the power supply voltage VAA, the power supply voltage VCC, the power supply voltage VDD-IC as the power supply input. The driver IC 45 inputs the drive waveform to the electrodes of the actuator of the channel group 41 via the electrode group 50 to deform the actuator and change the volume of the pressure chamber. With this configuration, the driver IC 45 causes ink in the pressure chamber to be ejected from the ejection nozzle.

[0064] FIG. 4 is a diagram illustrating a configuration example of the driver IC 45. The driver IC 45 includes a logic circuit 51, a level shifter 52, and a driver 53.

[0065] The logic circuit 51 operates with the power supply voltage VDD-IC. The logic circuit 51 generates a drive signal for controlling the switching element of the driver 53 based on the signal CK-IC, the reset signal RST-IC, the initialization signal INIT-IC, and the print data SDI-IC input as the control signals. The logic circuit 51 inputs the drive signal to the level shifter 52. The logic circuit 51 includes a register that temporarily stores the print data SDI-IC.

[0066] The terminals to which the control signals of the logic circuit 51 are input are also configured as the input protection circuit. That is, each of the signal input terminal for the clock signal CK-IC, the signal input terminal for the reset signal RST-IC, the signal input terminal for the initialization signal INIT-IC, and the signal input terminal for the print data SDI-IC is not connected to a diode on a positive side (forward direction from signal input terminal to power supply input terminal). With this configuration, even if the voltage of the signal input to the signal input terminal becomes higher than the power supply voltage VDD-IC, the current can be prevented from flowing from the signal input terminal to the power supply input terminal.

[0067] The level shifter 52 converts a voltage level of the drive signal input from the logic circuit 51 using the power supply voltage VCC. The level shifter 52 inputs the drive signal whose voltage level is converted to the driver 53.

[0068] The driver 53 is provided with two switching elements, each of which is configured with a p-MOSFET and an n-MOSFET, for each electrode of the channel group 41, for example. A gate of the switching element is connected to an output terminal of the level shifter 52. A source of the p-MOSFET is connected to the power supply voltage VAA, and a source of the n-MOSFET is

connected to GND. The electrodes of the channel group 41 are connected to respective drains of two switching elements, which are connection points of the two switching elements. With such a configuration, the driver 53 outputs the power supply voltage VAA or a GND level at timing in accordance with the drive signal input from the level shifter 52. Thus, the driver 53 inputs the drive waveform to each electrode of the channel group 41. As a result, the driver 53 causes ink to be ejected from the ejection nozzles of the channel group 41.

[0069] The recovery circuit 46 reduces the voltage of the VCC input terminal of the communication interface 42 to supply the voltage to the power supply input terminal of the logic circuit 51 of the driver IC 45, and prevents the potential of the power supply input terminal of the logic circuit 51 of the driver IC 45 (or the power supply input terminal of the logic power supply voltage generator 44) from being supplied to the power supply input terminal of the buffer IC 43. The recovery circuit 46 supplies the power supply voltage VDD to the logic power supply voltage generator 44 as the power supply voltage VDD-DI (first voltage).

[0070] As described above, the recovery circuit 46 includes the buffer IC 43, the first diode 61, the resistor 62, the Zener diode 63, and the second diode 64.

[0071] The first diode 61 has an anode connected to the VCC input terminal as the power supply input terminal of the communication interface 42, and a cathode connected to the power supply input terminal of the logic power supply voltage generator 44 via the resistor 62. The first diode 61 is a Schottky diode.

[0072] A connection point 70 is formed between the cathode of the first diode 61 and the power supply input terminal of the logic power supply voltage generator 44. The resistor 62 is formed between the cathode of the first diode 61 and the connection point 70.

[0073] The resistor 62 reduces the power supply voltage VCC from the VCC input terminal and supplies the power supply voltage VCC to the logic power supply voltage generator 44. For example, the resistance value of the resistor 62 is 10 KΩ.

[0074] As described above, the second diode 64 has an anode connected to the VDD input terminal as the power supply voltage input terminal of the communication interface 42 and a cathode connected to the connection point 70. The second diode 64 is a Schottky diode.

[0075] The Zener diode 63 also has an anode connected to the ground and a cathode connected to the connection point 70. The Zener diode 63 sets the upper limit of the voltage supplied to the logic power supply voltage generator 44. For example, the Zener voltage of the Zener diode 63 is 4.8 V.

[0076] In the configuration described above, the power supply voltage VDD-DI becomes 4.6 V if a connection failure does not occur in a path through which the power supply voltage VDD is transmitted. The logic power supply voltage generator 44 is supplied with the current primarily from the VDD input terminal, but is supplied with the current of 3.4 mA from the VCC input terminal.

[0077] If the connection failure occurs in the path through which the power supply voltage VDD is transmitted, the power supply voltage VDD-DI is supplied from the VCC input terminal to the logic power supply voltage generator 44 via the first diode 61 and the resistor 62. The power supply voltage VDD-DI also becomes 4.6 V The logic power supply voltage generator 44 is supplied with the current of 3.4 mA from the VCC input terminal.

[0078] In this case, since the supply of power to the buffer IC 43 is stopped, the buffer IC 43 does not transmit the control signal to the driver IC 45. That is, the control signal is at a substantial GND level. Therefore, since the clock signal CK-IC is not supplied to the logic circuit 51 of the driver IC 45, the driver IC 45 does not consume power. Accordingly, even if the current from the logic power supply voltage generator 44 to the logic circuit 51 is reduced, the potential of the power supply voltage VDD-IC of the logic circuit 51 is maintained, and thus no problem arises.

[0079] Next, the operation if the connection failure does not exist in the path through which the power supply voltage VDD is transmitted (during normality) will be described.

[0080] FIG. 5 is a timing chart illustrating the operation of the head controller 22 and the inkjet head 21 during normality. In FIG. 5, the horizontal axis indicates time and the vertical axis indicates voltage. FIG. 6 is a timing chart illustrating VCC (power supply voltage VCC), VDD (power supply voltage VDD), and VDD-DI (power supply voltage VDD-DI) in FIG. 5. In FIG. 6, the horizontal axis indicates time and the vertical axis indicates voltage.

[0081] At timing t1, if the inkjet printer 1 is powered on, the DC voltage DCV is supplied from the power supply circuit 23 to the head controller 22.

[0082] If the DC voltage DCV is supplied, at timing t2, the power supply voltage generator 32 generates the power supply voltage VAA-IN, the power supply voltage VCC-IN, the power supply voltage VDD-IN, and the power supply voltage VDD-LOG. The power supply voltage generator 32 supplies the power supply voltage VAA-IN, the power supply voltage VCC-IN, and the power supply voltage VDD-IN to the power supply sequence circuit 33 and supplies the power supply voltage VDD-LOG to the control IC 35.

[0083] At timing t3, if the print command is input to the control IC 35, the control IC 35 supplies the switching signal VOL-SW, which brings the power supply sequence circuit 33 into the enabled state, to the power supply sequence circuit 33. That is, the control IC 35 sets the switching signal VOL-SW to an H level. If the power supply sequence circuit 33 is brought into the enabled state by the switching signal VOL-SW, the power supply sequence circuit 33 starts outputting the power supply voltage VDD, the power supply voltage VCC, and the power supply voltage VAA in this order.

[0084] At timing t4, the power supply sequence circuit 33 starts outputting the power supply voltage VDD. At

this time, the recovery circuit 46 supplies the power supply voltage VDD to the logic power supply voltage generator 44 as the power supply voltage VDD-DI. At timing t4, the logic power supply voltage generator 44 of the inkjet head 21 supplies the power supply voltage VDD-IC to the driver IC 45. At timing t4, the control IC 35 starts outputting the clock signal CK and the initialization signal INIT to the buffer IC 43 of the inkjet head 21. At timing t4, the buffer IC 43 normalizes the clock signal CK and the initialization signal INIT, and supplies the clock signal CK-IC and the initialization signal INIT-IC to the driver IC 45.

[0085] At timing t5, the control IC 35 starts outputting the reset signal RST to the buffer IC 43 of the inkjet head 21. At timing t5, the buffer IC 43 normalizes the reset signal RST and supplies the reset signal RST-IC to the driver IC 45.

[0086] At timing t6, the power supply sequence circuit 33 starts outputting the power supply voltage VCC. Thus, the power supply voltage VCC is supplied to the driver IC 45.

[0087] At timing t7, the power supply sequence circuit 33 starts outputting the power supply voltage VAA. Thus, the power supply voltage VAA is supplied to the driver IC 45.

[0088] At timing t8, the control IC 35 starts outputting the print data SDI to the buffer IC 43 of the inkjet head 21. At timing t8, the buffer IC 43 normalizes the print data SDI and supplies the print data SDI-IC to the driver IC 45.

[0089] At timing t9, the control IC 35 causes the inkjet head 21 to start printing. For example, the control IC 35 lowers the initialization signal INIT from the H level to an L level by a predetermined number of clocks (for example, by one clock) at timing t9 if the output of the print data SDI for one line is completed. Thus, the initialization signal INIT-IC that the buffer IC 43 inputs to the driver IC 45 is also lowered to the L level. The logic circuit 51 of the driver IC 45 starts generating the drive signal using the clock signal CK-IC, the print data SDI-IC, and the power supply voltage VDD-IC with the fact that the initialization signal INIT-IC is lowered to the L level as a trigger. Thus, the level shifter 52 and the driver 53 start operating, and the drive waveform is input to the electrodes of the channel group 41. As a result, printing is executed.

[0090] At timing t10, if the control IC 35 recognizes that printing is completed, the control IC 35 supplies the switching signal VOL-SW, which brings the power supply sequence circuit 33 into the disabled state, to the power supply sequence circuit 33. That is, the control IC 35 sets the switching signal VOL-SW to the L level. If the power supply sequence circuit 33 is brought into the disabled state by the switching signal VOL-SW, the power supply sequence circuit 33 stops outputting the power supply voltage VAA, the power supply voltage VCC, and the power supply voltage VDD in this order.

[0091] At timing 111, the power supply sequence circuit 33 stops outputting the power supply voltage VAA. Thus, the supply of the power supply voltage VAA to the driver IC 45 is stopped.

[0092] At timing t12, the power supply sequence circuit 33 stops outputting the power supply voltage VCC. Thus, the supply of the power supply voltage VCC to the driver IC 45 is stopped.

[0093] At timing t13, the power supply sequence circuit 33 stops outputting the power supply voltage VDD. At timing t13, the control IC 35 stops outputting the clock signal CK, the reset signal RST, and the initialization signal INIT. That is, at timing t13, the control IC 35 lowers the clock signal CK, the reset signal RST, and the initialization signal INIT from the H level to the L level. Thus, the clock signal CK-IC, the reset signal RST-IC, and the initialization signal INIT-IC supplied from the buffer IC 43 to the driver IC 45 are also lowered from the H level to the L level. The recovery circuit 46 stops outputting the power supply voltage VDD-DI. Thus, the power supply voltage is not supplied to the power supply input terminal of the logic power supply voltage generator 44 as well. As a result, the supply of the power supply voltage VDD-IC to the driver IC 45 is stopped.

[0094] Next, the operation if the connection failure exists in the path through which the power supply voltage VDD is transmitted (during abnormality) will be described.

[0095] FIG. 7 is a timing chart illustrating the operation of the head controller 22 and the inkjet head 21 during abnormality. In FIG. 7, the horizontal axis indicates time and the vertical axis indicates voltage. FIG. 8 is a timing chart illustrating VCC (power supply voltage VCC), VDD (power supply voltage VDD) and VDD-DI (power supply voltage VDD-DI) in FIG. 7. In FIG. 8, the horizontal axis indicates time and the vertical axis indicates voltage.

[0096] At timing t1, if the inkjet printer 1 is powered on, the DC voltage DCV is supplied from the power supply circuit 23 to the head controller 22.

[0097] If the DC voltage DCV is supplied, at timing t2, the power supply voltage generator 32 generates the power supply voltage VAA-IN, the power supply voltage VCC-IN, the power supply voltage VDD-IN, and the power supply voltage VDD-LOG. The power supply voltage generator 32 supplies the power supply voltage VAA-IN, the power supply voltage VCC-IN, and the power supply voltage VDD-IN to the power supply sequence circuit 33 and supplies the power supply voltage VDD-LOG to the control IC 35.

[0098] At timing t3, if the print command is input to the control IC 35, the control IC 35 supplies the switching signal VOL-SW, which brings the power supply sequence circuit 33 into the enabled state, to the power supply sequence circuit 33. That is, the control IC 35 sets the switching signal VOL-SW to the H level. If the power supply sequence circuit 33 is brought into the enabled state by the switching signal VOL-SW, the power supply sequence circuit 33 starts outputting the power supply voltage VDD, the power supply voltage VCC, and the power supply voltage VAA in this order.

[0099] At timing t4, the power supply sequence circuit 33 starts outputting the power supply voltage VDD. However, when the connection failure exists in the path through which the power supply voltage VDD is transmitted, the power supply voltage VDD is not supplied to the logic power supply voltage generator 44 and the buffer IC 43 of the inkjet head 21. At timing t4, the control IC 35 starts outputting the clock signal CK and the initialization signal INIT to the buffer IC 43 of the inkjet head 21. Since the power supply voltage VDD is not supplied, the buffer IC 43 continues to stop operating. Therefore, the clock signal CK-IC and the initialization signal INIT-IC are not supplied from the buffer IC 43 to the driver IC 45.

[0100] At timing t5, the control IC 35 starts outputting the reset signal RST to the buffer IC 43 of the inkjet head 21. However, since the buffer IC 43 is not operating, the reset signal RST-IC is not supplied to the driver IC 45.

[0101] At timing t6, the power supply sequence circuit 33 starts outputting the power supply voltage VCC. Thus, the power supply voltage VCC is supplied to the driver IC 45. The power supply voltage VCC is input to the power supply input terminal of the logic power supply voltage generator 44 via the first diode 61 and the resistor 62 as the power supply voltage VDD-DI. The upper limit of the power supply voltage VDD-DI is set by the Zener diode 63. The logic power supply voltage generator 44 generates the power supply voltage VDD-IC using the power supply voltage VDD-DI and starts supplying the power supply voltage VDD-IC to the driver IC 45.

[0102] At timing t7, the power supply sequence circuit 33 starts outputting the power supply voltage VAA. Thus, the power supply voltage VAA is supplied to the driver IC 45.

[0103] At timing t8, the control IC 35 starts outputting the print data SDI to the buffer IC 43 of the inkjet head 21. However, since the buffer IC 43 is not operating, the print data SDI-IC is not supplied to the driver IC 45. In this case, printing is not executed.

[0104] At timing t9, the control IC 35 causes the inkjet head 21 to start printing. For example, the control IC 35 lowers the initialization signal INIT from the H level to the L level by a predetermined number of clocks (for example, by one clock) at timing t9 if the output of the print data SDI for one line is completed. However, since the buffer IC 43 is not operating, printing is not executed.

[0105] At timing t10, the control IC 35 supplies the switching signal VOL-SW, which brings the power supply sequence circuit 33 into the disabled state, to the power supply sequence circuit 33. That is, the control IC 35 sets the switching signal VOL-SW to the L level. If the power supply sequence circuit 33 is brought into the disabled state by the switching signal VOL-SW, the power supply sequence circuit 33 stops outputting the power supply voltage VAA, the power supply voltage VCC, and the power supply voltage VDD in this order.

[0106] At timing 111, the power supply sequence circuit 33 stops outputting the power supply voltage VAA. Thus, the supply of the power supply voltage VAA to the driver IC 45 is stopped.

[0107] At timing t12, the power supply sequence circuit 33 stops outputting the power supply voltage VCC. Thus, the supply of the power supply voltage VCC to the driver IC 45 is stopped. The recovery circuit 46 stops outputting the power supply voltage VDD-DI. Thus, the power supply voltage VDD-DI supplied to the power supply input terminal of the logic power supply voltage generator 44 is interrupted. As a result, the supply of the power supply voltage VDD-IC to the driver IC 45 is stopped.

[0108] At timing t13, the power supply sequence circuit 33 stops outputting the power supply voltage VDD. At timing t13, the control IC 35 stops outputting the clock signal CK, the reset signal RST, and the initialization signal INIT. That is, at timing t13, the control IC 35 lowers the clock signal CK, the reset signal RST, and the initialization signal INIT from the H level to the L level.

[0109] For example, if the power supply voltage VAA and the power supply voltage VCC are supplied to the driver IC 45 and the power supply voltage VDD-IC is not supplied to the driver IC 45, the drive signal is not supplied from the logic circuit 51 to the level shifter 52. The level shifter 52 is in an indefinite state if the power supply voltage VCC is supplied and the drive signal is not supplied from the logic circuit 51. In this case, the level shifter 52 may turn on the two switching elements of the driver 53 at the same time. If the two switching elements of the driver 53 are turned on at the same time, the power supply voltage VAA is applied to conductive paths of the two switching elements, and a through-current flows.

[0110] However, as described above, even if the connection failure exists in the path through which the power supply voltage VDD is transmitted, and the power supply voltage VDD is not supplied to the buffer IC 43 and the logic power supply voltage generator 44, the recovery circuit 46 can supply the power supply voltage VCC to the power supply input terminal of the logic power supply voltage generator 44 via the first diode 61 and the resistor 62. With this configuration, the logic power supply voltage generator 44 can generate the power supply voltage VDD-IC using the power supply voltage VCC. That is, the logic power supply voltage generator 44 can ensure the potential of the power supply input terminal to which the power supply voltage VDD-IC of the logic circuit 51 is input by the power supply voltage VCC. As a result, the recovery circuit 46 can prevent the through-current from flowing in the driver 53 even if the drive signal is not supplied from the logic circuit 51 to the level shifter 52 and the level shifter 52 is in the indefinite state. That is, the inkjet head 21 and the inkjet printer 1 according to this embodiment have high safety.

[0111] In addition, the buffer IC 43 is in a state of not inputting the control signal to the driver IC 45 if the power supply voltage VDD is not supplied. That is, the buffer IC 43 is in a state of inputting the clock signal CK-IC, the reset signal RST-IC, the initialization signal INIT-IC, and the print data SDI-IC, all of which are at the substantial

GND level, to the logic circuit 51 of the driver IC 45. In this case, since the logic circuit 51 of the driver IC 45 is not supplied with the clock signal CK-IC which is the reference clock, the logic circuit 51 does not operate and is in a state of not consuming power. Thus, the potential of the power supply input terminal of the logic circuit 51 can be ensured with the minimum current. As a result, the burden of power on the control IC 35 of the head controller 22 can be reduced.

[0112] The second diode 64, which prevents the power supply voltage VDD-DI generated by the power supply voltage VCC from being inputted to the power supply input terminal of the buffer IC 43, is connected between the power supply input terminal of the buffer IC 43 and the connection point 70. With this configuration, the buffer IC 43 can be prevented from being operated if the connection failure exists in the path through which the power supply voltage VDD is transmitted. Further, if the connection failure exists in the path through which the power supply voltage VDD is transmitted, by preventing the buffer IC 43 and the driver IC 45 from being operated, the detection of defects by the control IC 35 of the head controller 22 can be facilitated.

[0113] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the inventions. The accompanying claims are intended to cover such forms or modifications as would fall within the scope of the inventions.

Claims

1. An inkjet head (21) comprising:

a driver IC (45) that includes a logic circuit and a level shifter;
a logic power supply circuit that inputs a first voltage to a power supply input terminal thereof and supplies a voltage to the logic circuit; and
a first diode (61) that is provided with an anode connected to a second voltage input to the level shifter and a cathode connected to the power supply input terminal of the logic power supply circuit.

2. The head according to claim 1, wherein the first diode is a Schottky diode.

3. The head according to claim 1 or 2, further comprising:

a buffer IC (43) that inputs the first voltage to a power supply input terminal thereof and supplies a control signal to the logic circuit; and
a second diode (64) that is provided with an anode connected to the power supply input terminal of the buffer IC and a cathode connected to a connection point between the cathode of the first diode and the power supply input terminal of the logic power supply circuit.

4. The head according to claim 3, further comprising:
a Zener diode that is provided with an anode connected to GND and a cathode connected to the connection point.

5. The head according to claim 3 or 4, further comprising:
a resistor that is formed between the cathode of the first diode and the connection point.

6. The head according to any one of claims 3 to 5, wherein
the buffer IC is provided with an input-tolerant function.

7. The head according to any one of claims 3 to 6, wherein
each signal input terminal of the buffer IC is configured as an input protection circuit.

8. The head according to any one of claims 3 to 7, wherein

the driver IC further includes a driver,
the logic circuit generates a drive signal, and
the level shifter converts a voltage level of the drive signal input from the logic circuit and inputs the converted drive signal to the driver.

9. An inkjet printer comprising:

an inkjet head (21) that ejects ink onto a print medium; and
a head controller that supplies a first voltage and a second voltage to the inkjet head, wherein
the inkjet head includes

a driver IC (45) that includes a logic circuit and a level shifter,
a logic power supply circuit that inputs the first voltage to a power supply input terminal thereof and supplies a voltage to the logic circuit, and
a first diode (61) that is provided with an anode connected to the second voltage input to the level shifter and a cathode connected to the power supply input terminal of the logic power supply circuit.

FIG. 1

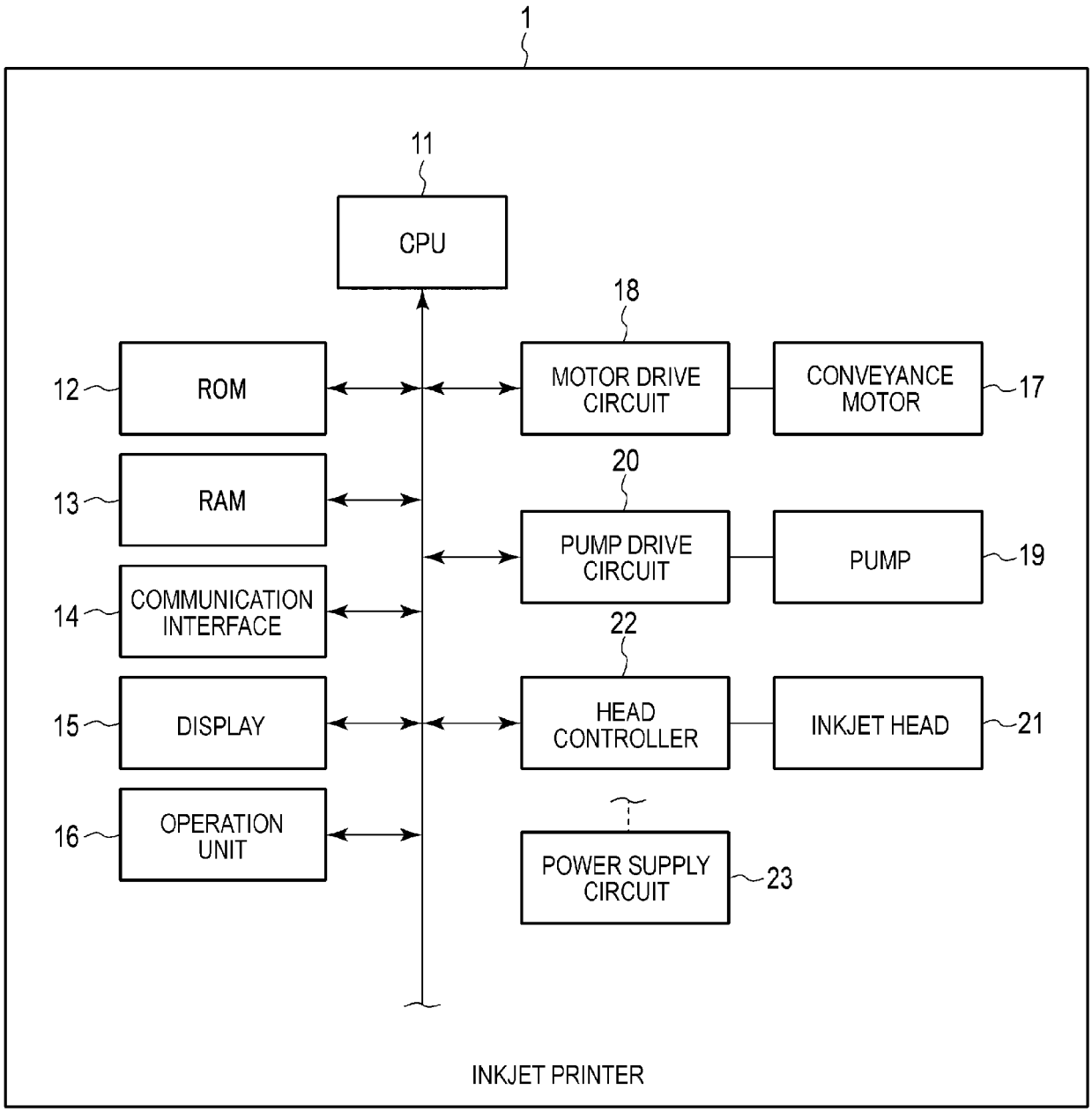

1
11
CPU
18
12
ROM
MOTOR DRIVE CIRCUIT
CONVEYANCE MOTOR
17
20
13
RAM
PUMP DRIVE CIRCUIT
PUMP
19
14
COMMUNICATION INTERFACE
22
15
DISPLAY
HEAD CONTROLLER
INKJET HEAD
21
16
OPERATION UNIT
POWER SUPPLY CIRCUIT
23
INKJET PRINTER

FIG. 2

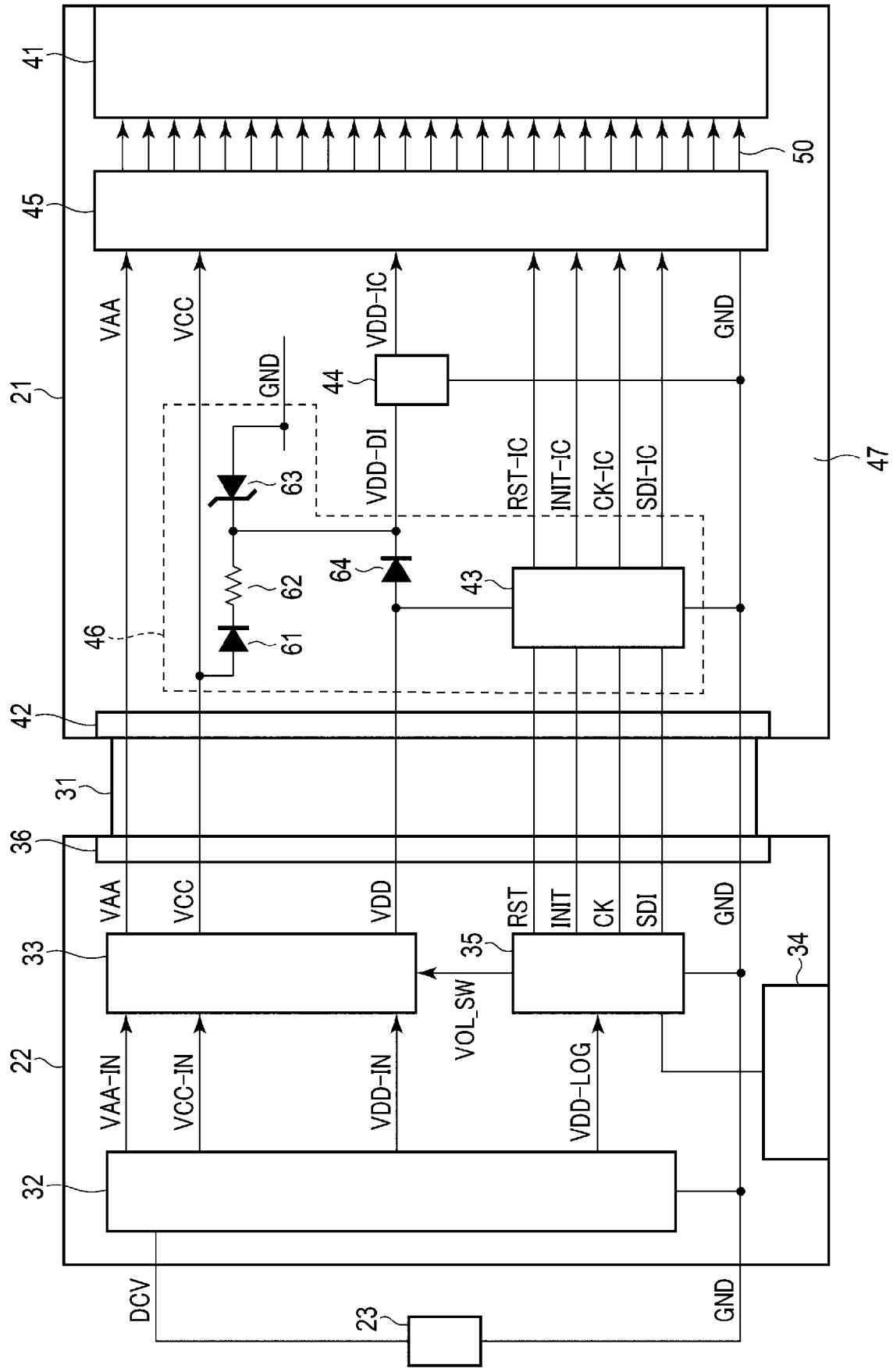

41
50
45
VAA
VCC
GND
VDD-IC
44
21
GND
63
VDD-DI
RST-IC
INIT-IC
CK-IC
SDI-IC
47
64
62
43
46
61
42
31
36
VAA
VCC
VDD
RST
INIT
CK
SDI
GND
33
35
34
VOL_SW
22
VAA-IN
VCC-IN
VDD-IN
VDD-LOG
32
DCV
23
GND

FIG. 3

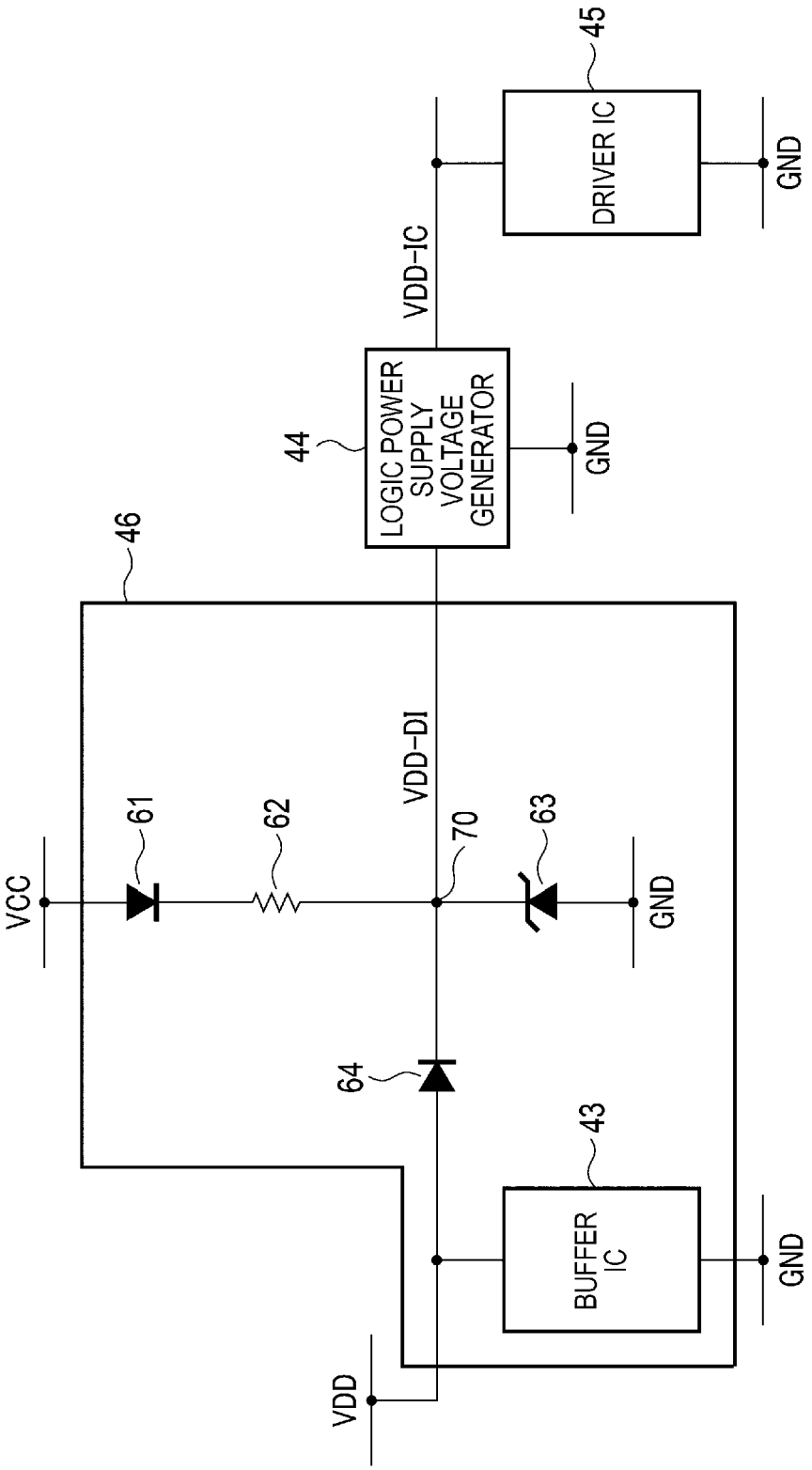

45
DRIVER IC
GND
VDD-IC
44
LOGIC POWER SUPPLY VOLTAGE GENERATOR
GND
46
VDD-DI
VCC
61
62
70
63
GND
64
43
BUFFER IC
GND
VDD

FIG. 4

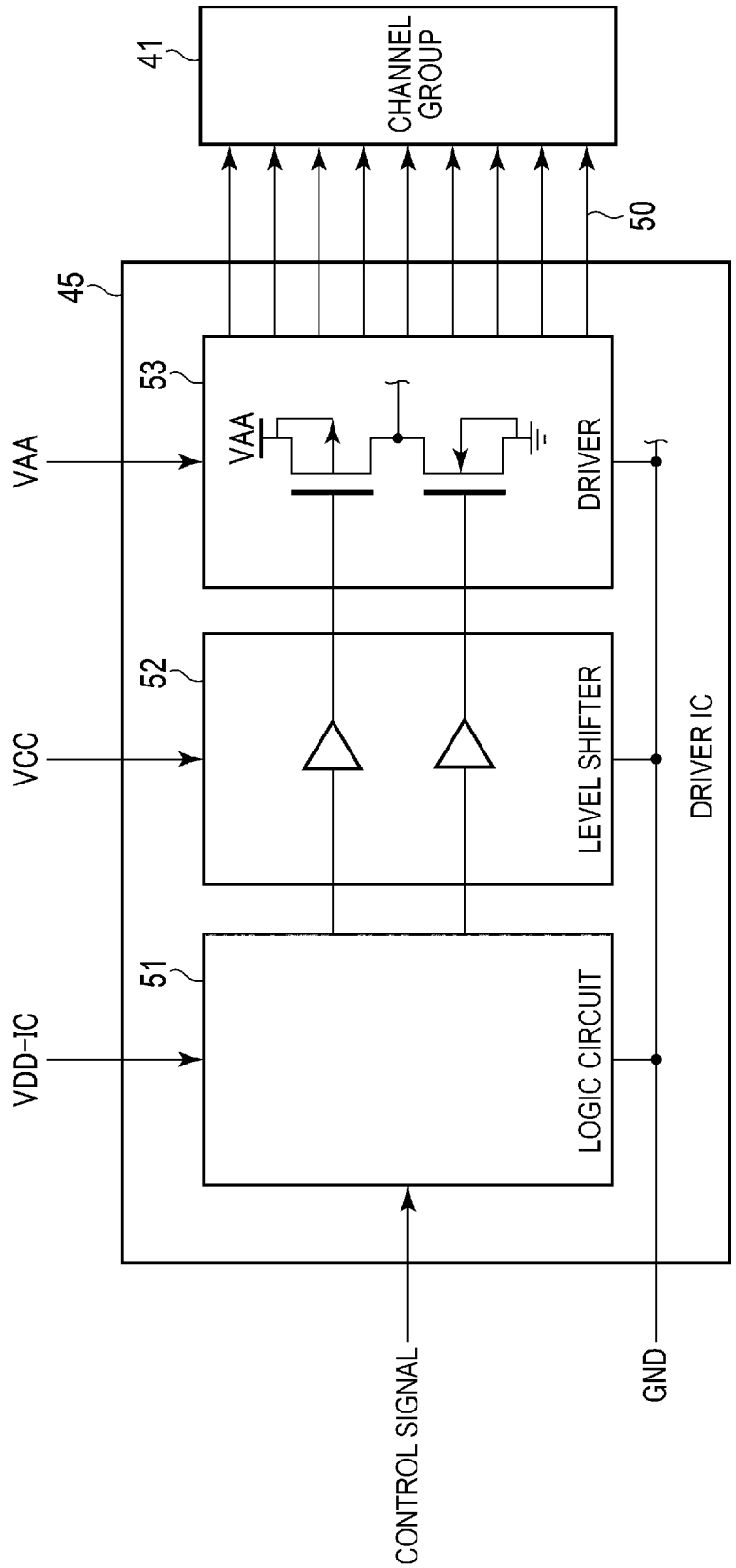

41
CHANNEL GROUP
50
45
53
VAA
VAA
DRIVER
52
VCC
LEVEL SHIFTER
51
VDD-IC
LOGIC CIRCUIT
DRIVER IC
CONTROL SIGNAL
GND

FIG. 5

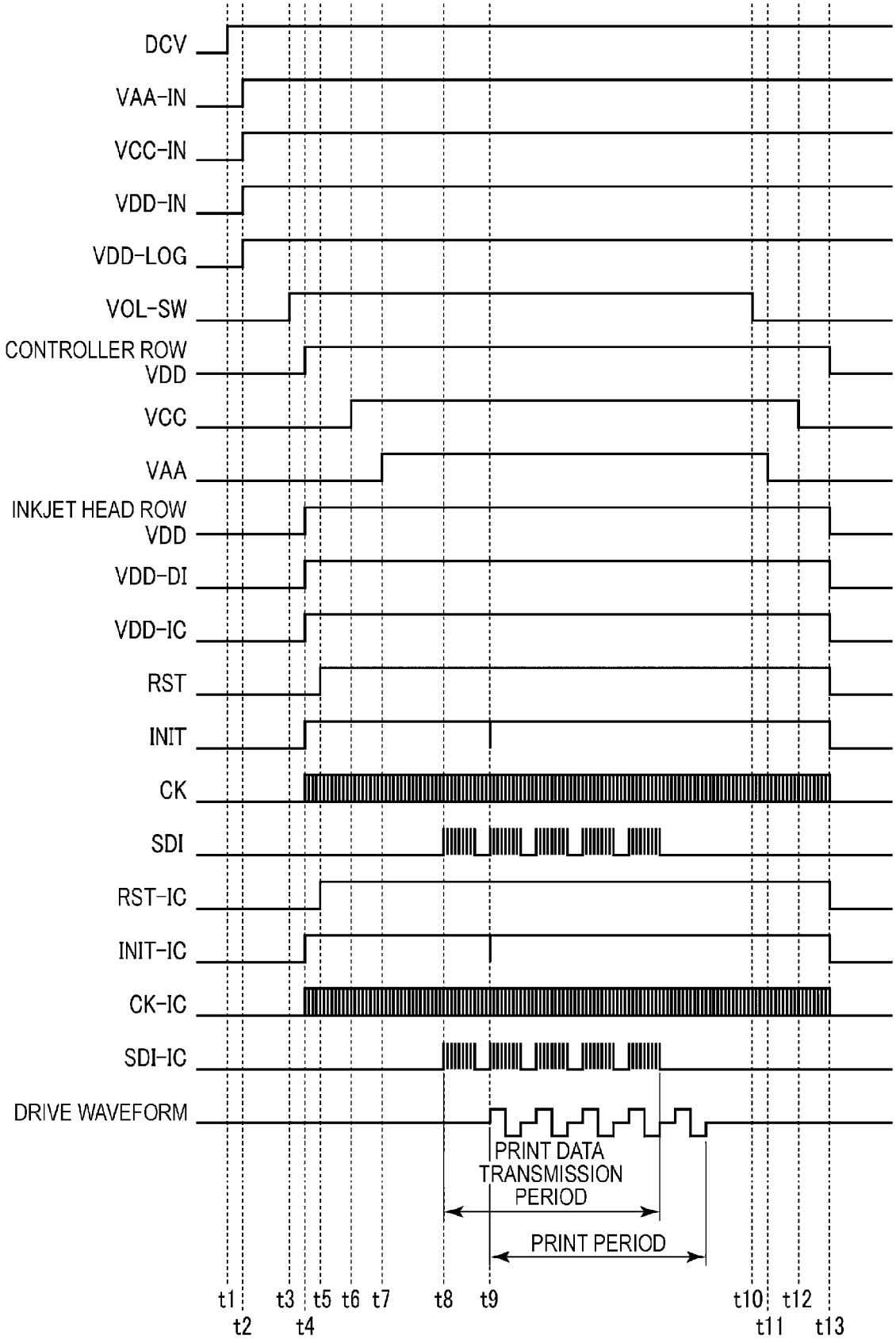

DCV
VAA-IN
VCC-IN
VDD-IN
VDD-LOG
VOL-SW
CONTROLLER ROW VDD
VCC
VAA
INKJET HEAD ROW VDD
VDD-DI
VDD-IC
RST
INIT
CK
SDI
RST-IC
INIT-IC
CK-IC
SDI-IC
DRIVE WAVEFORM
PRINT DATA TRANSMISSION PERIOD
PRINT PERIOD
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13

FIG. 6

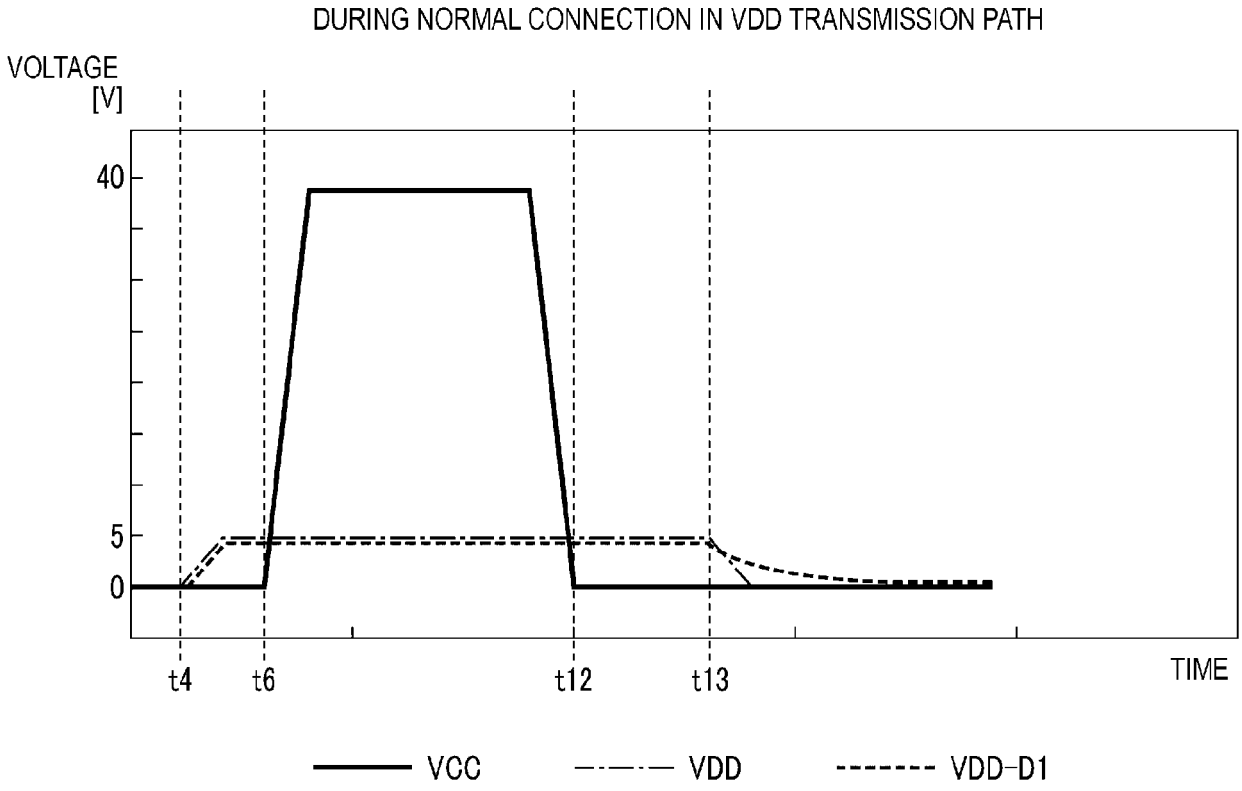

DURING NORMAL CONNECTION IN VDD TRANSMISSION PATH
VOLTAGE
[V]
40
5
0
t4
t6
t12
t13
TIME
VCC
VDD
VDD-D1

FIG. 7

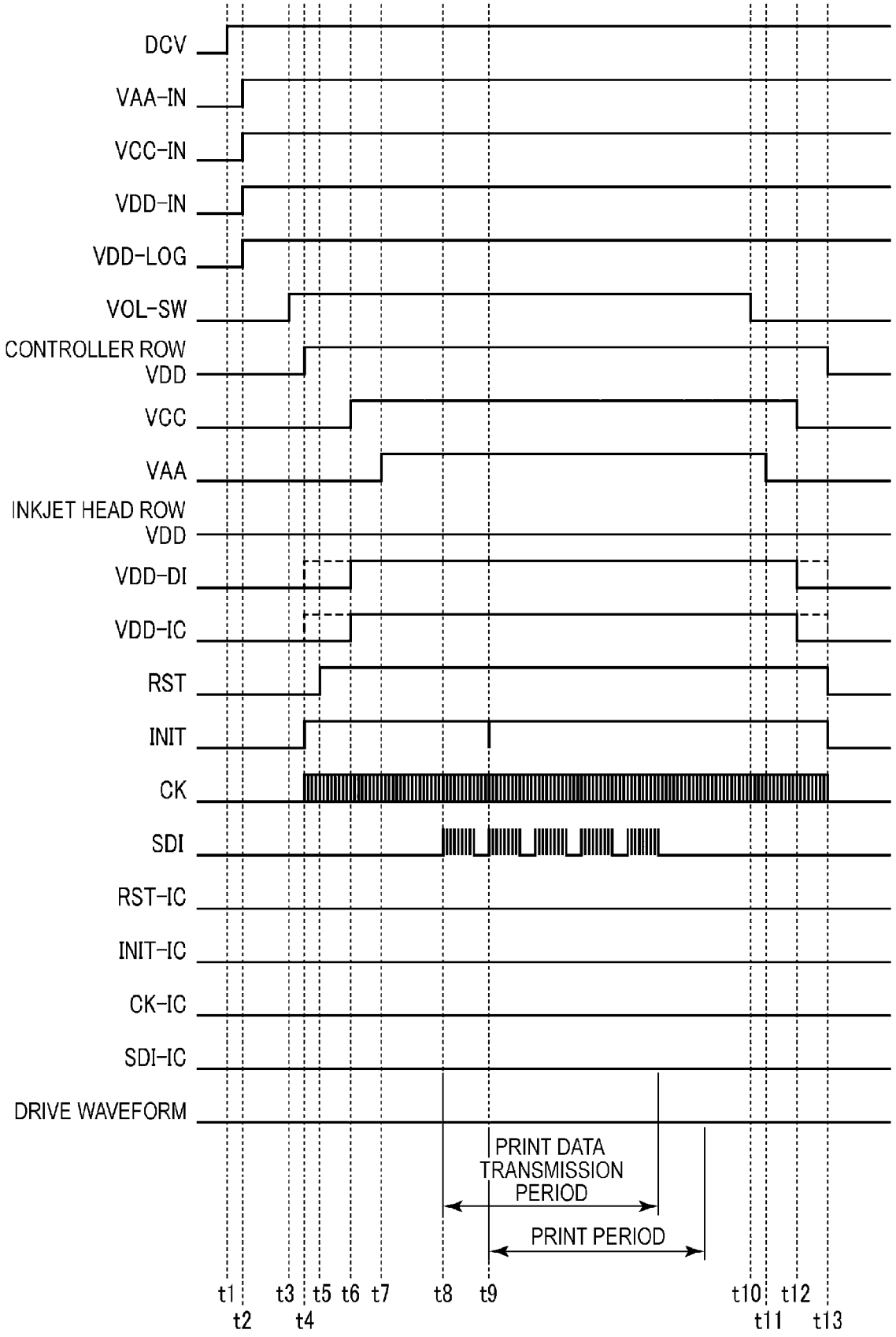
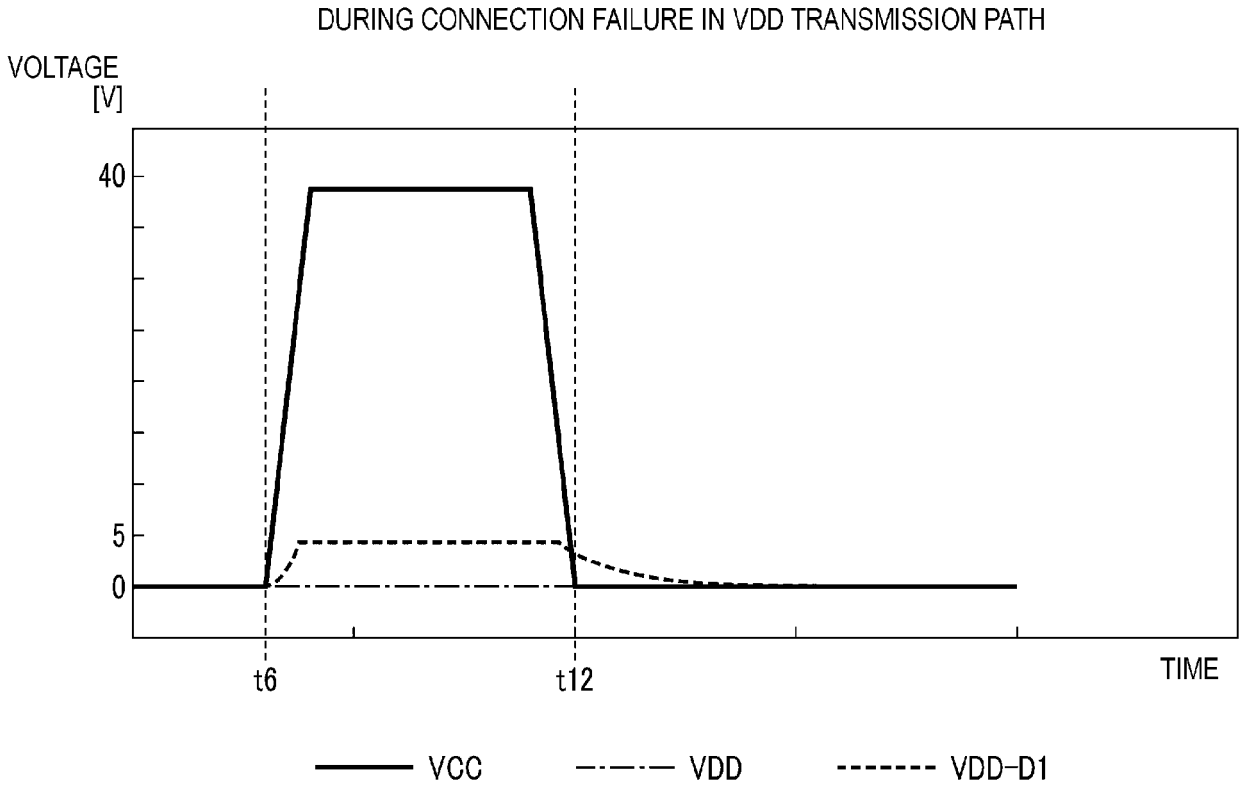

DCV
VAA-IN
VCC-IN
VDD-IN
VDD-LOG
VOL-SW
CONTROLLER ROW VDD
VCC
VAA
INKJET HEAD ROW VDD
VDD-DI
VDD-IC
RST
INIT
CK
SDI
RST-IC
INIT-IC
CK-IC
SDI-IC
DRIVE WAVEFORM
PRINT DATA TRANSMISSION PERIOD
PRINT PERIOD
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13

FIG. 8


DURING CONNECTION FAILURE IN VDD TRANSMISSION PATH
VOLTAGE
[V]
40
5
0
t6
t12
TIME
VCC
VDD
VDD-D1

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 23 20 5891

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A	JP 2019 038116 A (TOSHIBA TEC KK) 14 March 2019 (2019-03-14) * paragraphs [0055] - [0057], [0061] - [0064]; figures 2,3 *	1-9	INV. B41J2/045
A	US 2020/198326 A1 (HIYOSHI TERUYUKI [JP]) 25 June 2020 (2020-06-25) * paragraphs [0043] - [0051]; figure 2 *	1-9	

TECHNICAL FIELDS SEARCHED (IPC)

B41J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	22 March 2024	Öztürk, Serkan

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 23 20 5891

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

22-03-2024

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2019038116 A	14-03-2019	JP 6896559 B2	30-06-2021
		JP 2019038116 A	14-03-2019
US 2020198326 A1	25-06-2020	CN 111347791 A	30-06-2020
		EP 3670189 A1	24-06-2020
		JP 7118879 B2	16-08-2022
		JP 2020100030 A	02-07-2020
		US 2020198326 A1	25-06-2020

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82