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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

Filed July 19, 1954 38 Sheets-Sheet 1

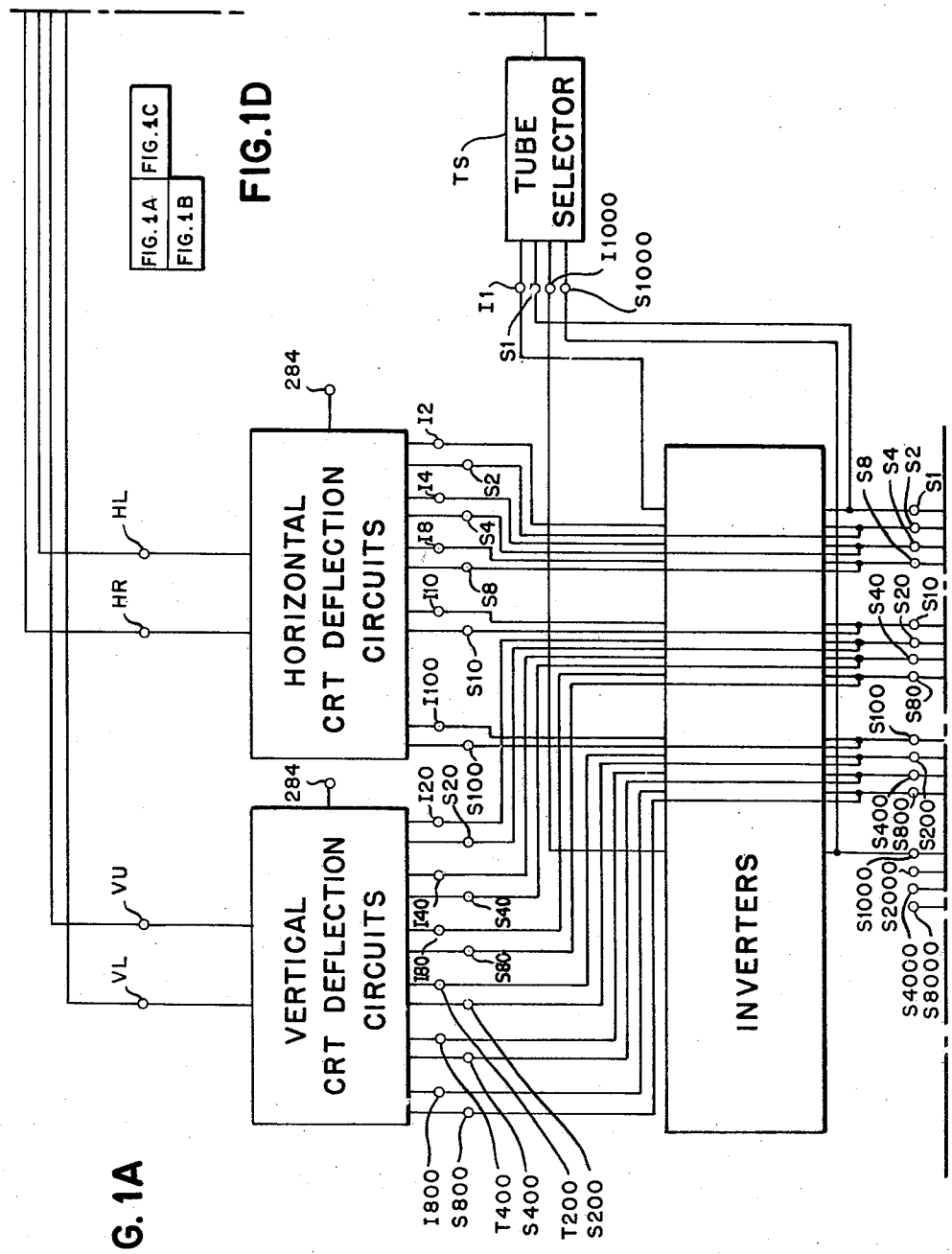

FIG. 1A

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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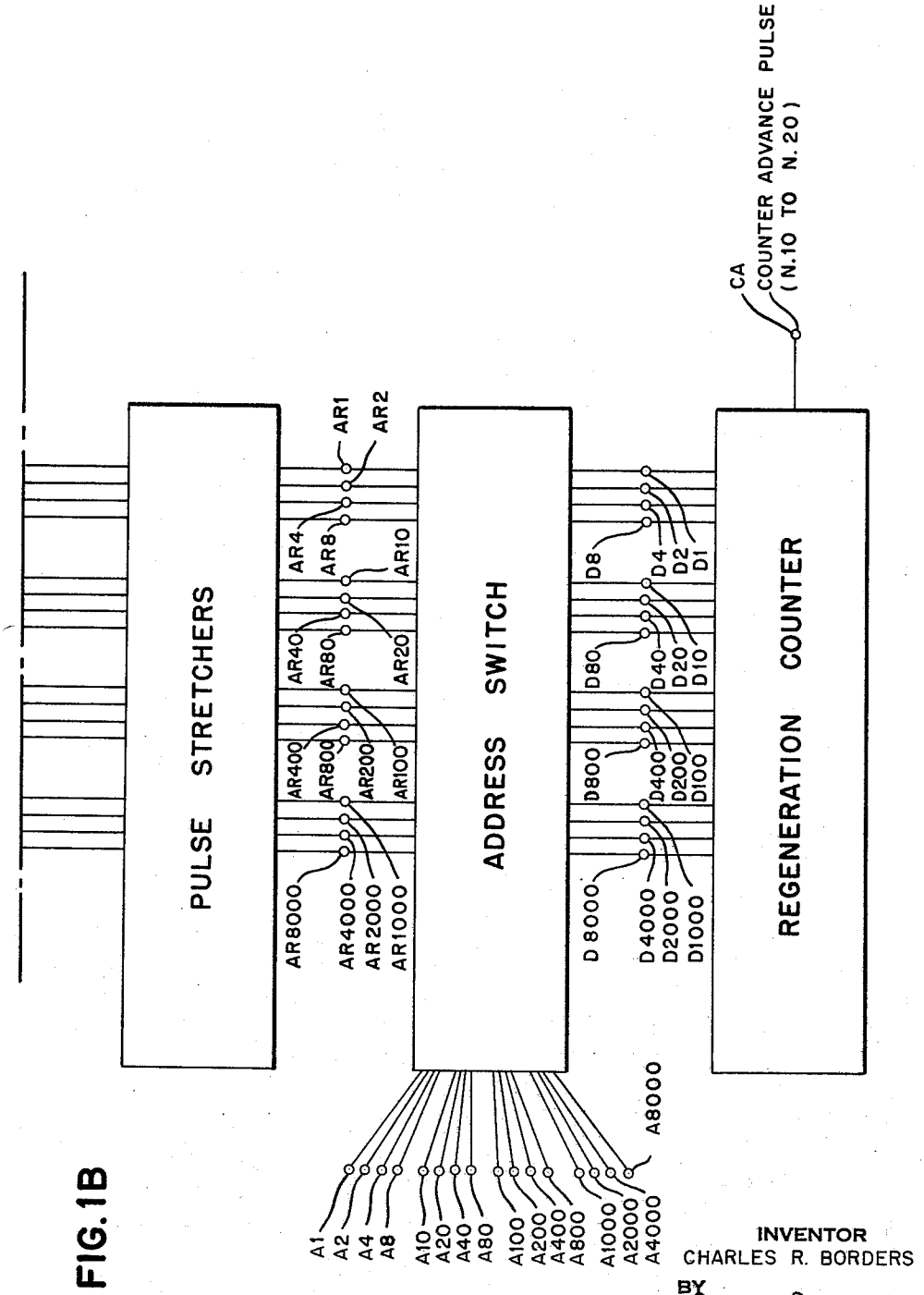

FIG. 1B

INVENTOR
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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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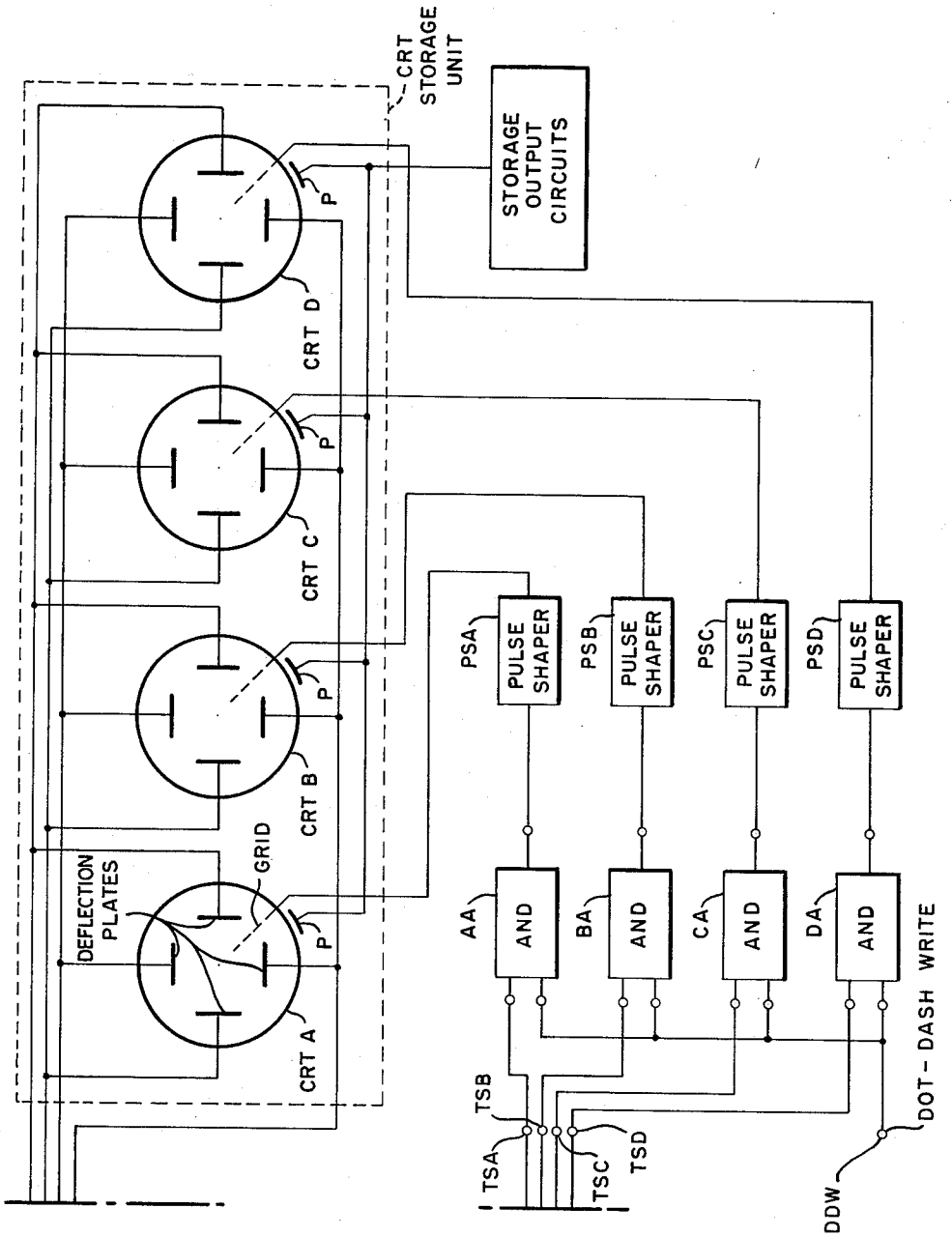

FIG. 1C

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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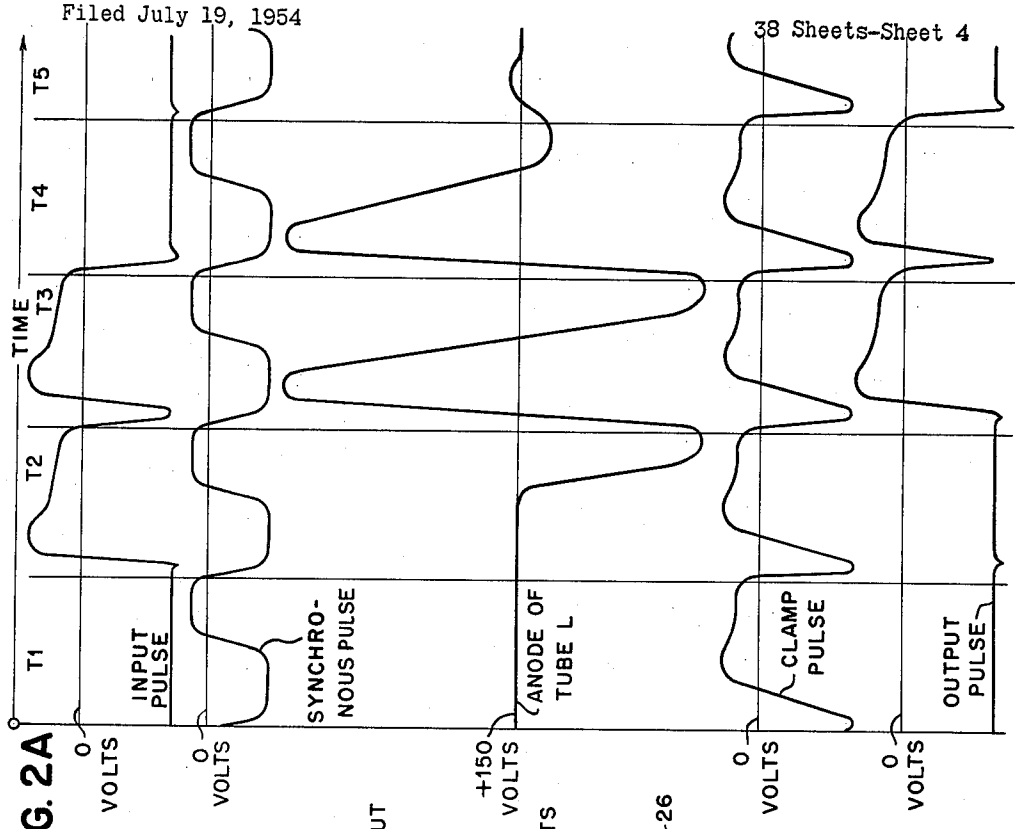

FIG. 2A

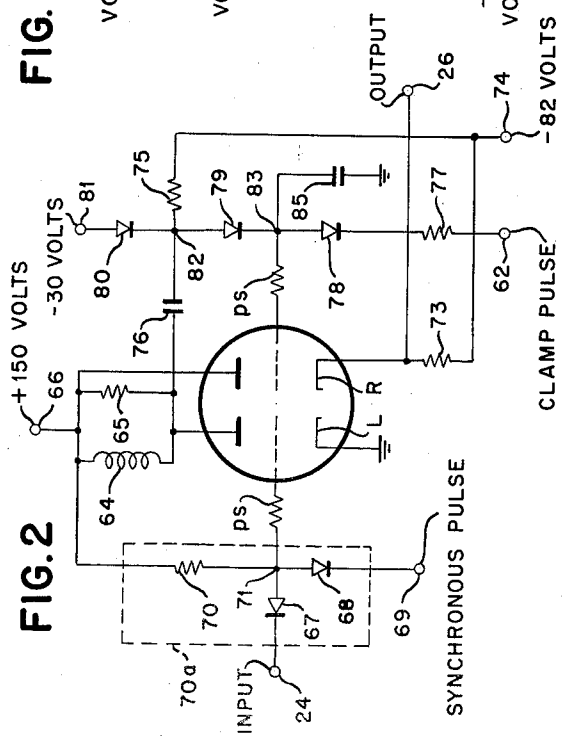

FIG. 2

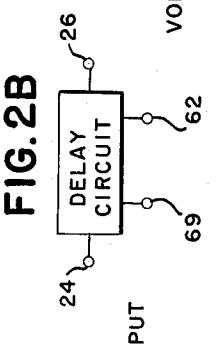

FIG. 2B

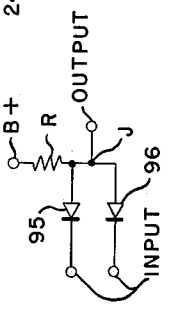

FIG. 3

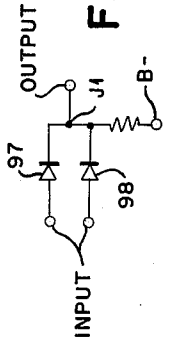

FIG. 4

INVENTOR.
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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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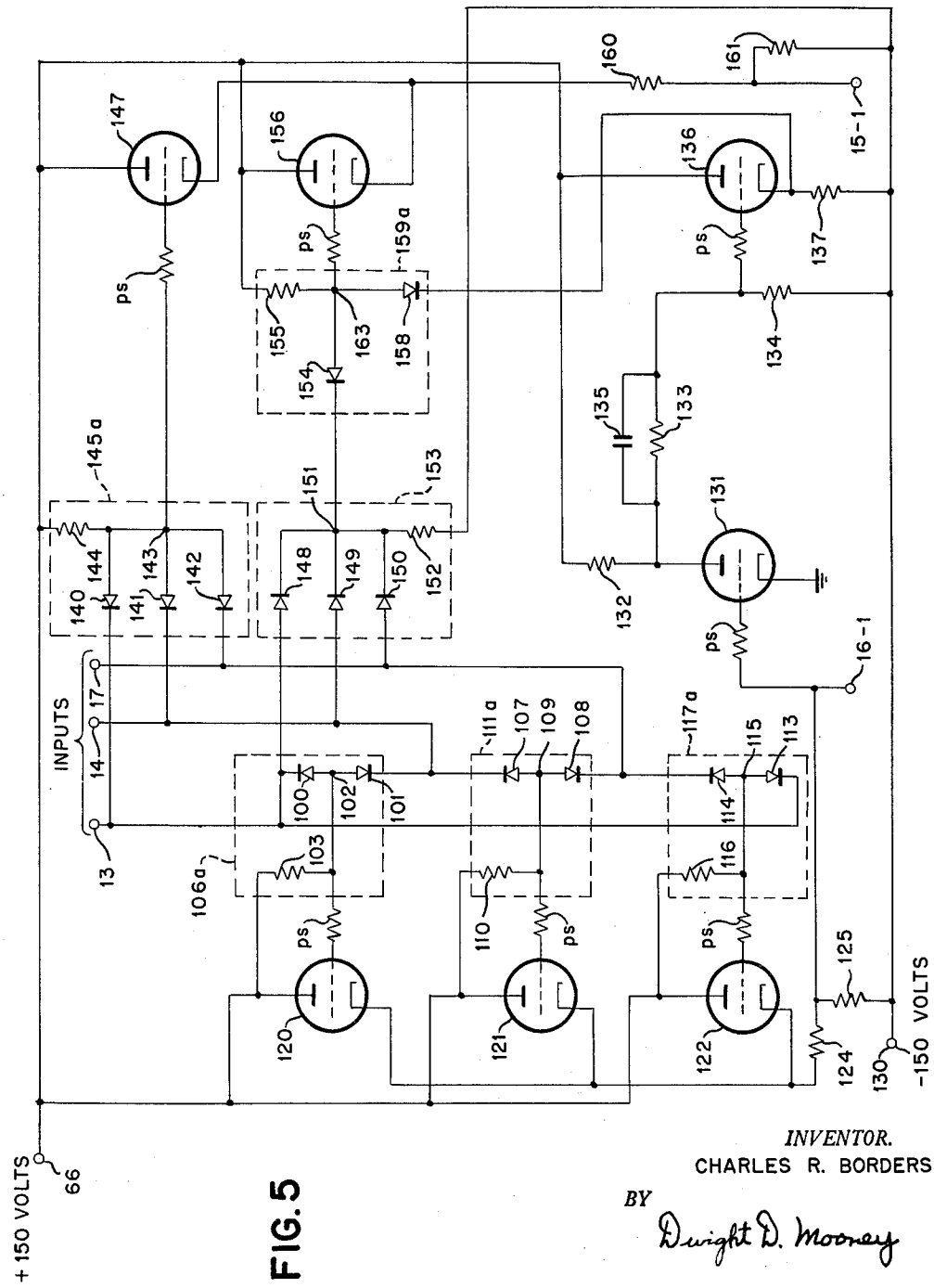

FIG. 5

INVENTOR.
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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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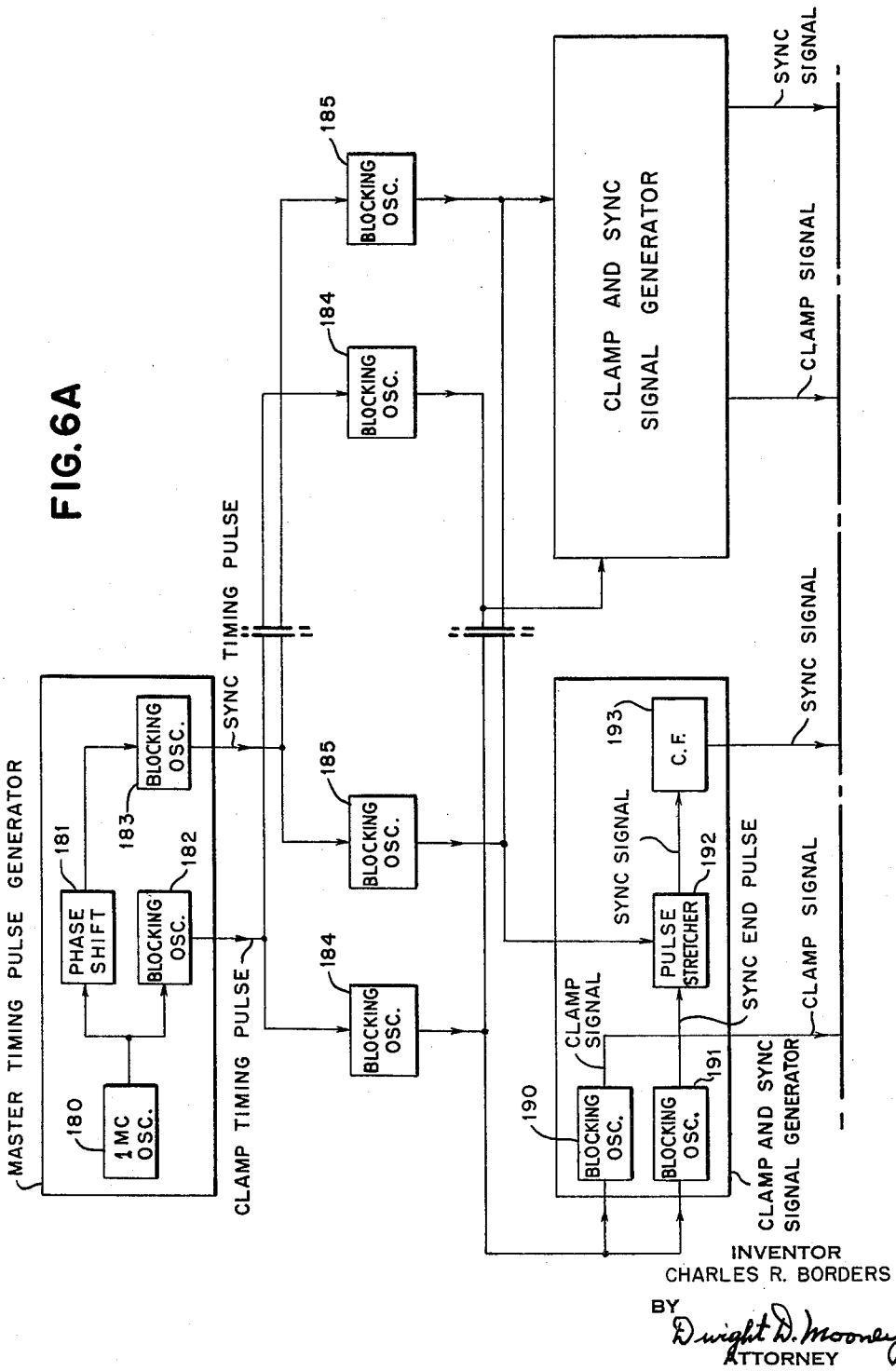
FIG. 6A



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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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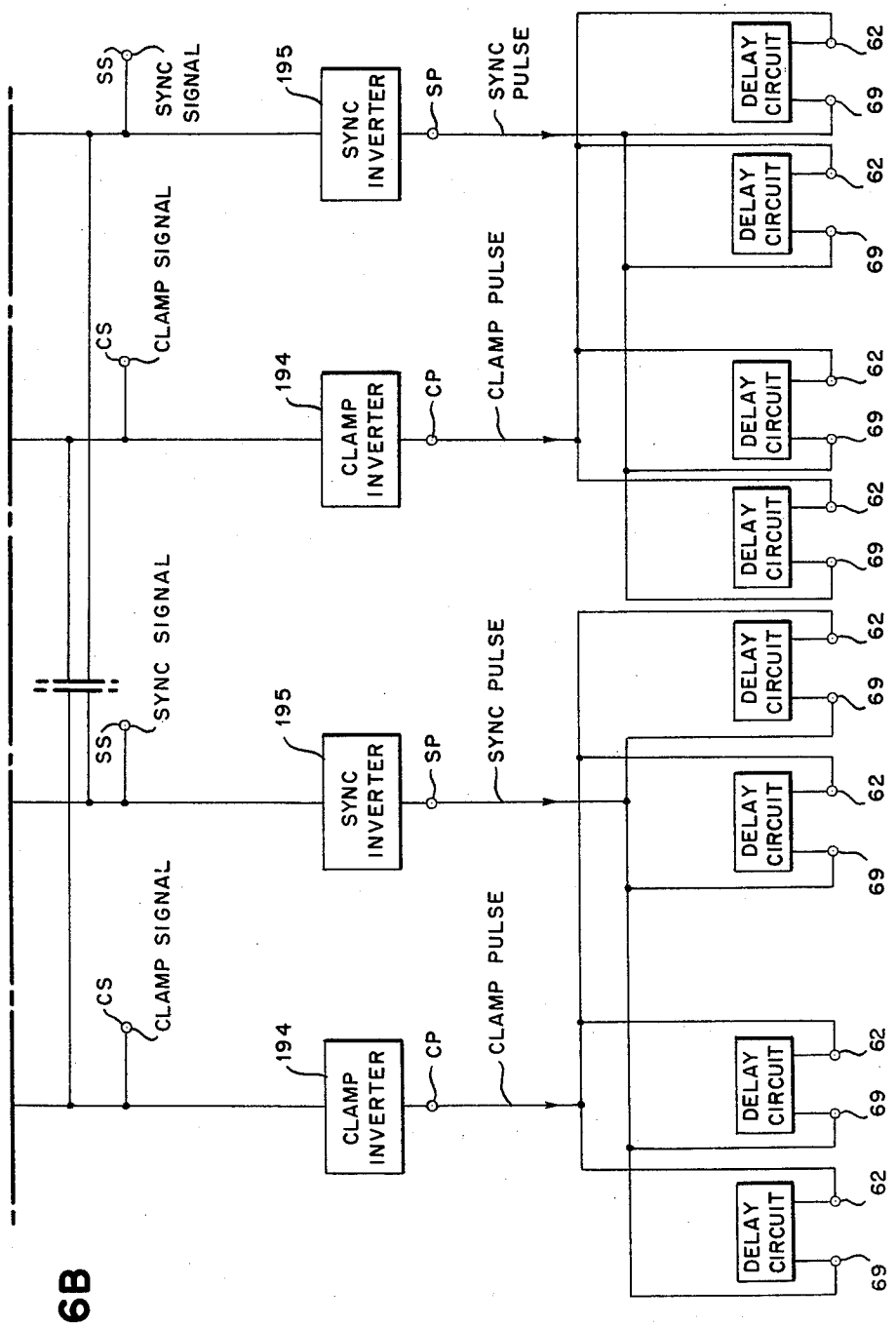

FIG.6B

INVENTOR
CHARLES R. BORDERS

BY Dwight D. Mooney
ATTORNEY

COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

Filed July 19, 1954 38 Sheets-Sheet 8

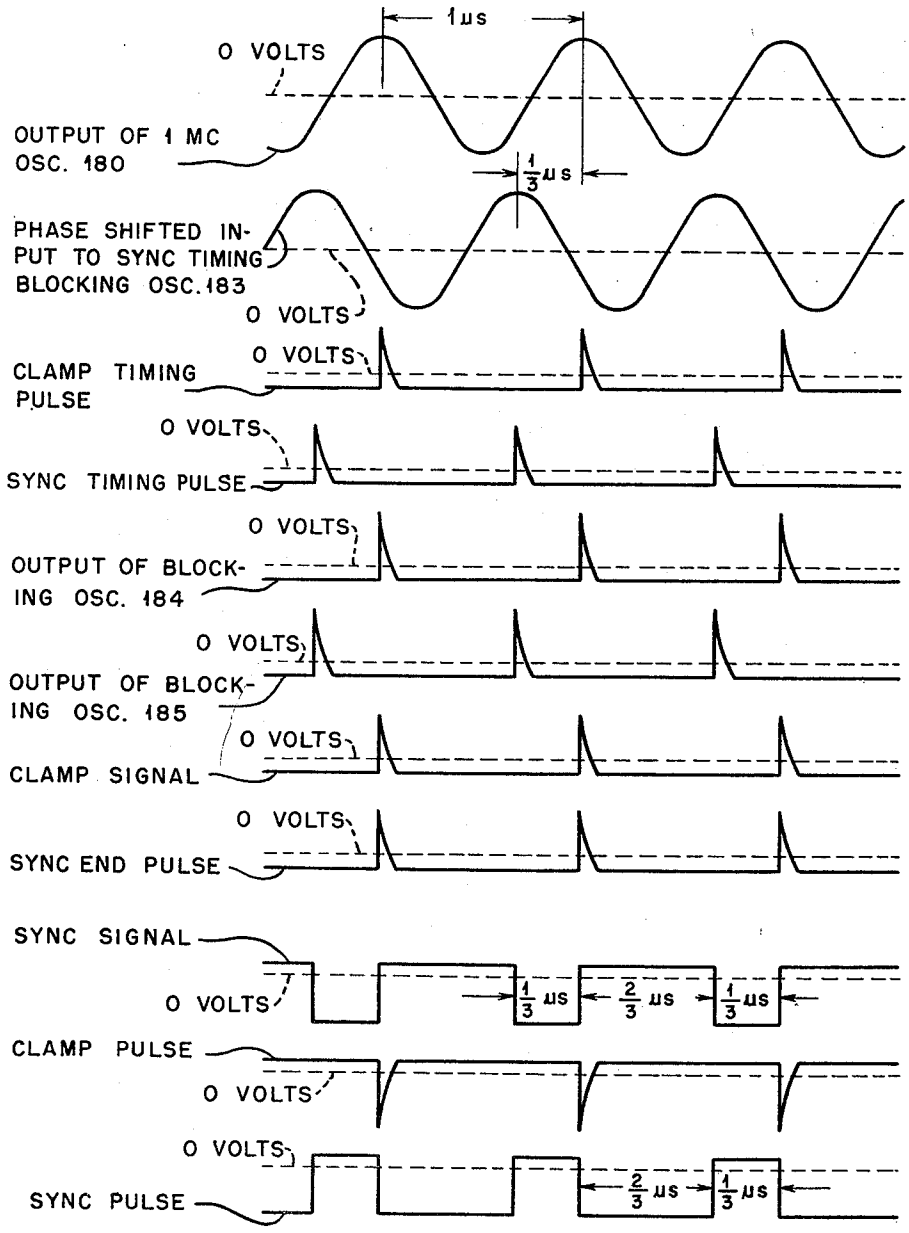

FIG. 6C

INVENTOR
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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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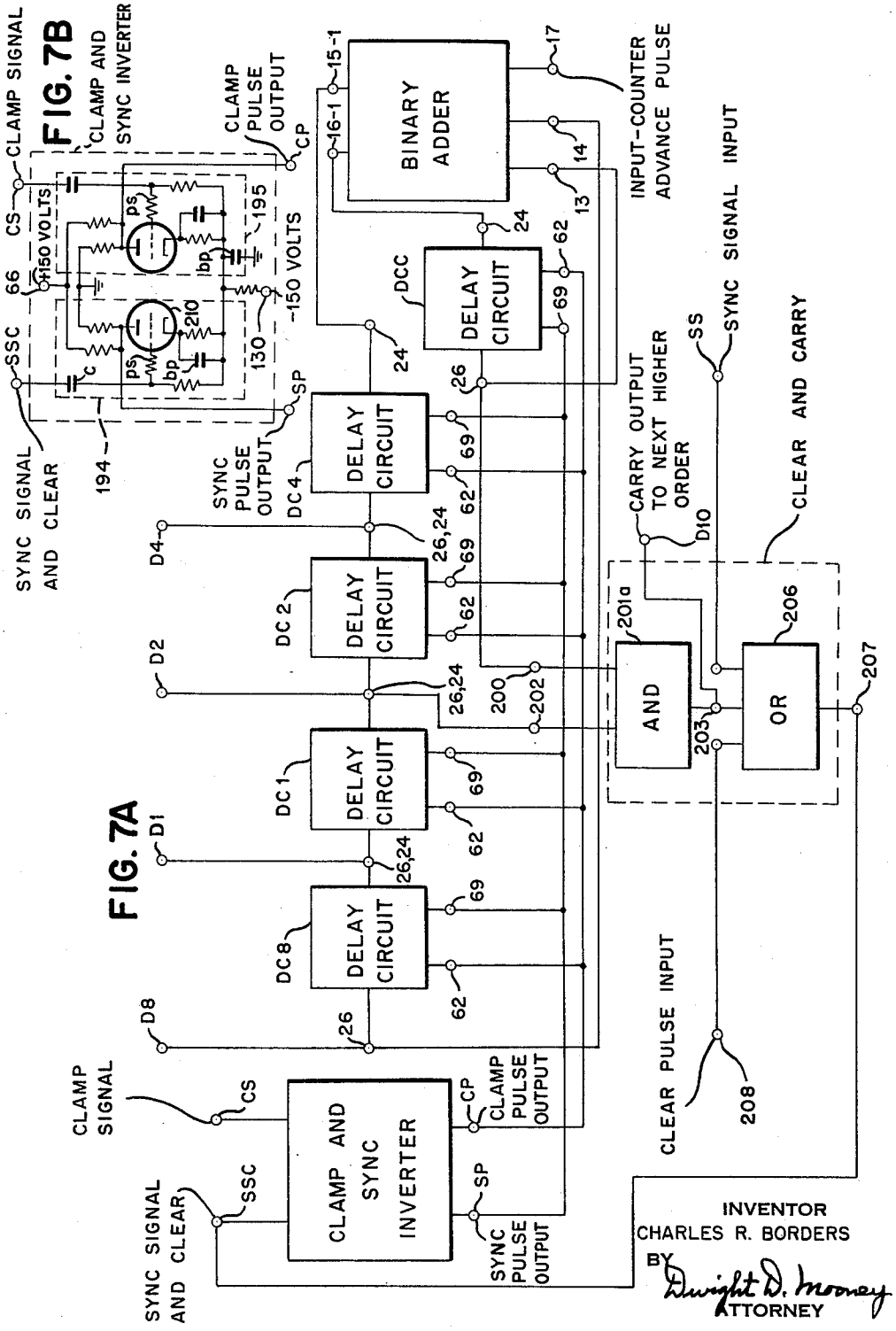

COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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		CIRCUIT POINTS (FIGS. 7A, 8A, 8B) UNITS ORDER									
TIME	OPERATION	17(INPUT)	14	13	16–1	15–1	D4	D2	D1	D8	D10
0.00		0	0	0	0	0	0	0	0	0	0
0.10		1	0	0	0	1	0	0	0	0	0
0.20		0	0	0	0	0	1	0	0	0	0
0.30		0	0	0	0	0	0	1	0	0	0
0.40		0	0	0	0	0	0	0	1	0	0
0.50		0	1	0	0	1	0	0	0	1	0
0.60		0	0	0	0	0	1	0	0	0	0
0.70		0	0	0	0	0	0	1	0	0	0
1.00	READOUT 1	0	0	0	0	0	0	0	1	0	0
1.10		1	1	0	1	0	0	0	0	1	0
1.20		0	0	1	0	1	0	0	0	0	0
1.30		0	0	0	0	0	1	0	0	0	0
1.40		0	0	0	0	0	0	1	0	0	0
1.50		0	0	0	0	0	0	0	1	0	0
1.60		0	1	0	0	1	0	0	0	1	0
1.70		0	0	0	0	0	1	0	0	0	0
2.00	READOUT 2	0	0	0	0	0	0	1	0	0	0
2.10		1	0	0	0	1	0	0	1	0	0
2.20		0	1	0	0	1	1	0	0	1	0
2.30		0	0	0	0	0	1	1	0	0	0
2.40		0	0	0	0	0	0	1	1	0	0
2.50		0	1	0	0	1	0	0	1	1	0
2.60		0	1	0	0	1	1	0	0	1	0
2.70		0	0	0	0	0	1	1	0	0	0
3.00	READOUT 3	0	0	0	0	0	0	1	1	0	0
3.10		1	1	0	1	0	0	0	1	1	0
3.20		0	1	1	1	0	0	0	0	1	0
3.30		0	0	1	0	1	0	0	0	0	0
3.40		0	0	0	0	0	1	0	0	0	0
3.50		0	0	0	0	0	0	1	0	0	0
3.60		0	0	0	0	0	0	0	1	0	0
3.70		0	1	0	0	1	0	0	0	1	0
4.00	READOUT 4	0	0	0	0	0	1	0	0	0	0
4.10		1	0	0	0	1	0	1	0	0	0
4.20		0	0	0	0	0	1	0	1	0	0
4.30		0	1	0	0	1	0	1	0	1	0
4.40		0	0	0	0	0	1	0	1	0	0
4.50		0	1	0	0	1	0	1	0	1	0
4.60		0	0	0	0	0	1	0	1	0	0
4.70		0	1	0	0	1	0	1	0	1	0

FIG. 7C

INVENTOR.
CHARLES R. BORDERS

BY Dwight D. Mooney
ATTORNEY

TIME	OPERATION	17(INPUT)	14	13	16-1	15-1	D 4	D 2	D 1	D 8	D 10
5.00	READOUT 5	0	0	0	0	0	1	0	1	0	0
5.10		1	1	0	1	0	0	1	0	1	0
5.20		0	0	1	0	1	0	0	1	0	0
5.30		0	1	0	0	1	1	0	0	1	0
5.40		0	0	0	0	0	1	1	0	0	0
5.50		0	0	0	0	0	0	1	1	0	0
5.60		0	1	0	0	1	0	0	1	1	0
5.70		0	1	0	0	1	1	0	0	1	0
6.00	READOUT 6	0	0	0	0	0	1	1	0	0	0
6.10		1	0	0	0	1	0	1	1	0	0
6.20		0	1	0	0	1	1	0	1	1	0
6.30		0	1	0	0	1	1	1	0	1	0
6.40		0	0	0	0	0	1	1	1	0	0
6.50		0	1	0	0	1	0	1	1	1	0
6.60		0	1	0	0	1	1	0	1	1	0
6.70		0	1	0	0	1	1	1	0	1	0
7.00	READOUT 7	0	0	0	0	0	1	1	1	0	0
7.10		1	1	0	1	0	0	1	1	1	0
7.20		0	1	1	1	0	0	0	1	1	0
7.30		0	1	1	1	0	0	0	0	1	0
7.40		0	0	1	0	1	0	0	0	0	0
7.50		0	0	0	0	0	1	0	0	0	0
7.60		0	0	0	0	0	0	1	0	0	0
7.70		0	0	0	0	0	0	0	1	0	0
8.00	READOUT 8	0	1	0	0	1	0	0	0	1	0
8.10		1	0	0	0	1	1	0	0	0	0
8.20		0	0	0	0	0	1	1	0	0	0
8.30		0	0	0	0	0	0	1	1	0	0
8.40		0	1	0	0	1	0	0	1	1	0
8.50		0	1	0	0	1	1	0	0	1	0
8.60		0	0	0	0	0	1	1	0	0	0
8.70		0	0	0	0	0	0	1	1	0	0
9.00	READOUT 9	0	1	0	0	1	0	0	1	1	0
9.10		1	1	0	1	0	1	0	0	1	0
9.20	CARRY AND CLEAR	0	0	1	0	1	0	1	0	0	1
9.30		0	0	0	0	0	0	0	0	0	0
9.40		0	0	0	0	0	0	0	0	0	0
9.50		0	0	0	0	0	0	0	0	0	0
9.60		0	0	0	0	0	0	0	0	0	0
9.70		0	0	0	0	0	0	0	0	0	0
0.00		0	0	0	0	0	0	0	0	0	0

FIG. 7D

FIG. 7E

FIG. 7C
FIG. 7D

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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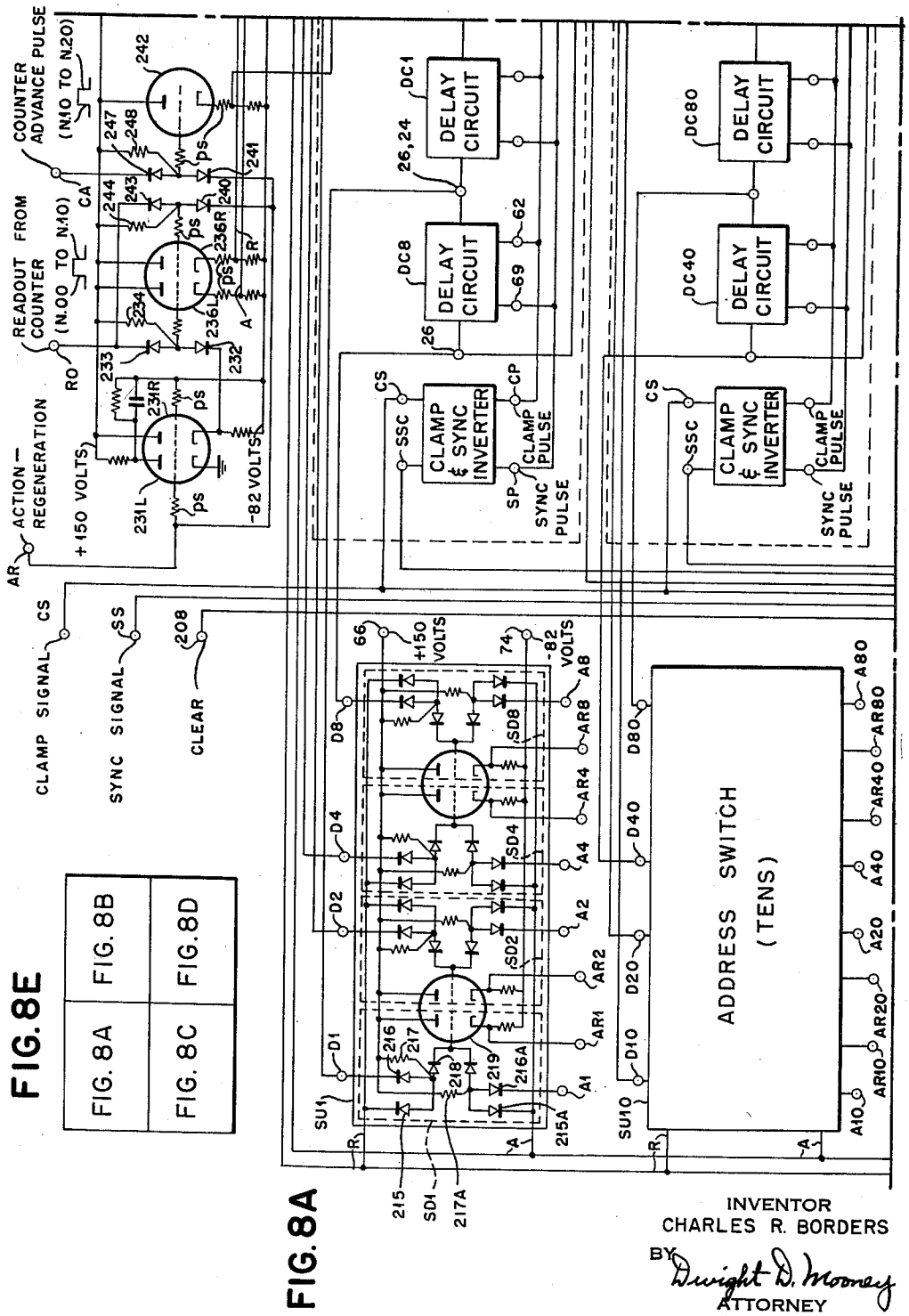

FIG. 8E

FIG. 8A	FIG. 8B
FIG. 8C	FIG. 8D

FIG. 8A

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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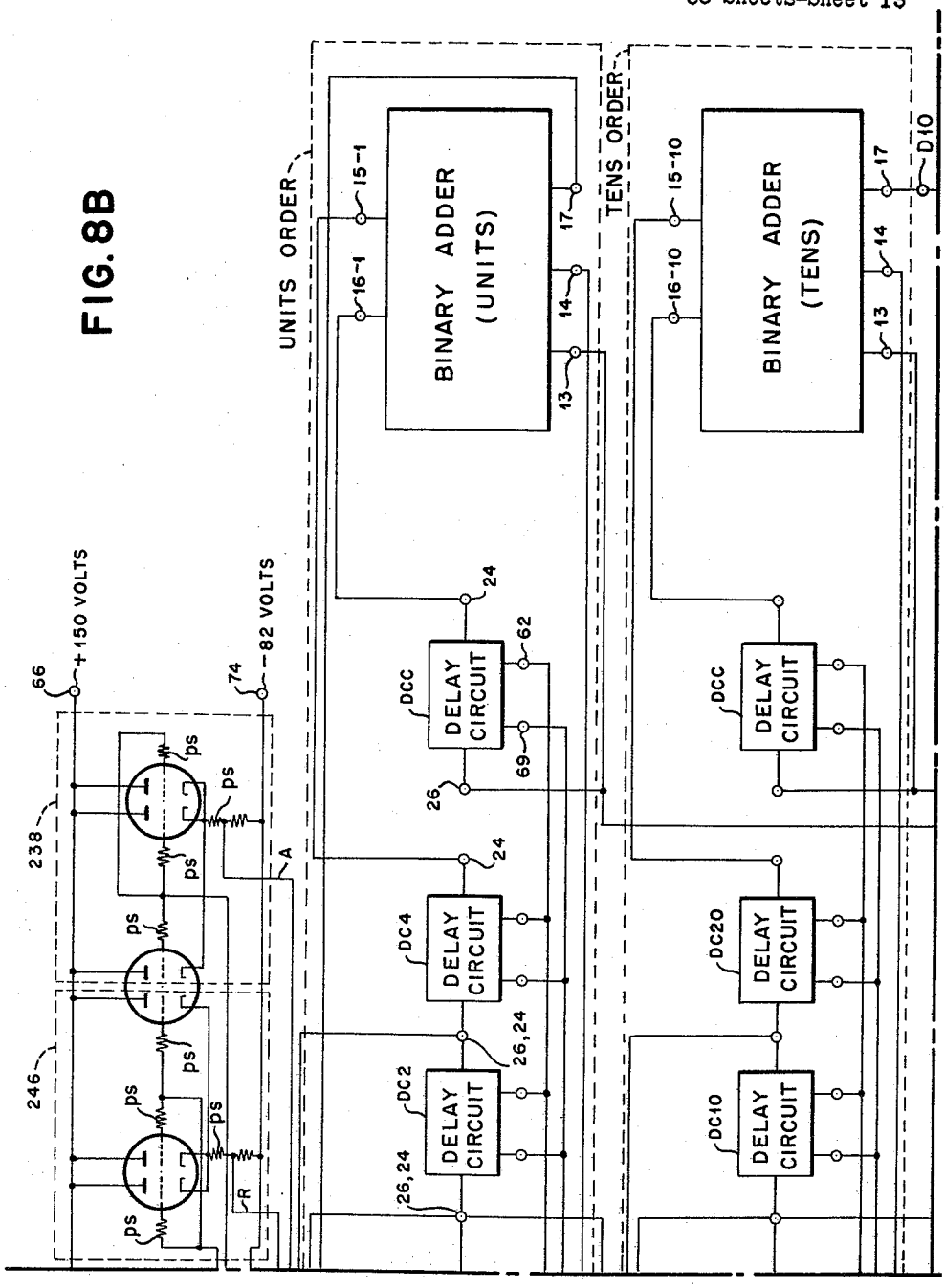
FIG. 8B



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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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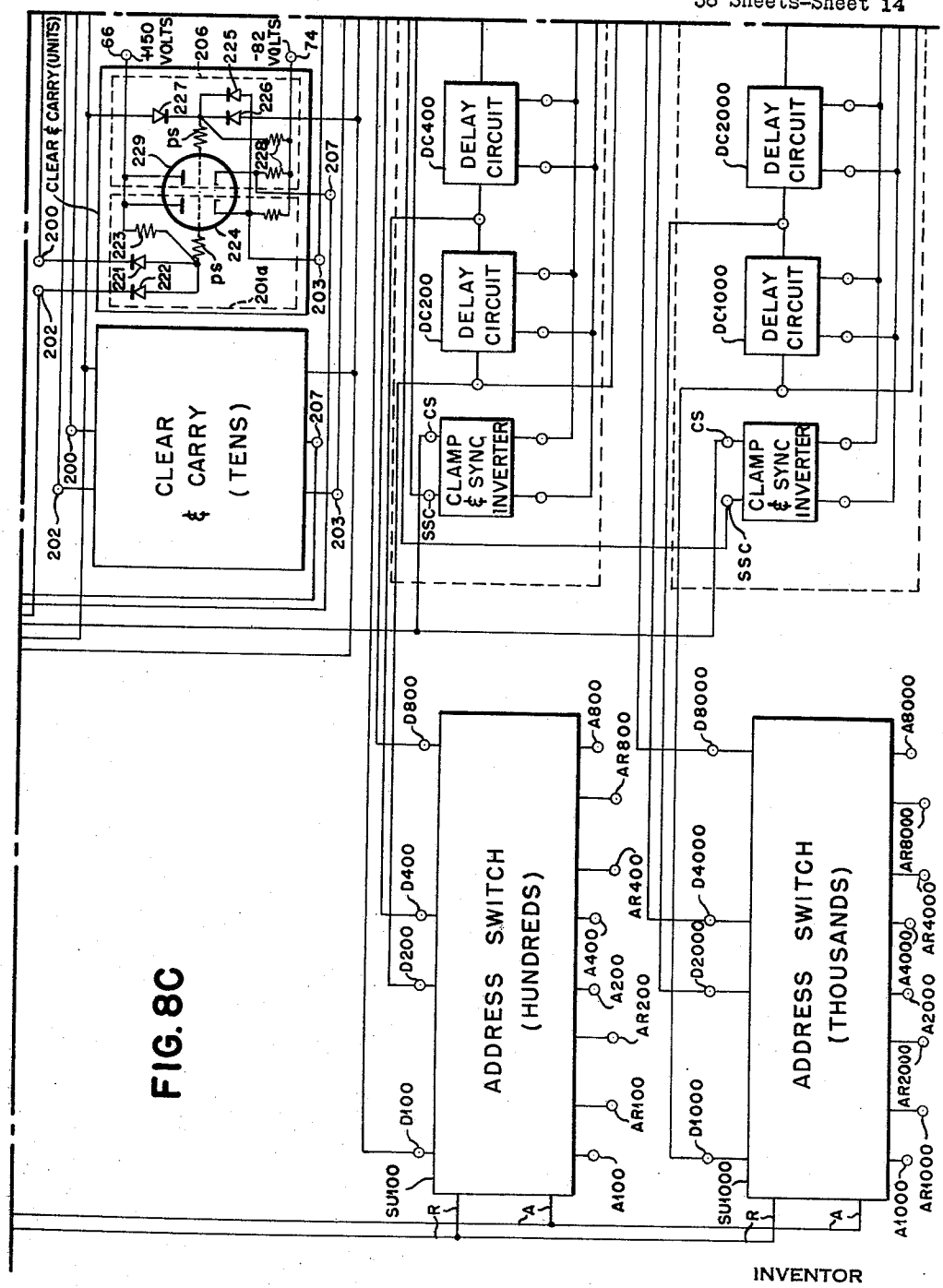

FIG. 8C

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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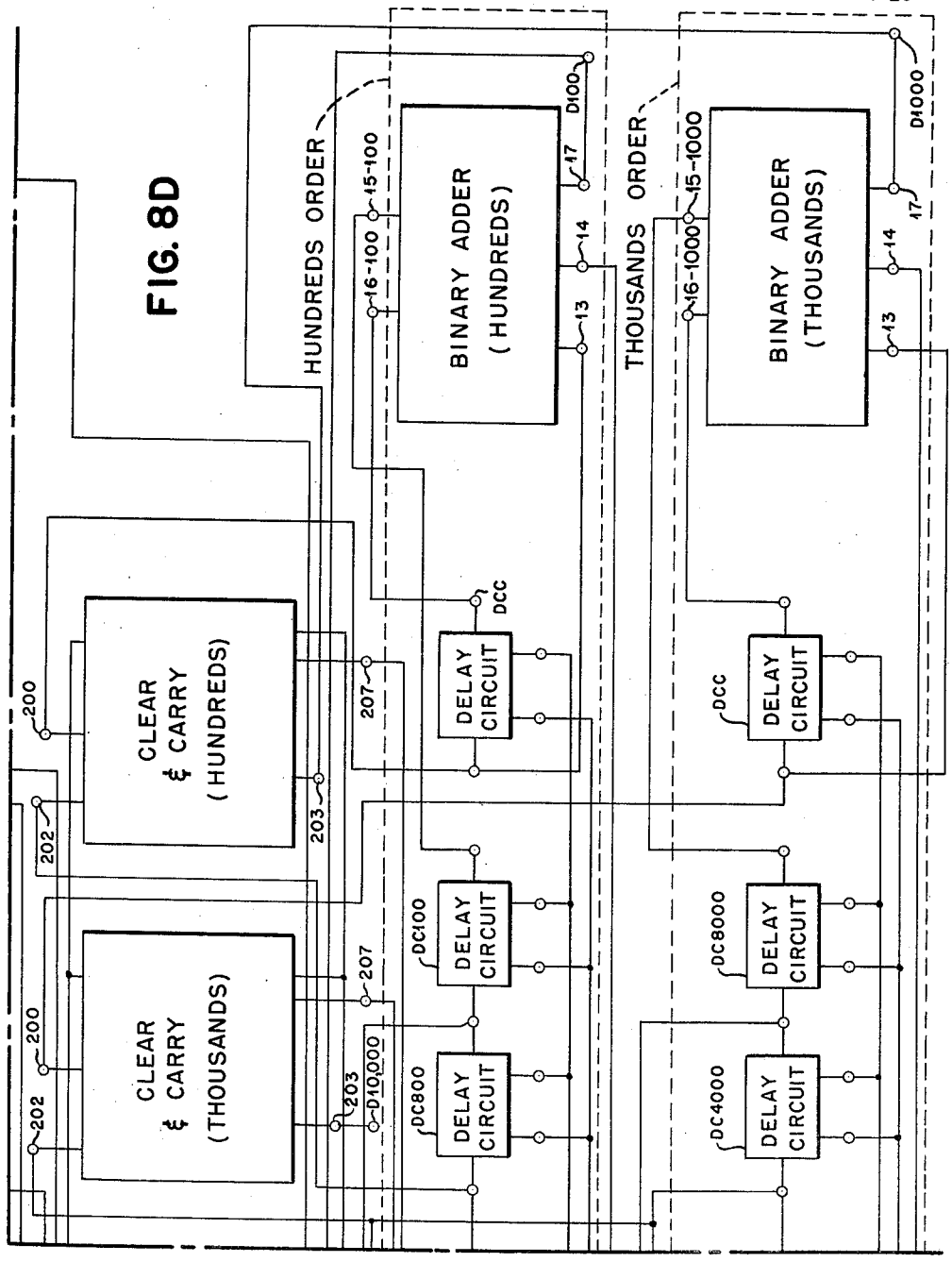
FIG. 8D



INVENTOR
CHARLES R. BORDERS

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TIME	OPERATION	CIRCUIT POINTS (FIGS. 7A, 8A, 8B) TENS ORDER									
		17(INPUT)	14	13	16-10	15-10	D20	D10	D80	D40	D100
9.20		1	0	0	0	1	0	0	0	0	0
9.30		0	0	0	0	0	1	0	0	0	0
9.40		0	0	0	0	0	0	1	0	0	0
9.50		0	0	0	0	0	0	0	1	0	0
9.60		0	1	0	0	1	0	0	0	1	0
9.70		0	0	0	0	0	1	0	0	0	0
10.00	READOUT 10	0	0	0	0	0	0	1	0	0	0
10.10		0	0	0	0	0	0	0	1	0	0
10.20		0	1	0	0	1	0	0	0	1	0
10.30		0	0	0	0	0	1	0	0	0	0
10.40		0	0	0	0	0	0	1	0	0	0
10.50		0	0	0	0	0	0	0	1	0	0
10.60		0	1	0	0	1	0	0	0	1	0
10.70		0	0	0	0	0	1	0	0	0	0
11.00	READOUT 11 (10 IN TENS, 1 IN UNITS)	0	0	0	0	0	0	1	0	0	0
98.00	READOUT 98 (90 IN TENS, 8 IN UNITS)	0	0	0	0	0	0	1	1	0	0
98.10		0	1	0	0	1	0	0	1	1	0
98.20		0	1	0	0	1	1	0	0	1	0
98.30		0	0	0	0	0	1	1	0	0	0
98.40		0	0	0	0	0	0	1	1	0	0
98.50		0	1	0	0	1	0	0	1	1	0
98.60		0	1	0	0	1	1	0	0	1	0
98.70		0	0	0	0	0	1	1	0	0	0
99.00	READOUT 99 (90 IN TENS, 9 IN UNITS)	0	0	0	0	0	0	1	1	0	0
99.10		0	1	0	0	1	0	0	1	1	0
99.20		1	1	0	1	0	1	0	0	1	0
99.30	CARRY AND CLEAR	0	0	1	0	1	0	1	0	0	1

FIG. 9A

INVENTOR.
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TIME	OPERATION	CIRCUIT POINTS (FIGS. 8C, 8D) HUNDREDS ORDER									
		17(INPUT)	14	13	16-100	15-100	D100	D800	D400	D200	D1000
99.30		1	0	0	0	1	0	0	0	0	0
99.40		0	0	0	0	0	1	0	0	0	0
99.50		0	0	0	0	0	0	1	0	0	0
99.60		0	0	0	0	0	0	0	1	0	0
99.70		0	1	0	0	1	0	0	0	1	0
100.00	READOUT 100 (100 IN HUNDREDS ORDER)	0	0	0	0	0	1	0	0	0	0
998.00	READOUT 998	0	0	0	0	0	1	1	0	0	0
998.10	900 IN HUNDREDS	0	0	0	0	0	0	1	1	0	0
998.20	90 IN TENS 8 IN UNITS	0	1	0	0	1	0	0	1	1	0
998.30		0	1	0	0	1	1	0	0	1	0
998.40		0	0	0	0	0	1	1	0	0	0
998.50		0	0	0	0	0	0	1	1	0	0
998.60		0	1	0	0	1	0	0	1	1	0
998.70		0	1	0	0	1	1	0	0	1	0
999.00	READOUT 999	0	0	0	0	0	1	1	0	0	0
999.10	900 IN HUNDREDS	0	0	0	0	0	0	1	1	0	0
999.20	90 IN TENS 9 IN UNITS	0	1	0	0	1	0	0	1	1	0
999.30		1	1	0	1	0	1	0	0	1	0
999.40	CARRY AND CLEAR	0	0	1	0	1	0	1	0	0	1

FIG. 9B

INVENTOR.
CHARLES R. BORDERS

BY Dwight D. Mooney
ATTORNEY

TIME	OPERATION	CIRCUIT POINTS (FIGS. 8C, 8D) THOUSANDS ORDER									
		17(INPUT)	14	13	16-1000	15-1000	D8000	D4000	D2000	D1000	D10,000
999.40		1	0	0	0	1	0	0	0	0	0
999.50		0	0	0	0	0	1	0	0	0	0
999.60		0	0	0	0	0	0	1	0	0	0
999.70		0	0	0	0	0	0	0	1	0	0
1000.00	READOUT 1000 (1000 IN THOUSANDS)	0	1	0	0	1	0	0	0	1	0
9998.00	READOUT 9998	0	1	0	0	1	1	0	0	1	0
9998.10	9000 IN THOUSANDS.	0	0	0	0	0	1	1	0	0	0
9998.20	900 IN HUNDREDS.	0	0	0	0	0	0	1	1	0	0
9998.30	90 IN TENS.	0	1	0	0	1	0	0	1	1	0
9998.40	8 IN UNITS.	0	1	0	0	1	1	0	0	1	0
9998.50		0	0	0	0	0	1	1	0	0	0
9998.60		0	0	0	0	0		1	1	0	0
9999.70		0	1	0	0	1		0	1	1	0
9999.00	READOUT 9999	0	1	0	0	1	1	0	0	1	0
9999.10	9000 IN THOUSANDS.	0	0	0	0	0	1	1	0	0	0
9999.20	900 IN HUNDREDS.	0	0	0	0	0		1	1	0	0
9999.30	90 IN TENS.	0	1	0	0	1		0	1	1	0
9999.40	9 IN UNITS.	1	1	0	1	0	1	0	0	1	0
9999.50	CARRY AND CLEAR	0	0	1	0	1		1	0	0	1
9999.60		0	0	0	0	0		0	0	0	0
9999.70		0	0	0	0	0		0	0	0	0
0000.00		0	0	0	0	0		0	0	0	0

FIG. 9C

FIG. 10

FIG. 7C
FIG. 7D
FIG. 9A
FIG. 9B
FIG. 9C

INVENTOR.
CHARLES R. BORDERS

BY Dwight D. Mooney
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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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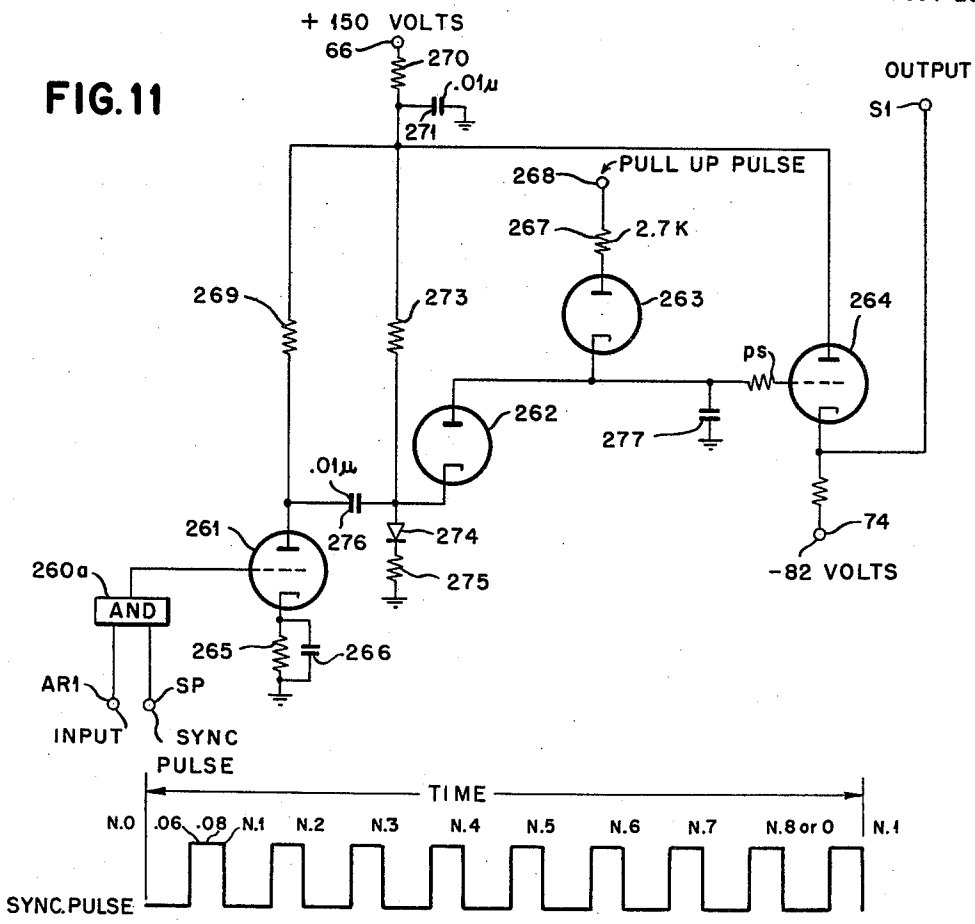
FIG. 11



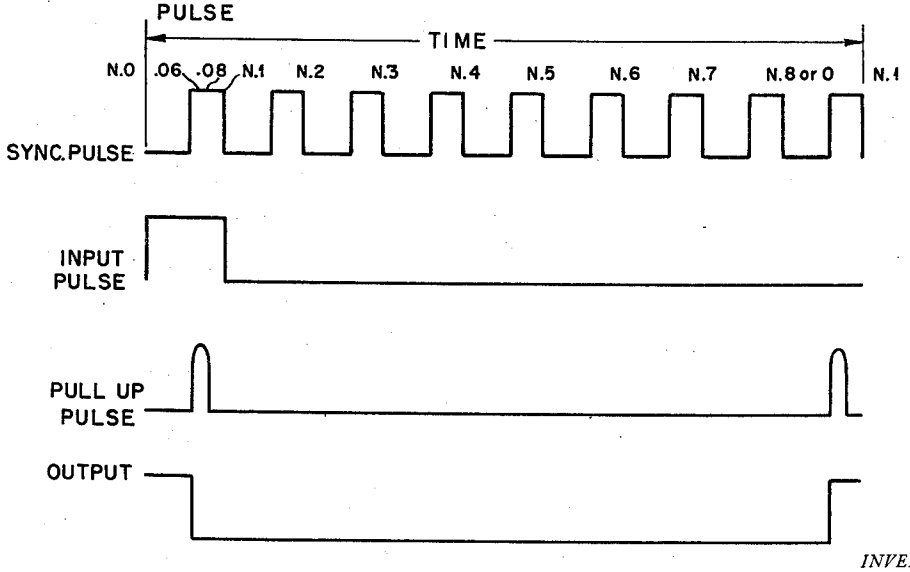


FIG. 11A

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Dec. 26, 1961 C. R. BORDERS 3,014,662

COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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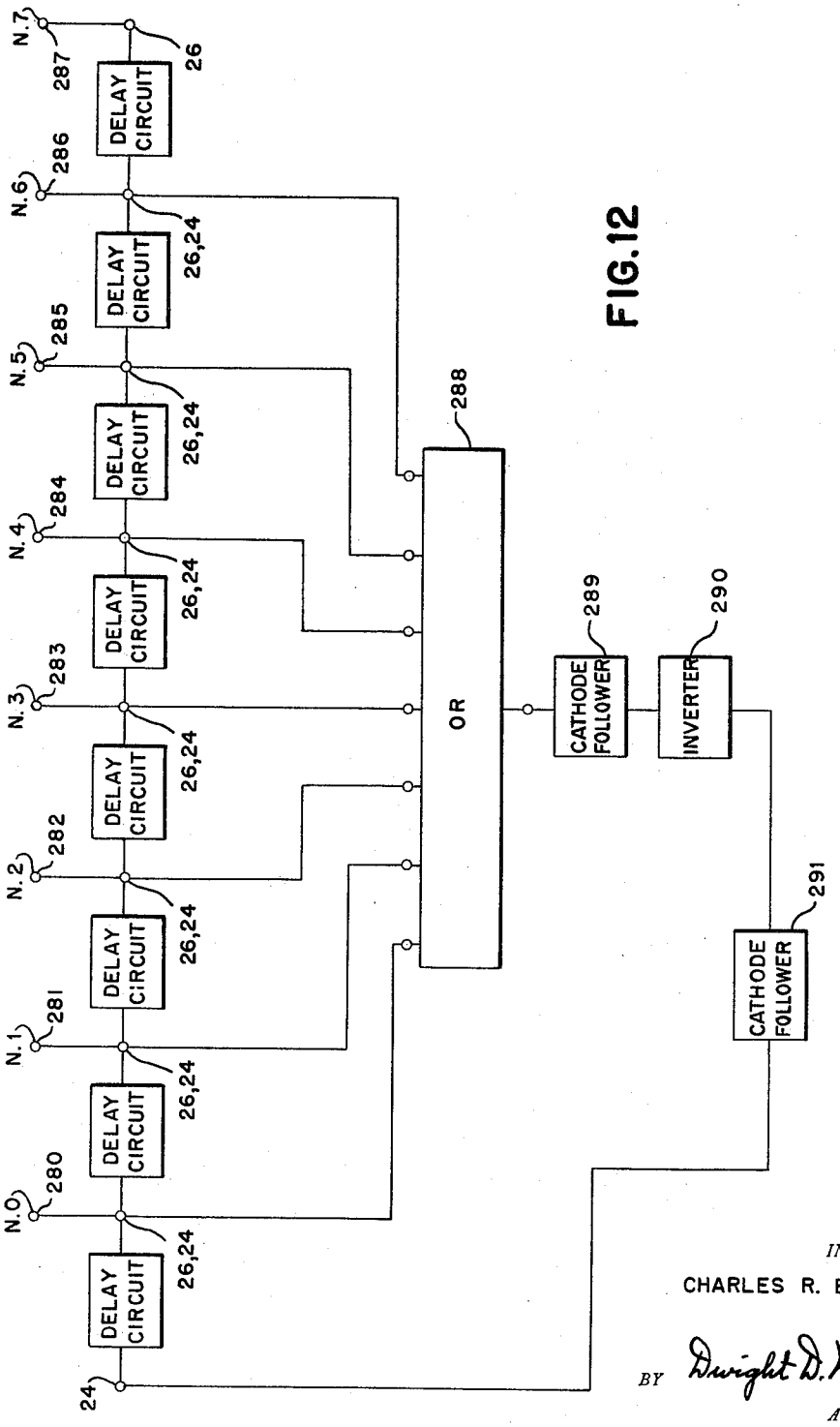

FIG.12

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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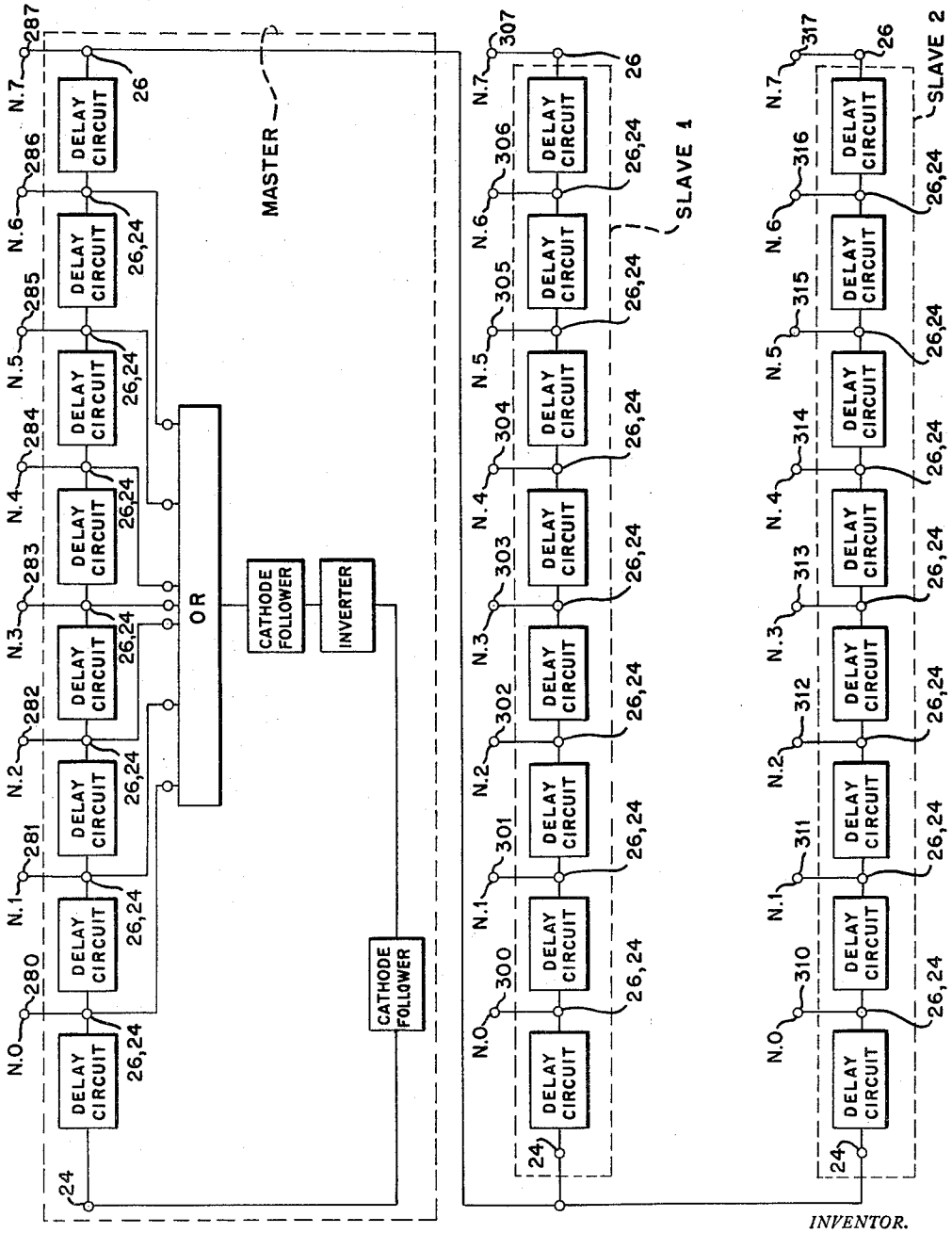

FIG. 12A

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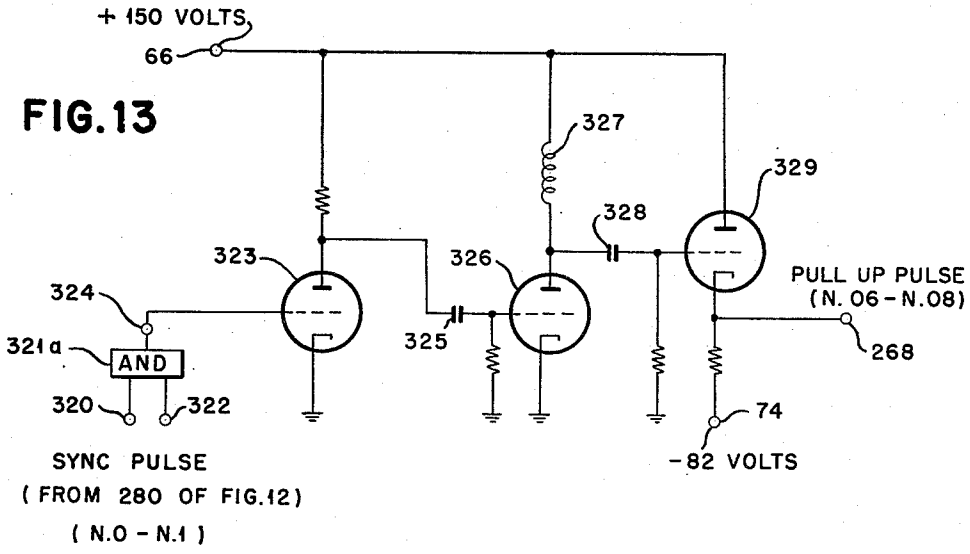
BY Dwight D. Mooney

ATTORNEY

FIG. 13



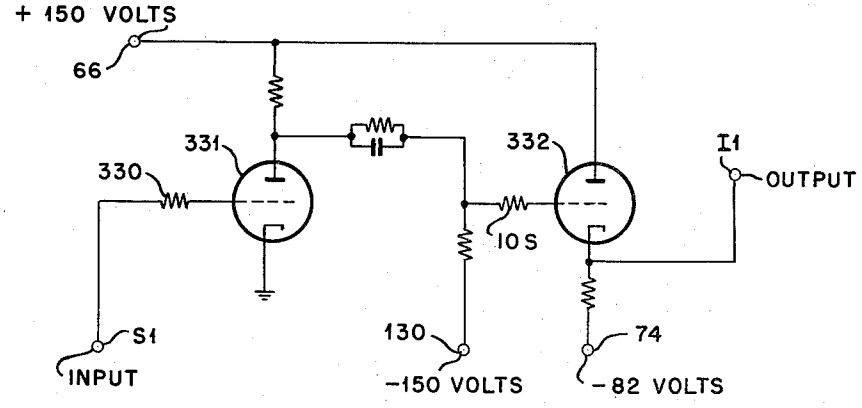


FIG. 14

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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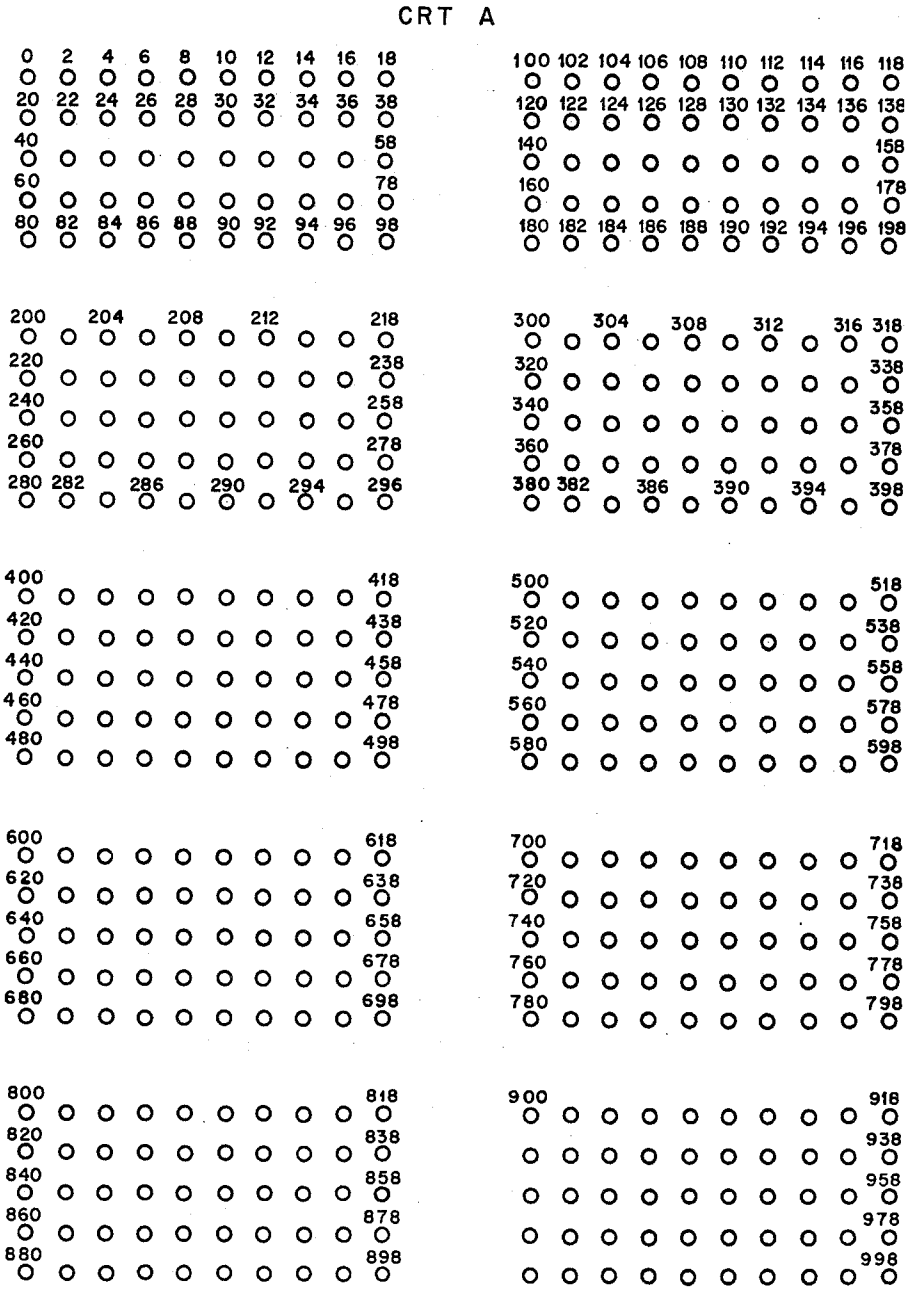

FIG. 15A

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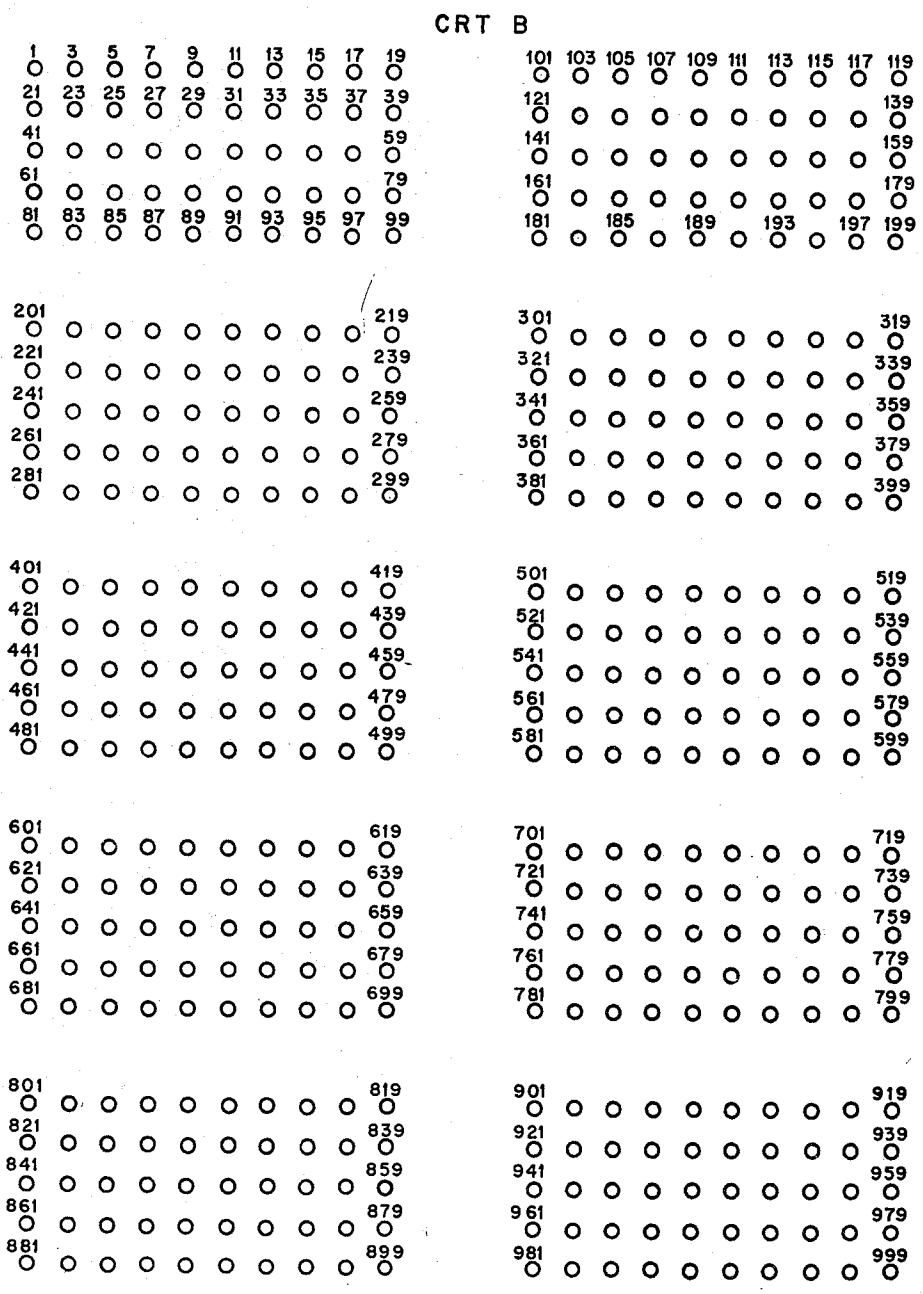

FIG.15B

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CRT C

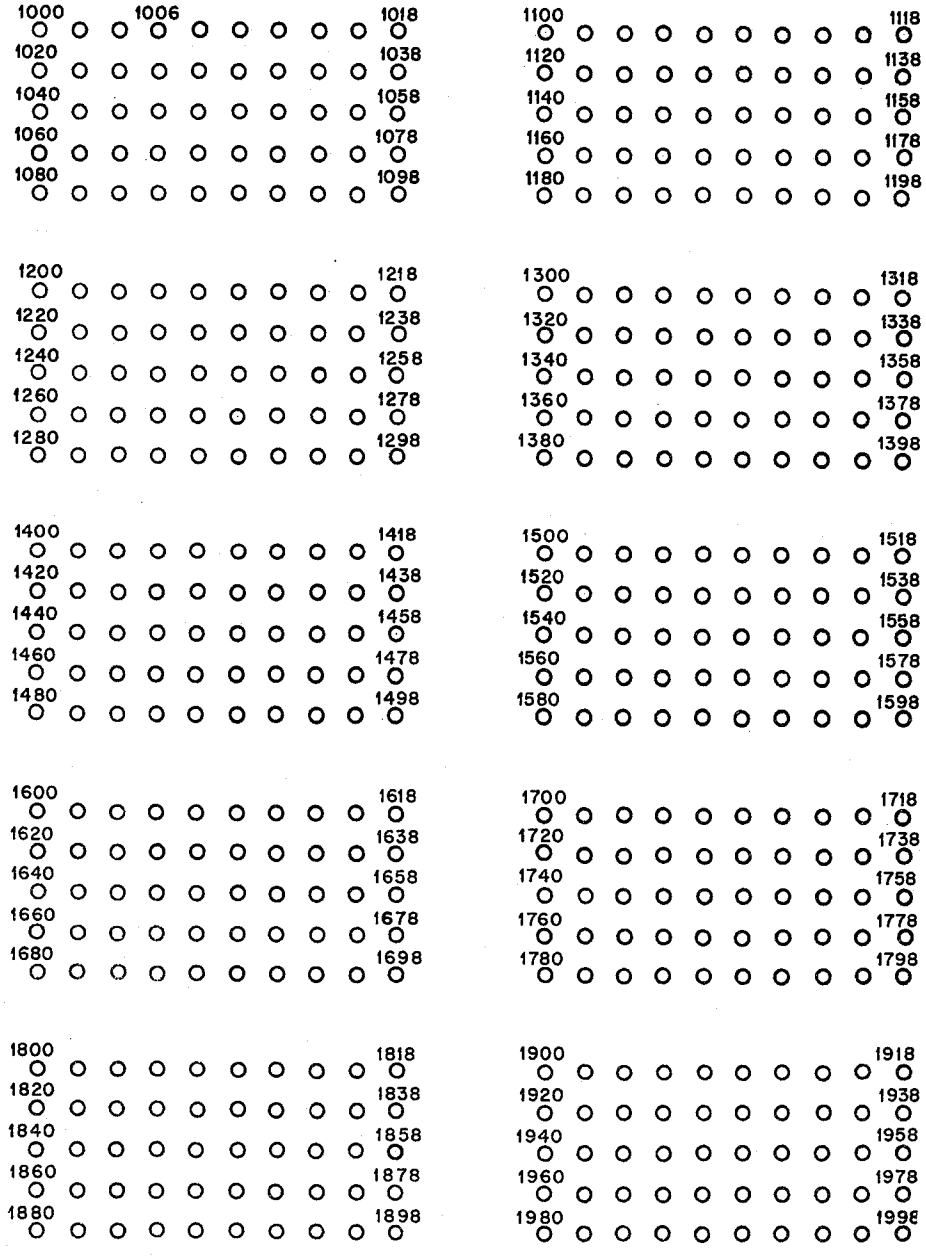

FIG. 15C

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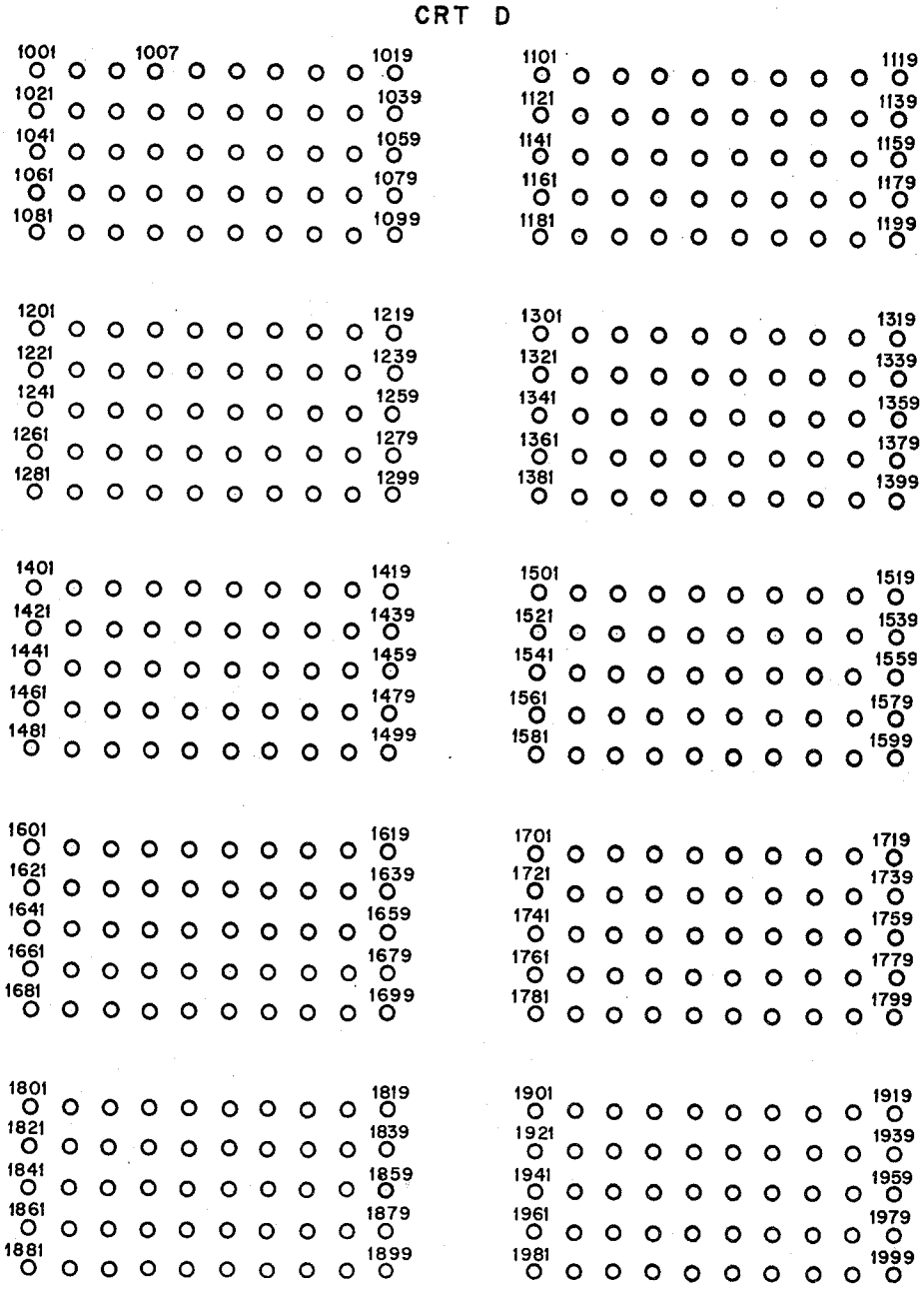

FIG.15D

INVENTOR.
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BY
Dwight D. Mooney

BINARY-DECIMAL ADDRESSES FOR HORIZONTAL & VERTICAL DEFLECTION CIRCUITS				DECIMAL NO. CORRESPONDING TO ADDRESSES
THOUSAND'S ORDER	HUNDRED'S ORDER	TEN'S ORDER	UNIT'S ORDER	
0000	0000	0000	0000	0
			0001	1
			0010	2
			0011	3
		TEN'S ORDER	0100	4
		INACTIVE	0101	5
			0110	6
			0111	7
			1000	8
		0000	1001	9
		0001		10
				11
				12
	HUNDRED'S ORDER	0001 REMAINS	INITIAL CYCLE	13
	IS INACTIVE	FOR EACH NEW	OF UNITS ORDER	14
		ADDRESS	REPEATED	15
				16
				17
THOUSAND'S ORDER		0001		18
IS INACTIVE		0001		19
		0010	0000	20
		0011		30
		0100		40
		0101	INITIAL CYCLE OF	50
		0110	UNITS ORDER RE-	60
		0111	PEATED EACH TIME	70
		1000	TEN'S ORDER ADVANCES	80
	0000	1001		90
	0001	0000	0000	100
	0010			200
	0011	INITIAL CYCLE OF		300
	0100	TEN'S ORDER RE-	INITIAL CYCLE OF	400
	0101	PEATED EACH	UNITS ORDER RE-	500
	0110	TIME HUNDRED'S	PEATED EACH TIME	600
	0111	ORDER ADVANCES	TEN'S ORDER ADVANCES	700
	1000			800
0000	1001			900
0001	0000	0000	0000	1000
	0001			1100
	0010			1200
	0011			1300
0001 REMAINS	0100	SAME		1400
FOR EACH NEW	0101		SAME	1500
ADDRESS	0110			1600
	0111			1700
	1000			1800
	1001	0000		1900
0001	1001	1001		1999
0010	0000	0000	0000	2000 (0)

FIG. 16

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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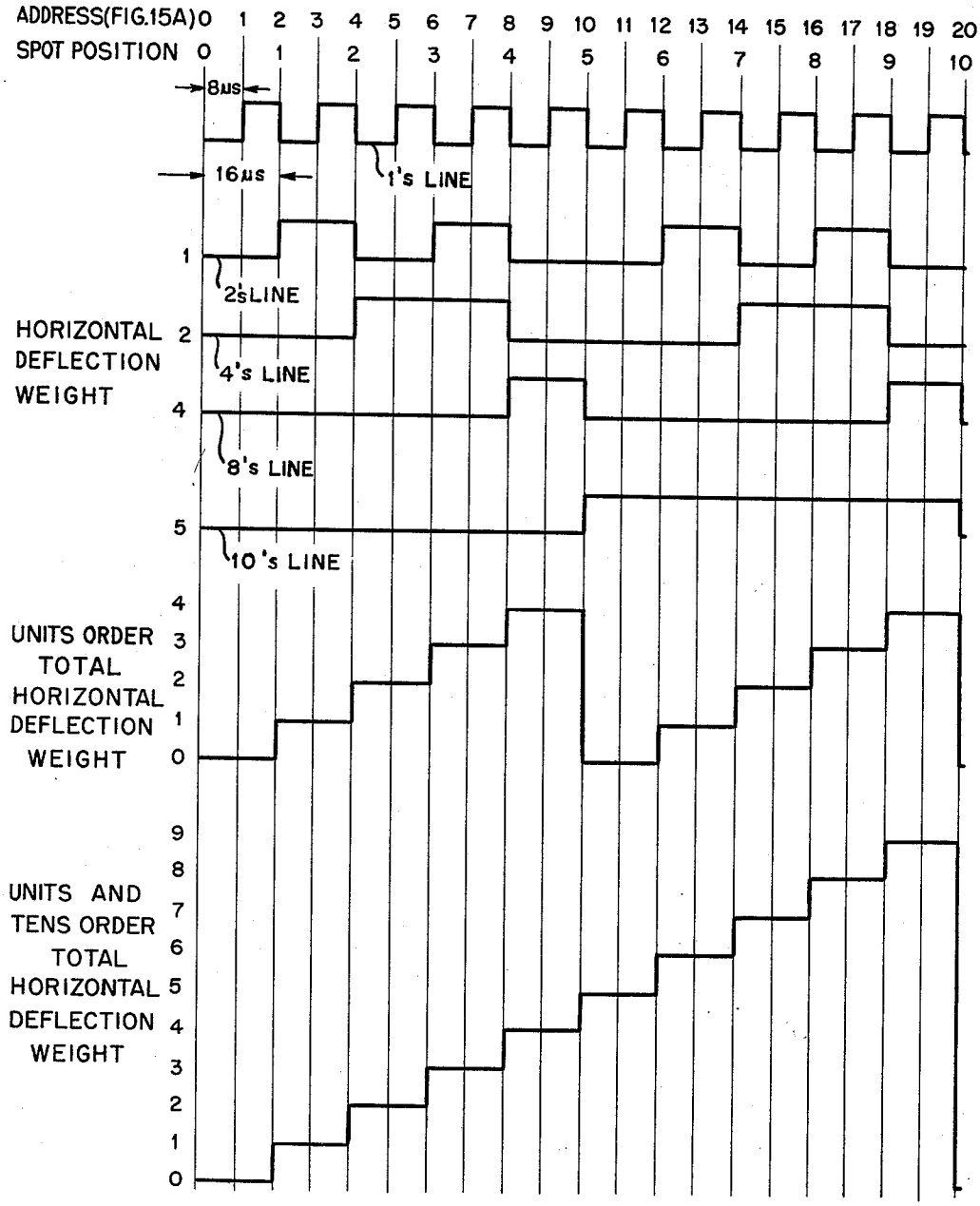

FIG.17

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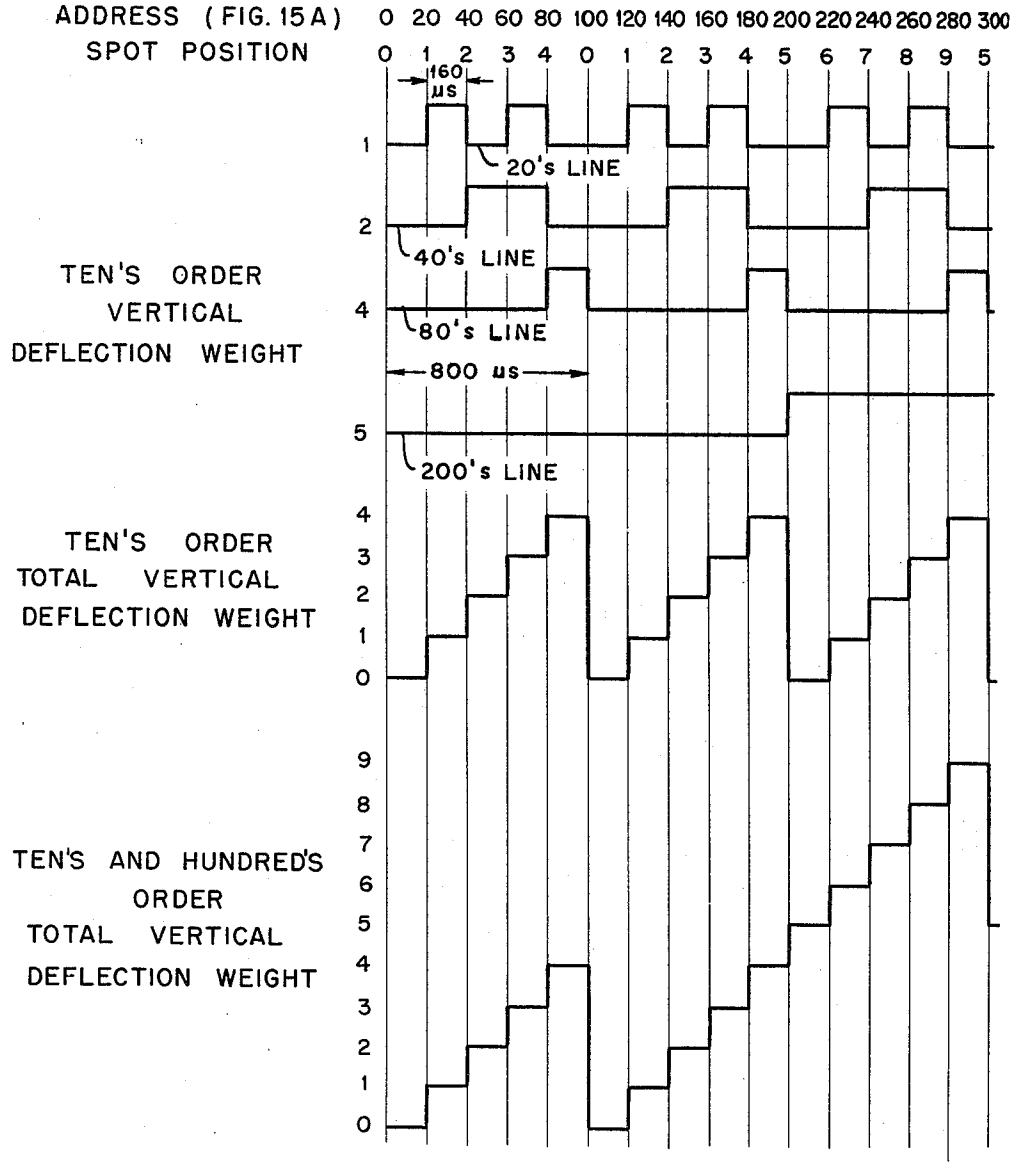

FIG. 18

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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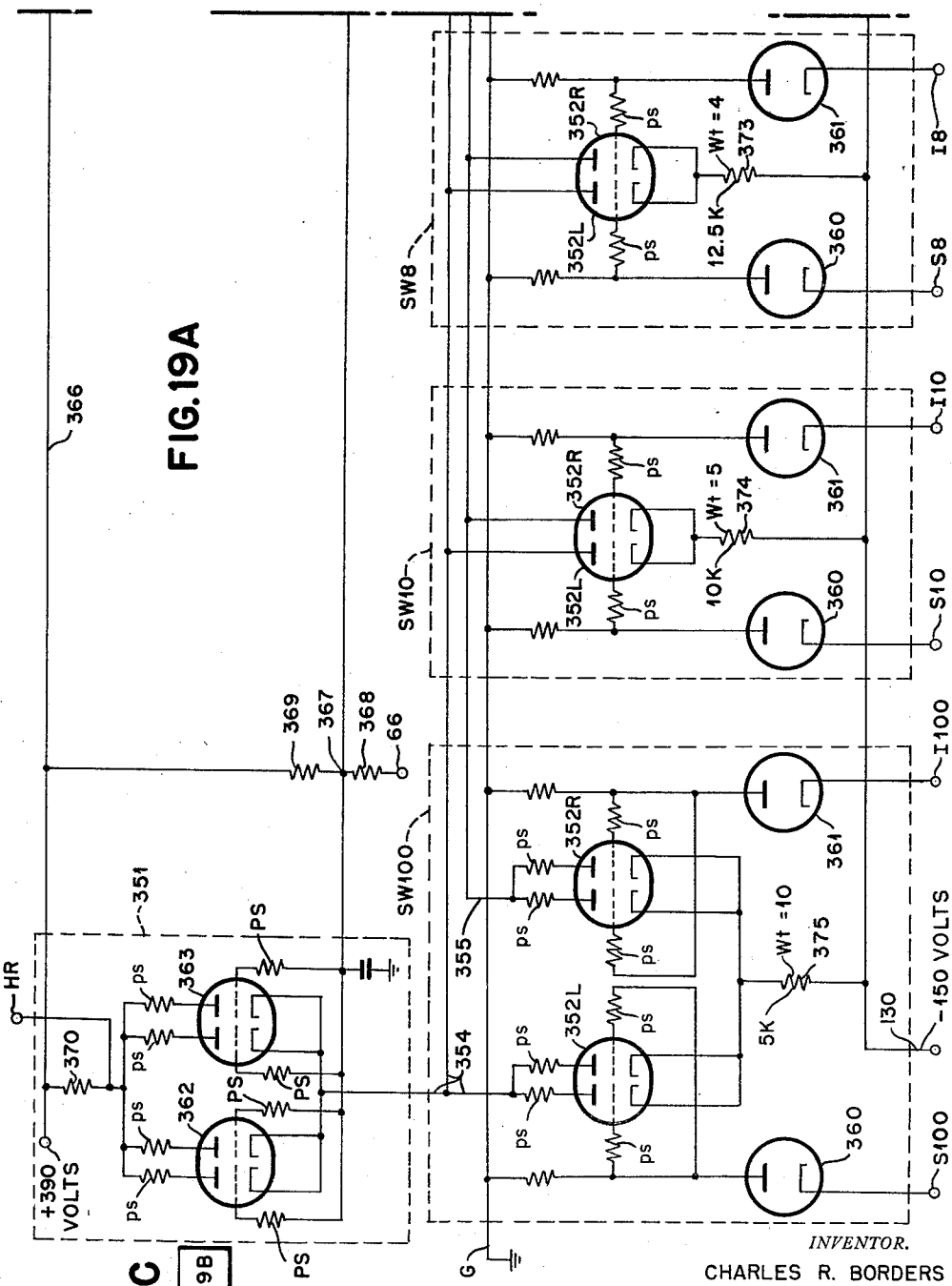

FIG. 19A

FIG. 19C

FIG. 19A	FIG. 19B

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Dec. 26, 1961 C. R. BORDERS 3,014,662

COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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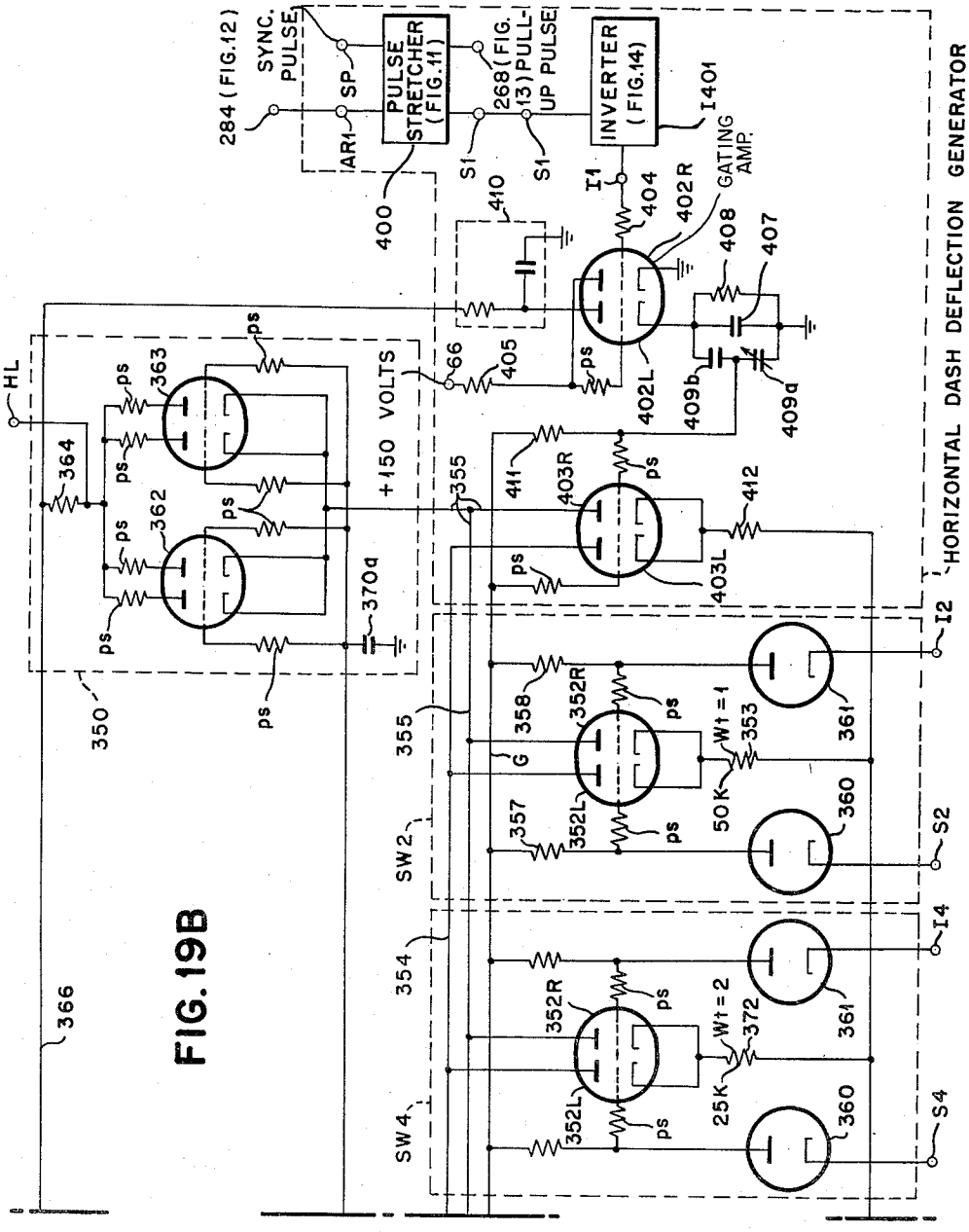

FIG. 19B

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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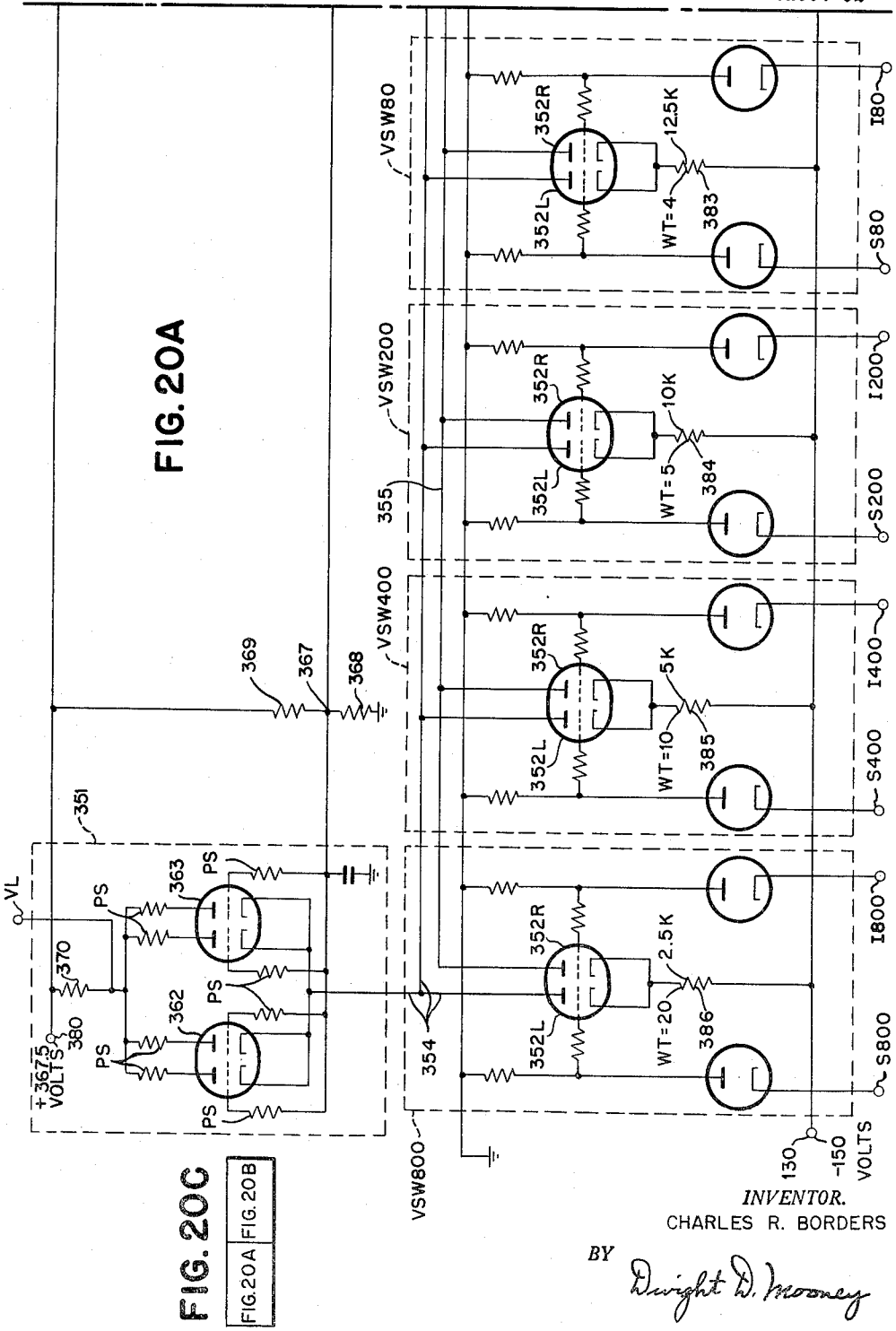

FIG. 20A

FIG. 20C

FIG. 20A	FIG. 20B

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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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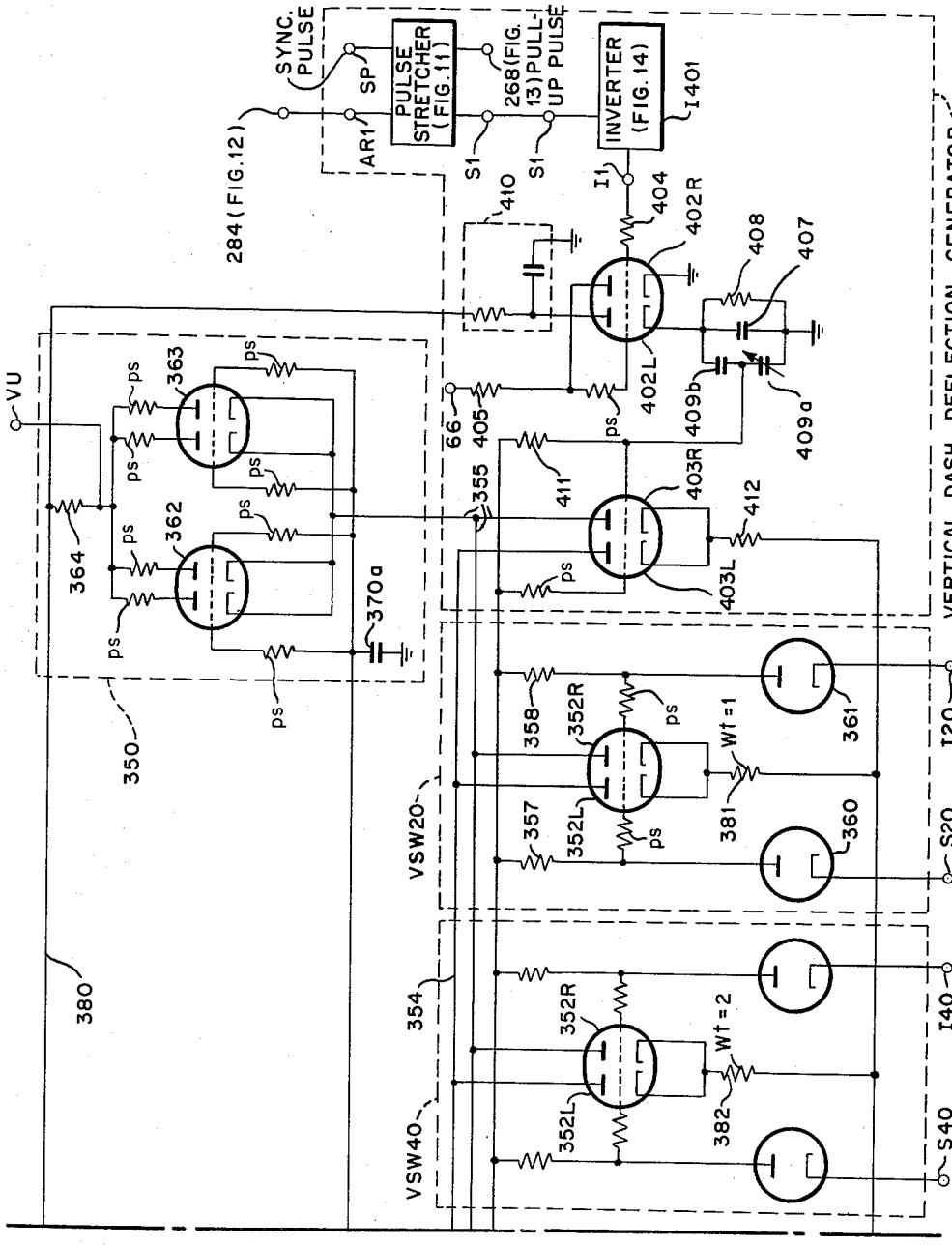

FIG. 20B

INVENTOR.
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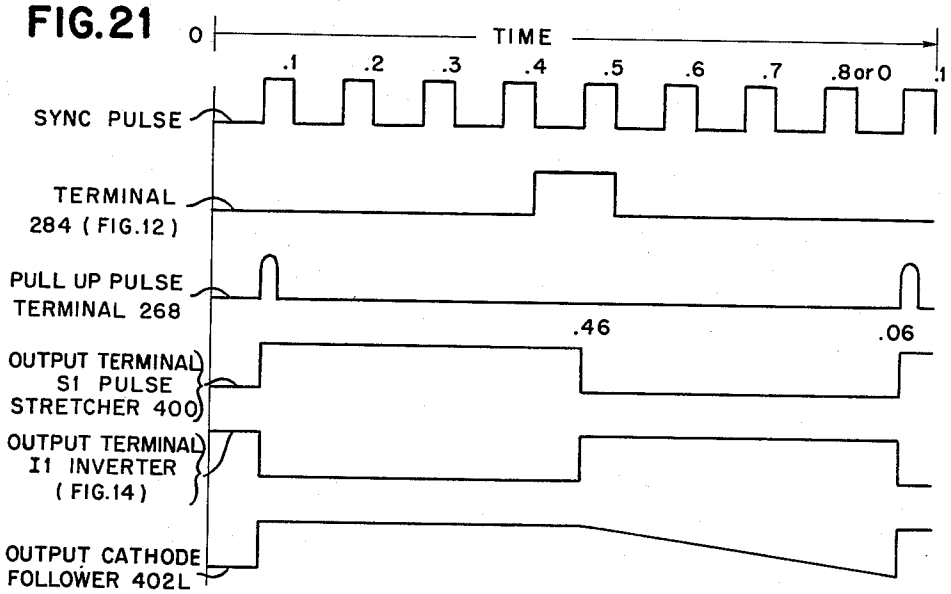
BY Dwight D. Mooney

FIG.21



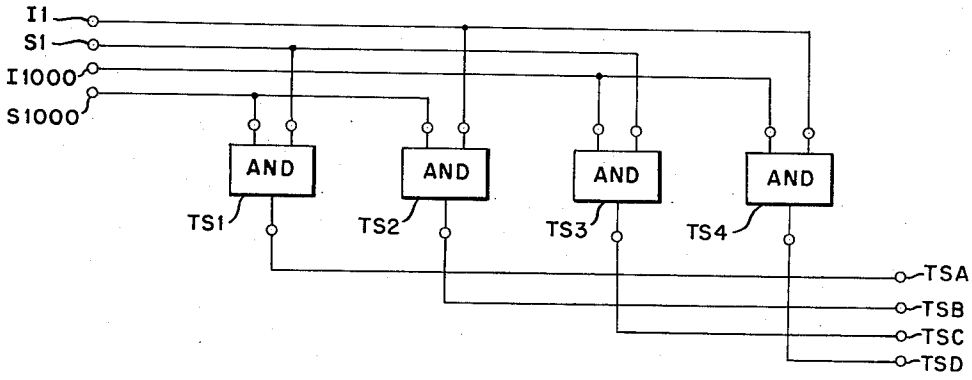


FIG.22

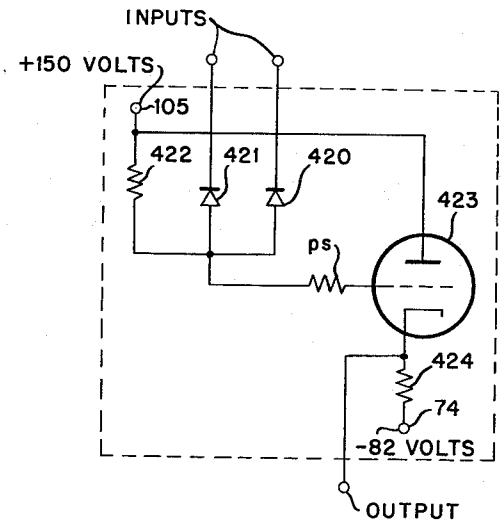


FIG.22A

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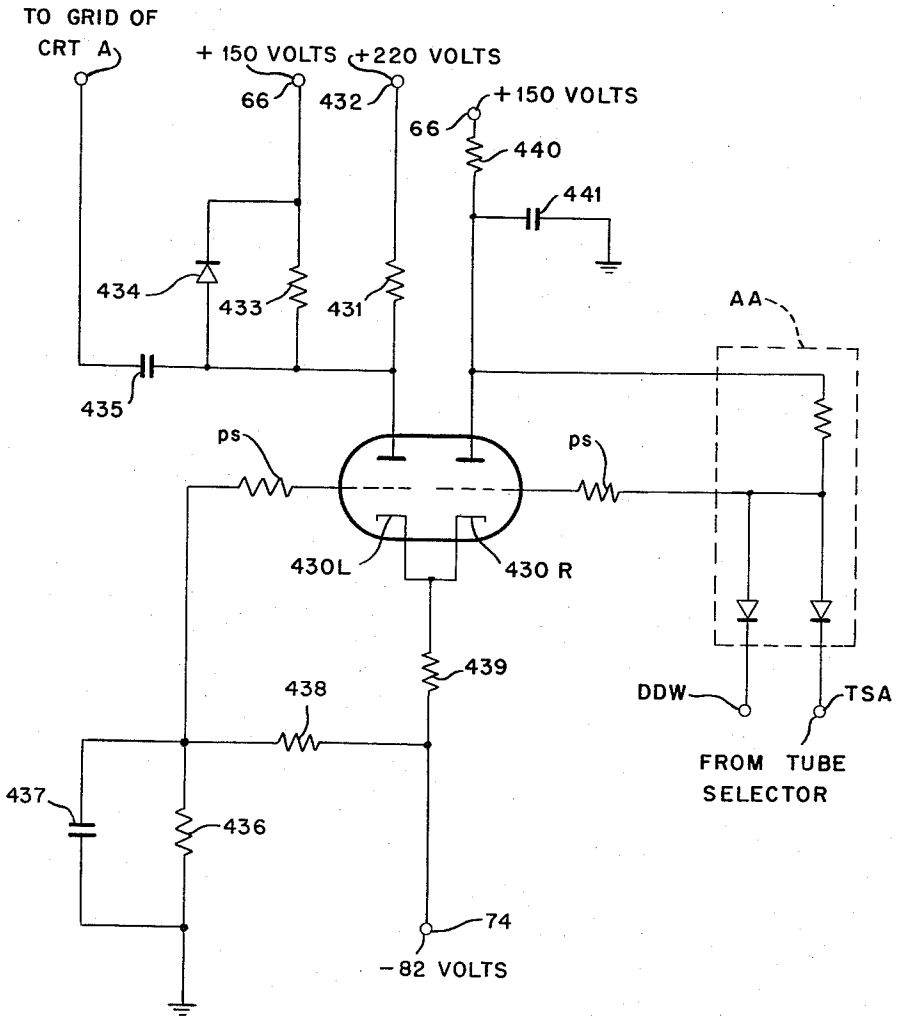
FIG. 23



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BY Dwight D. Mooney
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TIME	OPERATION	CIRCUIT POINTS (FIGS. 8C, 8D) THOUSANDS ORDER								
		17(INPUT)	14	13	16-1000	15-1000	D4000	D2000	D1000	D8000
9.30		0	0	0	0	0	1	0	1	0
9.40		0	1	0	0	1	0	1	0	1
9.50		0	0	0	0	0	1	0	1	0
9.60		0	1	0	0	1	0	1	0	1
9.70		0	0	0	0	0	1	0	1	0
10.00	READOUT 10	0	1	0	0	1	0	1	0	1
10.10		1	0	0	0	1	1	0	1	0
10.20		0	1	0	0	1	1	1	0	1
10.30		0	0	0	0	0	1	1	1	0
10.40		0	1	0	0	1	0	1	1	1
10.50		0	1	0	0	1	1	0	1	1
10.60		0	1	0	0	1	1	1	0	1
10.70		0	0	0	0	0	1	1	1	0
11.00	READOUT 11	0	1	0	0	1	0	1	1	1
11.10		1	1	0	1	0	1	0	1	1
11.20		0	1	1	1	0	0	1	0	1
11.30		0	0	1	0	1	0	0	1	0
11.40		0	1	0	0	1	1	0	0	1
11.50		0	0	0	0	0	1	1	0	0
11.60		0	0	0	0	0	0	1	1	0
11.70		0	1	0	0	1	0	0	1	1
12.00	READOUT 12	0	1	0	0	1	1	0	0	1
12.10		1	0	0	0	1	1	1	0	0
12.20		0	0	0	0	0	1	1	1	0
12.30		0	1	0	0	1	0	1	1	1
12.40		0	1	0	0	1	1	0	1	1
12.50		0	1	0	0	1	1	1	0	1
12.60		0	0	0	0	0	1	1	1	0
12.70		0	1	0	0	1	0	1	1	1

FIG. 24A

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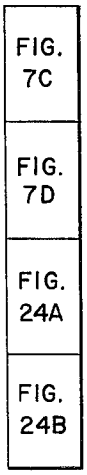
TIME	OPERATION	CIRCUIT POINTS (FIGS. 8C,8D) THOUSANDS ORDER								
		17(INPUT)	14	13	16-1000	15-1000	D4000	D2000	D1000	D8000
13.00	READOUT 13	0	1	0	0	1	1	0	1	1
13.10		1	1	0	1	0	1	1	0	1
13.20		0	0	1	0	1	0	1	1	0
13.30		0	1	0	0	1	1	0	1	1
13.40		0	1	0	0	1	1	1	0	1
13.50		0	0	0	0	0	1	1	1	0
13.60		0	1	0	0	1	0	1	1	1
13.70		0	1	0	0	1	1	0	1	1
14.00	READOUT 14	0	1	0	0	1	1	1	0	1
14.10		1	0	0	0	1	1	1	1	0
14.20		0	1	0	0	1	1	1	1	1
14.30		0	1	0	0	1	1	1	1	1
14.40		0	1	0	0	1	1	1	1	1
14.50		0	1	0	0	1	1	1	1	1
14.60		0	1	0	0	1	1	1	1	1
14.70		0	1	0	0	1	1	1	1	1
15.00	READOUT 15	0	1	0	0	1	1	1	1	1
15.10		1	1	0	1	0	1	1	1	1
15.20		0	1	1	1	0	0	1	1	1
15.30		0	1	1	1	0	0	0	1	1
15.40		0	1	1	1	0	0	0	0	1
15.50		0	0	1	0	1	0	0	0	0
15.60		0	0	0	0	0	1	0	0	0
15.70		0	0	0	0	0	0	1	0	0
0.00		0	0	0	0	0	0	0	1	0

FIG. 24B

FIG. 24C



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COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

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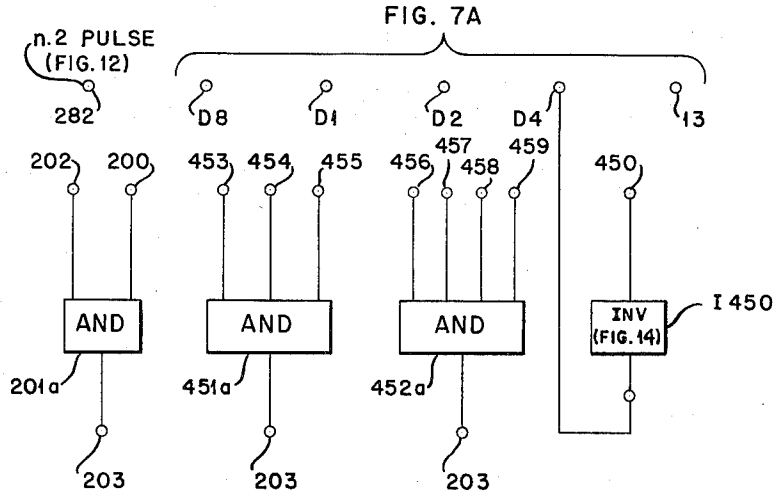
FIG. 25



TIME	COUNTING CAPACITY (CARRY AND CLEAR)	DESIGNATED TERMINALS CONNECTED TO TERMINALS LISTED IN SAME COLUMN						
		282 n.2PULSE	D4	D2	D1	D8	13	450
0.20	CC1	202	200					
1.20	CC2	202					200	
2.20	CC3		200			202		
3.20	CC4					202	200	
4.20	CC5		200		202			
5.20	CC6				202		200	
6.20	CC7		455		453	454		
7.20	CC8				453	454	455	
8.20	CC9	455	453	454				
9.20	CC10			202			200	
10.20	CC11	456	457	458		459		
11.20	CC12	456		457		458		459
12.20	CC13	456	457	458	459			
13.20	CC14	456		457	458			459
14.20	CC15		456	457	458	459		
15.20	CC16	456		457	458	459		

FIG. 26

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BY Dwight D. Mooney

United States Patent Office 3,014,662 Patented Dec. 26, 1961

3,014,662

COUNTERS WITH SERIALLY CONNECTED DELAY UNITS

Charles R. Borders, Alpine, N.J., assignor to International Business Machines Corporation, New York, N.Y., a corporation of New York

Filed July 19, 1954, Ser. No. 444,251
30 Claims. (Cl. 235—176)

This invention relates to electronic circuits and more particularly to a novel regeneration type counter.

In the binary notation only two digits are employed; i.e., 0 and 1. The binary digit 0 is represented by decimal digit 0 and the binary digit 1 is represented by decimal digit 1. These binary digits are referred to as bits. The digital positions or orders in a binary number, reading from right to left, correspond in value to 2^0, 2^1, 2^2, 2^3, 2^4, etc. or decimal digits 1, 2, 4, 8, 16, etc. respectively. For example, binary number 1001 represents decimal digit 9 which is determined by the addition of decimal digits 1 and 8 indicated by a binary 1 in the extreme right and left binary positions respectively. Hence, by using binary bits or pulses in groups of four wherein a pulse represents a binary 1 and the absence of a pulse represents a binary 0 any decimal digit from 0–9 inclusive may be written in the pure binary-notation.

This system of representing decimal numbers, digit for digit, in the pure binary notation is referred to herein as the binary-decimal system. The four consecutive binary orders, reading from right to left, represent the decimal digits 1, 2, 4 and 8 for the units decimal order and are accordingly referred to as the 1 bit, 2 bit, 4 bit and 8 bit respectively. It follows that the four binary orders of the tens decimal order represent the decimal digits 10, 20, 40 and 80, respectively. Likewise, in subsequent decimal orders, for example, the four respective binary orders of the hundreds decimal order represent the decimal digits 100, 200, 400 and 800 respectively.

As an example, 459 will be represented in the binary-decimal system by 0100,0101,1001. The four binary bits at the right represent the decimal digit 9 of the units order, the next four bits to the left represent the decimal digit 5 of the tens order, and the four bits at the extreme left represent the decimal digit 4 of the hundreds order.

Any decimal number from 0–15 inclusive can be represented by a group of four binary bits. If the decimal number is 16, than a binary carry occurs to the next group of binary bits to be added or to the next decimal order. However, in the binary-decimal system, only the decimal digits 0–9 inclusive are represented by each group of four binary bits.

The addition of two decimal digits or a decimal column of the decimal numbers to be added may provide at most a sum of 18 plus a carry. The range of decimal sums is, therefore, 0–19 inclusive. As stated, if this addition is performed in the pure binary notation, and the sum is 16 or more, a carry is provided and in any case if the sum is over 9 (1001), it is not expressed in the binary-decimal system by mere binary addition. It follows that the sum, in the binary-decimal system of two decimal numbers written in the binary-decimal system, may be obtained by adding the two numbers in the pure binary notation and providing circiut means response to a sum greater than 9 (1001), which circuit means will reduce such sums to the appropriate digit (less than ten) and a decimal carry.

A principal object of the invention is to provide a novel regeneration counter which produces a cyclic output representative of the value stored therein.

Another object is to provide a novel regeneration counter wherein binary bits are read in serially and the

binary sum of the bits read in is read out either serially or in parallel.

A further object is to provide a regeneration counter having a predetermined maximum storage capacity for any preselected value from 1 to 16, inclusive.

A still further object is to provide a regeneration counter which automatically effects clear and carry in response to any predetermined number of input pulses.

Another object is to provide a regeneration counter including a binary adder and a plurality of delay circuits for effecting storage of binary bits received in sequence and providing an output, representing the sum stored, in either parallel form or serial form.

Still another object of the invention is to provide a novel octal counter for producing similar pulses during each of eight uniform time intervals collectively comprising a predetermined cycle.

A further object is to provide a novel circuit means for cyclically producing uniformly spaced pulses in time wherein the initiation of the production of a certain preselected pulse of each cycle causes the initiation of a new cycle of operation.

Another object is to provide a novel regeneration counter having a plurality of serially connected orders wherein the amount stored in each order is in circulation and is read out periodically in response to a single read out pulse.

A further object is to provide a plural order counter wherein pulses representing the amount stored therein are in continuous circulation to provide a cyclically repetitious read out in the absence of successive read in.

A still further object is to provide a novel octal commutator operable as a master to produce eight uniformly spaced pulses during each cycle of operation and to control slave commutators for producing similar pulses synchronized therewith.

Other objects of the invention will be pointed out in the following description and claims and illustrated in the accompanying drawings, which disclose, by way of example, the principle of the invention and the best mode, which has been contemplated, of applying that principle.

In the drawings:

FIGS. 1A, 1B and 1C are block diagrams of a cathode ray storage system,

FIG. 1D shows the arrangement of FIGS. 1A, 1B and 1C to form a complete block diagram of the storage system,

FIGS. 2 and 2B are circuit and block diagrams respectively of a delay circuit employed in practicing the invention,

FIG. 2A shows waveforms explanatory of the operation of the circuit of FIG. 2.

FIG. 3 is a circuit diagram of a typical AND circuit employed by the invention,

FIG. 4 is a circuit diagram of a typical OR circuit employed by the invention,

FIG. 5 is a circuit diagram of a binary adder employed by the invention,

FIGS. 6A and 6B show in block diagram form a clamp and sync signal, and clamp and sync pulse source suitable for use with the delay circuits employed in practicing the invention,

FIG. 6C shows idealized waveforms explanatory of the operation of FIGS. 6A and 6B,

FIG. 7A shows in block diagram form one order of the regeneration counter of the invention,

FIG. 7B is a circuit diagram of a clamp and sync inverter suitable for use in FIG. 7A.

FIGS. 7C and 7D comprise a chart indicating a cycle of operation for the counter order shown in FIG. 7A,

FIG. 7E shows the arrangement of FIGS. 7C and 7D to form a single chart,

FIGS. 8A, 8B, 8C and 8D comprise a diagram of the regeneration counter of the invention and the address switch employed,

FIG. 8E shows the arrangement of FIGS. 8A, 8B, 8C and 8D to form a single diagram,

FIGS. 9A, 9B and 9C are charts explanatory of the operation of the counter of FIGS. 8A, 8B, 8C and 8D,

FIG. 10 shows the arrangement of FIGS. 7C, 7D, 9A, 9B and 9C to form a single chart explanatory of the operation of the entire counter of FIGS. 8A, 8B, 8C and 8D,

FIG. 11 is a circuit diagram of a pulse stretcher employed by the invention.

FIG. 11A is a timing chart explanatory of the operation of the pulse stretcher of FIG. 11,

FIG. 12 is a diagram of a free running octal commutator of the invention,

FIG. 12A is a diagram of a free running octal commutator of the invention employing master and slave commutators,

FIG. 13 shows a suitable circuit for providing the pull up pulse required for the operation of the circuit diagram of FIG. 11,

FIG. 14 is a circuit diagram of an inverter,

FIGS. 15A, 15B, 15C and 15D, respectively, show the physical arrangement of stored information upon the face of the CRTs A, B, C and D shown in FIG. 1C,

FIG. 16 is a chart showing the operation of the regeneration counter or voltages applied to the deflection circuits and to the tube selector to obtain a deflection of the electron beams to corresponding addresses,

FIG. 17 is a horizontal deflection weight voltage chart representing the voltage values employed to produce horizontal beam deflection to the indicated addresses and spot positions,

FIG. 18 is a vertical deflection weight voltage chart representing the voltage values employed to produce vertical beam deflection to the indicated addresses and spot positions,

FIGS. 19A and 19B show horizontal deflection circuits suitable for producing the storage pattern shown in FIGS. 15A, 15B, 15C and 15D.

FIG. 19C shows the placement of FIGS. 19A and 19B to form the complete horizontal deflection circuits,

FIGS. 20A and 20B comprise a circuit diagram of a vertical deflection circuit suitable for use with the invention,

FIG. 20C shows the arrangement of FIGS. 20A and 20B to realize a complete vertical deflection circuit diagram,

FIG. 21 shows waveforms realized from operation of the dash deflection generator shown in FIGS. 19B and 20B,

FIG. 22 is a block diagram of the tube selector,

FIG. 22*a* is a circuit diagram of a circuit suitable for use in the tube selector of FIG. 22,

FIG. 23 is a circuit diagram of a suitable AND circuit and pulse shaper circuit,

FIGS. 24A and 24B comprise a chart showing the operation of the regeneration counter when decimal numbers 9 to 15 are read out,

FIG. 24C shows the placement of FIGS. 7C, 7D, 24A and 24B to form a single chart showing operation of the regeneration counter for read out of all numbers from 0 to 15,

FIG. 25 is a diagrammatic showing which provides for connections to cause the regeneration counter of FIG. 7A to read out when it reaches any predetermined number from 0 to 15, and

FIG. 26 is a chart showing the particular connections made in FIG. 25 to obtain read out of each number from 1 to 16,

Various circuits used herein or particular points within the circuits are frequently referred to as Up or Down. Up means that the voltage present at the particular point or at the output of the circuit designated is positive with respect to ground. Down means that the voltage present at the particular point or at the output of the circuit designated is negative with respect to ground. If the control grid of a vacuum tube is referred to as Down, it means that the voltage at that control grid is below the cutoff value for the vacuum tube if the cathode thereof is grounded, otherwise it means that the voltage is at the lower of two values each of which is present during the operation of the tube.

Numerous coincidence circuits are employed herein. An AND circuit refers to a circuit which is operable to produce a positive voltage at its output terminal only when all of the input terminals thereof have a positive voltage applied thereto simultaneously. An OR circuit refers to a circuit operable to produce a positive voltage at its output terminal when only one or a plurality of the input terminals thereof have a positive voltage applied thereto.

When information is stored on a cathode ray tube it must be refreshed or is lost. The time during which this refreshing is effected is referred to herein as a regeneration cycle.

Information is read in or read out of cathode ray tube storage during a preselected operational cycle. This cycle is referred to herein as an action cycle.

As described herein each regeneration cycle and each action cycle have a duration of 8 microseconds or eight time intervals.

As used herein a word is represented by 16 decimal digits to be stored. The term CRT unit refers to four cathode ray tubes operated in parallel to accommodate the storage of a single binary bit of each of the words to be stored.

The system of timing designation used herein comprises a combination of octal and decimal representations. For example, in designation 1:15 the 1 to the left of the decimal point represents the number of cycles already performed, the 1 to the right of the decimal point represents the particular microsecond interval of the cycle, and the second number 5 to the right of the decimal point represents that the time referred to is $\frac{5}{10}$ of a microsecond in addition to the one microsecond represented by the 1 to the right of the decimal point. Hence, the time indicated is $1\frac{5}{10}$ microseconds after the beginning of the second cycle.

As a further example, the time designation 4.30 represents the beginning of the third microsecond interval of the fifth cycle, four cycles having already elapsed.

Each cycle has a duration of eight microseconds.

As a still further example a pulse may be said to be present from N.10 to N.20. This means that a pulse having a duration of one microsecond occurs between the first and second microsecond intervals of each cycle.

General description

The regeneration counter of the invention is illustrated as employed in an electrostatic cathode ray storage system. All operations of the storage system are effected during either an action cycle or a regeneration cycle.

Referring more particularly to FIGS. 1A, 1B and 1C, the input to the regeneration counter is a positive counter advance pulse applied to terminal CA from time N.10 to N.20 of each action and regeneration cycle. Circuit means are described hereinafter for rendering the counter advance pulse ineffective during an action cycle. Hence, the counter advance pulse is effective to advance the storage effected by the regeneration counter only during regeneration cycles. The output at the regeneration counter is available during one time interval of each regeneration cycle or during one-eighth of the time of that cycle. Each output of the regeneration counter consists of a preselected number of binary outputs or representations of binary bits in parallel and is used to position the electron beams of the cathode ray tubes to

a preselected position or address. Each subsequent counter advance pulse is added to the output of the counter, which output is used to cause the electron beams to assume the next preselected position or address during a regeneration cycle; during an action cycle the counter is effectively stationary. The regeneration counter therefore provides the address control required to obtain a refreshing or regeneration, during all regeneration cycles of the information electrostatically stored on the face of the cathode ray tubes. The output of the regeneration counter is present in the binary-decimal notation at the terminals D1–D8000 (FIG. 1B). The output of the regeneration counter serves as one input to the address switch (FIG. 1B). The address switch includes another group of input terminals designated A1–A8000. These terminals receive an input in the binary-decimal notation similar to the output of the regeneration counter and in each instance designate the one of the addresses or beam positions to be selected during that action cycle. The actual generation of the pulses applied to terminals A1–A8000 is not shown herein. It is understood that any suitable source may be employed.

The address switch includes a plurality of two-pole-two-position switches. The inputs of these separate switches are connected to corresponding terminals A1–A8000 and D1–D8000. For example, one switch has one of its input terminals connected to terminal D1 and its other input terminal connected to terminal A1. As a further example, the terminals A1000 and D1000 are connected to the respective inputs of another switch. During an action cycle, a voltage is applied to each address switch such that the switch is energized if an input is provided by the A terminal connected thereto. During a regeneration cycle, a voltage is applied to each switch such that the switch is energized if an input is provided by the D terminal connected thereto. During each cycle, action or regeneration, an output is present from time N.00 to N.10 at the output terminals AR1–AR8000 of the address switch. The output at these terminals is applied to the pulse stretchers (FIG. 1B) which provide outputs at the corresponding output terminals S1–S8000 during substantially the entire portion of that cycle. These output terminals S1–S1000 are connected to supply inputs to the inverters (FIG. 1A) to provide an output at the terminals I1–I1000.

The cathode ray tube (CRT) storage unit (FIG. 1C) comprises four cathode ray tubes CRT A, CRT B, CRT C and CRT D having their deflection plates connected in parallel so that the electron beam of each tube is always at the same position or address as that of the others. The tube selector (FIG. 1A) having its inputs supplied from terminals I1, S1, I1000 and S1000 determines which of the cathode ray tubes CRT A, CRT B, CRT C or CRT D is selected for read in, read out or regeneration during the particular action or regeneration cycle being performed. At any given time only one of the cathode ray tubes is operable. Hence, CRTs A, B, C and D function as a single tube and effect the storage of a single binary bit. Four cathode ray tubes are used instead of one in order to decrease the spot or density of storage areas and thereby decrease the effect of interaction between the storage areas. Since any decimal digit to be stored includes four binary bits, four such units or 16 cathode ray tubes will be required to store one decimal digit. Hence, if a word to be stored includes 16 decimal digits a total of 16×16 or 256 cathode ray tubes will be required.

The terminals S2–S10, S100, I2–10, and I100 are connected to supply inputs to the horizontal deflection circuits and terminals S2–S80, S200–S800, I20–I80 and I200–I800 are connected to supply inputs to the vertical deflection circuits. The output terminals HR and HL of the horizontal deflection circuits are connected respectively to the right and left horizontal deflection plates of the CRTs A, B, C and D. The output terminals VU and VL of the vertical deflection circuits are connected respectively to the upper and lower plates of the CRTs A, B, C and D. The voltage present at these outputs is such that the deflection of the electron beam in each CRT A, B, C and D follows a predetermined pattern in response to inputs to the terminals A1–A8000 and terminals D1–D8000.

Circuits under the control of the tube selector and an external voltage representative of a dot and a dash supply an increased voltage to the grid of the cathode ray tube selected to effect the read in of a dot or dash, as the case may be, during an action cycle. During a regeneration cycle these circuits effect the refreshing or regeneration of the information previously stored.

A pickup plate P is placed in proximity to the face of each CRT and connected in parallel to storage output circuits to effect a read out of the information stored.

Delay circuit

Referring more particularly to FIGS. 2 and 2A, the delay circuit shown is used repeatedly herein. This circuit is claimed in the application of Byron L. Havens, Serial No. 239,370, filed July 30, 1951, now Patent 2,624,839 on January 6, 1953 and reissued as Re. 23,699 on August 18, 1953. The curves of FIG. 2A demonstrate the operation of the circuit shown in FIG. 2. In order to facilitate the description, the time axis (abscissa) is divided into equal time intervals designated T1, T2, T3, T4 and T5, respectively. The length of each of these time intervals is dependent upon the particular circuit design and as used herein is equal to one microsecond or the time elapsing between the initiation of the addition of one decimal column and the initiation of the addition of the next decimal column to be added.

Briefly, an input pulse (FIG. 2A) is applied to the input terminal 24 of the circuit shown in FIG. 2 during one preselected time interval and produces an output pulse (FIG. 2A) at the output terminal 26 during the next subsequent time interval. An input pulse may be applied to the input terminal 24 during the same time interval, T3 for example, that an output pulse is produced at the output terminal 26. The flyback produced by an input pulse is used to set up the output pulse and the circuitry is such that there is complete isolation between the output and input pulse during any given time interval.

A clamp pulse (FIG. 2A) is applied to the terminal 62 to wipe out or remove the information stored in the delay circuit after that information has been utilized.

The anode of tube L is connected through inductance 64 and an anode load resistor 65, in parallel, to a +150 volt terminal 66. The inductance 64 is provided to increase the voltage swing in the positive direction at the anode of the tube L (FIG. 2A during T3 and T4) for a preselected time immediately after that tube is rendered non-conductive.

The diode rectifiers 67 and 68 connected respectively to input terminal 24 and terminal 69, and the resistor 70 connected between the juncture 71 of the diodes 67 and 68 and the +150 volt terminal 66 comprise an AND circuit generally designated as 70*a*. This juncture 71 is connected through a parasitic suppressor resistor *ps* to the control grid of the tube L.

The tube R is operated as a cathode follower and is always conductive during operation of the delay circuit. The cathode load resistor 73 is connected to a −82 volt terminal 74 which is also connected through a resistor 75 and a condenser 76 to the anode of the tube L. The terminal 62 is connected through a resistor 77 and diode rectifiers 78, 79 and 80, in series, to a −30 volt terminal 81. The juncture 82 is connected between the rectifiers 79 and 80 and between the resistor 75 and condenser 76. The juncture 83 joining rectifiers 78 and 79 is connected through a parasitic suppressor resistor *ps* to the control grid of the tube R and through a condenser 85 to ground.

During the time interval T1, an input pulse is not ap-

plied to the input terminal 24 and juncture 71 is therefore Down so that a positive voltage is not applied to the control grid of the tube L. During this time interval the tube L is non-conductive, tube R is conductive, and output terminal 26 is Down. The voltage at the anode of tube L is +150 volts and the condenser 76 is charged with 180 volts appearing across it, the left plate is at +150 volts and the right plate is at −30 volts. The juncture 82 cannot be appreciably more negative than the −30 volt terminal 81 because when such is attempted the rectifier 80 conducts and maintains the voltage at juncture 82 up to essentially that of the terminal 81. It is the conduction of rectifier 80 during the time interval T1 that keeps juncture 82 at approximately −30 volts. The resistor 75 tends to prevent the voltage at juncture 82 from drifting between the application of successive clamping pulses.

The juncture 83 is also at −30 volts and condenser 85 is charged with −30 volts on its upper plate and its lower plate is at 0 volts (ground). Rectifier 79 conducts when condenser 85 is being charged and when the clamping pulse (FIG. 2A) applied to the terminal 62 attempts to pull the juncture 83 below −30 volts, the voltage at the terminal 81. Hence, when the clamping pulse is most negative, the voltage at the control grid of the tube R has been pulled Down, and since tube R is a cathode follower, the voltage at the output terminal 26 is also pulled Down.

This action effects the wiping out of the information stored after that information has been used. In other words, the output pulse produced is brought to an end as shown at the beginning of time intervals T4 and T5 (FIG. 2A). When the clamping pulse thus goes negative the rectifier 78 is rendered conductive.

During the latter portion of time interval T2 the input pulse and synchronous pulse are both positive simultaneously. The juncture 71 is therefore Up and the tube L becomes heavily conductive and the voltage at its anode decreases rapidly (FIG. 2A). The condenser 76 discharges through the tube L. The resulting tendency of juncture 82 to acquire the same voltage increment as the anode of the tube L is arrested by the conduction of rectifier 80 and the voltage at this juncture remains −30 volts.

Just at the start of time interval T3 the synchronous pulse goes negative and the voltage at the juncture 71 and control grid of tube L accordingly goes Down and tube L is rendered non-conductive. As a result, the voltage at the anode of the tube L increases rapidly and actually exceeds +150 volts because this anode circuit is less than critically damped during the flyback time. It is this increased voltage of flyback, which initiates the output pulse. This voltage is transferred through condenser 76 to cause the voltage at juncture 82 to go Up (to approximately +5 volts) from −30 volts. The rectifier 79 then conducts to cause the juncture 83 and control grid of tube R to go Up and the upper plate of condenser 85 is charged positive relative to its lower or grounded plate. The voltage at the output terminal 26 connected to the cathode of the tube R follows the control grid thereof and goes Up to initiate the output pulse during the time interval T3.

As the voltage at the anode of the tube L decreases toward +150 volts the voltage at juncture 82 similarly decreases. During the latter portion of time interval T3 the voltage at juncture 82 is again approximately −30 volts. Both the terminals 24 and 69 again go positive as shown by the second input pulse and synchronous pulse which occur during the latter part of time interval T3 while the output terminal 26 is still Up.

As a result that tube L again becomes heavily conductive and the voltage at its anode decreases and the juncture 82 again remains at −30 volts because of the conduction through rectifier 80.

When the clamping pulse goes negative at the start of time interval T4, conduction through rectifiers 78, 79 and 80 results and juncture 83 as well as juncture 82 is placed at approximately −30 volts. The control grid of tube R and output terminal 26 therefore go Down and the output pulse, occurring during time interval T3 and produced in response to the input pulse applied during time interval T2, is terminated.

When the juncture 71 goes Down at the start of time interval T4, the tube L becomes non-conductive and its anode voltage starts to increase rapidly as described hereinbefore.

This increased voltage causes the juncture 82 to go Up, the juncture 83 to go Up and the output terminal 26 to go Up as indicated by the output pulse occurring during time interval T4. The voltage at the anode of the tube L finally settles, during the time interval T5, at a steady value of +150 volts in accordance with the damping effect. If an input pulse was applied during the time interval T4, the voltage at the anode of tube L would never reach a steady value of +150 volts during T5 time. Such is indicated by this anode voltage during the time interval T3.

Just prior to the anode of tube L reaching a steady voltage value the clamping pulse goes negative (time interval T5). At this time the juncture 82 has again assumed a voltage value of −30 volts, but the juncture 83 is still Up. When the clamping pulse causes the terminal 62 to go negative the rectifiers 78, 79 and 80 are rendered conductive and the voltage at the juncture 83 goes Down to terminate the output pulse at the beginning of time interval T5.

It is now clear that the use of flyback makes possible the production of an output pulse in one preselected time interval in response to an input pulse received during the next prior time interval and that rectifier circuitry and a clamping pulse are employed to effect complete isolation between input and output circuits simultaneously operable.

It is understood that any suitable delay circuit may be employed by the invention and that the various voltage values were given merely to facilitate the description and understanding of the circuit operation. Also, the particular values of the circuit components used will vary in accordance with the particular operation the delay circuit is required to perform.

FIG. 2B shows the circuit of FIG. 2 in block diagram form. Hereinafter, where a delay circuit is shown in block diagram form it is so designated and the terminals necessary to an understanding thereof are shown and designated as in FIG. 2.

FIG. 3 shows an AND circuit typical of the type employed by the invention. The resistor R connected between the juncture J and the source of positive voltage B+ tends to pull the juncture J up to the positive voltage value B+. The plates of the diode rectifiers 95 and 96 are connected to juncture J and the cathodes of these rectifiers are connected to the respective input terminals. Hence, the voltage at J can be no higher than the lower of the two voltages at the input terminals. The voltage at J will change only if the increased voltage is present at the more negative of the two input terminals. In such case, the voltage at J will rise until it reaches this increased voltage value. It is seen, therefore, that when both of the input terminals are Up, J and consequently the output terminal connected thereto are Up. Obviously, additional diodes may be connected between corresponding input terminals and the juncture J and the juncture will be Up only when all input terminals are Up.

FIG. 4 shows an OR circuit using diode rectifiers 97 and 98. The resistor R connected between the juncture J1 and a source of negative voltage B— tends to pull down the voltage at J1 to a value equal to that of B—. The cathodes of the diodes are connected to juncture 1 and the plates of these diodes are connected to respective input terminals. Hence, the voltage at J1 can be no

lower than the higher of the voltages at the input terminals. The voltage at J1 increases in accordance with the more positive voltage at the input terminals. Hence, when either of the input terminals is Up the terminal J1 and consequently the output terminal connected thereto is Up. Obviously, additional diodes may be connected between corresponding input terminals and the juncture J1 and the juncture will be Up when any one or more of the input terminals are Up.

Binary adder

Referring more particularly to FIG. 5 the circuit shown effects addition in true binary fashion and is therefore termed a binary adder. The presence of a pulse at one of the input terminals 13, 14 and 17 indicates the presence of binary 1 and the absence of a pulse thereat indicates a binary 0. Hence, to effect addition in true binary fashion the output must exhibit a binary 0 when no input pulse is applied to the input terminals 13, 14 and 17, a binary 1 when an input pulse is applied to one input terminal, a binary 0 and a binary 1 carry when pulses are applied to two input terminals, and a binary 1 and a binary 1 carry when pulses are applied to all three input terminals. These functions are performed by the circuitry shown.

Diode rectifiers 100 and 101 have their cathodes connected to the input terminals 13 and 14, respectively, and their plates commonly connected at juncture 102 which is connected through a pull up resistor 103 to the +150 volt line 66. The rectifiers 100 and 101 and the resistor 103 comprise an AND circuit 106*a*. When the input terminals 13 and 14 are Up the juncture 102 is Up. Similarly, the diode rectifiers 107 and 108 are connected between the input terminals 14 and 17 and the common juncture 109 is connected through pull up resistor 110 to the +150 volt line 66. The diode rectifiers 107 and 108 and the pull up resistor 110 comprise an AND circuit designated as 111*a*.

The diode rectifiers 113 and 114 are connected between the input terminals 13 and 17 and their common juncture 115 is connected through pull up resistor 116 to the +150 volt line 66. The rectifiers 113 and 114 and pull up resistor 116 comprise an AND circuit 117*a*. The respective junctures 102, 109 and 115 are connected through the parasitic suppressor resistors *ps* to the control grid of the tubes 120, 121 and 122, respectively. The plate of each of these tubes is connected to the +150 volt line 66 and their cathodes are commonly connected through a dropping resistor 124 and a load resistor 125 to the —150 volt line 130. The resistor 125 is a common load resistor for each of the cathode follower tubes 120, 121 and 122 and the dropping resistor 124 is provided to compensate for the cathode follower bias and thereby keep the cathodes of those tubes at approximately the same voltage as the most positive of their control grids. Since the cathodes of the tubes 120, 121 and 122 are commonly connected, the carry output terminal 16—1 is Up when one or more of the grids of the tubes 120, 121 and 122 are Up. These tubes 120, 121 and 122 therefore comprise a cathode follower type OR circuit. If any two of the input terminals 13, 14 and 17 are Up the corresponding AND circuit is rendered effective to cause the carry output terminal 16—1 to go Up. For example, if the input terminals 13 and 14 go Up, the juncture 102 of AND circuit 106*a* goes Up, the control grid of the tube 120 connected thereto goes Up, the cathode of tube 120 goes Up and the carry output terminal 16—1 goes Up. Also, if all three of the input terminals 13, 14 and 17 go Up, the junctures 102, 109 and 115 of AND circuit 106*a*, 111*a* and 117*a*, respectively, all go Up. The control grids of cathode follower tubes 120, 121 and 122 all go Up and carry output terminal 16—1 goes Up. Hence, if an input is present at two or three of the input terminals 13, 14 and 17 a carry output is provided. This complies with the rules of binary addition.

The carry output terminal 16—1 is also connected through a parasitic suppressor resistor *ps* to the control grid of inverter tube 131 having a grounded cathode and its plate connected through load resistor 132 to the +150 volt line 66. The plate of inverter tube 131 is also connected through a voltage divider comprising resistors 133 and 134 to the —150 volt line 130. A frequency compensating condenser 135 is connected, in parallel, with the resistor 133 and the juncture of resistors 133 and 134 is connected through a parasitic suppressor resistor *ps* to the control grid of the cathode follower tube 136 having its cathode connected through a load resistor 137 to the —150 volt line 130 and its plate connected to the +150 volt line 66. The control grid of the inverter tube 131 is connected to the carry output terminal 16—1 and is therefore Up when two or three of the input terminals 13, 14 and 17 are Up. It follows that the plate of the inverter tube 131 is Up when one of the input terminals 13, 14 and 17 is Up and when none of those terminals is Up. The cathode of the cathode follower tube 136 follows its grid and is therefore Up when one input is present or when no input is present.

The cathodes of diode rectifiers 140, 141 and 142 are connected to the input terminals 13, 14 and 17, respectively, and their plates connected to a common juncture 143 which is connected through a pull up resistor 144 to the +150 volt line 66. Rectifiers 140, 141 and 142 and pull up resistor 144 comprise an AND circuit 145*a*. The juncture 143 of AND circuit 145*a* is connected through parasitic suppressor resistor *ps* to the control grid of the cathode follower tube 147 having its plate connected to the +150 volt line 66.

The diode rectifiers 148, 149 and 150 have their plates connected to the input terminals 13, 14 and 17, respectively and their cathodes connected to a common juncture 151 which is connected through a pull down resistor 152 to the —150 volt line 130. The rectifiers 148, 149 and 150 and resistor 152 comprise an OR circuit 153. The juncture 151 or the output of OR circuit 153 is connected to the cathode of diode 154 having its plate connected through pull up resistor 155 to the +150 volt line 66 and through parasitic suppressor resistor 119 to the control grid of cathode follower tube 156.

Diode rectifier 158 has its plate connected to the plate of rectifier 154 and its cathode connected to the cathode of cathode follower tube 136. Diode rectifiers 154 and 158 and pull up resistor 155 comprise an AND circuit 159*a*.

The cathodes of cathode follower tubes 147 and 156 effectively comprise an OR circuit since they are commonly connected through a dropping resistor 160 and a load resistor 161 to the —150 volt line 130. The juncture at resistor 160 and 161 is connected to output terminal 15—1.

The juncture 143 of AND circuit 145*a* is Up only when all three of the input terminals 13, 14 and 17 are Up; i.e., only when three inputs are applied. As a result the control grid of cathode follower tube 147 goes Up and its cathode follows to cause the output terminal 15—1 to go Up when three inputs are present. The juncture 151 of OR circuit 153 goes Up when one or more of input terminals 13, 14 and 17 go Up. The cathode of cathode follower tube 136 goes Up when one input or no input is present. Hence, the juncture 163 of AND circuit 159*a* goes Up only when one of the input terminals 13, 14 and 17 is Up. When the juncture 163 of AND circuit 159*a* goes Up the grid and cathode of cathode follower tube 156 go Up and the output terminal 15—1 goes Up. Hence, output terminal 15—1 goes Up when one or three inputs are applied to the input terminals 13, 14 and 17.

Clamping and synchronous pulse source

The source for producing these pulses will be described in connection with the block diagram showings of FIGS. 6A and 6B and the idealized waveforms shown in FIG.

6C. The circuits actually employed are conventional and do not constitute part of this invention. The actual details of the individual circuits are therefore not shown.

The master timing pulse generator (FIG. 6A) comprises a one megacycle per second sine wave oscillator 180, phase shift device 181 and blocking oscillators 182 and 183. The phase shift circuit 181 causes a phase shift of the output of oscillator 180, so that the positive peak of the output of the phase shift circuit 181 is one-third of a microsecond removed in time from the corresponding positive peak of the output of oscillator 180. This phase shift is indicated in FIG. 6. The output of the oscillator 180 is applied to blocking oscillator 182 and the output of phase shift circuit 181 is applied to blocking oscillator 183 to produce the clamp timing pulse and synchronous (sync) timing pulse, respectively, as shown in FIG. 6. These pulses are produced in coincidence with the positive peaks of the corresponding input waveforms. The clamp timing pulse serves as the input of blocking oscillator 184 to produce a similar pulse of slightly greater amplitude and the sync timing pulse is applied to blocking oscillator 185 to produce a similar pulse of slightly greater amplitude. The output from blocking oscillators 184 and 185 is supplied to the clamp and sync signal generator to produce the clamp and sync signals shown in FIG. 1C.

The output of blocking oscillator 184 serves as the input of blocking oscillators 190 and 191 to produce the clamp signal and sync end pulse. The sync end pulse produced by blocking oscillator 191 is supplied to the pulse stretcher 192 which is energized by the output of blocking oscillator 185 and de-energized by the sync end pulse to produce the sync signal (FIG. 1C). This sync signal is then fed to a cathode follower 193. The clamp signals from blocking oscillator 190 and sync signals from cathode follower 193 are present at the terminals CS and SS, respectively, (FIG. 6B). The clamp signal supplies the input to a clamp inverter 194 and the sync signal provides the input to a sync inverter 195 to produce the clamp pulse and sync pulse, respectively, at the outputs of those inverters. The clamp pulse may be connected to the terminal 62 of a delay circuit such as shown in FIG. 2B and the sync pulse may be connected to the terminal 69 thereof. The clamp and sync inverters are each sufficient to supply approximately five such delay circuits without overloading. It is to prevent overloading that the blocking oscillators are employed as shown.

The broken horizontal lines in FIGS. 6A and 6B indicate that a repetition of the circuitry shown is omitted. For example, the output of a single master timing pulse generator may be connected to six or more blocking oscillators 184 and to six or more blocking oscillators 185. These blocking oscillators may supply forty clamp and sync signal generators and these forty clamp and sync signal generators may supply a total of four hundred clamp inverters and four hundred sync inverters. Hence, a single master timing pulse generator may be used to supply clamp and sync pulses to two thousand delay circuits.

Regeneration counter

Briefly, the regeneration counter, as shown in FIG. 7A, employs four serially connected delay circuits. The output of the last delay circuit is connected to the input of the first through a binary adder which receives the input or counter advance pulses. This coupling between the last and first delay circuits permits continuous storage or regeneration of the amount previously stored in the counter. The output of each delay circuit is utilized to provide a parallel output in the binary-decimal system. This output is read out, during a regeneration cycle, in the serial type plural order counter by means of read out circuits rendered selectively operable by a control circuit. The control circuit renders the read out circuits inoperative during an action cycle and also prevents a counter advance pulse from being applied to the binary adder so that the amount previously stored in the counter is again stored or regenerated.

The output terminal of the carry delay circuit (DCC) and the output of the second delay circuit are connected to an AND circuit to cause the output terminal of that AND circuit to go Up in response to each tenth counter advance pulse applied. The output of this AND circuit is coupled to an input of the binary adder of the next higher order to thus apply a carry input pulse or counter advance pulse thereto. The output of this AND circuit is also coupled to each delay circuit to render all the delay circuits inoperative when a carry pulse occurs, and this causes a clearing from the counter of the amount stored therein.

The regeneration counter may be connected as illustrated in FIGS. 25 and 26 to provide an output when any predetermined number of pulses (1–16 inclusive, as shown herein) are stored therein.

The operation of a single order of the regeneration counter shown in FIG. 7A will be described by conjoint reference to FIGS. 7A, 7B, 7C and 7D.

FIGS. 7C and 7D are arranged as shown in FIG. 7E to form a single chart illustrating the operation of the counter.

FIG. 7A comprises a suitable binary adder such as described in connection with FIG. 5 whose output terminal 15—1 is connected to four series connected delay circuits designated from right to left as DC4, DC2, DC1 and DC8. The output terminals 26 of these respective delay circuits are connected to the terminals D4, D2, D1 and D8. The output terminal 26 of delay circuit DC8 is also connected to the input terminal 14 of the binary adder. The carry output terminal 16—1 of the binary adder is connected to the input terminal of the delay circuit DCC whose output terminal 26 is connected to the input terminal 13 of the binary adder to apply the carry output of the adder to the input thereof during the next time interval.

The clamp pulses and sync pulses are applied to the terminals 62 and 69, respectively, of the delay circuits to effect the operation thereof described in connection with FIGS. 2 and 2A. These clamp and sync pulses at the terminals CP and SP, respectively, are supplied by the clamp and sync inverter having input terminals CS and SSC. The terminal CS corresponds to the terminal CS of FIG. 6B. This clamp and sync inverter may be of any conventional type such as shown in FIG. 7B and briefly described hereinafter.

At time 0.00 (FIGS. 7C and 7D), the counter is in the initial or starting condition as indicated by the 0 (absence of a pulse at the circuit points shown). At time 0.10 an input or counter advance pulse is applied to the input terminal 17 of the binary adder as indicated by the presence of a 1 in FIG. 7C. Since no other input is applied to the binary adder at time 0.10 a single output pulse appears at output terminal 15—1 substantially simultaneous with the application of the input to input terminal 17. During the next following time interval (0.20) the pulse at output terminal 15—1 of the binary adder effects operation of the delay circuit DC4 as described in connection with FIGS. 2 and 2A and a pulse appears at the terminal D4 connected to the output terminal 26 of delay circuit DC4 and the input terminal 24 of delay circuit DC2. Hence, at time 0.20 the only pulse present in the regeneration counter is that present at terminal D4. At time 0.30 this pulse effects operation of delay circuit DC2 and appears at the output terminal D2. During time 0.40 this pulse effects operation of delay circuit DC1 and appears at the terminal D1.

During time 0.50 this pulse effects operation of delay circuit DC8 and a pulse appears at terminal D8. This same pulse is transferred from the terminal D8 to the input terminal 14 of the binary adder and again causes a pulse to appear at the output terminal 15—1 of the binary adder. During time 0.60 delay circuit DC4 is again rendered operable and a pulse appears at terminal

D4. Similarly, at time 0.70 a pulse appears at terminal D2 and at time 1.00 a pulse appears at terminal D1.

It is seen that if no further input is applied to the input terminal 17 of the binary adder that a continuous and repetitious operation of the counter will be effected in the manner described above. This continuous and repetitious operation is utilized to effect counting. At one preselected time interval during each cyclic operation of the counter, the terminals D1, D2, D4 and D8 are examined for the presence or absence of a pulse. The first time during which such an examination is made is time 1.00. As stated above, a pulse is present during this time at the terminal D1 and this pulse is assigned the decimal value 1. During the next following time or the time 1.10 an input pulse to be counted is applied to the input terminal 17. Also, during the time interval 1.10 a pulse appears at the terminal D8 as a result of the pulse present at the terminal D1 during the time 1.00. The pulse at the terminal D8 is applied to the input terminal 14 of the binary adder. Hence, inputs are applied to the terminals 14 and 17 of the binary adder. As a result, the output terminal 15—1 of the binary adder does not exhibit a pulse and a pulse appears at the carry terminal 16—1 of the binary adder.

During time 1.20 the pulse previously at the carry terminal 16—1 of the binary adder causes operation of the carry delay circuit DCC to apply a pulse to the input terminal 13 of the binary adder. This pulse at the input terminal 13 causes a pulse to appear at the output terminal 15—1 of the adder. At the times 1.30, 1.40 and 1.50, a pulse appears at the respective terminals D4, D2, and D1. At time 1.60 the pulse appears at terminal D8 and is transferred therefrom to the input terminal 14 of the binary adder to cause a pulse to appear at the output terminal 15—1 of the adder.

At time 1.70 a pulse is caused to appear at terminal D4 and at time 2.00 a pulse appears at the terminal D2. Also, at time 2.00 the terminals D4, D2, D1 and D8 are again examined. Hence, the pulse read out from the terminal D2 represents a decimal value of 2.

At time 2.10 a pulse is present at the terminal D1 and an input pulse is applied to the terminal 17 of the binary adder. The pulse applied to terminal 17 causes a pulse to be produced at the output terminal 15—1 of the adder. At time 2.20 a pulse appears at the terminal D8 and input terminal 14 of the binary adder. The pulse applied to the input terminal 14 of the binary adder causes a pulse to appear at its output terminal 15—1. Also, the pulse present at the terminal 15—1 during time 2.10 causes a pulse to appear at terminal D4 during this time 2.20.

Similar pulse transfer operation within the counter is continued until time 3.00. At this time terminals D4, D2, D1 and D8 are again examined and pulses found to appear at terminals D1 and D2. The read out of pulses from these terminals corresponds to a decimal value of 3.

At times 3.10 an input pulse is again applied to the input terminal 17 of the binary adder. Pulse transfer operation is continued in the manner set forth above and read out is effected from the terminal D4 at time 4.00. The read out of a pulse from the terminal D4 corresponds to read out of a decimal value of 4.

A similar operation is continued with read out being effected during each successive eighth time interval, an input being applied to the input terminal 17 of the binary adder during the next time interval following read out until an input is applied to the terminal 17 at time 9.10.

It is seen that a decimal 5 is read out at time 5.00, a decimal 6 is read out at time 6.00, a decimal 7 is read out at time 7.00, a decimal 8 is read out at time 8.00 and a decimal 9 is read out at time 9.00. An examination of the pulses present at the terminals D4, D2, D1 and D8 of FIG. 7A indicates that the numeric suffix of the terminal designation corresponds to the decimal read out therefrom. For example, at time 6.00 a decimal 6 is read out as a result of the pulses present at the terminals D2 and D4 and at time 9.00 a decimal 9 is read out as a result of the pulses present at terminals D1 and D8.

At time 9.20 a pulse appears at the input terminal 13 of the binary adder as a result of the pulse present at the output terminal 16—1 thereof at the time 9.10. This same pulse also appears at the input 200 of the two input AND circuit 201*a*. A pulse appears at the terminal D2 as a result of the pulse present at the terminal D4 at time 9.10. The pulse present at the terminal D2 is also present at the input terminal 202 of AND circuit 201*a*. Since pulses are present at the input terminals 200 and 202 of AND circuit 201*a*, both these inputs are Up and the output terminal 203 threof is also Up. This terminal is connected to the terminal designated D10 and provides a pulse which may be used as a carry output pulse to the next higher order which, in this particular example, would necessarily be the tens order.

It is seen from an examination of FIGS. 7C and 7D that the terminals D2 and 13 have a pulse present thereat simultaneously at no time prior to time 9.20. Hence, the input terminals 200 and 202 of AND circuit 201*a* are simultaneously in the Up condition for the first time during the counter's operation and a carry output is therefore provided only at time 9.20.

Clearing a counter order

The counter is cleared or reset to the zero or starting position only prior to starting or when testing and not during any normal operation. To effect clearing a positive sync pulse (FIGS. 2A and 6C) is prevented from arriving at the delay circuits DC1–DC8 and DCC. In accordance with the description of the delay circuit of FIG. 2 this prevents operation of the delay circuits and the amounts or pulses stored in the counter are therefore lost.

In addition to the carry output being made available at terminal D10 to be used as an input to the next higher order of the counter, it is also used to effect automatic resetting of the order from which it is derived. The output terminal 203 of AND circuit 201*a* also serves as an input terminal of the three-input OR circuit 206. The AND circuit 201*a* and OR circuit 206 are referred to herein as the clear and carry circuit. The output terminal 207 of OR circuit 206 is connected to input terminal SSC of the clamp and sync inverter. This unit contains inverters corresponding to the inverters 194 and 195 shown in FIG. 6B. The two input terminals SSC and CS receive the sync and clamp signals respectively and invert them to provide positive sync pulses and negative clamp pulses at the respective output terminals SP and CP of the inverter. The terminals SP and CP are connected to the terminals 62 and 69, respectively, of the delay circuits.

The OR circuit 206 is provided as a means for preventing the arrival of a positive sync pulse at the delay circuits and thereby effect clearing from the counter of the amount of pulses stored therein. This sync pulse is effectively prevented from arriving at the delay circuits or is deleted by preventing it from going positive during a particular time interval. The output terminal 207 of OR circuit 206 is as positive as the most positive voltage applied to its input terminals. Hence, if the output terminal of AND circuit 201*a* is Down and the clear pulse input terminal 208 is Down, the sync signal applied to the remaining input terminal of OR circuit 206 causes a negative sync signal to be transferred to the input terminal SSC of the clamp and sync inverter. A positive sync pulse is therefore transferred from the output terminal SP of the inverter to the terminal 69 of the delay circuits DC1–DC8 and DCC. At time 9.20 the carry output pulse present at terminal 203 is more positive than the sync signal applied to the input of OR circuit 206. As a result of this carry pulse the output terminal 207 of OR circuit 206 is Up, the input terminal SSC of the clamp

and sync inverter is Up, and the output terminal SP of the clamp and sync inverter is Down. The fact that terminal SP is Down prevents operation of the delay circuits and effects a clearing of the pulses present in the counter.

When it is desired to insure that the counter will be set at the 0 position prior to starting operation, a positive clear pulse is applied from any appropriate source (not shown) to the clear pulse input terminal **208**. As in the case of the positive carry pulse applied to an input OR circuit **206**, this positive clear pulse produces a negative pulse at the output terminal SP of the clamp and sync inverter and causes any pulses which may be present in the counter to be lost. Hence, it is seen that when either a positive clear or carry pulse is applied to an input of OR circuit **206** the negative sync signal applied thereto is rendered ineffective to thereby delete the sync pulse which would otherwise be present at the output terminal SP of the clamp and sync inverter.

Referring more particularly to FIG. 7B details of the clamp and sync inverter unit are shown including, a particular circuit arrangement suitable for use as the sync inverter which is indicated as **194** and a similar circuit arrangement suitable for use as the clamp inverter which is designated as **195**. Since each of these circuit arrangements is similar to the other, description will be confined to the circuit **194**. The input terminal SSC is connected through a condenser C and a parasitic suppressor resistor *ps* to the control grid of the tube **210**. This control grid and the cathode of the tube **210** are connected through appropriate bias resistors to the −150 volt terminal **130**. conventional by-pass condensers *bp* are provided as shown. The plate of the tube **210** is connected through load resistors to ground and to the +150 volt line **66**. The plate of the tube **210** is connected to the output terminal SP. Hence, the input pulse applied to the input terminal SSC connected to the control grid is 180° out of phase with the pulse produced at the output terminal SP connected to the plate of that tube.

Counter operation

The four counter orders as used herein will now be described with reference to the circuit diagram formed by placing FIGS. 8A, 8B, 8C and 8D as indicated in FIG. 8E and the chart formed by placing FIGS. 7C, 7D, 9A, 9B and 9C as indicated by FIG. 10. Briefly, the counter comprises the units order, the tens order, the hundreds order and the thousands order connected to the corresponding address switch units SU1, SU10, SU100 and SU1000, respectively. Clear and carry units (FIGS. 8C and 8D) correspond to the respective orders of the counter.

A positive input or counter advance pulse is applied to terminal CA (FIG. 8A) at time N.10 to N.20 and a positive read out pulse is applied to the terminal RO (FIG. 8A) at time N.00 to N.10 during each cycle. The action-regeneration terminal AR (FIG. 8A) is continuously Up during a regeneration cycle and is continuously Down during an action cycle.

The switch units SU1, SU10, SU100, and SU1000 are similar and detailed description will be undertaken with reference to switch unit SU1 (FIG. 8A). The switch unit SU1 comprises four separate switches designated SD1, SD2, SD4 and SD8, respectively, the numeral indicating the decimal weight of the binary digit to which each switch corresponds. The actual structure of each switch is similar to the other. The diodes **215** and **216** and the pull up resistor **217** connected between the juncture of the plates of the diodes and the +150 volt line **66** comprise an AND circuit. The cathode of diode **216** is connected to the terminal D1 of the units order of the counter and the cathode of diode **215** is connected to the regeneration line R. Hence, when the line R and the terminal D1 are both Up the juncture of the diodes and the plate of diode **218** connected to that juncture are also Up. This causes the control grid and cathode of the cathode follower tube **219** and the action-regeneration output terminal AR1 connected to that cathode to go Up.

Similarly, when the terminal D1 and the regeneration line R are both Down, the juncture of diodes **215** and **216** and the plate of diode **218** are Down. As a result the action-regeneration output terminal AR1 is Down. Diodes 215A, 216A, 218A and pull up resistor 217A are similarly connected between the control grid of cathode follower tube **219**, the action line A and the action cycle address terminal A1 so that when the action line A and the terminal A1 are both Up the action-regeneration output terminal AR1 is also Up. The action cycle address terminal A1 is Up when the action cycle address includes a value corresponding to the 1 bit of the units order of a binary-decimal digit.

The clear and carry circuits for each order of the counter (FIGS. 8C and 8D) are similar. Referring to the clear and carry (units) (FIG. 8C), the circuit detail of AND circuit **201***a* and OR circuit **206** of FIG. 7A are shown. AND circuit **206***a* comprises two diodes **221** and **222** having their cathodes connected respectively to terminals **200** and **202** and the common juncture of their plates connected through pull up resistor **223** to the +150 volt line **66** and through a parasitic suppressor resistor *ps* to the grid of the cathode follower tube **224**. The output terminal **203** connected to the cathode of tube **224** is also connected to terminal D10 and to the input terminal **17** of the binary adder of the tens order. Hence, when terminals **200** and **202** are both Up carry is effected from the units order to cause the terminal D10 and the terminal **17** of the binary adder of the tens order to go Up and thereby apply an input to the tens order in response to the carry from the units order.

The three-input OR circuit **206** comprises diodes **225**, **226** and **227** having their cathodes commonly connected through pull down resistor **228** to the −82 volt line **74** and through parasitic suppressor resistor *ps* to the cathode follower tube **229**. The plate of diode **227** is connected to the terminal SS (FIG. 8A) to which a sync signal is applied during each time interval. This causes the control grid of the cathode follower tube **229** and the terminal **207** connected to the cathode of that tube to go Up and thereby apply a sync signal to the terminal SSC of the clamp and sync inverter of the units order.

When the presence of carry from the units order causes the cathode of cathode follower tube **224** to go Up the plate of diode **225** connected thereto also goes Up. This causes the control grid and cathode of cathode follower tube **229** to go Up. The terminal **207** connected to the cathode of tube **229** also goes Up and causes the terminal SSC of the clamp and sync inverter of the units order to go Up and effects clearing of the units order in a manner described in connection with FIG. 7A. The plate of diode **226** is connected to clear terminal **208** (FIG. 8A) and when the clear terminal is Up the terminal **207** is Up and the terminal SSC is Up to effect a clearing of the units order of the counter.

It will be noted that the plate of each of the diodes **226** of the OR circuit **206** of the clear and carry circuits for each order of the counter are commonly connected and that the plates of the diodes **227** are also commonly connected. This means that a sync and clear pulse may effect a clearing of all orders of the counter and that a sync signal is applied from the terminal SS (FIG. 8A) simultaneously to the clear and carry unit for each order.

As stated the action-regeneration terminal terminal AR is Up during a regeneration cycle and is Down during an action cycle.

Circuit operation during a regeneration cycle will now be described. When the terminal AR goes Up the control grid of inverter tube **231L** goes Up and its plate goes Down. A decreased voltage is therefore transferred from the plate of the tube **231L** through the resistor and condenser in parallel and the parasitic suppressor resistor to

the control grid of the cathode follower tube 231R. This causes the cathode of tube 231R to go Down and the cathode of diode 232 connected thereto to go Down. The diodes 232 and 233 and the pull up resistor 234 connected between the juncture of the plates of the diodes and the +150 volt line 66 comprise an AND circuit.

It is seen that when the terminal RO is Up from time N.00 to N.10 during a regeneration cycle that the control grid and cathode of cathode follower tube 236L will be Down since the cathode of diode 232 is Down. The action line A connecting from the cathode of tube 236L to the control grids of the tubes of the heavy duty cathode follower 238 is Down and the action line A connected from cathode follower 238 to the address switch units SU1, SU10, SU100 and SU1000 is Down. Hence, an input applied to the terminals A1–A8000 will not produce an output at the action-regeneration output terminals AR1–AR8000 of the switch.

The output of the action-regeneration terminal AR is also connected to the cathodes of the diodes 240 and 241 having their plates connected respectively to the control grids of the cathode follower tubes 236R and 242. The plate of diode 240 is also connected to the plate of diode 243 and through pull up resistor 244 to the +150 volt line 66. The cathode of diode 243 is connected to read out terminal RO. Hence, diodes 240 and 243 and resistor 244 comprise an AND circuit. Since the cathode of diode 240 is Up during an entire regeneration cycle the control grid and cathode of tube 236R will be Up during a regeneration cycle when a read out pulse is applied to terminal RO from time N.00 to time N.10. Since the cathode of tube 242 is Up, the regeneration line R connected thereto and to the control grids of the tubes of the heavy duty cathode follower tube 246 is Up. Likewise, the cathodes of the tube of the cathode follower 246 and the regeneration line R connected thereto are Up. Since this regeneration line connects to the cathode of the rectifier 215 of each of the switches in the switch units SU1, SU10, SU100 and SU1000 the action-regeneration output terminals AR1-AR8000 will be Up from N.00 to N.10 of each regeneration cycle.

During an action cycle the action-regeneration terminal AR is Down. The negative voltage applied to the control grid of the tube 231L from the terminal AR causes that tube to become non-conductive, and the negative voltage applied to the cathodes of rectifiers 240 and 241 prevents conduction of tubes 236R and 242 in response to positive voltages applied to the read out terminal RO and the counter advance terminal CA, respectively. The cathode of tube 236R is therefore Down and the regeneration line R is Down.

When tube 231L is rendered non-conductive the resulting increased plate voltage is transferred through the resistor and capacitor in parallel to the control grid of tube 231R. This causes the voltage at the cathode of tube 231R to go Up and the cathode of rectifier 232 connected thereto to go Up. Accordingly, when a positive read out pulse is applied to terminal RO from time N.00 to N.10 the control grid and cathode of tube 236L go Up. Accordingly, the action line A goes Up and the cathode of each rectifier 215A of the switch units SU1, SU10, SU100 and SU1000 go Up. It is seen, therefore, that if during the time N.00 to N.10 of an action cycle any one of the terminals A1–A8000 is Up that the corresponding action regeneration output terminal AR1–AR8000 will go Up.

Counter advance pulses are applied to the counter advance pulse terminal CA from time N.10 to N.20. During a regeneration cycle the counter advances or effects additional storage in response to the counter advance pulse. During the action cycle the counter merely retains the amount already stored therein and the counter advance pulse is rendered ineffective because terminal AR (FIG. 8A) is Down.

The voltages applied to the action-regeneration terminal AR, the read out terminal RO, the counter advance terminal CA and terminals A1–A8000 may be derived from any suitable source. For example, the read out pulse and counter advance pulse may be derived from terminals 280 and 281, respectively, of the octal counter shown in FIG. 12 and described hereinafter.

When a counter advance pulse is applied to terminal CA the cathode of rectifier 247 goes Up. The plate of this rectifier is connected to the plate of rectifier 241, through pull up resistor 248 to the +150 volt line 66 and through parasitic suppressor resistor *ps* to the control grid of cathode follower tube 242. Rectifiers 241 and 247 and pull up resistor 248 comprise an AND circuit. The control grid of tube 242 is therefore Up when a counter advance pulse is applied to the terminal CA because the cathode of rectifier 241 is also Up as a result of terminal AR being Up. The cathode of tube 242 is therefore Up and the input terminal 17 of the binary adder for the units order connected thereto is also Up. Hence, an input is applied to the units order of the counter each time a counter advance pulse is applied to the terminal CA providing the action-regeneration terminal AR is Up.

A complete operating cycle of the counter is readily understood by considering FIGS. 7C, 7D, 9A, 9B and 9C arranged as indicated in FIG. 10 in conjunction with the circuit diagram of the counter arranged as indicated in FIG. 8E.

From time 0.00 to 9.20 the units order effects storage as described in connection with FIG. 7A. At time 1.00, for example, the terminal D1 (FIG. 8A) is Up, the regeneration line R is Up and the action-regeneration output terminal AR1 is Up. This indicates that a decimal value of 1 is read out at the counter; all other action-regeneration terminals AR2–AR8000 remain Down. Finally, at time 9.00 the terminals D1 and D8 are Up and action-regeneration output terminals AR1 and AR8 are Up thereby indicating that a decimal 9 has been read out of the counter.

At time 9.20 input terminal 13 of the binary adder of the units order and terminal D2 (FIG. 8A) are Up. These terminals are connected to the input terminals 200 and 202, respectively (FIG. 8C) of the clear and carry circuit for the units order. When terminals 200 and 202 are Up the cathode of cathode follower tube 224 is Up, and the terminal 203 connected thereto is Up. Terminal D10 (FIGS. 8C and 8D) connected to this terminal 203 is also connected to the input terminal 17 of the binary adder of the tens order. When the cathode of tube 224 goes Up, the control grid and cathode of tube 229 goes Up and the terminal 207 connected thereto and to the terminal SSC of the clamp and sync inverter of the units order (FIG. 8) also goes Up. In the manner previously described this effects a clearing of the units order of the counter and this order is again in the condition indicated at time 0.00 (FIG. 7C).

Inputs to the tens, hundreds and thousands orders of the counter are supplied in each instance by the next lower order of the counter only when that lower order effects clear and carry. This is to say that inputs are applied to a higher order only when the lower order completes a cycle of operation. At time 9.2 (FIG. 9A) carry from the units order causes the input terminal 17 and the output terminal 15—10 of the binary adder of the tens order to go Up. During the next time interval, 9.30, delay circuit DC20 is rendered operative and terminal D20 (FIG. 8A) goes Up. This has no effect, however, upon switch unit SU10 because both the action line A and the regeneration line R are Down. Similarly, at time 9.40 the terminal D10 goes Up, at time 9.50 terminal D30 goes Up and at time 9.60 terminal D40 goes Up. As terminal D40 goes Up input terminal 14 of the binary adder of the tens order goes Up and its output 15—10 also goes Up. Accordingly, terminal D20 is Up at 9.70 time. At time 10.00 the terminal D10 is Up, a read out pulse is applied to terminal RO and the action-

regeneration output terminal AR10 goes Up to indicate a reading out of a decimal value of 10.

Circulatory operation of the tens order is continued in a normal manner until time 11.00. At this time output terminal D10 is again Up. Also, output terminal D1 is Up as indicated at time 1.00 of FIG. 7C. Hence, the action regeneration output terminals AR1 and AR10 are Up to indicate a reading out of the decimal value of 11.

This operation is continued with an input pulse being applied to the tens order of the counter each time the units order effects carry and clear. At time 98.00 (FIG. 9A) the terminals D10 and D80 of the units order are Up and the terminal D8 (time 8.00, FIG. 7B) is Up. Circulatory operation of the tens order is continued and at time 99.00 the terminals D10 and D80 are again Up. At time 98.10 a counter advance pulse is applied to terminal CA (time 8.10, FIG. 7B). Normal or circulatory operation of the units order is continued until time 99.00 (time 9.00, FIG. 7D) at which time the terminals D1 and D8 are Up and 9 is read out of the units order. At time 99.10 (time 9.10, FIG. 7B) a counter advance pulse is again applied to the terminal CA and at time 99.20 carry and clear is effected by the units order (time 9.20, FIG. 7D) and an input is applied to the input terminal 17 of the binary adder of the tens order. It is seen that the terminals 14 and 16—10 of the binary adder for the tens order are Up and that terminals D20 and D40 are Up.

During time 99.30 the pulse present at the terminal D20 renders delay circuit DC10 operative and appears at its output which is connected to the terminal D10 (FIG. 8A) and the terminal 202 of the clear and carry circuit (FIG. 8C) of the tens order. Also, the pulse present at the carry terminal 16—10 of the binary adder for the tens order energizes delay circuit DCC of the tens order and causes the input terminal 13 of the binary adder to go Up and also the input terminal 200 of the clear and carry circuit for the tens order to go Up. As a result the tens order is cleared when the terminal D–100 (FIG. 8D) goes Up to apply an input to the input terminal 17 of the binary adder of the hundreds order (FIG. 9B).

Normal operation of the counter continues and at time 100.00 the terminal D–100 (FIG. 8C) is Up, regeneration line R is Up and action-regeneration output terminal AR100 is Up, thereby reading out a decimal value of 100 from the counter. The action-regeneration output terminals associated with the units and tens orders are all Down.

At time 998.00 the output terminals D100 and D800 (FIG. 8C) are Up thereby effecting read-out of the decimal value of 900 from the hundreds order. The terminals D80 and D10 are Up thereby indicating a read-out of the decimal value of 90 from the tens order and the terminal D8 is Up thereby indicating read-out of the decimal value of 8 from the units order.

Similarly, at time 999.00 a decimal value of 999 is read out of the counter. This is indicated by the following terminals being Up: D100, D800, D80, D10, D8 and D1.

At time 999.40 the input terminals 200 and 202 of the clear and carry circuit for the hundreds order are Up. This causes the terminal 207 connected to the clear and carry circuit and terminal D–1000 (FIG. 8D) to go Up. When terminal 207 goes Up, the hundreds order is cleared and the output present at terminal D–100 is applied to the input terminal 17 of the binary adder of the thousands order. Normal counter operation is continued and at time 1000.00 the terminal D–1000 (FIG. 8C) is Up and the decimal value of 1000 is read out.

Counter operation continues as illustrated in FIGS. 7C, 7D, 9A, 9B and 9C. At time 9999.50 the input terminals 200 and 202 of the clear and carry circuit of the thousands order are Up, the output terminal 207 of this circuit is Up and effects a clearing of the thousands order of the counter. The terminal D–10,000 (FIG. 8D) is also Up and may be connected to a subsequent counter order (not shown). The entire counter is now cleared and a cycle of operation has been completed. No further storage is effected until time 0.10 of the next cycle of operation.

It should be noted that clear and carry is effected in each order in the time interval immediately following receipt of an input by that order. Since the carry or output from an order occurs during the time interval next following an input thereto, it is seen that the carry and clear operation of each higher successive order of the counter will be advanced by one time interval. For example, carry and clear occurs in the units order at time 9.20 and carry and clear occurs in the tens order at time 99.30. Obviously, therefore, the last carry and clear operation in the units order will occur at time 9999.20, the tens order at time 9999.30, in the hundreds order at time 9999.40 and in the thousands order at time 9999.50.

Considering the units order the delay circuits DC8, DC1, DC2 and DC4, reading from left to right, represent the decimal digits 8, 1, 2 and 4 respectively. In the tens order, reading from left to right, the delay circuits DC40, DC80, DC10 and DC20 represent the decimal values 40, 80, 10 and 20 respectively. To correspond to the units order these delay circuits should represent the decimal values 80, 10, 20 and 40 respectively. This difference or shift of the delay circuit from the extreme right to the extreme left is caused by the single time interval delay in applying the input to the tens order as compared to the input applied to the units order. Since a similar delay is encountered between the tens and hundreds orders and between the hundreds and thousands orders a similar shift in the designated values of the delay circuits is required.

Pulse stretcher

Referring more particularly to FIG. 11, input terminal AR1 of the pulse stretcher corresponds to the output terminal AR1 of the regeneration counter (FIG. 8A). As pointed out above, the address information or input from the regeneration counter is present only during the time interval N.0–N.1 of an action or regeneration cycle. In order to successfully operate the deflection circuits which control the positioning of the beam of the cathode ray storage tube, it is necessary that address information be present during the entire action or regeneration cycle. The pulse stretcher provides such an address at output terminal S1 by stretching or extending the output received from the terminal AR1 of the regeneration counter over the entire action or regeneration cycle. Hence, when input terminal AR1 is Up from N.0 to N.1 the output terminal S1 is Up for that entire cycle.

The pulse stretcher in FIG. 11 will be described by conjoint reference to FIGS. 11 and 11A and includes a two input AND circuit 260*a*, an inverter tube 261, pull down diode 262, pull up diode 263 and cathode follower tube 264, and circuits associated therewith. The cathode of inverter tube 261 is connected through the self biased resistor 265 and by-pass condenser 266 to ground. The cathode of cathode follower tube 264 is connected through a load resistor to the —82 volt terminal 74 and to output terminal S1. The plate of tube 263 is connected through pull up resistor 267 to a terminal 268 (FIGS. 11 and 13) to which a positive pull up pulse (FIG. 11A) is applied at time N.06–N.08. The plate of inverter 261 is connected through load resistor 269 to the decoupling resistor 270 and decoupling capacitor 271 connected to the +150 volt terminal 66 and to ground, respectively. The resistor 270, resistor 273, crystal diode 274 and resistor 275 comprise a voltage divider connected between +150 volt terminal 66 and ground.

The crystal diode 274 having its plate connected directly to the cathode of pull down diode 262 and through coupling capacitor 276 to the plate of inverter 261 and

provides a higher impedance when the plate of inverter 261 is Down than when that plate is Up. The plate of pull down diode 262 is connected to the cathode of pull up diode 263 and this common connection is connected to ground through a storage condenser 277 and through parasitic suppressor resistor ps to the control grid of cathode follower 264. It is seen that the charge on the storage condenser 277 will determine the conductive condition of the cathode follower tube 264 and that the charge on the condenser is determined by the voltage at the commonly connected cathode and plate of the diodes 263 and 262, respectively.

If an input pulse (FIG. 11A) is applied to the input terminal AR1 of AND circuit 260*a* it will have no effect upon the control grid of tube 261 connected to the output of the AND circuit until a positive sync pulse is applied to the input terminal SP of the AND circuit. This sync pulse occurs approximately at time .06 during each time interval of a cycle (FIG. 2A), and may be obtained from the terminal SP of FIG. 6B. Hence, eight such pulses are supplied during an action or regeneration cycle (FIG. 11A). However, the only sync pulse which can cause operation of AND circuit 260*a* is the one which occurs at time .06 of each cycle since an input pulse may be applied only during the time N.0–N.1.

At time N.06 both an input pulse and a sync pulse are applied to AND circuit 260*a* and the control grid of inverter 261 goes Up. Tube 261 is rendered conductive and its plate goes Down. As a result a negative pulse is applied to the cathode of pull down diode 262 and tends to pull the plate of that diode Down to the voltage of its cathode; for example, say —40 volts. However, the pull up diode 263 and its associated pull up resistor 267 are part of the plate load of pull down diode 262.

As the plate of pull down diode 262 tends to assume the negative value of its cathode, a positive going pull up pulse occurring only at N.06–N.08 time is applied to the terminal 268. As a result, the voltage at the plate of pull up diode 263 is increased and tends to pull its cathode up to a similar voltage; for example, say +50 volts. However, the voltage at the plate of pull down diode 262 overrides the positive voltage at the cathode of pull down diode 263, the storage condenser 277 discharges and its upper plate is placed approximately at —25 volts. The control grid and cathode of tube 264 therefore go Down and the output (FIG. 11A) terminal S1 goes Down and stays Down until the next pull up pulse is applied to terminal 268. This occurs at time .06–.08 of the next cycle. If an input pulse is applied to terminal AR1 during this next cycle the pull up pulse would again be overridden and the output terminal S1 will remain Down. However, if no input pulse is applied to terminal AR1 the pull up pulse causes the upper plate of storage condenser 277 to be placed at a positive voltage equal to the most positive voltage, say +5 volts, attained by the pull up pulse. When the upper plate of storage condenser 277 goes positive cathode follower tube 264 is rendered conductive and its cathode and the output terminal S1 go Up.

The larger the value of pull up resistor 267 the less will be the current required through the pull down resistor 269 to override the pull up pulse applied to terminal 268. However, the upper value of the resistor 267 is limited in that the time constant of resistor 267 and storage condenser 277 must be sufficiently small to permit the storage condenser 277 to be charged by the relatively narrow positive pull up pulse.

A similar pulse stretcher is provided to receive outputs from each of the output terminals AR2-AR8000 of the address switch.

Octal commutator

Referring more particularly to FIG. 12 the octal commutator includes eight delay circuits connected in series. The seven junctures connected to successive delay circuits in the series chain and the output terminal 26 of the last delay circuit in the series chain (extreme right of FIG. 12) are connected to output terminals 280–287 inclusive. The seven junctures of the delay circuits are also connected to a seven-input OR circuit 288 whose output terminal is connected to a cathode follower 289. The output of cathode follower 289 is supplied to an inverter 290 whose output is connected to a cathode follower 291. The output of cathode follower 291 is connected to the input terminal 24 of the first delay circuit in the series chain (extreme left of FIG. 12).

When any one of the seven junctures of the delay circuits is Up, the output of OR circuit 288 is Up, the output of cathode follower 289 is Up, the output of inverter 290 is Down, the output of cathode follower 291 is Down, and the input terminal 24 of the first delay circuit is Down. Hence, no input is applied to the first delay circuit.

However, if all of the junctures of the delay circuits are Down the output of OR circuit 288 is Down, the output of cathode follower 289 is Down, the output of inverter 290 is Up, the output of cathode follower 291 is Up and the input terminal 24 of the first delay circuit is Up. This causes operation of the first delay circuit as described in connection with FIGS. 2 and 2A.

Initially, therefore, when the power is turned on to energize the commutator the input terminal 24 of the first delay circuit is Up. This causes operation of the first delay circuit and causes its output terminal 26 and input terminal 24 of the second delay circuit to go Up. The input to OR circuit 288 connected to this juncture goes Up. The output of OR circuit 288 goes Up and the operation of cathode follower 289 and 291 and inverter 290 as described above causes the input terminal 24 of the first delay circuit to go Down. The output terminal 280 connected to the juncture of the first and second OR circuits also goes Up and provides a positive output pulse. The time of this happening is arbitrarily designated as time N.0.

During the next time interval the second delay circuit is rendered operative to cause the juncture of the second and third delay circuits to go Up, the OR circuit 288 to again be rendered operative and output terminal 281 to go Up. At this time N.1 the output terminal 280 which was Up at time N.0 goes Down and the terminal 281 goes Up. In a similar manner output terminal 282 goes Up at time N.2 and output terminal 281 goes Down, output terminal 283 goes Up at N.3 and output terminal 282 goes Down.

Finally, at time N.7 the output terminal 287 goes Up, all inputs to the OR circuit 288 go Down to cause the input terminal 24 of the first delay circuit to go Up. At this time N.7 an output may be derived from the output terminal 287.

It is deemed clear from the above that any desired number of delay circuits may be connected in series instead of the eight delay circuits shown. For example, four, ten, eighteen, etc. can be connected in series, as demonstrated in FIG. 12, through an OR circuit having a corresponding number of inputs to the input of the first delay circuit to establish a free running commutator having a cycle corresponding to the number of delay circuits employed.

During the next time interval the first delay circuit is rendered operative and causes the output terminal 280 and the associated input to the OR circuit 288 to go Up and thereby cause the input to the first delay circuit to go Down.

During successive time intervals an output pulse appears at the next higher output terminal until the output terminal 287 goes Up and the cycle of commutator operation is again automatically repeated.

It is seen that this commutator is free running and requires no external source of pulses other than those required for operation of delay circuits. During each time interval of an action or regeneration cycle, a single

output pulse is provided. If, for example, a pulse is desired from time N.0 to time N.1 it may be obtained by connecting to the output terminal **280** which provides an output pulse from time N.0 to time N.1 and at no other time. Similarly, output terminal **286** provides an output pulse from time N.6 to time N.7.

If it is desired to provide a plurality of output pulses during each time interval from N.0–N.7, such may be accomplished by using the commutator of FIG. 12 as a master commutator.

Referring more particularly to FIG. 12A, the master commutator is as shown in FIG. 12. The output terminal **26** of the last delay circuit in the series chain of the master commutator is connected to the input terminal **24** of the first delay circuit (extreme left) of two series chains as in each of eight delay circuits and termed slave **1** and slave **2**, respectively. The output terminals of slave **1** are designated **300–307** and produce outputs at times N.0–N.7, respectively. Similarly, the output terminals of slave **2** are designated **310–317** and produce outputs at times N.0–N.7, respectively. The junctures of the delay circuits of slaves **1** and **2** are not connected to any other circuitry. These slaves of the master commutator are under the complete control of the master commutator.

It is seen that an input will not be applied to the first delay circuit of slaves **1** and **2** until the master commutator has completed one cycle of operation. When the master commutator does complete one cycle of operation, the input terminals **24** of the first delay circuit of slaves **1** and **2** go Up. At this same time the input terminals **24** of the first delay circuit of the master commutator goes Up. During the next time interval the first delay circuit of the master and slave commutators is operative. At N.0 of the next cycle the output terminals **280**, **300** and **310** go Up to provide three separate pulses between time N.0 and N.1 at each of these output terminals. The slave commutators are now in synchronism and each produces an output corresponding to the output of the master commutator.

It is understood that additional slave commutators may be connected to output **287** just as slaves **1** and **2** and that slave commutators may also be connected to the output terminals **307** and **317** of slaves **1** and **2**, respectively.

If slave commutators are connected in parallel with the output terminal **307** two cycles of operation of the master commutator will be required to synchronize the slaves so connected with the master.

Pull up pulse source

Referring more particularly to FIG. 13 a synchronous pulse (terminal SP, FIG. 6B) is applied to the input terminal **320** of two input AND circuit **321***a* and the input terminal **322** of AND circuit **321***a* is connected to the output terminal **280** of FIG. 12. The amplifier tube **323** is conductive only when the output terminal **324** of AND circuit **321***a* is Up and this output terminal **324** is Up only when pulses are applied simultaneously to the inputs **320** and **322**. A single sync pulse is applied to the input terminal **320** during each time interval of the action and regeneration cycles. However, a pulse is applied to the input terminal **322** only when the output terminal **280** of FIG. 12 is Up or from time N.0 to N.1 of each cycle. Since a sync pulse occurs at time N.06–N.1 the output **324** of AND circuit **321***a* is Up from time N.06 to N.1 of each action and regeneration cycle.

When output terminal **324** is Up, the control grid of amplifier **323** is Up and its plate is Down. This causes transfer of a negative pulse through the coupling condenser **325** to the control grid of tube **326**. This causes the normally conductive tube **326** to be cut off at time N.06 and its plate to rise toward +150 volts to which it is connected through peaking coil **327**. The peaking action of this coil is similar to that obtained by the use of coil **64**, FIG. 2 and causes a positive pulse to be transferred through the coupling condenser **328** to the control grid of cathode follower tube **329**. This pulse causes the cathode of tube **329** and the output terminal **268** connected thereto to go Up.

At time N.1 the control grid of tube **323** goes Down, the plate of tube **323** and the control grid of tube **326** go Up, the plate of tube **326** and the grid of tube **329** go Down, and the cathode of tube **329** follows its control grid and goes Down to cause the output terminal to go Down. Hence, a positive pull up pulse is provided at the terminal **268** from time N.06 to N.1 of each action and regeneration cycle. This terminal **268** is synonymous with the terminal **268** of FIG. 11 and provides a pull up pulse to permit operation of the circuit of FIG. 11 as described above.

Inverters

Referring more particularly to FIG. 14 the input terminal S1 of the inverter corresponds with the output terminal S1 of the pulse stretcher. The input pulse to the terminal S1 is transferred through the limiting resistor **330** to the control grid of the inverter tube **331**. When terminal S1 goes Up the control grid of tube **331** goes Down and its plate goes Up. A positive pulse is transferred from the plate of the tube **331** to the control grid of cathode follower tube **332**. As a result the cathode of cathode follower tube **332** and the output terminal I1 connected thereto go Up.

Likewise, when terminal S1 goes Down, the control grid of tube **331** goes Down and its plate goes Up. This causes the control grid and cathode of tube **332** and the output terminal I1 to go Up. It is seen that when the input terminal I1 is Down and when the input terminal S1 is Down, the output terminal I1 is Up. For example, if the input at terminal S1 represents a decimal 1 the output at terminal I1 represents an inverted 1.

A similar inverter is connected to the output terminal of each pulse stretcher.

Connection of deflection circuits

The actual connection of the deflection circuits is shown in FIGS. 1A and 1C. However, a complete understanding of these connections is dependent upon the understanding of the actual physical arrangement or display of information stored upon the face of the cathode ray tubes (CRTs).

This display or pattern will be explained in connection with FIGS. 15A, 15B, 15C and 15D. From FIGS. 15A, 15B, 15C and 15D it is seen that the storage areas or positions on the face of each CRT are grouped into ten horizontal areas. Each of these areas includes ten vertical columns of storage areas and five horizontal rows of storage areas, each of these areas therefore includes fifty discrete beam positions or storage areas. Since there are ten such rectangular areas, the face of each cathode ray tube provides a total of 500 discrete beam positions and the CRTs A, B, C and D provide a total of 2000 discrete beam positions. This represents a storage capacity of 2000 bits and provides for the storage of one predetermined binary bit or order of one decimal digit of each word; for example, the lowest binary bit of the units order decimal digit of each of the 2000 words capable of being stored. Hence, the fact that each of the 2,000 beam positions of each CRT unit stores the same binary bit of the same decimal order means that sixty-four CRT units or 256 cathode ray tubes will store 2,000 sixteen decimal digit words. This word size is reduced when certain bits are used for algebraic sign, or for checking, or for other purposes.

The various beam positions are designated on the drawings by circles and are assigned a decimal number corresponding thereto. The upper left position of the upper left rectangular area of FIG. 15A is designated the 0 beam position, the next beam position to the immediate right is the 2 position, next the 4 position—until the 18 position at the extreme right. The extreme left position

on the next lower or second row is the 20 position, next the 22 position, etc. Finally, the last or extreme right position on the fifth row is the 98 position. Hence, this rectangular area includes all even numbered beam positions from 0 to 98 inclusive.

The beam positions within the upper right rectangular area are similarly arranged and include all even numbered positions from 100 to 198 inclusive. The next lower rectangular area on the left includes all even numbered positions from 200–298 inclusive and the area to its right all even numbered positions from 300–398 inclusive.

This system or scheme of designations is applied throughout so that the lowest beam position at the extreme right is position 998. Hence, CRT A provides for all even numbered positions from 0–998 inclusive.

FIG. 15B shows the numbered beam positions for CRT B position 1 corresponding to position 0 in FIG. 15A and position 3 to position 2 in FIG. 15A. This same scheme of designation is applied throughout so that CRT B provides for all odd numbered positions from 1–999 inclusive.

Similarly, FIG. 15C includes the even numbered positions from 1000–1998 inclusive and FIG. 15D includes the odd numbered positions from 1001–1999 inclusive.

If it is desired to refresh or regenerate all the information stored at the 2000 storage positions, the electron beam will be moved in a step-by-step fashion so as to effect the proper tube selection and regenerate the information in proper position sequence. The regeneration of the information at a single position is accomplished during a single regeneration cycle. The sequential regeneration of the information at all of the 2000 positions is accomplished during 2000 sequential regeneration cycles referred to herein as a complete regeneration cycle.

The actual voltages supplied to produce electron beam deflections to the address indicated in FIGS. 15A, 15B, 15C and 15D are represented by the chart of FIG. 16 and shown graphically in FIGS. 17 and 18.

In FIG. 16 the units, tens, hundreds and thousands orders represent the corresponding decimal orders and the binary representations, when reading from right to left, in each column represent the binary orders from the lowest to the highest. For example, the 0 in the upper right position of the units order column represents the lowest binary order and the 0 in the upper left of the thousands order represents the highest binary order. The decimal numbers in the extreme right column represent the addresses or beam positions on the face of CRT's A, B, C and D (FIG. 1C). The electron beams are brought to these various positions or addresses in response to voltages representing the binary representations corresponding to those addresses. In FIGS. 17 and 18 the horizontal and vertical deflection weight respectively of certain specified connections to the horizontal and vertical deflection circuits is graphically represented. The deflection weights are represented by the numbers 0–9 inclusive.

In FIG. 17 the horizontal deflection weight of the 4's line is 2. This means that the number 2 represents the relative contribution of the voltage provided by the 4's line in effecting horizontal deflection of the electron beams. In each instance the deflection weight indicates the voltage contribution of the designated line in effecting deflection of the electron beam.

The 2's line of FIG. 17 corresponds to terminal I2 (FIG. 1A) and goes Up when it provides a beam deflecting voltage. Similarly, the 4's line corresponds to terminal I4, the 40's line to terminal I40, etc.

Addresses shown in FIGS. 16, 17 and 18 correspond to those for CRT's A, B, C and D (FIG. 1C) illustrated in FIGS. 15A, 15B, 15C and 15D respectively. The spot positions shown in FIGS. 17 and 18 are numbered to correspond to the number of times the electron beams have actually been shifted or re-positioned to be on the address corresponding thereto. In other words, the spot position indication ignores tube selection. For example, when the electron beams are in spot position 3, the address sought may be either 6 (FIG. 15A), 7 (FIG. 15B), 1006 (FIG. 15C), or 1007 (FIG. 15D), the actual address being determined by the tube selector (FIG. 1A).

The step-by-step sequential positioning of the electron beams shown by FIGS. 16, 17 and 18 is accomplished during a complete regeneration cycle. Initially, the electron beams are in the upper left positions and the tube selector has selected tube A to be operable. At the end of the first regeneration cycle (8 microseconds, FIG. 17), the 1's line goes Up. This is indicated by the presence of a pulse at address 1, FIG. 17, and in the lowest binary order of the units order corresponding to address 1, FIG. 16. This causes the tube selector to select tube B. At the end of the second regeneration cycle 16 microseconds, designated in FIG. 17, the 2's line goes Up and the 1's line goes Down. This causes the electron beam to be shifted to address 2 and tube A to be selected. At this time, regeneration of addresses 0 and 1 have been completed and the electron beams have been shifted one spot position and regeneration of address 2 is begun. Eight microseconds later, the 1's line again goes Up and tube B is selected so that regeneration of address 3 is begun. Eight microseconds later at spot position 2, the 1's line and 2's line go Down and the 4's line goes Up. At this time tube A is selected and regeneration of address 4 is begun. It is seen from the units order total horizontal deflection weight curve that the total weight of the deflection voltage is twice that provided when the 2's line alone is Up. It follows, therefore, that the 2's line going Up causes a deflection of one spot position and the 4's line going Up causes a deflection of 2 spot positions. At address 6, the 2's line again goes Up and its deflection weight voltage of 1 is added to that of the 4's line to provide a total deflection weight of 3. When the 2's line and the 4's line are Up, regeneration of addresses 6 and 7 is effected. Next, the 2's line and the 4's line go Down and the 8's line goes Up. The electron beams are now at spot position 4 and address 8 is selected. The 8's line, therefore, must provide a total deflection weight voltage of 4. When the 1's line next goes Up, regeneration of address 9 is effected.

When the regeneration of address 9 is completed the 8's line goes Down. All lines of the units order are now Down and the units order is in its initial starting position. At this time the 10's line or the lowest binary order of the tens order (FIG. 16) goes Up. When the 10's line goes Up the total horizontal deflection weight voltage which is the units and tens orders total horizontal deflection weight voltage (FIG. 17) causes the electron beams to be shifted to spot position 5 and tube A is selected so that regeneration of address 10 is begun. The 10's line remains Up while the units order repeats its cycle of operation. Hence, the deflection weight voltages provided by the 2's, 4's and 8's lines are added to that of the 10's line to provide the units and tens order total horizontal deflection weight curve shown in FIG. 17. These voltages effect deflection of the beam through the remaining spot positions up to and including 9 and effects regeneration of the addresses through address 19.

When regeneration of address 19 is completed, the units order returns to its initial 0 position and the 10's line goes Down. The horizontal deflection of the electron beams is, therefore, 0 and the addresses 0–19 shown in FIGS. 15A and 15B have been regenerated.

The 20's line (FIG. 18) now goes Up. This is shown by pulse output at the second binary order of tens order in FIG. 16. This 20's line of the tens order is assigned a vertical deflection weight voltage of 1 and is, therefore, connected to the vertical CRT deflection circuits (terminals S20 and I20, FIG. 1A). When the 20's line goes Up this causes a one spot position downward deflection of the beams so that the electron beams are now

positioned at addresses 20, 21, 1020 and 1021. As stated above, the 1's line is now Down so that tube A is selected. Hence, regeneration of address 20 is begun. As previously pointed out the 1's line goes Up at the end of the first 8 microsecond period and the tube B is selected so that regeneration of address 20 is begun. The electron beams remain in this same vertical position until addresses 20–39 inclusive are regenerated. Hence, while the beams are in this vertical position the operation described in connection with FIG. 17 is repeated. At the end of 160 microseconds the 20's line goes Down and the 40's line goes Up. The total vertical deflection weight voltage now applied, which is the 10's order vertical deflection weight voltage, is now twice that just previously applied so that the 40's line is assigned a vertical deflection weight voltage of 2. Regeneration of address 40–59 is now effected in the manner above described.

Subsequently, at the end of another 160 microseconds, the 20's line goes Up to position the beam at spot position 3 (FIG. 18) where it remains in its vertical position until addresses 60–79 are regenerated. During this time both the 20's and 40's lines are Up (FIGS. 16 and 18). The 20's and 40's lines then go Down and the 80's line goes Up to position the beam at spot position 4 to effect regeneration of addresses 80–99.

Addresses 0–99 inclusive have now been regenerated. A total regeneration time of 800 microseconds has elapsed and the 20's, 40's and 80's lines are Down.

The 100's line connected to the horizontal deflection circuits (FIG. 1A) now goes Up. The horizontal deflection voltage supplied by the 100's line is assigned a deflection weight value of 10. This causes the electron beams to be positioned on addresses 100, 101, 1100 and 1101. The above described is now repeated to effect regeneration of addresses 100–199 inclusive. At this time the 100's lines goes Down and the 200's line (FIG. 18) connected to the vertical deflection circuits goes Up. The voltage supplied by the 200's line is assigned a deflection weight value of 5 and causes the electron beams to be positioned at addresses 200, 201, 1200 and 1201. The units and tens orders cycles described above are again repeated to effect a regeneration of addresses 200–299 inclusive. The deflection weights of the 20's, 40's and 100's lines of the tens order are for the first time added to the deflection weight of the 200's line to produce the tens and hundreds order total deflection weight voltages shown in FIG. 18. The units order and tens order return to their 0 positions. The 200's line remains Up and the 100's line goes Up. The vertical deflection voltage applied to the electron beams has a weight of 5 because the 200's line is Up. The horizontal deflection weight voltage value is 10 because the 100's line is Up. Hence, the electron beams are positioned to addresses 300, 301, 1300 and 1301. Addresses 300–399 are now regenerated as described above.

The 100's line and the 200's line then go Down and the 40's line (FIG. 1A) connected to the vertical deflection circuits and supplying a voltage having a vertical deflection weight of 10 goes Up. This causes electron beams to be positioned at addresses 400, 401, 1400 and 1401. The addresses 400–499 are now regenerated as described herein above.

The 100's line then goes Up to cause the electron beams to be positioned to addresses 500, 501, 1500 and 1501. Regeneration of addresses 500–599 is now effected. When this is accomplished, the 100's line goes Down and the 200's line goes Up. The 200's line and the 400's line are now up so that the weight of the total vertical deflection voltage is 15. This causes the electron beams to be positioned at addresses 600, 601, 1600 and 1601. Addresses 600–699 are now regenerated.

The 100's line again goes Up so that the electron beams are positioned to addresses 700, 701, 1700 and 1701. Addresses 700–799 are now regenerated.

The 100's, 200's and 400's lines now go Down. The 800's line (FIG. 1A) connected to the vertical deflection circuits and assigned a vertical deflection weight of 20 goes Up. This causes the electron beams to be positioned at addresses 800, 801, 1800 and 1801. Addresses 800–899 are now regenerated.

The 100's line again goes Up causing the electron beams to be positioned to addresses 900, 901, 1900 and 1901. Addresses 900–999 are now regenerated.

All lines of the units, tens and hundreds orders now go Down and the 1000's line connected to the tube selector goes Up. This means that CRT A and CRT B will no longer be selected and that CRT C and CRT D will be alternately selected in response to the voltage supplied by the 1's line in the same manner that CRT A and CRT B were alternately selected when addresses 0–999 were regenerated. The electron beams are now at addresses 0, 1, 1000 and 1001. The cycle of operation described above is now repeated to effect regeneration of addresses 1000–1999. A complete regeneration cycle is now accomplished. The electron beams are returned to their initial positions.

It is noted that the 2,000's line now goes Up. This is of no consequence, however, since in this embodiment the 2,000 line is not employed.

Deflection circuits

Referring more particularly to FIGS. 19A and 19B the horizontal deflection circuit comprises five switching units designated SW2, SW4, SW8, SW10 and SW100 and stabilizing circuits 350 and 351.

The switching unit SW2 (FIG. 19B) is typical of those employed herein. This switching unit comprises twin triode tubes 352L and 352R connected to operate as cathode followers. The commonly connected cathodes are connected through a load resistor 353 to the —150 volt line 130. The plate of tube 352L is connected directly to line 354 and the plate of tube 352R is connected directly to line 355. The control grids of tubes 352L and 352R are connected through parasitic resistors ps and the resistors 357 and 358, respectively, to the ground line G. These grids are also connected through the parasitic resistors to the plates of diodes 360 and 361, respectively. The cathode of diode 360 is connected to terminal S2 (FIGS. 19A and 1A) and the cathode of diode 361 is connected to terminal I2 (FIGS. 19A and 1A).

Similarly, the cathodes of the diodes 360 and 361 of the switching units SW4, SW8, SW10 and SW100 are connected to the terminals S4, I4; S8, I8; S10, I10; S100 and I100 of FIG. 1A.

Again, consider the switching unit SW2 as exemplary. When a decimal 2 is included in the address the terminal S2 is Down and the terminal I2 is Up. Conversely, when no 2 is included in the address the terminal I2 is Up and the terminal S2 is Down. The condition of the remaining S and I terminals is similarly determined by the presence or absence of the corresponding decimal number. When a 2 is not included in the address, the terminal I2 is Down and the terminal S2 is Up. Since terminal I2 is Down the cathode of diode 361 is Down and the potential difference between the cathode and plate of diode 361 is sufficient to cause conduction therethrough. The plate and the control grid of tube 352R connected thereto then go Down. As a result the control grid of 352R is cut off and tube 352R is rendered non-conductive. At this same time, the diode 360 is cut off because the terminal S2 is Up, the potential difference between the plate and cathode of diode 361 being insufficient to permit conduction. The control grid of tube 352L is therefore placed at the same potential as ground line G and tube 352L is rendered conductive. If a 2 is included in the address the conductive condition of diodes 360 and 361 is reversed, the terminal S2 is Down so that diode 360 is rendered conductive, thereby causing tube 352L to be

rendered non-conductive. The terminal I2 is Up. This causes diode 361 to be cut off and tube 352R is rendered conductive.

Hence, when a 2 is not present in the address all of the current through load resistor 353 passes through tube 352L and when a 2 is included in the address all of the current through load resistor 353 passes through tube 352R.

Stabilizing circuit 350 includes two twin triode tubes 362 and 363. The cathodes of these tubes are commonly connected to the line 355 and the plates are commonly connected through parasitic resistors and a resistor 364 to the +390 volt line 366. The control grids of tubes 362 and 363 are connected through parasitic resistors to a potential point 367, intermediate resistors 368 and 369 connected respectively to the +150 volt terminal 66 and the +390 volt line 366. These control grids are also connected to ground through a decoupling condenser 370*a*.

The tube 352R of the switching units SW2, SW4, SW8, SW10 and SW100 are commonly connected to the cathodes of tubes 362 and 363 of the stabilizing circuit 350. When all the tubes 352R are non-conductive the current path from the +390 volt line 366 through resistor 364, tubes 362 and 363, and tubes 352R to the −150 volt line 130 is interrupted thereby so that the tubes 362 and 363 are rendered non-conductive. However, when one or more of the tubes 352R is conductive, the tubes 362 and 363 are also conductive and a voltage drop occurs across resistor 364 connected between the plates of tubes 362 and 363 and the +390 volt line 366. A signal is therefore exhibited at the terminal HL which is connected to the left horizontal deflection plate of the cathode ray tubes CRT A, CRT B, CRT C and CRT D (FIG. 1C).

The stabilizing circuit 351 is similar to circuit 350 and the resistor 370 is identical with resistor 364. The commonly connected cathodes of tubes 362 and 363 of circuit 351 are commonly connected to the line 354 which joins the plates of the tubes 352L of the switching units SW2, SW4, SW8, SW10 and SW100. As will be understood from the description hereinafter, the stabilizing circuits 350 and 351 stabilize the plate voltages of the tubes 352R and 352L respectively so that those voltages are independent of the total current flowing through the circuits 350 and 351. The stabilizing circuits 350 and 351 serve as the load impedance for the various tubes 352R and 352L respectively. Actually, the stabilizing circuits 350 and 351 cause the voltage changes which would normally appear at the plates of tubes 352R and 352L, respectively, due to the change in current flow, to appear at the terminals HL and HR respectively.

Hence, each stabilizing circuit and the related tubes of the switching units function basically as a cascode amplifier. A cascode amplifier is described at page 440 of "Vacuum Tube Amplifiers," volume 18, first edition, Radiation Laboratory Series, published by McGraw-Hill Book Co., Inc., 1948, and edited by Valley and Wallman. The operation of the tubes 362 and 363 of the stabilizing circuits is comparable to that of cathode followers in that the cathode voltage approximates the control grid voltage, e.g. within 10 volts.

As previously explained, to obtain the address representations or deflection pattern shown in FIGS. 15A, 15B, 15C and 15D, it is necessary that the signal applied to the horizontal deflection plates when a decimal 2 is included in the address have an assigned deflection weight of 1. Similarly, the signal to the horizontal deflection plates when a decimal 4, decimal 8, decimal 10 or decimal 100 is included in the address must have assigned deflection weights of 2, 4, 5 and 10, respectively. This is synonymous with saying, that the currents flowing through resistor 353 of SW2, resistor 372 of SW4, resistor 373 of SW8, resistor 374 of SW10, and resistor 375 of SW100 are related as 1, 2, 4, 5 and 10, respectively. Since these currents must be so related it follows that the value of the resistors must be related in a like manner. Hence, resistor 353 may have a value of 50K (50,000 ohms), resistor 372 of 25K (resistor 373 of 12.5K, resistor 374 of 10K and resistor 375 of 5K.

It is noted that each of the tubes 352L and 352R of switching unit SW100 is a twin triode connected in parallel. Such is necessitated by the high current flow through the 5K resistor 375.

In order for the address representations or deflection patterns shown in FIGS. 15A, 15B, 15C and 15D to be produced it is necessary that equal deflection of the electron beam be provided when it is shifted from any one spot position to the next. The total current flowing through resistors 364 and 370 is always a constant value. In order to shift the electron beam from one spot position to the next, the current flowing through one of the resistors, say 370, is decreased by a predetermined amount; for example 3 milliamperes and the current flowing through resistor 364 is increased by the same amount.

Since a deflection weight value of 1 causes a shift or deflection of the electron beam one spot position a change in current flow of 3 milliamperes may be said to represent a deflection weight of 1. The total or maximum deflection weight is represented by the summation of 1, 2, 4, 5 and 10 or by 22. The total current flowing at all times is therefore 22×3 or 66 milliamperes. When the address is 0, the terminals S2, S4, S8, S10 and S100 are Down. All of the tubes 352L are therefore conductive. It follows that all current flows through the line 354 and resistor 370 (FIG. 19A). The terminal HR is connected to the right horizontal deflection plates of the CRTs A, B, C and D and the electron beams are caused to be in the extreme left position (FIGS. 15A, 15B, 15C and 15D). Hence, the deflection circuits may be said to be in the 0 or initial stable condition.

As stated, when the electron beams are in spot position 0, tubes 352L of the switching units SW2, SW4, SW8 and SW100 are conductive and the total current of 66 milliamperes flows through resistor 370. The actual operation of the horizontal deflection circuits of FIGS. 19A and 19B to obtain the beam deflections indicated in FIGS. 15A, 15B, 15C and 15D is more easily realized by conjoint reference to FIGS. 15A, 15B, 15C and 15D, and FIG. 17.

When the electron beams are to be placed at spot position 1, the terminal S2 goes Down and the terminal I2 goes Up (2's line, FIG. 17). The tube 352R of switching unit SW2 (FIG. 19B) is rendered conductive and the 3 milliamperes of current flowing through this tube 352R also flows through resistor 364 and causes a voltage change which is applied to the lefthand horizontal plates of CRTs A, B, C and D (FIG. 1B). Just prior to the 2's line going Up this 3 milliamperes of current flowed through resistor 370 (FIG. 19C); hence, when the electron beams are in spot position 1, 63 milliamperes of current flows through resistor 370 and 3 milliamperes flows through resistor 364.

When the electron beams are to be placed at spot position 2, the 2's line goes Down and the 4's line goes Up (FIG. 17).

It follows that the tube 352R of switching unit SW2 becomes non-conductive and the tube 352L thereof becomes conductive. This means that the 3 milliamperes flowing through switching unit SW2 is again caused to flow through resistor 370 (FIG. 19A). Also, the tube 352L of switching unit SW4 is rendered non-conductive and tube 352R thereof is rendered conductive. Since the ohmic value of resistor 372 of switching unit SW4 is one half that of resistor 353 of switching unit SW2 a total of 6 milliamperes now flows through tube 352R. This current also flows through the resistor 364 (FIG. 19B). Hence, a total of 60 milliamperes now flows through resistor 370 (FIG. 19A) and a total of 6 milliamperes flows through the resistor 364 (FIG. 19B). The electron beams are now placed at spot position 2.

When the electron beams are to be placed at spot posi-

tion 3 tube 352L of switching unit SW2 becomes non-conductive and the tube 352R thereof becomes conductive. Hence the 3 milliamperes of current flowing through switching unit SW2 is again caused to flow through resistor 364 and is added to the 6 milliamperes of current already flowing through resistor 364 as a result of the conduction of tube 352R of switching unit SU4.

When the electron beams are to be placed at spot position 4, the tubes 352L of switching units SW2 and SW4 again become conductive to cause the 9 milliamperes of current normally flowing through those switching units to again flow through the resistor 370. At this same time, the 8's line (FIG. 17) goes Up and the tube 352L of switching unit SW8 is rendered non-conductive and the tube 352R is rendered conductive. This causes the 12 milliamperes of current flowing through switching unit SW4 to now flow through the resistor 364. This causes the electron beams to be placed at spot position 4.

When the electron beams are to be placed at spot position 5, the 8's line goes Down (FIG. 17) causing the tube 352L of the switching unit SW8 to become conductive and the 12 milliamperes which were flowing through resistor 364 to flow through resistor 370. At the same time, the 10's line (FIG. 17) goes Up and the tube 352L goes Up. The terminal S10 therefore goes Down and the terminal I10 goes Up. The tube 352L is rendered non-conductive and the tube 352R is rendered conductive. The 20 milliamperes of current flowing through switching unit SW10 are now caused to flow through the resistor 364 and the electron beams are at spot position 5. Conduction of tube 352R of switching unit SW10 continues while the operation of switching units SW2, SW4, SW8 is repeated. This causes the electron beams to be placed at the spot positions 6, 7, 8 and 10, respectively.

When the electron beam is to be placed at spot position 10, all of the switching units return to their initial position, the actual positioning to spot position 10 being determined by operation of the vertical deflection circuits described subsequently.

When the electron beams are to be placed at the spot position corresponding to addresses 100, 101, 1100 and 1101, the switching units SW2, SW4, SW8 and SW10 are returned to initial condition. The terminal S100 goes Down and the terminal I100 goes Up. This causes the tube 352L of switching unit SW100 to become non-conductive and the tube 352R thereof to become conductive. As a result the 30 milliamperes of current flowing through switching unit SW100 now flows through resistor 364 and the electron beams are at the addresses indicated above.

The tube 352R of switching unit SW100 remains conductive and subsequent horizontal deflection is effected in the manner described above until the electron beams are to be placed at the spot position corresponding to addresses 118, 119, 1118 and 1119. To effect such, the tube 352R of switching units SW8, SW10 and SW100 are caused to be conductive. This means that a total of 57 milliamperes flows through the resistor 364 and that the remaining current or 9 milliamperes flows through the resistor 370. The electron beams are now in their most extreme deflection position.

When the beams are at the opposite extremity of deflection or in the 0 spot position, a total current of 66 milliamperes flowed through the resistor 370 and 0 current flowed through resistor 364. This unbalance in the flow of current means that the deflection pattern will not be centered on the face of the cathode ray tubes.

Referring more particularly to FIGS. 20A and 20B the vertical deflection circuit comprises vertical switching units VSW20, VSW40, VSW80, VSW200, VSW400, and VSW800; and stabilizing circuits 350 and 351. These switching units and the stabilizing circuits are similar to those described in connection with the horizontal deflection circuits of FIGS. 19A and 19B. The particular voltage and component values of the two circuits are not necessarily the same. A +367.5 volt line 380 is provided in place of the +390 volt line 366 shown in FIGS. 19A and 19B. The resistor 368 (FIG. 20A) is connected between the potential point 367 and ground; whereas, it is connected between the potential point and the +150 volt line 66 in FIG. 19A. Variations in the particular component values as well as supply voltage lines is necessitated by the different current values utilized by the vertical deflection circuits.

Connection of the S and I terminals to the tubes 360 and 361 respectively of the vertical switching units corresponds to that shown in FIG. 1A. The cathode resistor 381 of switching unit VSW20 has a value of 50K and corresponds to a vertical deflection weight of 1. The respective cathode resistors 382, 383, 384, 385, and 386 of switching units VSW40, VSW80, VSW200, VSW400 and VSW800 are of 25K, 12.5K, 10K, 5K and 2.5K respectively. Hence, in the order named these resistors represent vertical deflection weights of 2, 4, 5, 10 and 20. Again, the incremental current change required to effect deflection of the electron beams from one spot position to the next is 3 milliamperes. Since the total vertical deflection weight is the sum of 1, 2, 4, 5, 10 and 20 or 42 the total current flowing through the resistor 370 when the electron beams are in the 0 vertical spot position is 126 milliamperes and the current flowing through the resistor 364 is 0 milliamperes.

An understanding of the actual circuit operation is facilitated by conjoint reference to FIGS. 20A and 20B, FIG. 18, FIGS. 15A, 15B, 15C and 15D. As stated, when the electron beams are in the vertical spot position 0, all of the tubes 352L of the vertical switching units are conductive and 126 milliamperes of current flows through resistor 370 and 0 milliamperes flows through resistor 364. Accordingly, all of the I input terminals to the vertical switching units are Down and all of the S input terminals to the units are Up. When the electron beams are to be placed at spot position 1, the 20's line (FIG. 18) goes Up. This means that terminal S20 goes Down and terminal I20 goes Up. As a result tube 352L of switching unit VSW20 is rendered non-conductive and tube 352R thereof is rendered conductive. As a result 3 milliamperes of current now flows through resistor 364 (FIG. 20B) and 123 milliamperes flows through resistor 370 (FIG. 20A). This now places the electron beams in spot position 1.

Next, the electron beams are to be deflected to vertical spot position 2. The 20's line goes Down (FIG. 18) and the 40's line goes Up (FIG. 18). As a result the switching unit VSW20 is returned to its initial condition, tube 352L of switching unit VSW40 is rendered non-conductive and the tube 352R thereof is rendered conductive. The total current flowing through switching unit VSW40 is 6 milliamperes and this current now flows through resistor 364. The remaining current or 120 milliamperes flows through resistor 370. The electron beams are now positioned at spot position 2.

When the electron beams are to be placed at spot position 3, the 20's line goes Up (FIG. 18). This causes the tube 352R of switching unit VSW20 to be rendered conductive and the 3 milliamperes of current flowing through switching unit VSW20 now flows through resistor 364 in addition to the 6 milliamperes flowing therethrough as a result of conduction through switching unit VSW40. A total of 9 milliamperes of current now flows through resistor 364 and 117 milliamperes flows through resistor 370. The electron beams are now in spot position 3.

When the electron beams are to be placed in spot position 4, the 20's line (FIG. 18) and the 40's line (FIG. 18) go Down and the 80's line (FIG. 18) goes Up. Accordingly, switching units VSW20 and VSW40 are returned to their initial condition and the current flowing therethrough now flows through resistor 370 (FIG. 20A).

The tube 352R of switching unit VSW80 is rendered conductive and the 12 milliamperes of current flowing through switching unit VSW80 now flows through resistor 364. The electron beams are now in spot position 4. While the electron beams are in this vertical spot position, the addresses 80–99 (FIGS. 15A and 15B) or the addresses 1080–1099 (FIGS. 15C and 15D) may be visited by the electron beams in response to operation of the horizontal deflection circuits described above. Next, it is necessary that the electron beams be placed at the spot position corresponding to addresses 100, 101, 1100 and 1101 (FIGS. 15A, 15B, 15C and 15D). In order that such be accomplished the electron beams must be under a vertical deflection of 0.

The 80's line (FIG. 18) therefore goes Down and the switching unit VSW80 is returned to its initial condition. The electron beams are now at the vertical spot position 0. The cycle of operation described above is repeated (FIG. 18). This causes addresses 100–199 (FIGS. 15A and 15B) or addresses 1100–1199 (FIGS. 15C and 15D) to be visited by the electron beams. Next, the electron beams must be placed at a vertical spot position such that they will visit the addresses 200, 201, 1200 and 1201 (FIGS. 15A, 15B, 15C and 15D). These addresses correspond to a vertical spot position of 5. In order to position the electron beams at spot position 5, the 80's line (FIG. 18) goes Down and the 200's line goes Up. The switching unit VSW80 is therefore returned to its initial condition and the tube 352R of switching unit VSW200 is rendered conductive. This causes the 30 milliamperes of current flowing through switching unit VSW200 to flow through resistor 364. The electron beams are now at spot position 5.

The above described cycle of operation is now repeated i.e. the operation placing the electron beams at spot positions 1, 2, 3, 4 and 0 respectively, to place the electron beams at spot positions 6, 7, 8, 9 and 5 (FIG. 18).

The 200's line remains Up so that the tube 352R of switching unit VSW80 remains conductive and the electron beams are again progressively positioned in the step-by-step manner described above through spot positions 5–9.

It is now necessary that the electron beams be placed in spot position 11 (not shown in FIG. 18) corresponding to addresses 400 (FIG. 15A), 401 (FIG. 15B), 1400 (FIG. 15C) and 1401 (FIG. 15D). In order to position the electron beams at spot position 11, the 200's line goes Down so that the 20 milliamperes of current flowing through switching unit VSW200 now flows through resistor 370. At the same time, the 400's line (not shown, FIG. 18) goes Up and the tube 352R thereof is rendered conductive so that the 30 milliamperes of current flowing through switching unit VSW400 now flows through the resistor 364. The total current flowing through resistor 364 is now 30 milliamperes and the total current flowing through resistor 370 is 96 milliamperes. The operation described above is repeated twice in order to twice progressively position the electron beams in a step-by-step manner through the vertical positions 11–15. This causes visitation of the electron beams to the addresses 400–599 (FIGS. 15A and 15B) or 1400–1599 (FIGS. 15C and 15D).

The 200's line then goes Up to cause the tube 352R of the switching unit VSW200 to be rendered conductive so that the 15 milliamperes of current flowing through switching unit VSW200 now flows through resistor 364. Tube 352R of switching unit VSW400 remains conductive so that the total current flowing through resistor 364 is 30+15 or 45 milliamperes. The current flowing through resistor 370 is therefore 81 milliamperes. This causes the electron beams to be placed in spot position 16 corresponding to addresses 600 (FIG. 15A), 601 (FIG. 15B), 1600 (FIG. 15C), and 1601 (FIG. 15D). Operation above described is twice repeated in order to twice progressively position the electron beams through spot positions 16–20. This causes visitation of the electron beams to addresses 600–799 (FIGS. 15A and 15B) or 1600–1799 (FIGS. 15C and 15D).

The electron beams are next placed at spot position 21 corresponding to addresses 800 (FIG. 15A), 801 (FIG. 15B), 180 (FIG. 15C), 1801 (FIG. 15D). The 800's line goes Up so that the tube 352R of switching unit VSW800 is rendered conductive to cause the 60 milliamperes of current flowing through switching unit VSW800 to flow through the resistor 364, the remaining current from the switching units or 66 milliamperes flows through resistor 370. A repetition of the above described operation takes place until the beam is placed at the vertical spot position 25 corresponding to the addresses 880 (FIG. 15A), 881 (FIG. 15B), 1800 (FIG. 15C) and 1801 (FIG. 15D). When the beams are in this vertical position the greatest current which will flow through the resistor 364 flows when the tube 352R of switching units VSW800 annd VSW80 are conductive. At this time the total deflection weight is 20+4 or 24 so that the greatest current flow through the resistor 364 is 24×3 or 72 milliamperes. This means that the current flowing through the resistor 370 is 54 milliamperes. Hence, as in the horizontal deflection circuits an unbalance of current flow is present. The addresses are therefore not vertically centered on the face of the cathode ray tubes.

If at this time address 1999 has been visited the entire beam deflection operation is completed and the electron beams return to their initial position. However, if at this time the last address visited is 999, the electron beams return to their initial positions and the next address visited is 1000 (FIG. 15C). A similar deflection operation is then effected to visit addresses 1000–1999.

It is seen that the actual deflection effected to visit addresses 0–999 is identical with that which must be effected to visit addresses 1000–1999. This is clear from FIGS. 15A, 15B, 15C and 15D, FIGS. 16, 17 and 18 and FIGS. 1A and 1C since no connection from the thousands order is associated with either the horizontal or vertical deflection circuits. Connection from the thousands order is made only to the tube selector.

Dash deflection generator

The purpose of the dash deflection generator is to provide a preselected linear displacement of the cathode ray tube beam to thereby effect storage of a dash as distinguished from a dot which is stored without such deflection. In other words, the spot on the face of a cathode ray tube representing storage of a dash is physically larger than that representing the storage of a dot. As described herein the linear displacement effected to store a dash is provided from time N.46 to N.06.

If it is desired that the displacement of the beam in the horizontal plane alone is to represent a dash, then the voltage produced by the dash deflection generator is applied to the horizontal deflection plates of the cathode ray storage tube and not to the vertical deflection plates. Such displacement is provided by a horizontal dash deflection generator. If displacement of the beam in the vertical plane alone is to represent a dash, then the voltage produced by the dash deflection generator is applied only to the vertical deflection plates. Such deflection is provided by a vertical dash deflection generator. If a dash is to be represented by displacement in both the horizontal and vertical planes, then dash deflection voltage must be applied to both the horizontal and vertical deflection plates. In such case both a horizontal and vertical dash deflection generator is required.

The horizontal dash deflection generator (FIG. 19B) includes a pulse stretcher 400, an inverter I401, gating amplifier tube 402R, cathode follower tube 402L and cathode follower tube 403L and 403R.

Sync pulses (FIG. 21) are applied to terminal SP of pulse stretcher 400 and the input terminal AR1 of the pulse stretcher is connected to terminal 284 (FIG. 12).

An input pulse is therefore supplied from the terminal **284** of the octal counter of FIG. 12 from time N.40–N.50 (FIG. 21). A pull up pulse is applied to terminal **268** of pulse stretcher **400** from the terminal **268** (FIG. 13). FIG. 11 shows the circuit of the pulse stretcher **400**.

As shown in FIG. 21 the output terminal S1 of the pulse stretcher **400** goes Up at time N.06 and goes Down at N.46. The output terminal I1 of the inverter **I401** therefore goes Down at N.06 and goes Up at N.46. The output terminal I1 of inverter **401** is connected through limiting resistor **404** to the control grid of gating amplifier tube **402R** having its cathode connected to ground and its plate connected through load resistor **405** to the +150 volt terminal **66** and through parasitic suppressor resistor ps to the control grid of cathode follower tube **402L**.

The plate of gating amplifier tube **402R** therefore drives the cathode follower tube **402L**. Hence, when the control grid of amplifier tube **402R** is Down from N.06–N.46 its plate is Up and the control grid of cathode follower tube **402L** is Up and when the control grid of amplifier tube **402R** is Up from N.46 to N.06 its plate is Down and the voltage at the cathode of cathode follower tube **402L** tends to go Down or follow the voltage at its grid. However, the cathode is unable to follow the grid for the reason stated hereinafter.

The cathode of cathode follower tube **402L** is connected to ground through a condenser **407** and resistor **408** connected in parallel. Condensers **409*a*** and **409*b*** are connected in series with each other and in parallel with the condenser **407**. The plate of tube **402L** is connected to the +390 volt line **366** and to ground through a decoupling network **410** comprising a decoupling resistor and a decoupling condenser connected as shown. Condenser **409*a*** and **409*b*** serve as a voltage divider to attenuate the voltage provided by condenser **407**. When the cathode of cathode follower tube **402L** is Up from time N.06–N.46 the condenser **407** is charged. When the control grid of cathode follower tube **402L** is Down from N.46–N.06 the cathode tends to follow the control grid but is unable to do so because of the charge on the condenser **407**. During this time the condenser **407** discharges through resistor **408**. This voltage is attenuated by the condensers **409*a*** and **409*b***. The voltage waveform designated output cathode follower **402L** in FIG. 21 shows the linear voltage produced as a result of the discharge of capacitor **407**. Such a voltage is present at the juncture of condensers **409*a*** and **409*b*** connected to the control grid of cathode follower tube **403R** through parasitic resistor ps and to the ground line G through bias resistor **411**.

The plate of cathode follower tube **403R** is connected by line **355** to the cathode follower stabilizing circuit **350**. The cathodes of cathode follower tubes **403R** and **403L** are connected through common load resistor **412** to the —150 volt line **130**. The plate of cathode follower tube **403L** is connected through line **354** to the stabilizing circuit **351** (FIG. 19A). Hence, it is seen that the current flowing through cathode follower tube **403R** flows through the terminal HL (FIG. 19B) connected to the left horizontal deflection plates of the cathode ray tubes (FIG. 1C) and that the current flowing through cathode follower tube **403L** flows through terminal HR (FIG. 19A) connected to the right horizontal deflection plate of the cathode ray tubes. (FIG. 1C).

If the cathode follower tubes **403L** and **403R** are electrically identical and their respective control grids are at the same voltage, equal current will flow through the plates of these tubes. If the voltage at the control grid of tube **403R** is now decreased slightly while the voltage at the conrol grid of tube **403L** is maintained at the same voltage, the plate current flowing through tube **403R** will decrease while the plate current flowing through tube **403L** will increase. The increase in the plate current of **403L** is substantially equal to the decrease in the plate current of **403R** so that the voltage drop across load resistor **412** remains constant. During time interval N.06–N.46 the plate currents flowing through tubes **402L** and **402R** are substantially equal. However, during time N.46–N.06 the voltage at the juncture of condensers **409*a*** and **409*b***, which is decreasing at a substantially linear rate, causes the voltage at the control grid of tube **403R** to decrease at the same linear rate. This causes a decrease in the current flowing through the plate of the tube **403R** and hence a decrease in the current flowing through terminal HL (FIG. 19B). Accordingly, the current flowing through the plate of tube **403L** and hence through terminal HR (FIG. 19A) is increased by an amount substantially equal to the decrease of the current flowing through the plate of tube **403R**. The increased current flowing through terminal HR and the decreased current flowing through terminal HL causes the electron beams to be shifted to the left a preselected amount controlled and determined by the voltage change resulting from this increment of current change. A linearly varying voltage is therefore applied to the horizontal deflection plates of the cathode ray tubes during time interval N.46–N.06 because of the push-pull action of cathode follower tubes **403L** and **403R** having their plates connected to the lines **354** and **355**, respectively (FIG. 19B).

The dash deflection generator for effecting displacement of the electron beams in the vertical plane is identical with that described above for obtaining beam displacement in the horizontal plane. The vertical dash deflection generator is shown in FIG. 20B. From the above description of the horizontal dash deflection generator it is seen that the current flowing through the terminal VU (FIG. 20B) linearly decreases during time N.46–N.06 and that the current flowing through the terminal VL (FIG. 20A) linearly increases by substantially a similar amount during the same time interval. Hence, the electron beams of the cathode ray tubes are deflected upward as a result of operation of the vertical dash deflection generator. The actual deflection of the electron beams is therefore along a path which is the vector sum of the beam displacement in the vertical and horizontal planes. If, as described, the horizontal and vertical dash deflection generators are identical, then the beam displacement will be along a line at forty-five degrees with the horizontal.

Cathode ray tube selection

As explained hereinbefore, the electron beams of all the cathode ray tubes CRT A, CRT B, CRT C and CRT D (FIG. 1C) are positioned simultaneously to the same relative position on the face of the tube. However, read in, read out, and regeneration of only a single address is effected during any one time interval or cycle. This is accomplished by applying an increased voltage to the grid of the cathode ray tube whose face includes a particular address. To effect this tube selection the tube selector TS (FIGS. 1A and 22) is provided.

Referring to FIG. 22 the tube selector TS comprises four AND circuits TS1, TS2, TS3 and TS4. Each of these AND circuits is as shown in FIG. 22A. Two rectifiers **420** and **421** and a load resistor **422** are connected as shown to form an AND circuit. The two input terminals are connected to the cathodes of the rectifiers **420** and **421** respectively. A common juncture of the rectifiers and resistor **422** is connected through a parasitic resistor ps to the control grid of a cathode follower tube **423** having its cathode connected through load resistor **424** to the —82 volt terminal **74** and to the output terminal. The plate of tube **423** is connected to the +150 volt line **105**. When both input terminals are Up, the control grid of tube **423** is Up and the output terminal

is Up. If one or both of the input terminals are Down, the output terminal is Down.

The terminals I1, S1, I1000 serve as inputs to the tube selector. It is understood from the above description that the terminal I1 is Up only when decimal digit 1 is present, S1 is Up when decimal digit 1 is not present, I1000 is Up only when 1000 is present, and S1000 is Up when 1000 is not present. Terminals S1, S1000 are connected to the input terminals of AND circuit TS1.

The two input terminals of AND circuit TS1 are therefore Up simultaneously only when 1000 is not present and when 1 is not present. If 1000 is not present the address is less than 1000 and if 1 is not present the address is even numbered. Therefore, output terminal TSA connected to AND circuit TS1 is Up only when the address is even numbered and less than 1000. This means terminal TSA is Up for even numbered addresses from 0–998 or the addresses shown in FIG. 15A.

Terminals I1 and S1000 are Up simultaneously only when 1000 is not present and when a 1 is present. The terminal TSB is Up only when the address is odd numbered and less than 1000. This indicates that the address is odd numbered and between 1 and 999 as indicated in FIG. 15B.

Terminals S1 and I1000 are connected to the inputs of AND circuit TS3. The input terminals to the AND circuit TS3 are Up simultaneously only when a 1 is not present and when a 1000 is present. Terminal TSC connected to AND circuit TS3 is therefore Up when the address is even numbered and over 1000 or for the even numbered addresses from 1000–1998 as shown in FIG. 15C.

Terminals I1 and I1000 are connected to the inputs of AND circuit TS4. These inputs are Up simultaneously only when a 1 is present and when a 1000 is present. The terminal TSD connected to AND circuit TS4 is therefore Up when the address is odd numbered and over 1000 or for addresses 1001–1999 as shown in FIG. 15D.

Referring to FIG. 1C the terminals TSA, TSB, TSC and TSD are connected to one input of AND circuits AA, BA, CA and DA respectively. The other inputs of AND circuits AA, BA, CA and DA are commonly connected to dot-dash write terminal DDW.

One of the terminals TSA, TSB, TSC and TSD is Up from the time N.06–N.00 (see FIG. 11A) of each cycle. If a dot is to be written the terminal DDW is Up from the time N.40 to N.47 and if a dash is to be written terminal DDW is Up from time N.40 to N.00. The provision of means for supplying a voltage to write a dot or a dash does not constitute part of this invention and is not shown herein.

Assuming that a dot is to be written and the address at which it is to be written appears on CRT A (FIG. 15A) the terminal TSA is Up from time N.06 to N.00. Both input terminals of AND circuit AA will be Up only from time N.4 to N.47 causing the output terminal of AND circuit AA to be Up during this time. Pulse shaper PSA is therefore operative from time N.40 to N.47 to apply an increased or Up voltage to the grid of cathode ray tube CRT A. This causes the writing of a dot at the particular address to which the beam is positioned. Similarly, a dash causes an Up voltage to be applied to the grid of the cathode ray tube from time N.40 to N.00 to cause the writing of a dash. In a similar manner AND circuits BA, CA and DA and their corresponding pulse shapers PSB, PSC and PSD, respectively, cause the writing of a dot or a dash, as the case may be, on the respective cathode ray tubes CRT B, CRT C and CRT D.

The AND circuit AA and the pulse shaper PSA are shown in circuit diagram form (FIG. 23). The AND circuit BA and pulse shaper PSB, AND circuit CA and pulse shaper PSC and AND circuit DA and pulse shaper PSD each comprise a similar circuit. These pulse shapers are utilized to provide a pulse free of ragged leading and trailing edges.

Referring to FIG. 23 the tube 430R is operated as a cathode follower and the tube 430L is operated as a grounded grid amplifier. The plate of tube 430L is connected through resistor 431 to the +220 volt terminal 432, through resistor 433 and rectifier 434 to the +150 volt line 66, and to the control grid of CRT A through condenser 435. The control grid of tube 430L is connected through parasitic resistor *ps* and resistor 436 and by-pass condenser 437 to ground, and through parasitic resistor *ps* and resistor 438 to the −82 volt terminal 74. The cathodes of tubes 430R and 430L are commonly connected through load resistor 439 to the −82 volt terminal 74. The plate of tube 430R is connected through resistor 440 to the +150 volt line 66 and through capacitor 441 to ground. Resistor 440 and capacitor 441 comprise a decoupling filter.

If the output terminal of AND circuit AA is Down the control grid of tube 430R is Down. The control grid of tube 430L is so biased by the voltage divider comprising resistors 436 and 438 that the tube 430L is plate current conductive and is therefore Down.

When the output of AND circuit AA is Up the control grid of tube 430R is Up and the cathode of tube 430R accordingly Up. Since this cathode is connected to the cathode of tube 430L the cathode of tube 430L is Up. This causes a sufficient decrease in the bias between the cathode and the control grid of tube 430L to cause tube 430L to be cut off. Accordingly, the voltage at the plate increases so that an increased voltage is transferred through capacitor 435 to the terminal connected to the control grid of cathode ray tube CRT A to cause that terminal to go Up.

When the plate of tube 430L goes Up it can never go more positive than substantially 150 volts since rectifier 434 is connected between its plate and the +150 volt line 66. When the plate of tube 430L becomes more positive than 150 volts, the plate of the rectifier 434 becomes more positive than its cathode and conduction is effected through the rectifier 434 to prevent the plate of tube 430L from becoming more positive.

It is noted in FIG. 1C that the pulse shapers PSA, PSB, PSC and PSD are connected directly to the control grids of the cathode ray tubes. It is understood that a suitable bias is applied to this control grid and to the other elements of the tubes such that the potentials derived from the pulse shapers will effect an intensification of the electron beam to cause a dot and a dash, respectively, will be written upon the face of the tube selected.

Read out of the value stored in the CRT storage unit may be effected by any suitable storage output (FIG. 1C). When reading out either a dot or a dash a signal is derived from the pickup plate P associated with the cathode ray tube from which read out is effected. The storage output circuits determine, from the nature of the read out signal derived from the pickup plate, whether a dot or a dash is read out. The actual output circuits employed may be of any suitable type and do not constitute part of this invention.

Utilization of regeneration counter (FIG. 7A) to read out or carry and clear at any value from 1–16 inclusive

The connection and operation of the regeneration counter of FIG. 7A to effect read out of a single pulse or clear and carry in response to each numerical value from 1–16 inclusive will be described by conjoint reference to the chart as illustrated by FIG. 24C and FIGS. 25 and 26. In this description the information corresponding to time 9.20 should be the last used in FIG. 7D, the information corresponding to time 9.30 being found in FIG. 24A.

As explained hereinbefore, the counter of FIG. 7A effects carry and clear after 10 has been read out. This carry and clear is effected through AND circuit 201*a* as a result of the output terminal 26 of delay circuit DCC and the terminal D2 being Up at time 9.20. FIG. 25 shows the

terminals D1, D2, D4 and D8 of FIG. 7A, the terminal 282 of FIG. 12, the AND circuit 201a of FIG. 7A, a three-input AND circuit 451a, a four-input AND circuit 452a and an inverter I450 having its input terminal connected to the terminal D4. The input terminals of these AND circuits are connected to preselected ones of the terminals D1, D2, D4, D8, 282 and output terminal 450 of inverter I450 to provide a counter which will effect carry and clear in response to any read in value from 1–16 inclusive.

FIGS. 24A and 24B show that a pulse is present or absent at the various circuit points specified during each time interval from 9.30 through 15.70 to 0.00.

When it is desired to effect carry and clear in response to one input pulse the terminal 282 is connected to input terminal 202 of AND circuit 201a and the terminal D4 is connected to the other input terminal, terminal 200, of AND circuit 201a (FIG. 26). Then at time 0.20 terminal 202 is Up as a result of an N.2 pulse (FIG. 12) applied thereto and input terminal 200 is Up because terminal D4 connected thereto is Up. Output terminal 203 of AND circuit 201a is therefore Up and carry and clear are effected as described in connection with FIG. 7A.

Hence, the counter clears and carries after receipt of each input pulse and is truly a one position counter.

When it is desired to clear and carry after receipt of two input pulses the terminal 282 and terminal 13 (connected directly to output terminal 26 of delay circuit DCC) are connected, respectively, to the input terminals 202 and 200 of AND circuit 201a (FIGS. 25 and 26). At time 1.20 (FIG. 7C) the terminal 13 is Up. Likewise, the terminal 282 is Up and the output terminal 203 of AND circuit 201a goes Up to effect clear and carry.

When it is desired to effect clear and carry after receipt of three input pulses the terminals D4 and D8 are connected to the input terminals 200 and 202, respectively, (FIGS. 25 and 26). At time 2.20 (FIG. 7C) the terminals D4 and D8 are Up to effect clear and carry as described above.

When it is desired to effect clear and carry in response to four input pulses the terminals 13 and D8 (FIGS. 25 and 26) are connected to input terminals 200 and 202, respectively, of AND circuit 201a. At time 3.20 (FIG. 7C) the terminals 13 and D8 are both Up to cause clear and carry of the counter to be effected.

When it is desired to effect clear and carry in response to each fifth input pulse the terminals D4 and D1 (FIGS. 25 and 26) are connected to the input terminals 200 and 202 of AND circuit 201a. At time 4.20 (FIG. 7C) the terminals D4 and D1 are Up to cause clear and carry to be effected.

When it is desired to effect clear and carry in response to each sixth input pulse the terminals 13 and D1 (FIGS. 25 and 26) are connected to the input terminals 200 and 202 respectively of AND circuit 201a. At time 5.20 (FIG. 7D) the terminals 13 and D1 are Up to cause clear and carry to be effected.

When it is desired to effect clear and carry in response to each seventh input pulse the terminals D1, D8 and D4 (FIGS. 25 and 26) are connected, respectively, to the input terminals 453, 454 and 455 of the three-input AND circuit 451a. At time 6.20 (FIG. 7D) the terminals D1, D8 and D4 are Up to cause the output terminal 203 of AND circuit 451a to go Up. This causes clear and carry to be effected in the manner described above.

When it is desired to effect clear and carry in response to each eighth input pulse the terminals D1, D8 and 13 (FIGS. 25 and 26) are connected, respectively, to the input terminals 453, 454, 455 of AND circuit 451a. At time 7.20 (FIG. 7D) terminals 13, D1 and D8 are Up to cause clear and carry to be effected.

When it is desired to effect clear and carry in response to each ninth input pulse the terminals D4, D2 and 282 (FIGS. 25 and 26) are connected, respectively, to the input terminals 453, 454 and 455 of the three-input AND circuit 451a to cause clear and carry to be effected. At time 8.20 (FIG. 7D) the terminals D2 and D4 are Up. The terminal 282 is also Up (FIG. 12) to cause the output terminal 203 of AND circuit 451a to be Up. This causes clear and carry to be effected in the manner described above.

When it is desired to effect clear and carry in response to each tenth input pulse the terminals 13 and D2 are connected, respectively, to the input terminals 200 and 202 (FIGS. 25 and 26) as shown in FIG. 7A and clear and carry is effected at time 9.20 (FIG. 7D) in the manner described in connection with FIG. 7A.

When it is desired to effect clear and carry in response to each eleventh input pulse the terminals 282, D4, D2 and D8 (FIGS. 25 and 26), respectively, are connected to the input terminals 456, 457, 458, and 459 of the four-input AND circuit 452a (FIG. 25). At time N.2 the terminal 282 (FIG. 12) is Up and terminals D4, D2 and D8 (FIG. 24A) are Up. The output terminal 203a of AND circuit 452a therefore goes Up and clear and carry is effected as described in connection with FIG. 7A.

When it is desired to effect clear and carry in response to each twelfth input pulse the terminals 282, D2 and D8 and output terminal 450 of inverter I450 (FIGS. 25 and 26) are connected, respectively, to the input terminals 456, 457, 458 and 459 of the four-input AND circuit 452a. At time 11.20 the terminal 282 (FIG. 12) and terminals D2 and D8 (FIG. 24A) are Up. The terminal D4 (FIG. 24A) connected to the input terminal of inverter I450 is Down so that the output terminal 450 of inverter I450 is Up. The output terminal 203 of AND circuit 452a is therefore Up and clear and carry is effected as described above.

If it is desired to effect clear and carry in response to each thirteenth input pulse the terminals 282, D4, D2 and D1 (FIGS. 25 and 26) are connected, respectively, to the input terminals 456, 457, 458 and 459 of AND circuit 452a. At time 12.20 (FIG. 24A) the terminal 282 (FIG. 12) is Up and terminals D4, D2, and D1 (FIG. 24A) are Up. The output terminal 203 of AND circuit 452a is therefore Up and clear and carry is effected as described above.

If it is desired to effect clear and carry in response to each fourteenth input pulse the termina's 282, D2, D1 and 450 (FIGS. 25 and 26) are connected, respectively, to the input terminals 456, 457, 458 and 459 of the four-input AND circuit 452a. At time 13.20 (FIG. 24B) the terminal 282 (FIG. 12) is Up and terminals D2 and D1 (FIG. 24B) are Up. The terminal D4 (FIG. 24B) is Down. The output terminal 450 of inverter I450 is therefore Up. All input terminals to the AND circuit 452 are therefore Up and its output terminal 453 is Up to effect clear and carry in the manner described above.

If it is desired to effect clear and carry in response to each fifteenth input pulse the terminals D4, D2, D1 and D8 (FIGS. 25 and 26) are connected to the input terminals 456, 457, 458 and 459, respectively, of the four-input AND circuit 452a. At time 14.20 (FIG. 24B) the terminals D4, D2, D1 and D8 are Up. The output terminal 203 of AND circuit 452a is therefore Up to cause clear and carry to be effected in the manner described above.

If it is desired to effect clear and carry in response to each sixteenth input pulse the terminals 282, D2, D1 and D8 (FIGS. 25 and 26) are connected, respectively, to the input terminals 456, 457, 458 and 459 of the four-input AND circuit 452a. At time 15.20 the terminal 282 (FIG. 12) is Up and terminals D2, D1 and D8 (FIG. 24B) are Up. The output terminal 203 of AND circuit 452a is therefore Up and clear and carry is effected as described above.

It is seen that selective or cyclically operable switching means may be employed to connect the input terminals of circuits 201a, 451a, 452a and I450 to terminals D4, D2, D1, D8 and 282 to automatically vary the cycle of counter operation in accordance with any desired pattern.

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to a preferred embodiment, it will be understood that various omissions and substitutions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art, without departing from the spirit of the invention. It is the intention, therefore, to be limited only as indicated by the scope of the following claims.

What is claimed is:

1. A regeneration counter including an adder for obtaining the sum of at least two inputs applied thereto; a plurality of serially connected circuits each for producing an output in response to each input applied thereto, said output being produced a predetermined time interval after said input is applied; synchronizing means connected to all of said circuits for determining said output time interval, a connection from the output of the last of said serially connected circuits to an input of said adder; and means connected to said synchronizing means and responsive to said adder and to one of said circuits for interrupting the operation of said circuits by interrupting the output of said synchronizing means.

2. An octal counter cyclically energizable to produce an output pulse during each of eight successive time intervals including eight delay circuits connected in series chain, each delay circuit having an input and an output terminal; eight counter output terminals, one being connected to the output terminal of each delay circuit; OR circuit means connected to be energized from a pulse present at the output terminal of any delay circuit, except the last, in the chain; and circuit means coupled between said OR circuit means and the input terminal of the first delay circuit in said chain to energize said first delay circuit, said last named circuit means including an inverter and being responsive to an output at any one of said first seven delay circuits in said chain to withhold said energization of said first delay circuit.

3. A binary-decimal counter including a binary adder for effecting addition of an input in accordance with the rules of binary addition and providing a sum at an output terminal; a plurality of counting elements connected in series chain, each having an input and an output terminal, each output terminal also serving as an output terminal of said counter; a coincidence circuit connected to a juncture between an output and a succeeding input of said counting elements and to said binary adder and operable when each of the connections transfer a certain voltage condition to said coincidence circuit simultaneously; and circuit means coupling said coincidence circuit and each of said counting elements to transmit a voltage condition to each of said counting elements when said coincidence circuit is rendered operable.

4. A binary-decimal counter for effecting binary addition and providing a binary-decimal output determined by the presence and absence of Up and Down voltage conditions during predetermined time intervals including a binary adder having input means, said adder effecting addition of Up voltage conditions in accordance with the rules of binary addition and providing an Up voltage condition representing the binary sum at a sum output terminal and an Up voltage condition representing the carry obtained in deriving said sum at a carry output terminal; circuit means for transferring the Up voltage condition at said carry terminal to said adder input means during the next predetermined time interval; a plurality of counting circuits connected in series chain, each having an input and an output terminal and producing an Up voltage condition at the output terminal during the next predetermined time interval after an Up voltage condition is present at the input terminal; a connection from said sum terminal to the input terminal of the first counting circuit in said chain and from the output terminal of the last counting circuit in said chain to said adder input means, and apparatus connected to the output terminals of all of said counting circuits to determine the count indicated by the respective Up voltage conditions.

5. The invention set forth in claim 4 including a two-input AND circuit having one input terminal connected to the juncture of the second and third counting circuits of said chain and the other input terminal connected to said input means to transfer Up voltage conditions to said AND circuit to provide an Up voltage condition at the output of the AND circuit when the binary-decimal sum equivalent to the decimal number 10 is present in said counter.

6. The invention set forth in claim 5 including circuit means coupling the output of said AND circuit to each of said plurality of counting circuits to render said counting circuits inoperative when the output of said AND circuit provides an Up voltage condition.

7. In a regeneration counter having an adding circuit connected to receive input pulses during certain time intervals of a cycle of counter operation and provide a series of sum output pulses; a series of delay circuits responsive to said output pulses; a coincidence circuit having a plurality of input terminals and an output terminal; at least one connection from said delay circuits to an input terminal of said coincidence circuit and a connection from said adding circuit to another input terminal of said coincidence circuit for conjointly rendering said coincidence circuit responsive to provide a predetermined electrical condition at the output terminal of said coincidence circuit to indicate completion of a certain cyclic operation; counter output means connected to each of said delay circuits; and read out means connected to said output means to selectively control the output therefrom to provide a timed cyclic read out of the value stored in said counter.

8. A binary-decimal counter including a binary adder for supplying an output in response to at least one input pulse applied thereto, four delay circuits connected in series chain, each having an input and an output terminal, and wherein the collective output at the output terminals represents the amount stored in said counter; said adder being connected to receive an input from the output terminal of the last of said delay circuits and to deliver an output to the input terminal of the first of said delay circuits to form a recirculating pulse path; circuit means connected to said output terminals for cyclically reading out said collective output and determining, by the time of the cyclic occurrence of the read out, the value represented by each of the outputs; and read in circuit means connected to apply an input pulse to said adder a predetermined time following said read out.

9. In a regeneration counter having a cycle of operation divisible into eight equal time intervals including: first, second, third, and fourth delay circuits connected in series chain, each circuit having an input terminal for receiving an input pulse during one of said time intervals and an output terminal for exhibiting an output pulse in response to said input pulse during the next successive time interval; a binary adder having three input terminals, the first being connected for receiving a counter advance pulse during one of said equal time intervals, a carry output terminal, and a sum output terminal connected to the input terminal of said first delay circuit for supplying, during each time interval, a pulse representing the binary sum of the pulses applied to said input terminals during that same time interval, said carry output terminal being coupled to the second of said input terminals; first, second, third and fourth output terminals for providing a parallel output in binary code of the sum of the counter advance pulses applied to said binary adder; and switching circuit means coupling said first, second, third and fourth output terminals to the output terminals of said first, second, third, and fourth delay circuits respectively and operable to cause read out of said parallel output during a predetermined one of said equal time intervals.

10. The invention set forth in claim 9 including a

connection from the output terminal of the said fourth delay circuit to the third input terminal of said binary adder whereby the output presented at the output terminal of the fourth delay circuit is added in accordance with the rules of binary addition to the inputs present at the two input terminals of the binary adder during that same time interval.

11. The invention set forth in claim 9 wherein said switching circuit means includes a coincidence circuit corresponding to each of said delay circuits, each coincidence circuit being responsive to produce a single output when first and second input terminals thereof have a preselected voltage applied thereto simultaneously; means connected for producing a steady voltage at the first input terminals of each of said coincidence circuits during the predetermined time interval when said parallel output is to be read out; a connection from the output terminal of said first, second, third, and fourth delay circuits to the second input terminal of the corresponding coincidence circuits so that each of said coincidence circuits is rendered responsive when a predetermined voltage is transferred to said second input terminal from the output terminal of the corresponding delay circuit to read out the values indicated thereby.

12. In a counter for providing a continuous cyclic indication of the amount stored therein; a plurality of denominational orders, each of said orders including four delay circuits provided with input and output terminals and connected in series chain to effect a stepped delay of each pulse applied to the input terminal of the first delay circuit of said chain; a fifth delay circuit; a binary adder having three input terminals for effecting the addition of three inputs in accordance with the rules of binary addition, a sum output terminal connected to the input terminal of the first delay circuit of said chain, and a carry output terminal connected to one of said adder input terminals through said fifth delay circuit; a connection between the output terminal of the last of the delay circuits in said chain and another of the input terminals of said adder to thereby form a circulatory storage circuit to effect continuous circulation of the amount stored in said counter; each of said orders, except the highest having a carry circuit, including coincidence circuit means connected for response to simultaneous voltages at the output terminal of the second delay circuit in said chain and at the output of said fifth delay circuit to provide a carry pulse to the next higher order; a connection from each carry circuit to the other input terminal of the adder of the next higher order to transfer a carry pulse thereto; switching circuit means corresponding to each delay circuit of each series chain and responsive to two electrical conditions to produce an output; connections from the output terminal of each delay circuit of each series chain to said corresponding switching circuit means; control circuit means for timing the delivery of an input pulse to the other input terminal of the adder of the lowest order to increase the amount stored in said adder, said control circuit means being operative at a later period in the cyclic operation of said orders to supply an electrical condition to each of said switching circuit means whereby the simultaneous presence of two electrical conditions at any of said switching circuits causes the amount stored in said counter to be simultaneously read out as outputs of said switching circuit means.

13. In a system having an action cycle for effecting read in to and read out from a storage device for storing manifestations representative of preselected values and a regeneration cycle for regenerating the values previously stored, a regeneration counter comprising; a binary adder for adding inputs simultaneously received in accordance with the rules of binary addition to produce sum and carry outputs representative of the binary summation of said inputs; means operable during each regeneration cycle to provide an advance input signal to said adder; a series of delay circuits connected in series chain, each delay circuit effecting a predetermined delay of an input applied thereto to produce an output a predetermined time thereafter; means coupling said sum output of said adder to the input of the first delay circuit in said chain; and means coupling the output of the last of said delay circuits in said chain to another input of said adder and a clear and carry circuit connected for response to the timed occurrence of output signals from at least two outputs pre-selected from all of said outputs and operable to provide a denomination carry output and to clear all of said delay circuits after a predetermined number of advance input signals have been applied to said adder.

14. The invention set forth in claim 13 including output terminals coupled to the output of each of said delay circuits for exhibiting the sum of the value stored in said storage device.

15. The invention set forth in claim 13 including read out means coupled to the output of each of said delay circuits in said chain; and control circuit means responsive to the receipt of a first pulse during each regeneration cycle connected to cause said read out means to be responsive to a certain voltage at the outputs of said delay circuits to thereby cause said output terminals to indicate said sum, and responsive to a second pulse during each regeneration cycle to activate said advance input signal means to increase the value stored in said counter.

16. The invention set forth in claim 15 wherein said control circuit means includes circuits for rendering the former non-responsive to said first and second pulses during said action cycle to cause said device to continuously store the values stored therein during the last previous regeneration cycle of operation.

17. A binary-decimal counter wherein the cycle of counter operation is divided into eight successive time intervals including; a binary adder for adding pulses applied to the input thereof and providing a sum and a carry output; four series connected delay circuits for effecting storage of electrical pulses, the input of the first of said series connected delay circuits being connected to the sum output of said adder to cause said delay circuits to be rendered sequentially operable in accordance with said sum output; a coupling between the output of the last of said series connected delay circuits and the input of said adder to cause repeated storing of said pulses previously stored; decimal carry means responsive to the carry output of said binary adder and to the output of one of said delay circuits for producing a pulse representing a decimal carry from said counter; and control circuit means connected to an input of said adder for effecting read in to said counter of a pulse to be stored during one preselected time interval and connected to the outputs of all of said delay circuits for effecting read out from said counter during a different time interval, each delay circuit representing a decimal value determined by the correlation of said read out and read in and the time interval of their occurrence.

18. In combination, a binary adder for adding inputs simultaneously received in accordance with the rules of binary addition to produce an output representative of the binary sum of said inputs; four delay circuits connected in series chain each delay circuit effecting a predetermined delay of an input applied thereto to produce an output a predetermined time thereafter; means coupling the output of said adder to the input of the first delay circuit in said chain; means coupling the output of the fourth delay circuit in said chain to an input of said adder; a coincidence circuit having a plurality of input terminals and a single output terminal; a source for providing a cyclically recurring pulse; and means for selectively connecting said input terminals to said delay circuit, said binary adder, and said source to produce an output pulse at said single output terminal when any preselected number of pulses

between 1-16 inclusive are applied to said first delay circuit.

19. The invention set forth in claim 18 including clear circuit means connected to said single output terminal and said delay circuits to render said delay circuits inoperative in response to said output pulse.

20. A repeating counter comprising a plurality of pulse delay units connected serially and operable for progressive transmission of pu'ses entered from a pulse source at the first of said units with a precise delay time in each of said units, and apparatus connected for response to the pulse outputs from at least one of said units before the last for clearing the counter before the count operation is repeated.

21. A repeating counter comprising a plurality of uniform delay units providing uniform time delay periods connected serially and operable for progressive transmission of pulses entered from a pulse source at the first of said units, an output connection from each of said units for indicating various count values, and apparatus connected to at least one of said unit output connections before the last for operation in response to pulse outputs therefrom to clear the counter before the count operation is repeated.

22. A repeating counter comprising a plurality of one pulse electronic time delay circuits connected serially and operable for progressive transmission of a pulse entered from a pulse source at the first of said circuits, a synchronizing signal apparatus connected to all of said circuits for synchronizing the delay operations thereof, an output connection from each of said circuits for indicating various count values, and clearing apparatus connected to at least one of said circuit output connections before the last for operation in response to pulse outputs therefrom and connected to clear the counter before the count operation is repeated.

23. A counter for delivering a regularly repeating output pulse train sequence successively at a plurality of counter output terminals; each pulse train sequence consisting of a pulse-on portion consisting of at least one pu'se period during which a pulse is supplied, and a pulse-off portion consisting of at least one pulse period during which no pulse is supplied; which comprises a plurality of serially connected one pulse delay storage elements each having output terminals which together comprise the output terminals of the counter, each of said delay elements being operable during each pulse cycle to transmit and clear a pulse stored therein and to receive and store an input pulse received thereby; input apparatus normally operable during every pulse period connected to supply an input pulse to the first of said delay elements; said serially connected delay elements being comprised of a first serially connected group including the first delay element, the number of elements in said first group being equal to the number of pulse periods in said pulse-on portion of said pulse train sequence, and a second serially connected group including the first delay element after said first group, the number of elements in said second group being equal to the number of pulse periods in said pulse-off portion of said pulse train sequence; and clearing apparatus connected from the inputs of all of said elements in said second group to said input apparatus and operable in response to a pulse at any of said second group element inputs for inhibiting the normal operation of said input apparatus.

24. In a cyclically operable commutator, a plurality of serially connected one pulse delay storage elements each having output terminals, a source of synchronizing pulses connected to synchronize all of said delay elements, each of said delay elements being operable during each pulse cycle to transmit and c'ear a pulse stored therein and to receive and store an input pulse occurring in the presence of a pulse from said synchronizing pulse source, input apparatus normally operable during every pulse period connected to supply an input pulse to the first of said delay elements, and clearing apparatus connected for operation in response to an output pulse from any of said delay e'ements except the last for inhibiting the normal operation of said input apparatus.

25. A cyclically operable counter comprising a master circuit including a plurality of serially connected one pulse delay storage elements each having output terminals for successively delivering a repeating pu'se train sequence, input apparatus normally operable during every pulse period connected to supply an input pulse to the first of said delay elements, clearing apparatus connected to all of said output terminals except the last and operab'e in response to an output pulse from any of said connected output terminals for inhibiting the normal operation of said input apparatus, at least one slave circuit including a plurality of one pulse delay storage elements each having output terminals for successively de'ivering an electrically independent repeating pulse train sequence corresponding to the sequence delivered by said master circuit, a control connection from one of said master circuit output terminals to the input of the first delay element of said slave circuit, and a source of synchronizing pulses connected to synchronize all of said delay elements, each of said delay elements being operable during each pulse cycle to transmit and clear a pulse stored therein and to receive and store an input pulse occurring in the presence of a pulse from said synchronizing pulse source.

26. A dynamic storage binary counter comprising a plurality of substantially similar pulse delay units connected for progressive transmission of pulses in serial fashion in a circulatory loop, said loop being closed through a full binary adder by a connection from the output of the last delay unit to one of the adder inputs and by a connection from the adder sum output to the input of the first delay unit, the output connections of said delay units having a series of progressively decreasing assigned binary order va'ues in relation to the direction of pulse transmission, an auxiliary pulse delay unit having the same delay period as said previously recited delay units connected to receive the carry output of said adder and to deliver a delayed pulse to another of the inputs of said adder in response thereto, a timing device operable in synchronism with said loop, a read out device controlled by said timing device and operab'e at a predetermined time in the period of operation of said loop to read out the designated values indicated by the presence of pulses at said loop delay unit output connections at that time, and an advance pulse device controlled by said timing device and operable at a predetermined time in the period of operation of said loop to supply advance pulses to be counted to the third input of said adder.

27. In a cyclically operab'e counter for storing a cumulative count of single pulses received during a predetermined portion of different cycles of operation, a cycle timing commutator, an individual counter circut for each of a plurality of denominational orders, each of said counter circuits including a plurality of serially connected one pulse delay storage elements, a binary pulse adder having a sum output connected to the input of the first of said delay elements to form a closed recirculating count storage loop, a carry loop for said adder comprising a one pulse delay storage element connected from the adder carry output to another adder input, a source of synchronizing pulses which is synchronized with said cycle timing commutator and connected to all of said delay elements, each of said delay elements being operable during each pulse cycle to transmit and clear a pulse stored therein and to receive and store an input pulse occurring in the presence of a pulse from said synchronizing pulse source, an advance pulse connection to an input of said adder, apparatus connected for control by said cycle timing commutator and operable during a predetermined synchronized pulse period of every counter cycle for which a pulse is to be counted to transmit a counter advance pulse to the advance pulse connection of the lowest order, the counter circuit of each order including clearing

apparatus operable at a subsequent predetermined counter cycle pulse period in response to delay element output voltages indicating a completion of the count in that order for clearing that order by interrupting the operation of said synchronizing pulse source and operable for all orders except the last for transmitting an order carry pulse to the advance pulse connection for the next higher order, and read out apparatus connected for control by said cycle timing commutator and operable during a predetermined counter cycle pulse period for simu'taneously reading out all output pulses present at all delay elements in said count storage loops of all counter circuit orders.

28. In a counter for supplying coded output pulses representative of the number of input pulses counted; a p'urality of denominational orders, each order having circulatory circuit storage means for effecting continuous recirculation of values stored therein and a plurality of output connections for indicating said information as coded output pulses; read in circuit means for advancing the value stored in said counter including input circuit means connected to the lowest of said orders for selectively supplying input pulses thereto, each of said orders including a carry circuit operable upon the comp'etion of the count in said order to supply a carry input pulse to the next higher order and clearing circuit means connected to said carry circuit for operation to clear the order in response to the carry pulse supplied to the next higher order; and read out means operable at a predetermined period in the operation of said circulatory storage means to simultaneously read out all of said coded output pulses at said output connections.

29. In a cyclica'ly operable counter for storing a cumulative count of single pulses received during a predetermined portion of different cycles of operation. a cycle timing commutator comprising a plurality of serially connected one pulse delay storage elements, input apparatus normally operab'e during every pulse period to supply an input pulse to the first of said delay elements, clearing apparatus connected for operation in response to an output pulse from any of said delay elements except the last for inhibiting the normal operation of said input apparatus, a counter circuit comprising a plurality of serially connected one pu'se delay storage elements, a binary pulse adder having a sum output connected to the input of the first of said counter delay elements and having an input connected to the last of said counter delay elements to form a closed recirculating count storage loop, a carry loop for said adder comprising a one pulse delay storage element connected from the adder carry output to another adder input, a source of synchronizing pulses connected to synchronize all of said de'ay elements, each of said delay elements being operable during each pulse cycle to transmit and clear a pulse stored therein and to receive and store an input pulse occurring in the presence of a pulse from said synchronizing pulse source, apparatus connected for operation in response to an output pulse from one of said delay elements of said cycle timing commutator during a predetermined pulse period of every counter cycle for which a pulse is to be counted to transmit a counter advance pulse to an input of said adder, read out apparatus connected for operation in response to an output pulse from another one of said commutator delay elements during another predetermined counter cycle pulse period for simultaneously reading out all output pulses present at all delay elements in said count storage loop, and counter clearing apparatus connected for operation at a subsequent predetermined counter cycle pulse period in response to counter delay element output voltages indicating a completion of the count for clearing said counter delay elements.

30. A counter comprising a plurality of pulse delay units connected for progressive transmission of pulses in serial fashion, each of said pulse delay units having an output connection for providing timed output pulse signals, an OR circuit connected to receive the output signals of all except the last of said delay units, an inverter connected to receive the output from said OR circuit and a connection from the output of said inverter circuit to the input of the first of said delay units to provide a pulse input suppression signal in response to an output from any of said delay units except the last.

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