



US 20130267046A1

(19) **United States**

(12) **Patent Application Publication**  
**OR-BACH et al.**

(10) **Pub. No.: US 2013/0267046 A1**

(43) **Pub. Date: Oct. 10, 2013**

(54) **METHOD FOR FABRICATION OF A SEMICONDUCTOR DEVICE AND STRUCTURE**

(52) **U.S. Cl.**  
USPC 438/14; 438/401; 257/E21.214; 257/E21.521

(76) Inventors: **Zvi OR-BACH**, San Jose, CA (US);  
**Deepak C. SEKAR**, San Jose, CA (US);  
**Brian CRONQUIST**, San Jose, CA (US)

(57) **ABSTRACT**

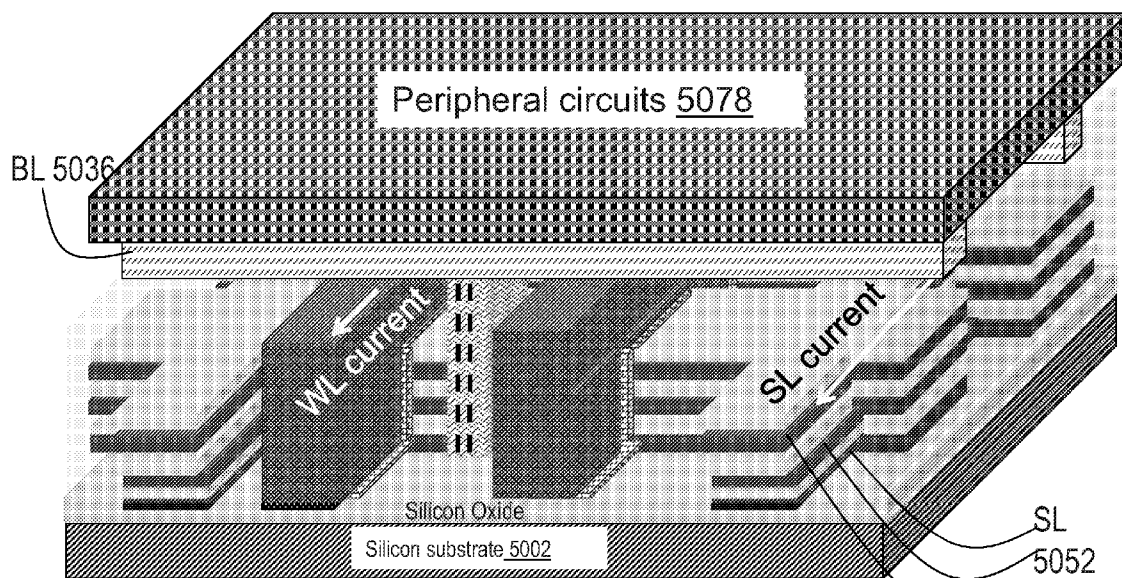
(21) Appl. No.: **13/441,923**

(22) Filed: **Apr. 9, 2012**

A method to process an Integrated Circuit device including processing a first layer of first transistors, then processing a first metal layer overlaying the first transistors and providing at least one connection to the first transistors, then processing a second metal layer overlaying the first metal layer, then processing a second layer of second transistors overlaying the second metal layer, wherein the second metal layer is connected to provide power to at least one of the second transistors.

**Publication Classification**

(51) **Int. Cl.**  
**H01L 21/66** (2006.01)  
**H01L 21/302** (2006.01)



- |                               |  |                     |  |                    |  |                 |  |
|-------------------------------|--|---------------------|--|--------------------|--|-----------------|--|
| Gate dielectric 5028          |  | Silicon oxide 5032  |  | n+ Silicon 5026    |  | BL contact 5034 |  |
| Resistance change memory 5038 |  | Gate electrode 5030 |  | Silicon oxide 5022 |  | BL 5036         |  |

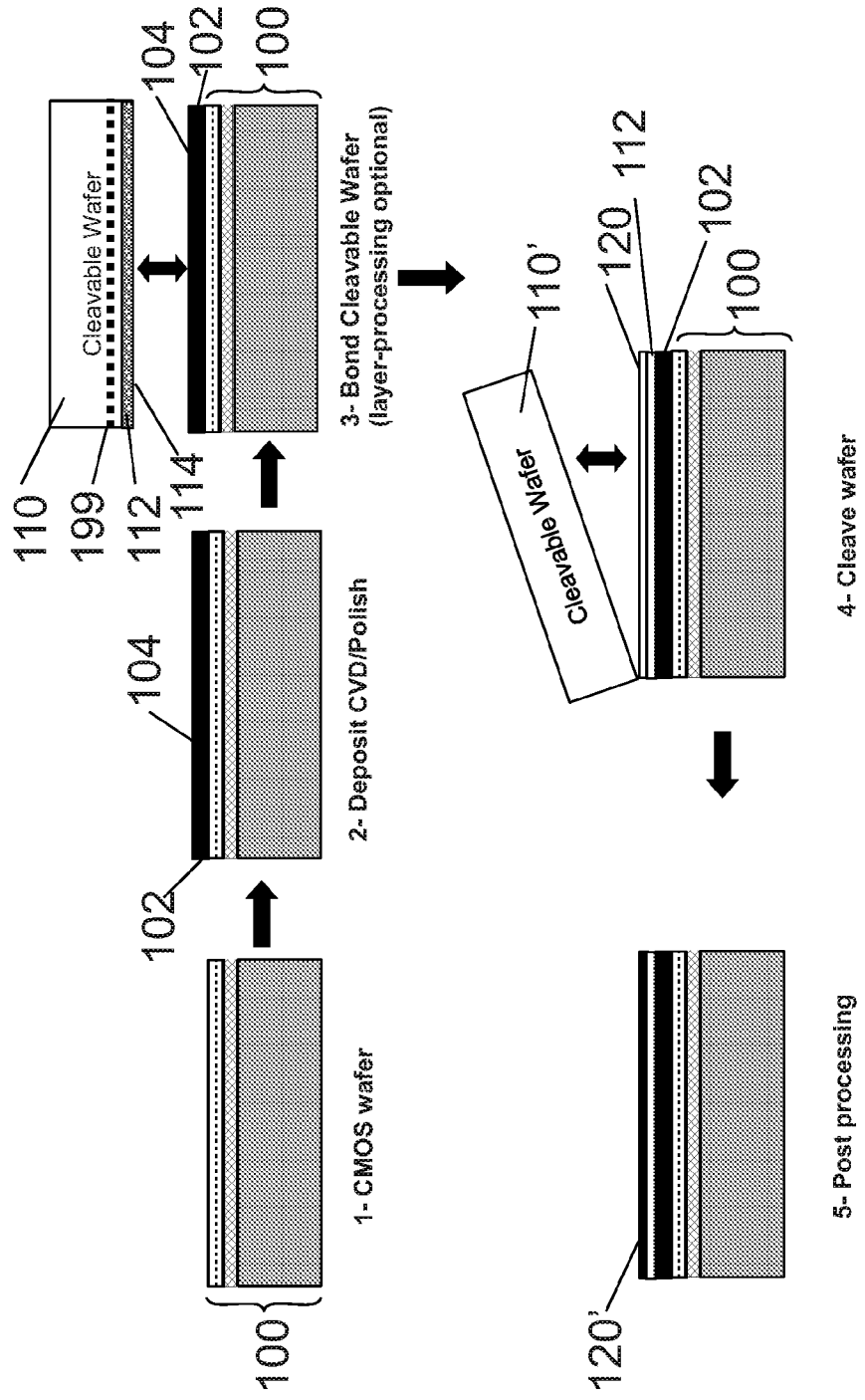


FIG. 1

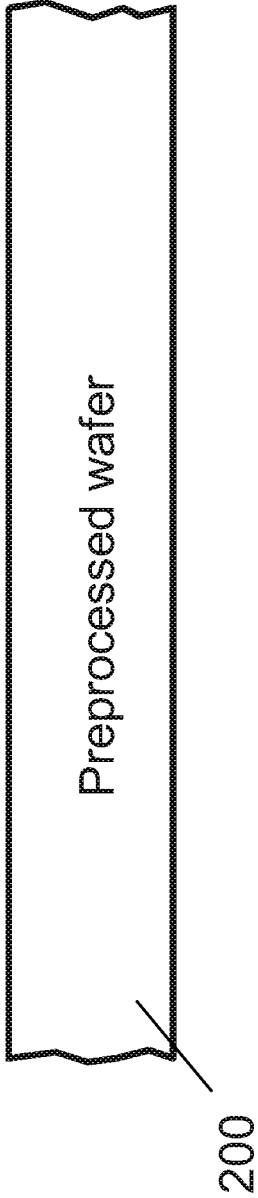


FIG. 2A

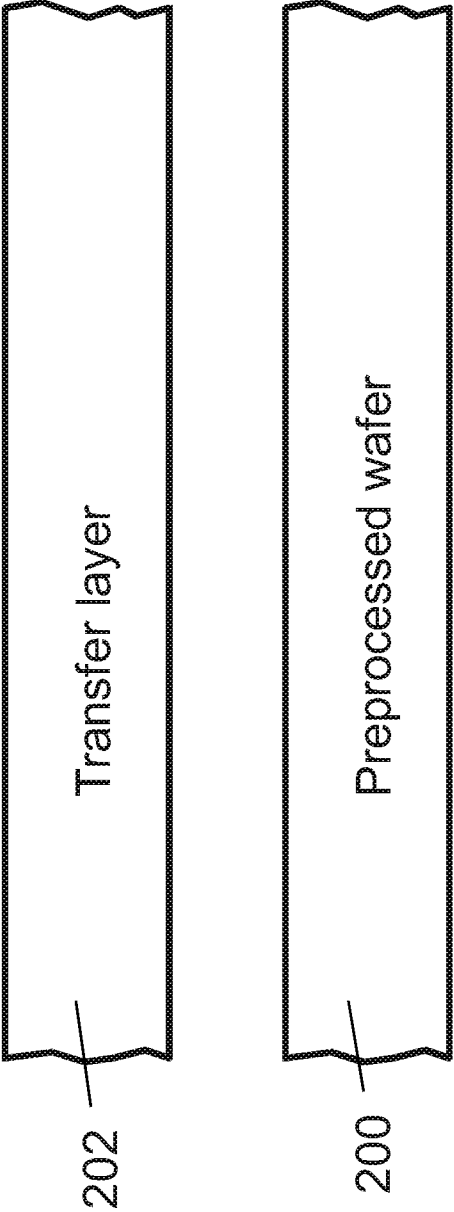


FIG. 2B

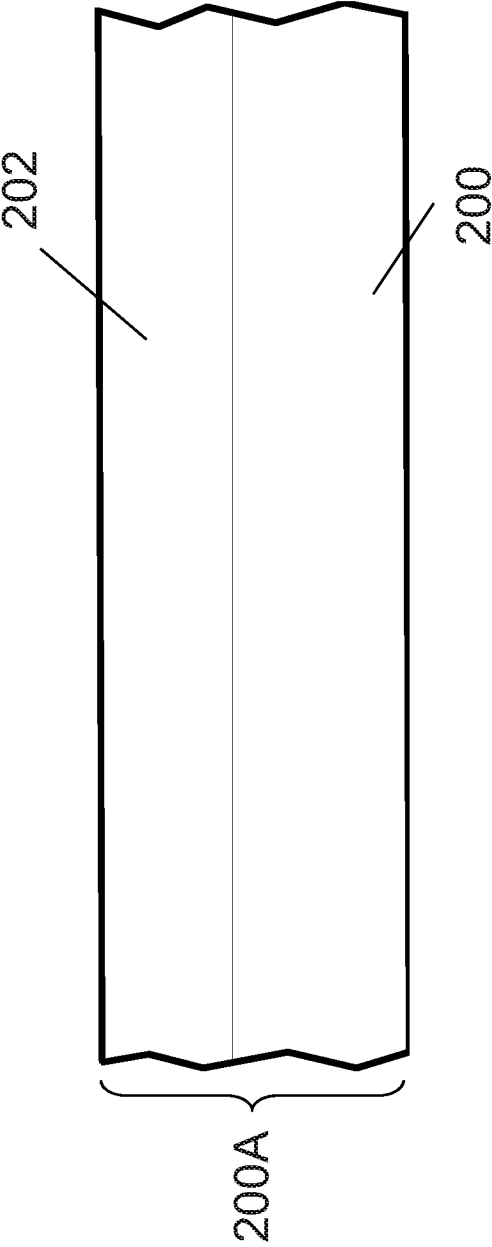


FIG. 2C

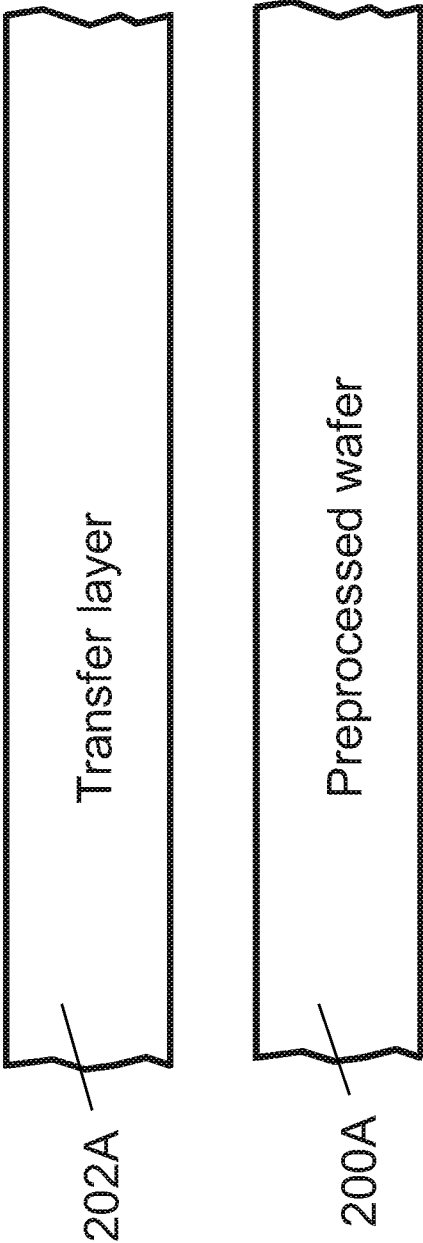


FIG. 2D

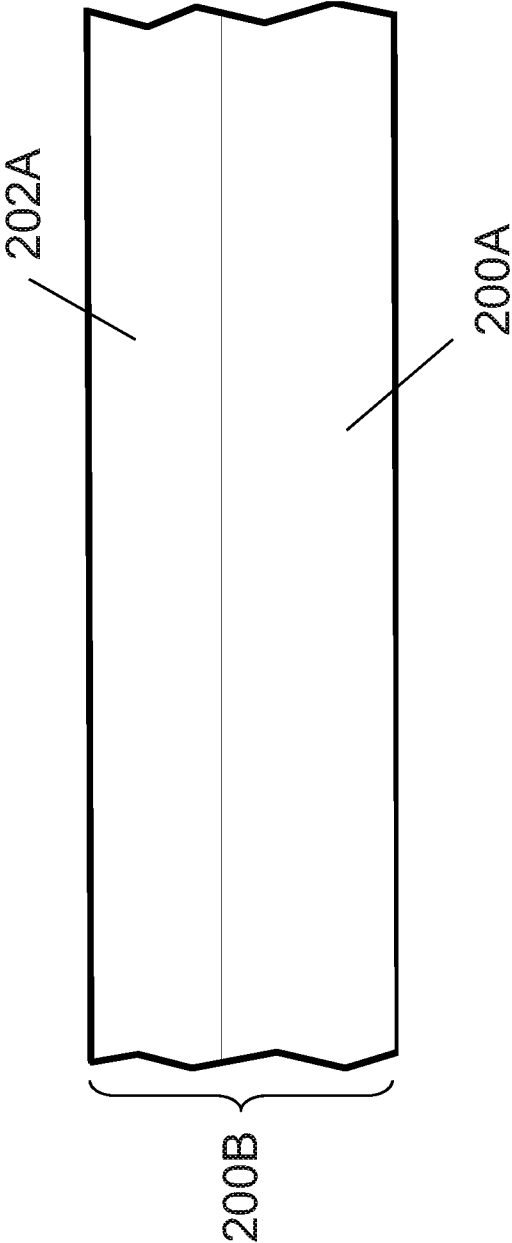


FIG. 2E

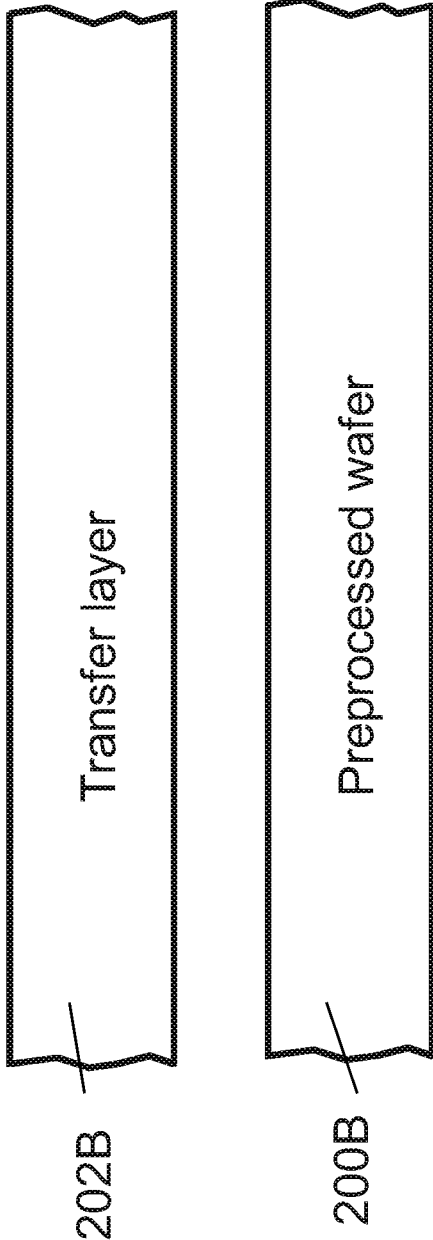


FIG. 2F



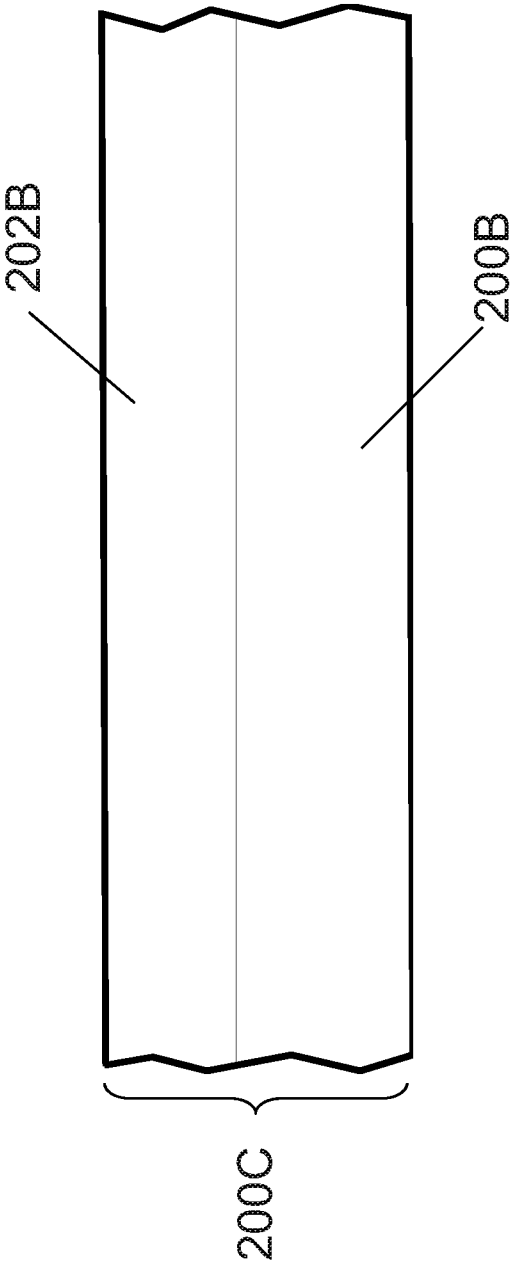


FIG. 2G

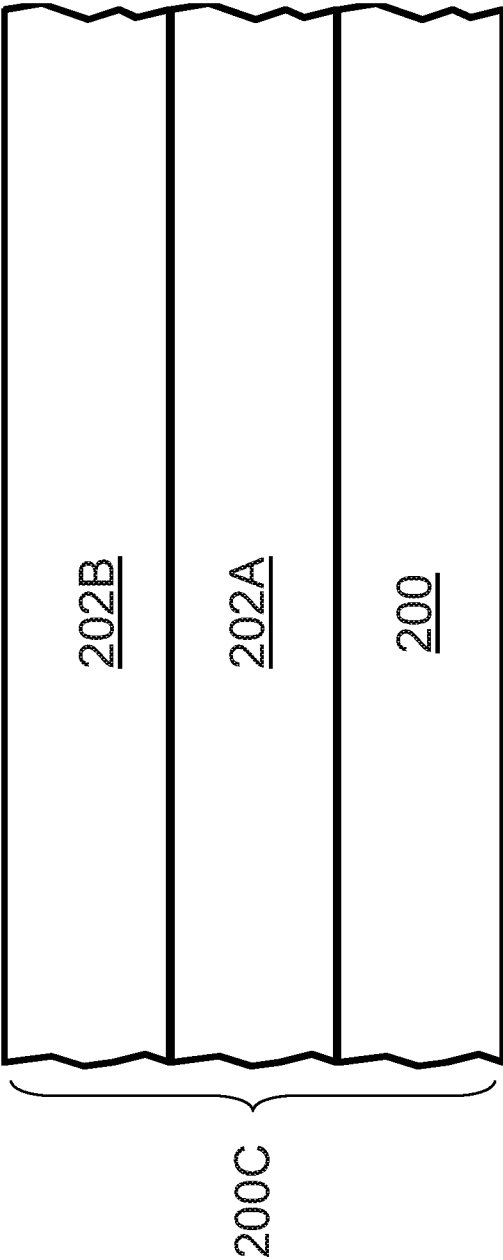


FIG. 2H

FIG. 3A

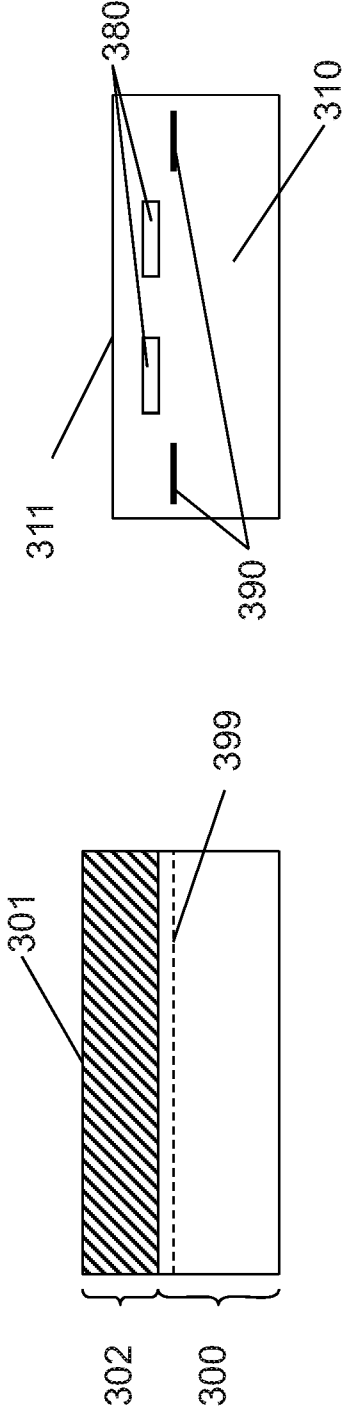


FIG. 3B

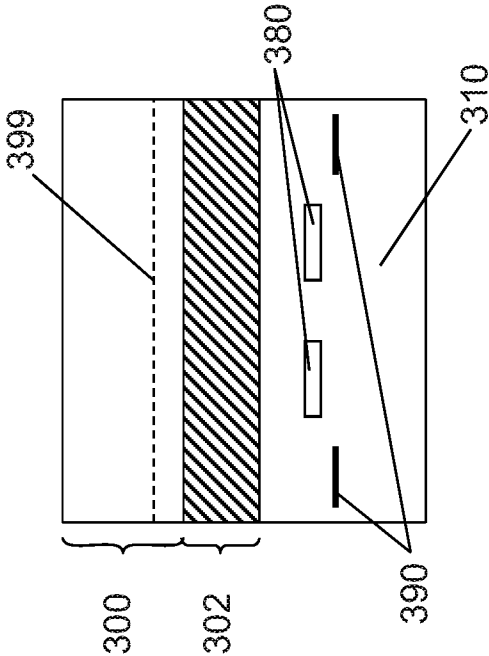


FIG. 3C

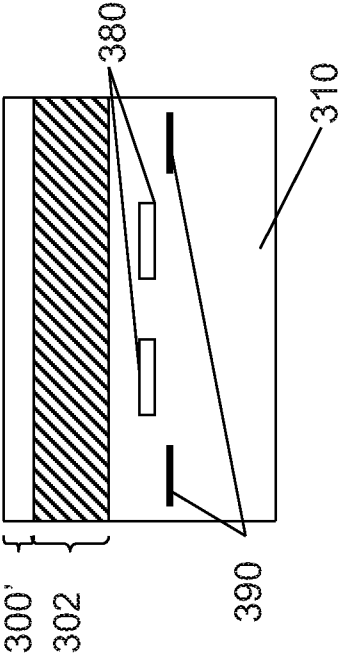
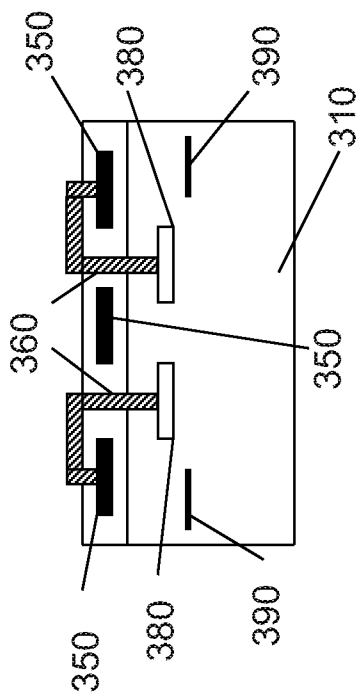


FIG. 3D



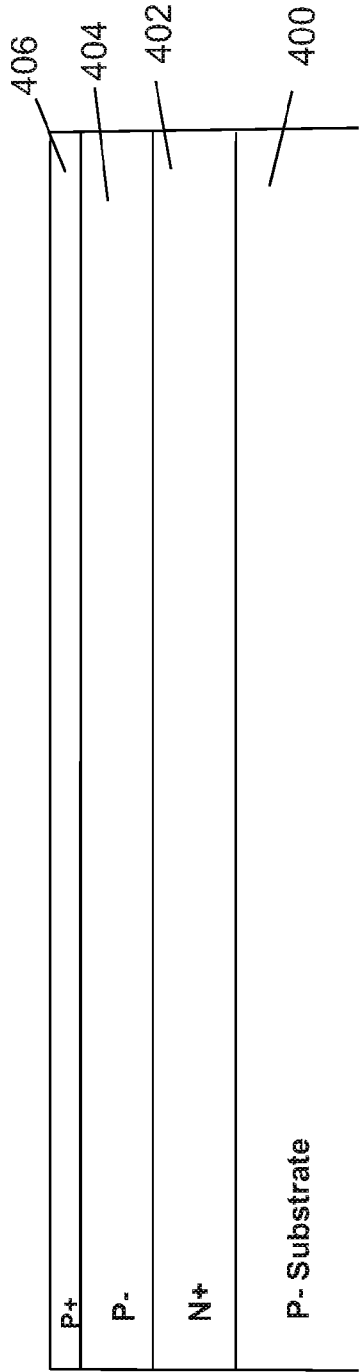


FIG 4A

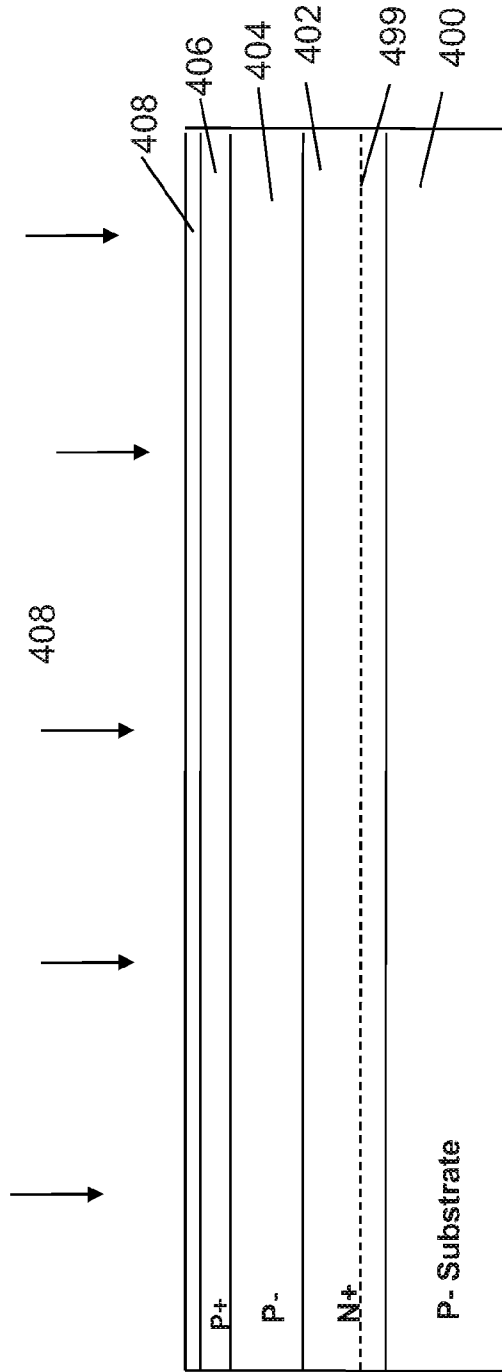


FIG 4B

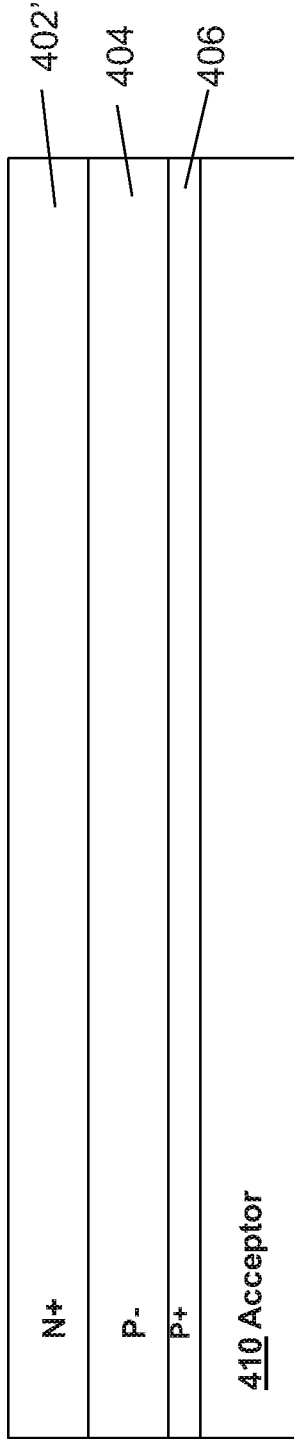


FIG 4C

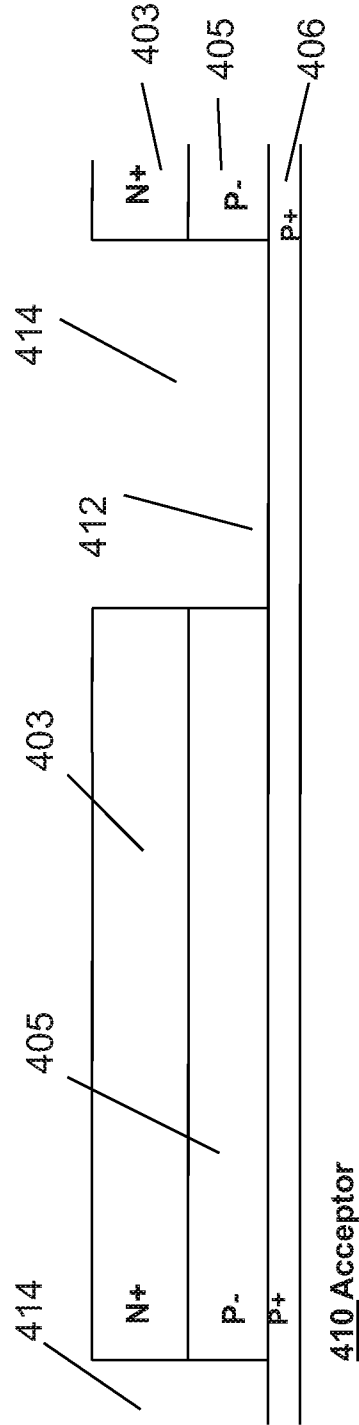


FIG 4D



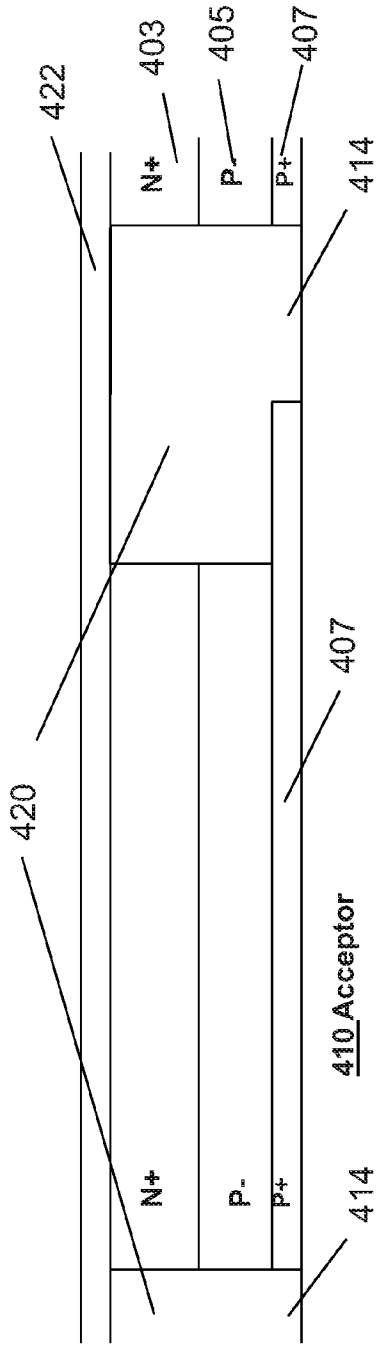


FIG 4E

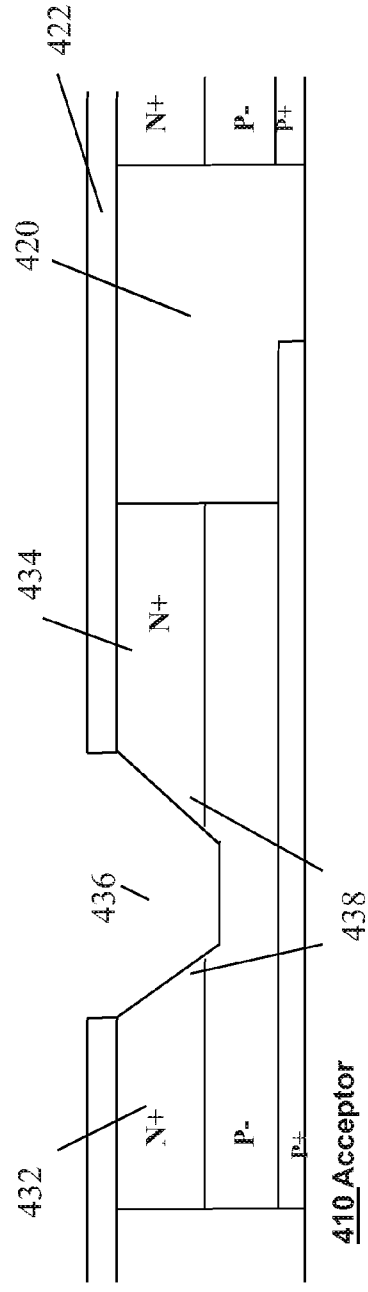


FIG 4F

FIG 4G

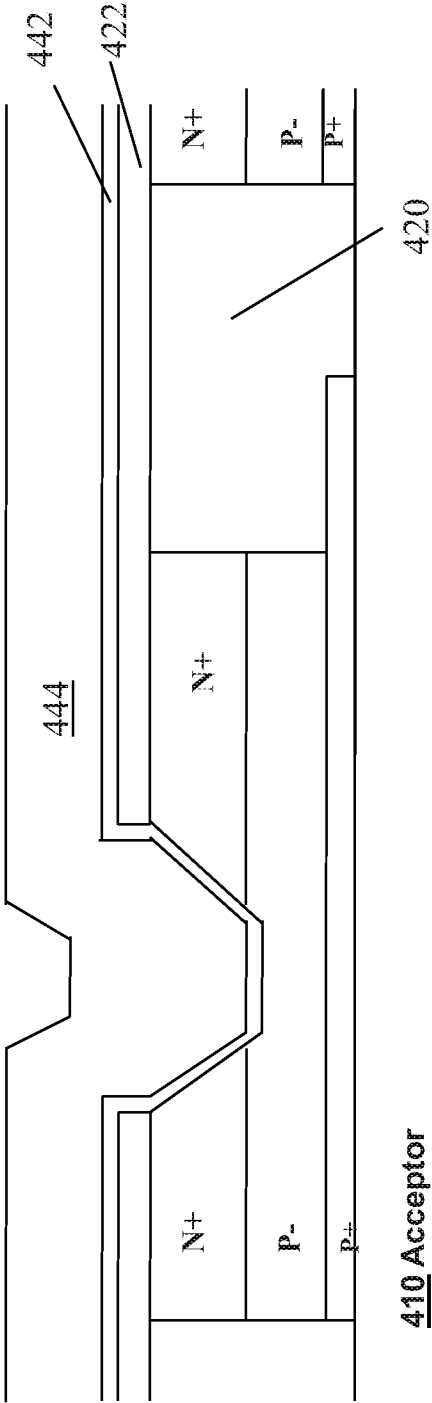
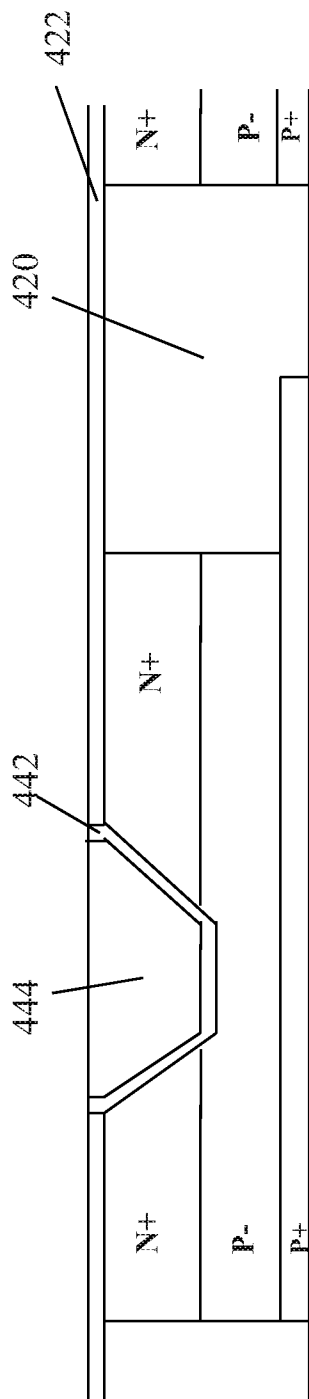


FIG 4H



410\_Acceptor

FIG 4I

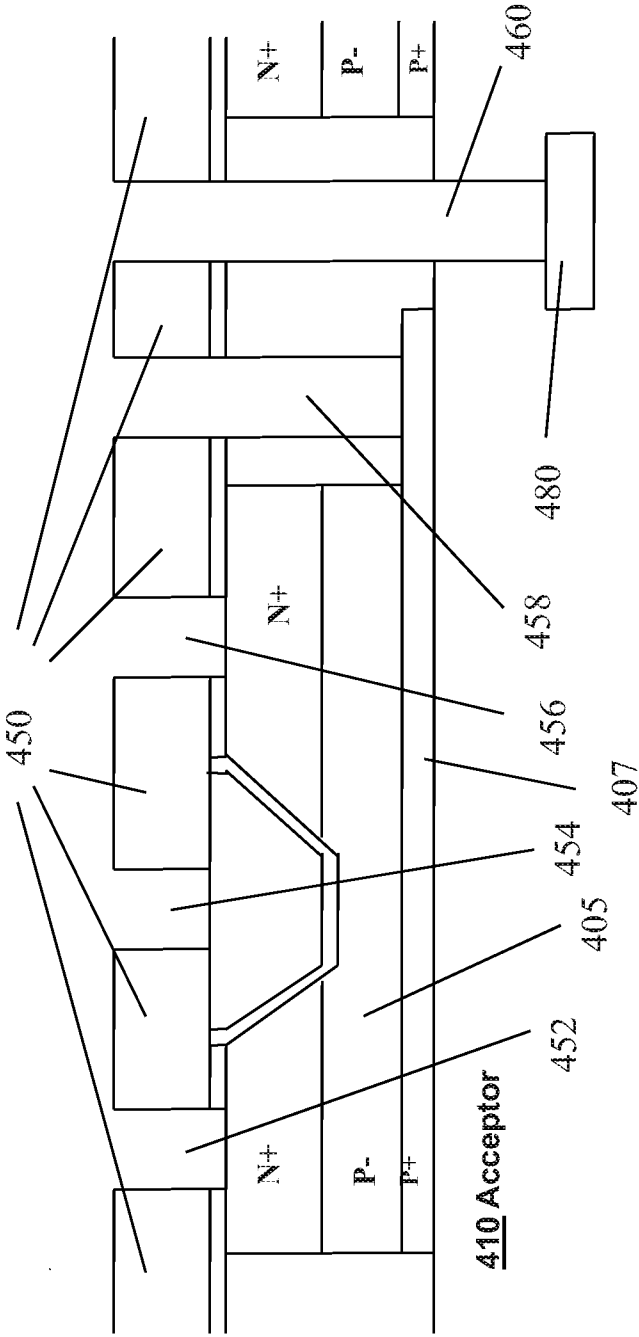
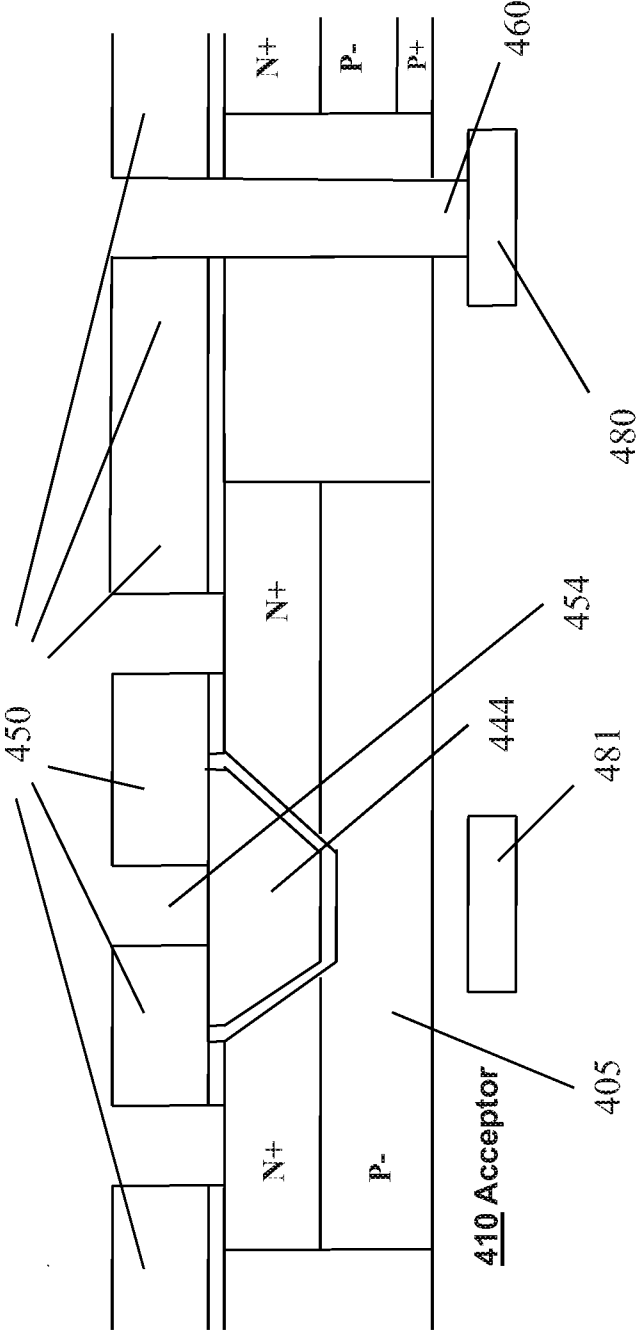
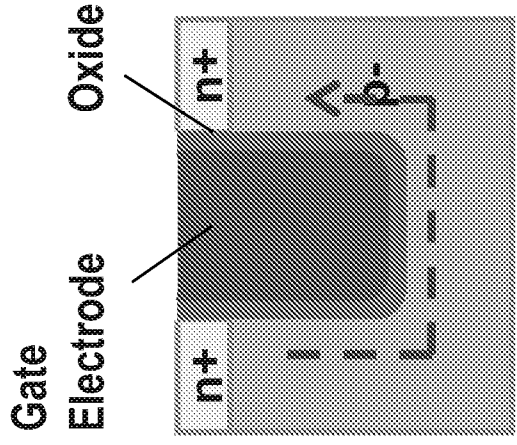


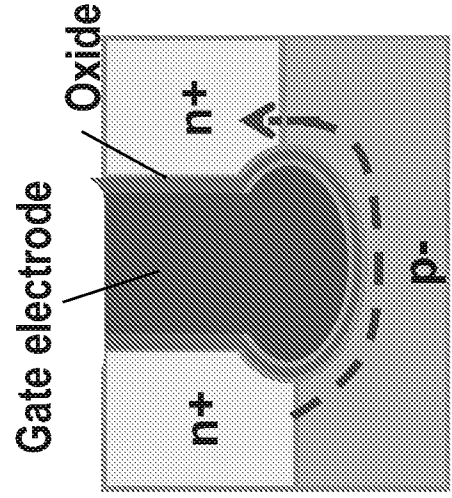
FIG 4J



Standard RCAT



Spherical-RCAT (SRCAT)



Current flow in two dimensional plane, indicated by - ->

Prior Art

FIG. 5

FIG. 6A

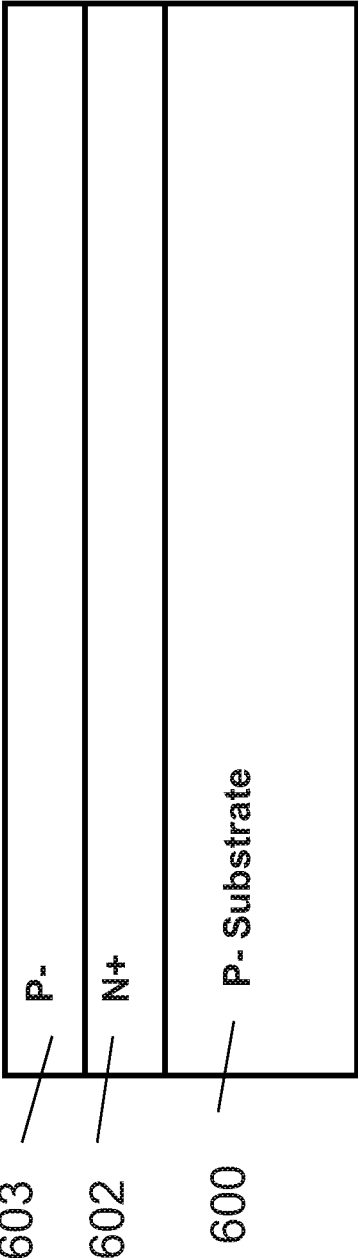


FIG. 6B

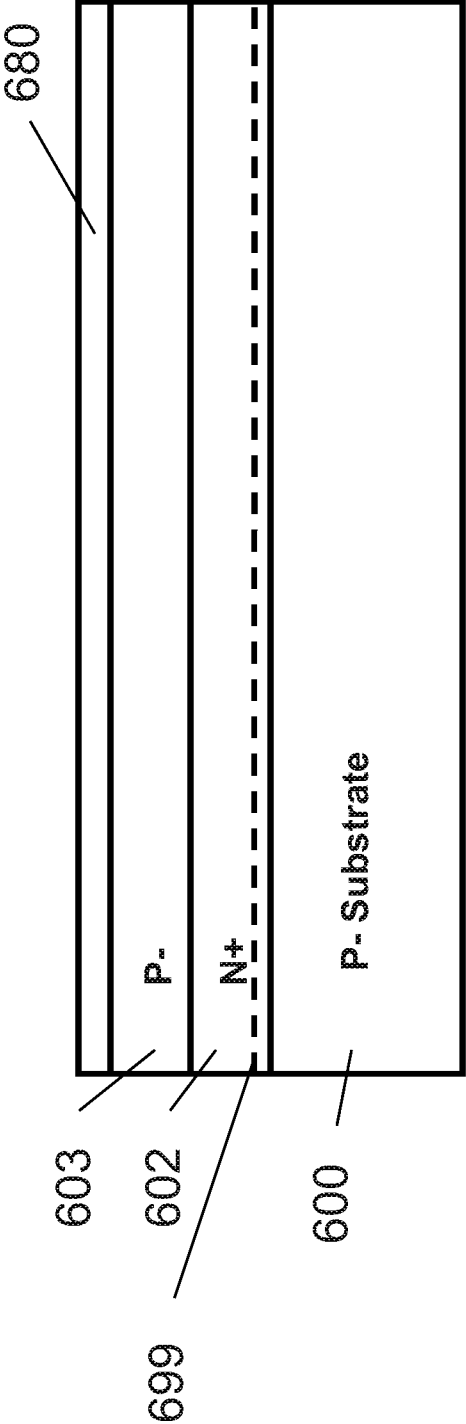




FIG. 6C

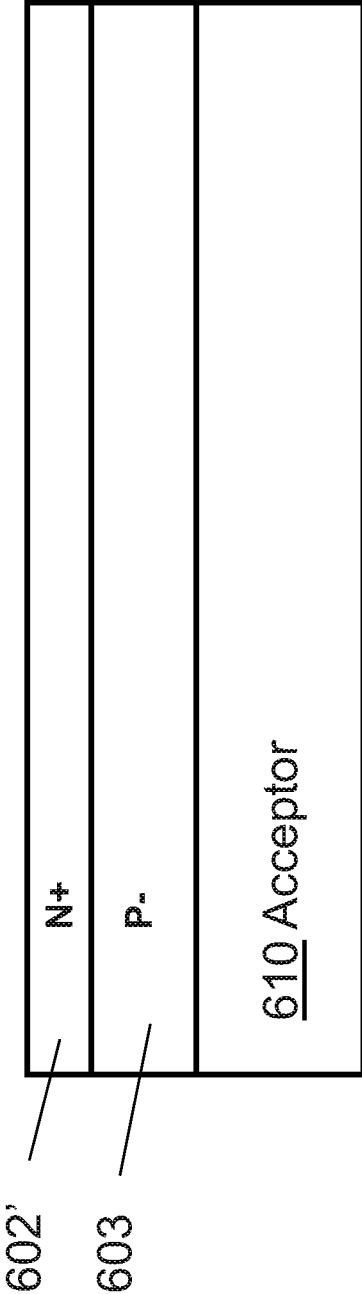
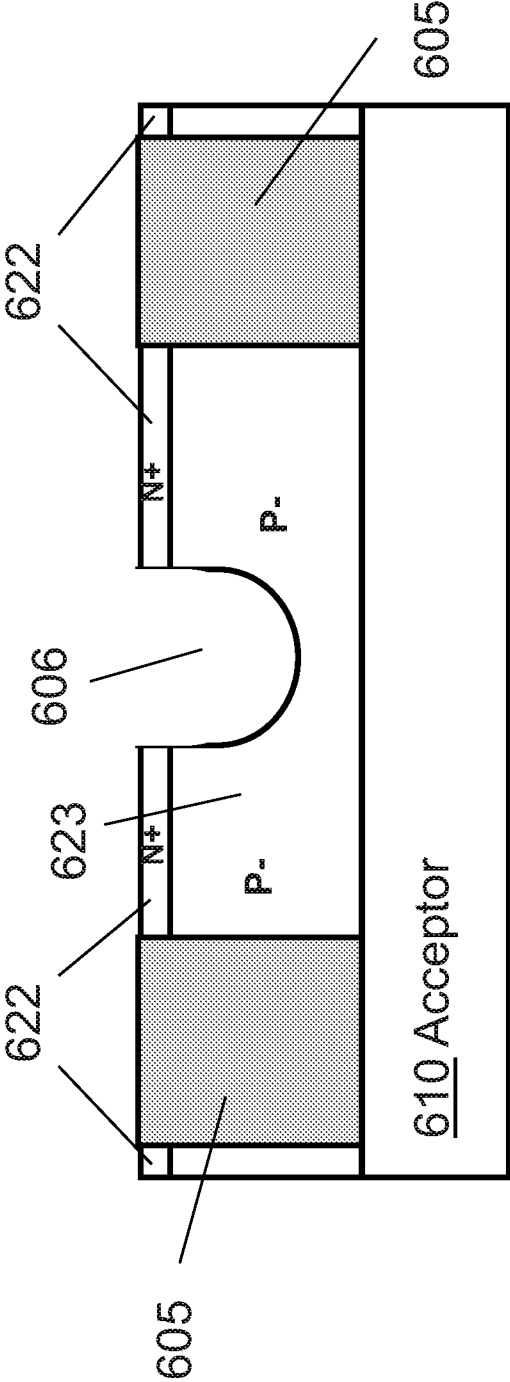


FIG. 6D



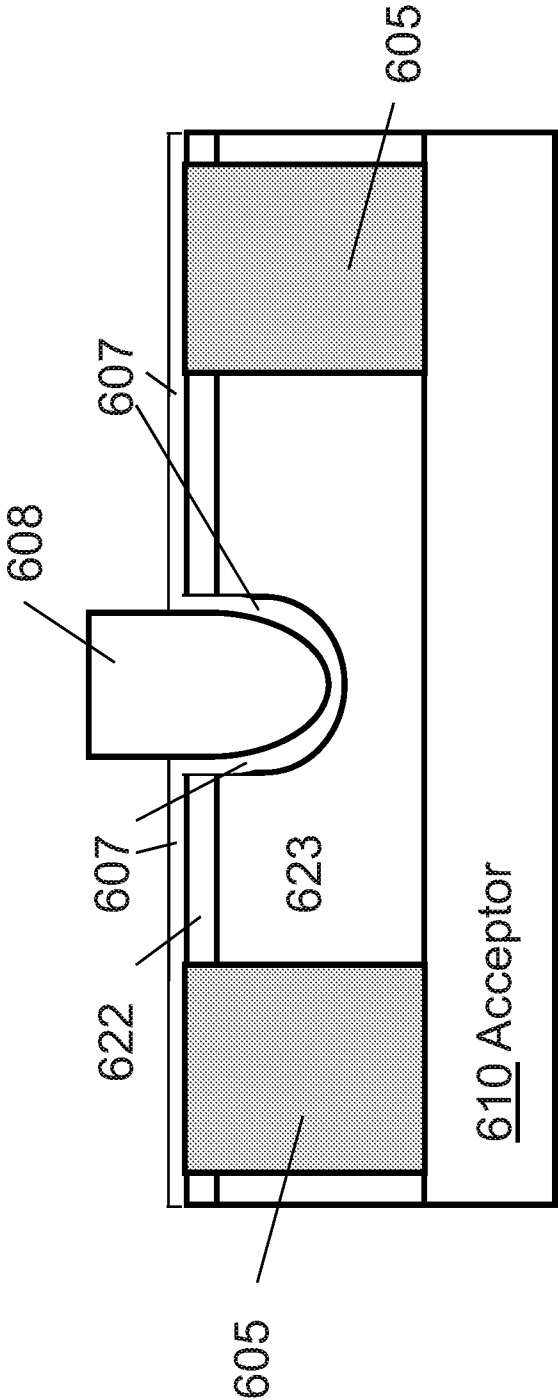


FIG. 6E

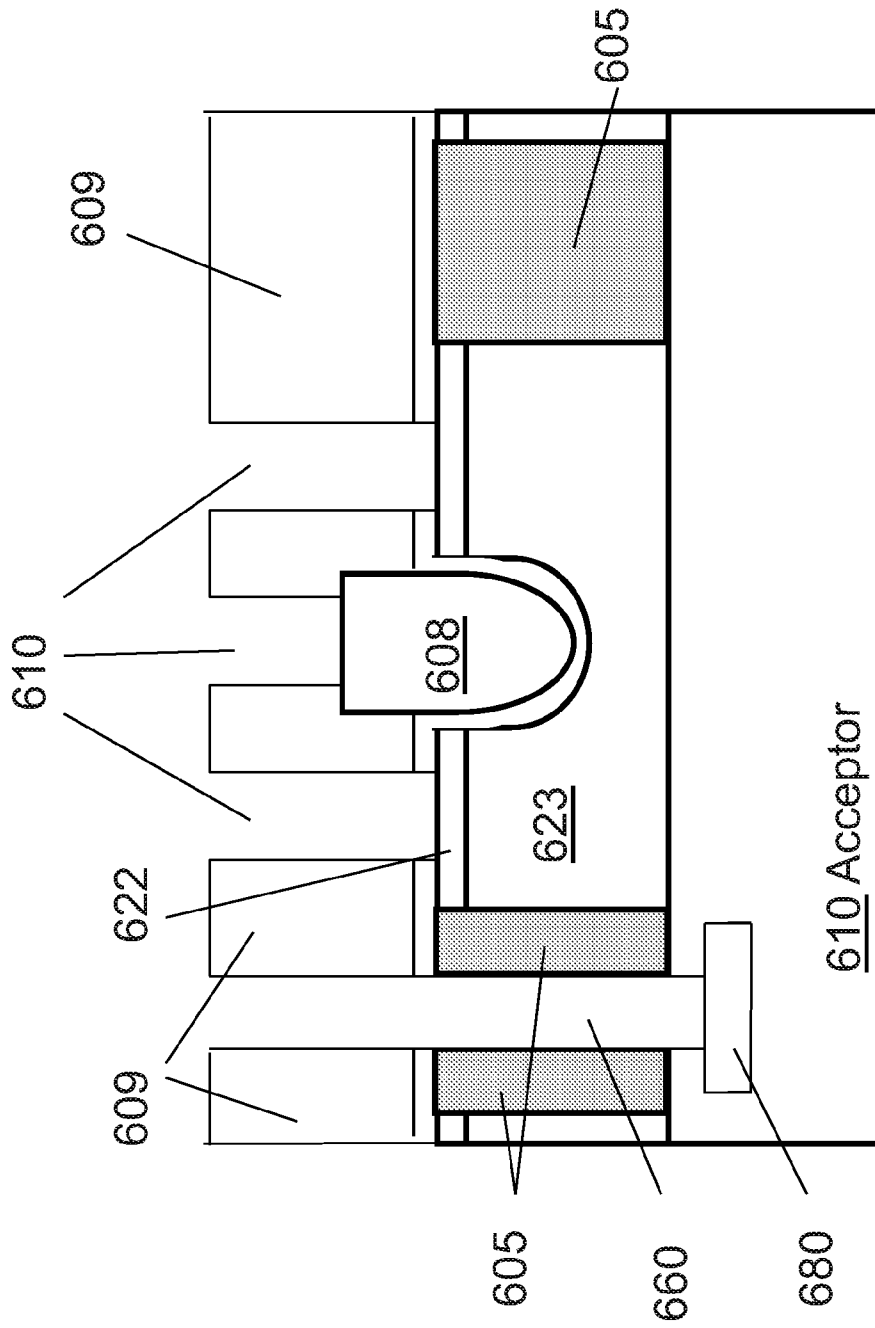


FIG. 6F

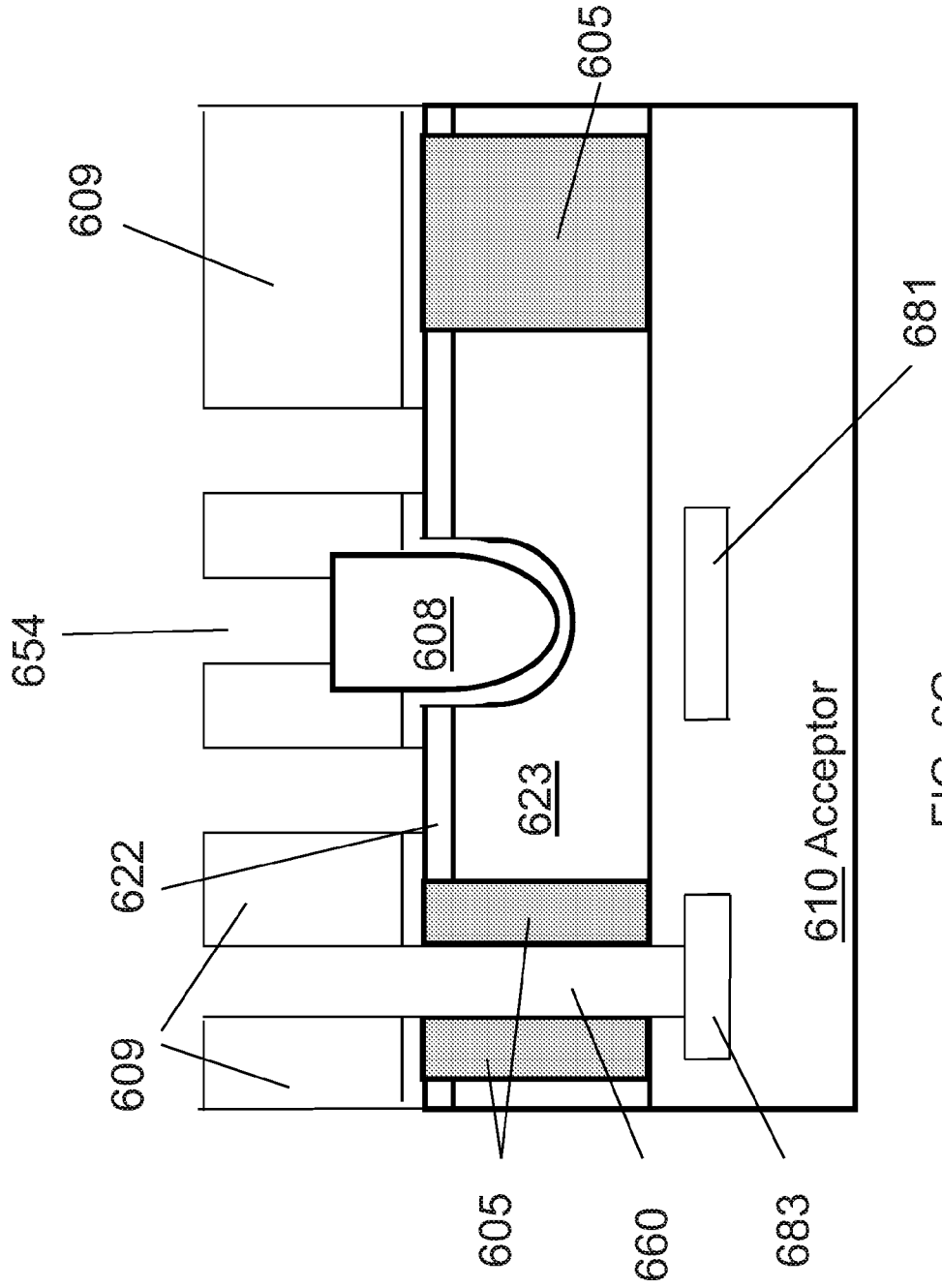


FIG. 6G

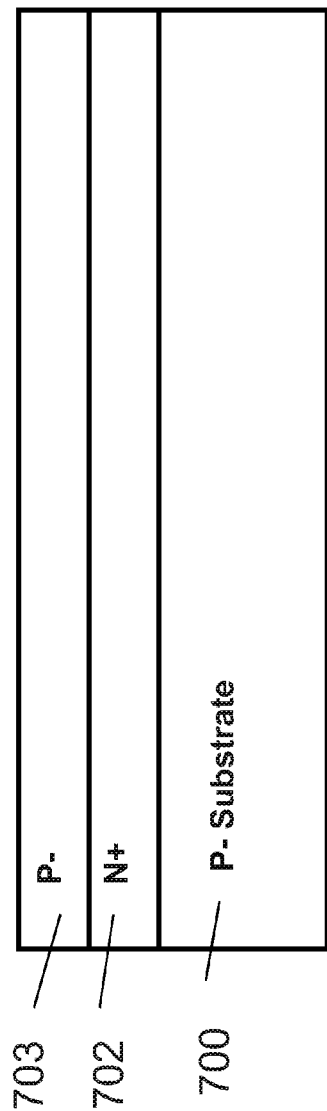


FIG. 7A

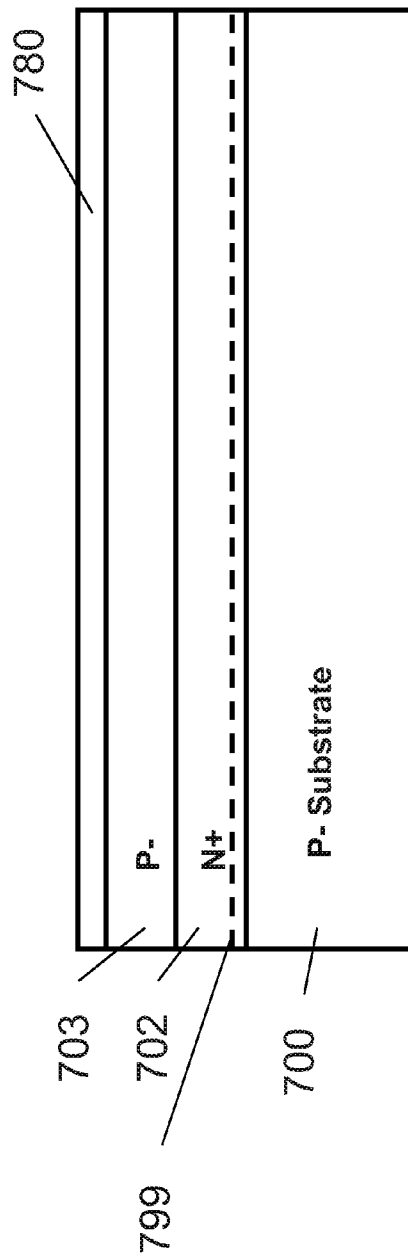


FIG. 7B

FIG. 7C

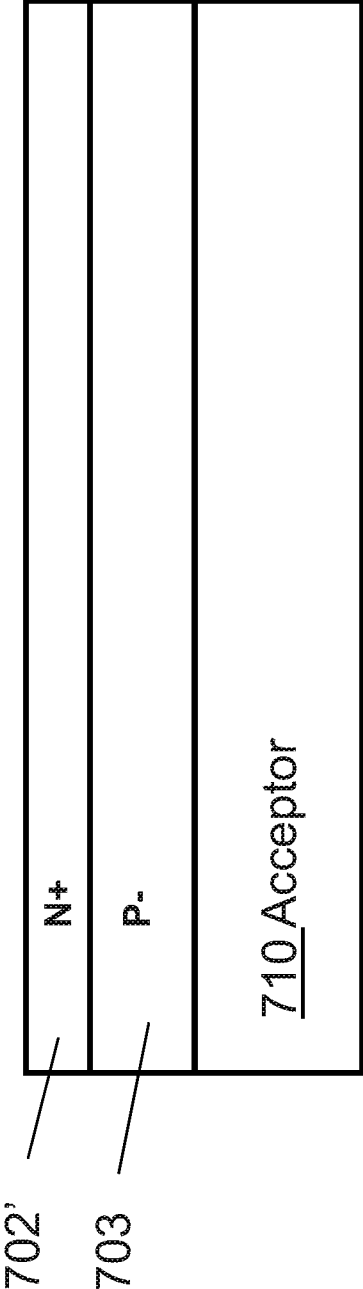
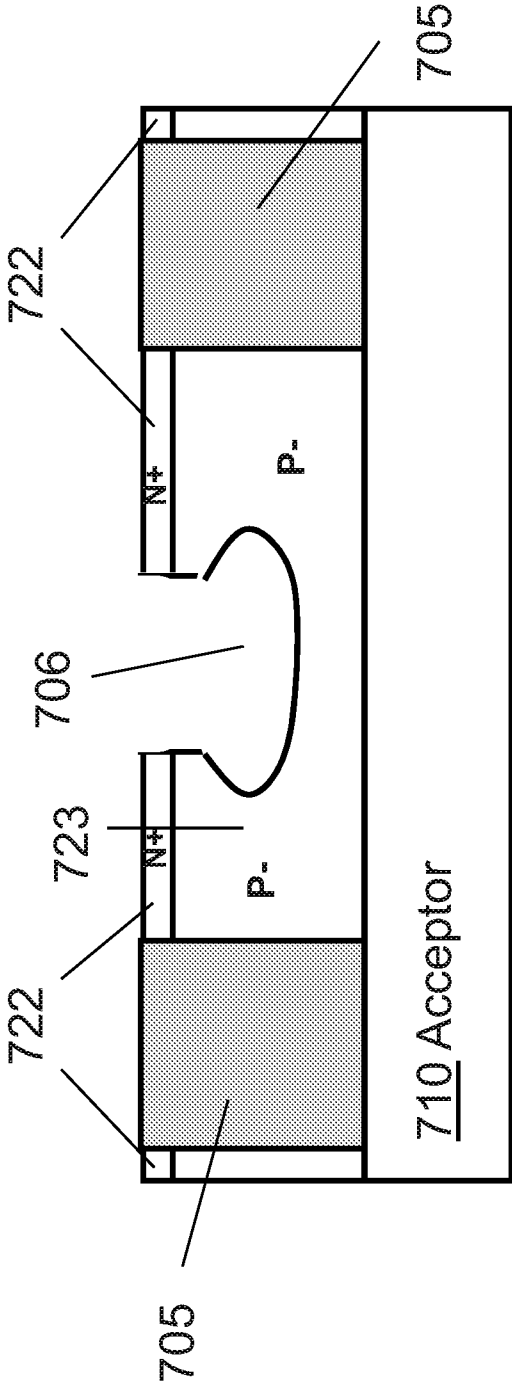


FIG. 7D





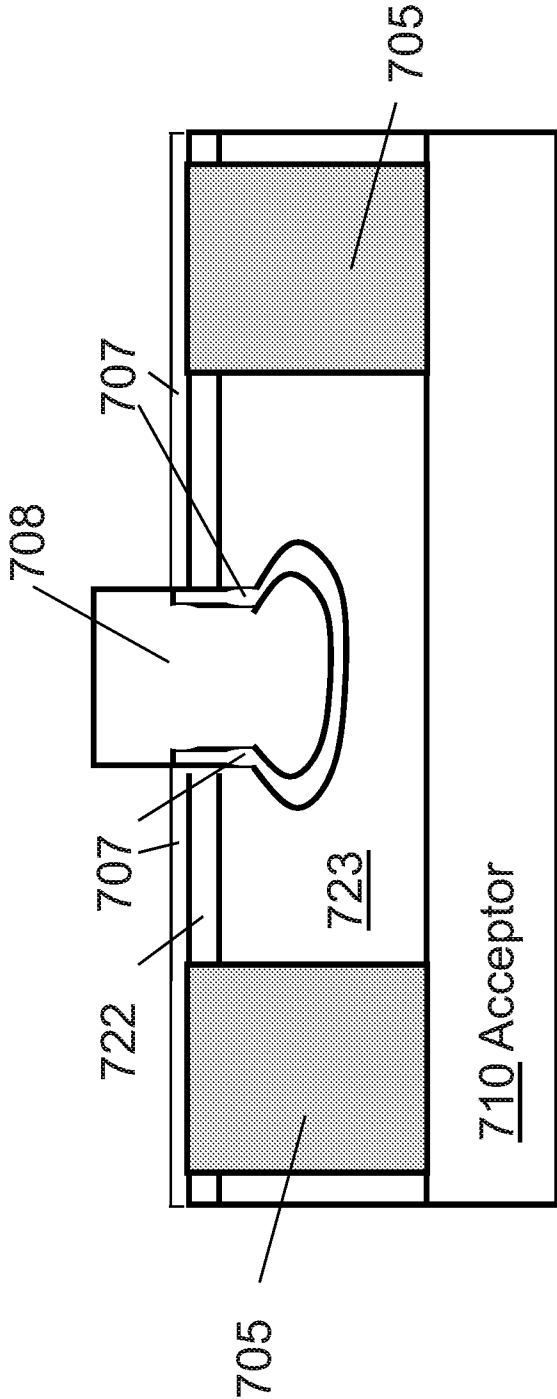


FIG. 7E

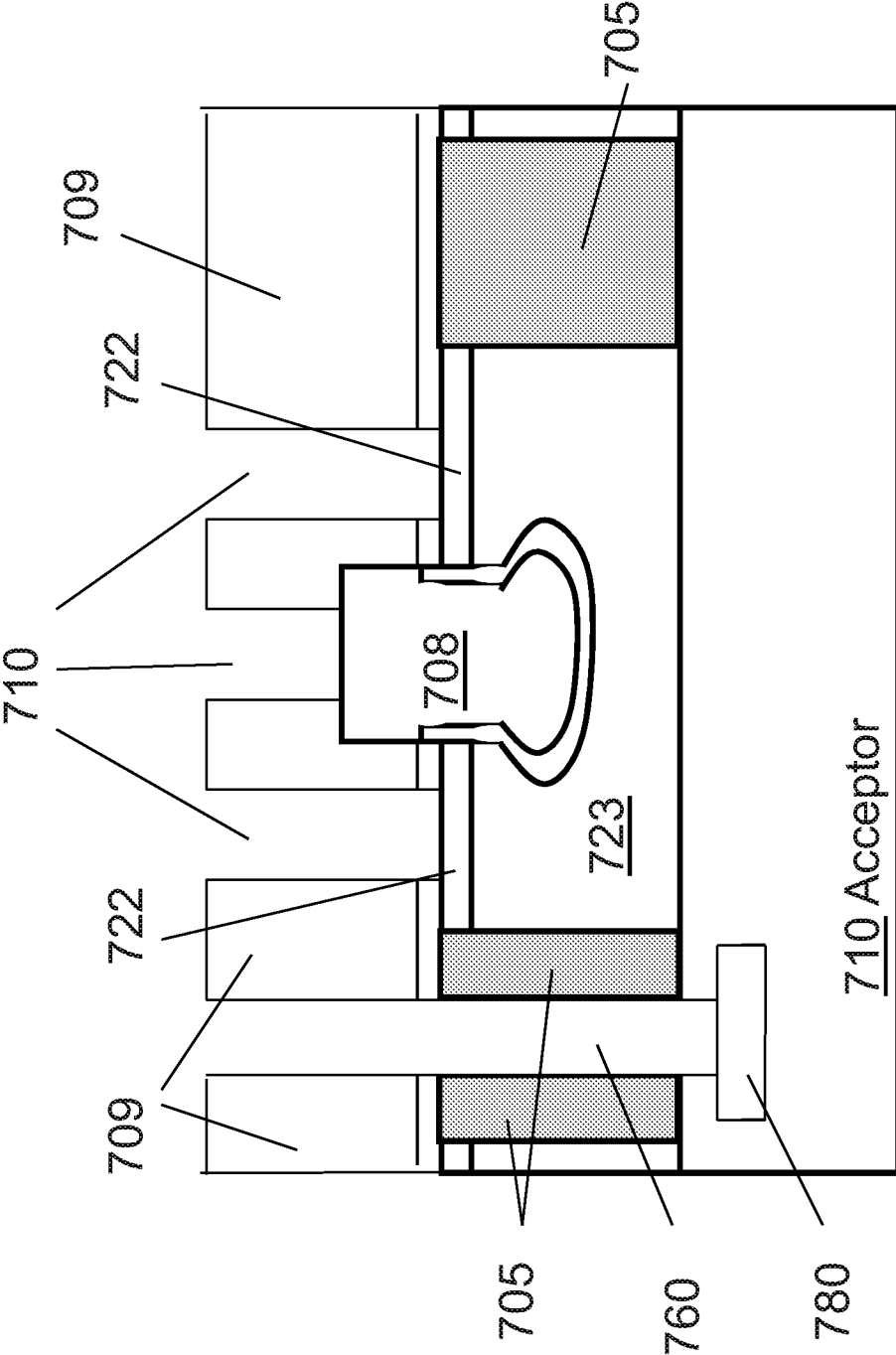
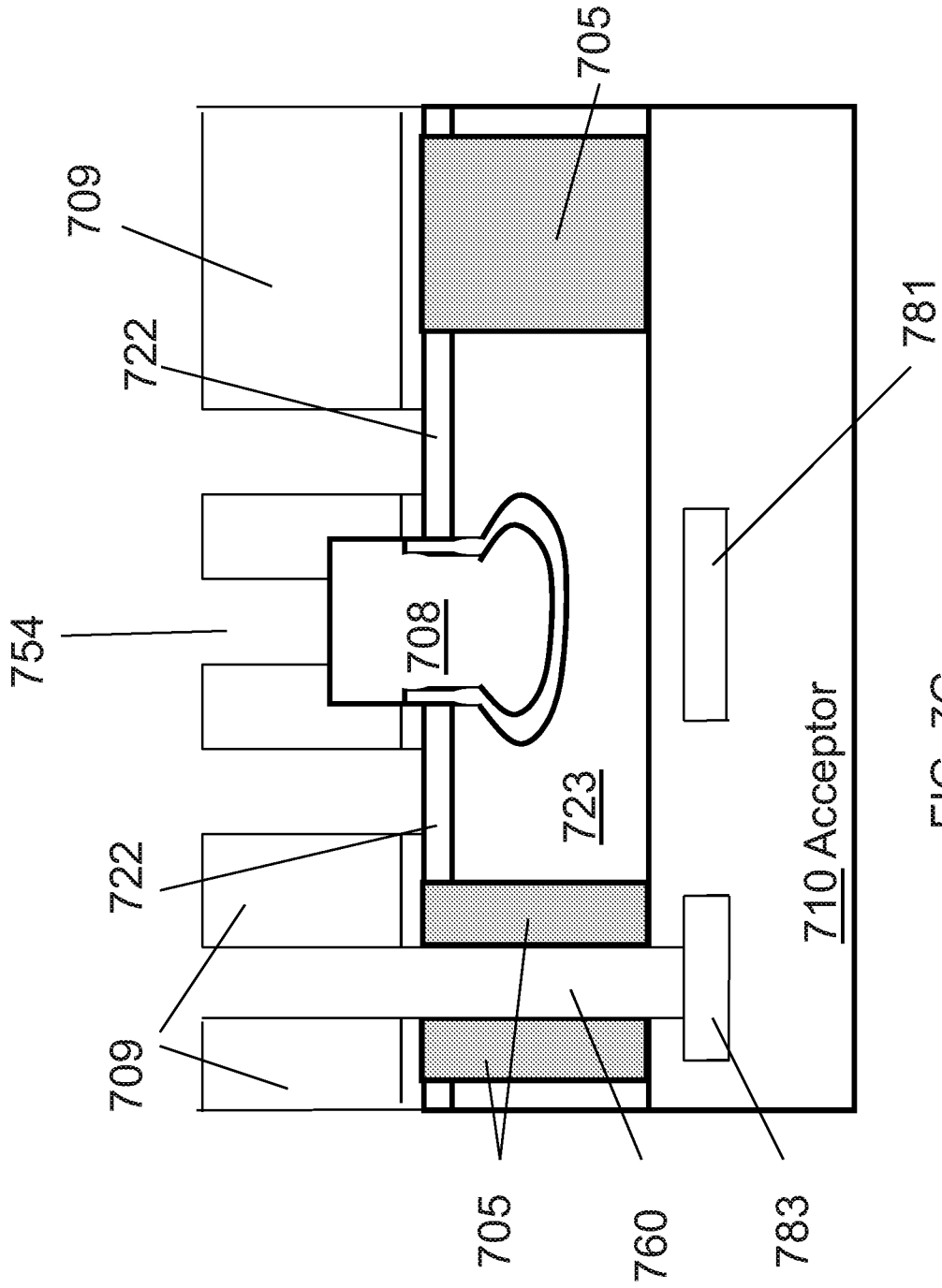
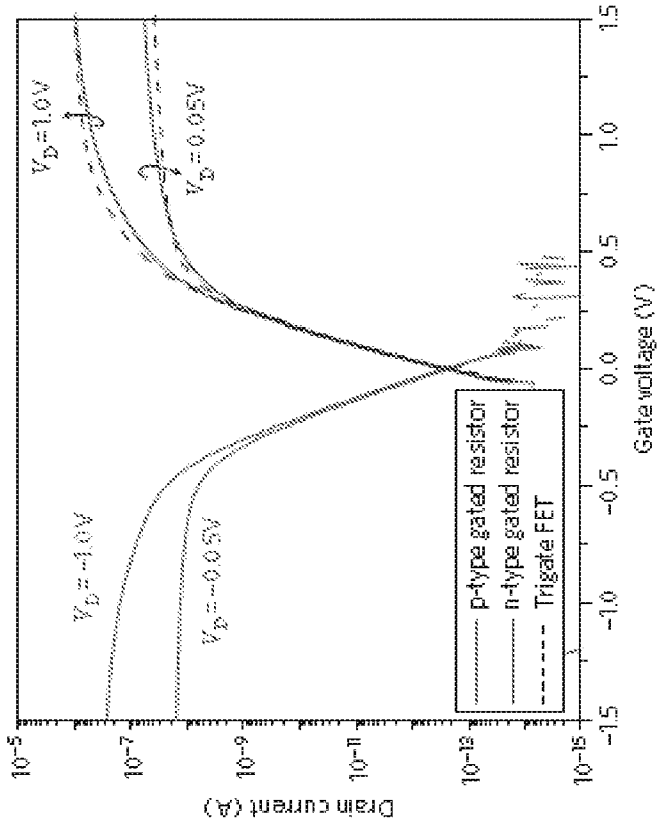
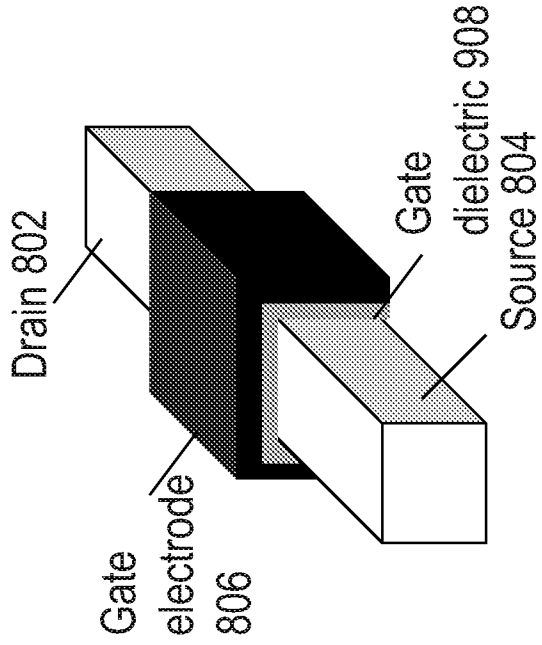


FIG. 7F





V<sub>D</sub> = drain voltage



Prior Art

Fig. 8

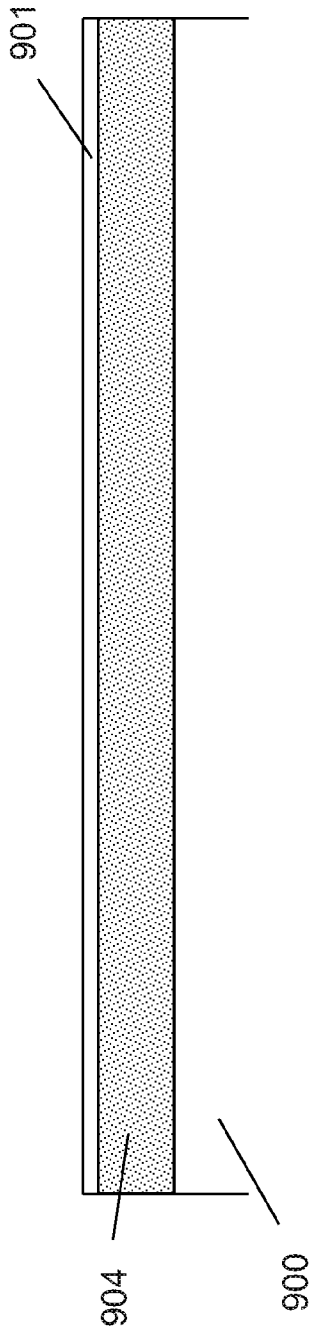


FIG. 9A

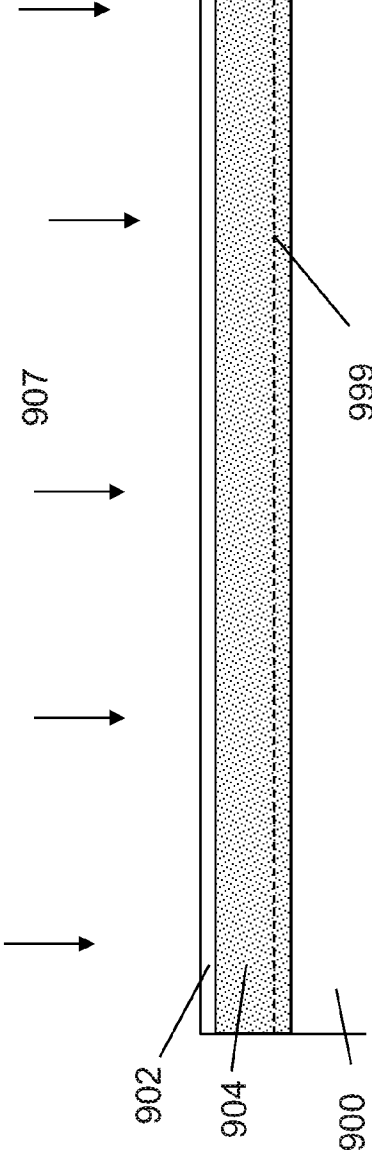


FIG. 9B

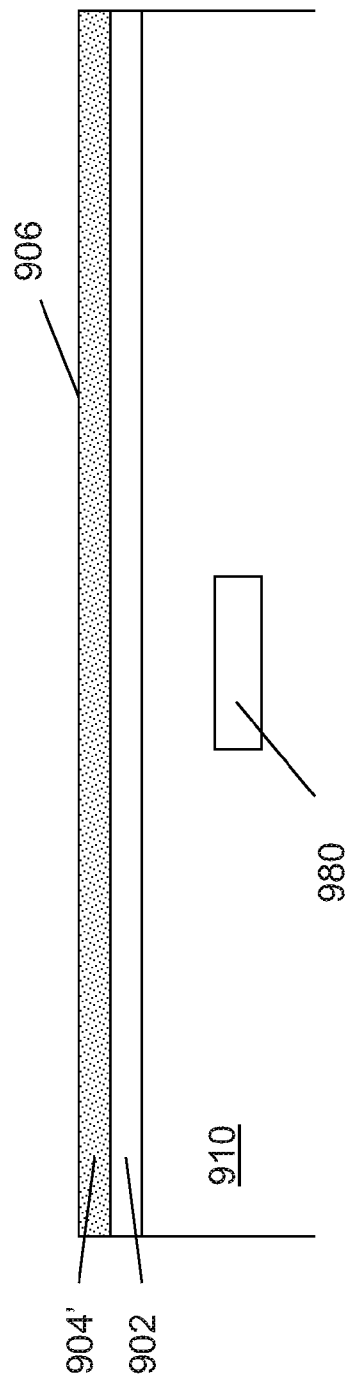


FIG. 9C

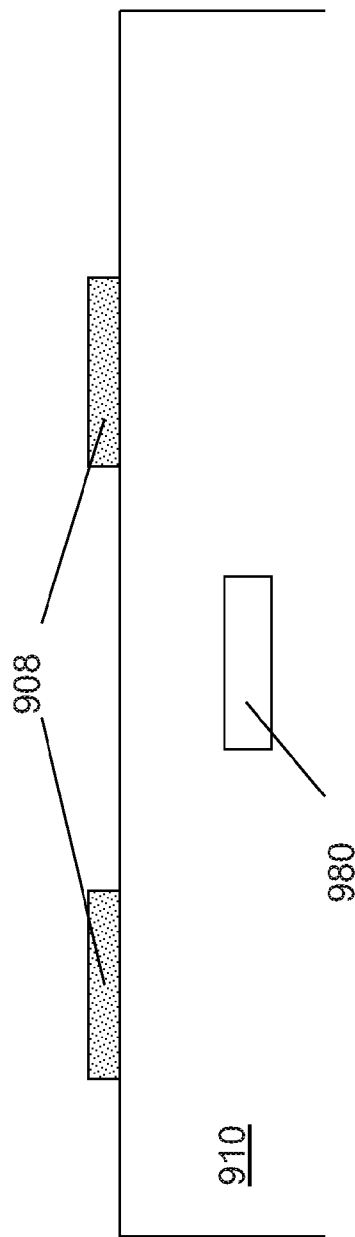


FIG. 9D

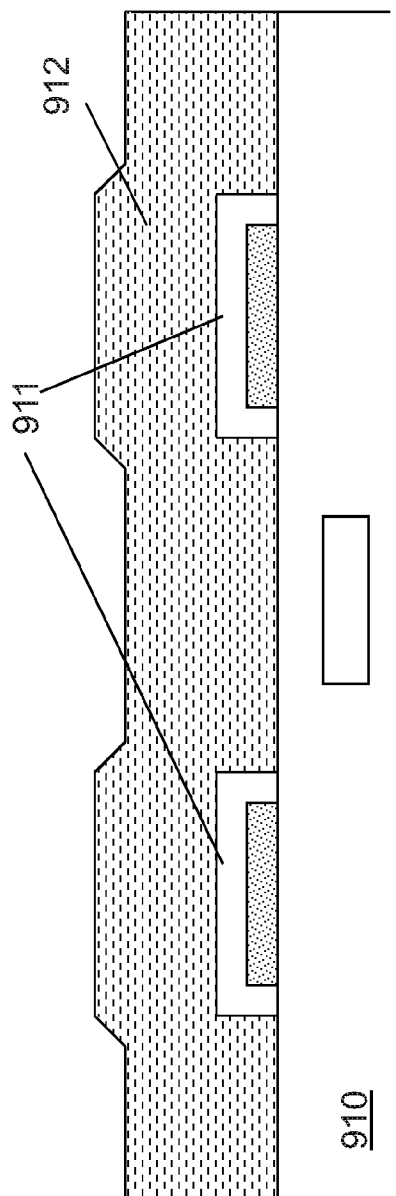


FIG. 9E

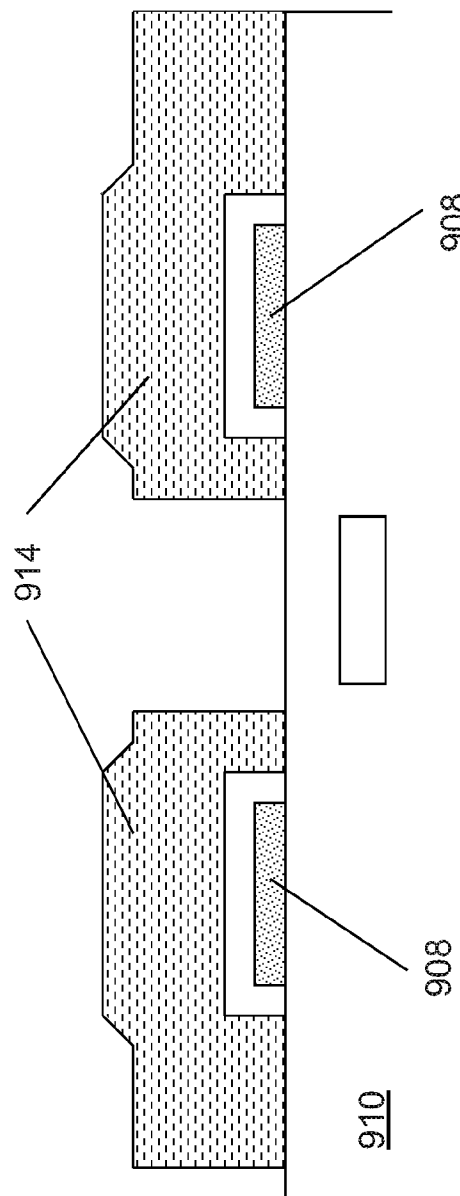


FIG. 9F

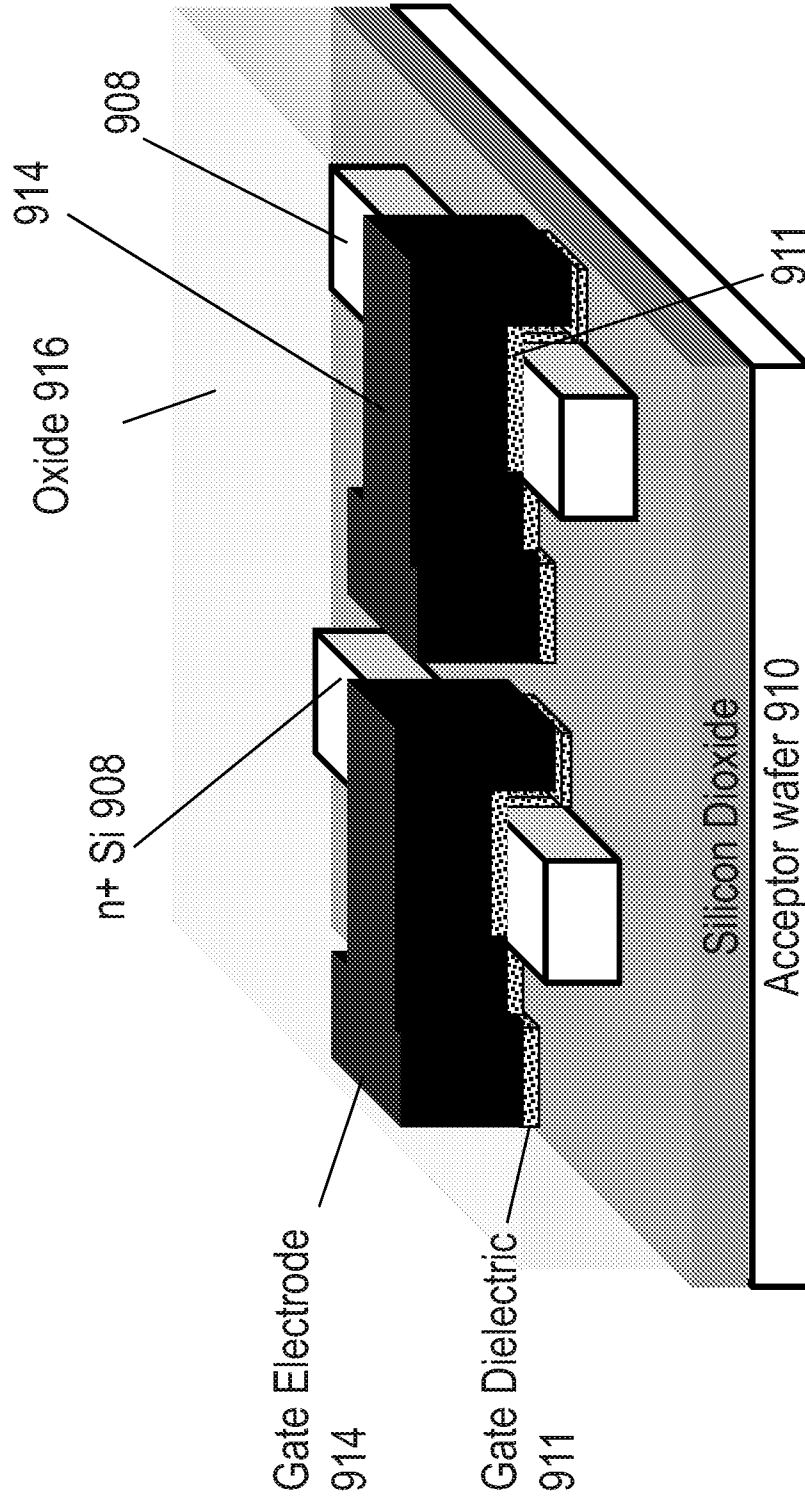


FIG. 9G



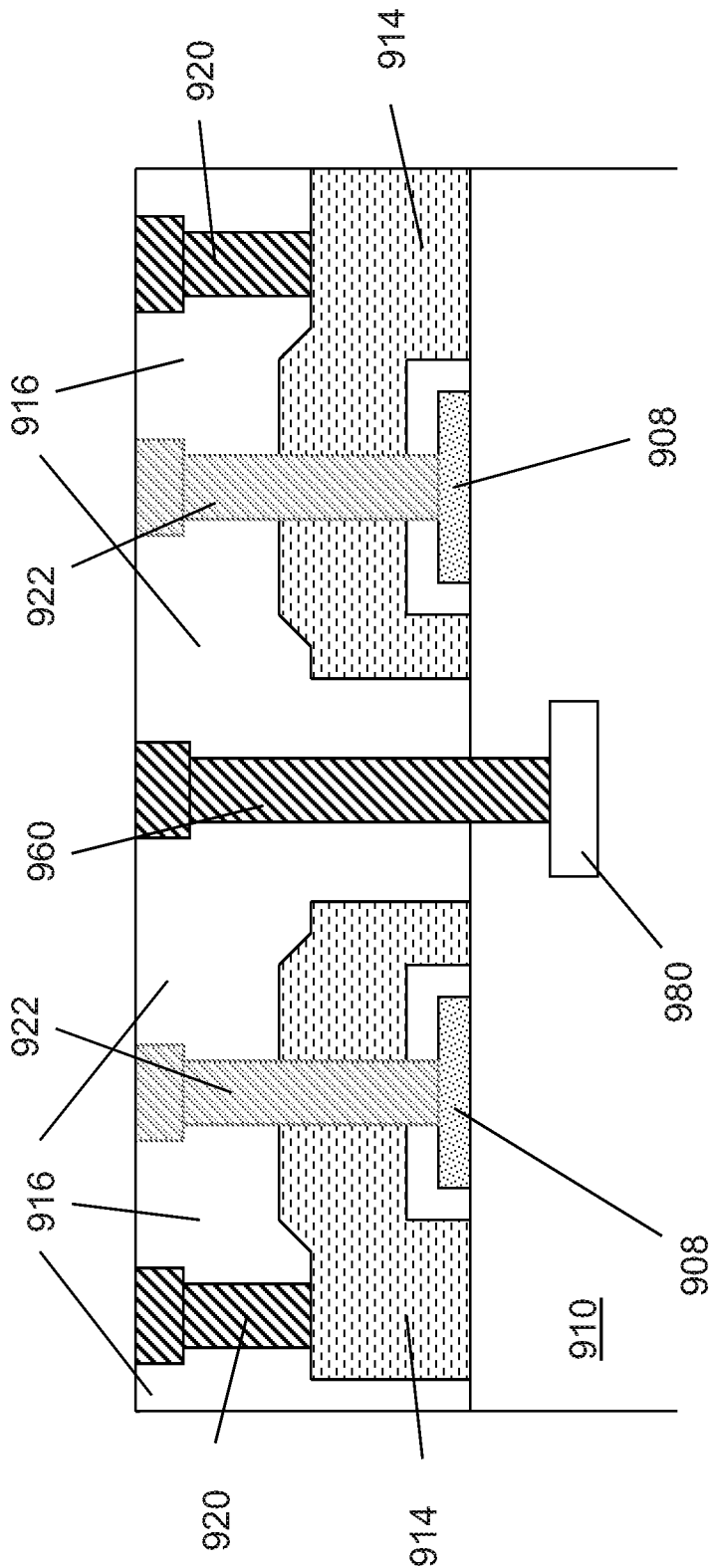


FIG. 9H

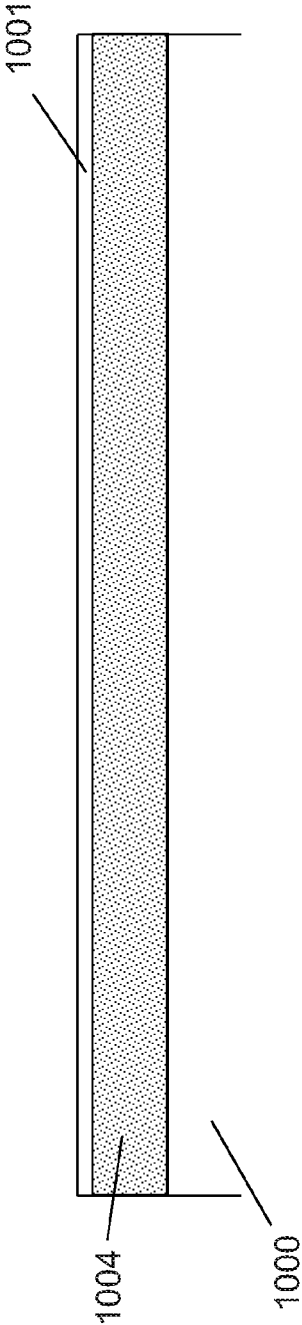


FIG. 10A

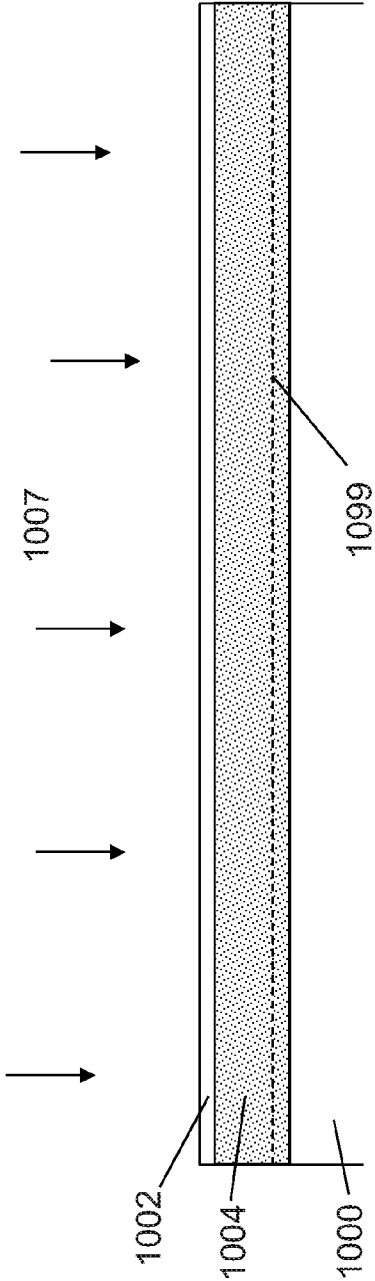


FIG. 10B

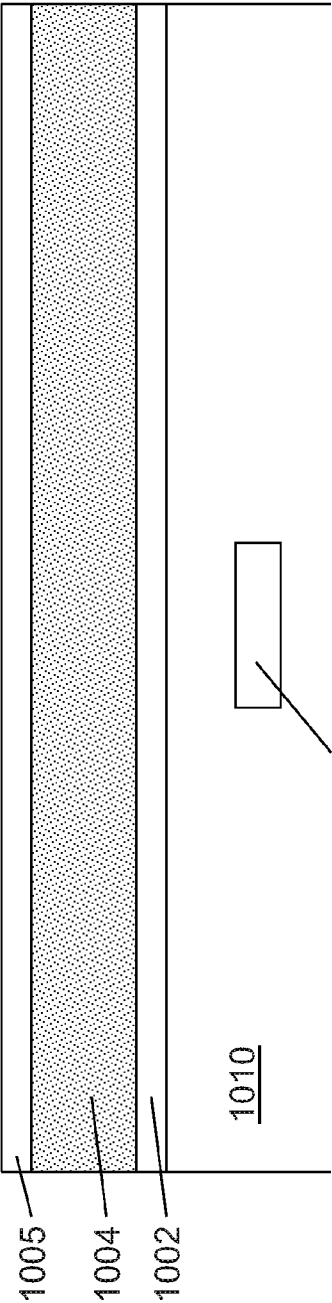


FIG. 10C

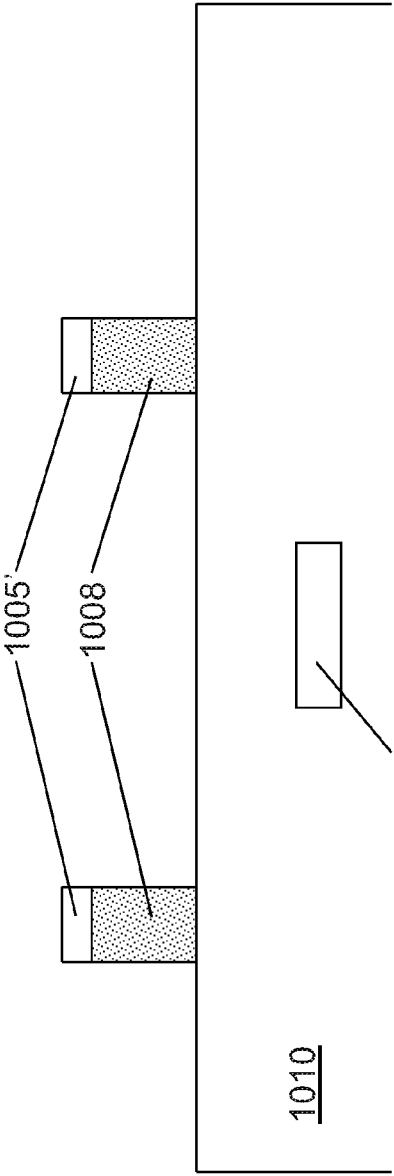


FIG. 10D

FIG. 10E

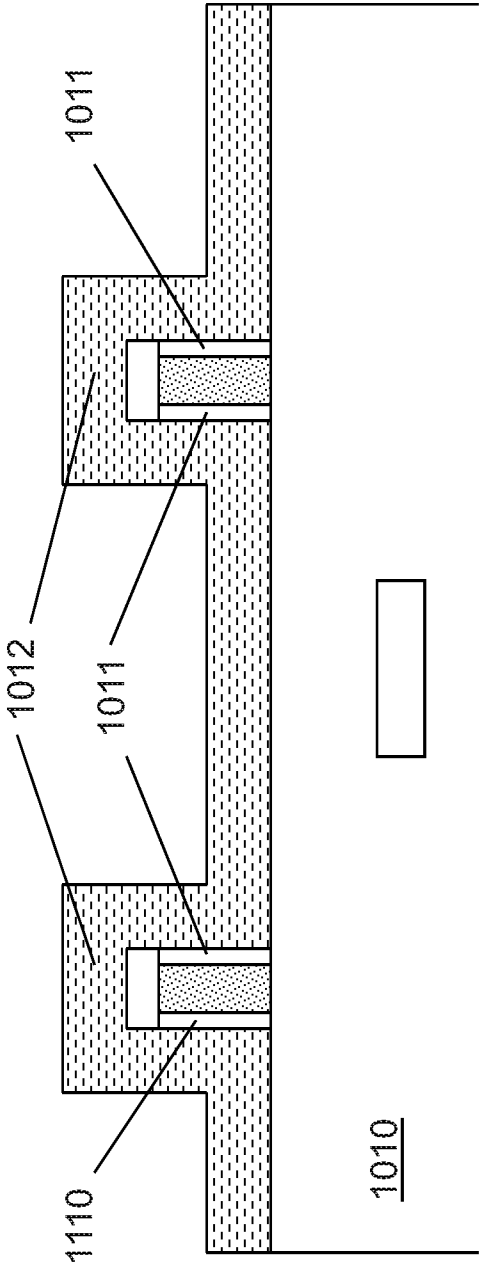
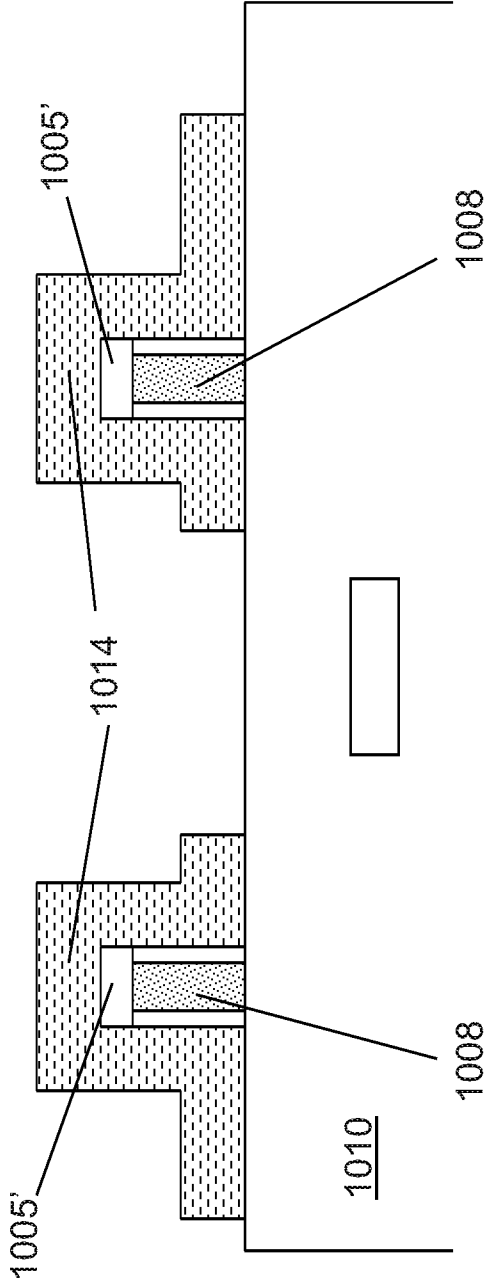


FIG. 10F



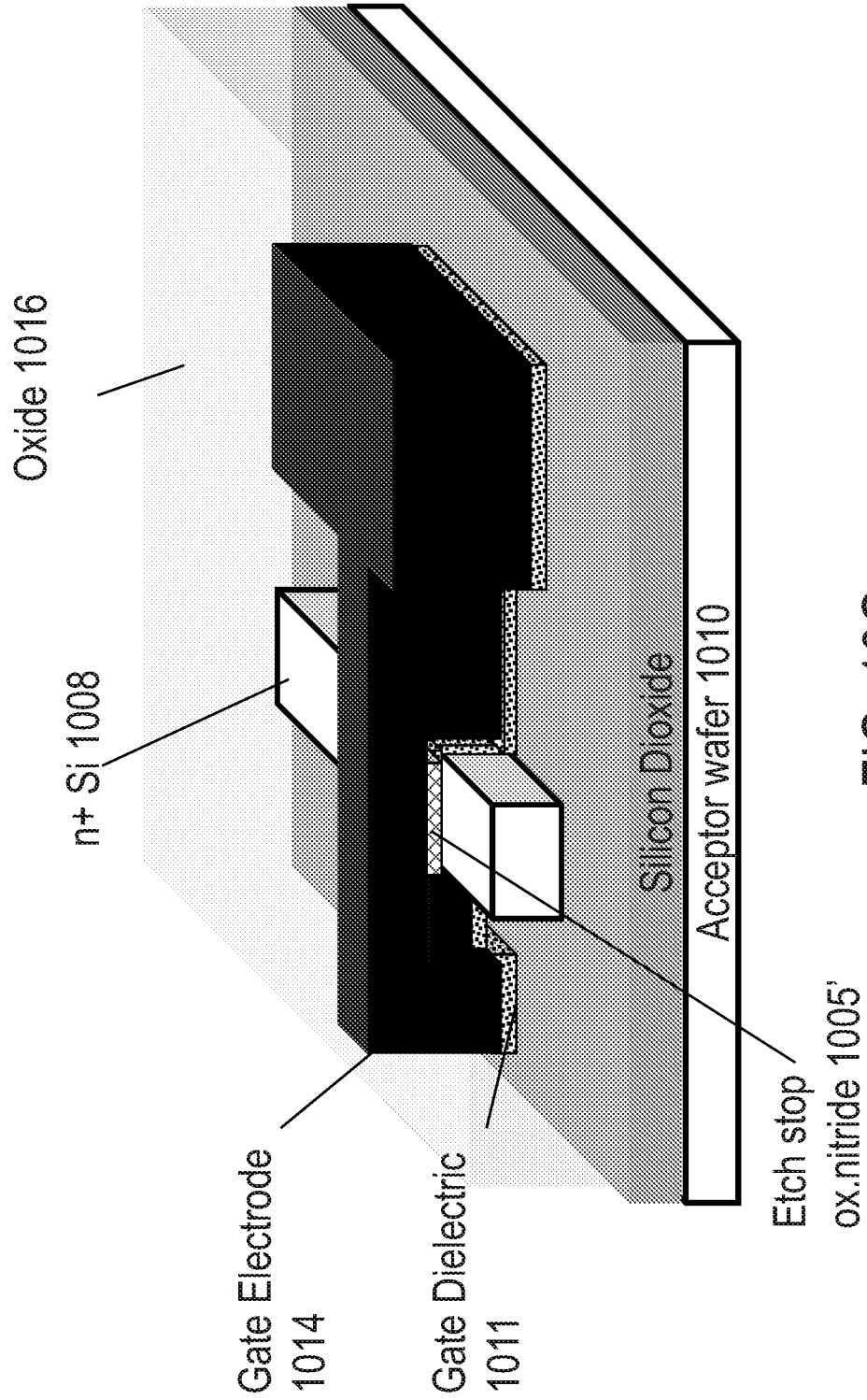


FIG. 10G

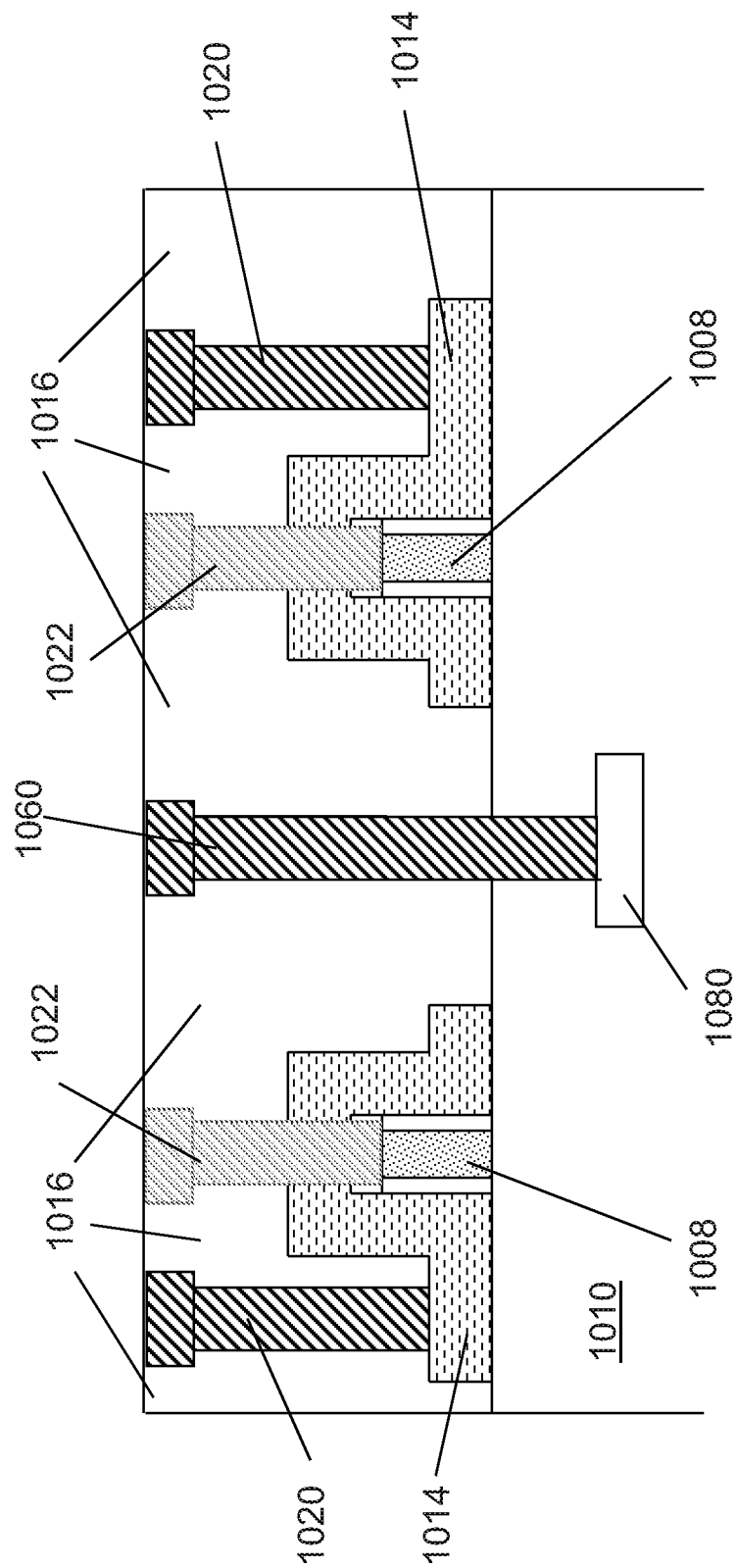


FIG. 10H

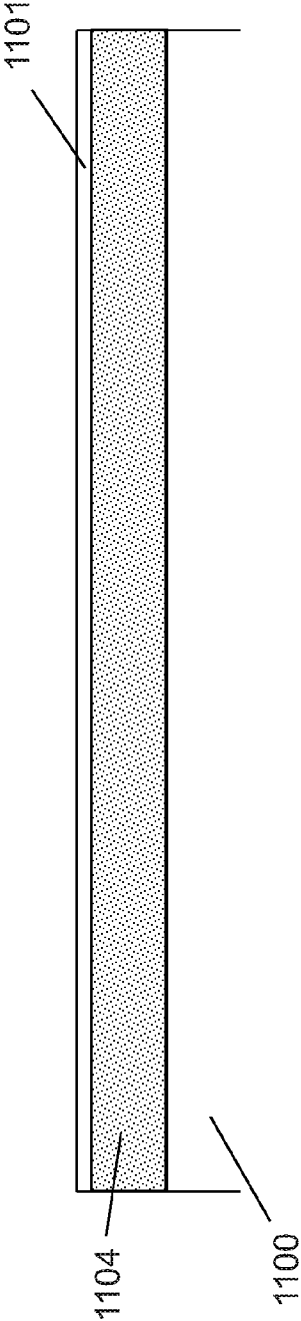


FIG. 11A

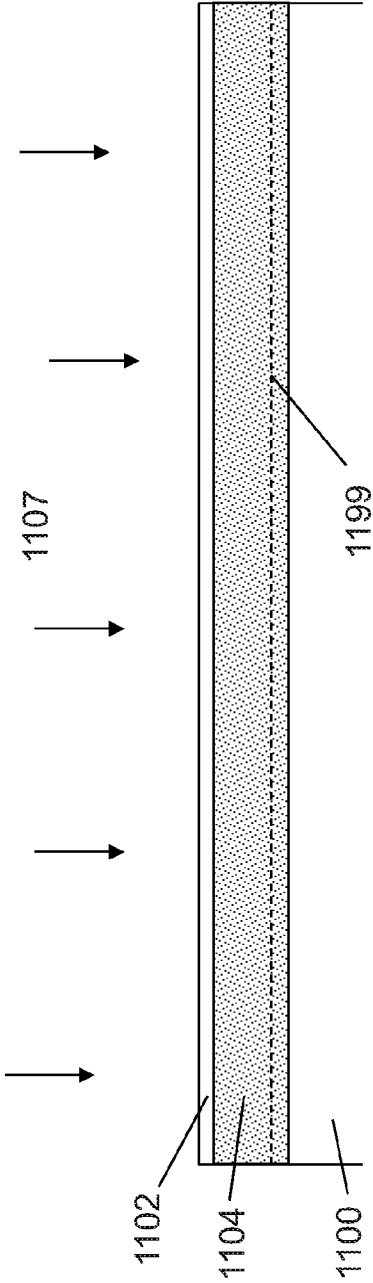


FIG. 11B



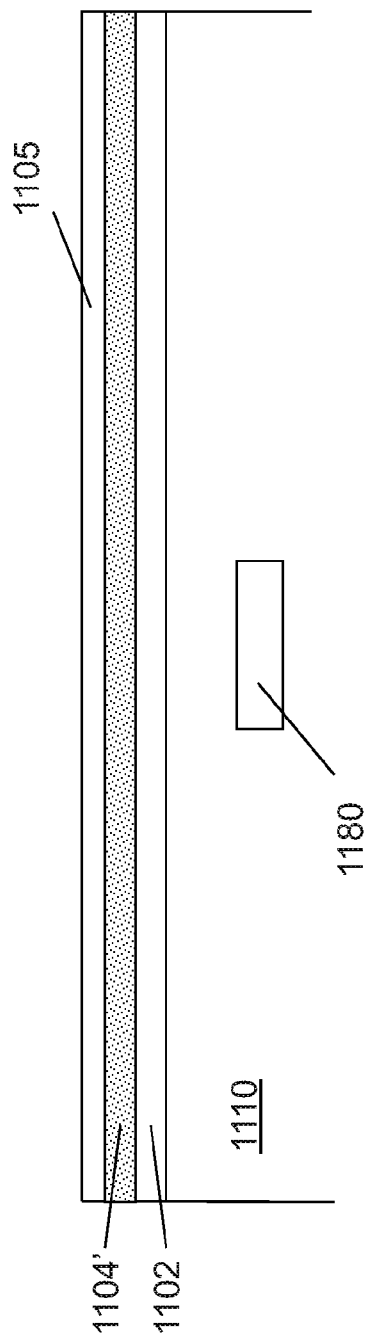


FIG. 11C

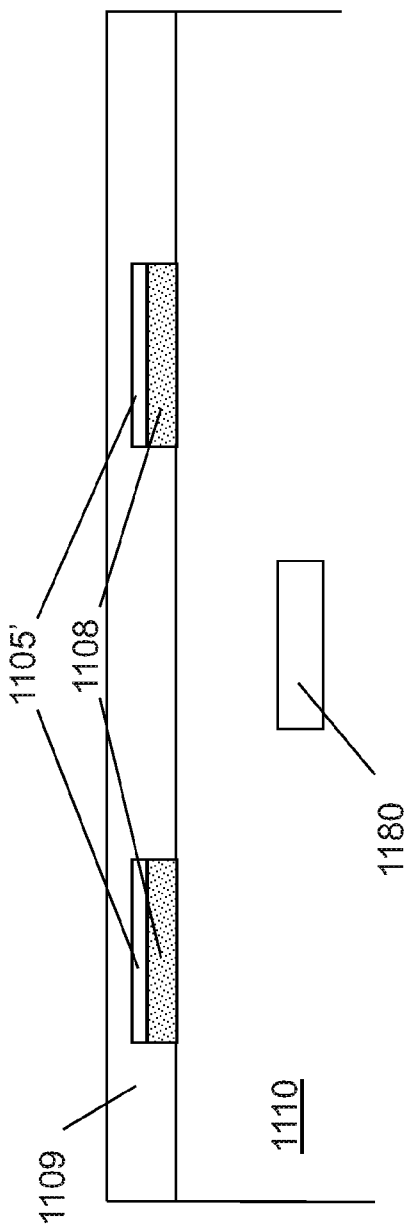


FIG. 11D

FIG. 11E

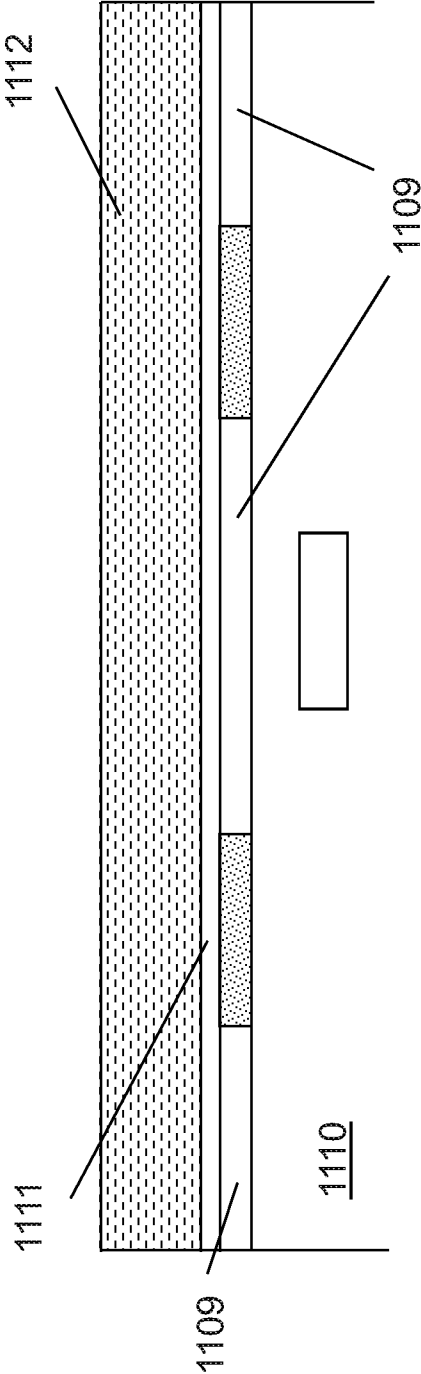
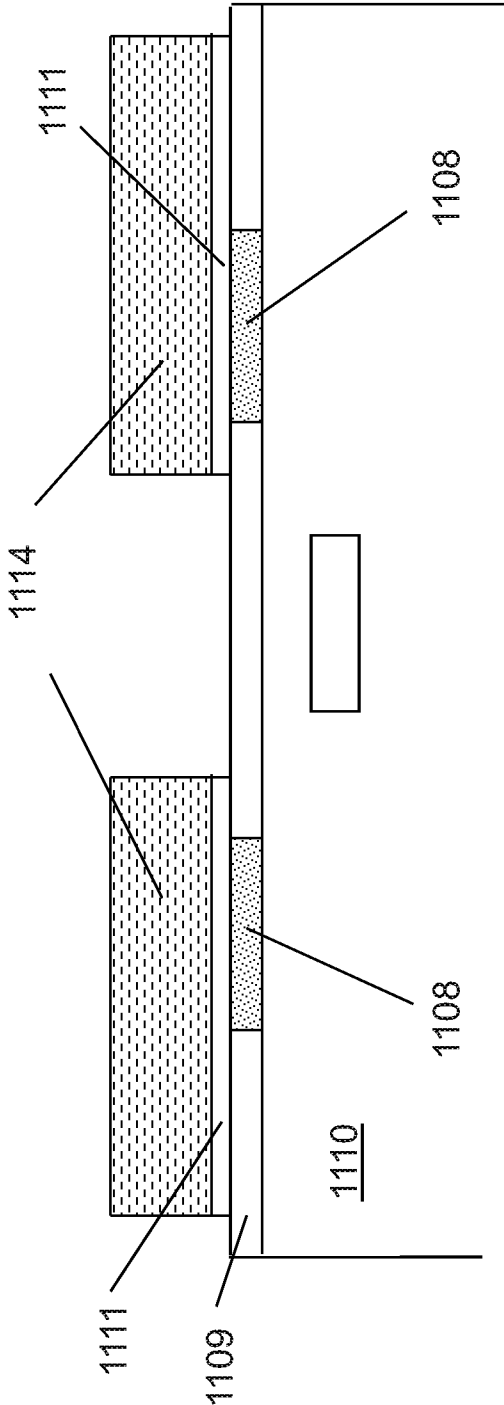


FIG. 11F



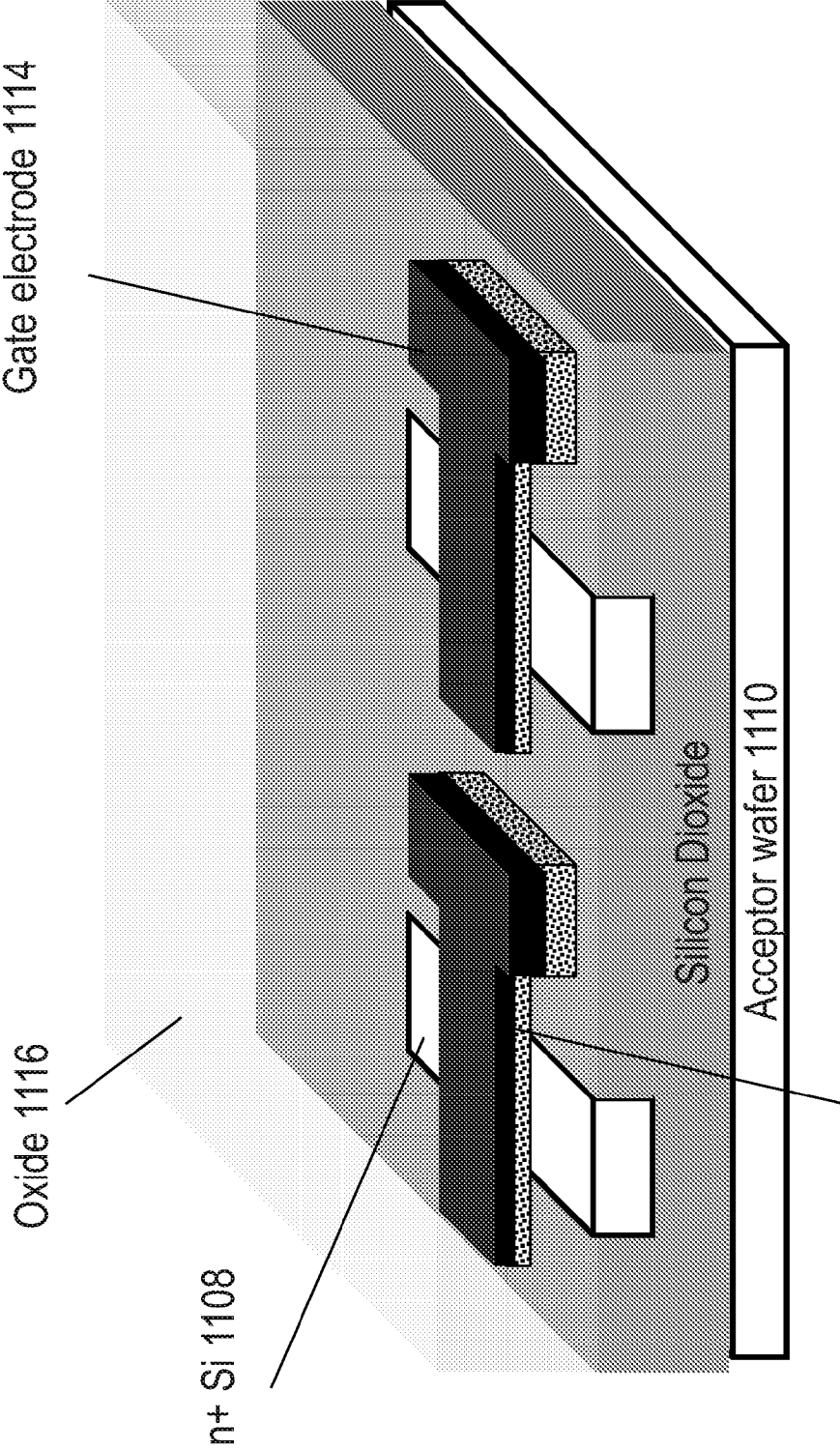


FIG. 11G

Gate dielectric 1111

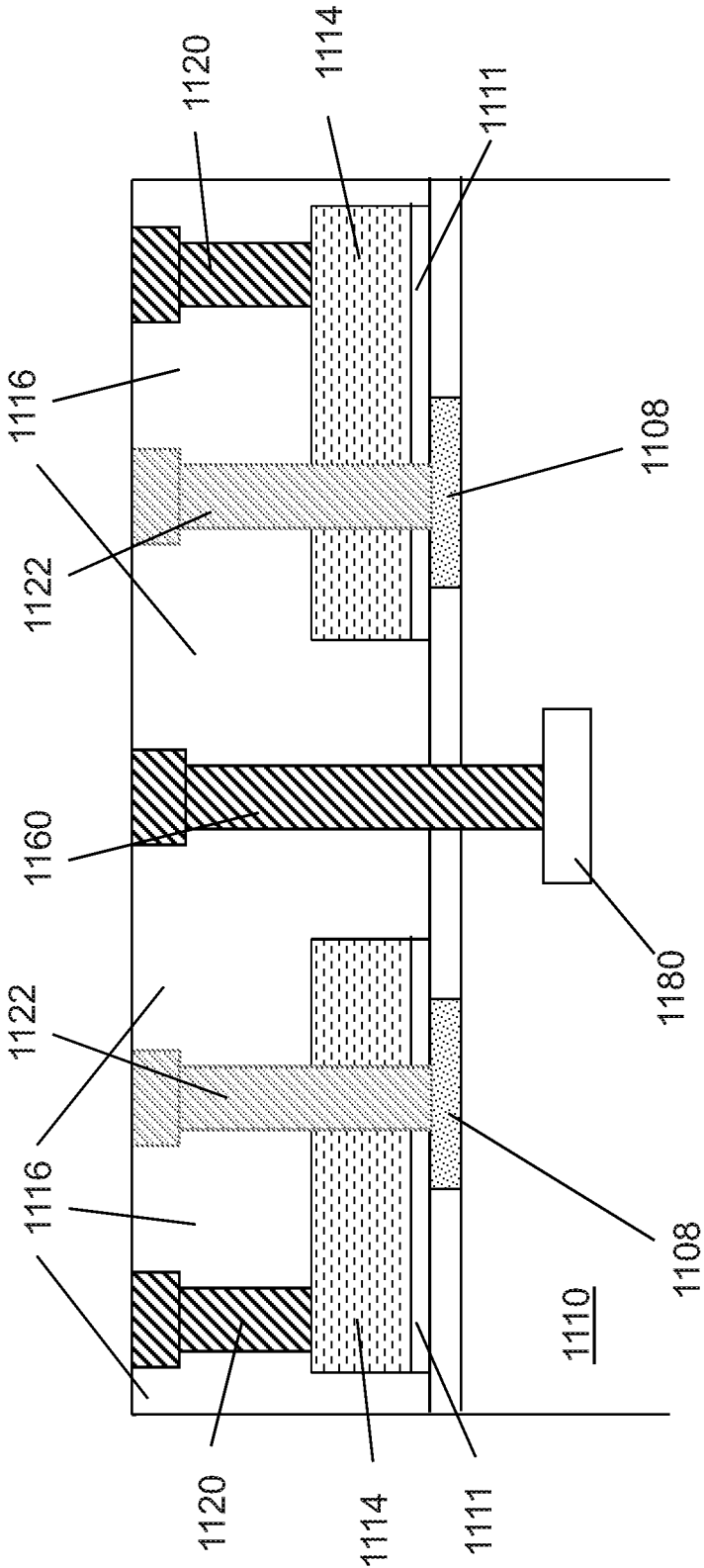


FIG. 11H

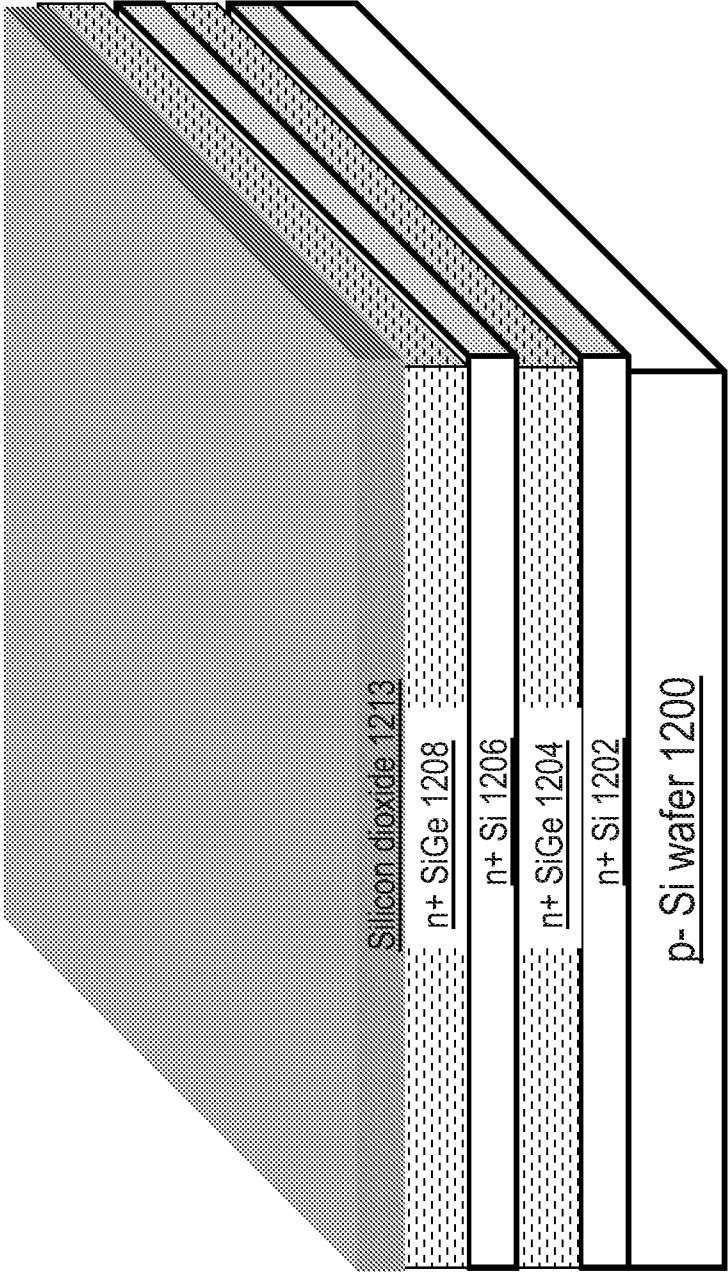


FIG. 12A

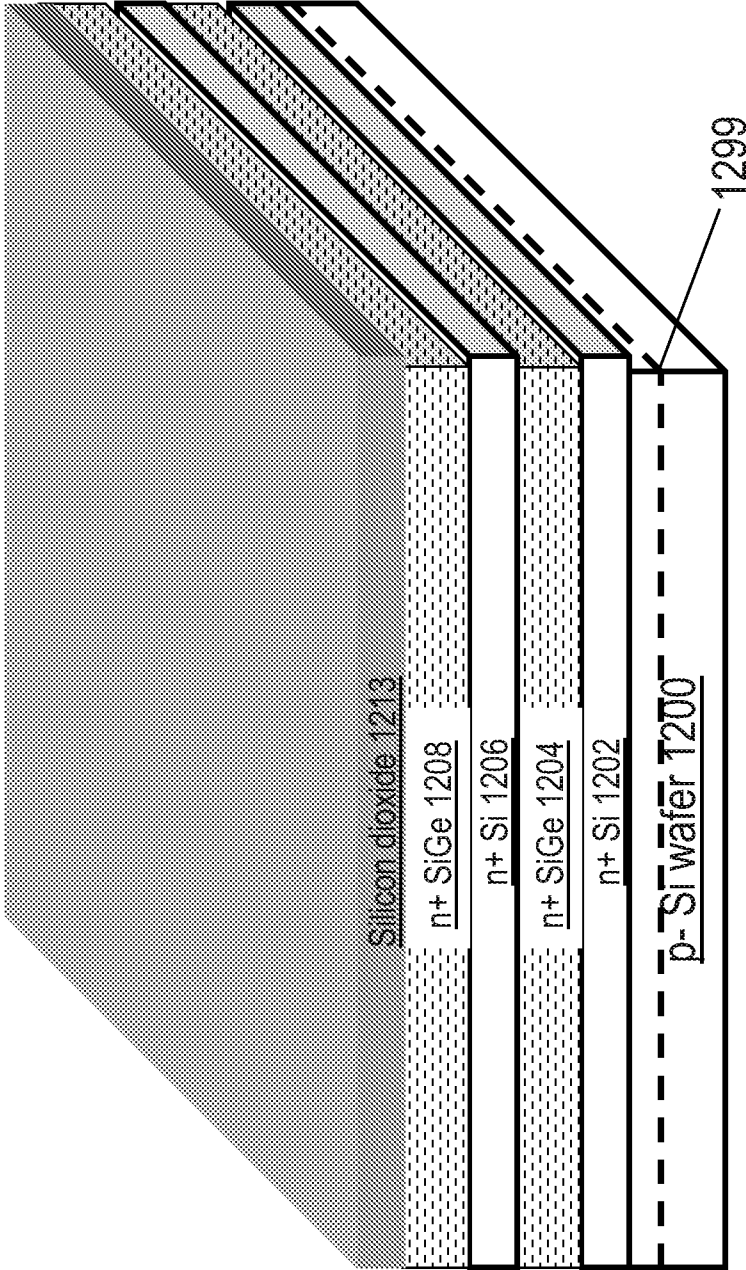


FIG. 12B

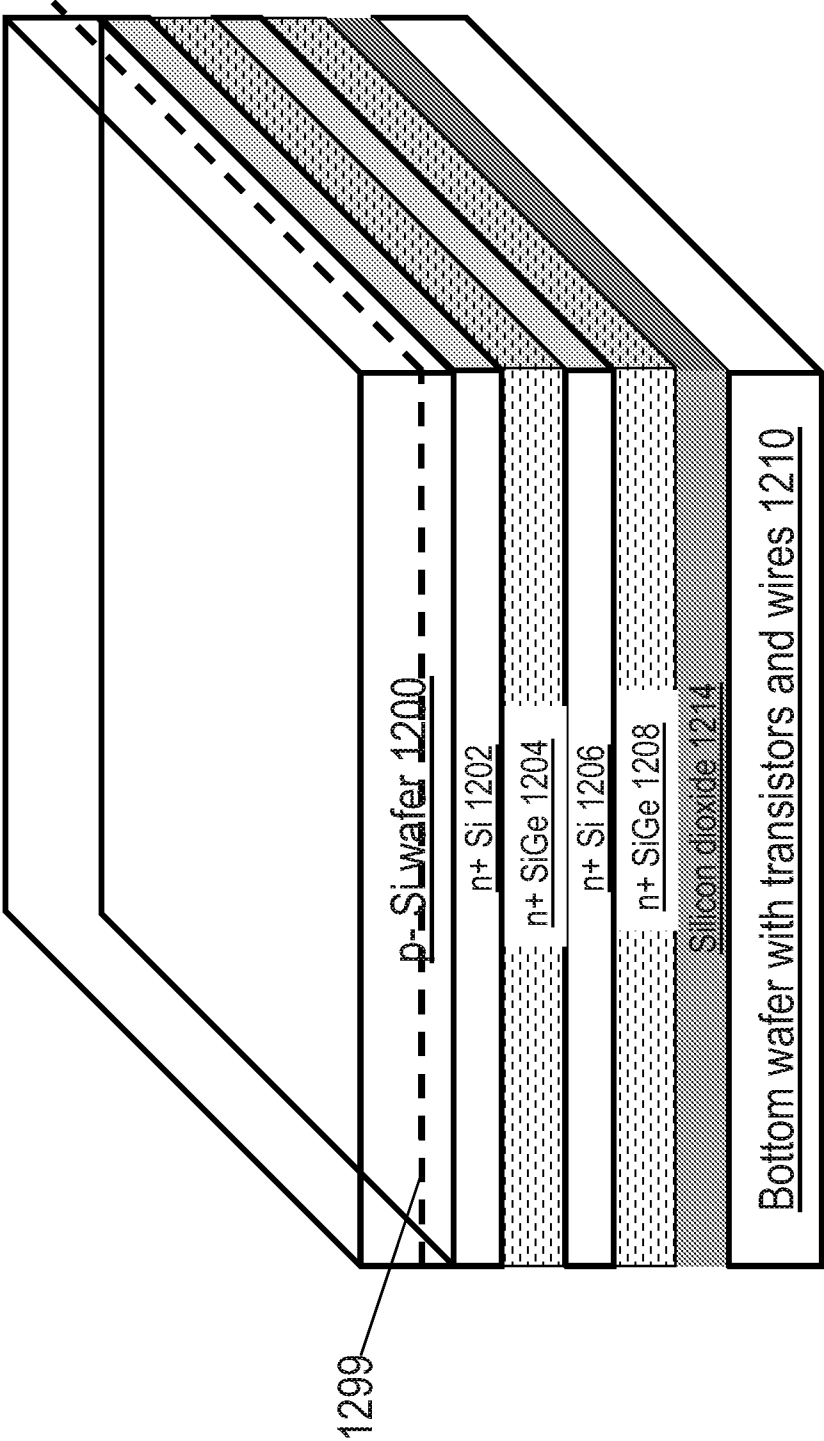


FIG. 12C



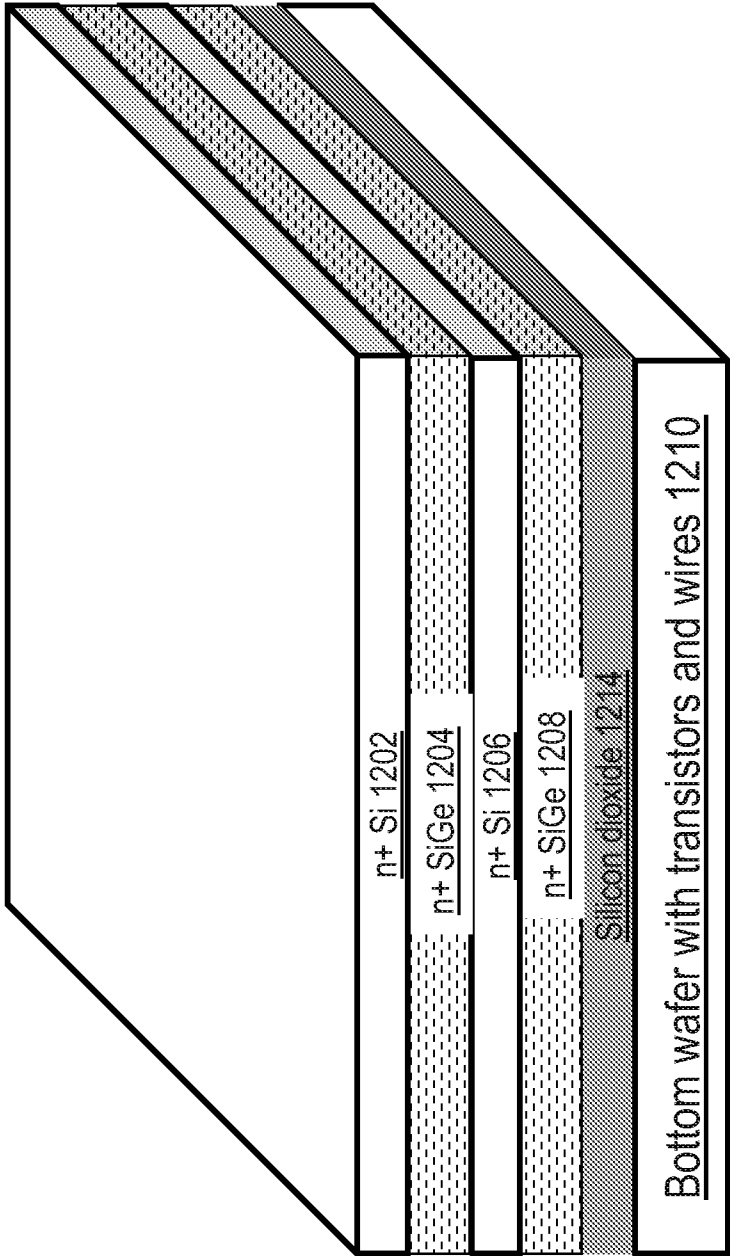


FIG. 12D

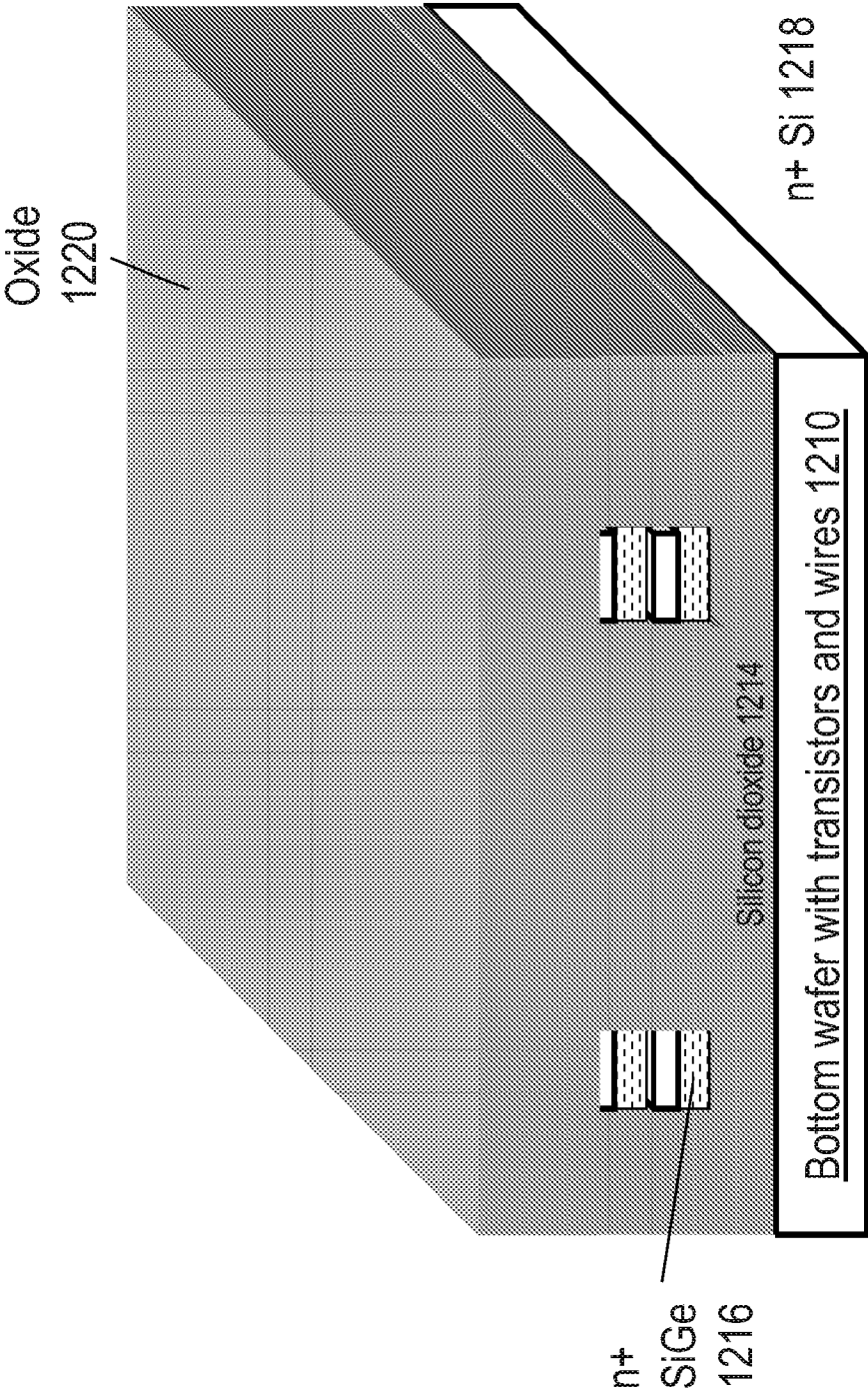


FIG. 12E

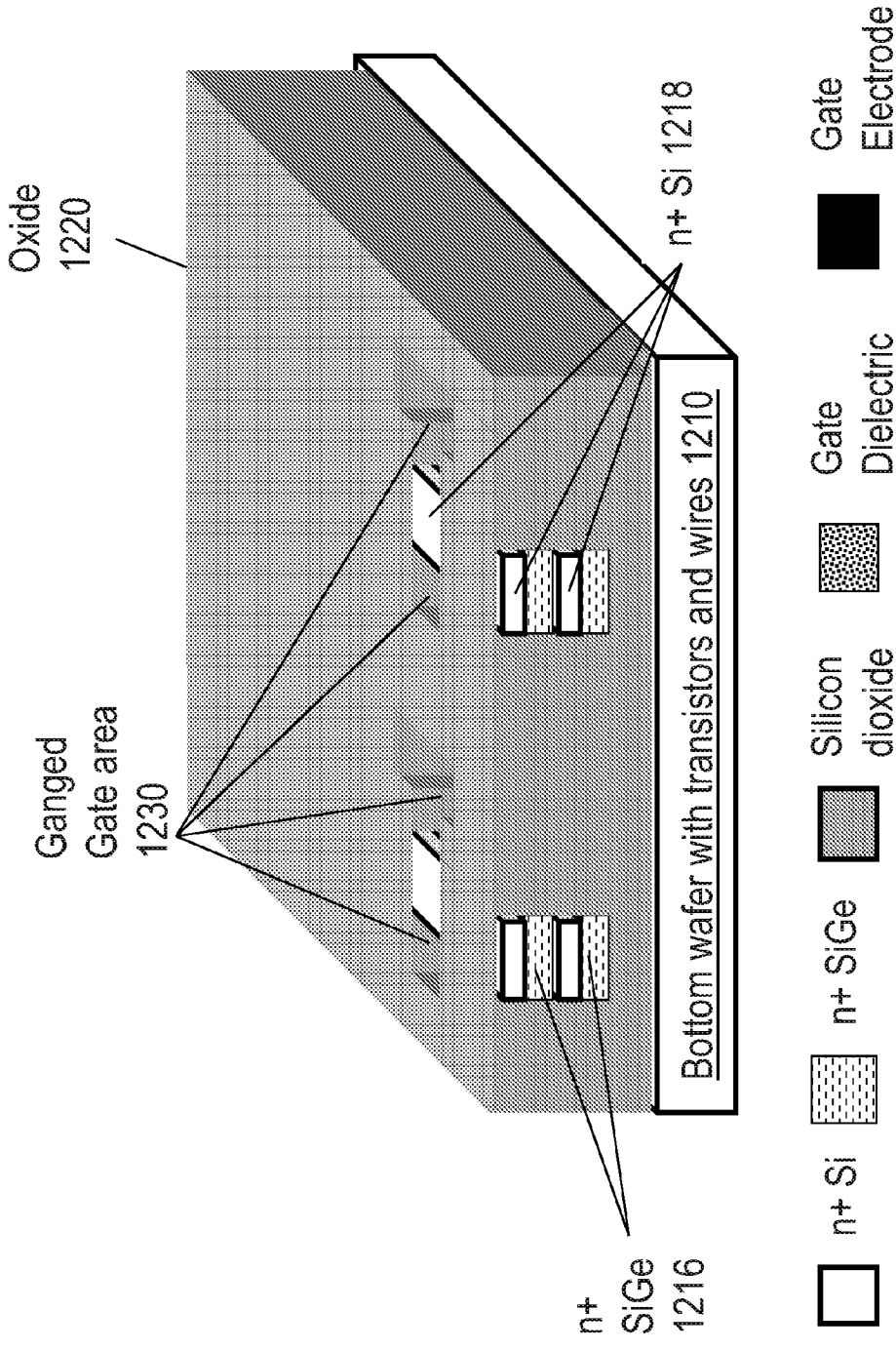


FIG. 12F

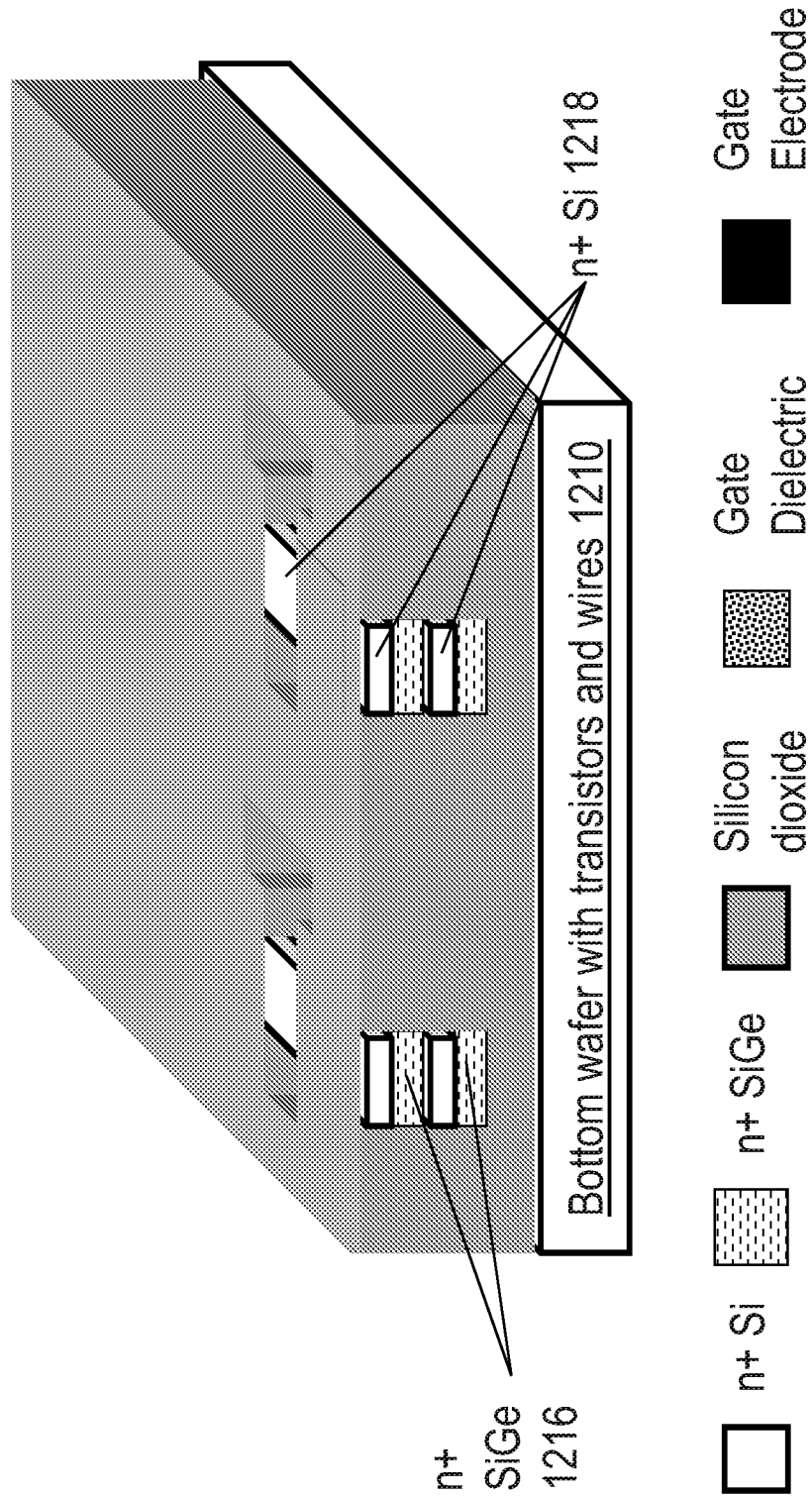


FIG. 12G

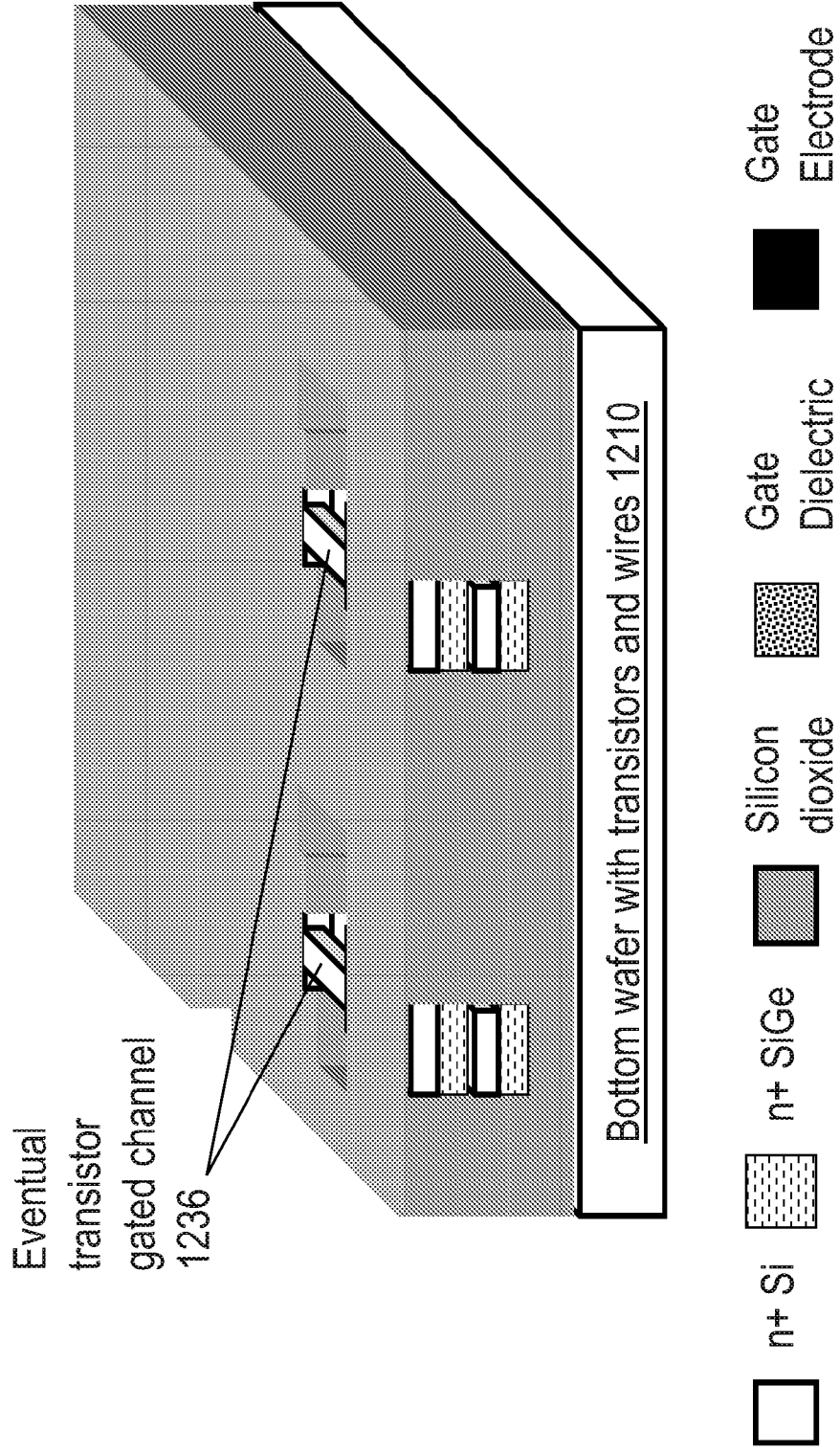


FIG. 12H

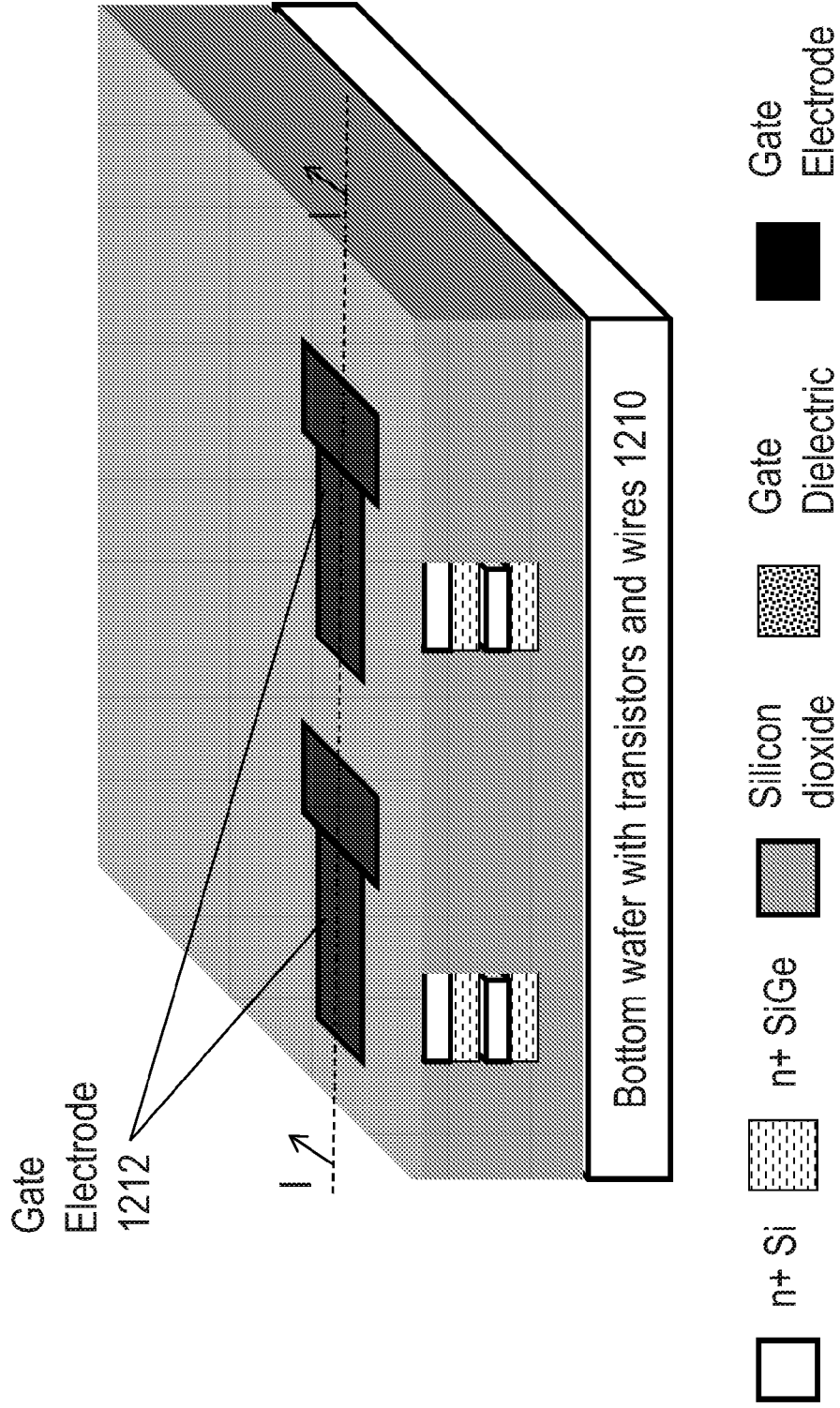


FIG. 12I

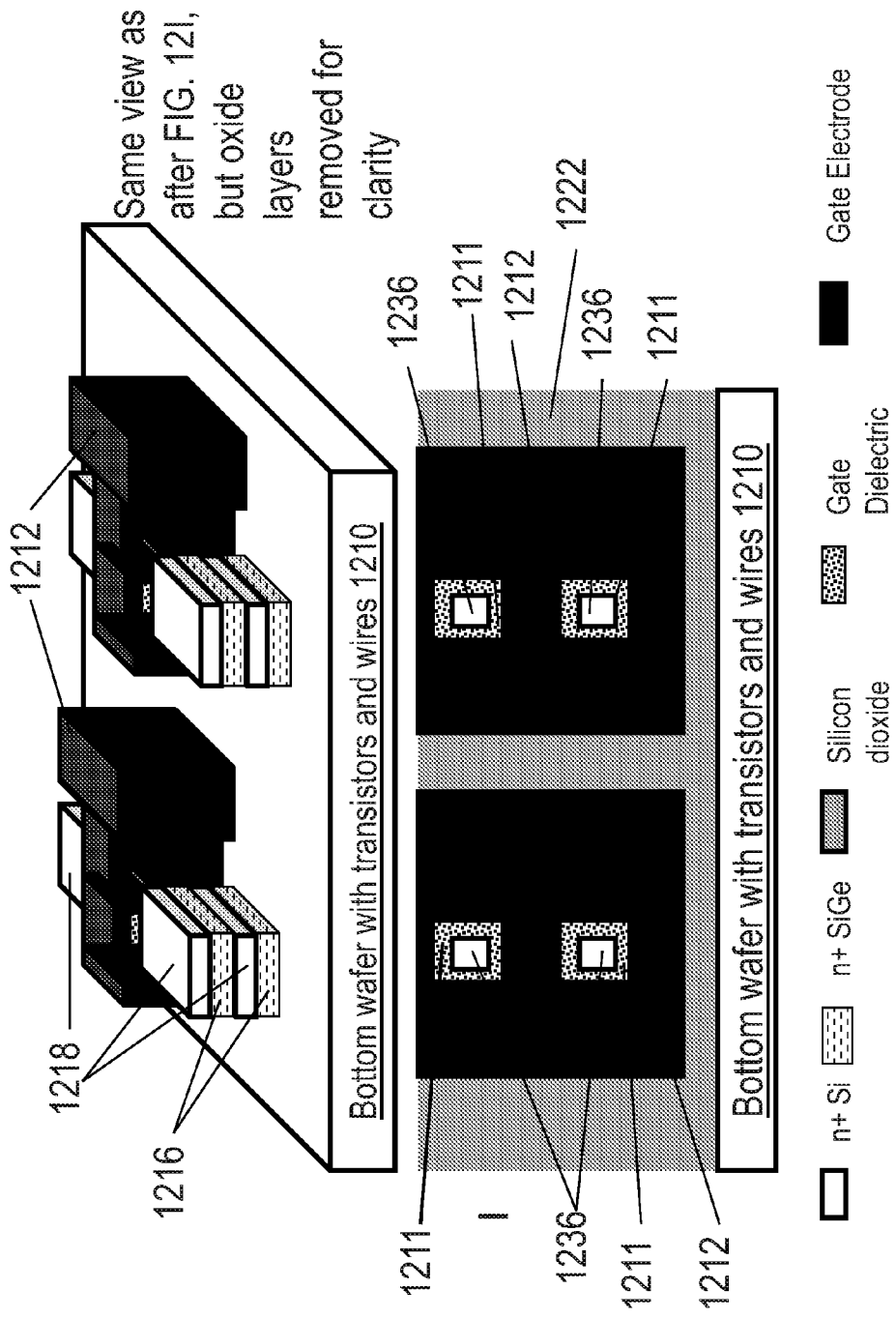


FIG. 12J

Single Gated N+ Resistor with P+ gate, Gate-ox = 10nm, Channel Length = 1 $\mu$ m; D (Depth) = 20nm

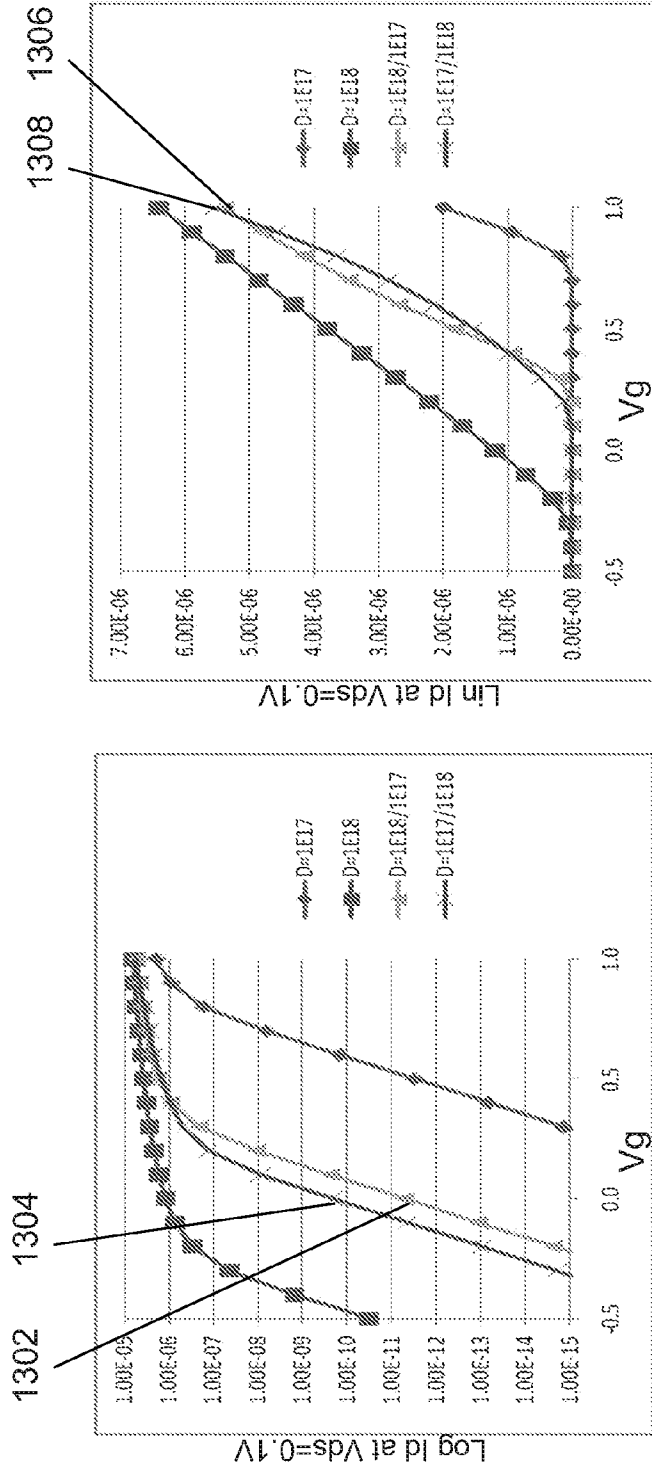


FIG. 13B

FIG. 13A



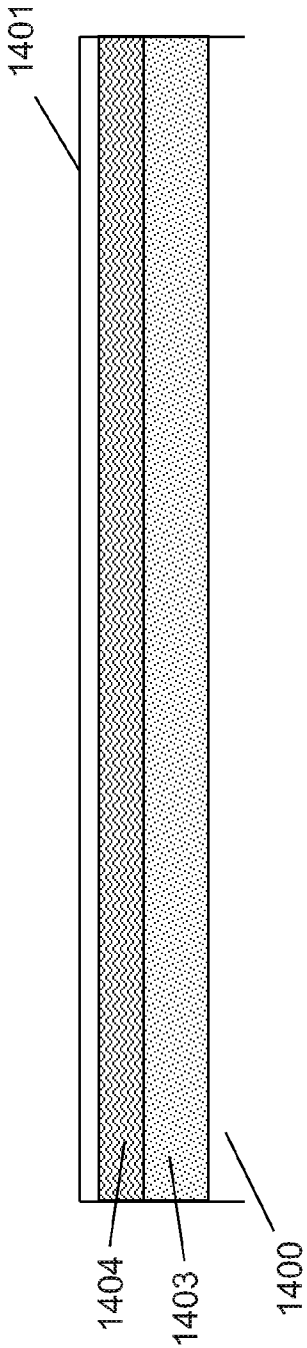


FIG. 14A

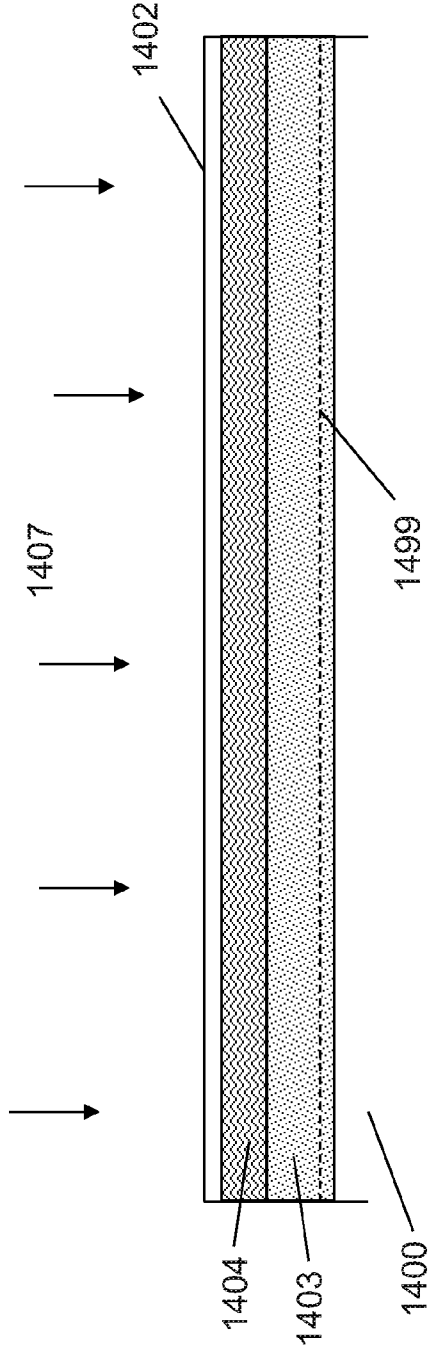


FIG. 14B

FIG. 14C

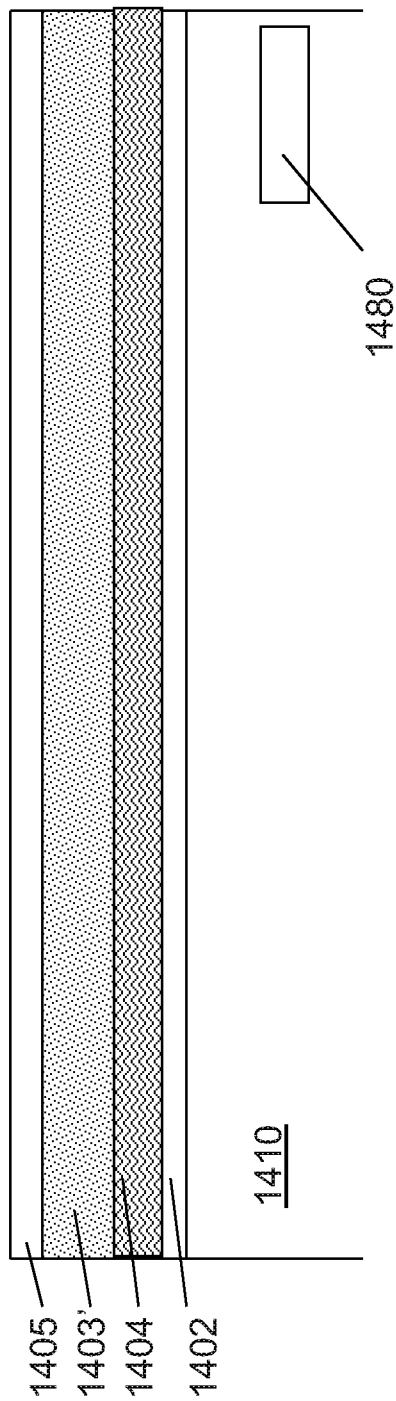


FIG. 14D

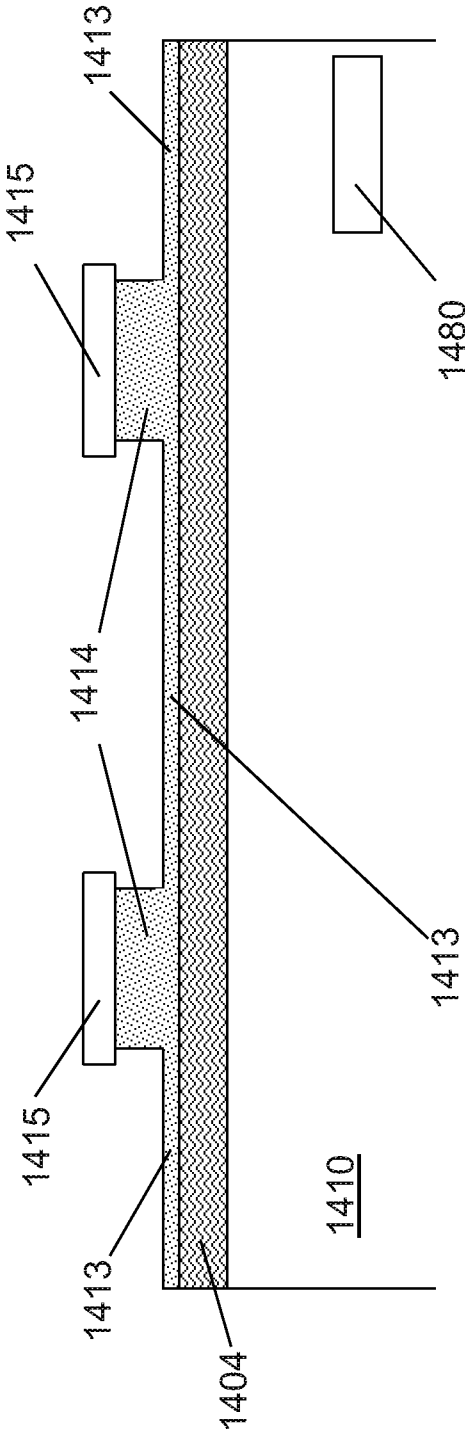


FIG. 14E

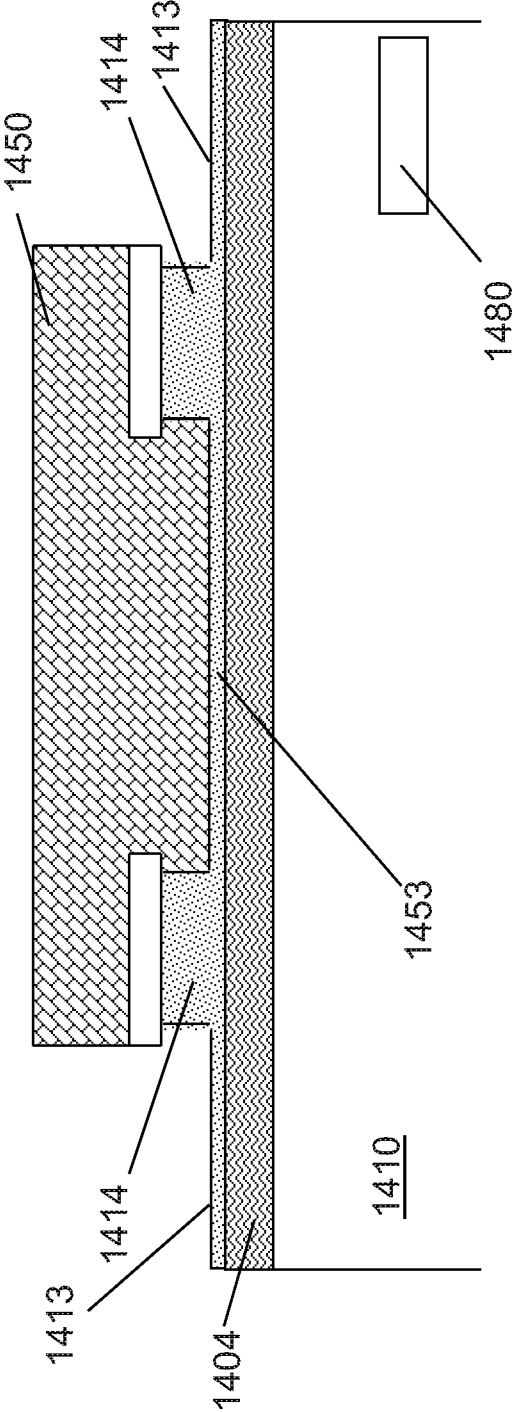
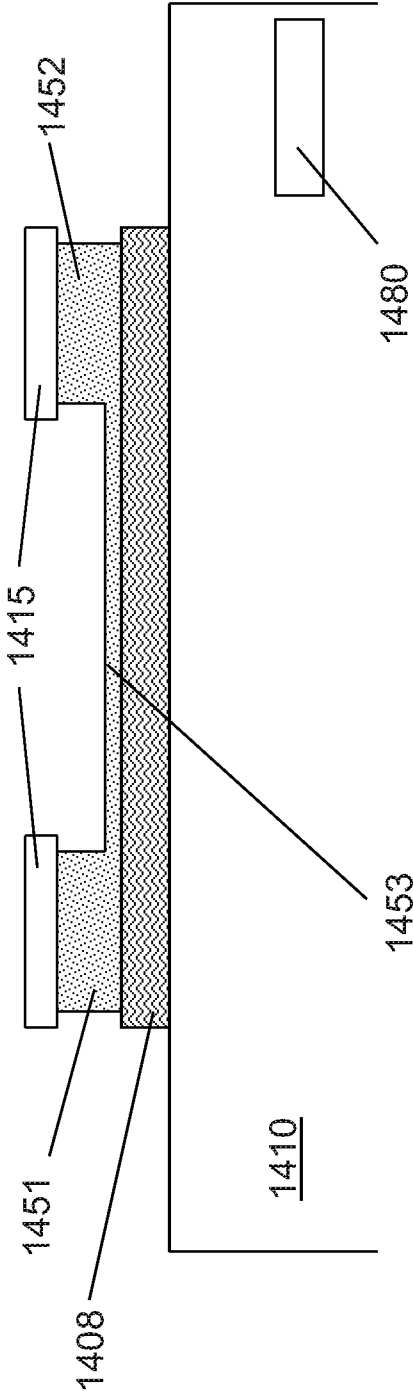


FIG. 14F



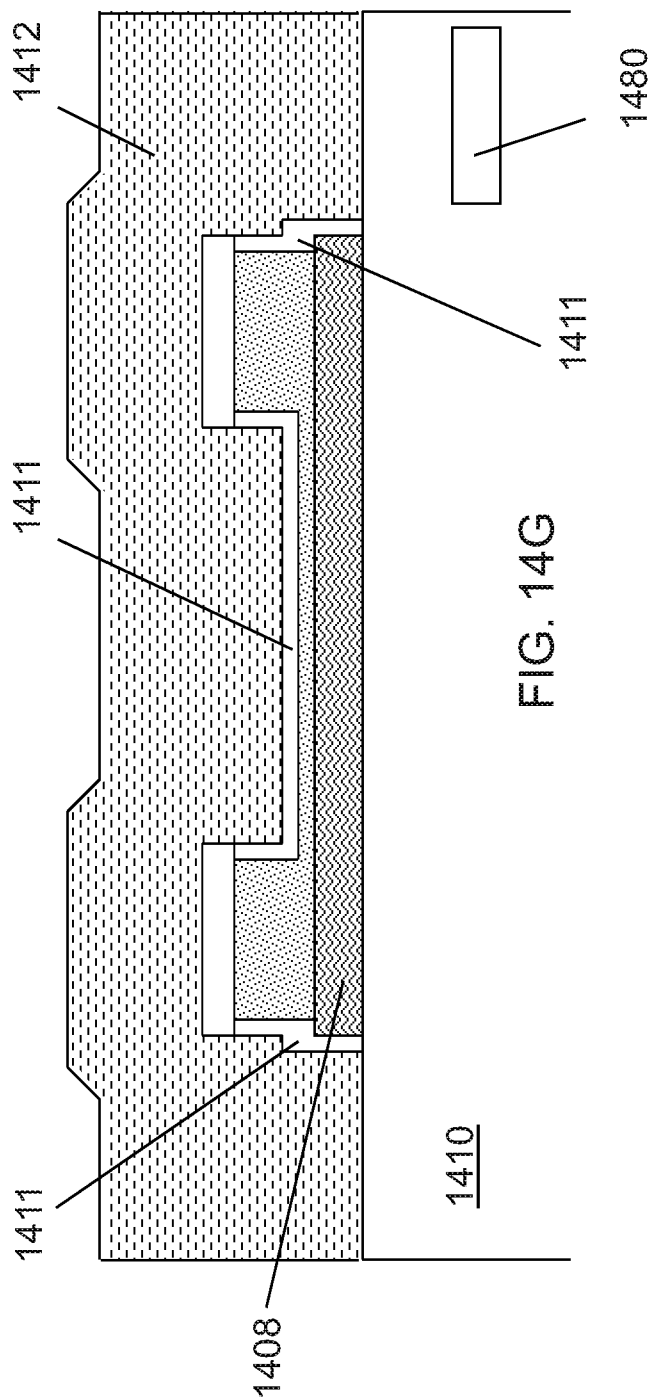


FIG. 14G

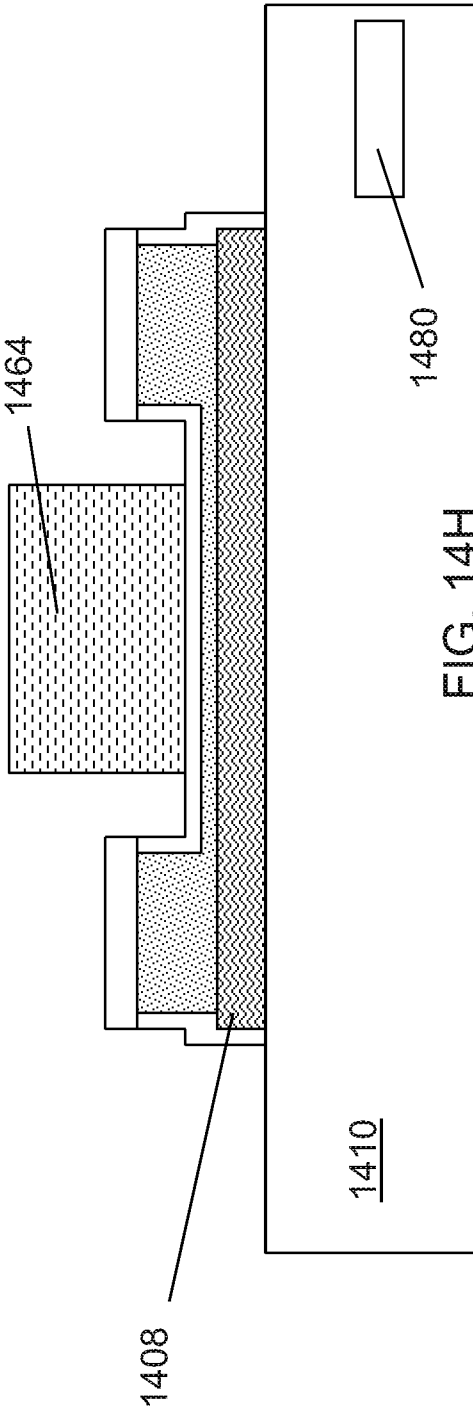


FIG. 14H

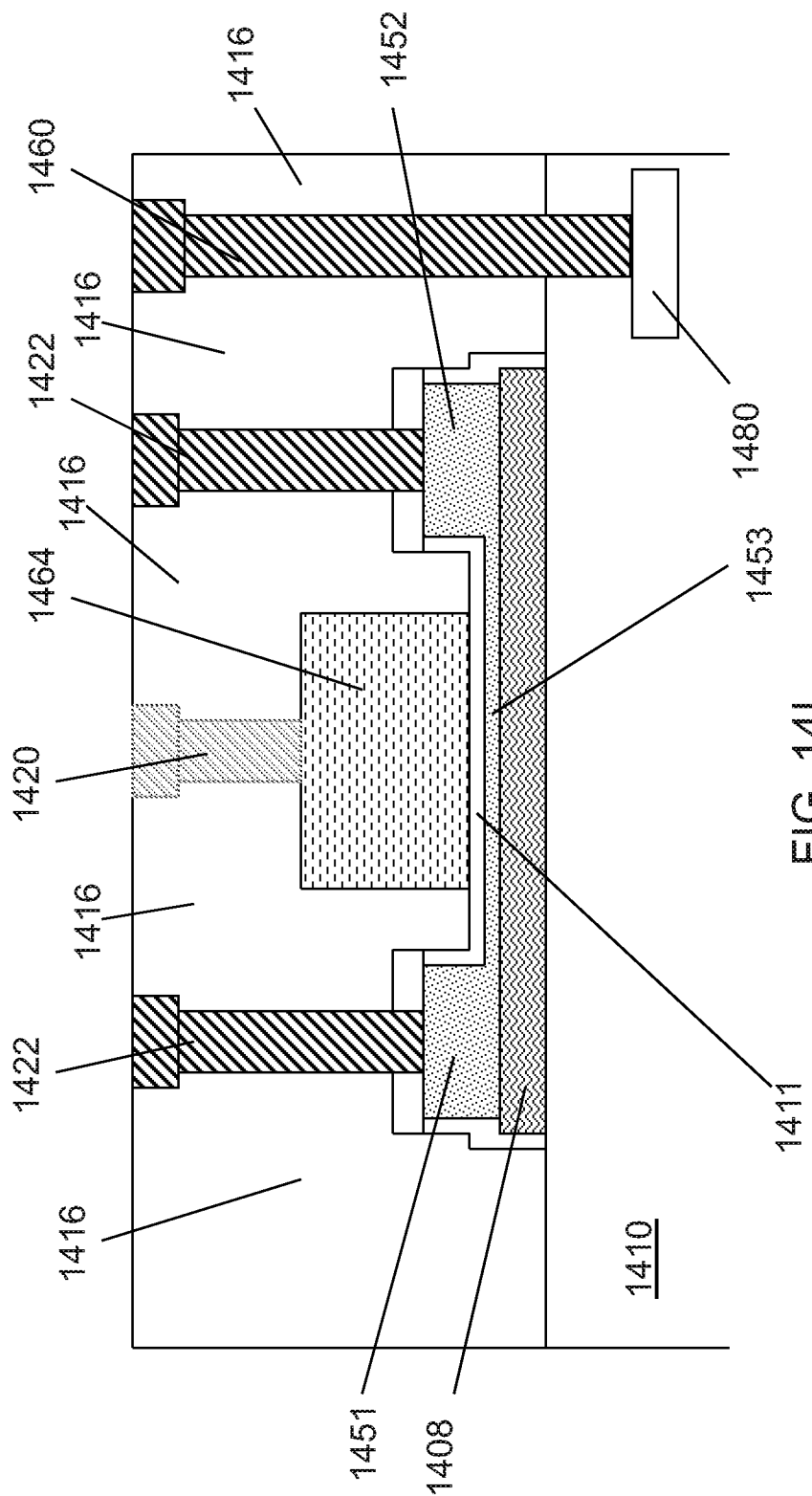


FIG. 14I



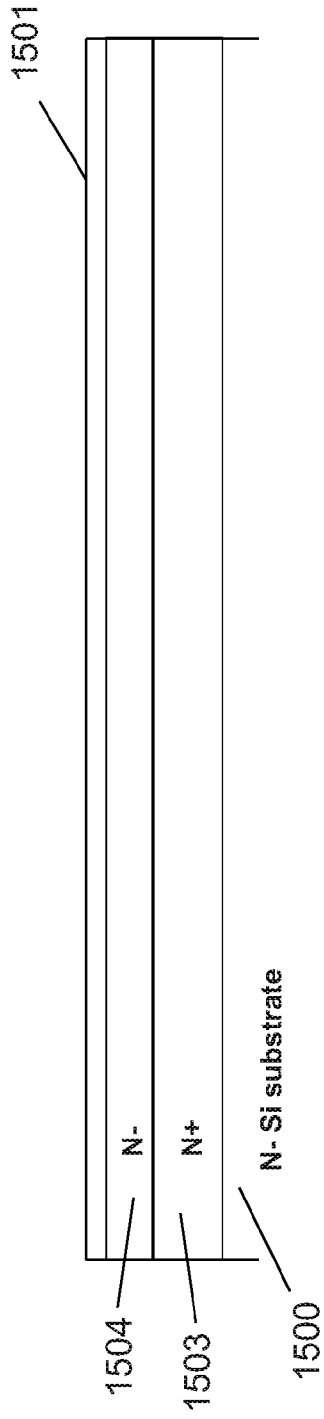


FIG. 15A

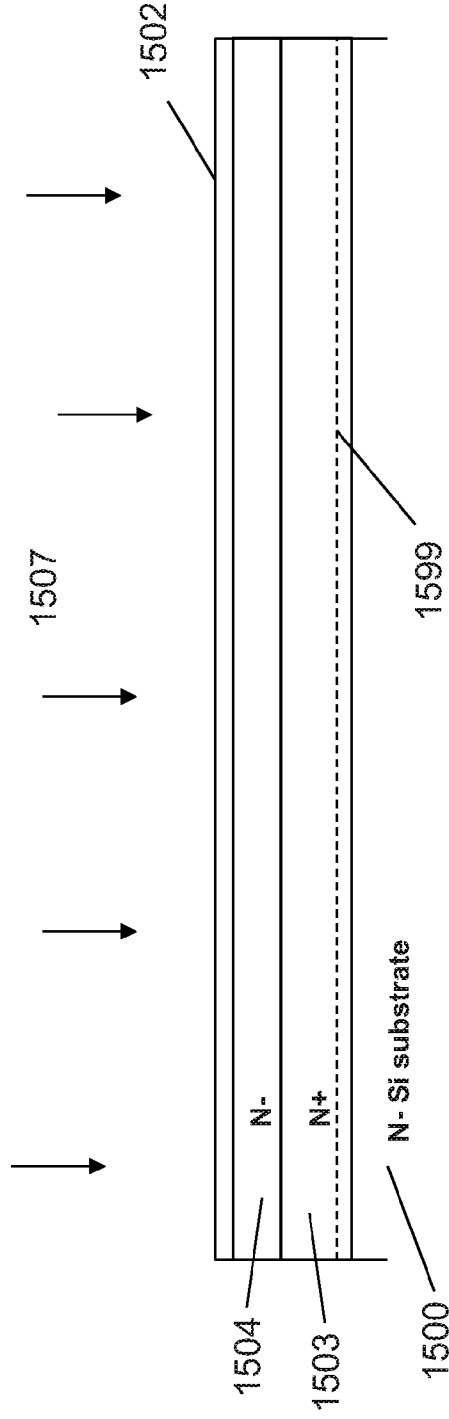


FIG. 15B

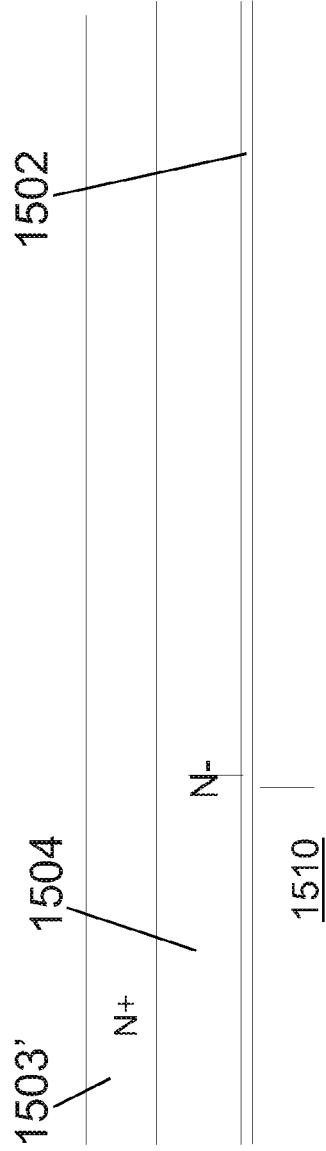


FIG. 15C

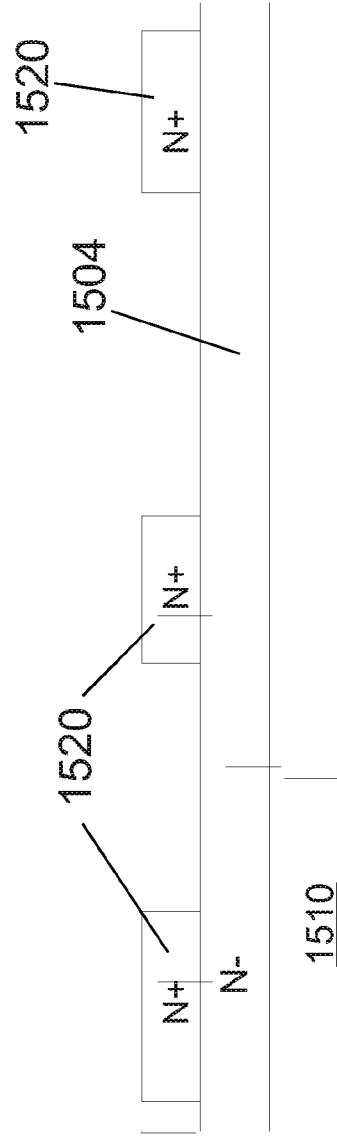


FIG. 15D

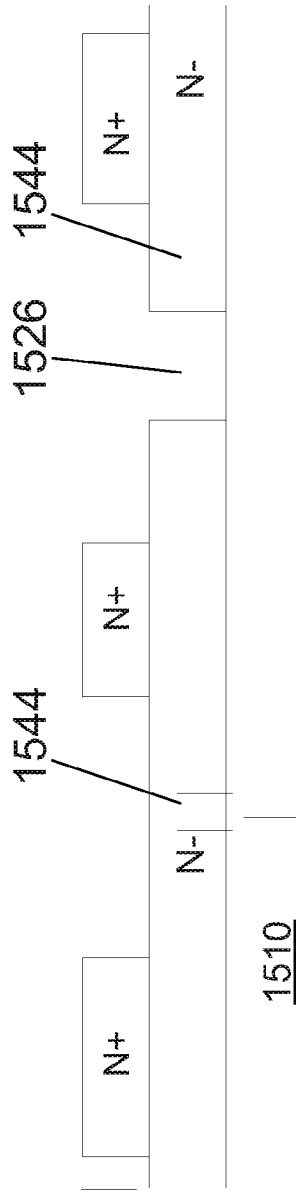


FIG. 15E

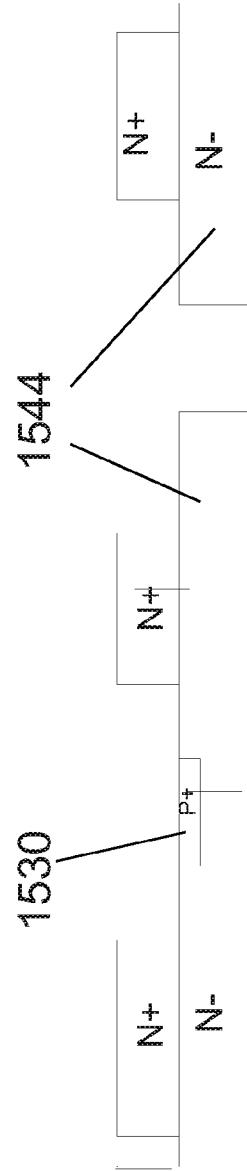


FIG. 15F

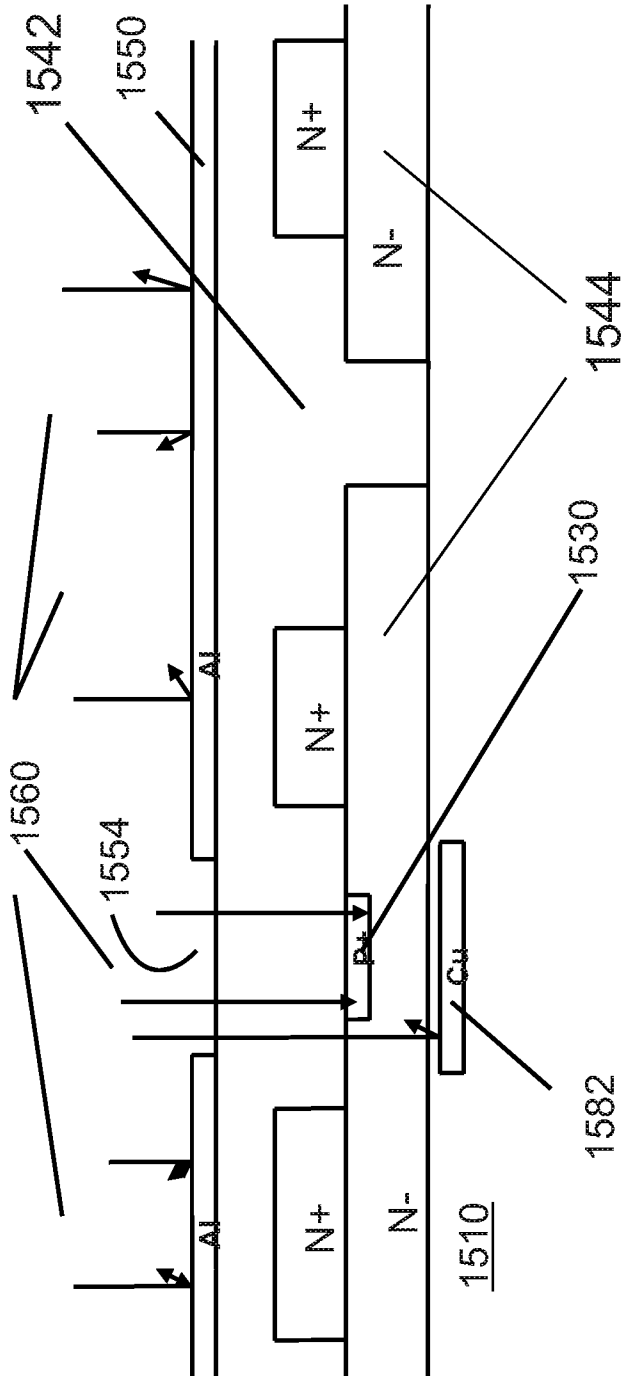


FIG. 15G

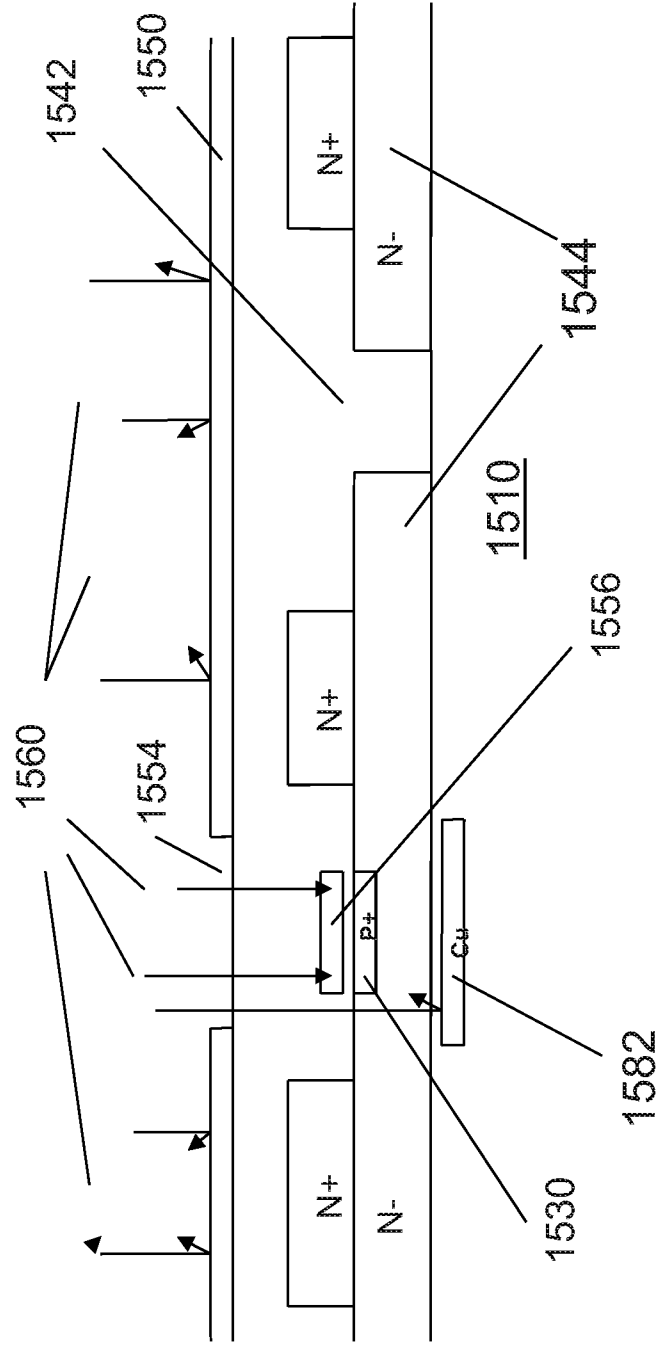


FIG. 15H

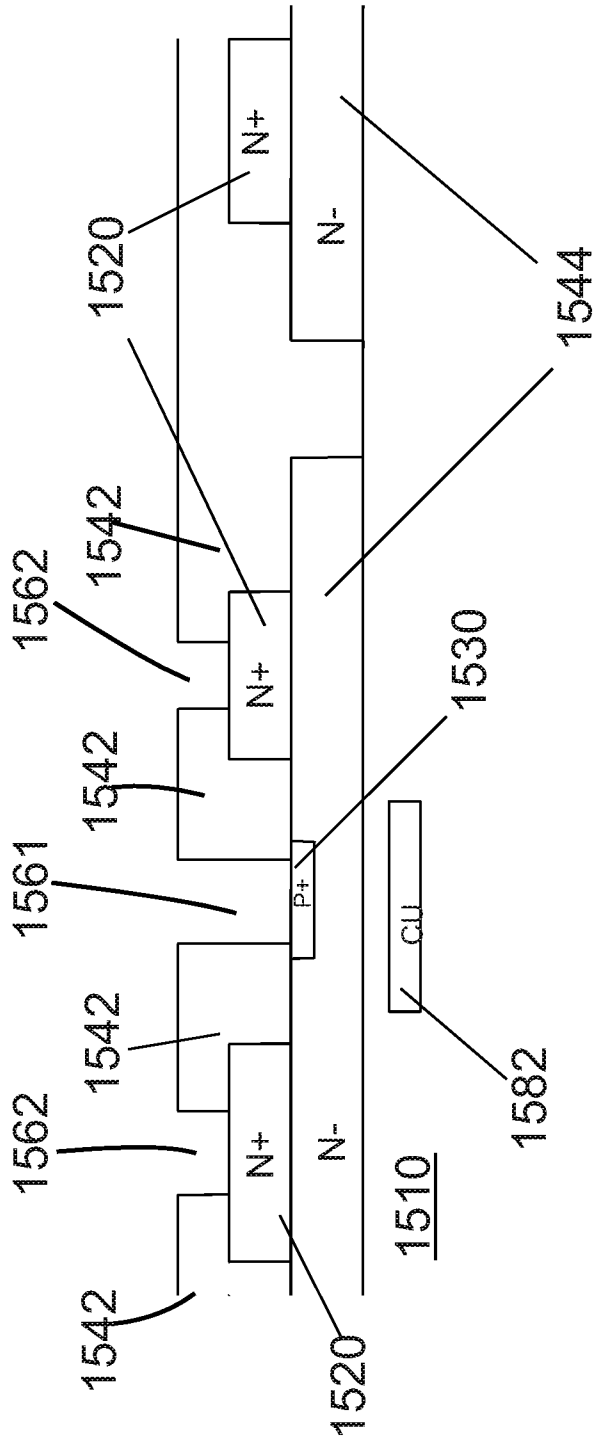


FIG. 15I

FIG. 16A

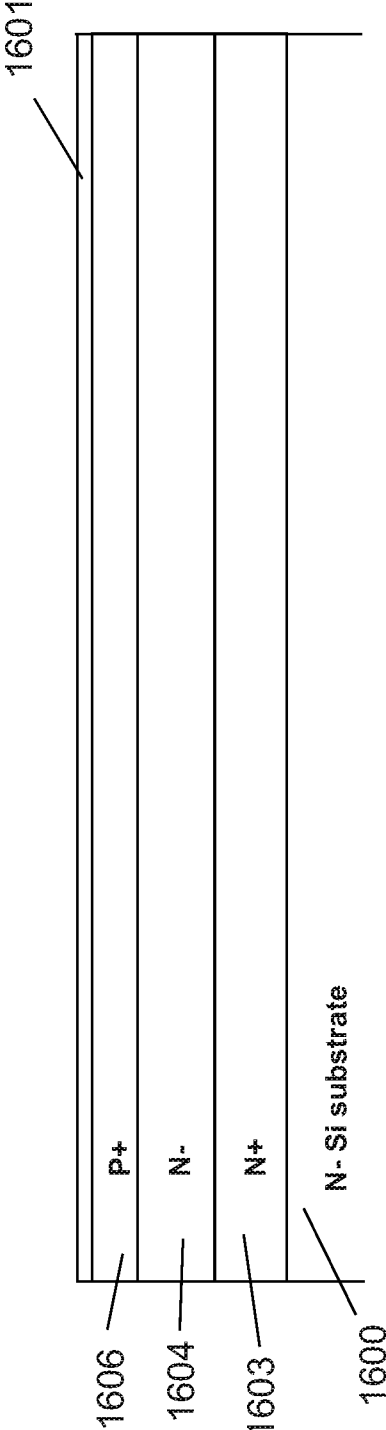
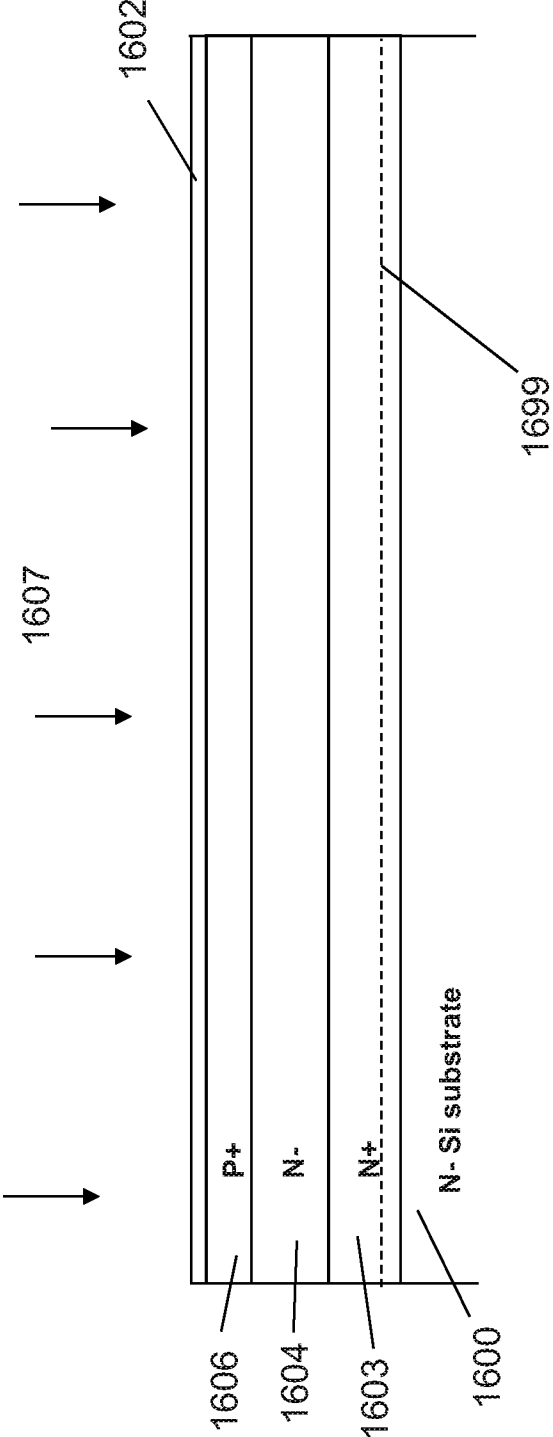


FIG. 16B





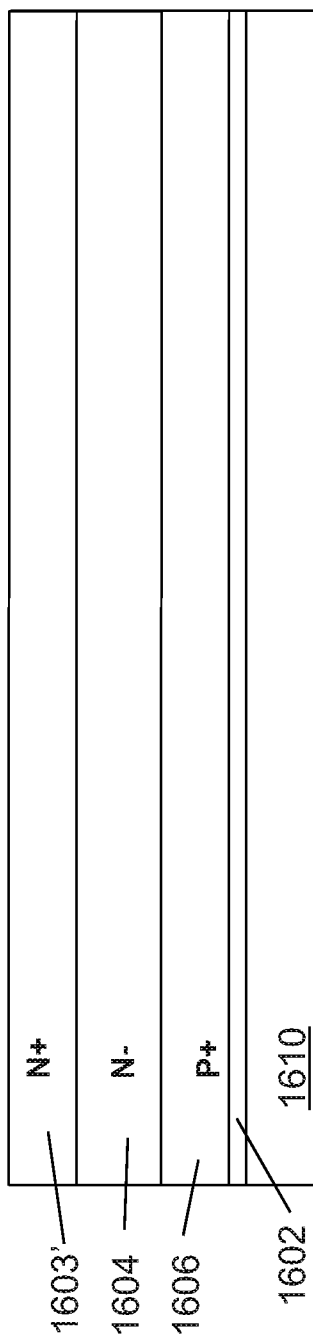


FIG. 16C

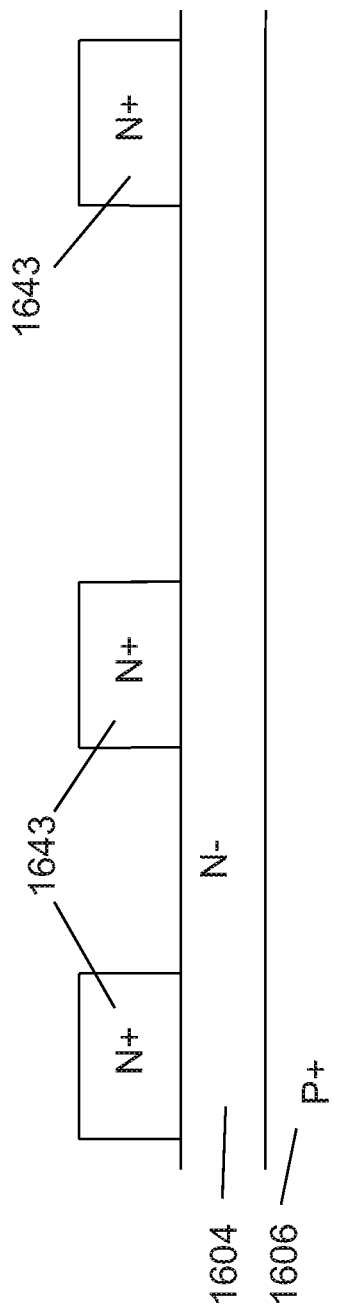


FIG. 16D

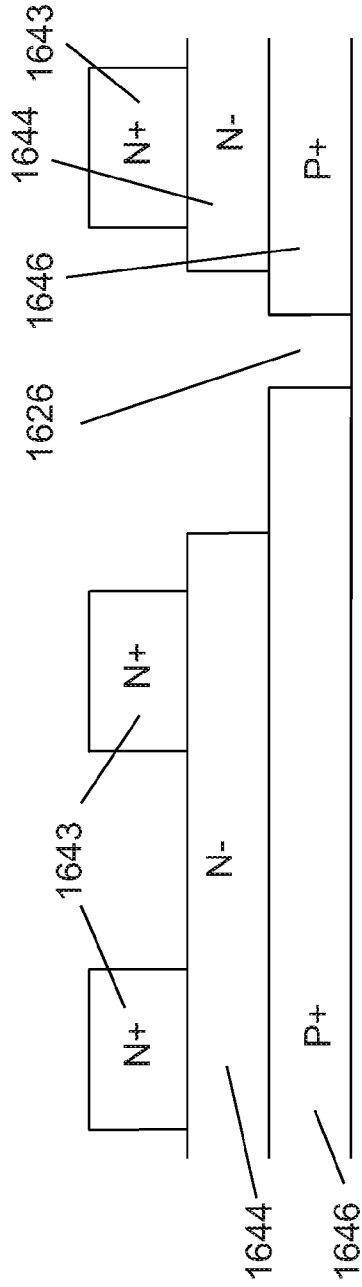


FIG. 16E

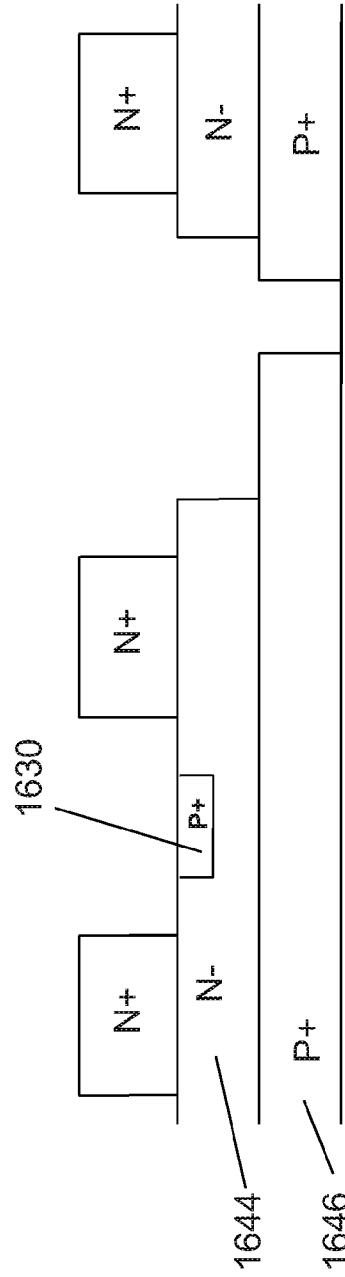


FIG. 16F

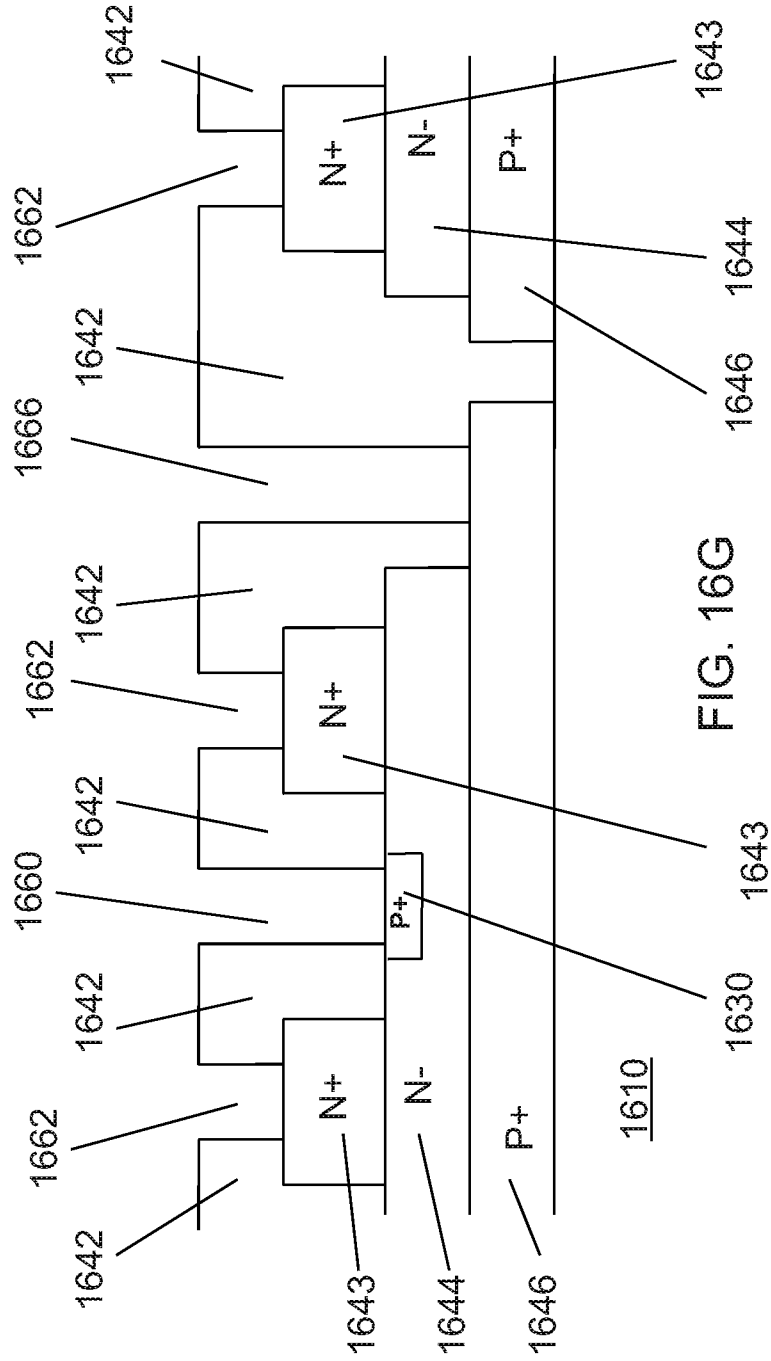


FIG. 16G

FIG. 17A

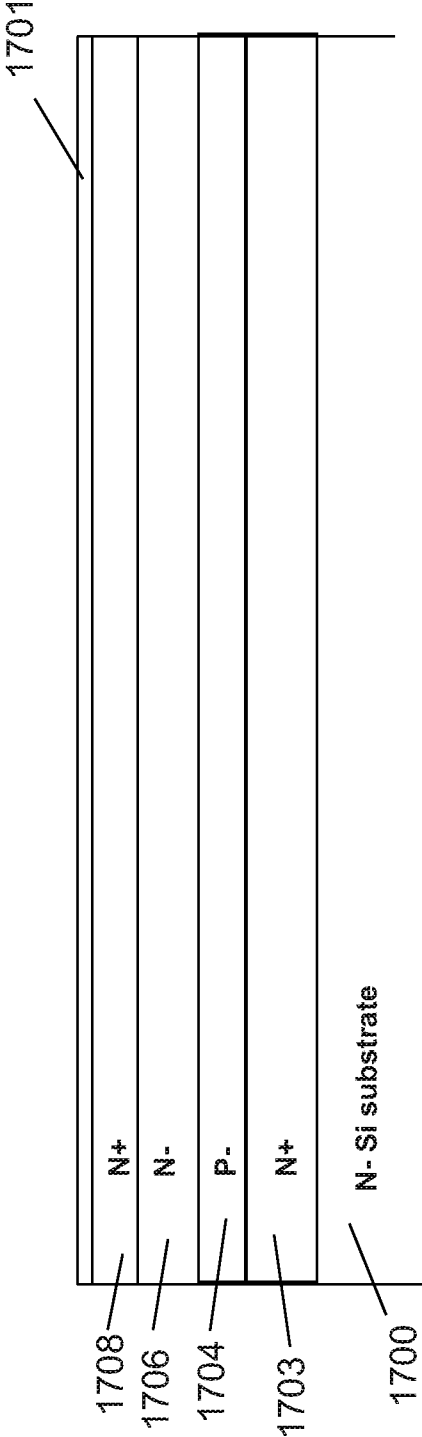
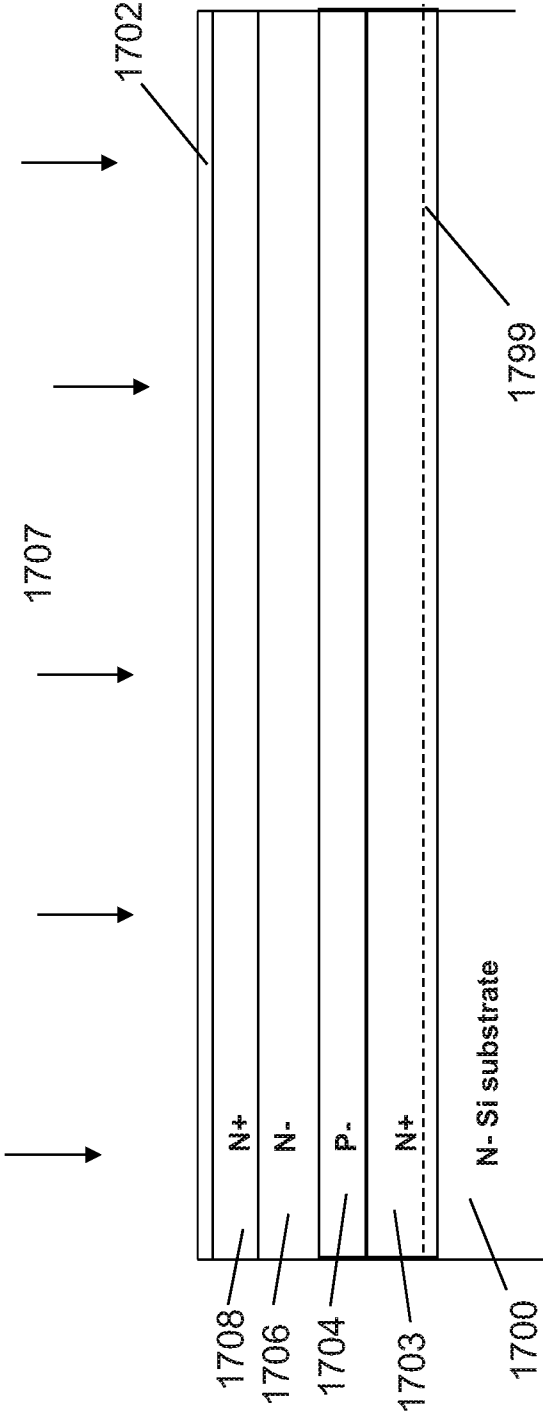


FIG. 17B



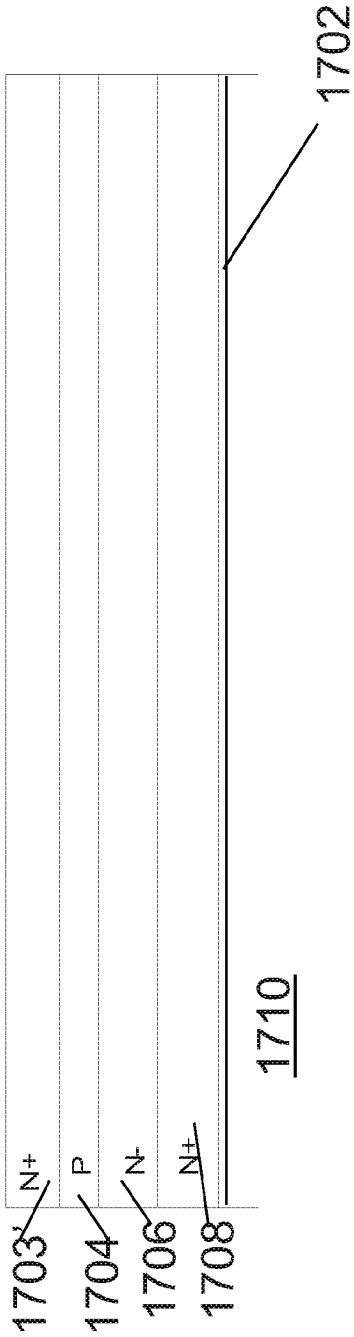


FIG. 17C

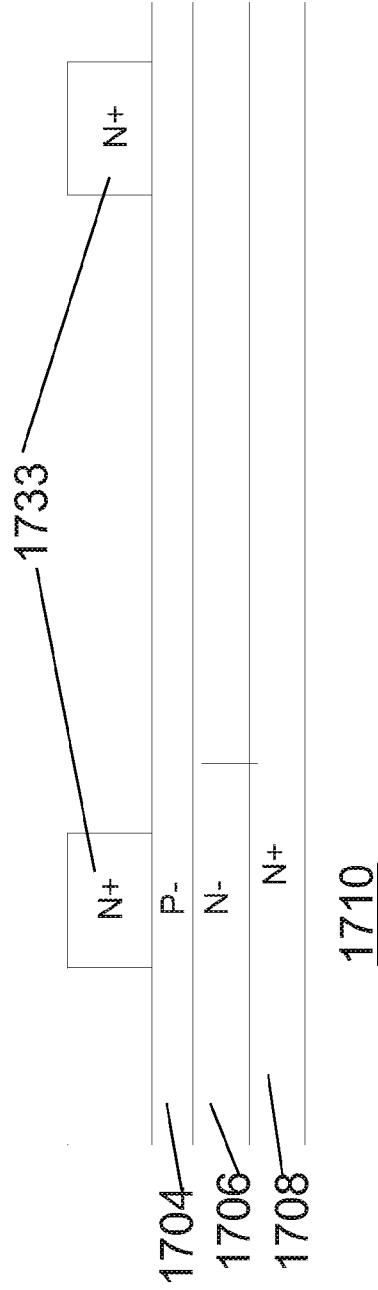


FIG. 17D

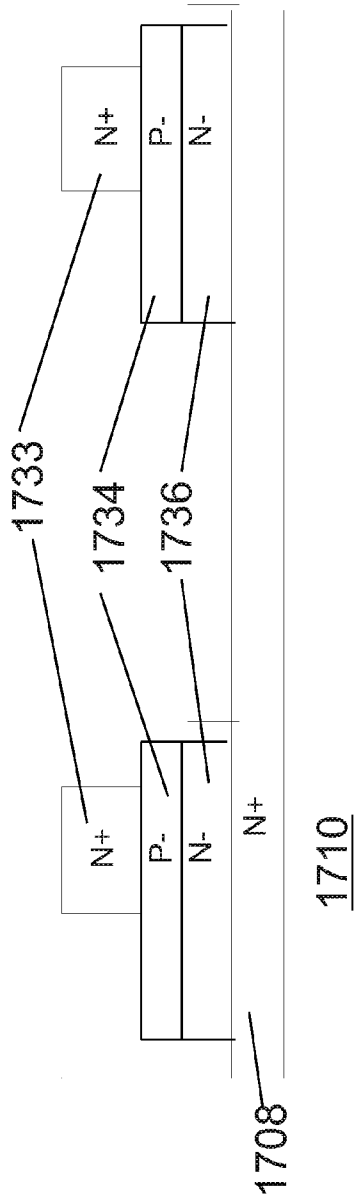


FIG. 17E

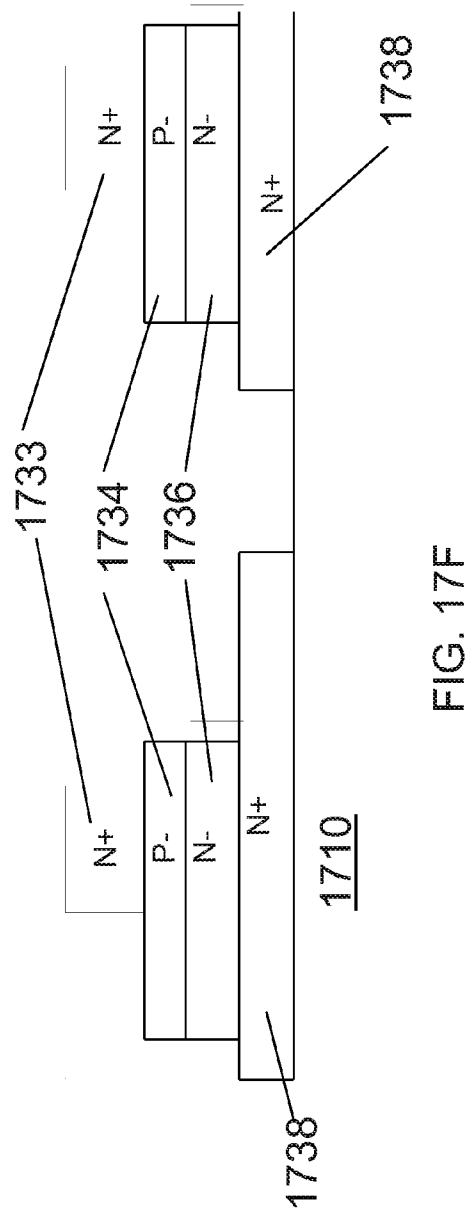


FIG. 17F

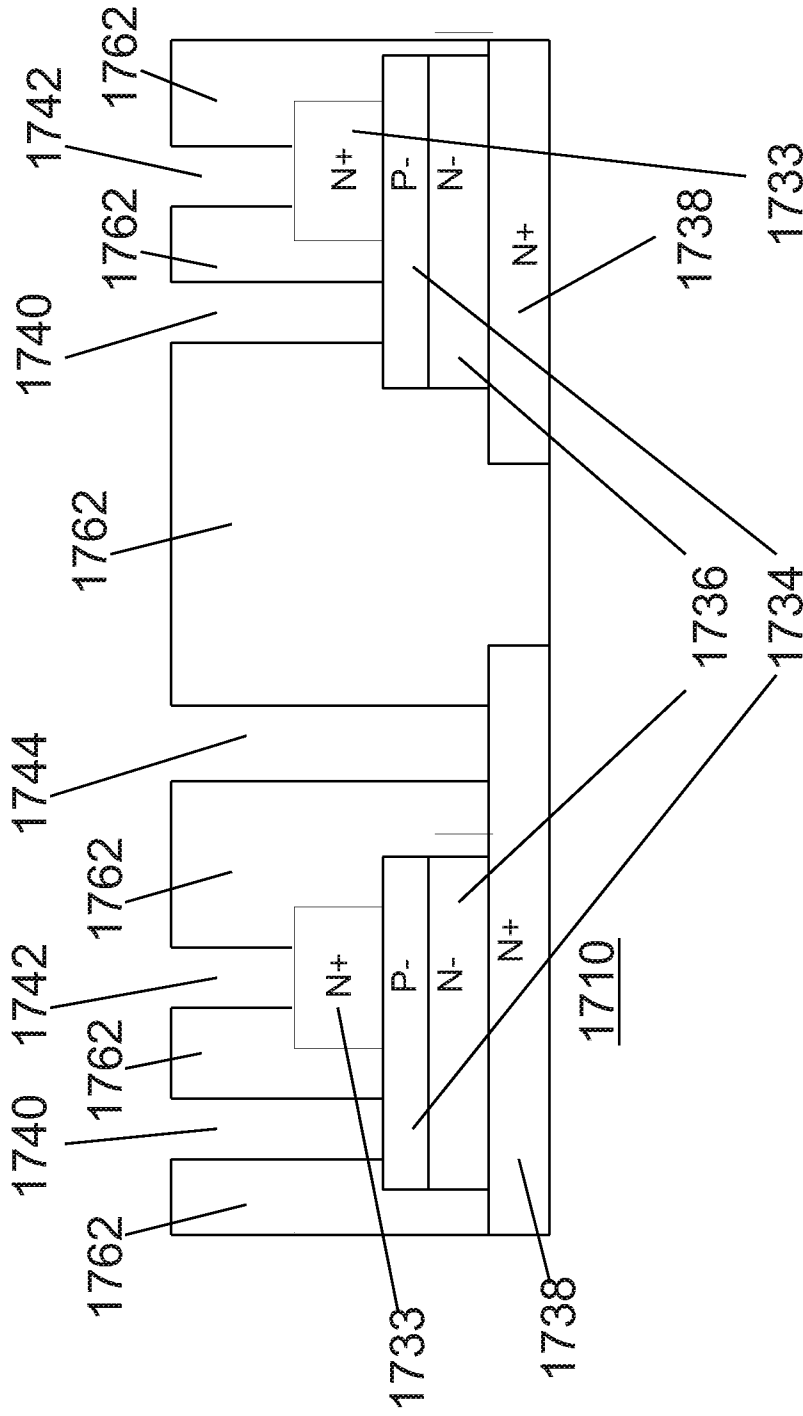


FIG. 17G



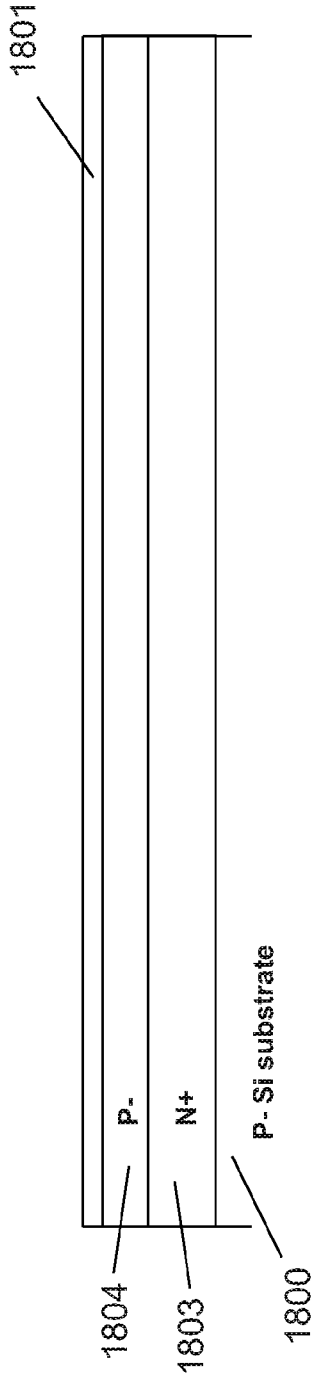


FIG. 18A

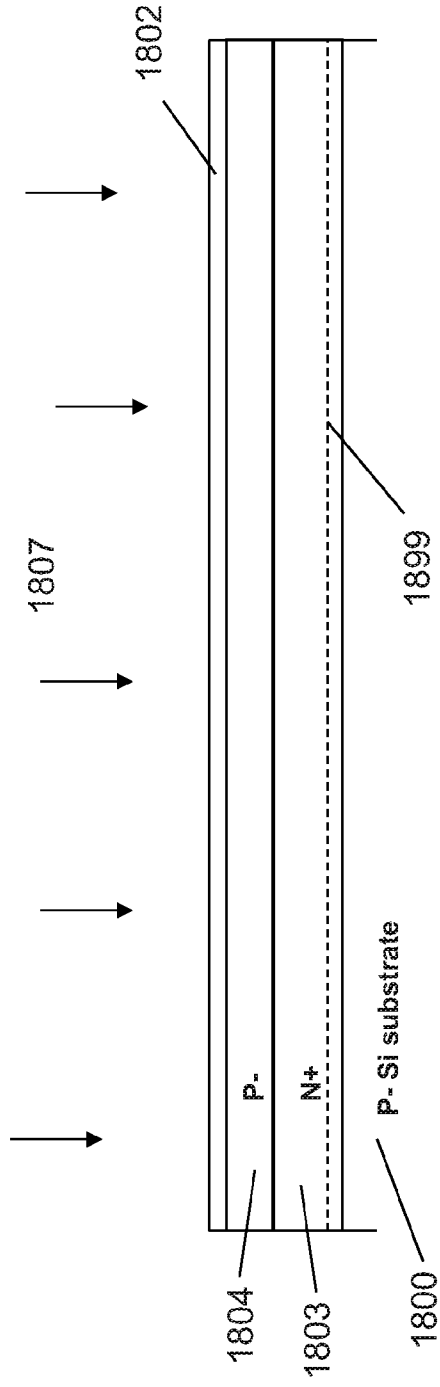


FIG. 18B

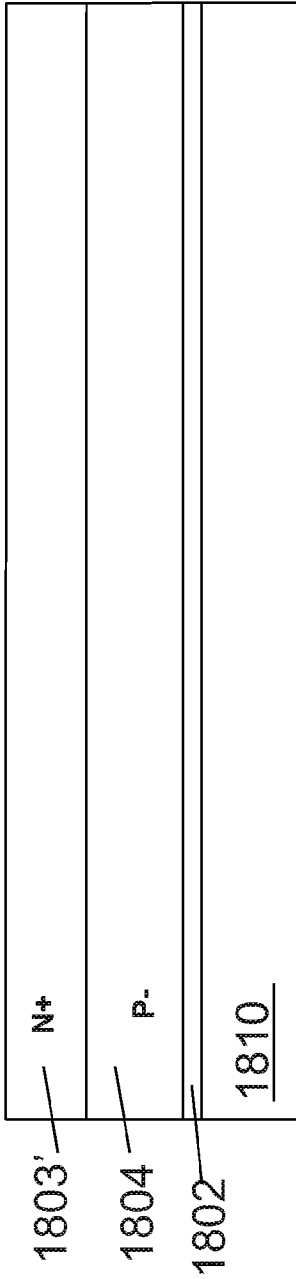


FIG. 18C

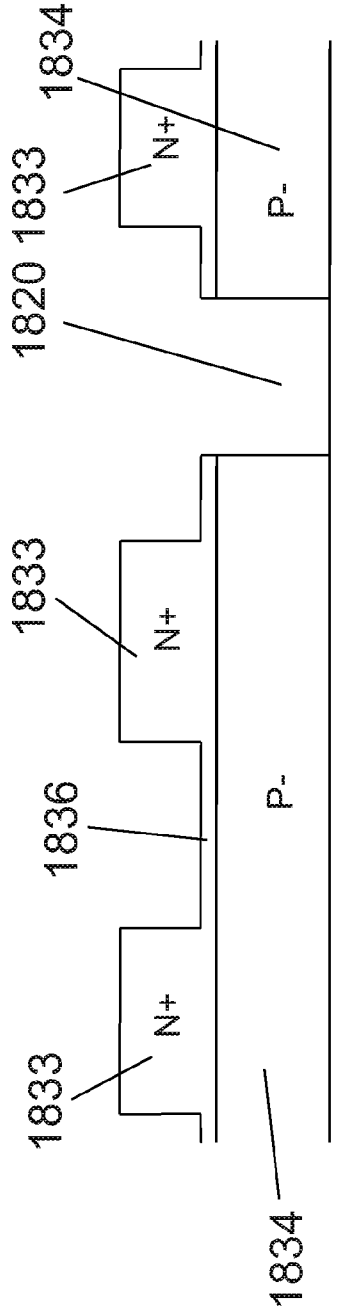


FIG. 18D

FIG. 18E

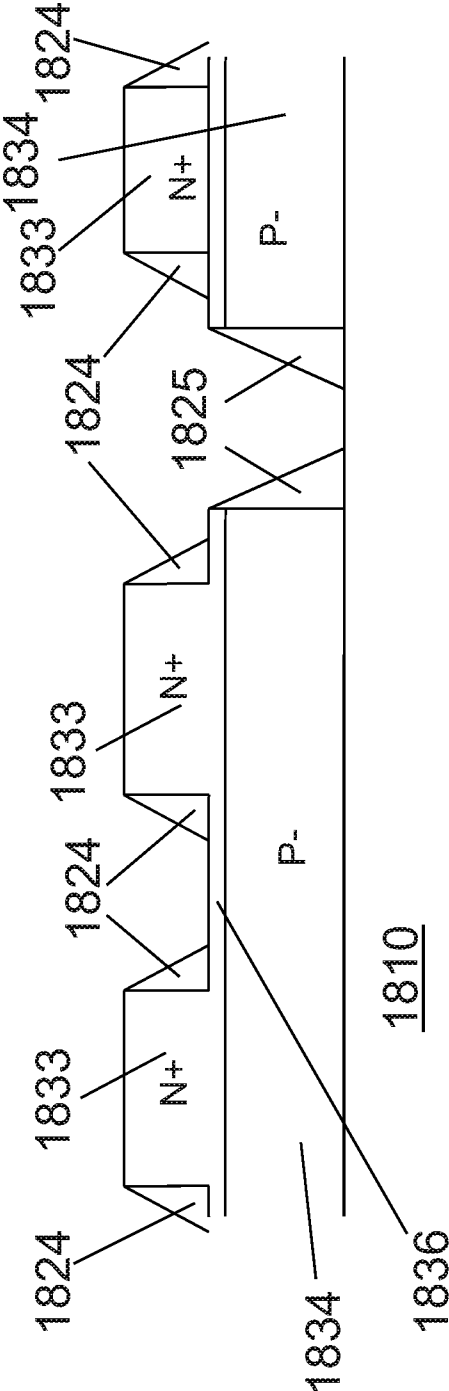
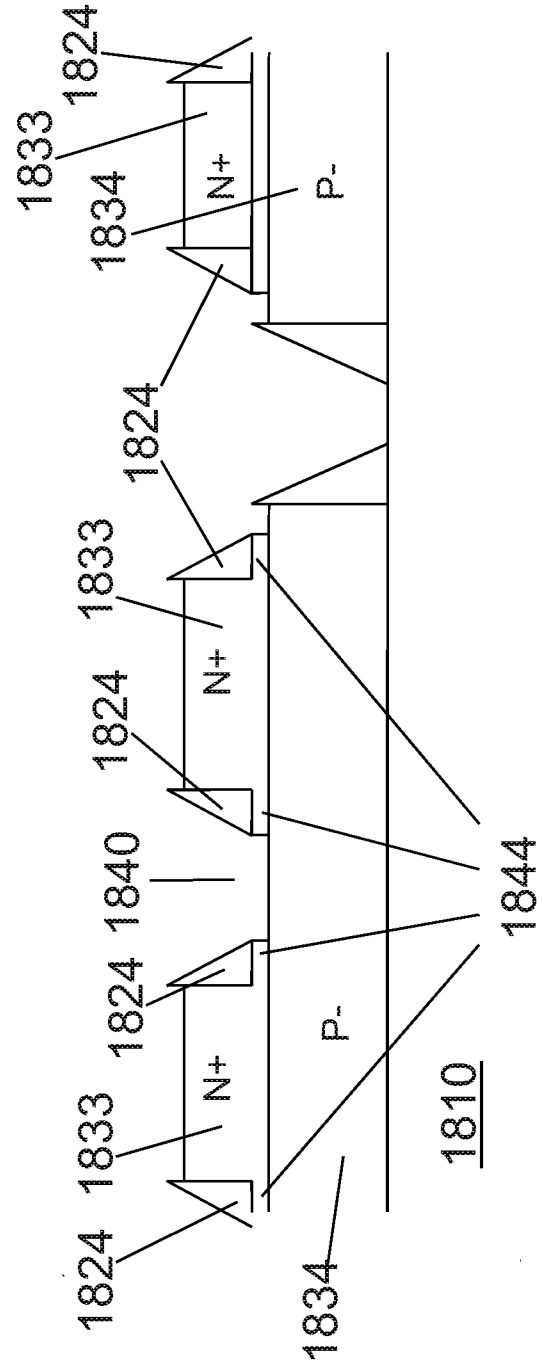


FIG. 18F



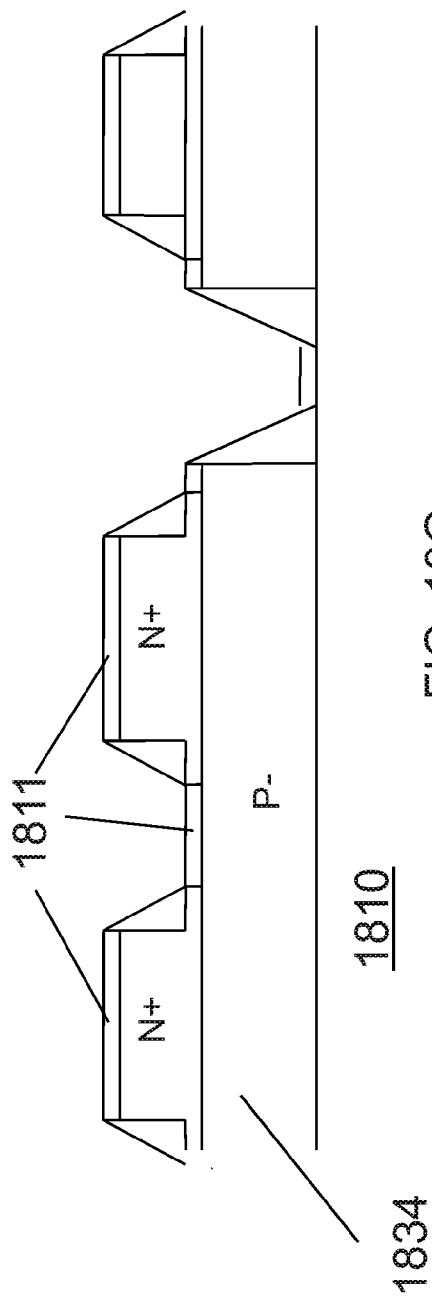


FIG. 18G

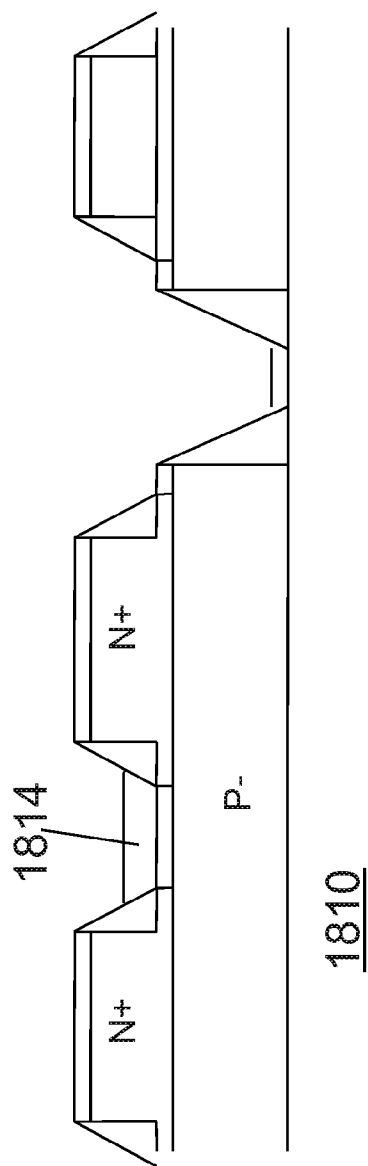


FIG. 18H

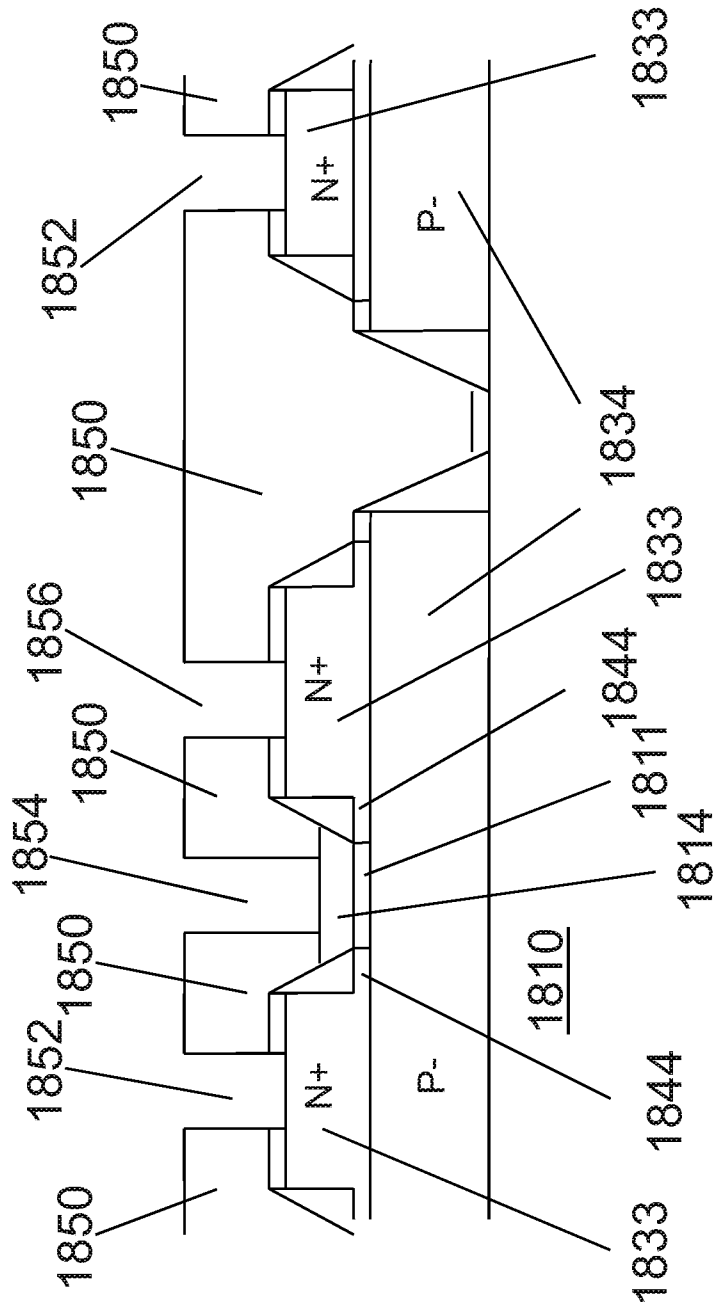


FIG. 18I

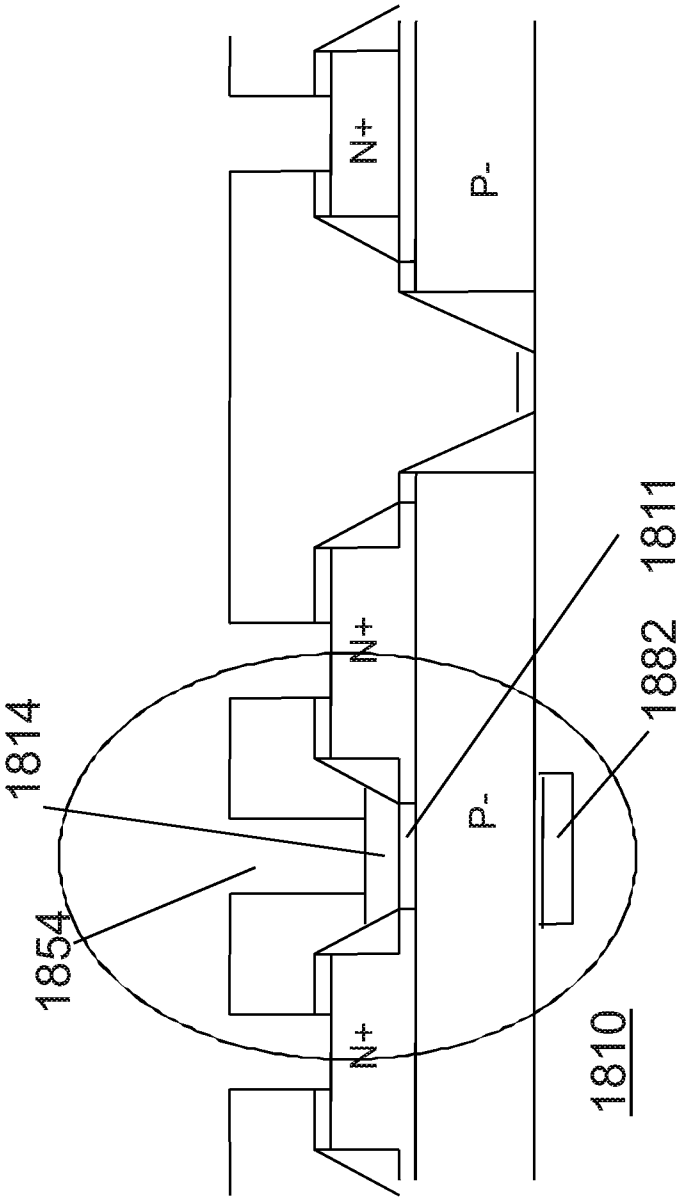


FIG. 18J

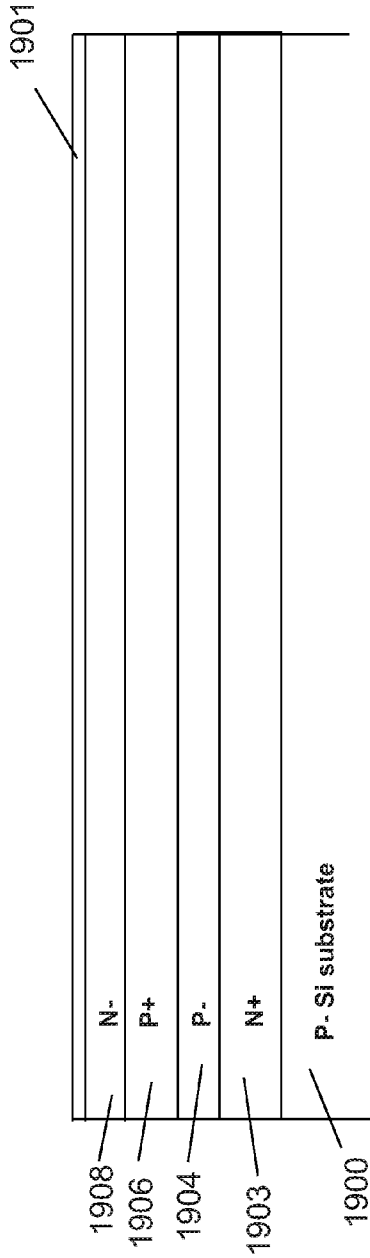


FIG. 19A

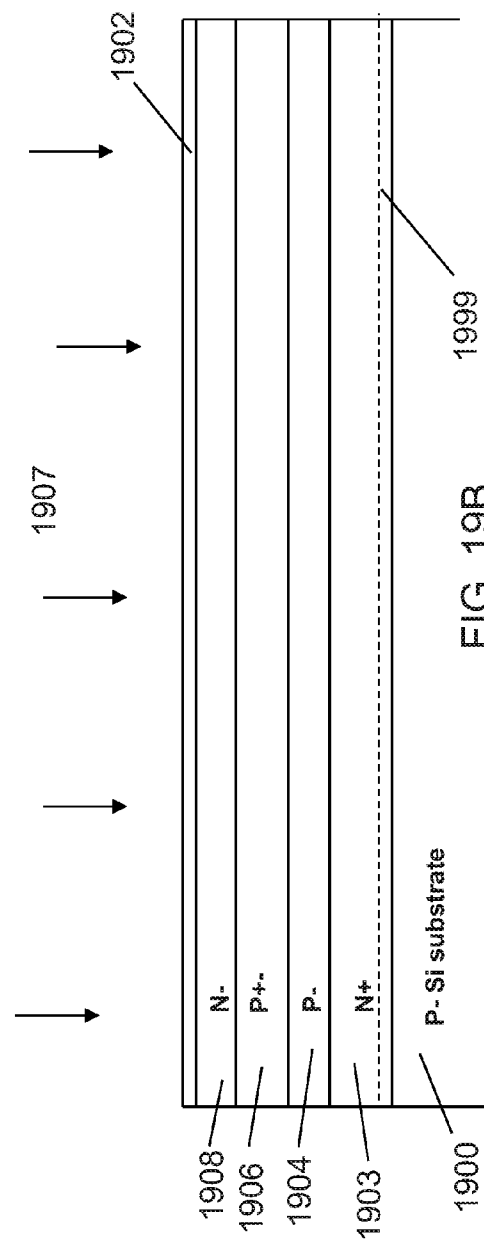


FIG. 19B



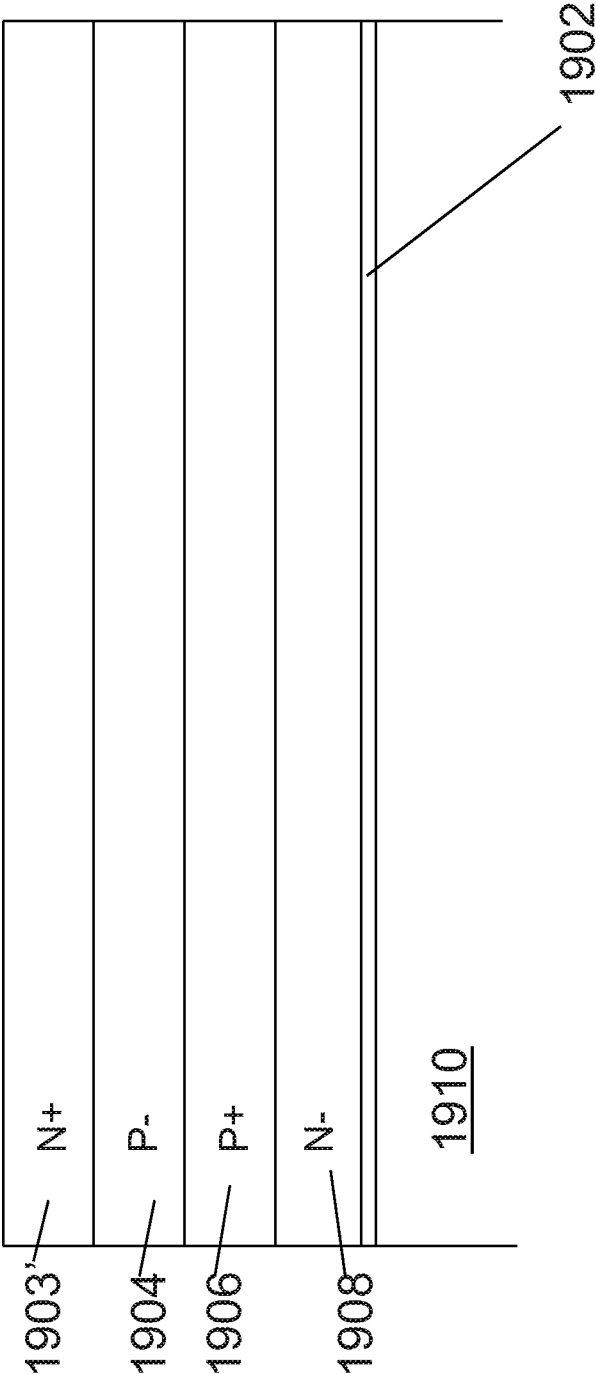


FIG. 19C

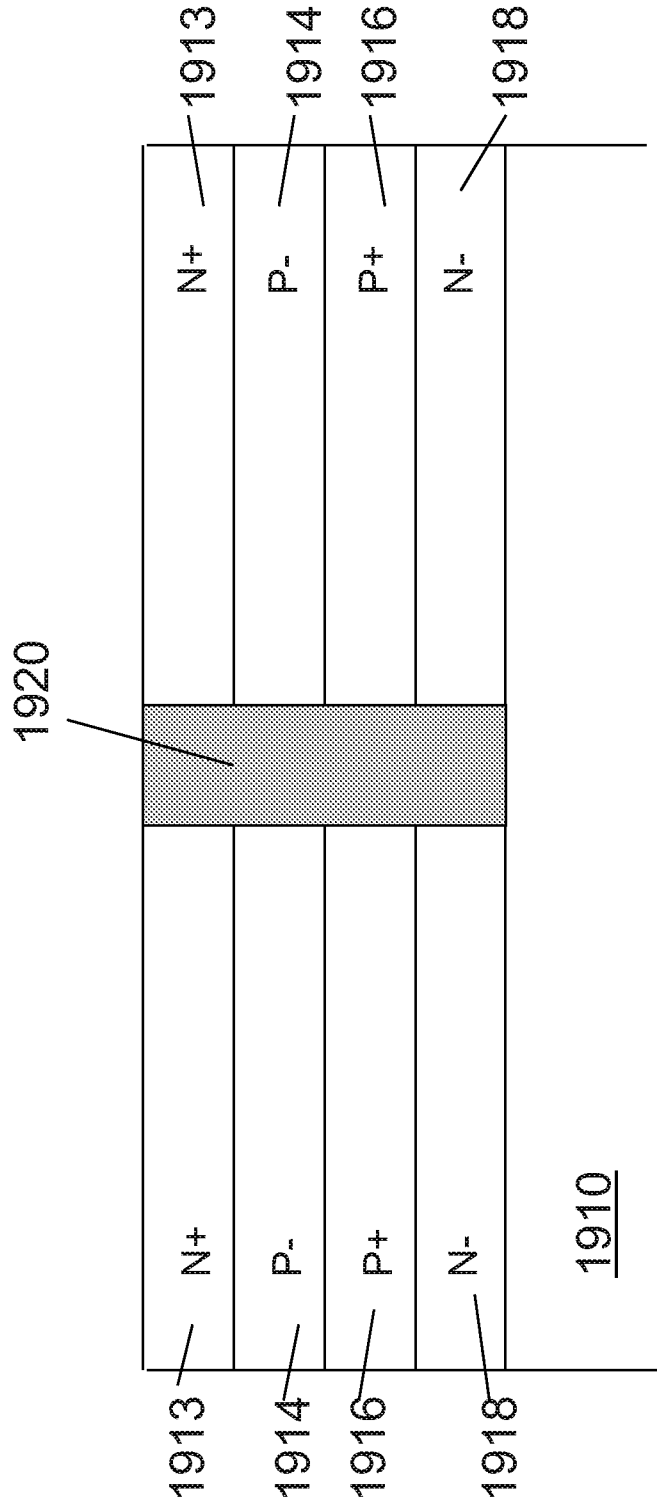


FIG. 19D

n-RCAT

p-RCAT

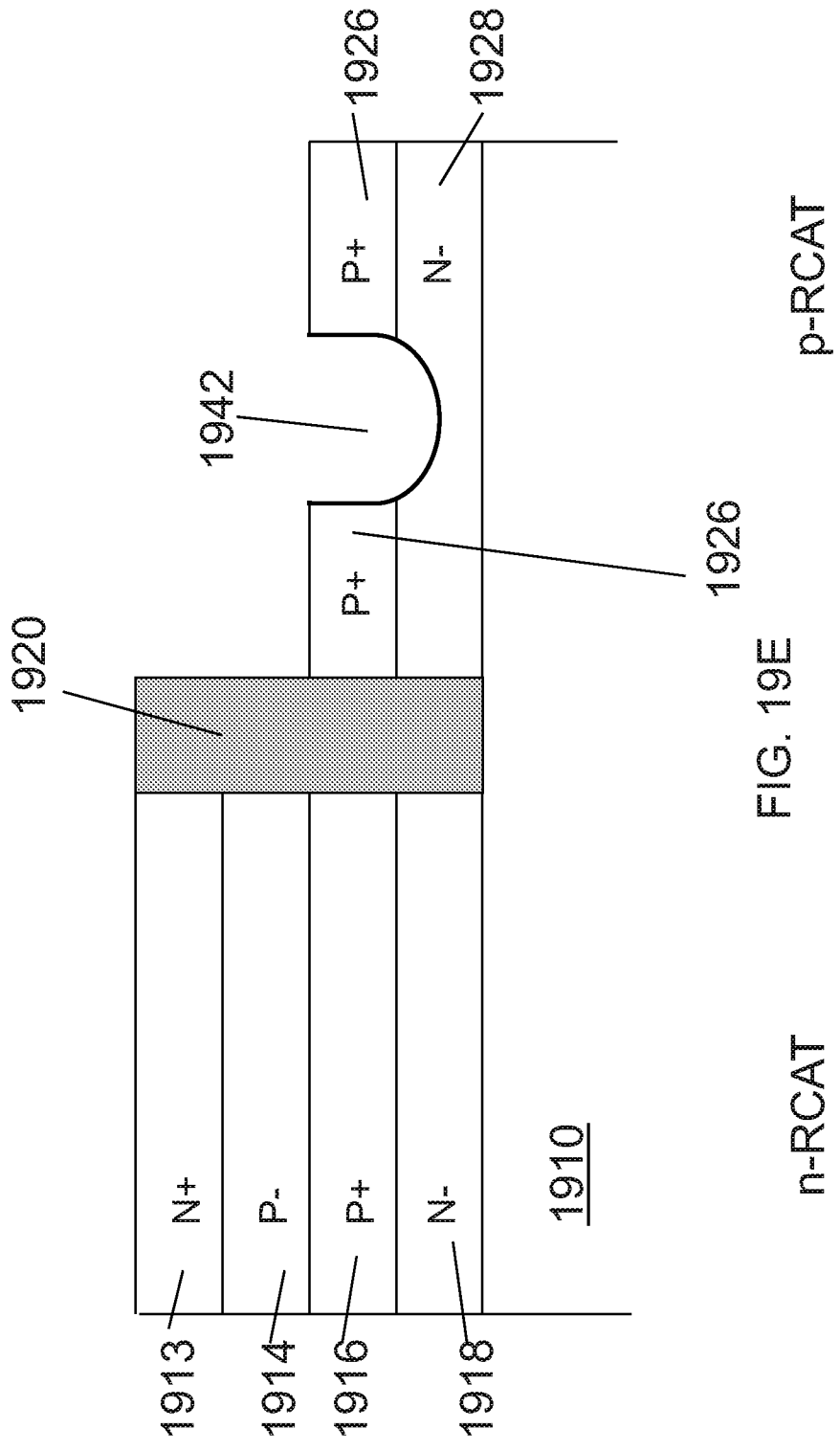


FIG. 19E

n-RCAT

p-RCAT

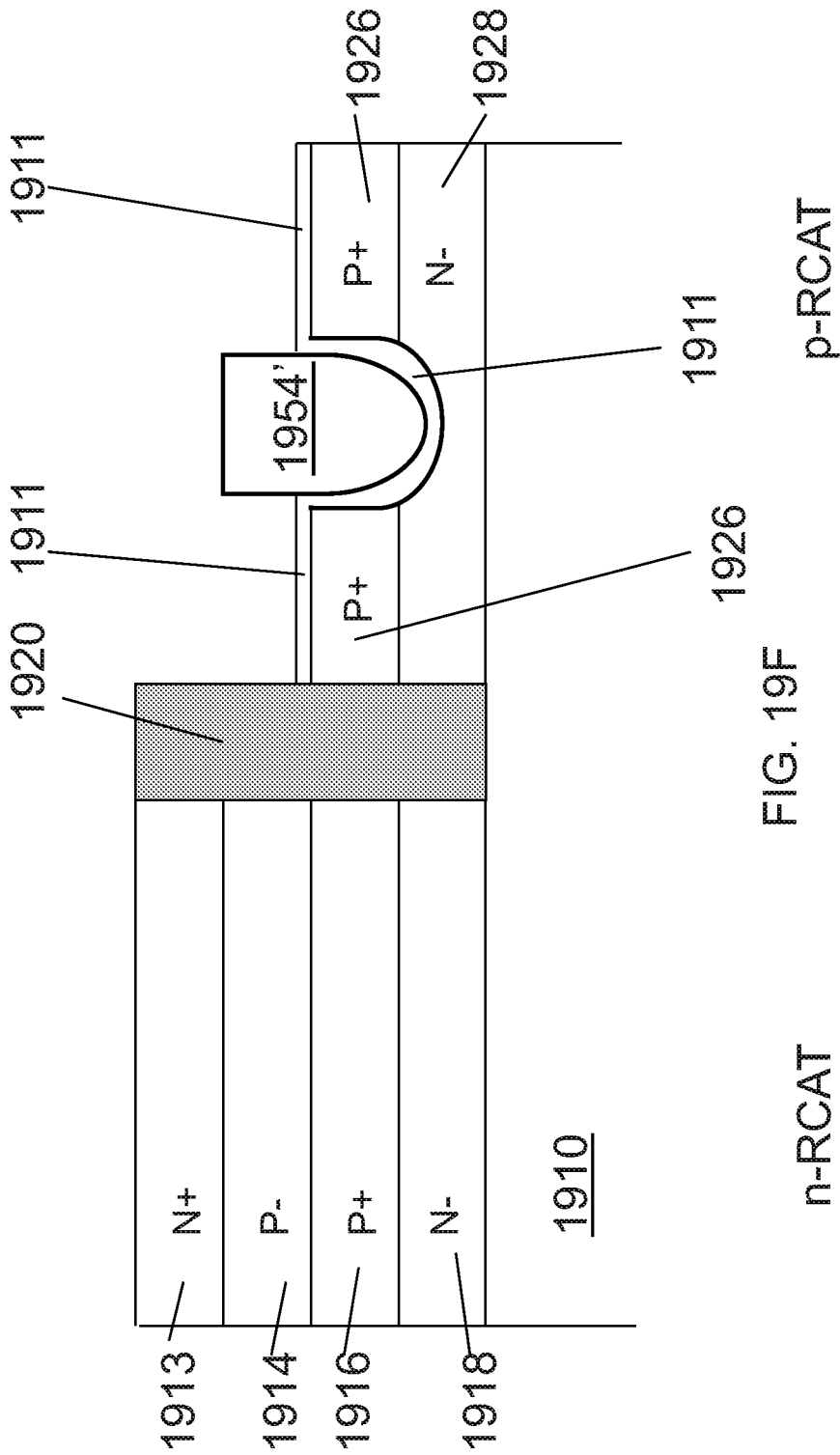


FIG. 19F

n-RCAT

p-RCAT

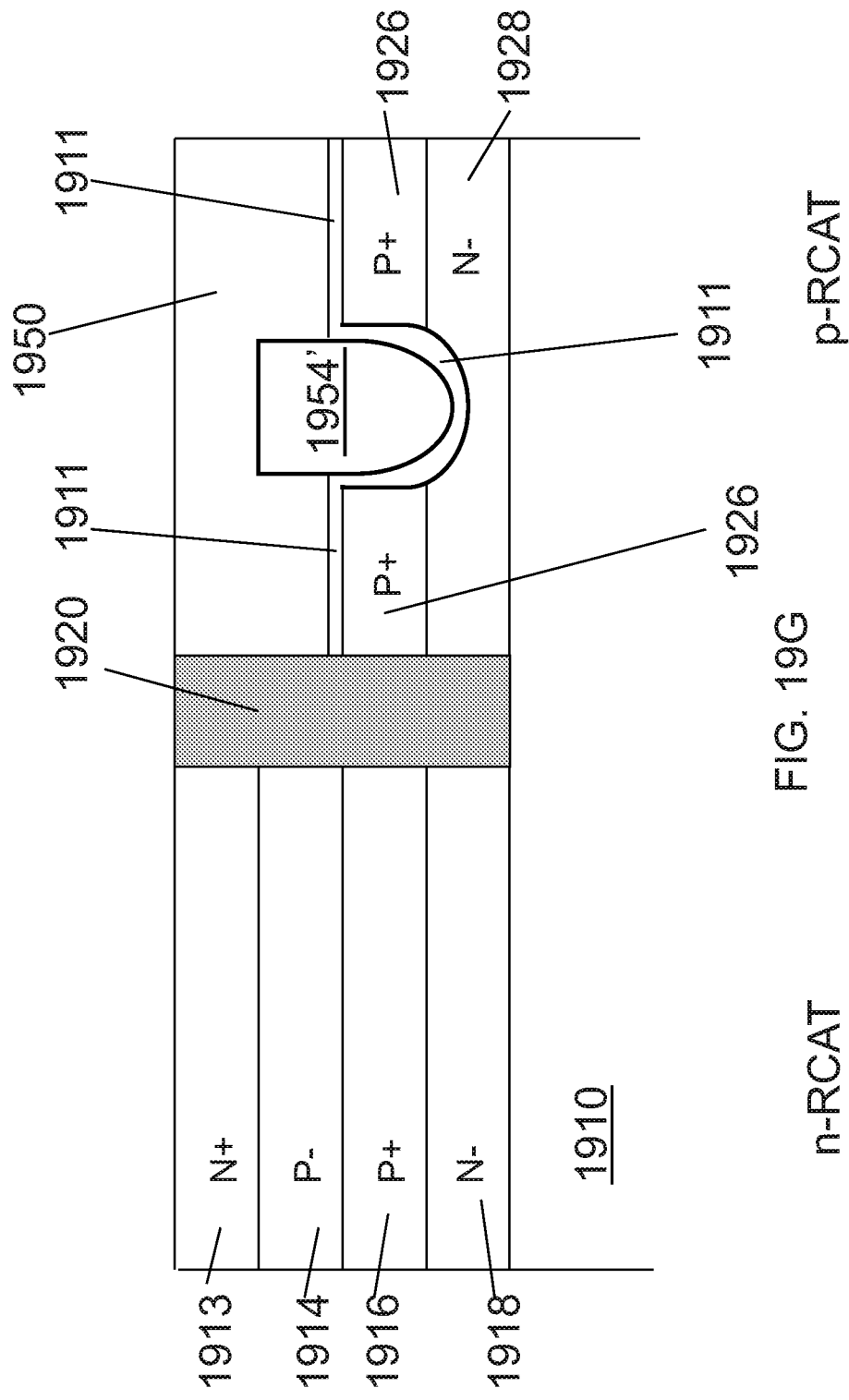


FIG. 19G

n-RCAT

p-RCAT

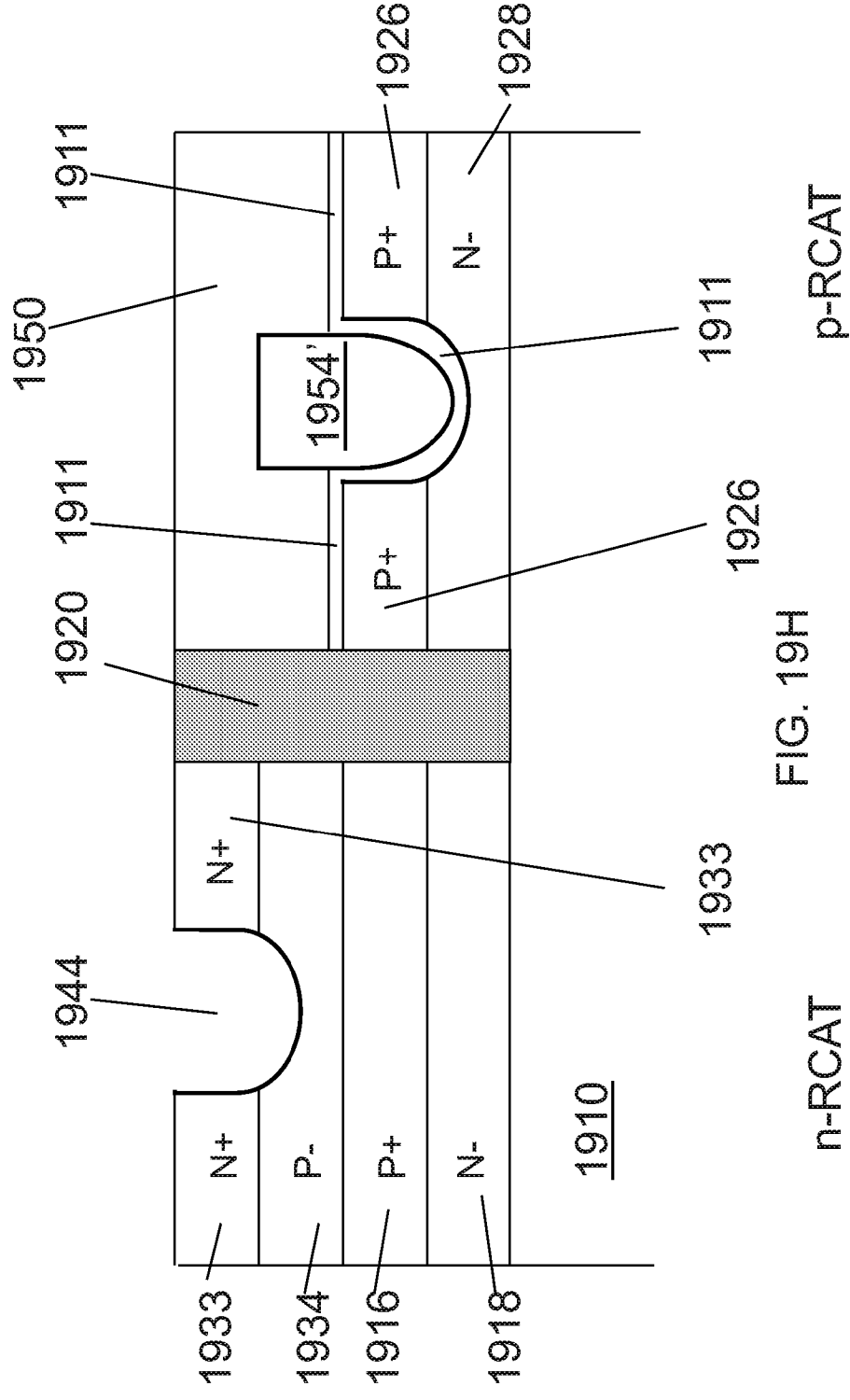
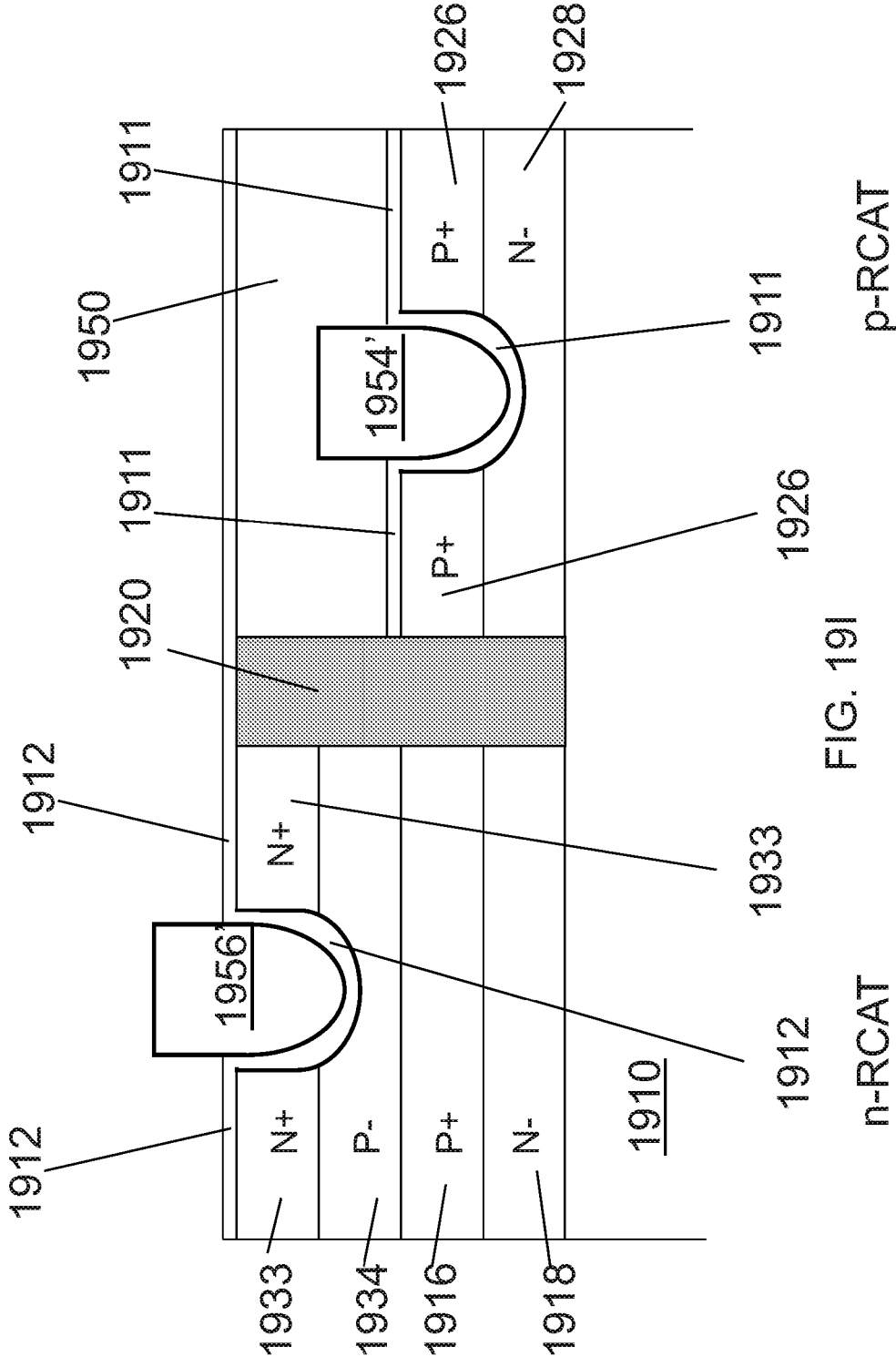


FIG. 19H

p-RCAT

n-RCAT



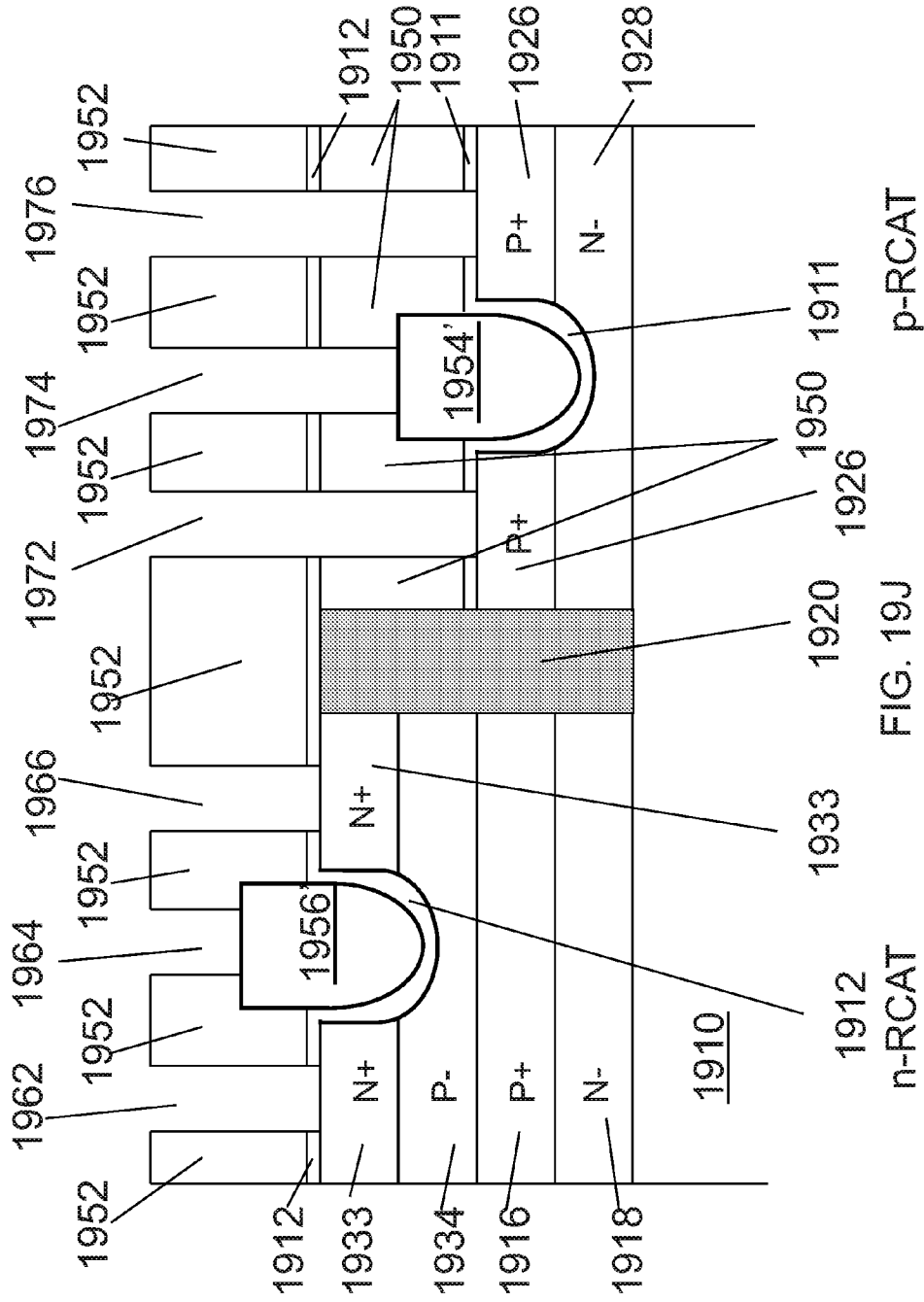


FIG. 19J p-RCAT

FIG. 19J n-RCAT



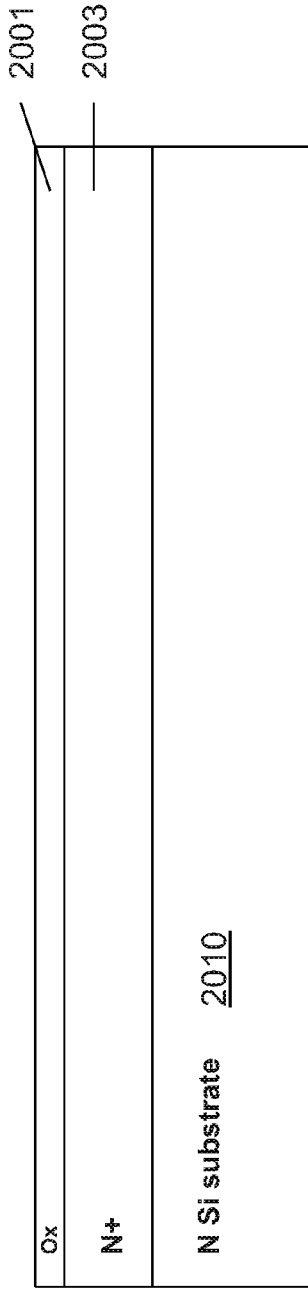


FIG. 20A

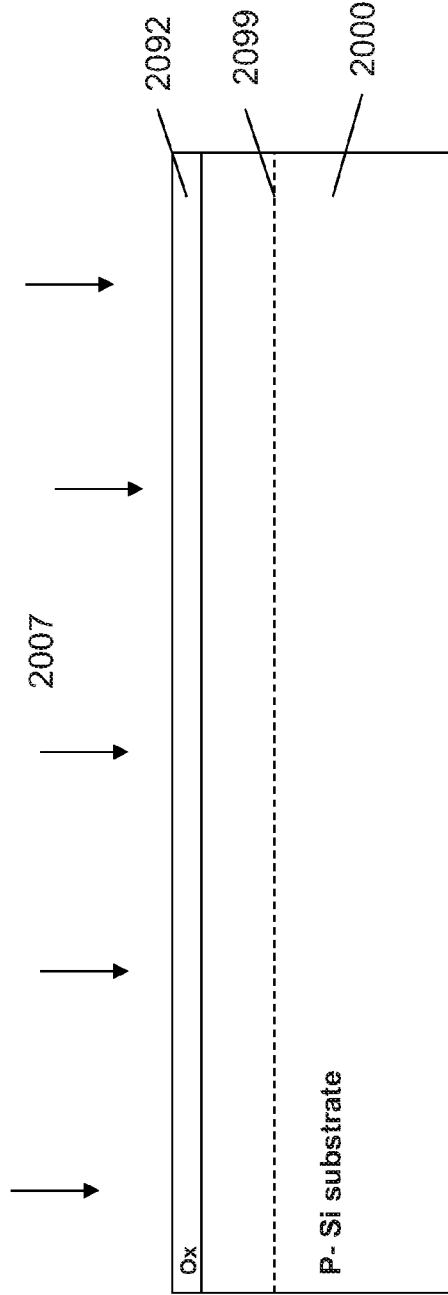


FIG. 20B

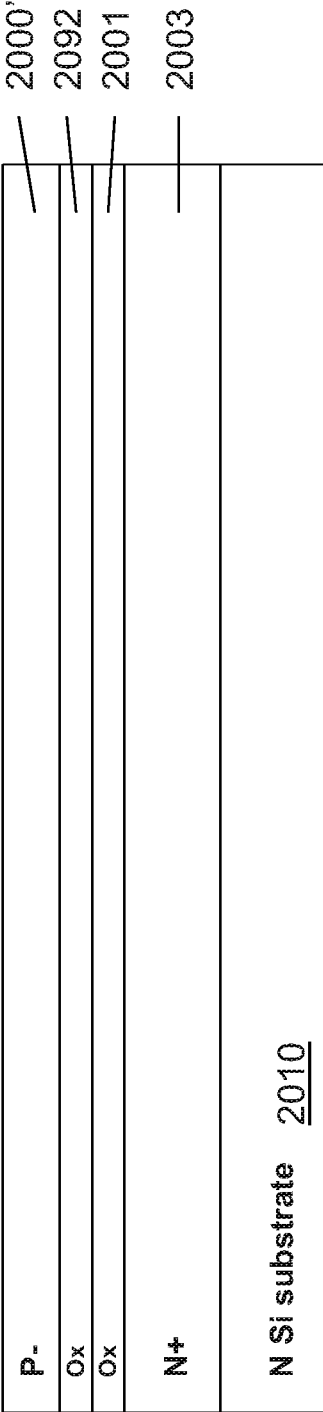


FIG. 20C

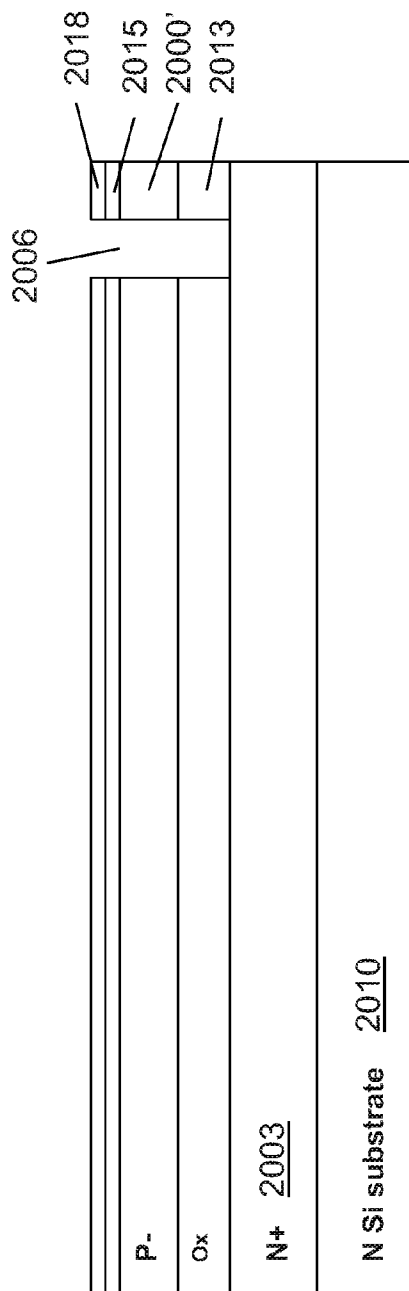


FIG. 20D

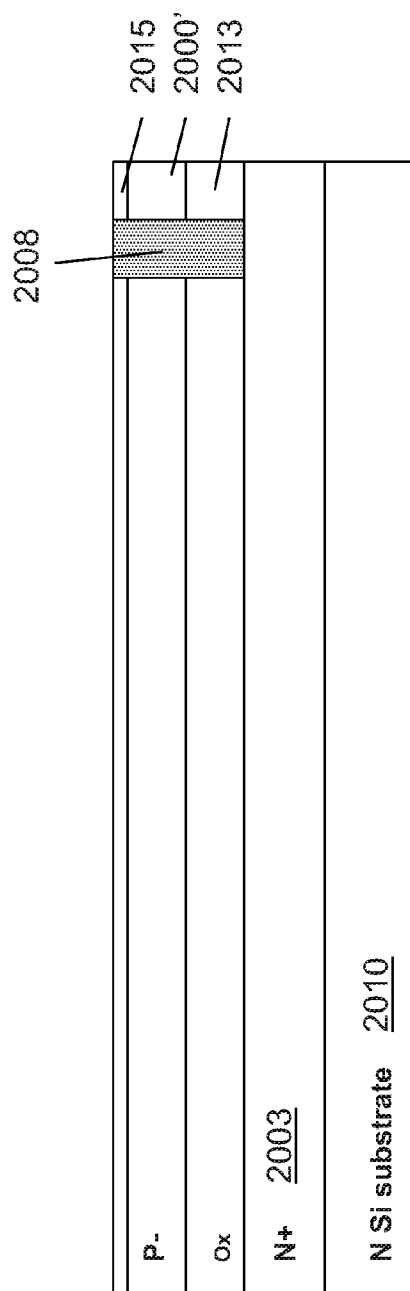
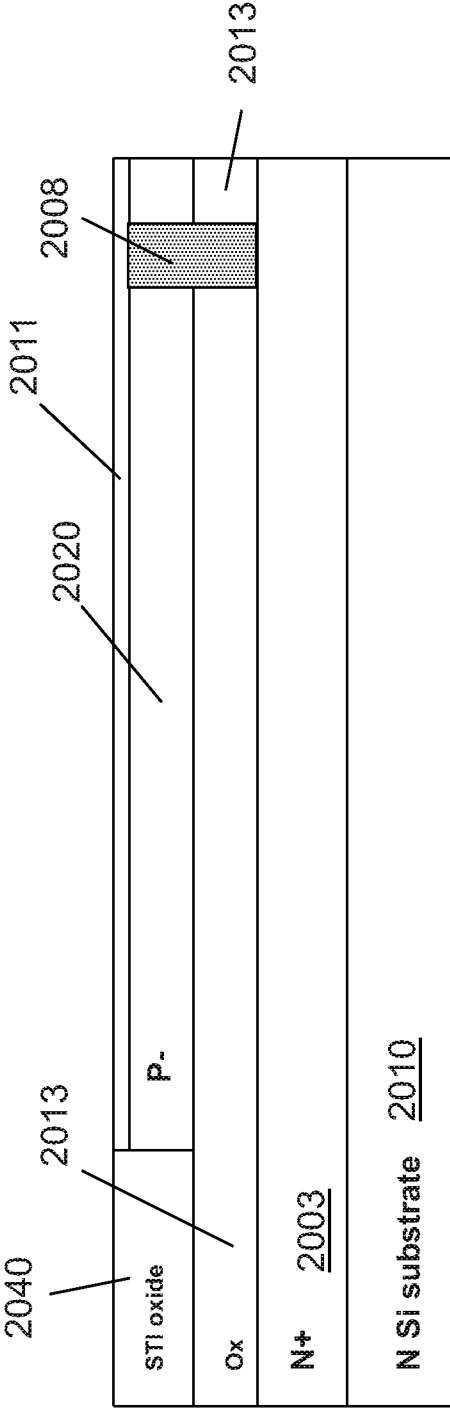
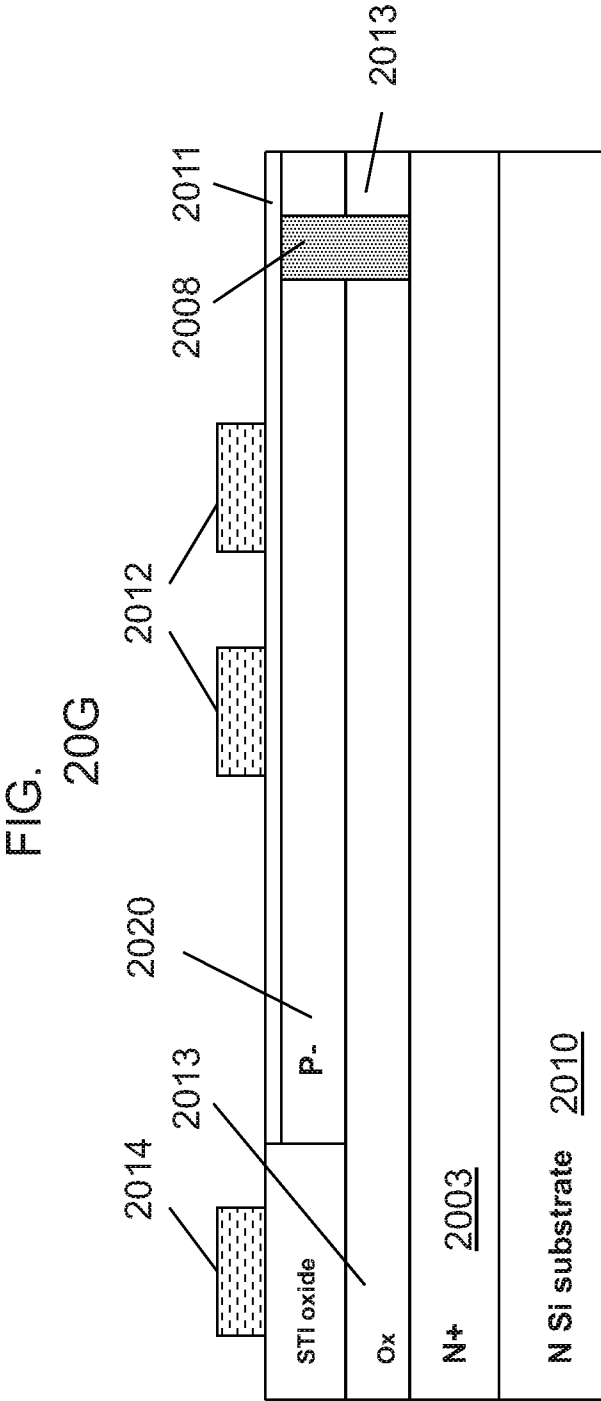


FIG. 20E

FIG. 20F





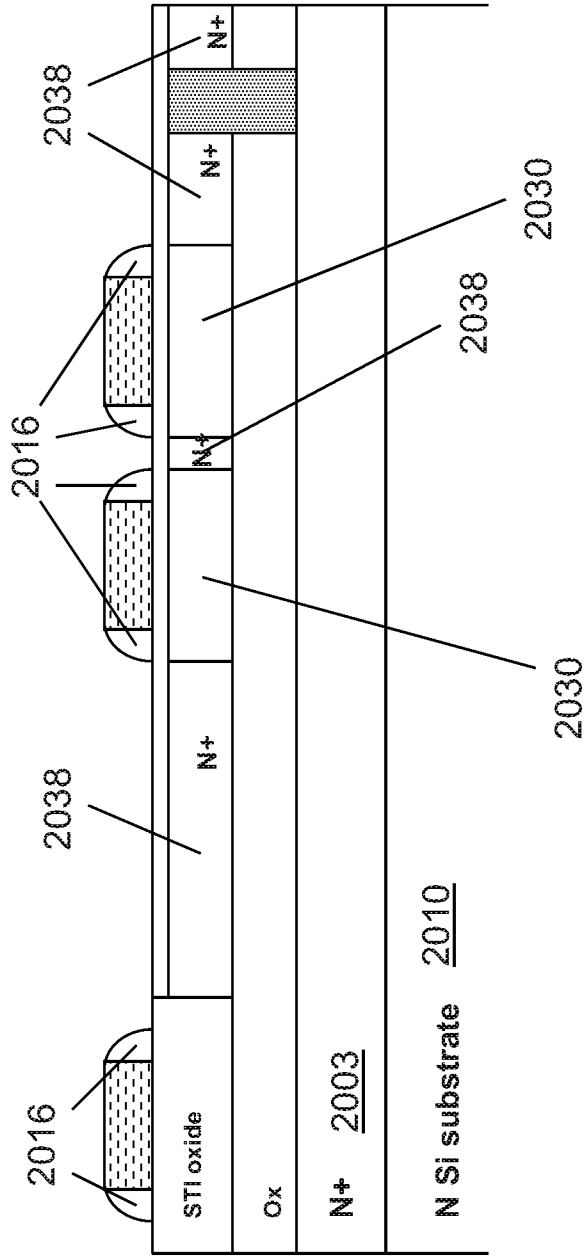


FIG. 20H

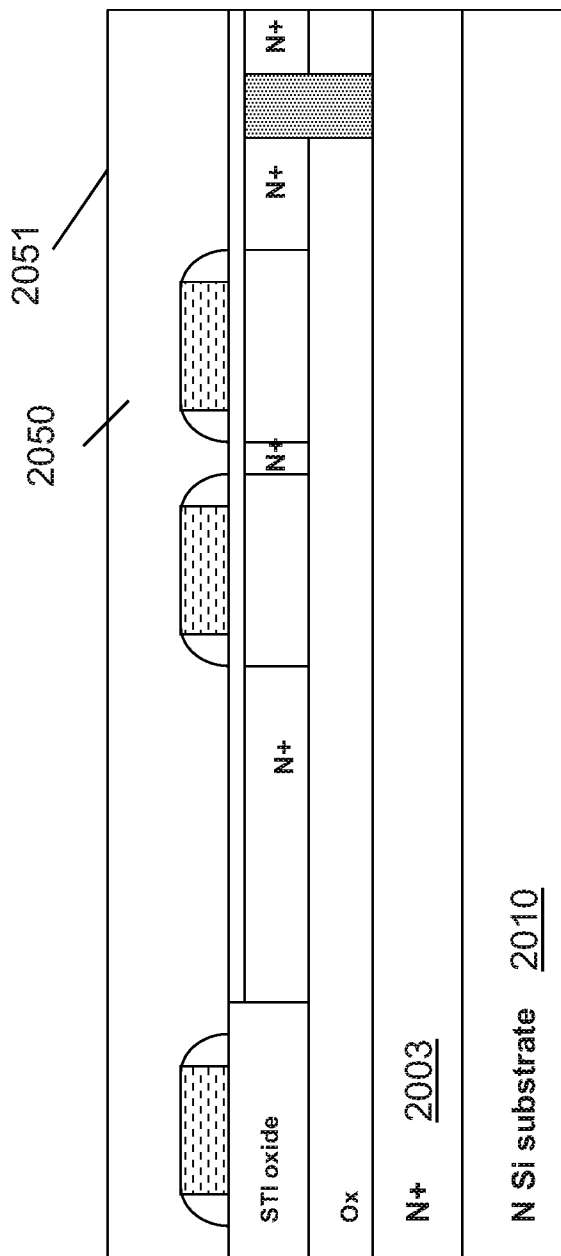


FIG. 20I

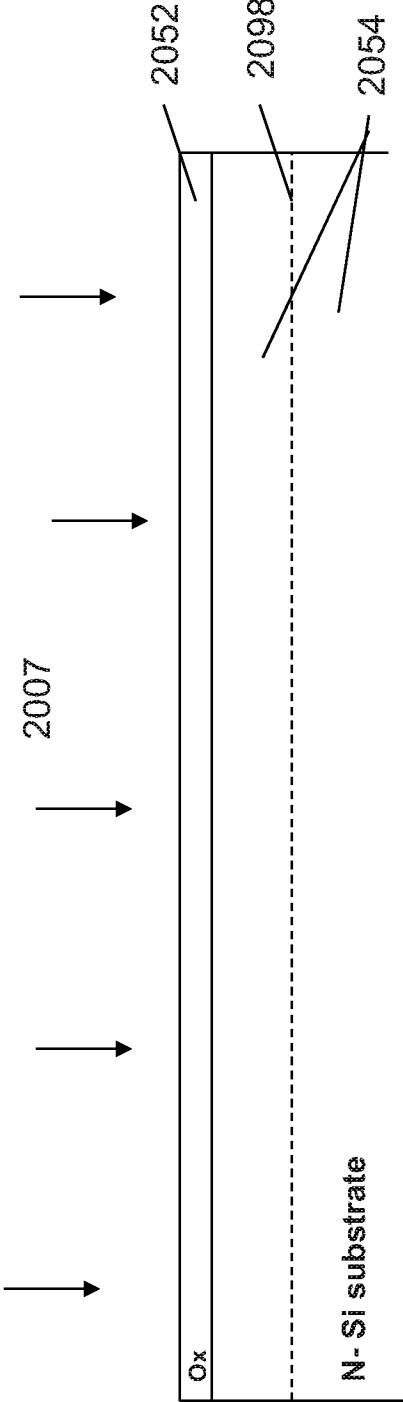


FIG. 20J



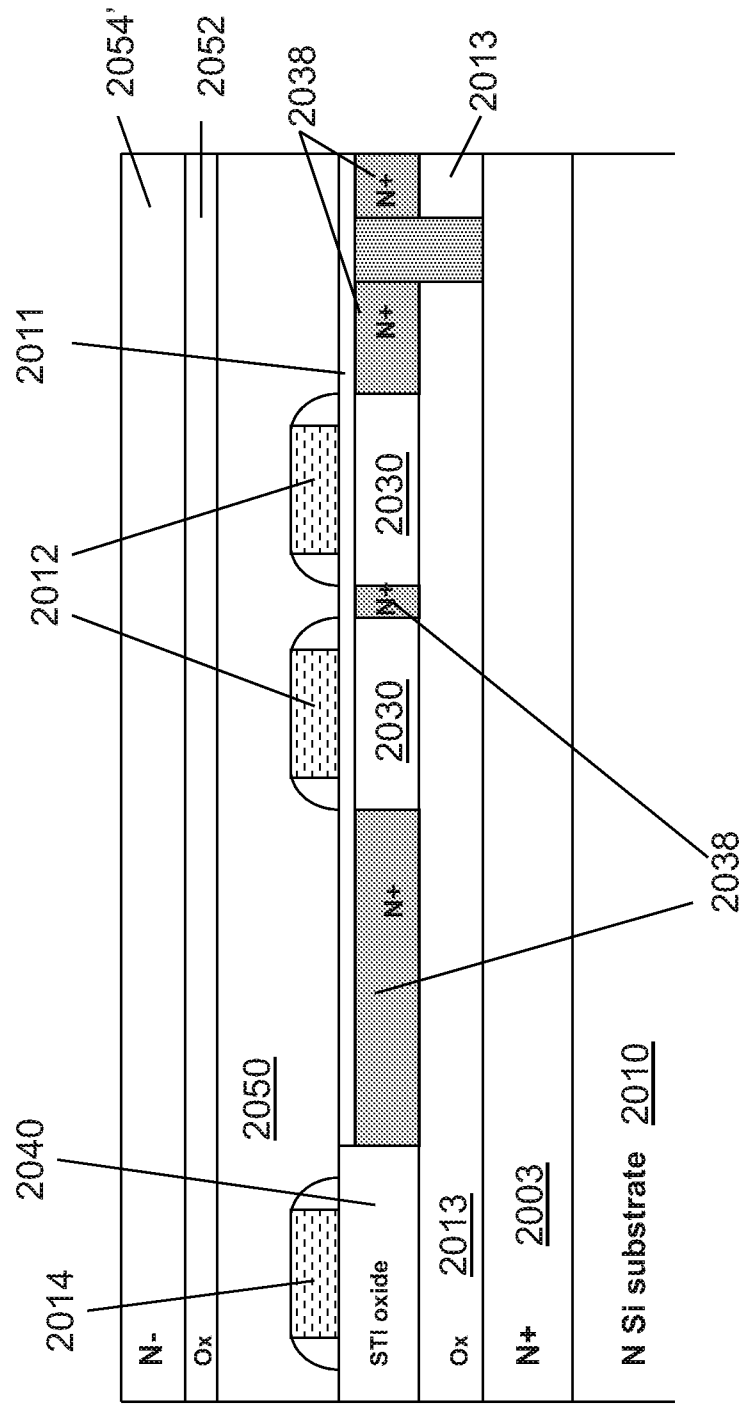


FIG. 20K

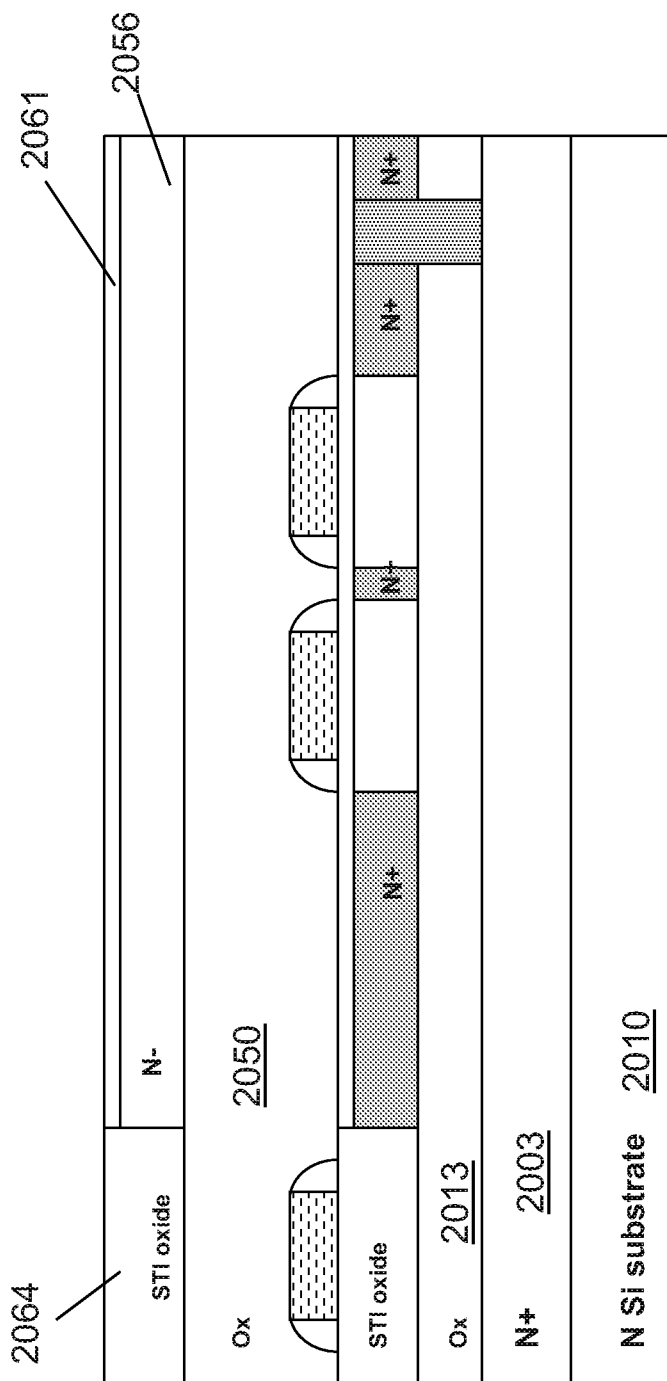


FIG. 20L

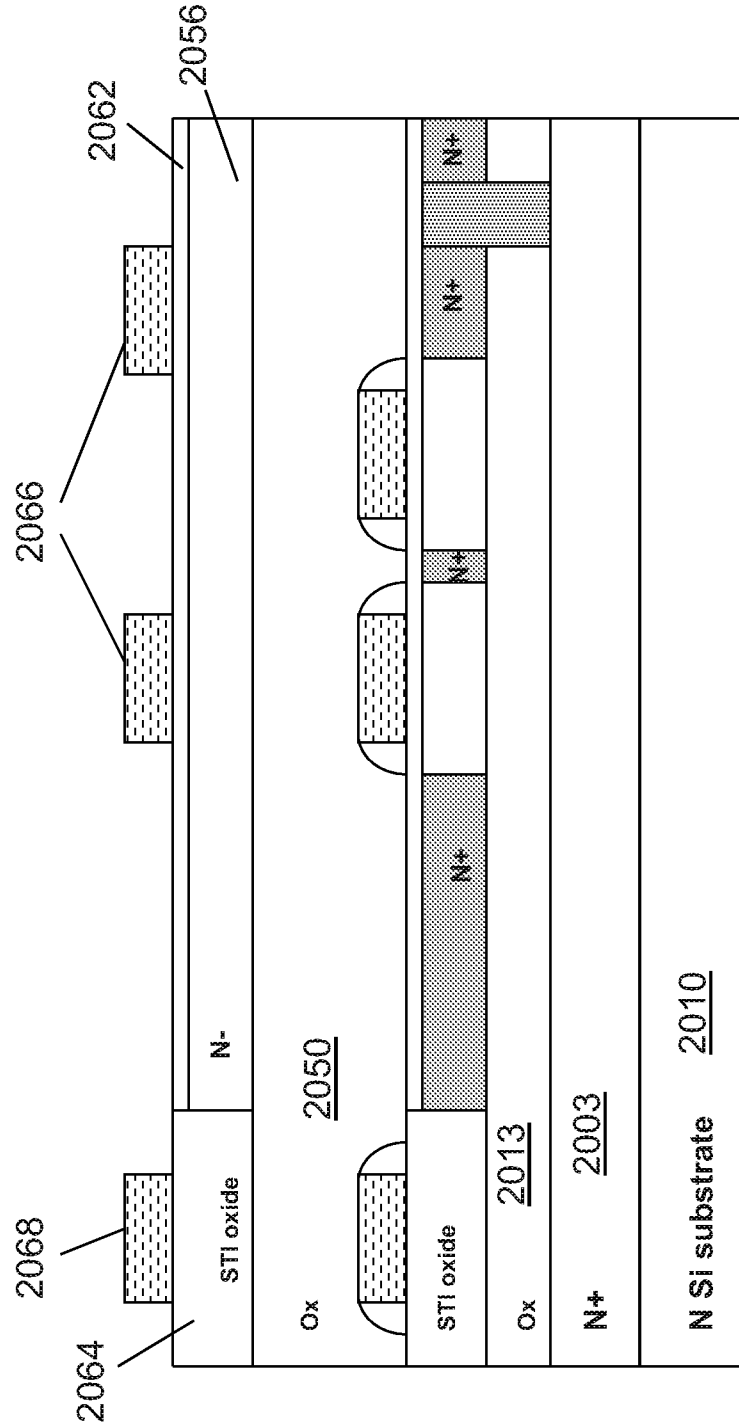


FIG. 20M

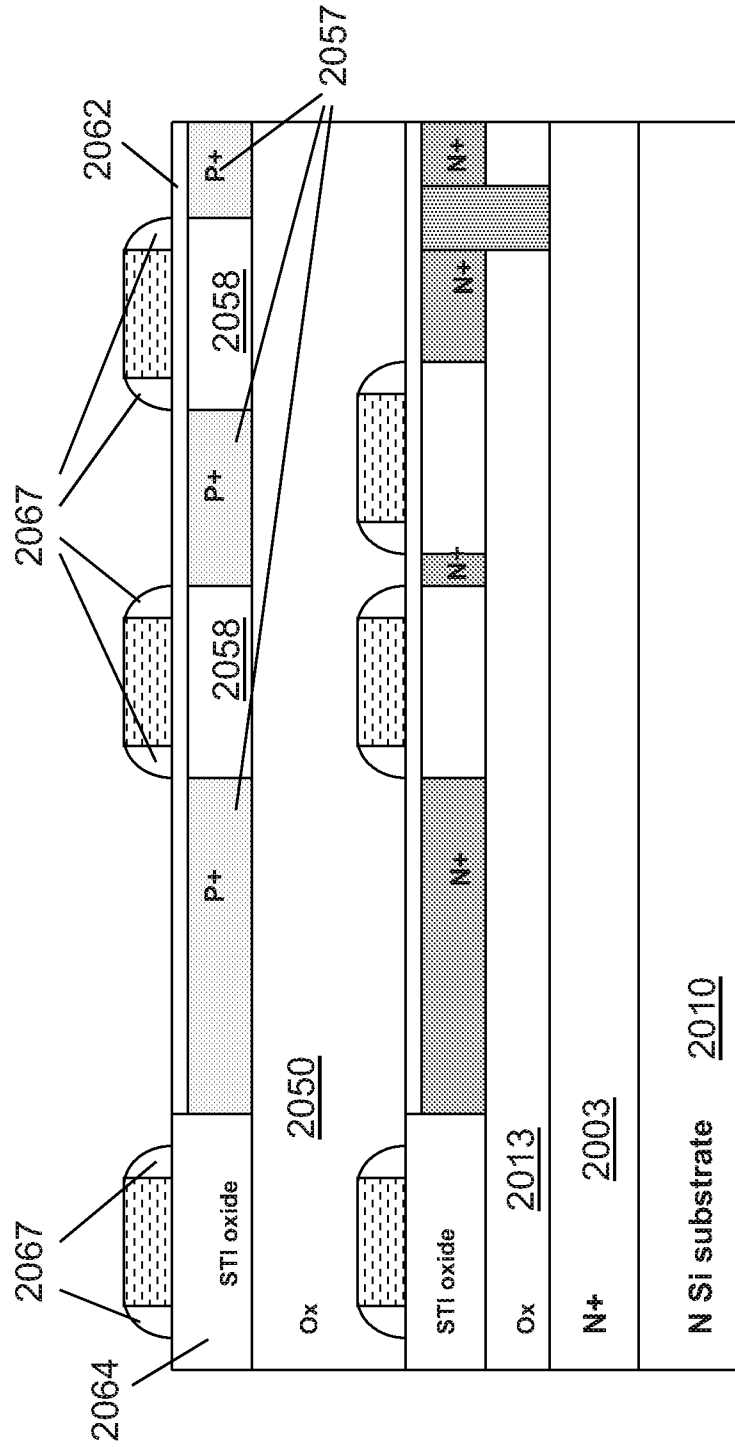


FIG. 20N

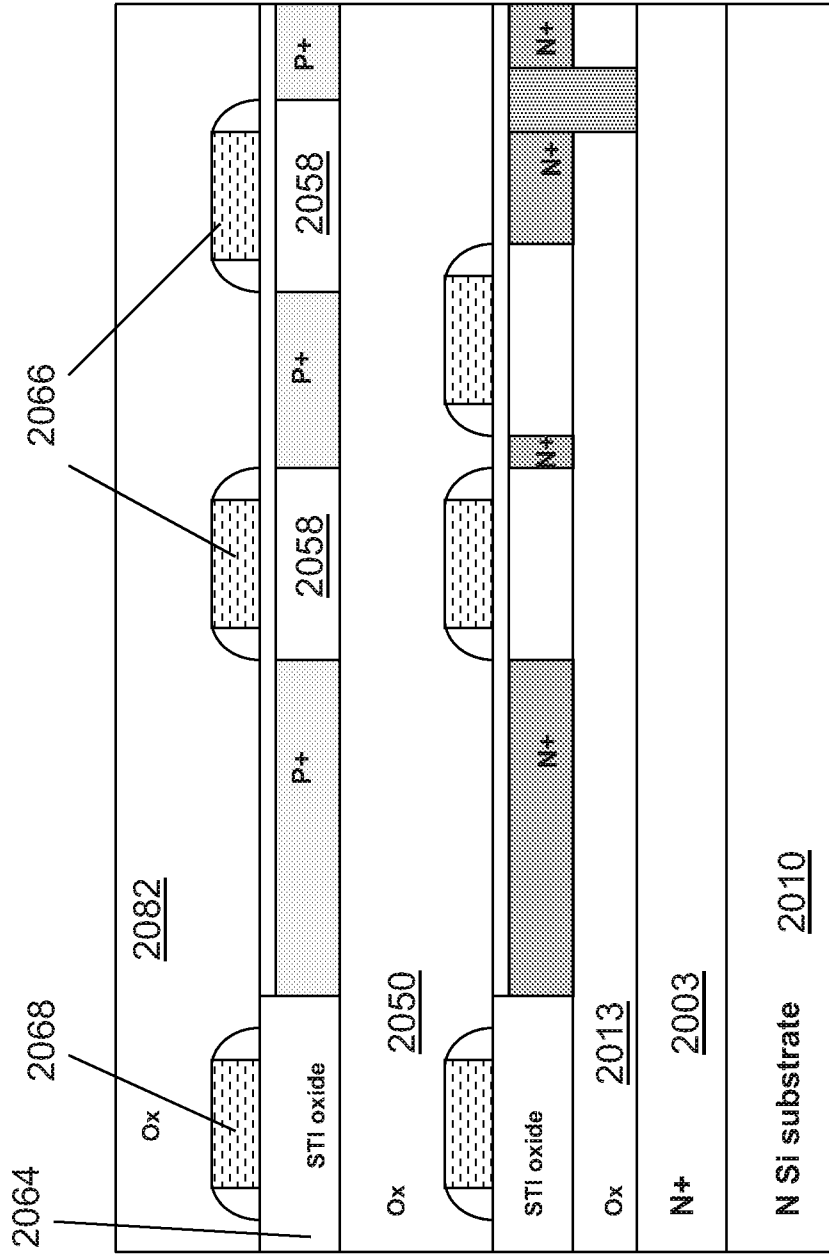


FIG. 200

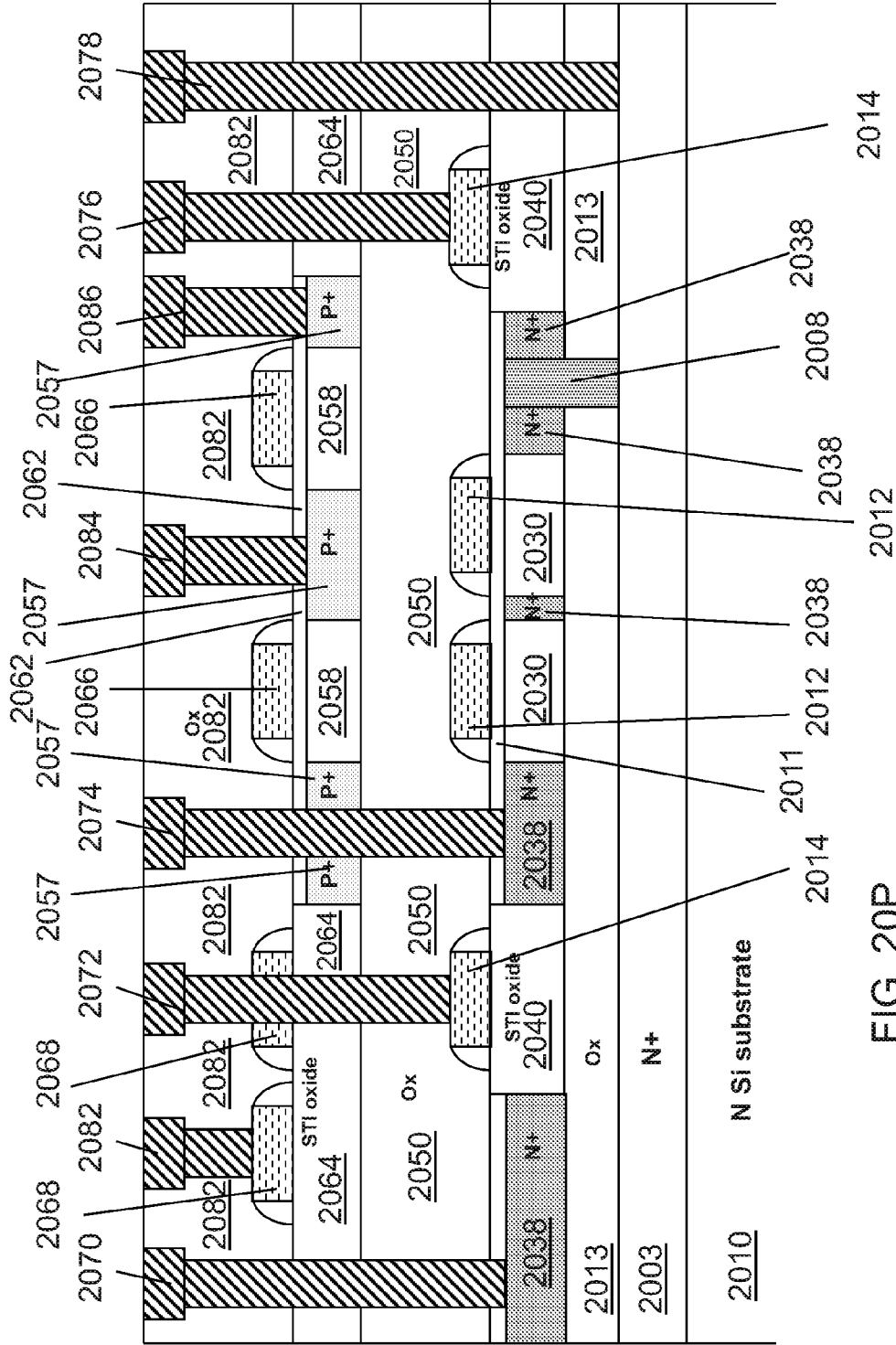
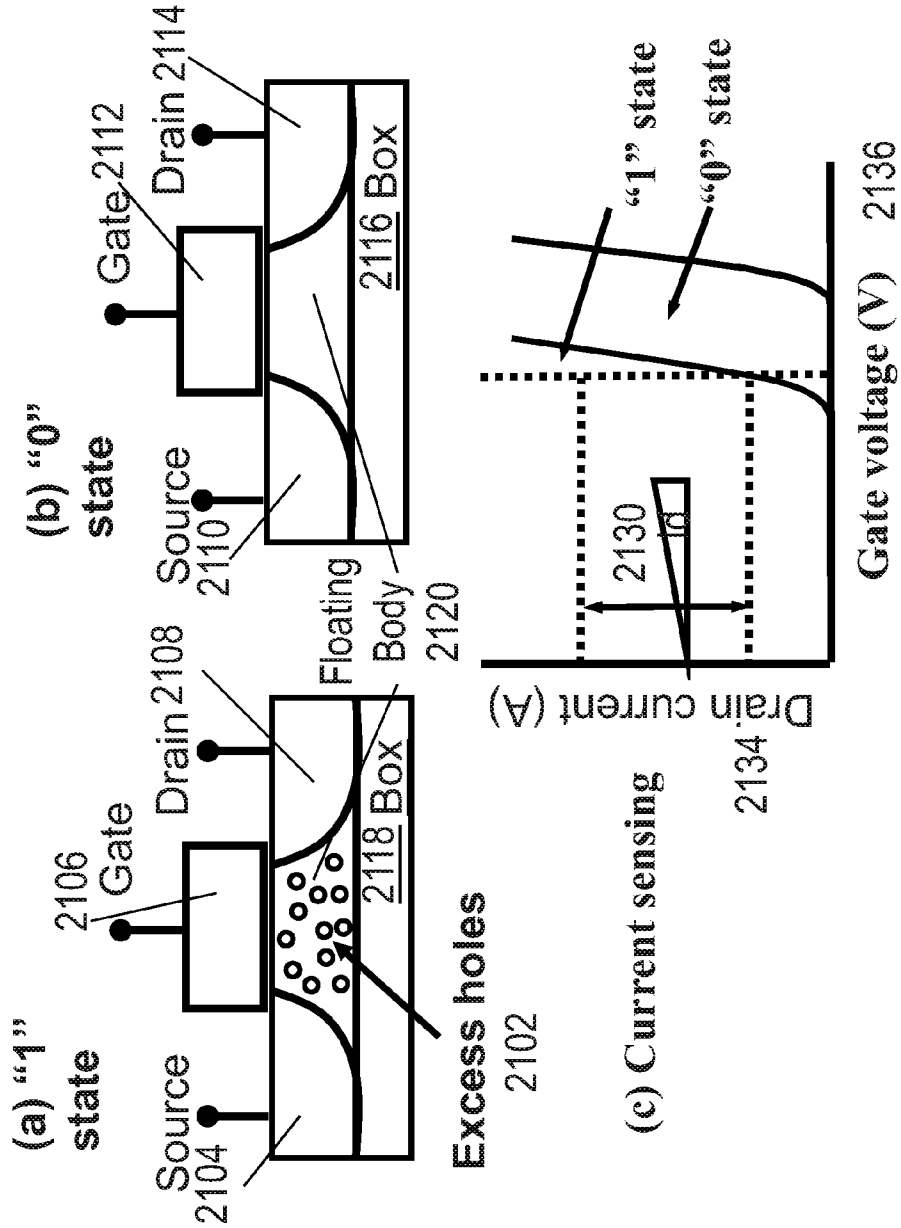


FIG. 20P

FIG. 21 Prior Art



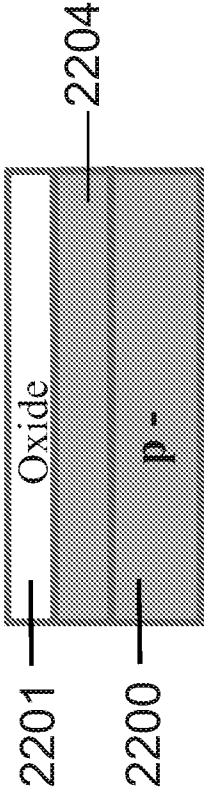


FIG. 22A



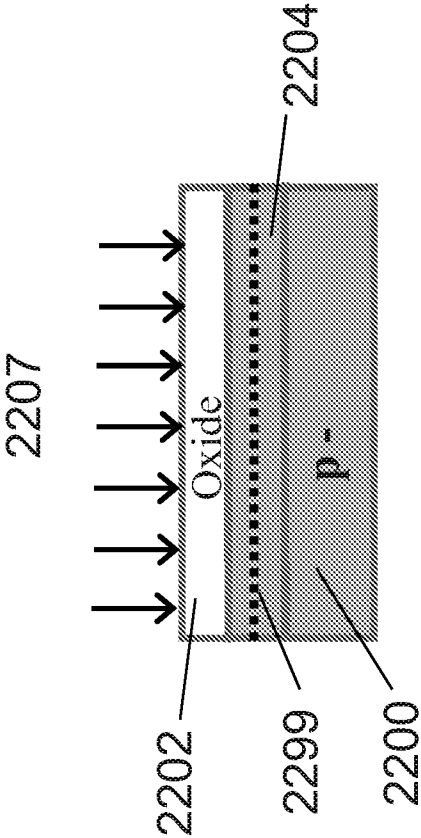


FIG. 22B

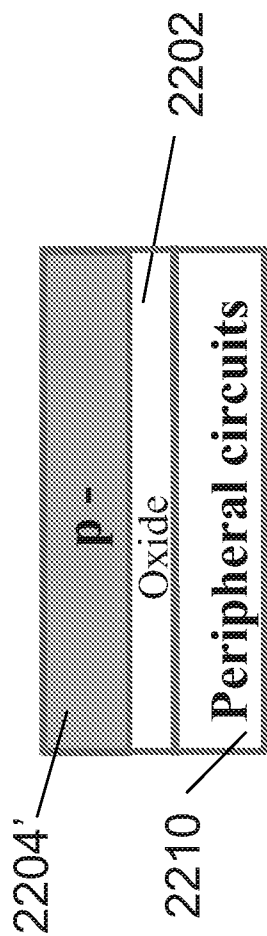


FIG. 22C

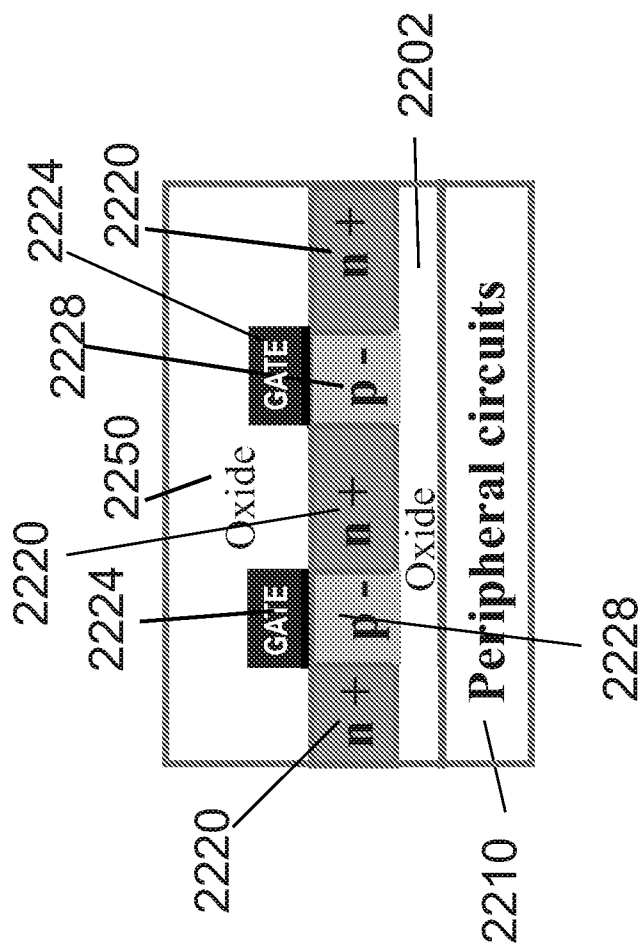


FIG. 22D

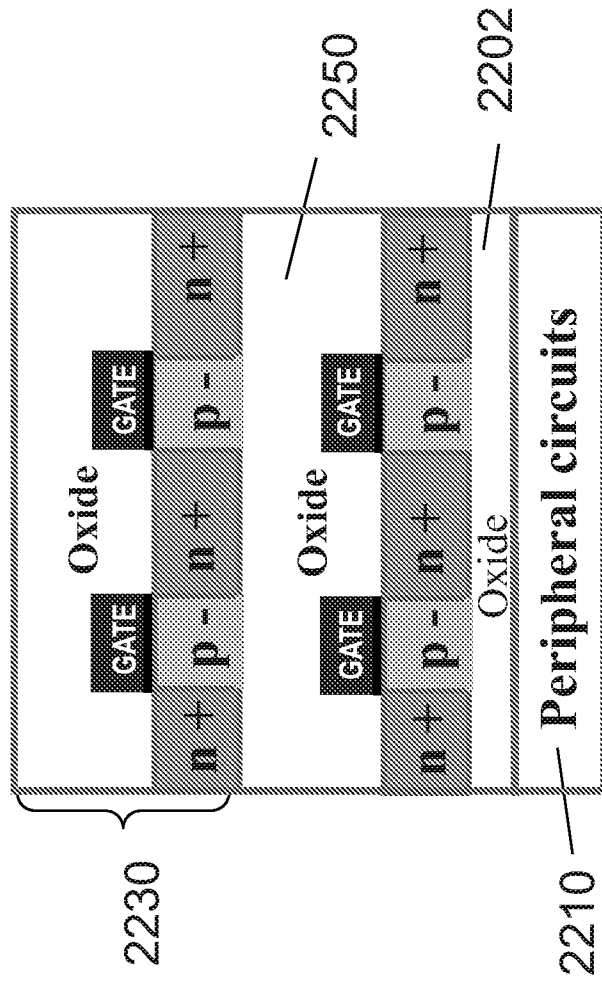


FIG. 22E

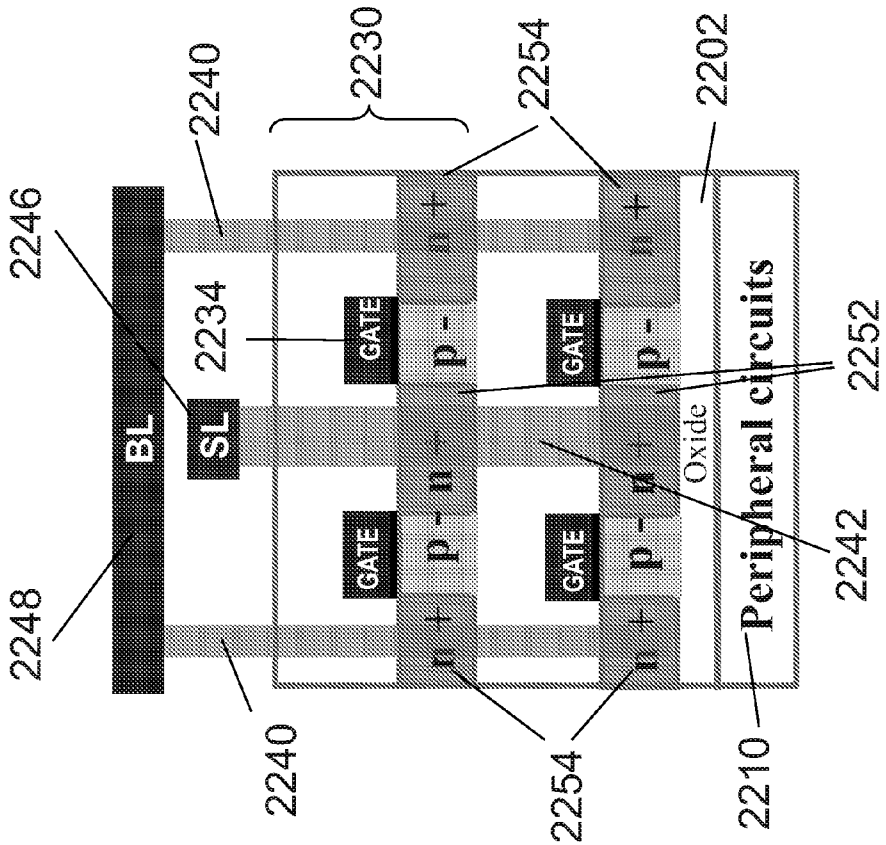


FIG. 22F

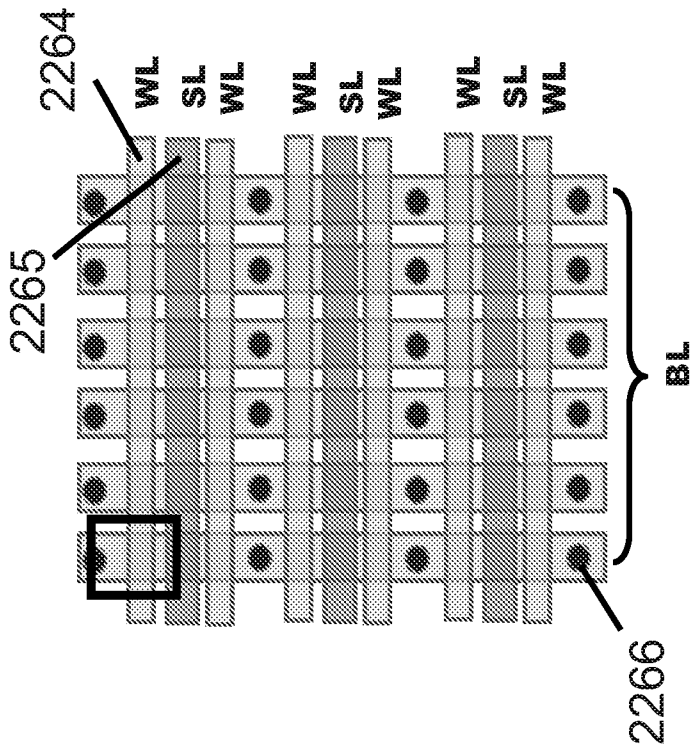


FIG. 22G

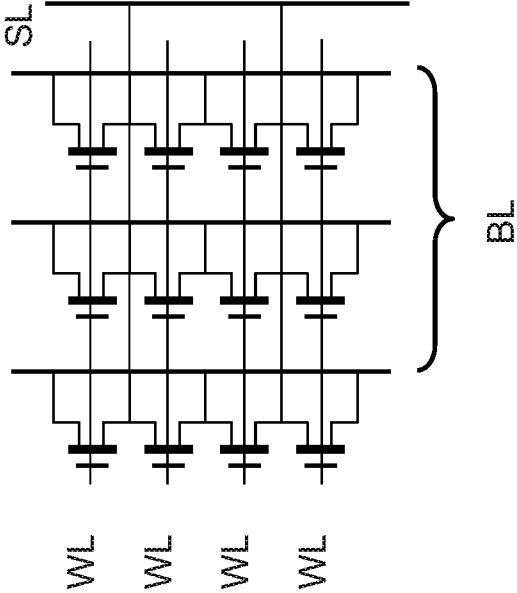


Fig. 22H

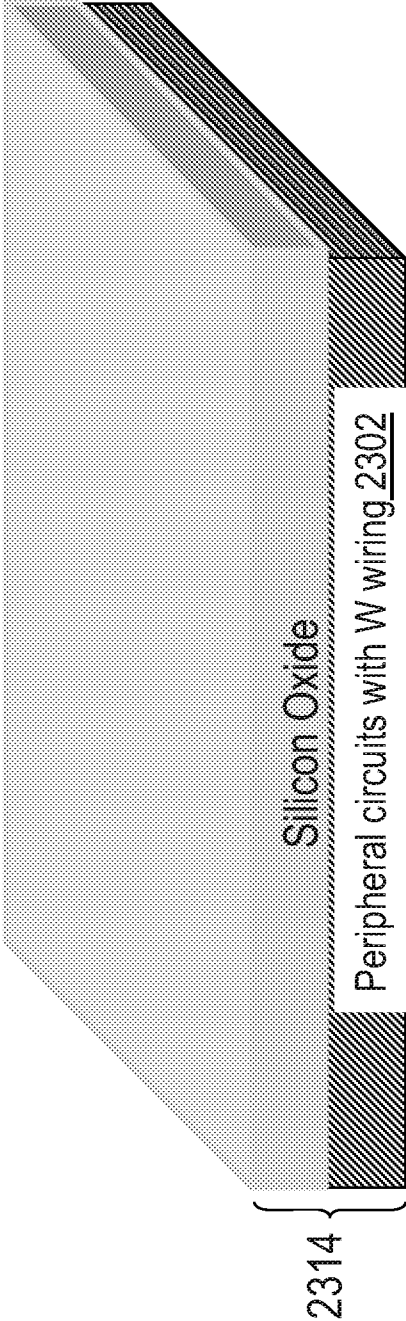


FIG. 23A



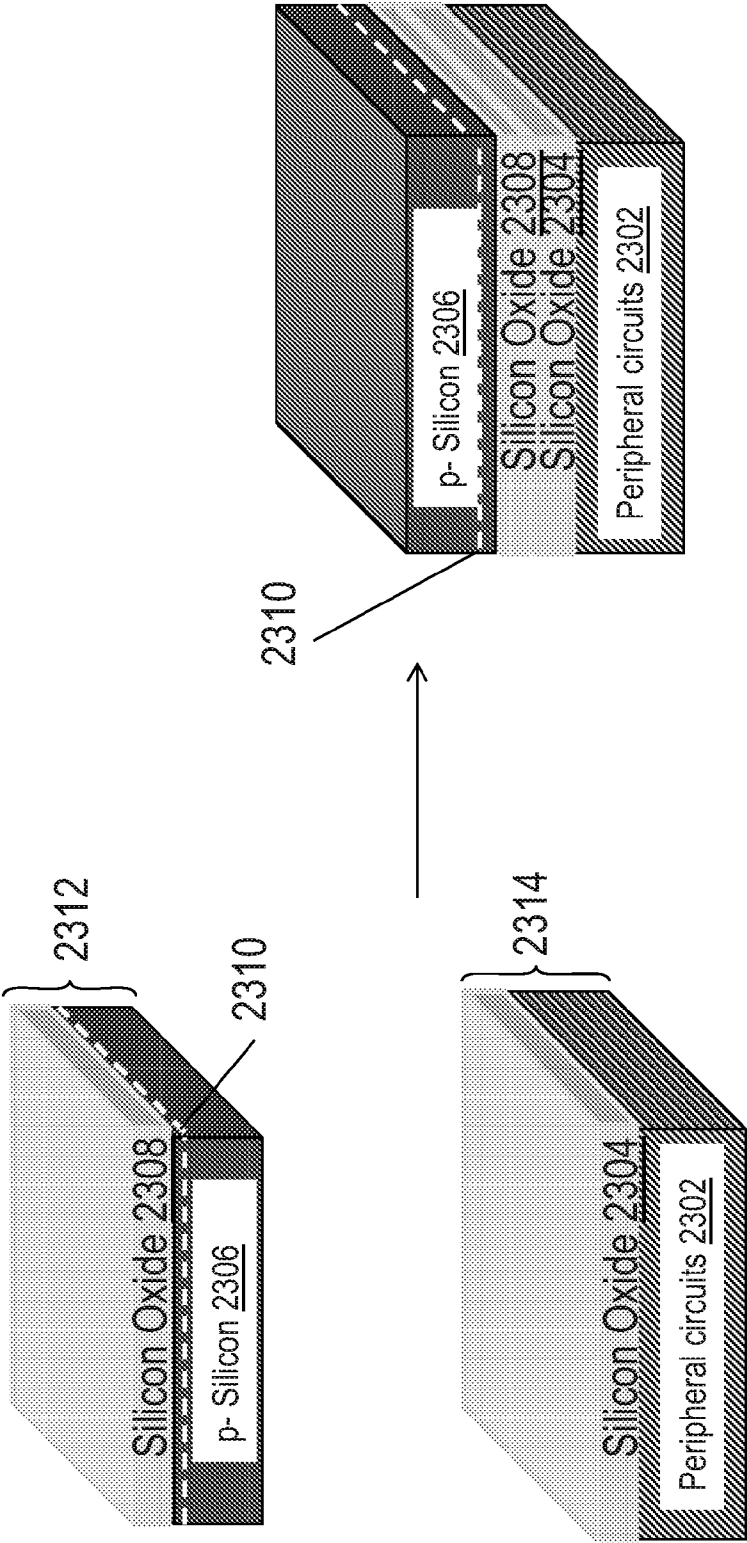


FIG. 23B

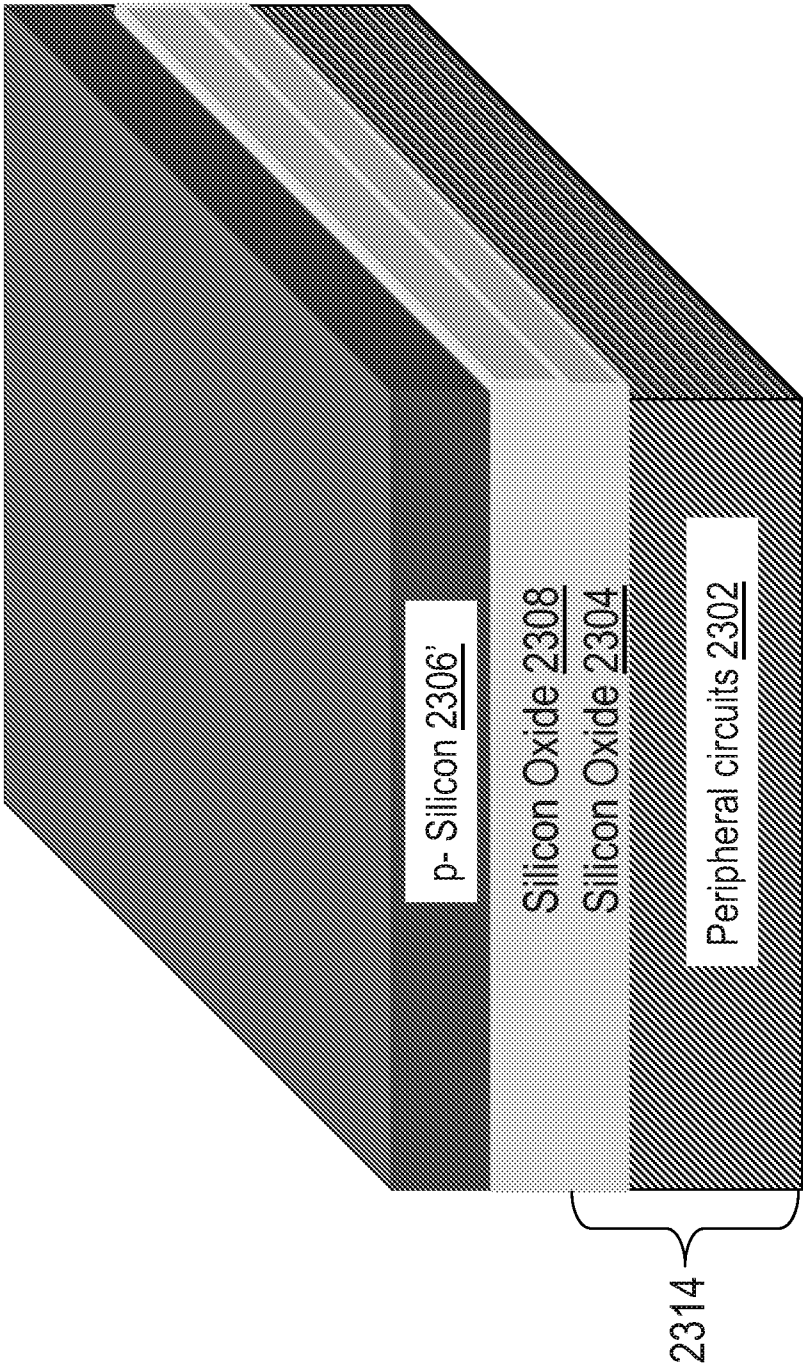


FIG. 23C

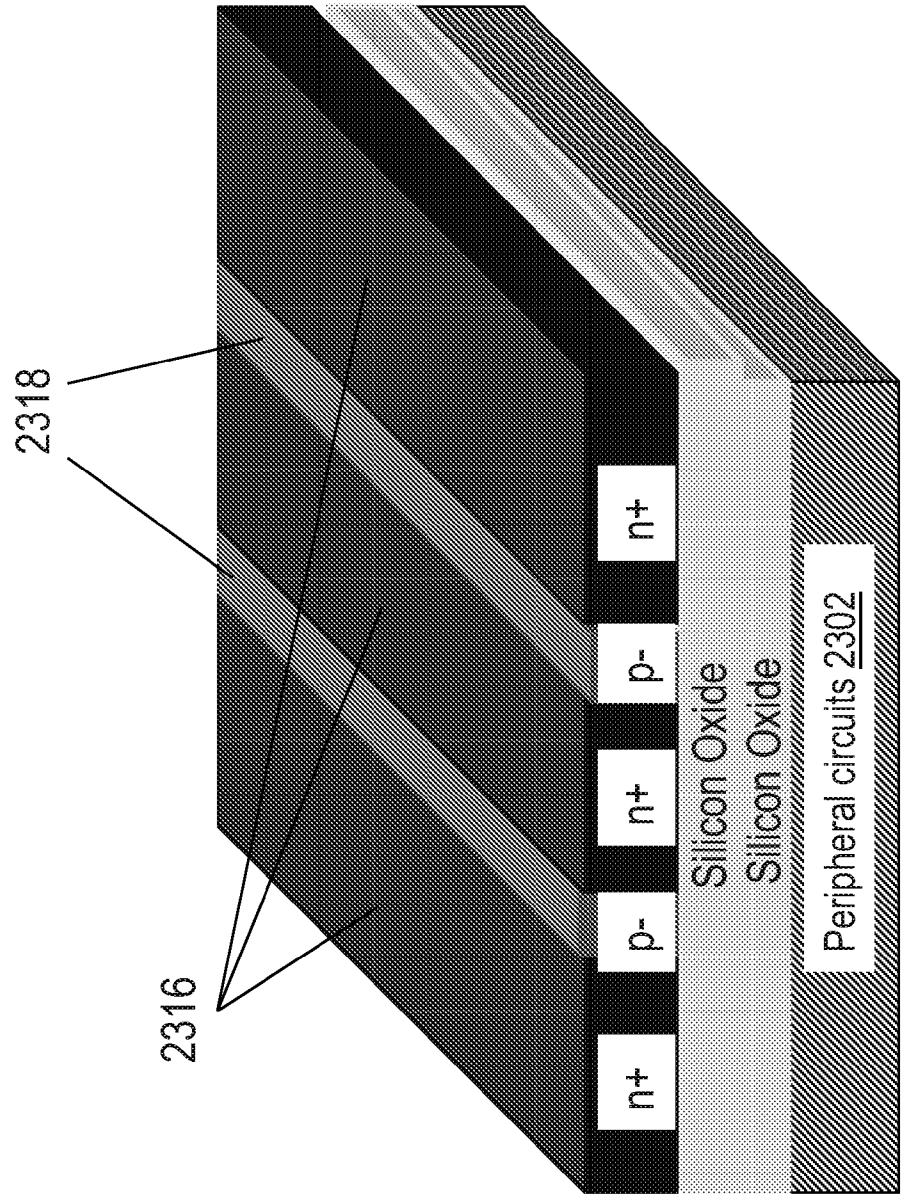


FIG. 23D

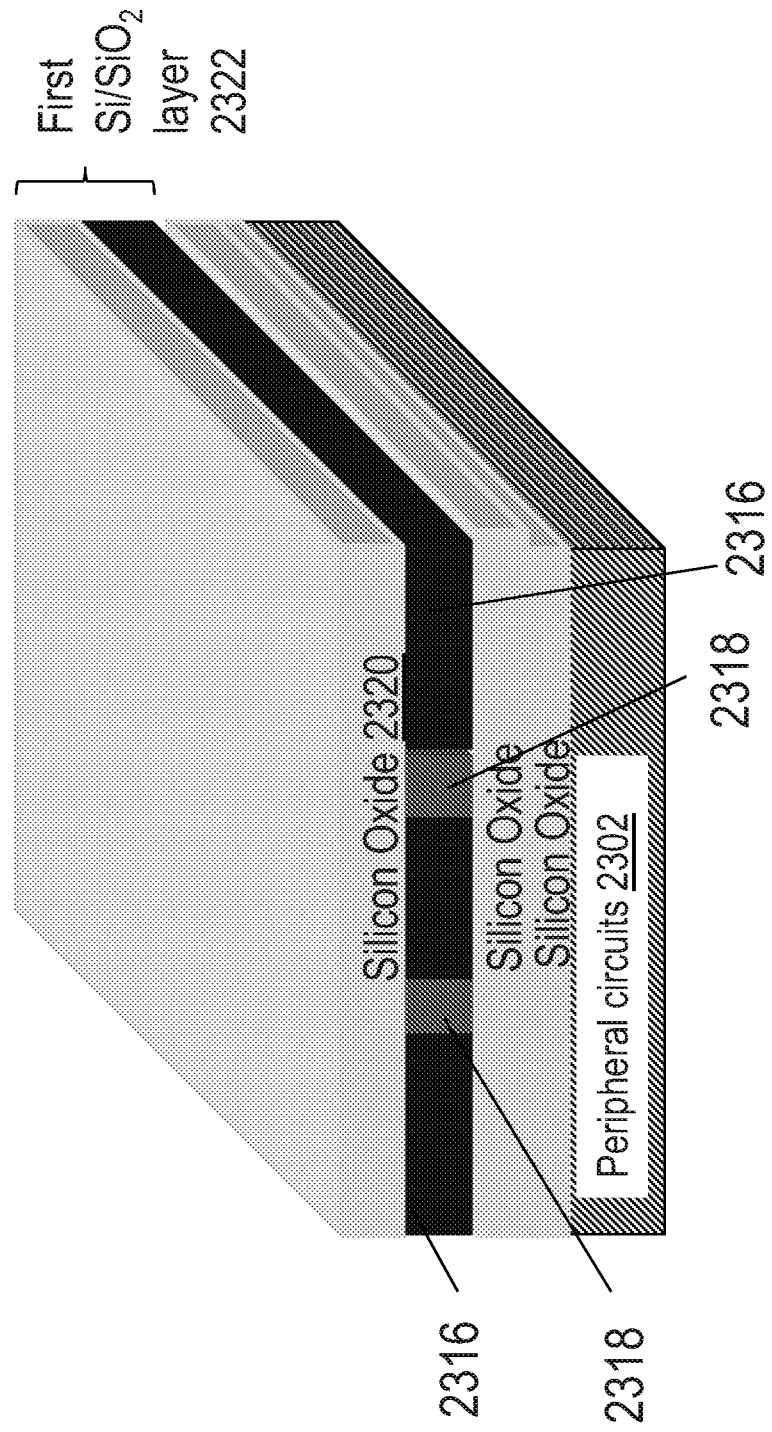


FIG. 23E

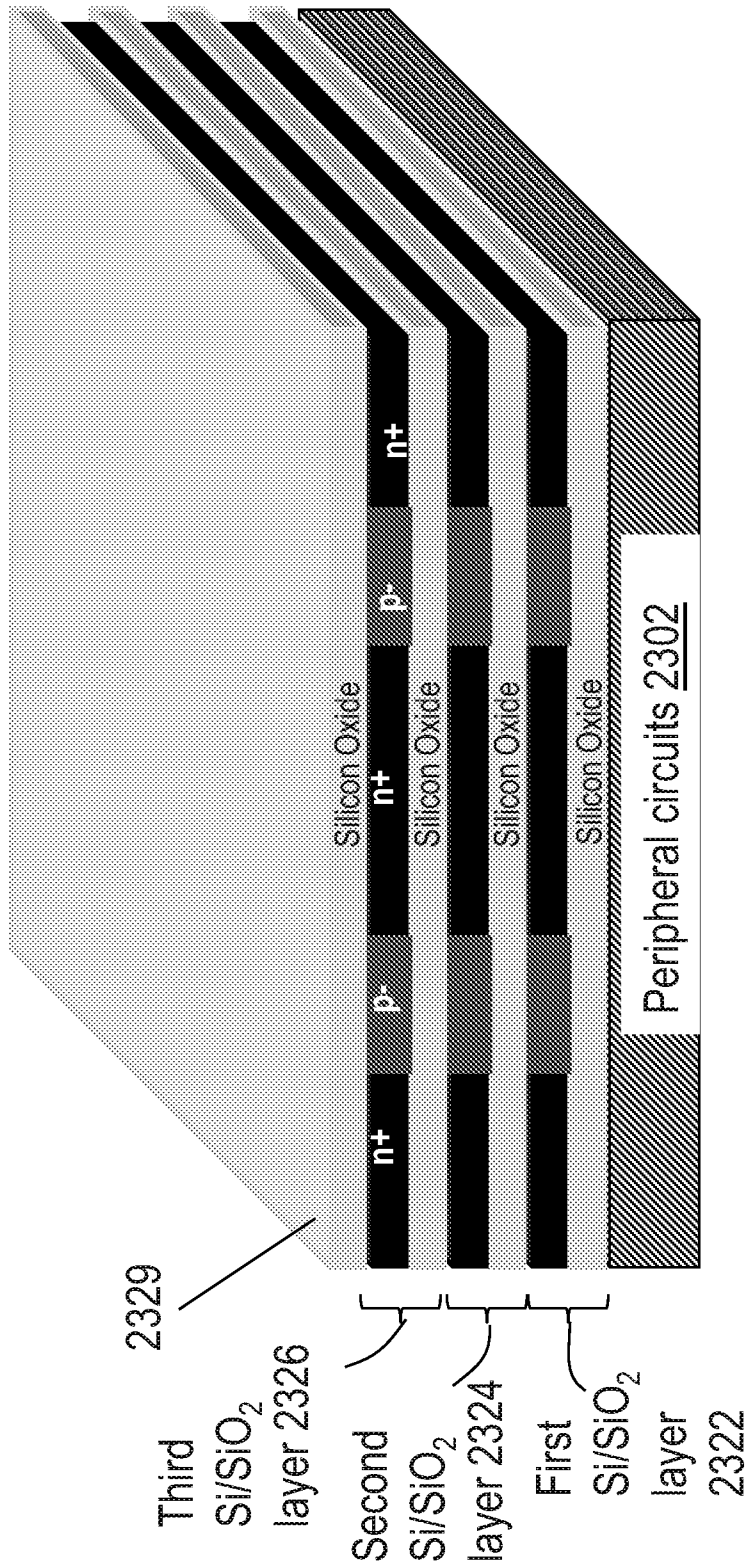
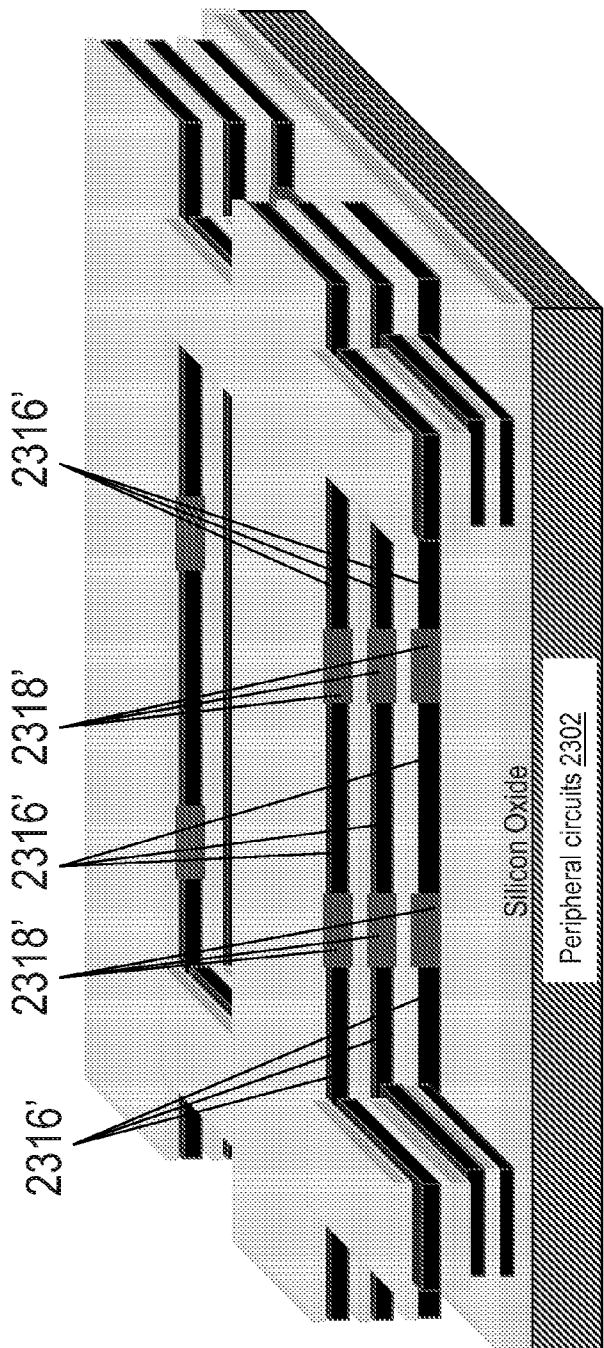


FIG. 23F



Symbols

- p- Silicon 2318'
- Silicon oxide
- n+ Silicon 2316'

FIG. 23G

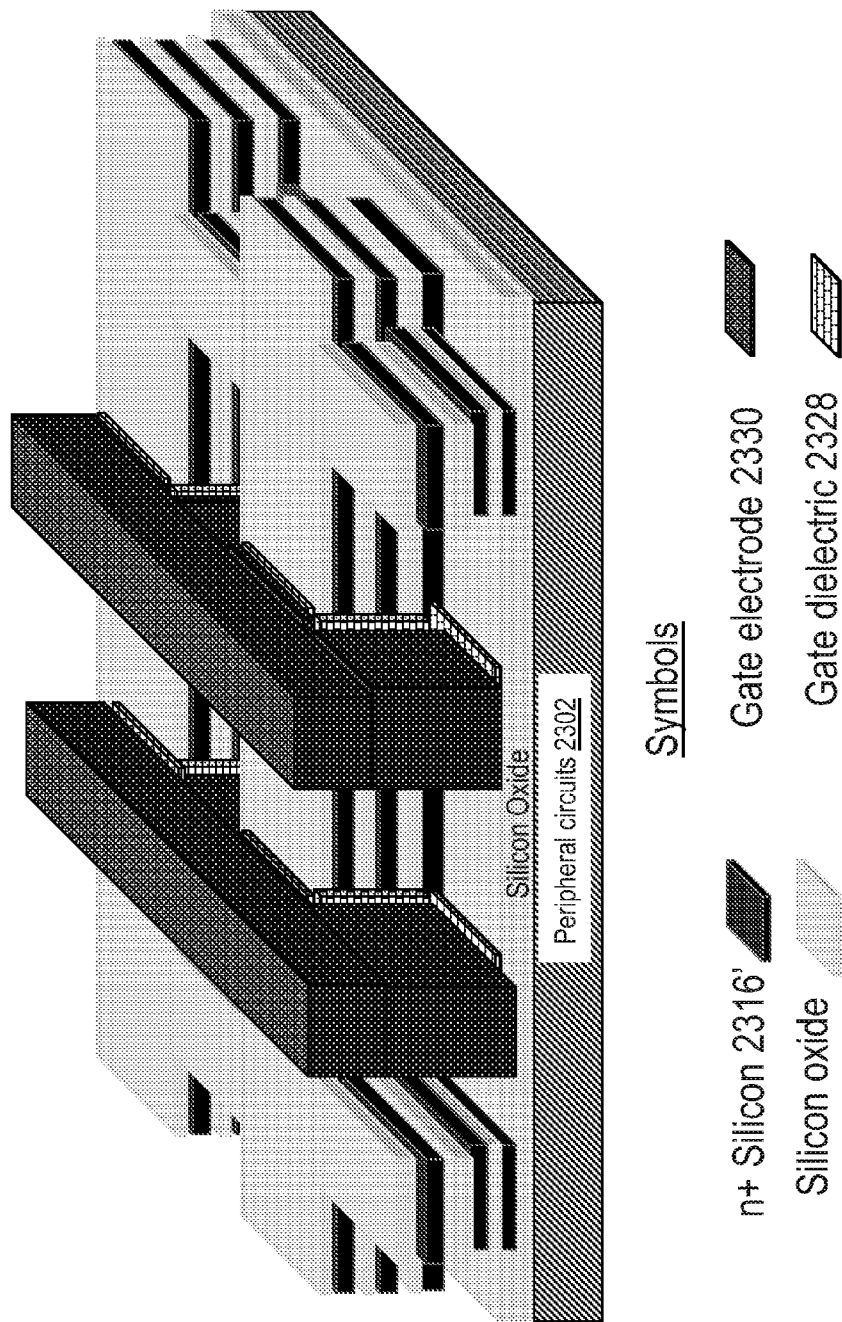
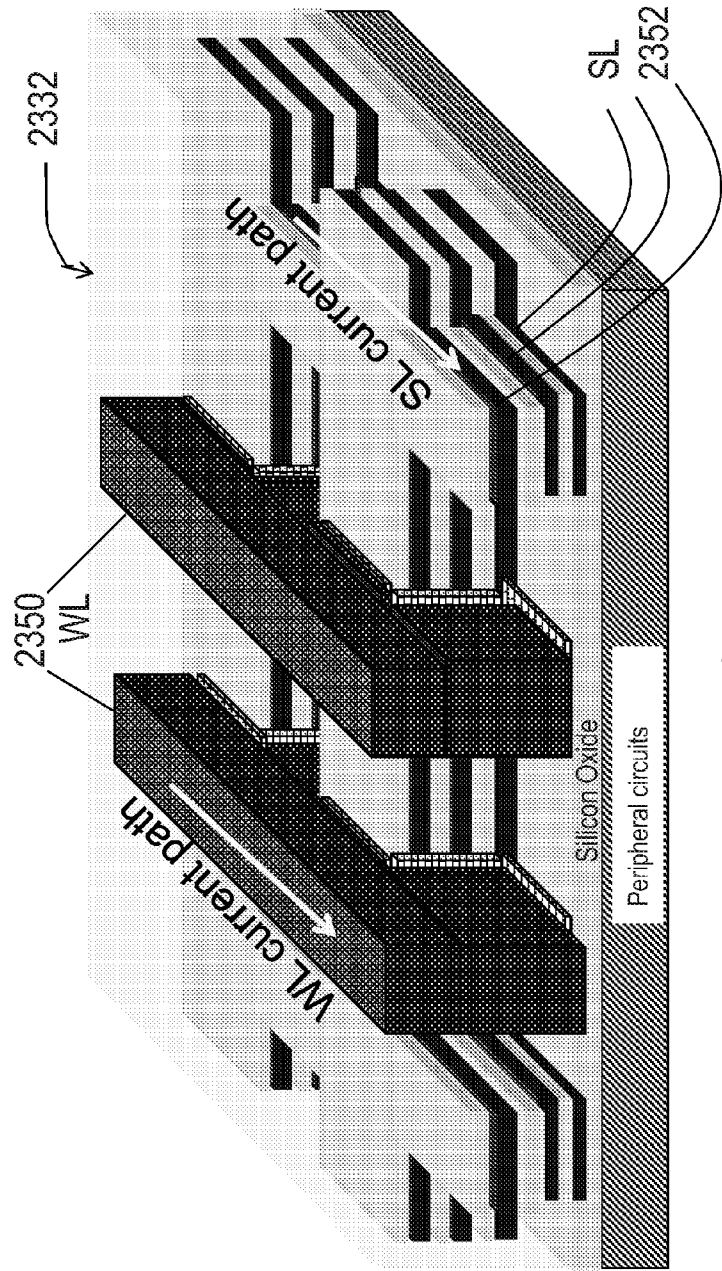


FIG. 23H



Symbols

- Gate dielectric 2328
- Silicon oxide
- Gate electrode 2330
- n+ Silicon 2316'
- Silicon oxide

FIG. 23I



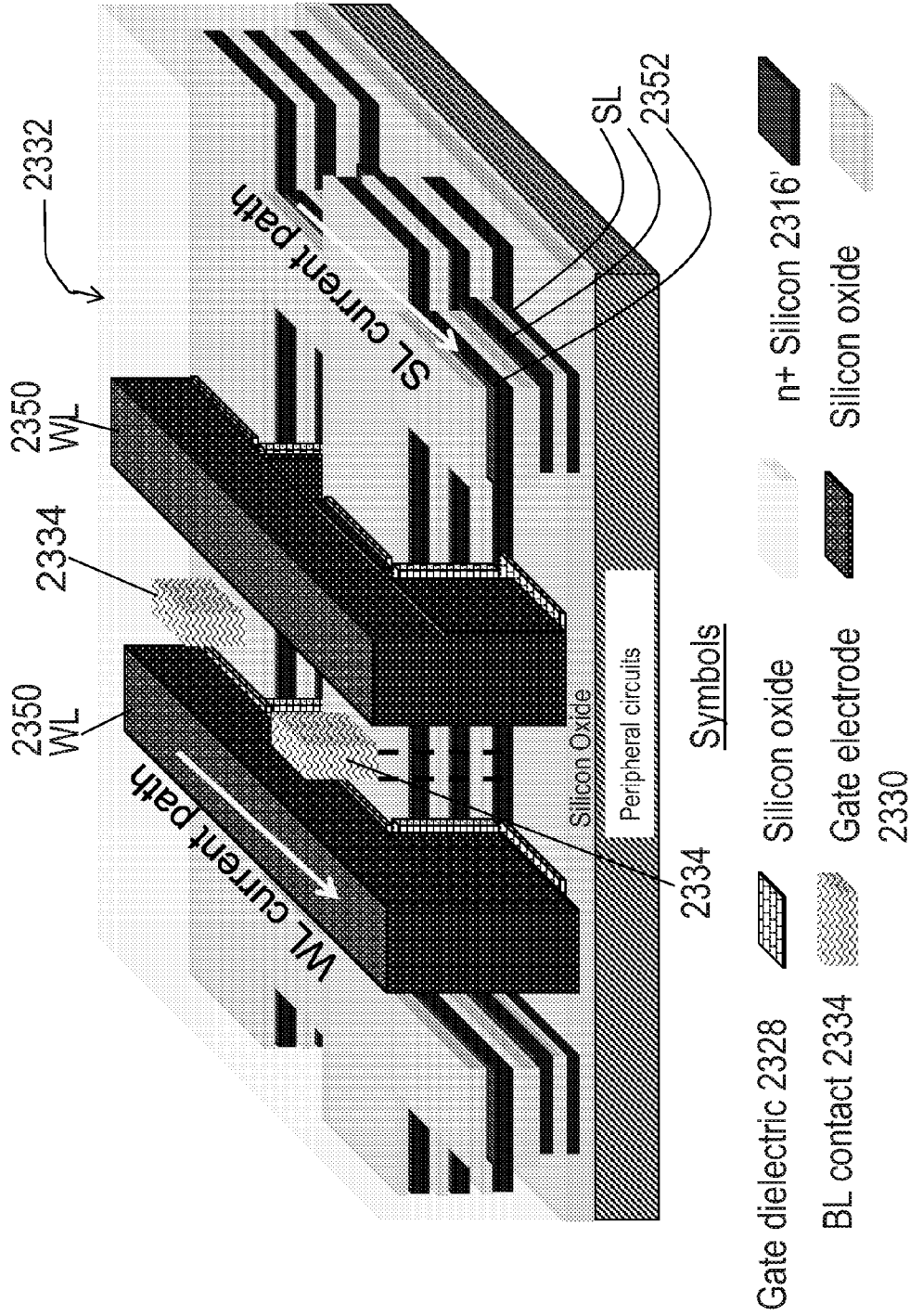


FIG. 23J

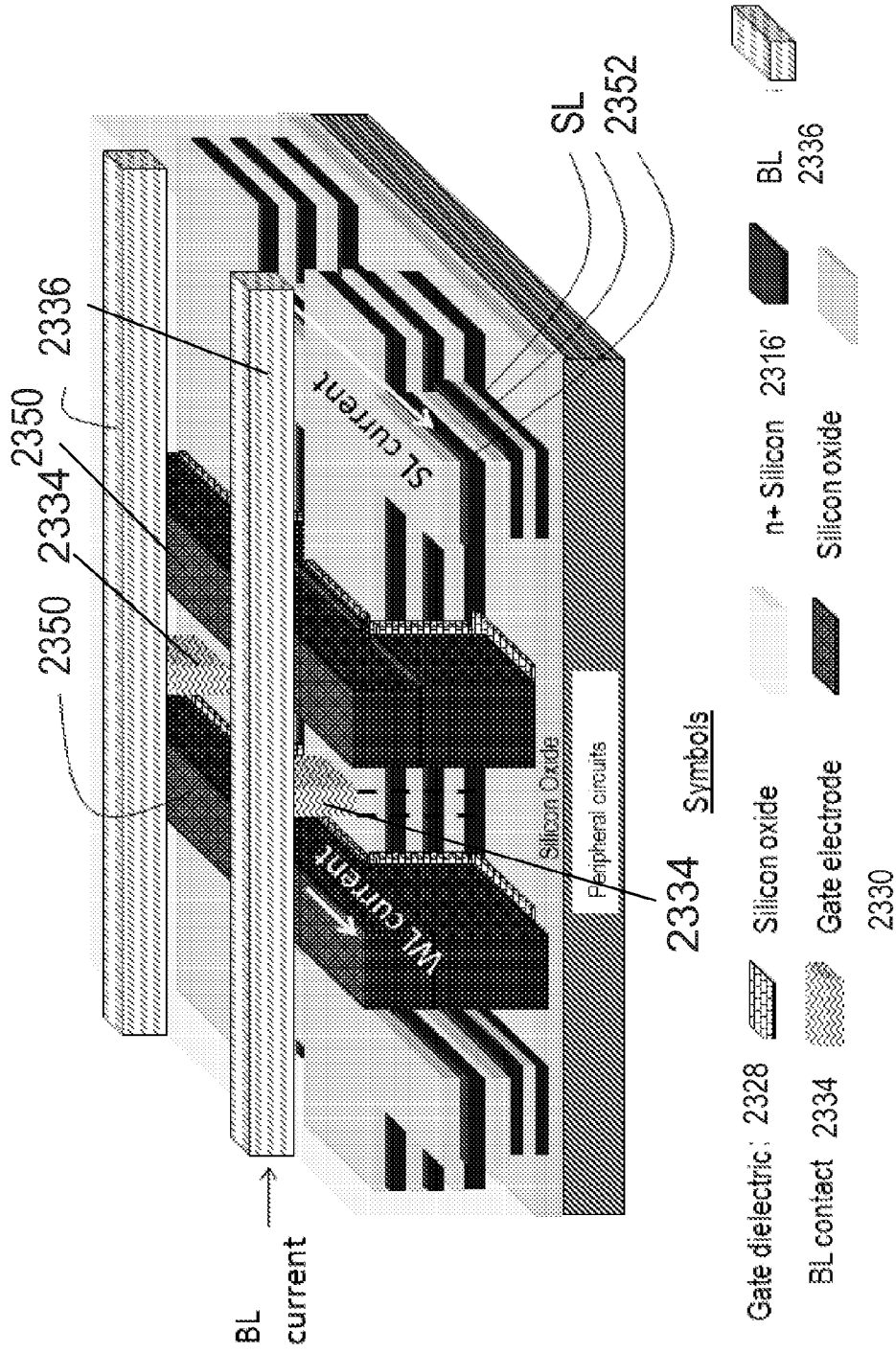


FIG. 23K

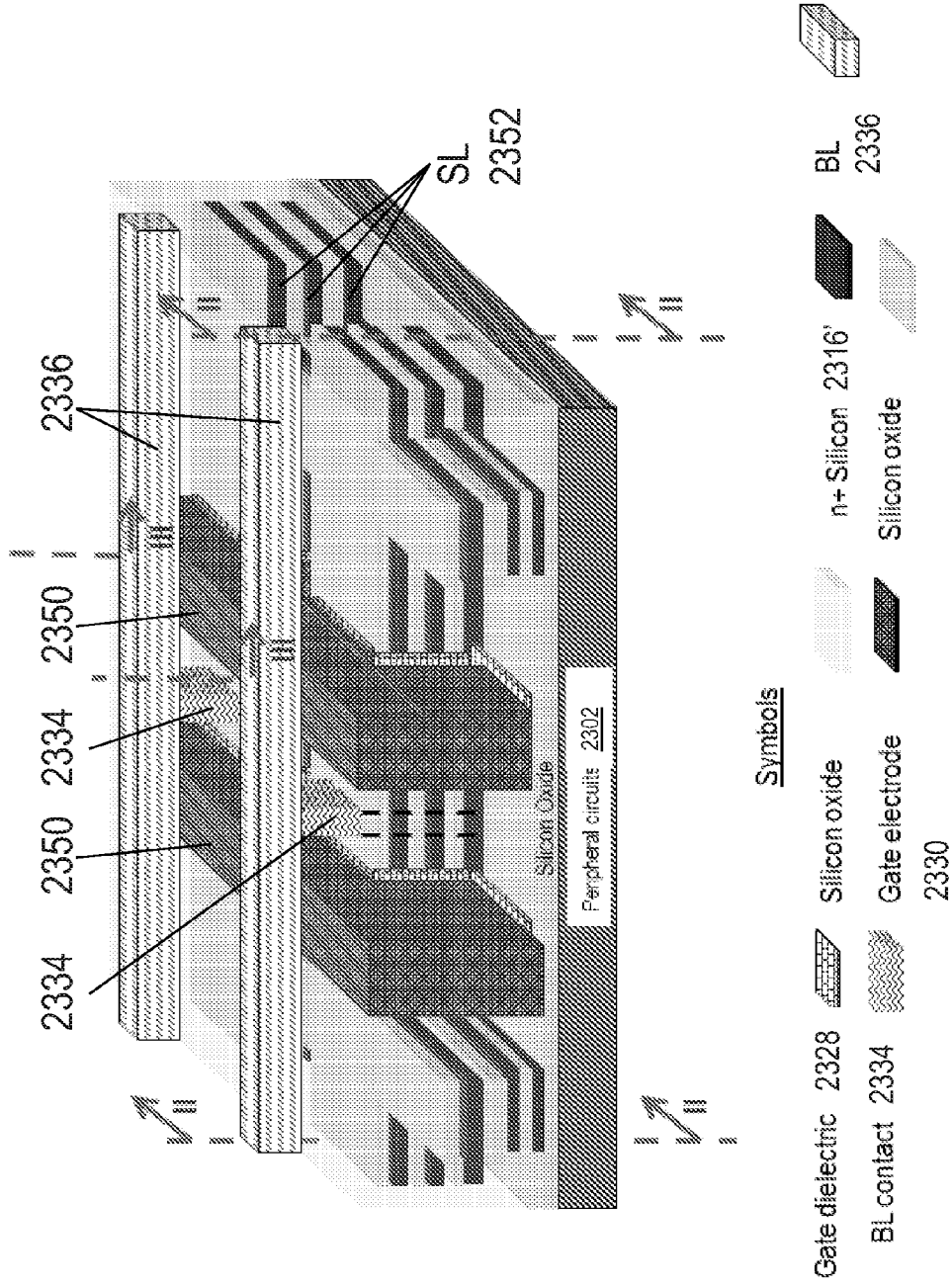
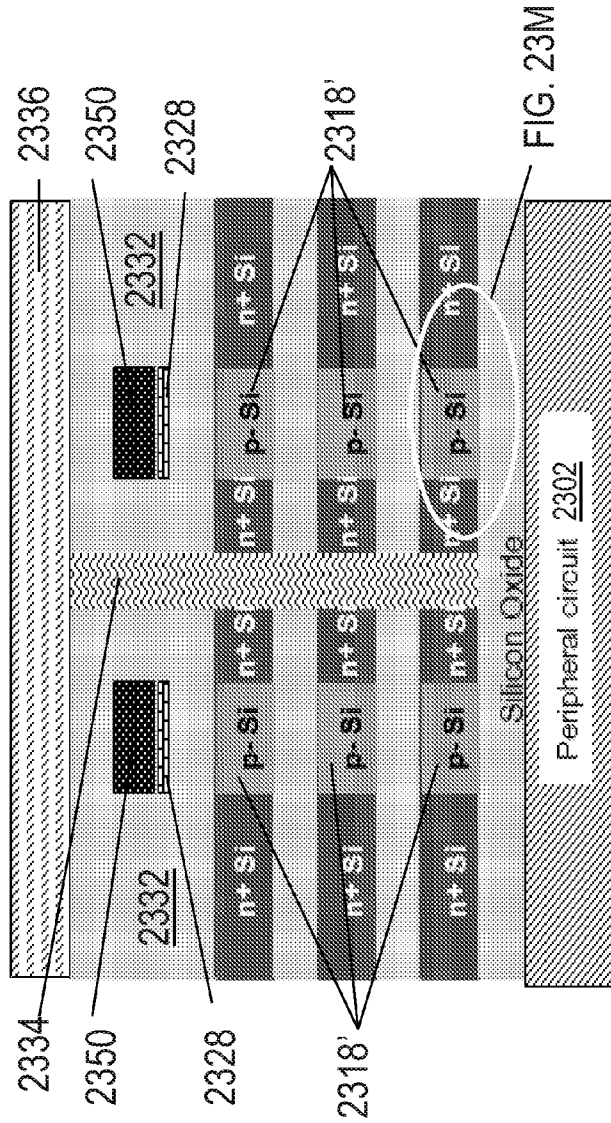


FIG. 233L



View along II plane

Symbols

- Gate dielectric 2328
- BL contact 2334
- Gate electrode 2330
- Silicon oxide
- n+ Silicon 2316'
- Silicon oxide
- BL 2336

FIG. 23L1

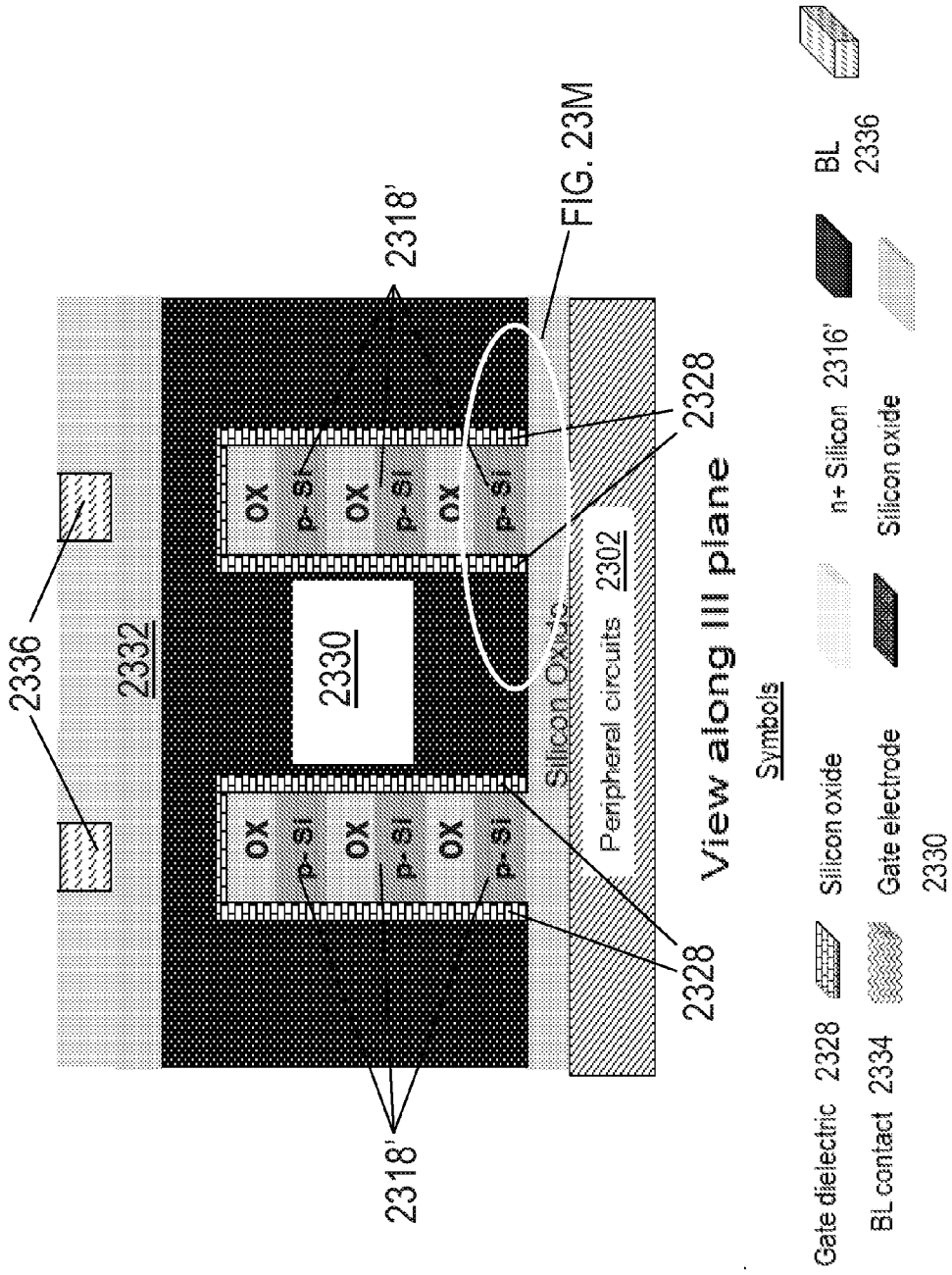


FIG. 23L2

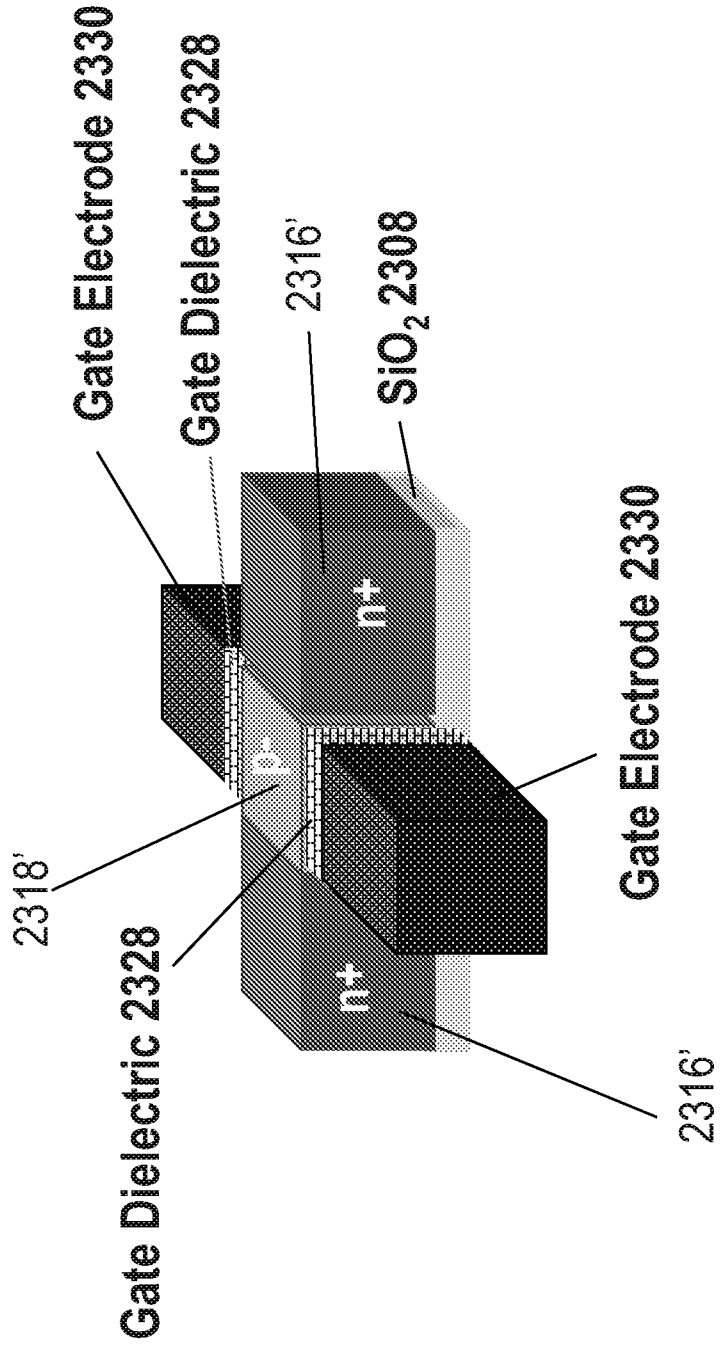


FIG. 23M

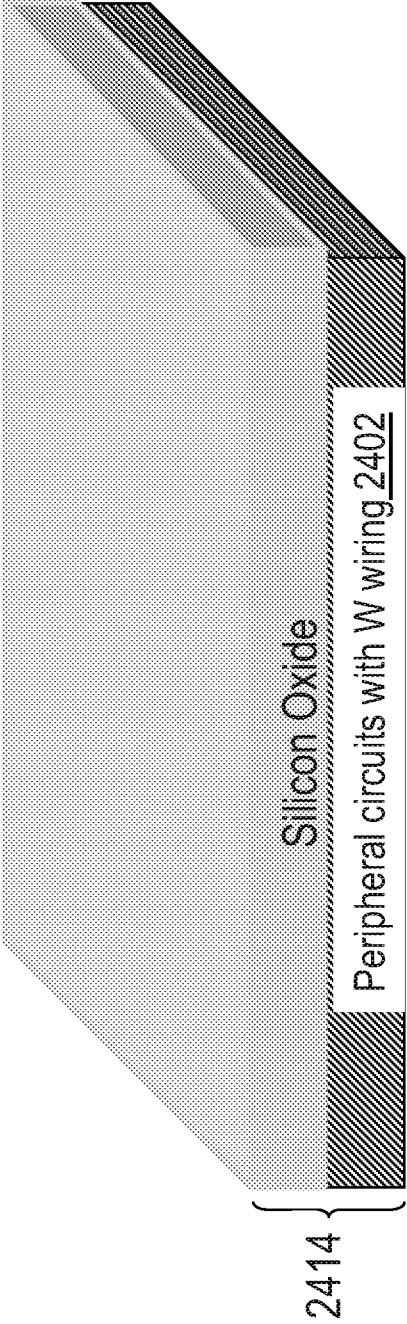


FIG. 24A

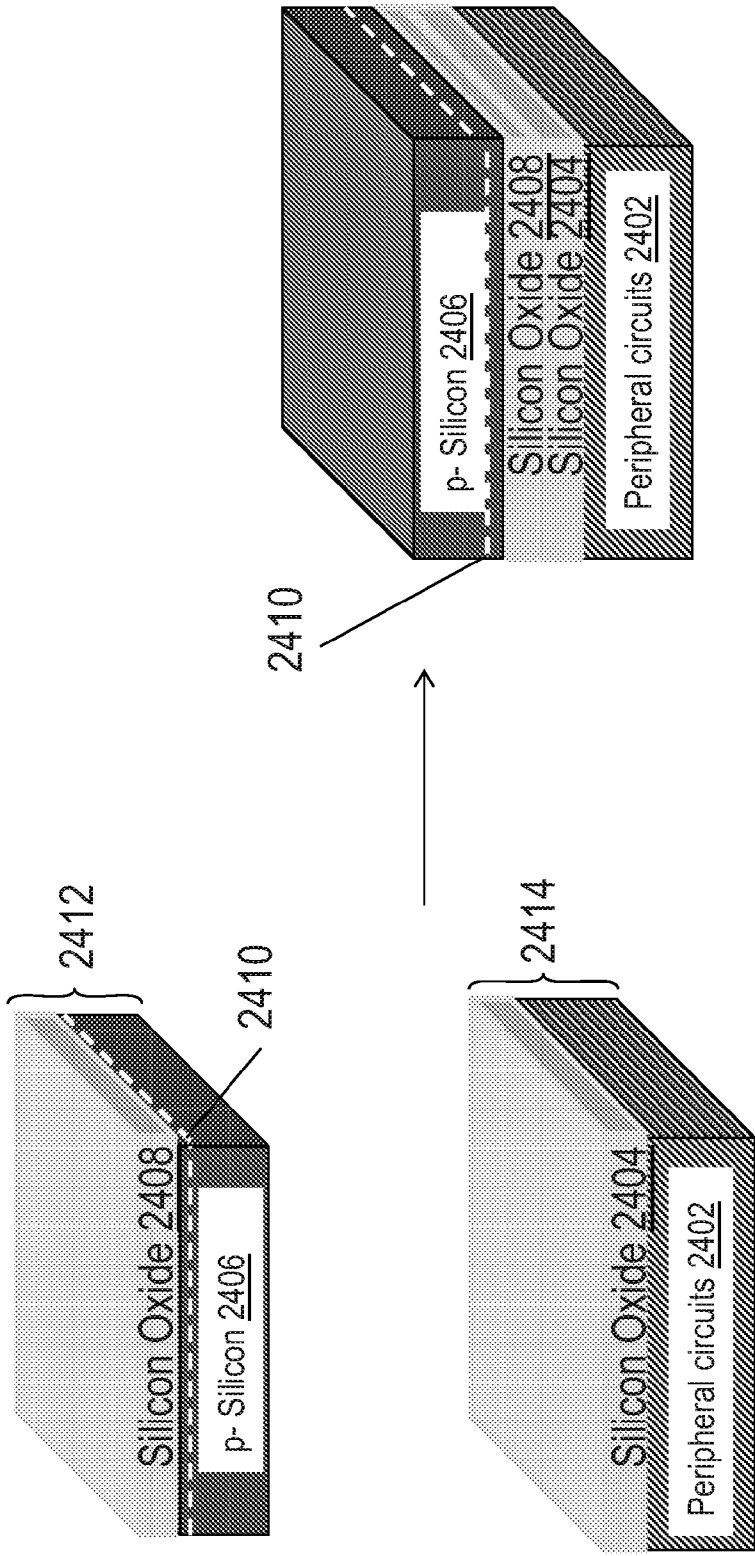


FIG. 24B



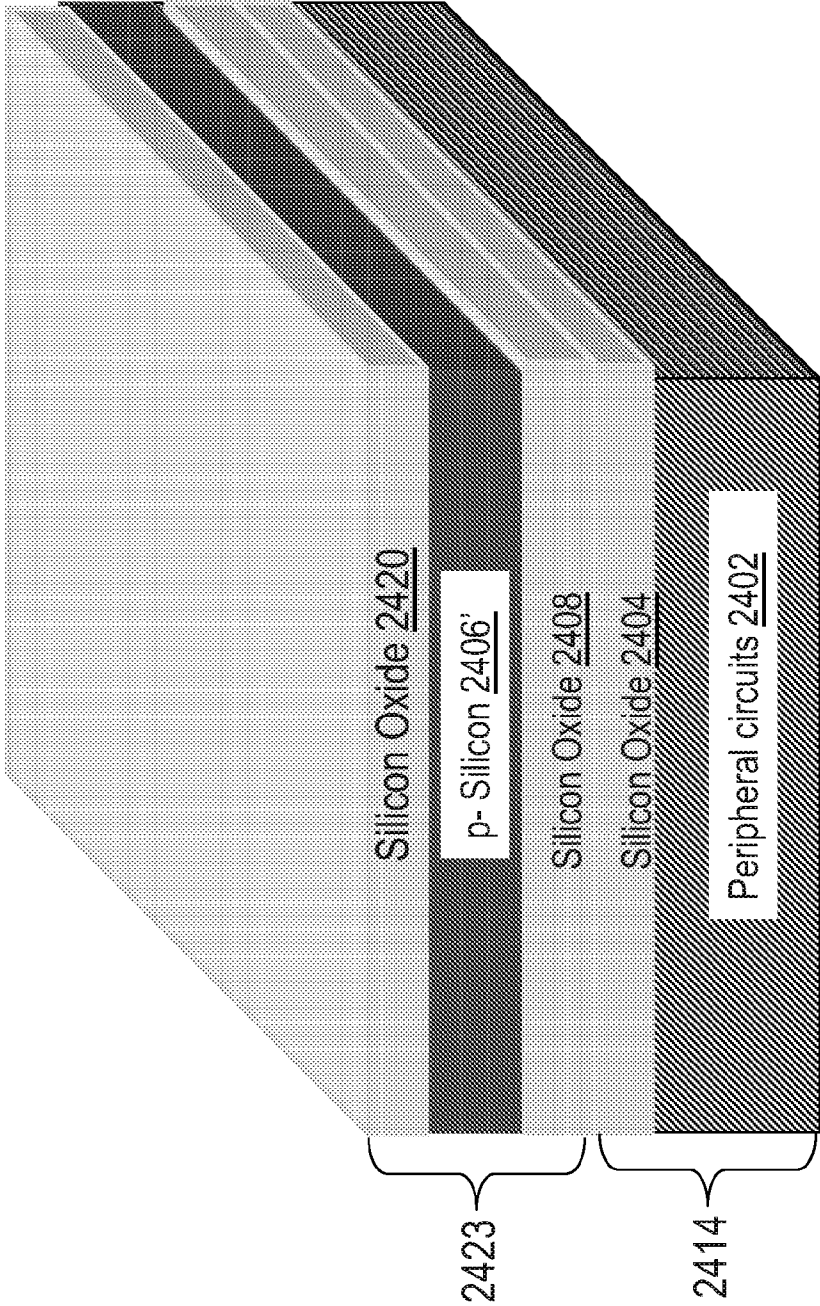


FIG. 24C

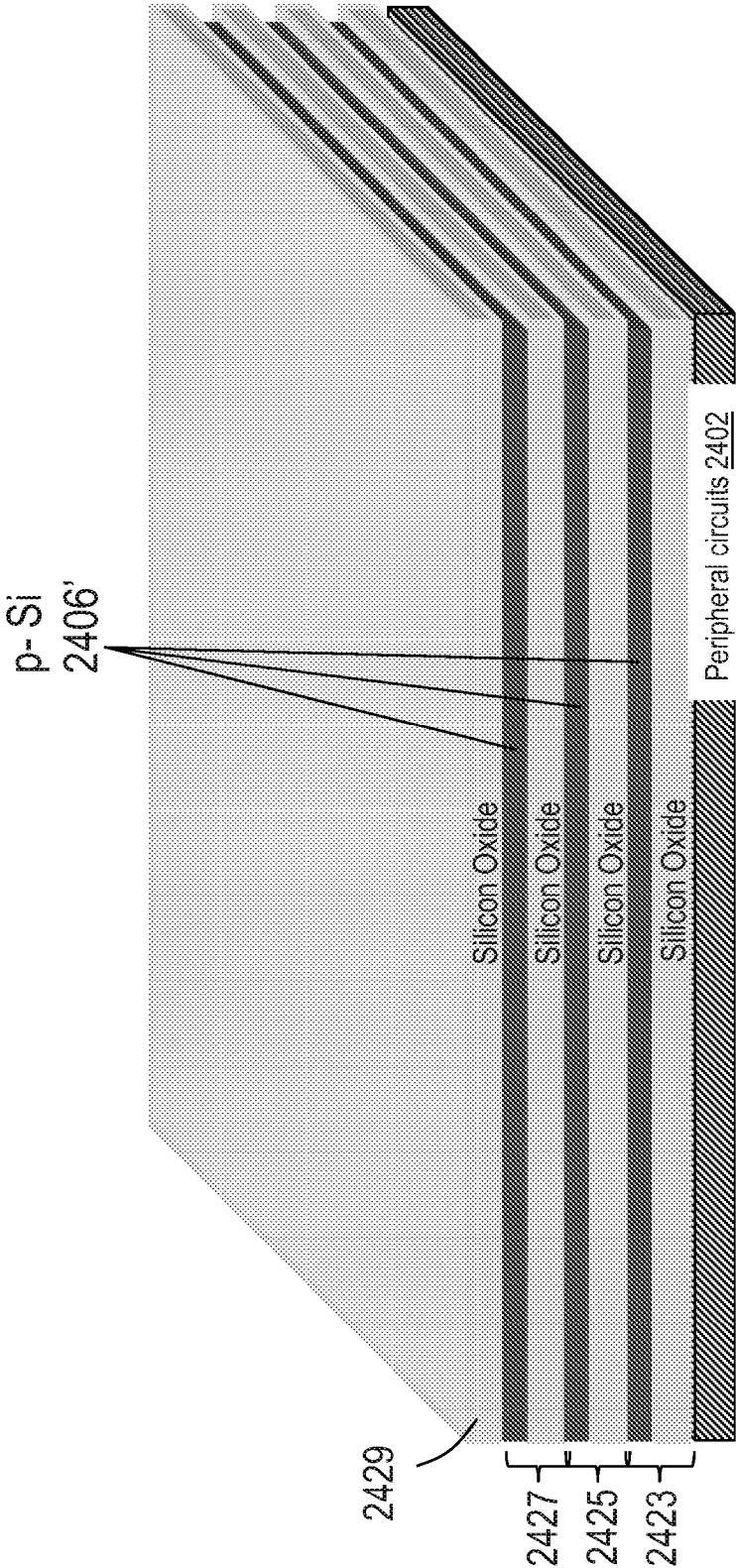


FIG. 24D

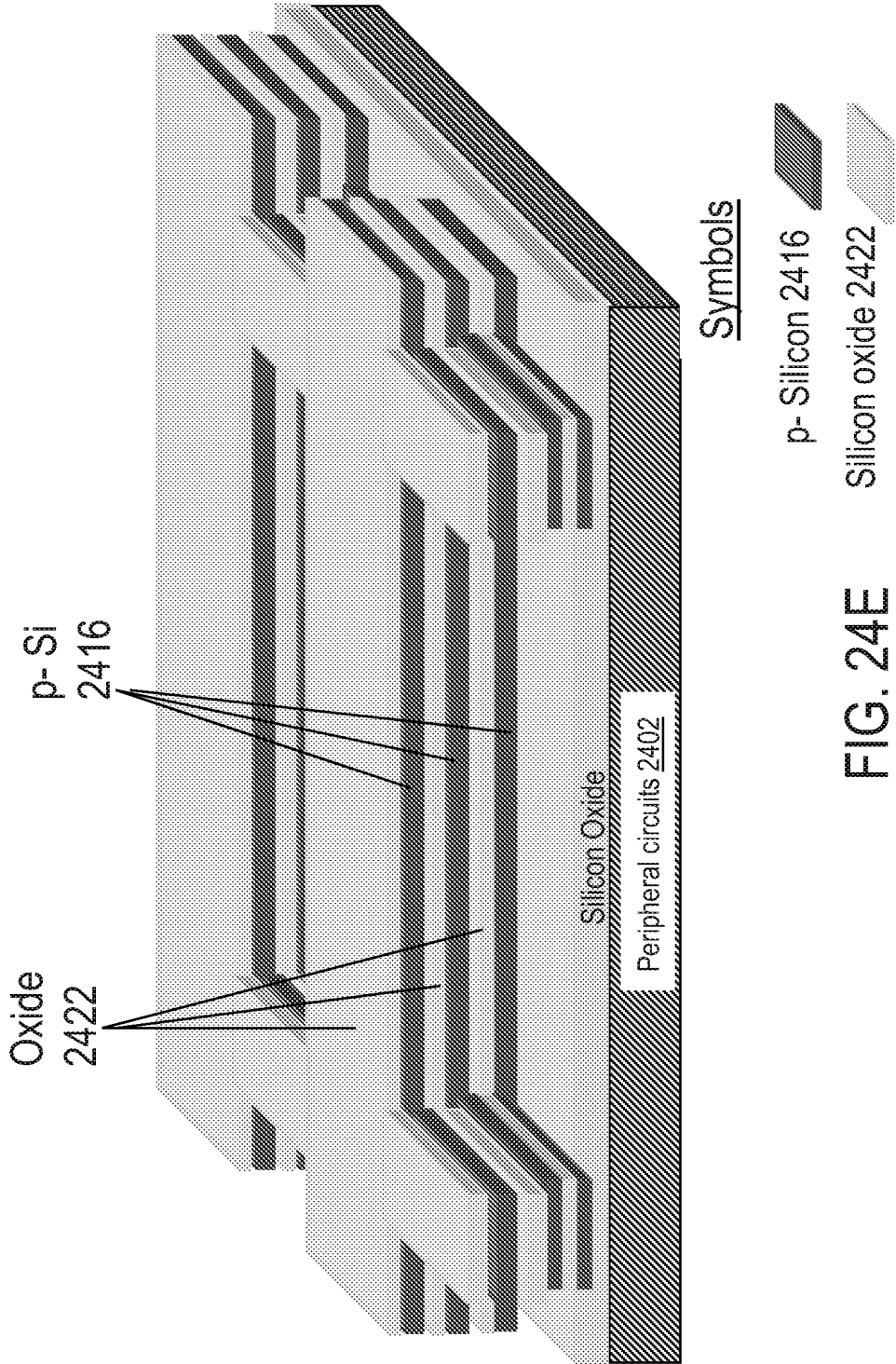


FIG. 24E

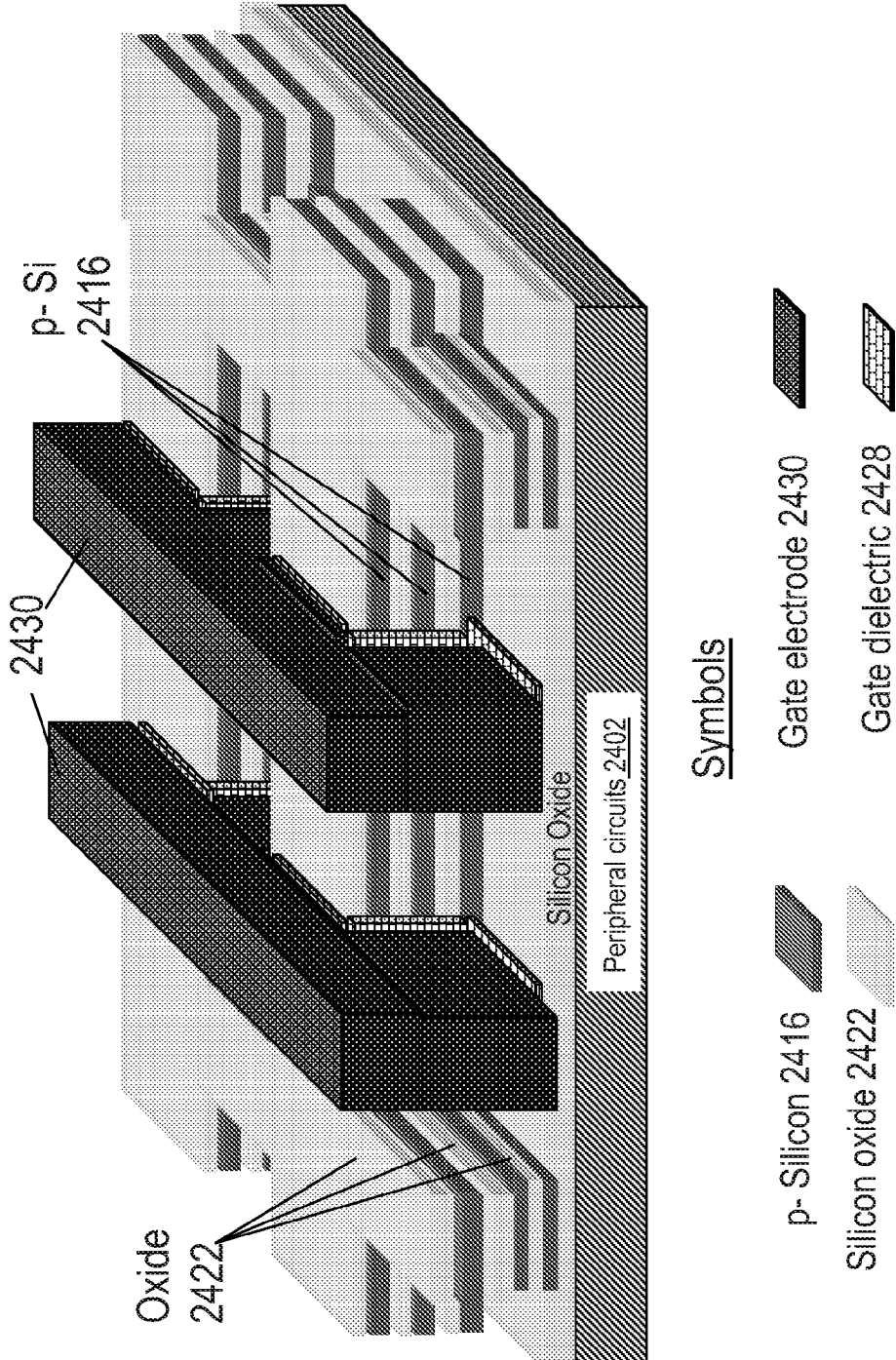


FIG. 24F

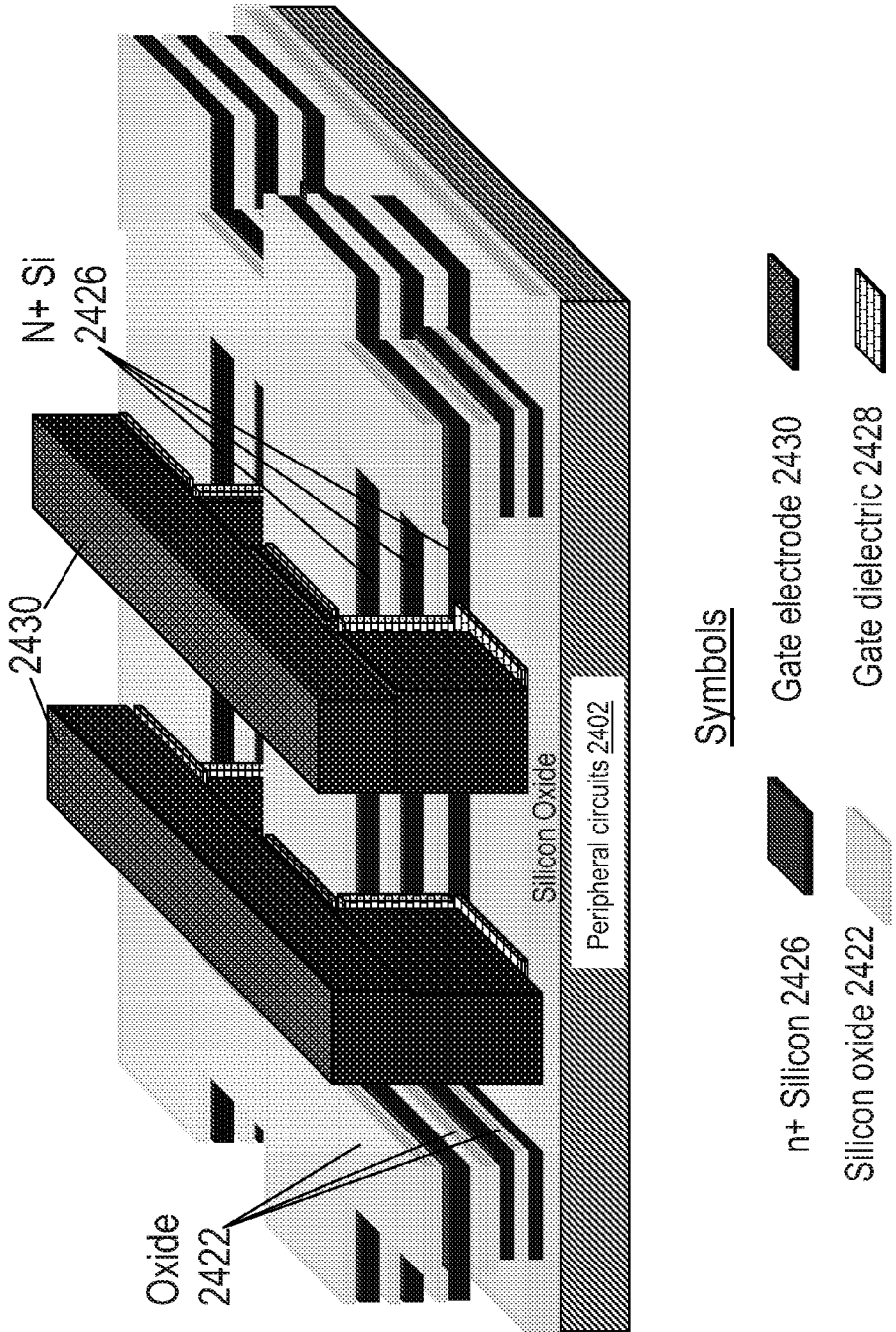
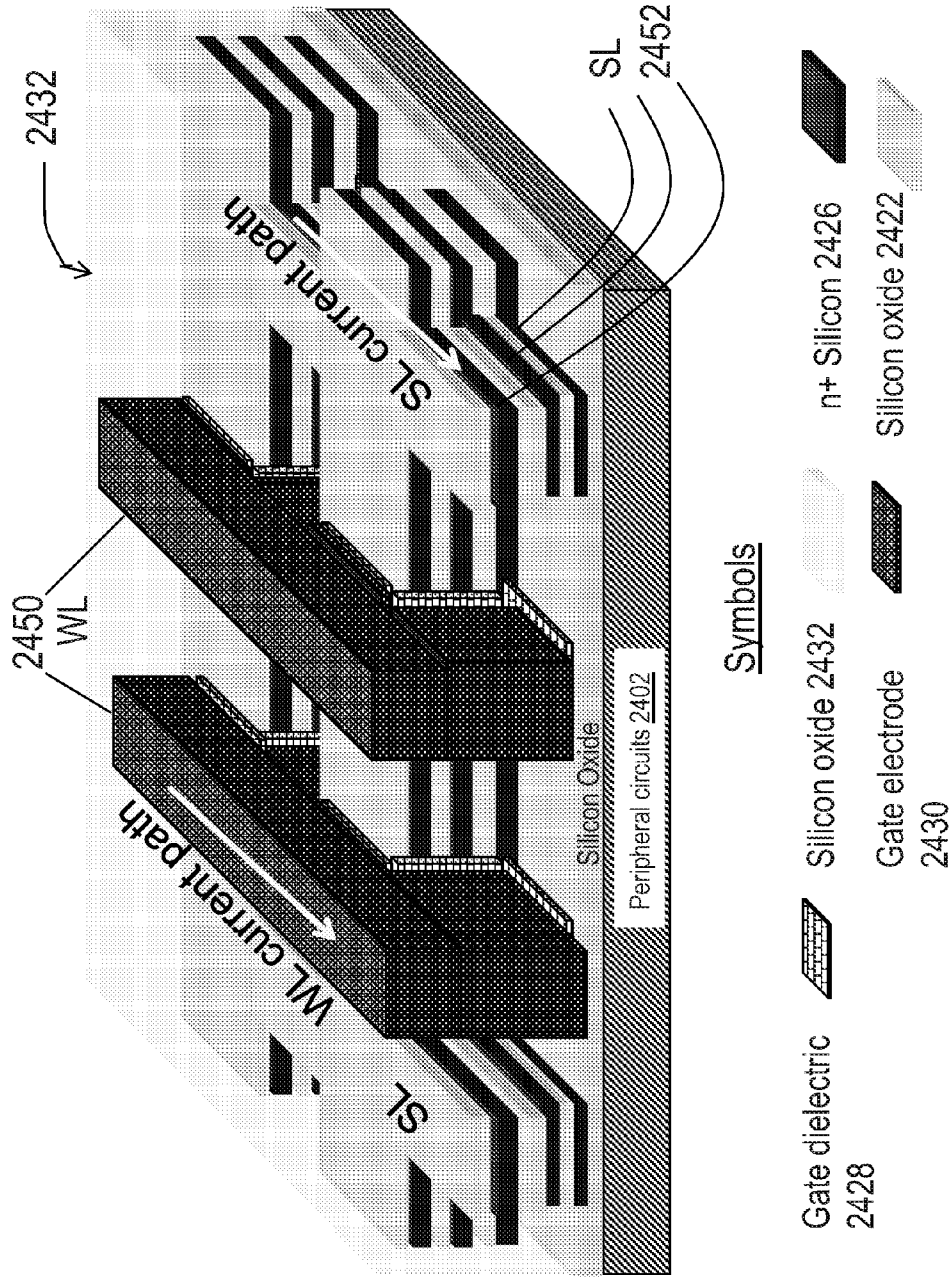


FIG. 24G



Symbols

- Gate dielectric 2428
- Gate electrode 2430
- Silicon oxide 2432
- n+ Silicon 2426
- Silicon oxide 2422

FIG. 24H

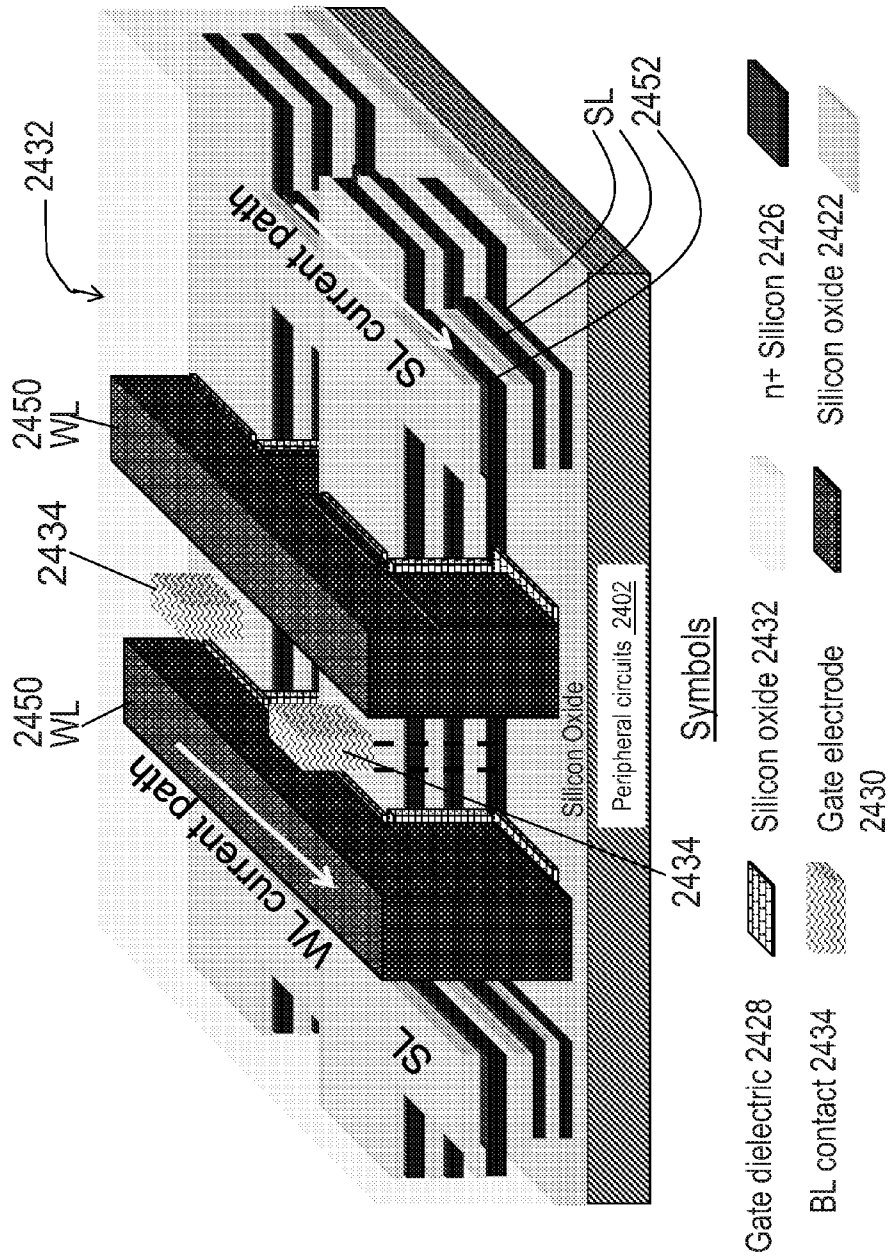


FIG. 24I

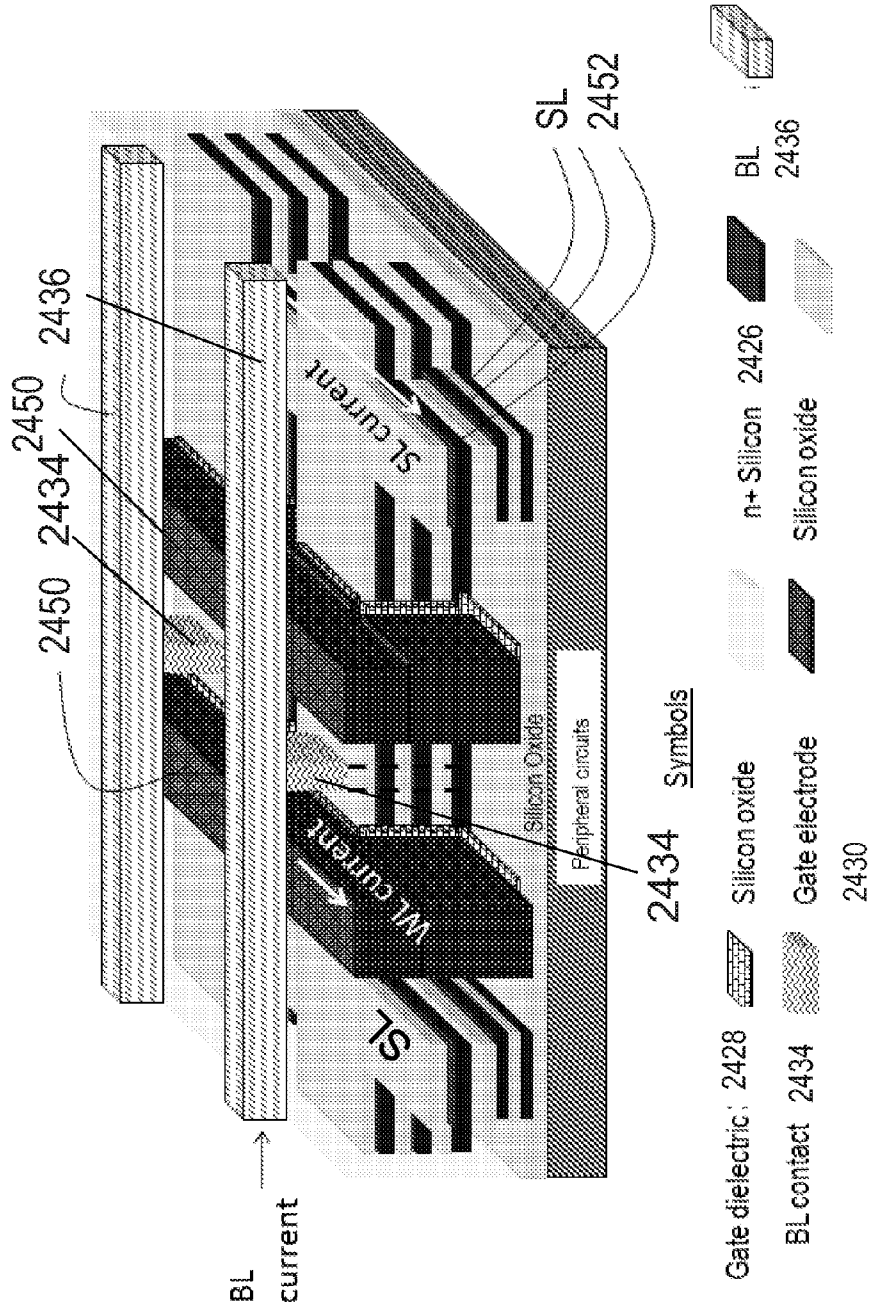


FIG. 24J



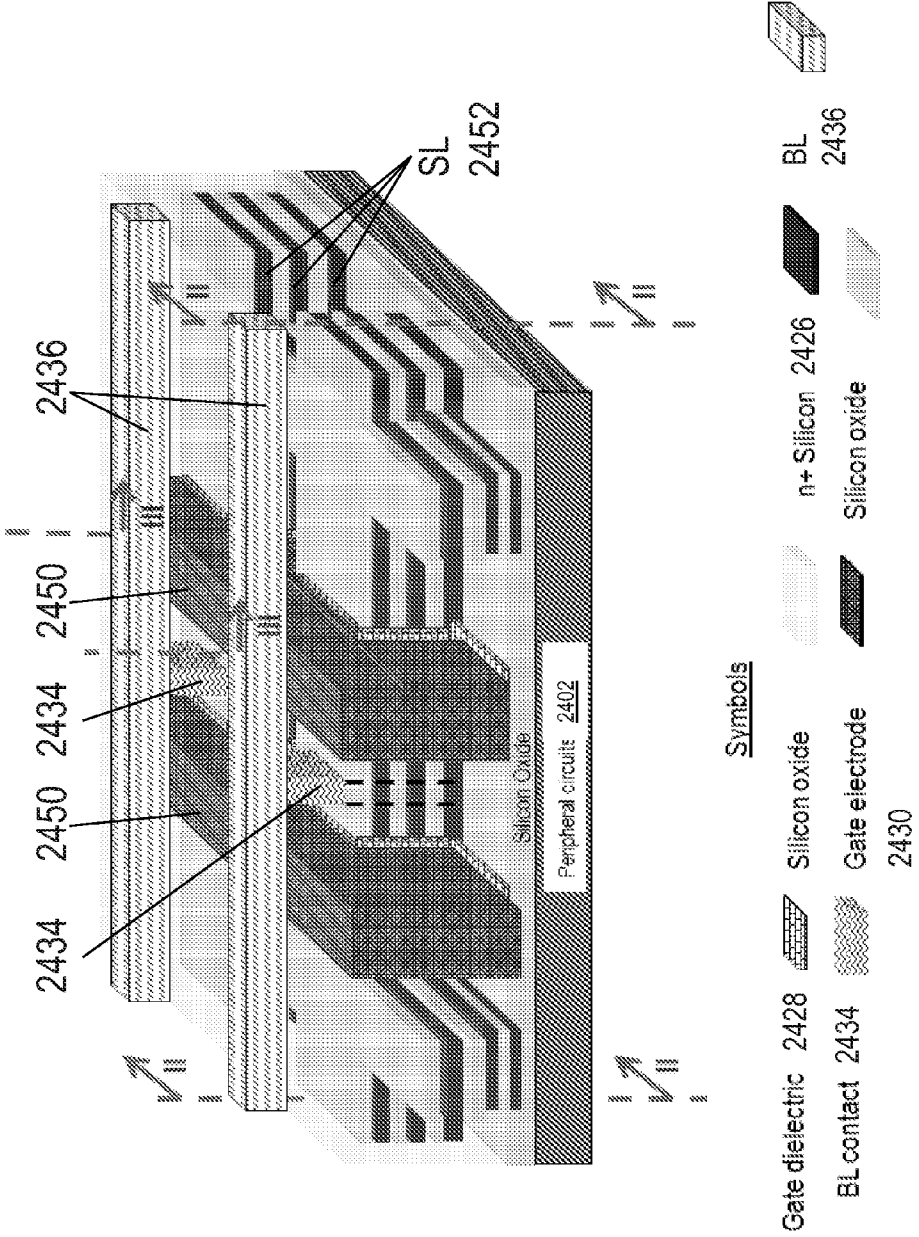
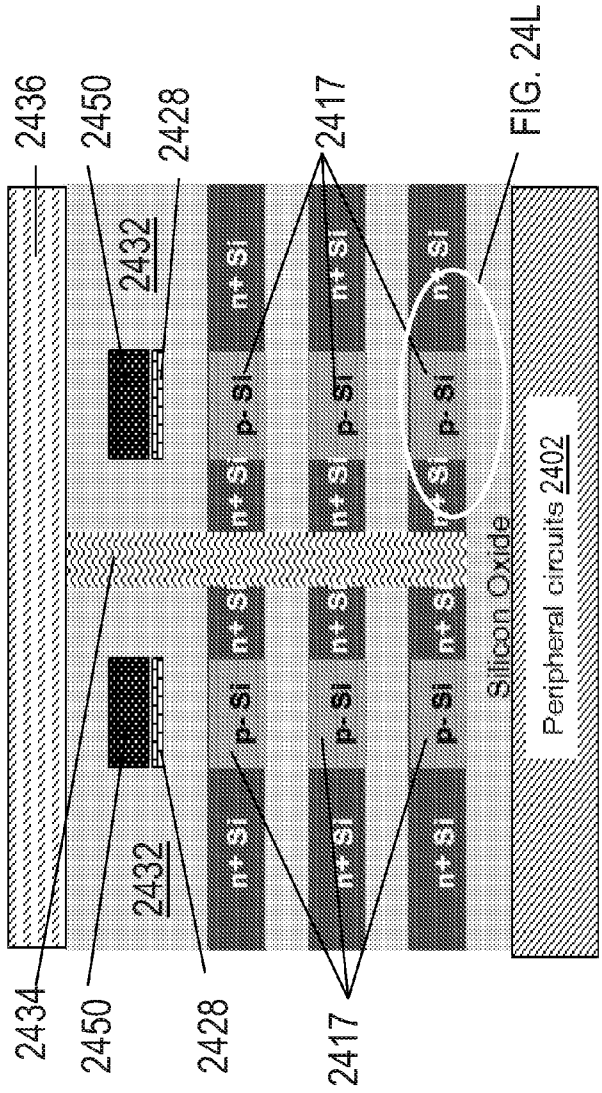


FIG. 24K



View along II plane

Symbols

- Gate dielectric 2428
- BL contact 2434
- Gate electrode 2430
- Siicon oxide
- n+ Silicon 2426
- Siicon oxide
- BL 2436

FIG. 24K1

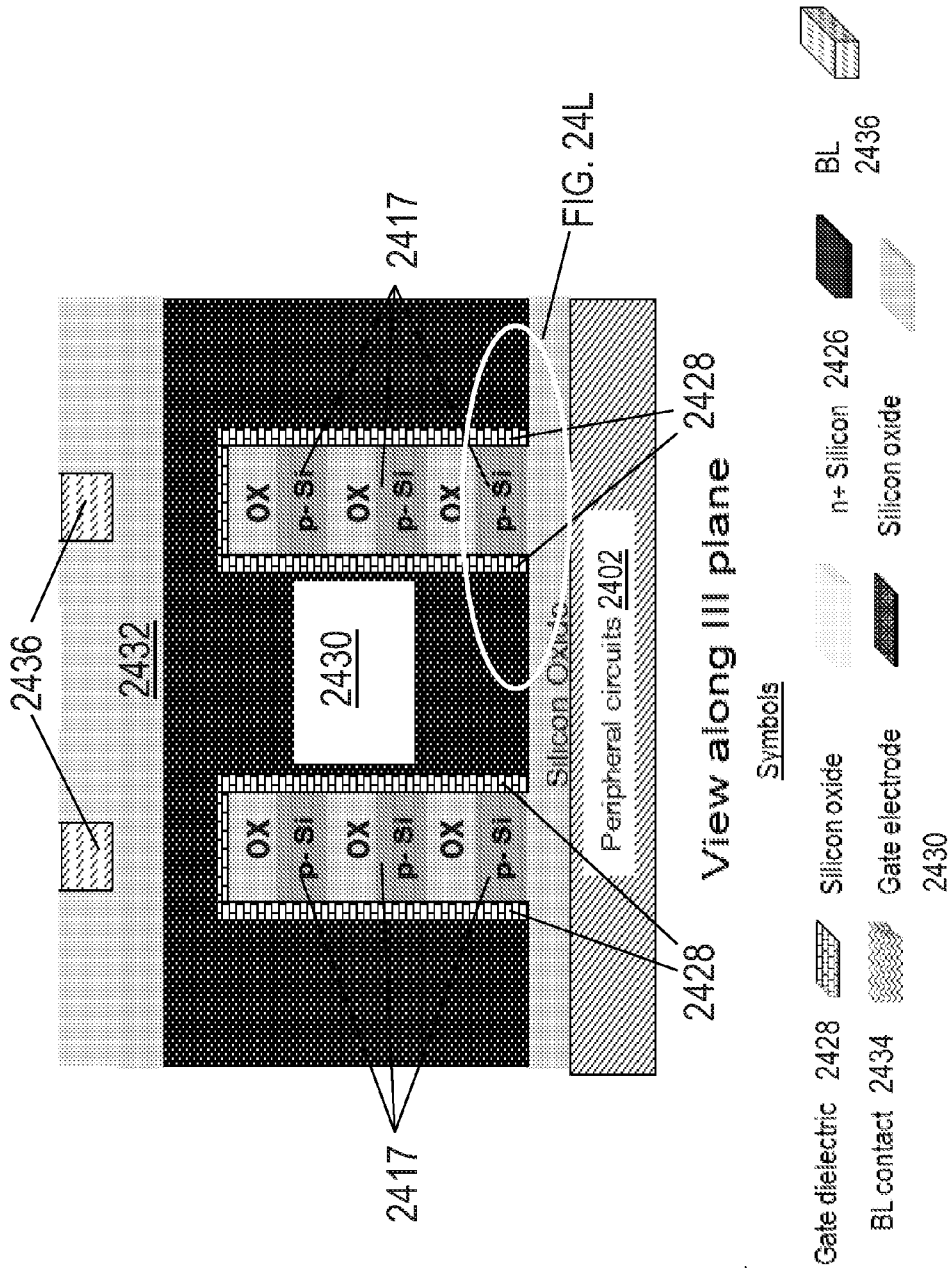


FIG. 24K2

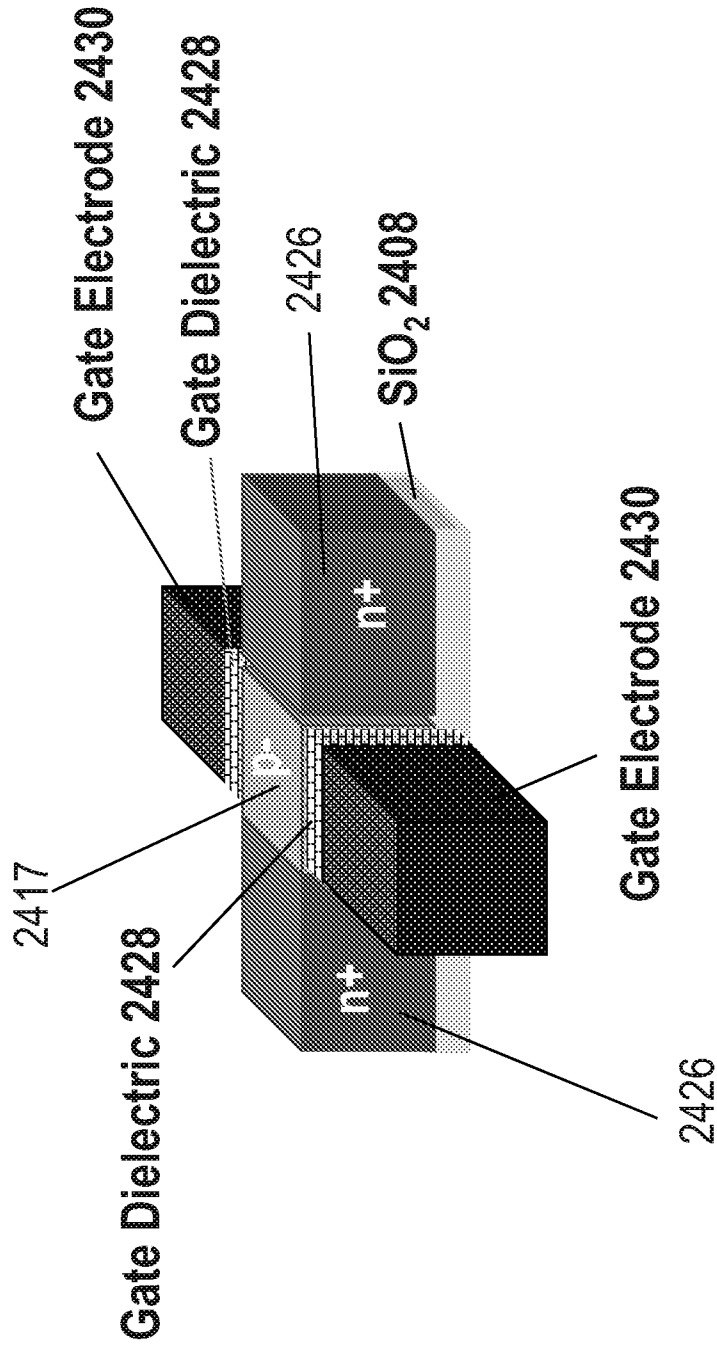


FIG. 24L

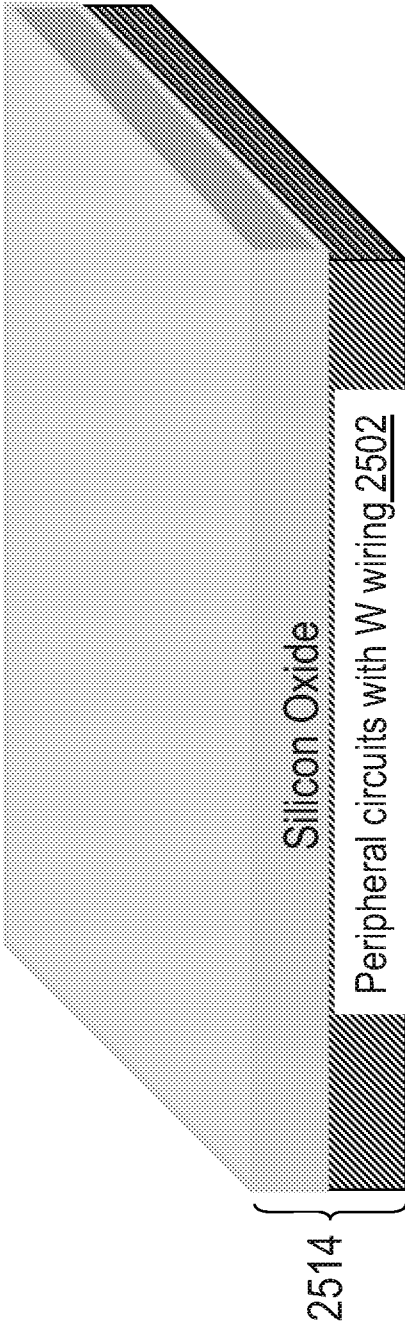


FIG. 25A

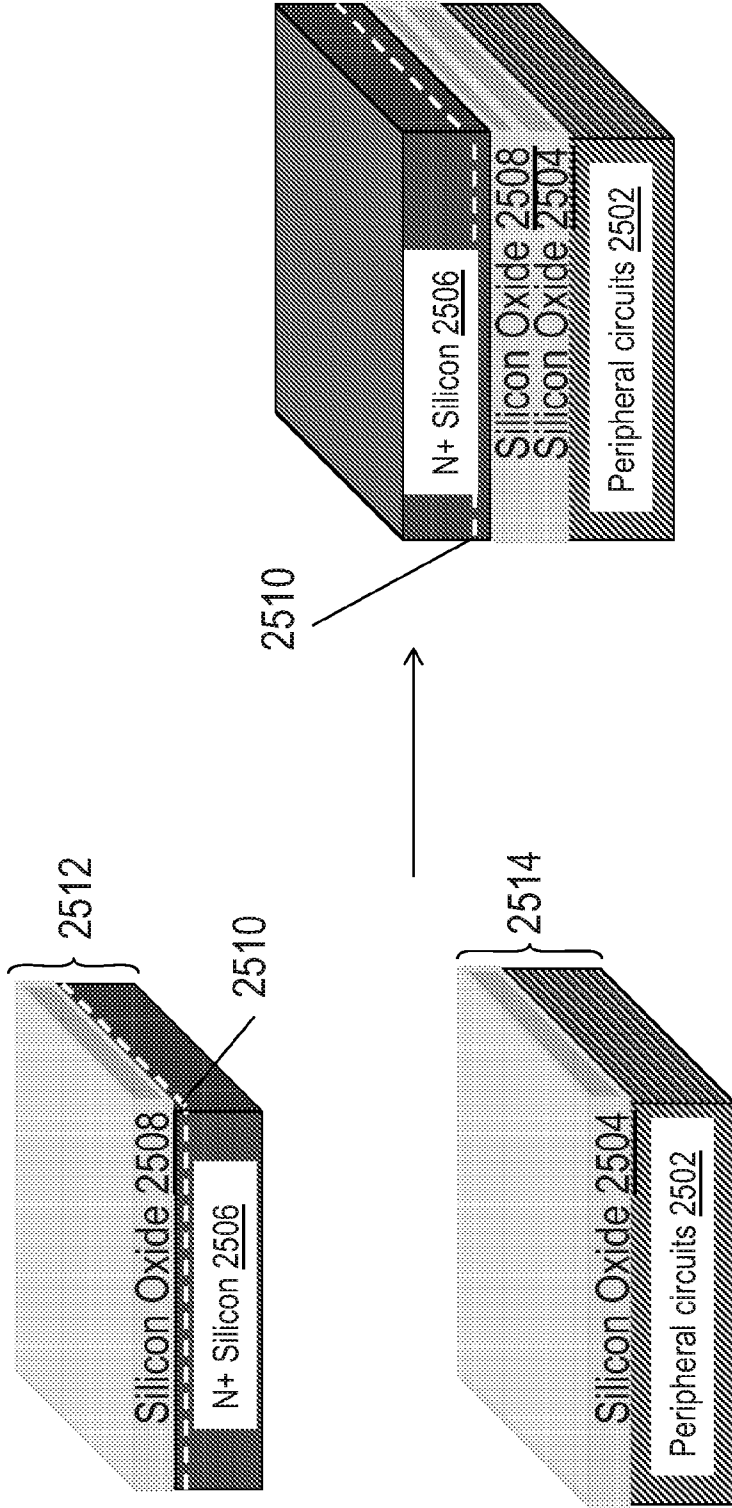


FIG. 25B

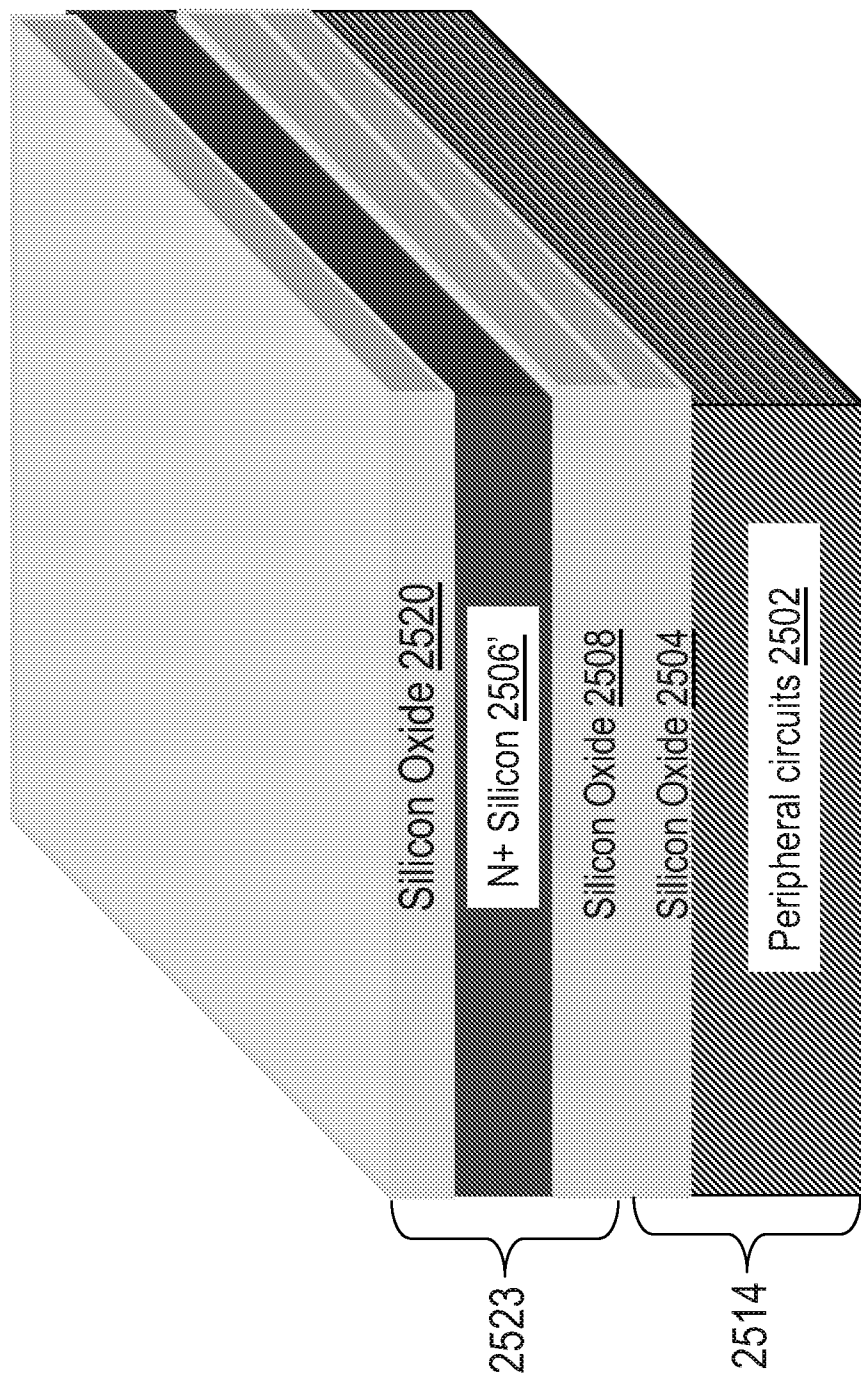


FIG. 25C

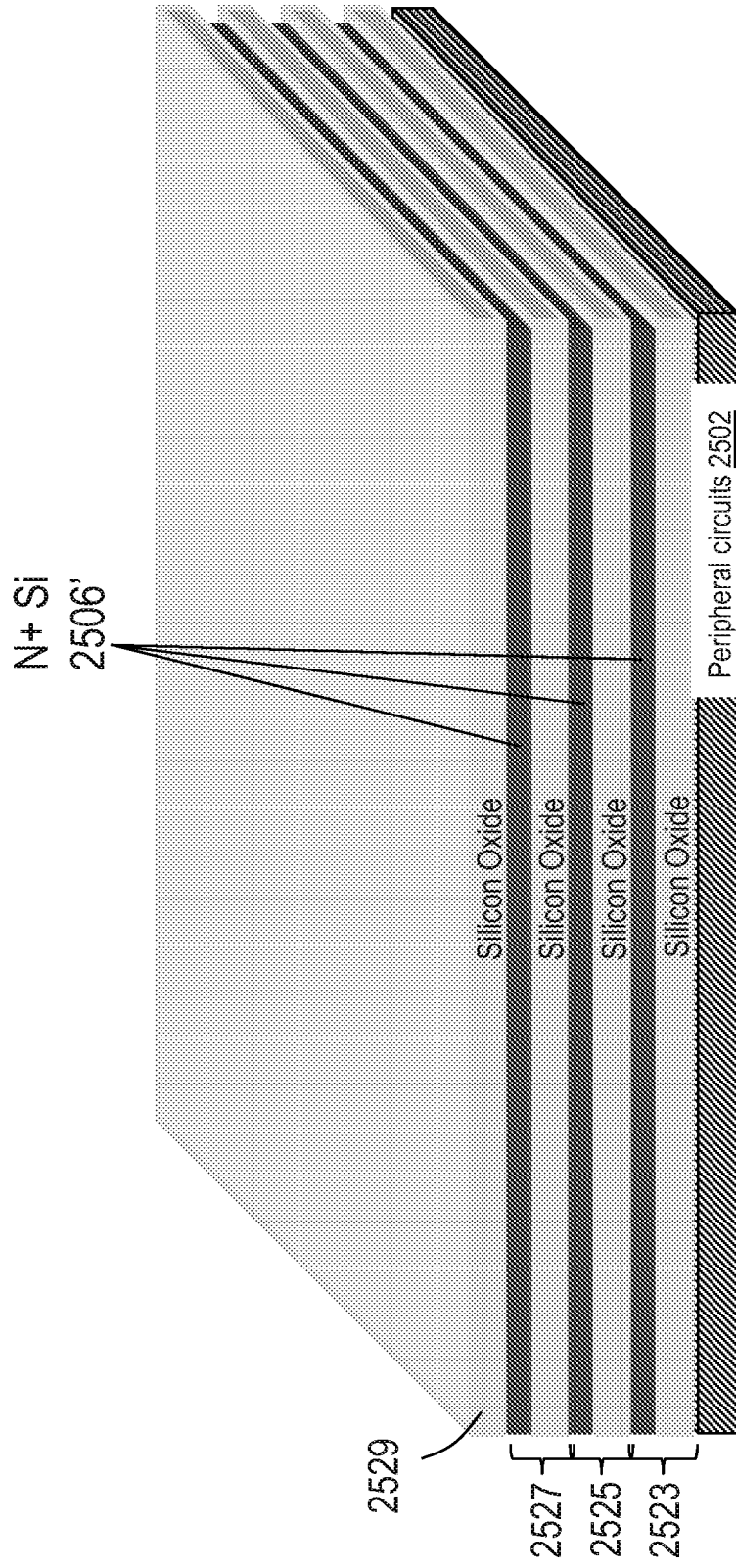


FIG. 25D



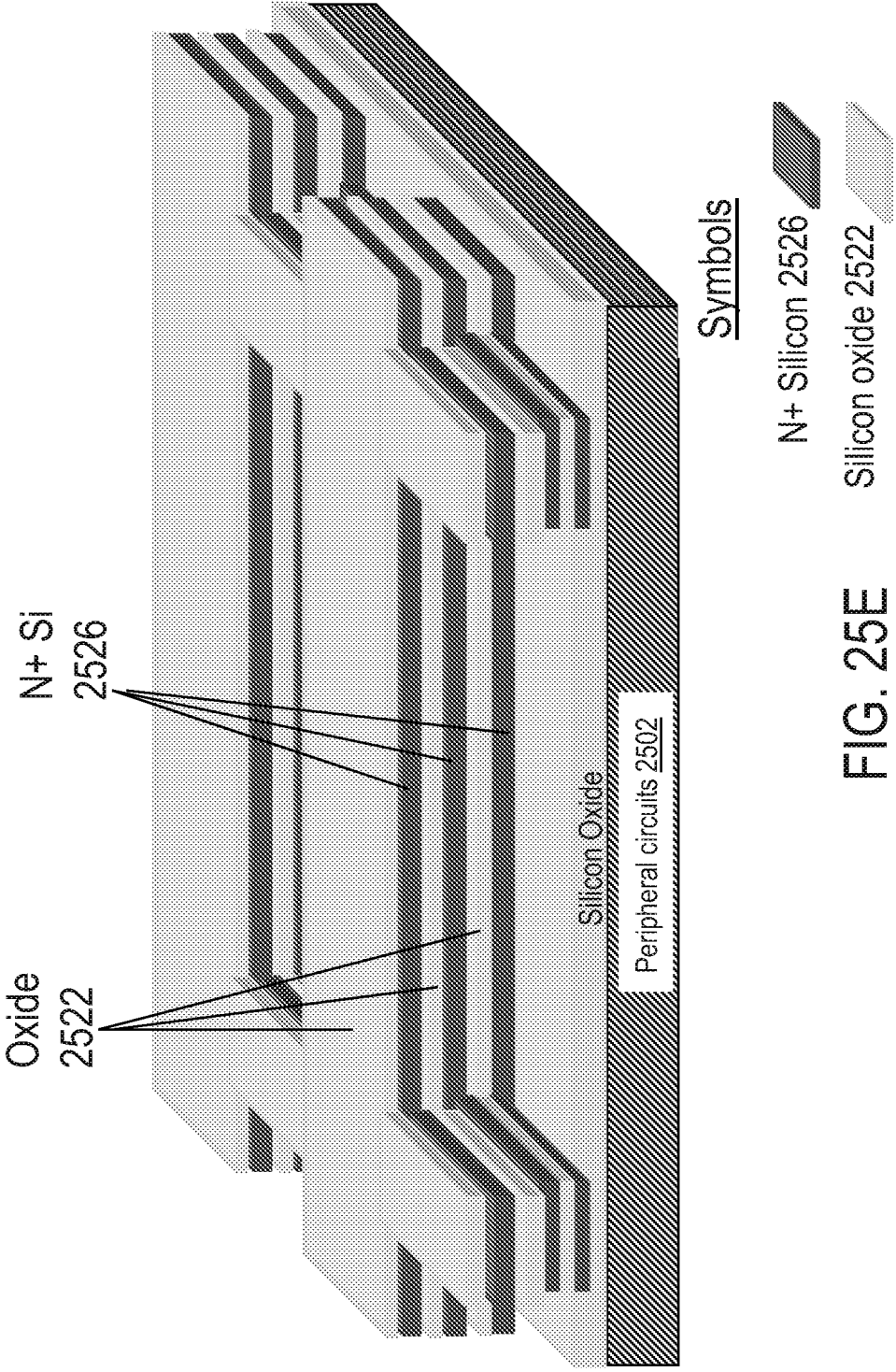


FIG. 25E

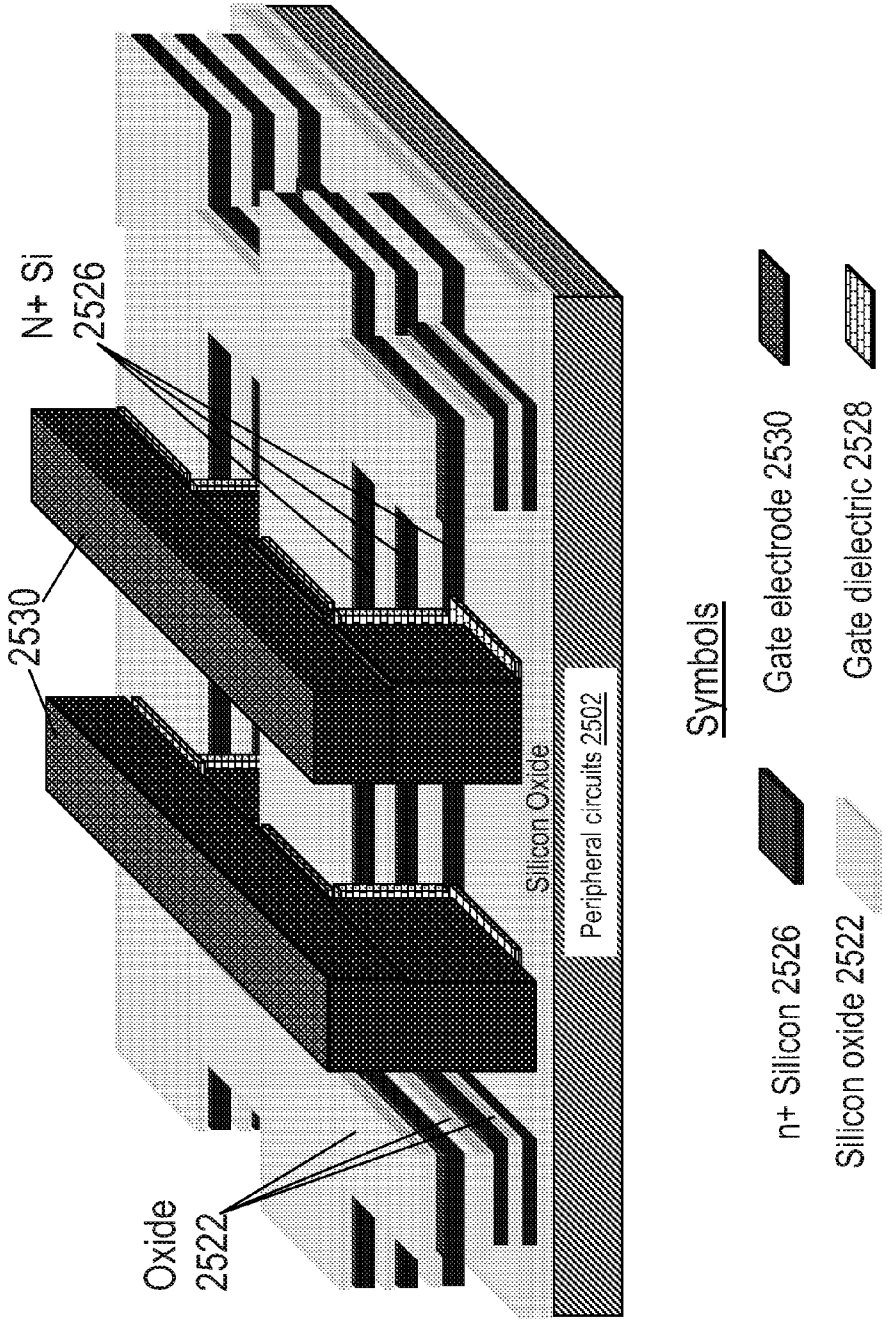
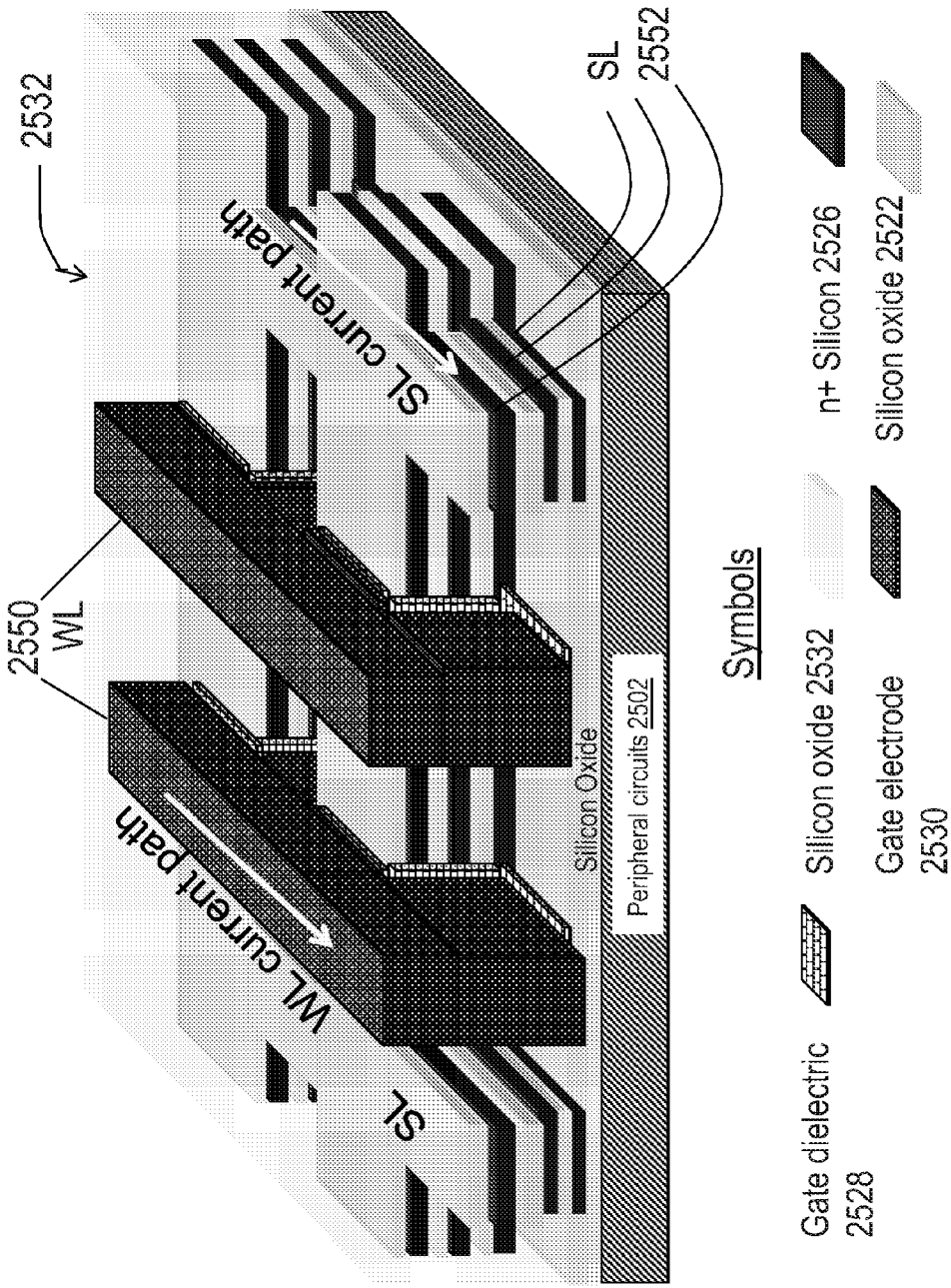


FIG. 25F



Symbols

- Gate dielectric 2528
- Silicon oxide 2532
- Gate electrode 2530
- n+ Silicon 2526
- Silicon oxide 2522

FIG. 25G

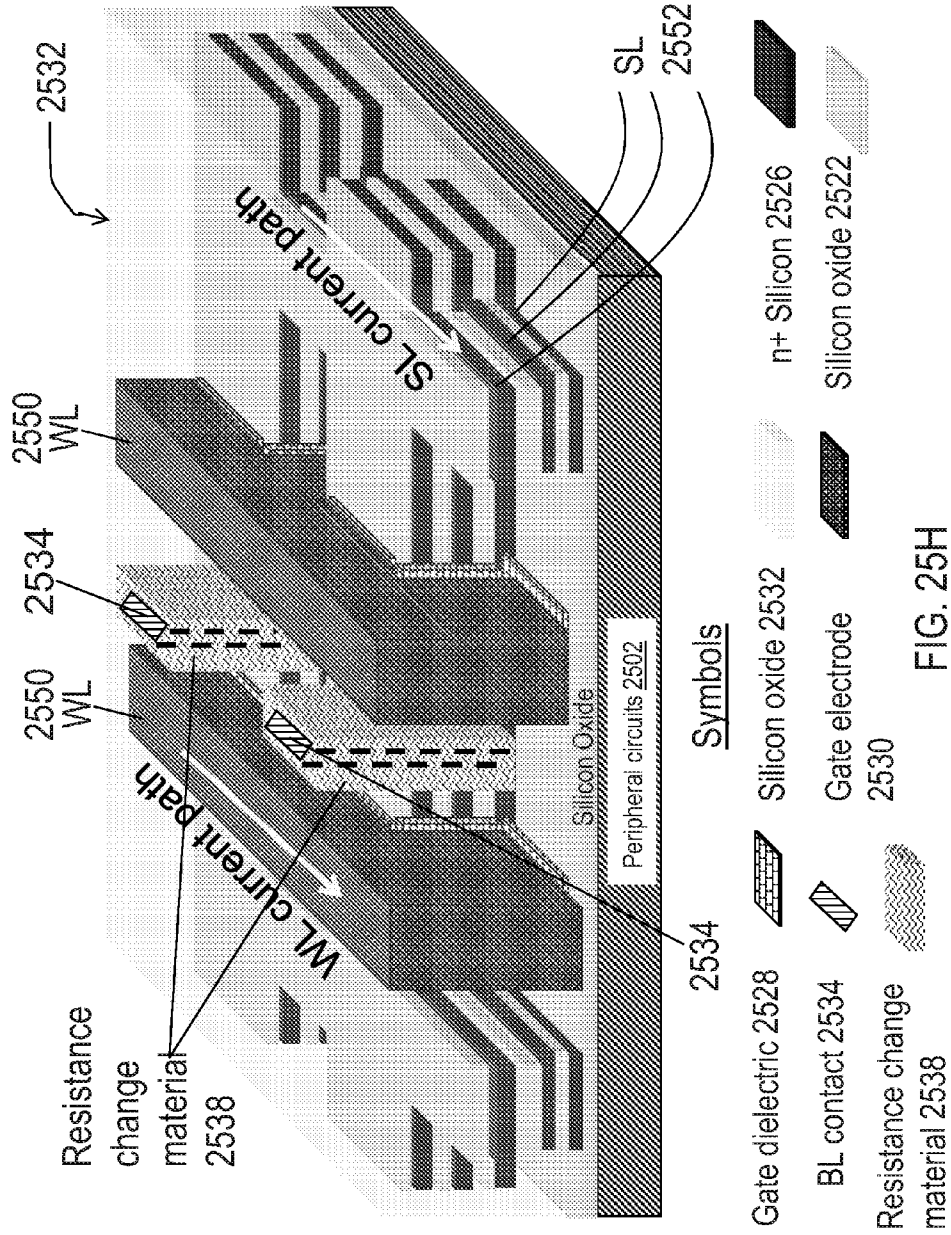
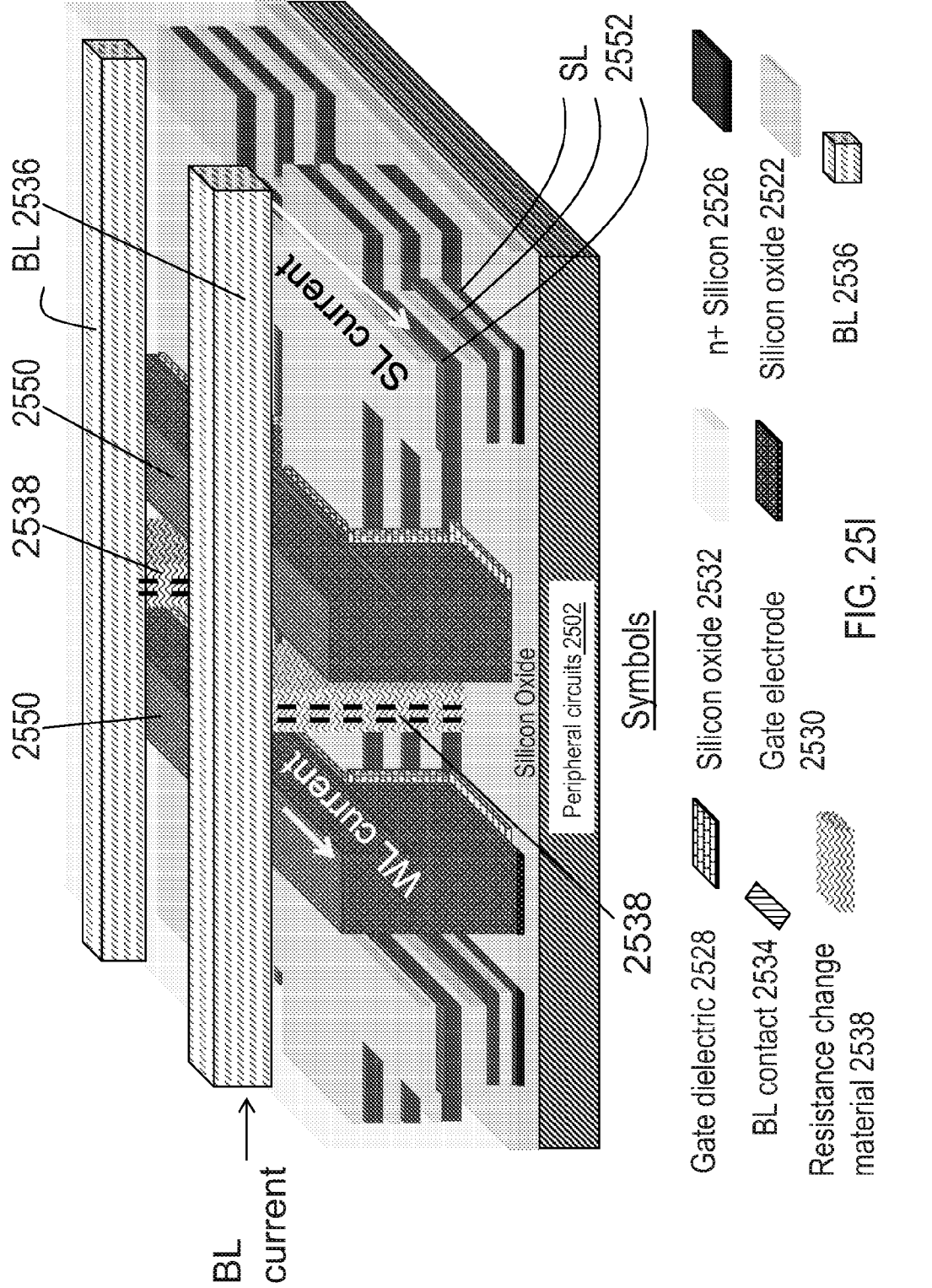


FIG. 25H



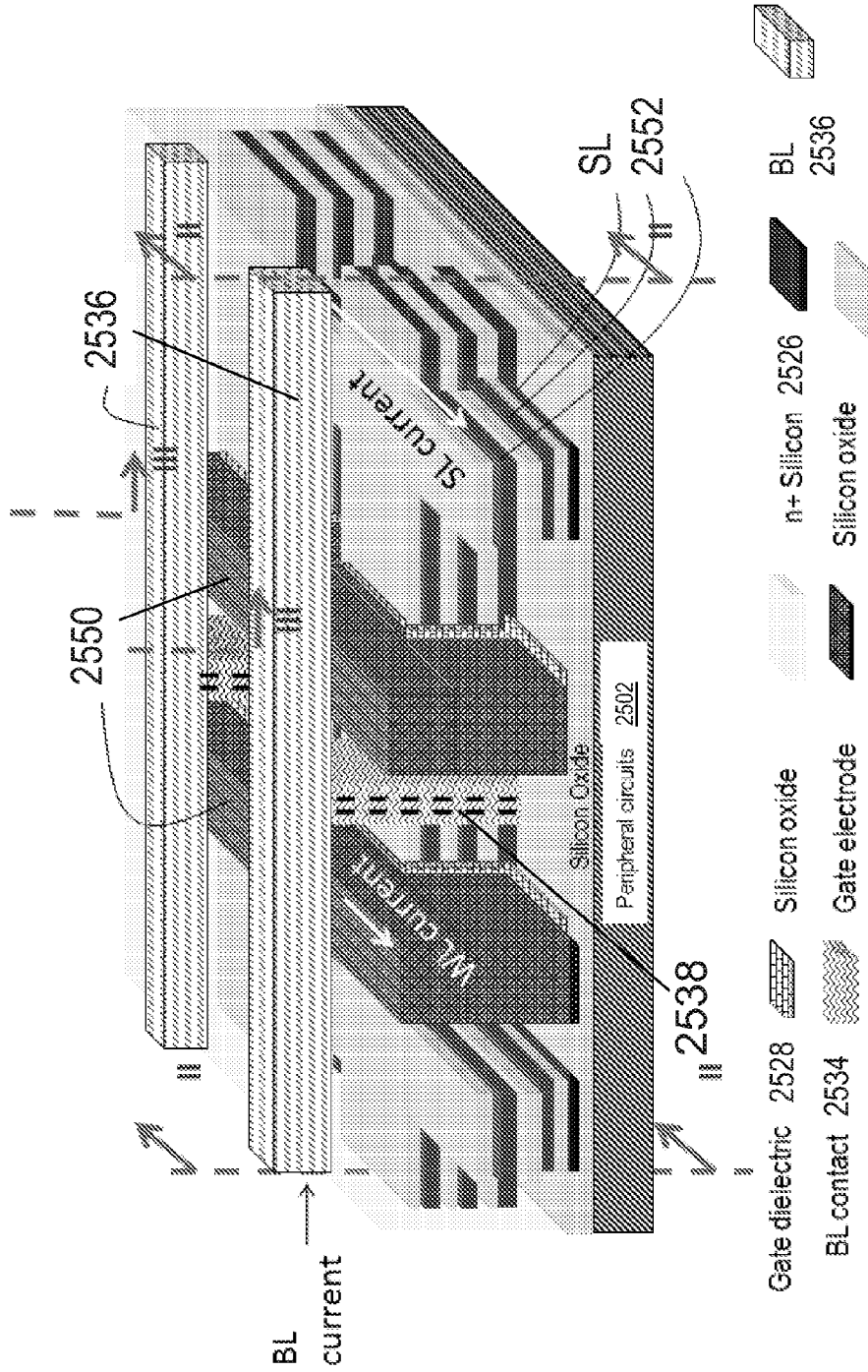
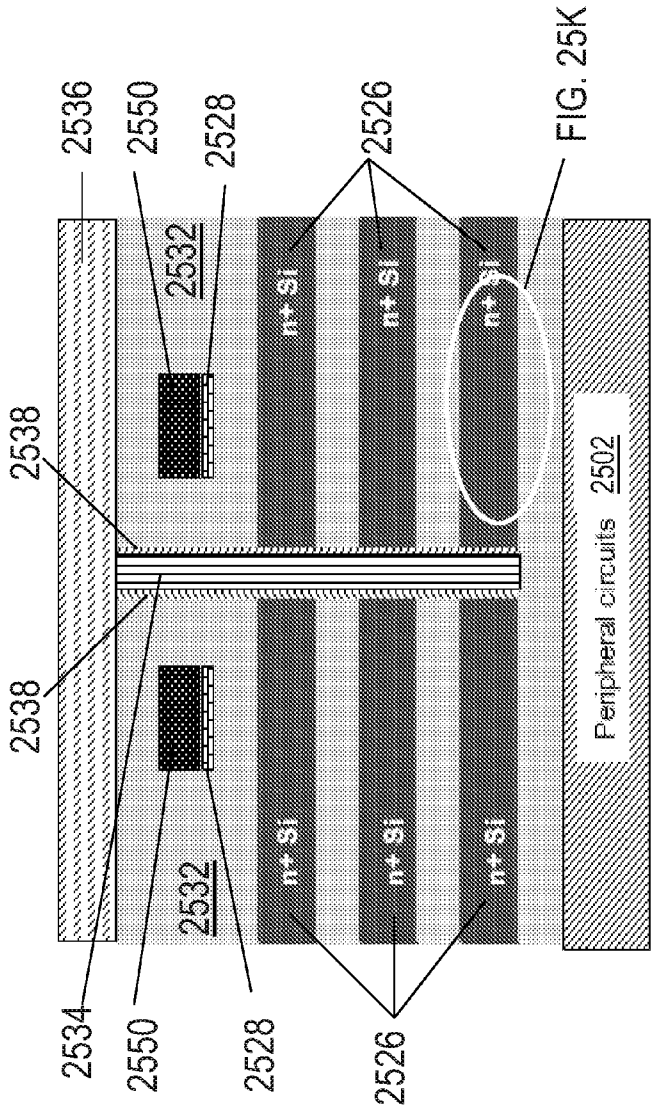


FIG. 25J



View along II plane

Symbols

Gate dielectric 2528	Silicon oxide	n+ Silicon 2526	BL 2536
BL contact 2534	Gate electrode 2530	Silicon oxide	
Resistance change material 2538			

FIG. 25J1

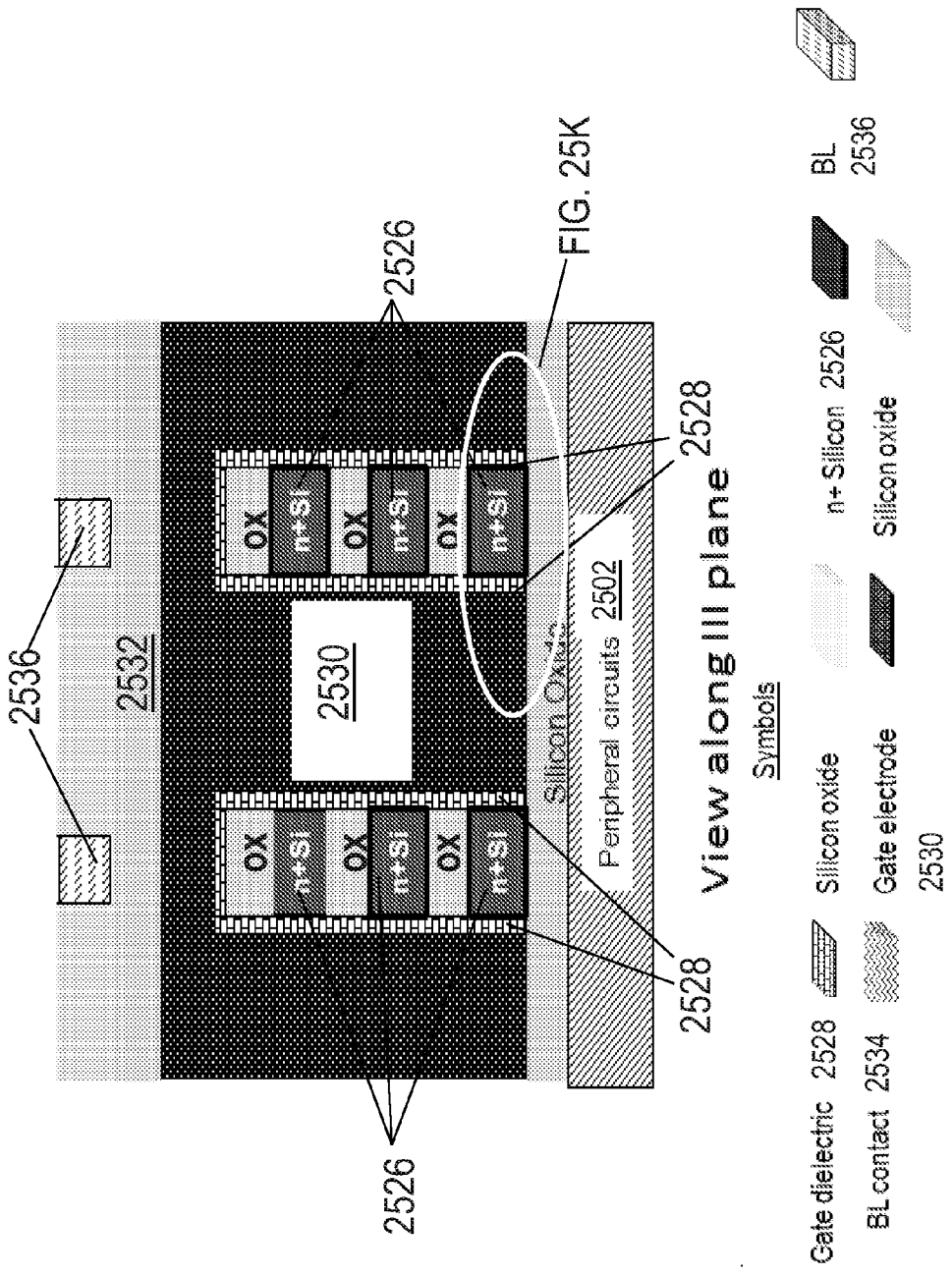


FIG. 25J2



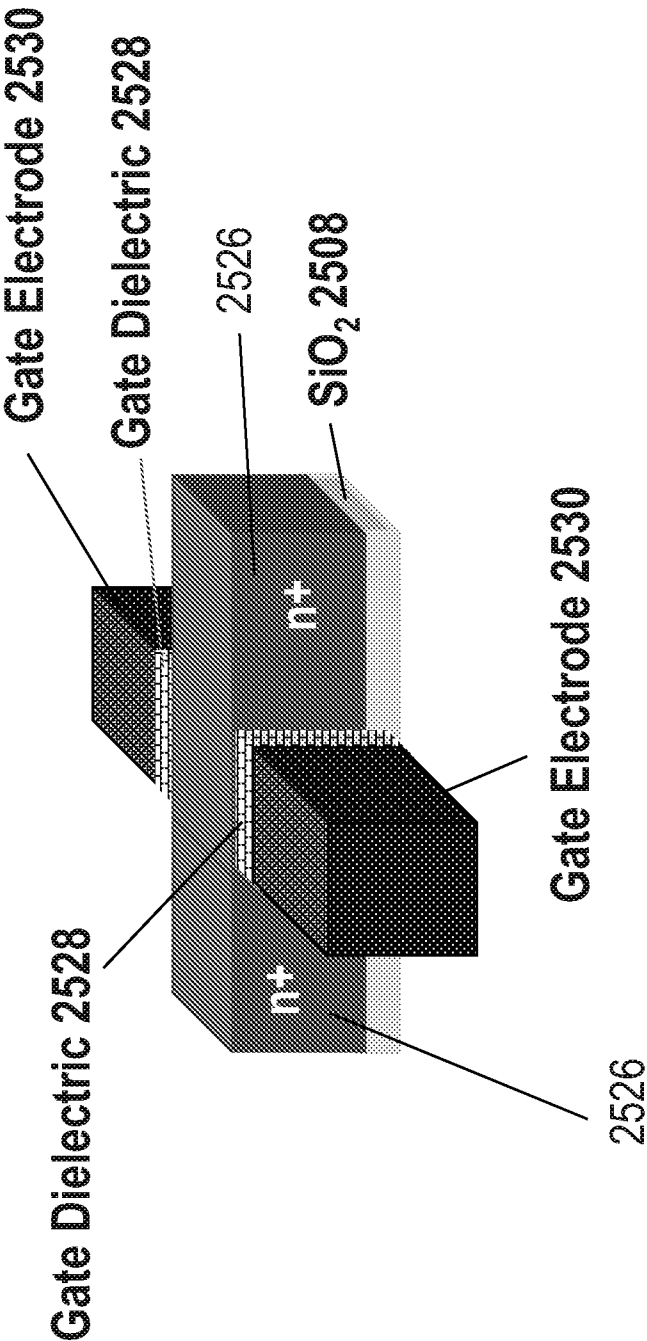


FIG. 25K

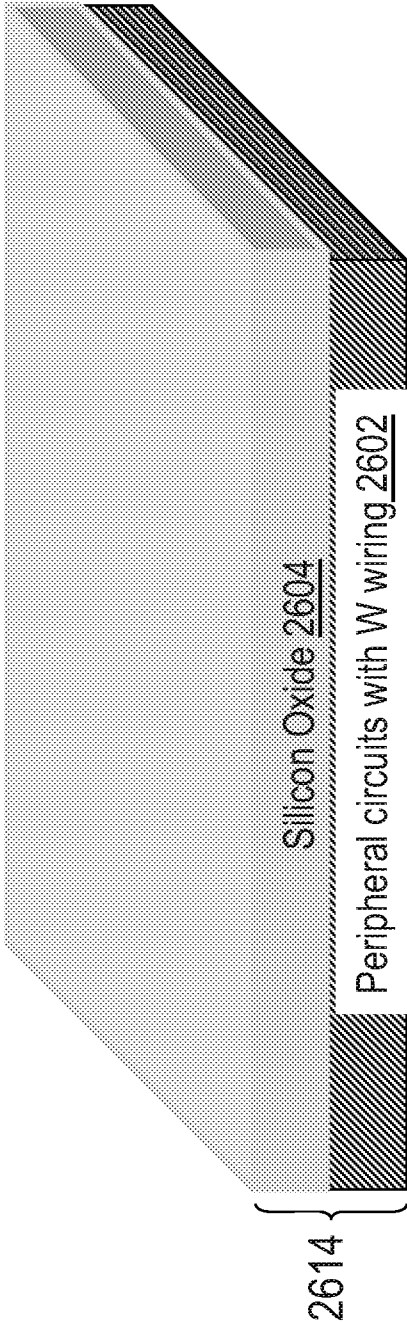


FIG. 26A

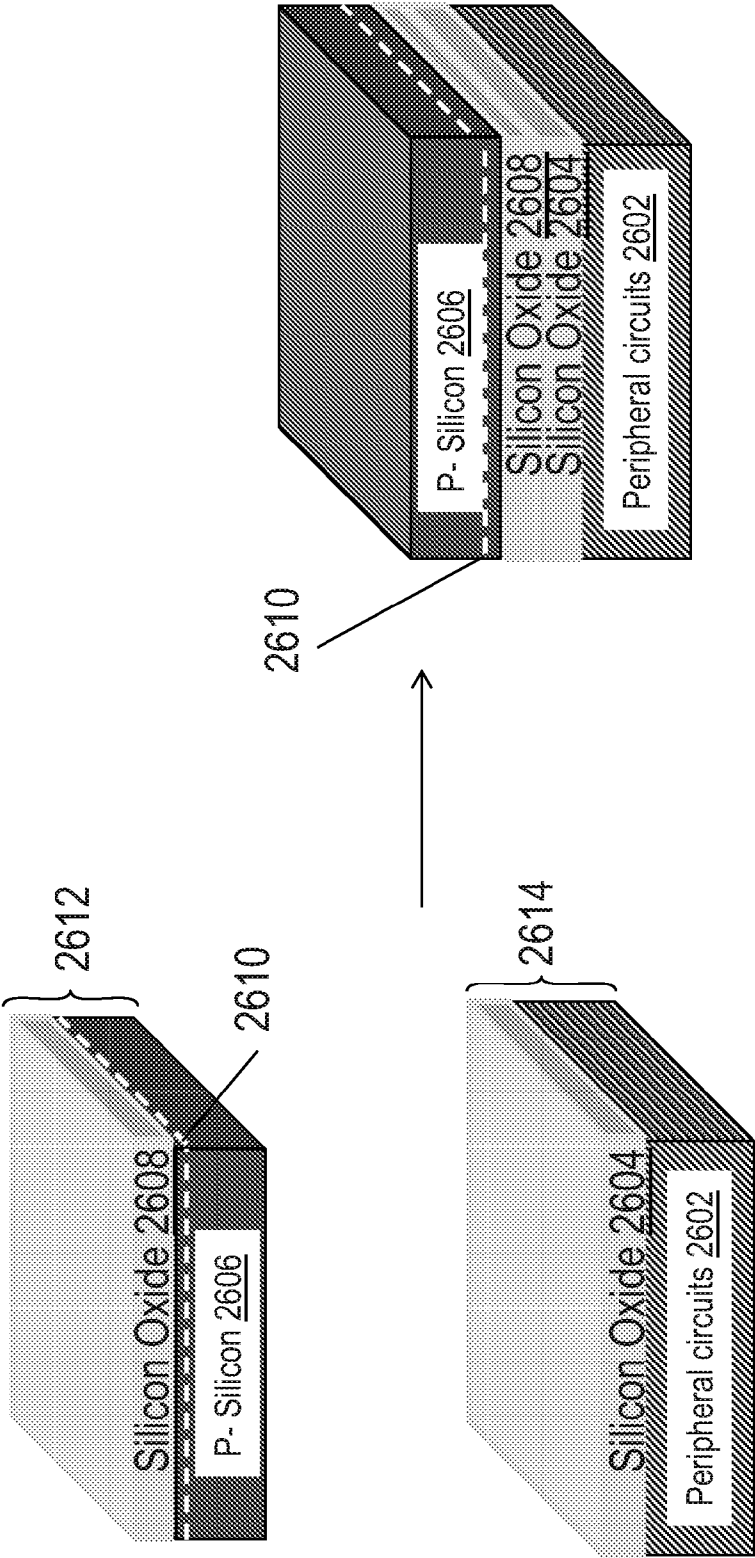


FIG. 26B

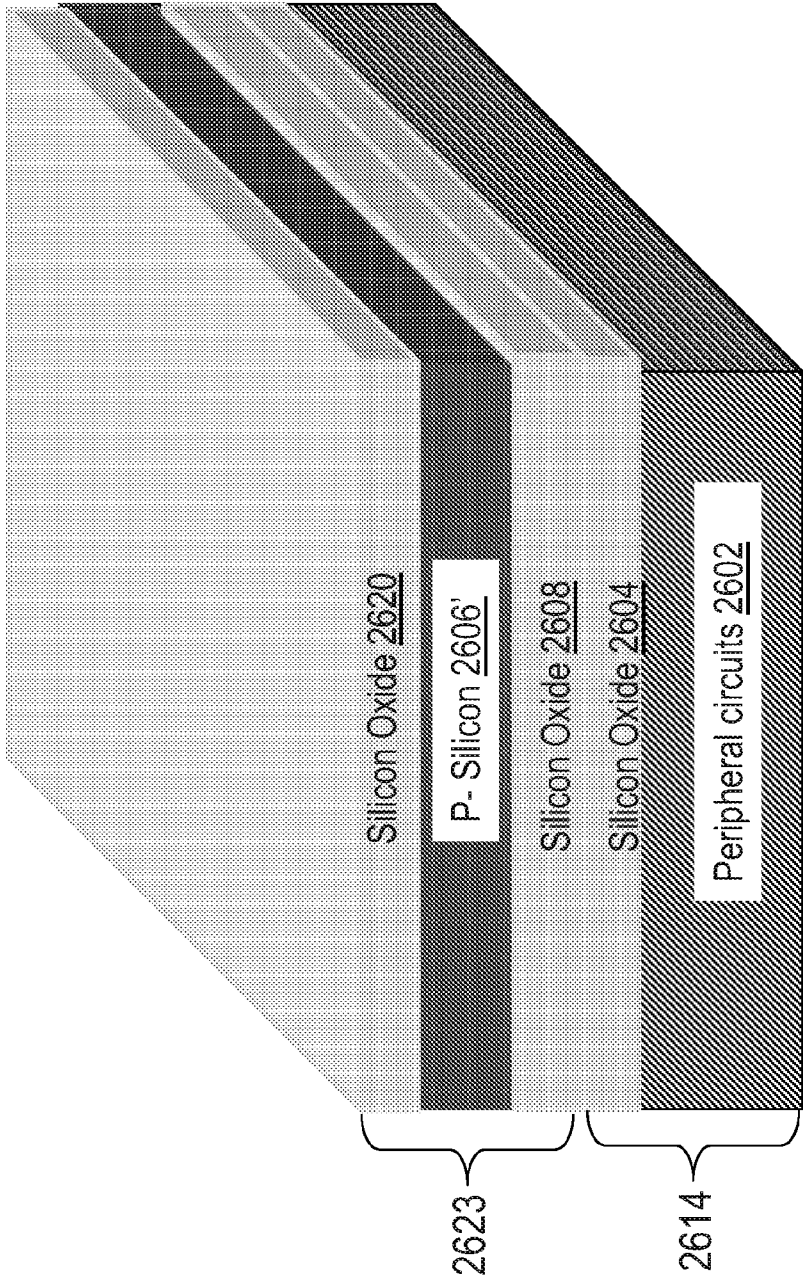


FIG. 26C

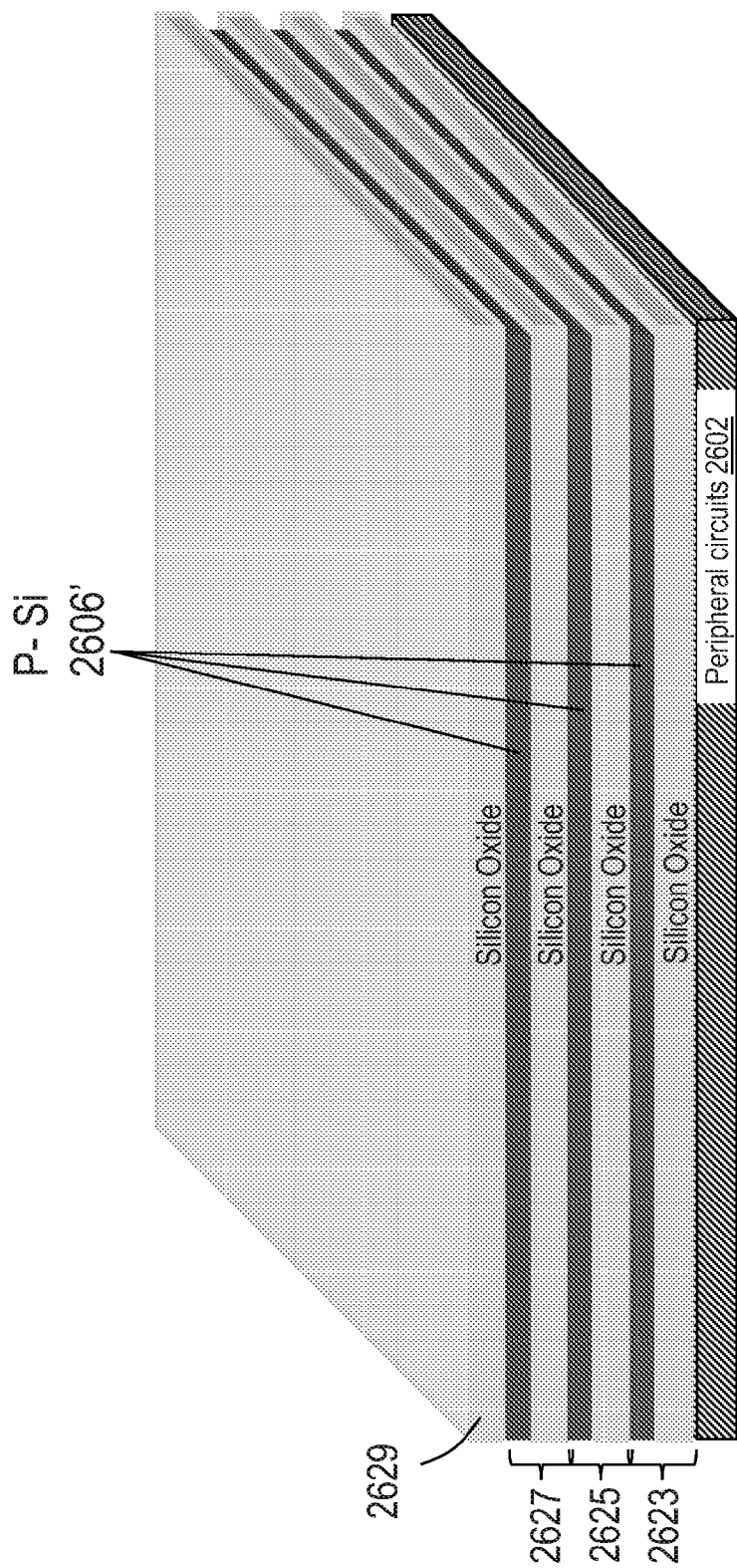


FIG. 26D

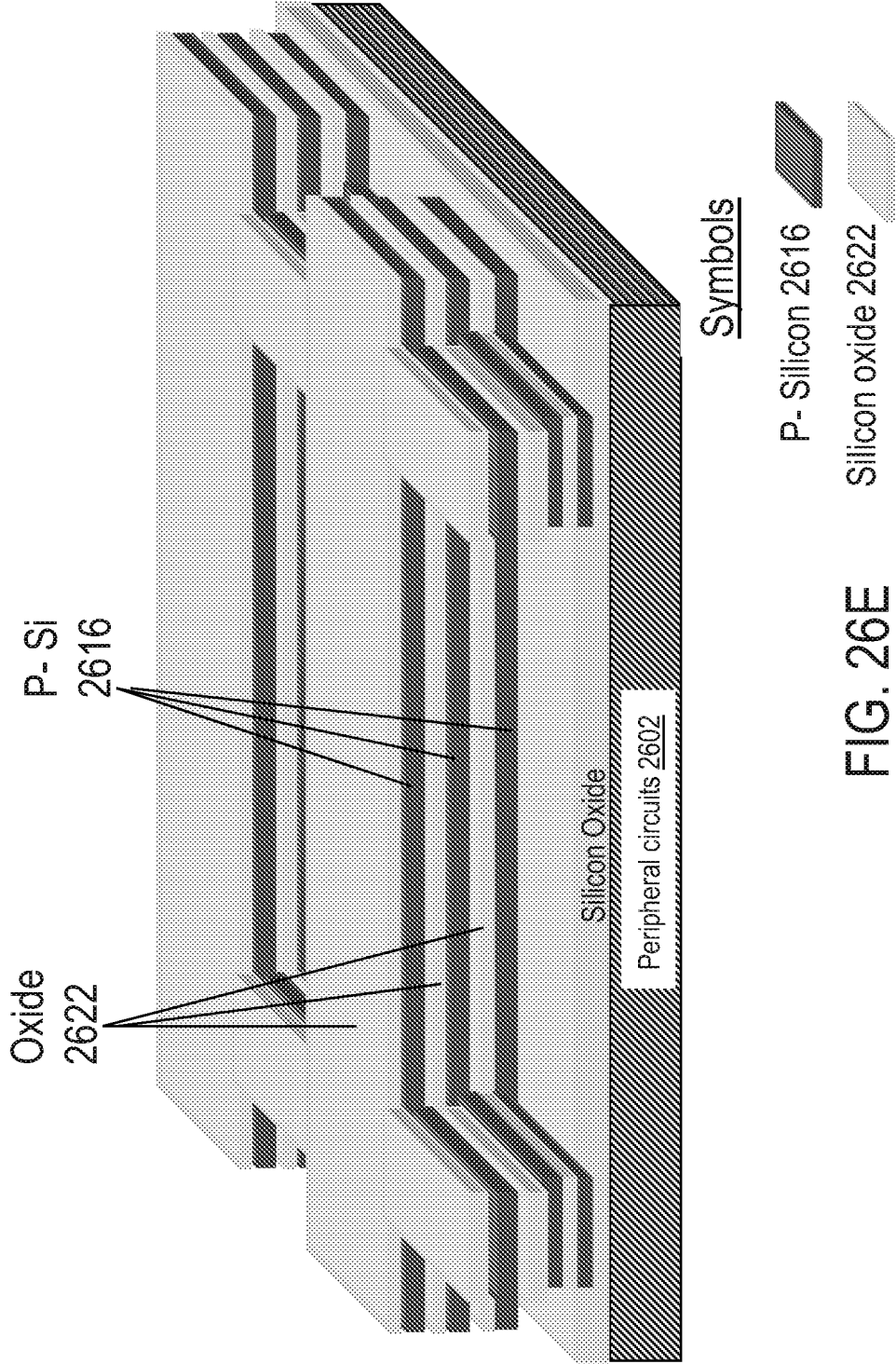


FIG. 26E

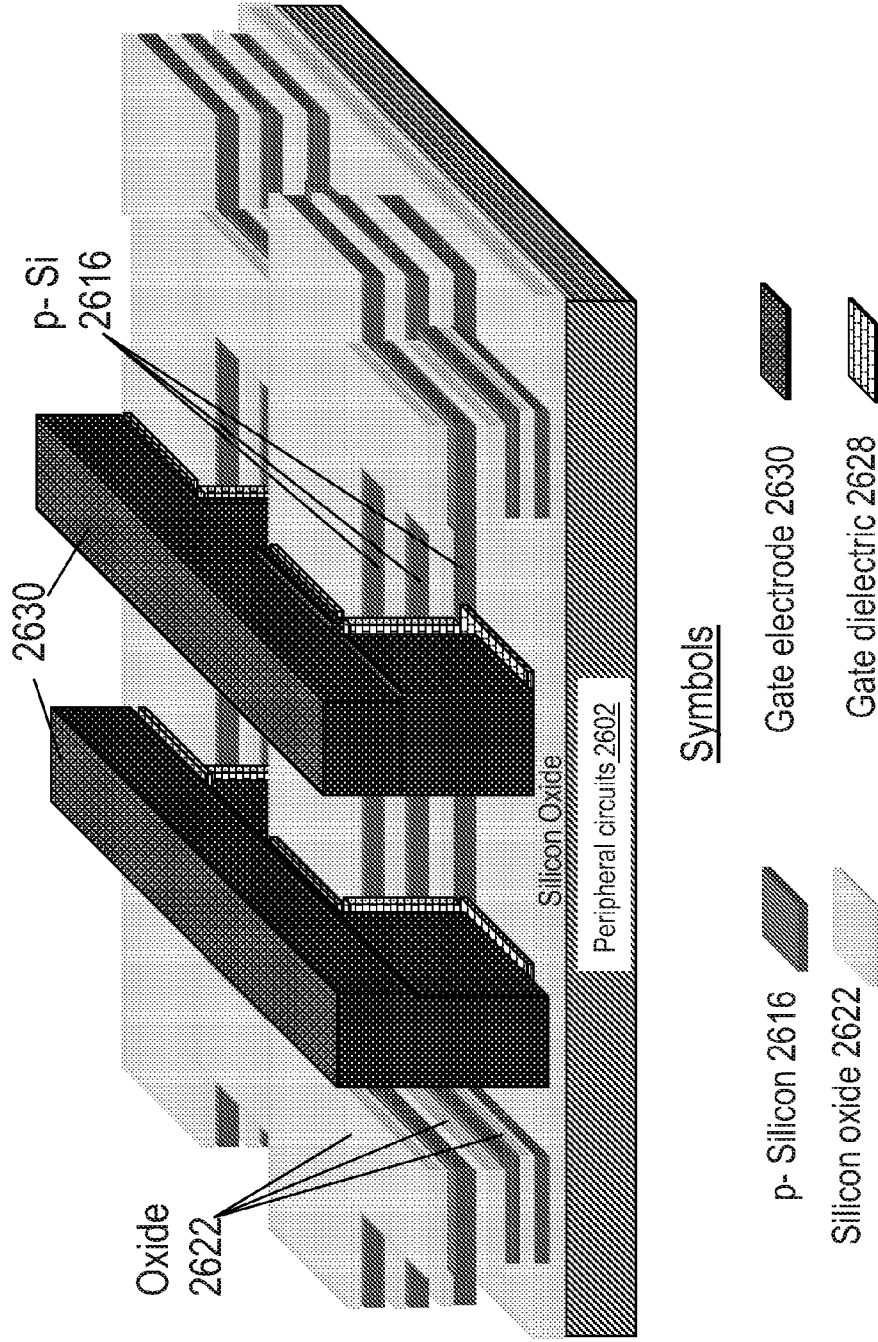


FIG. 26F

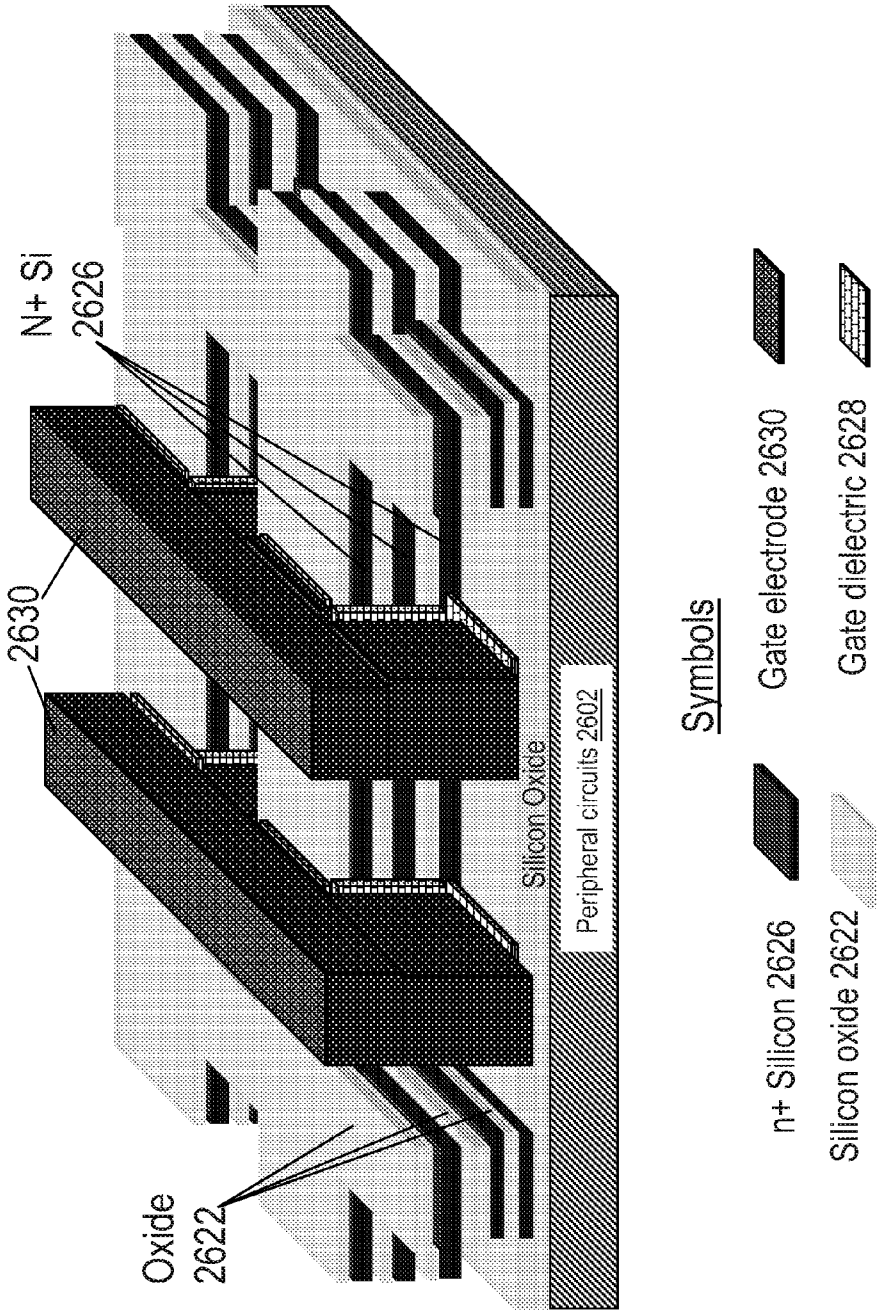


FIG. 26G



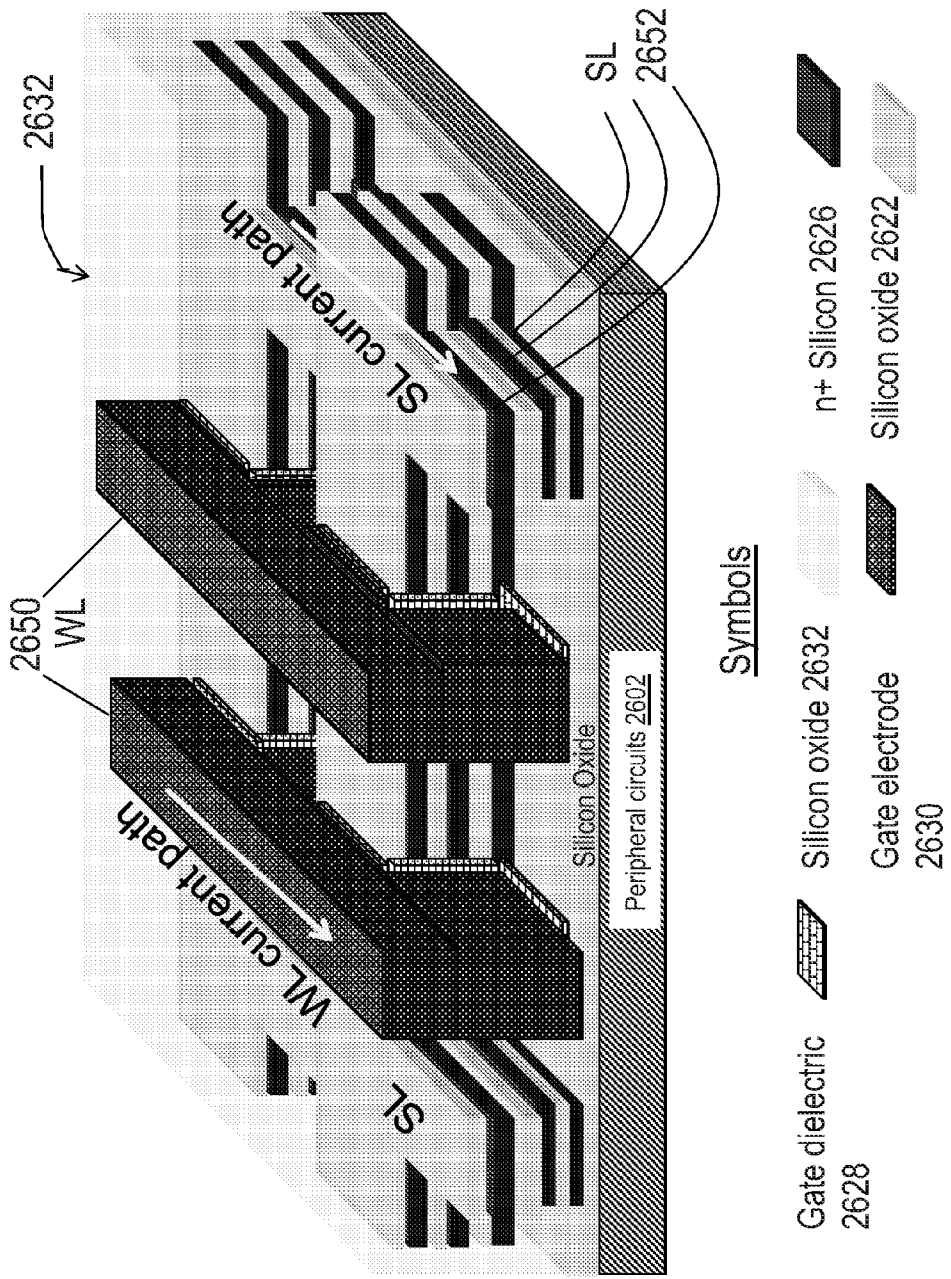
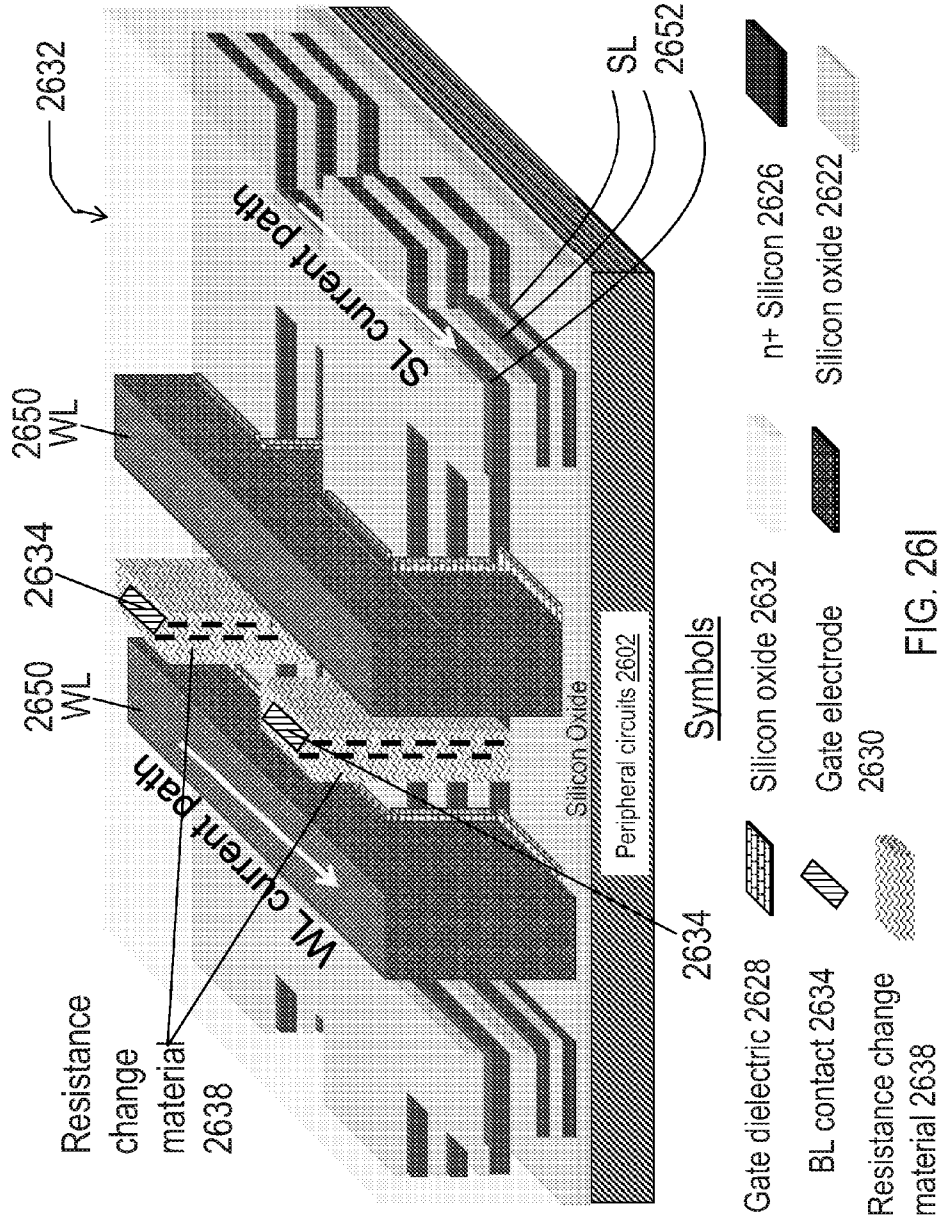


FIG. 26H



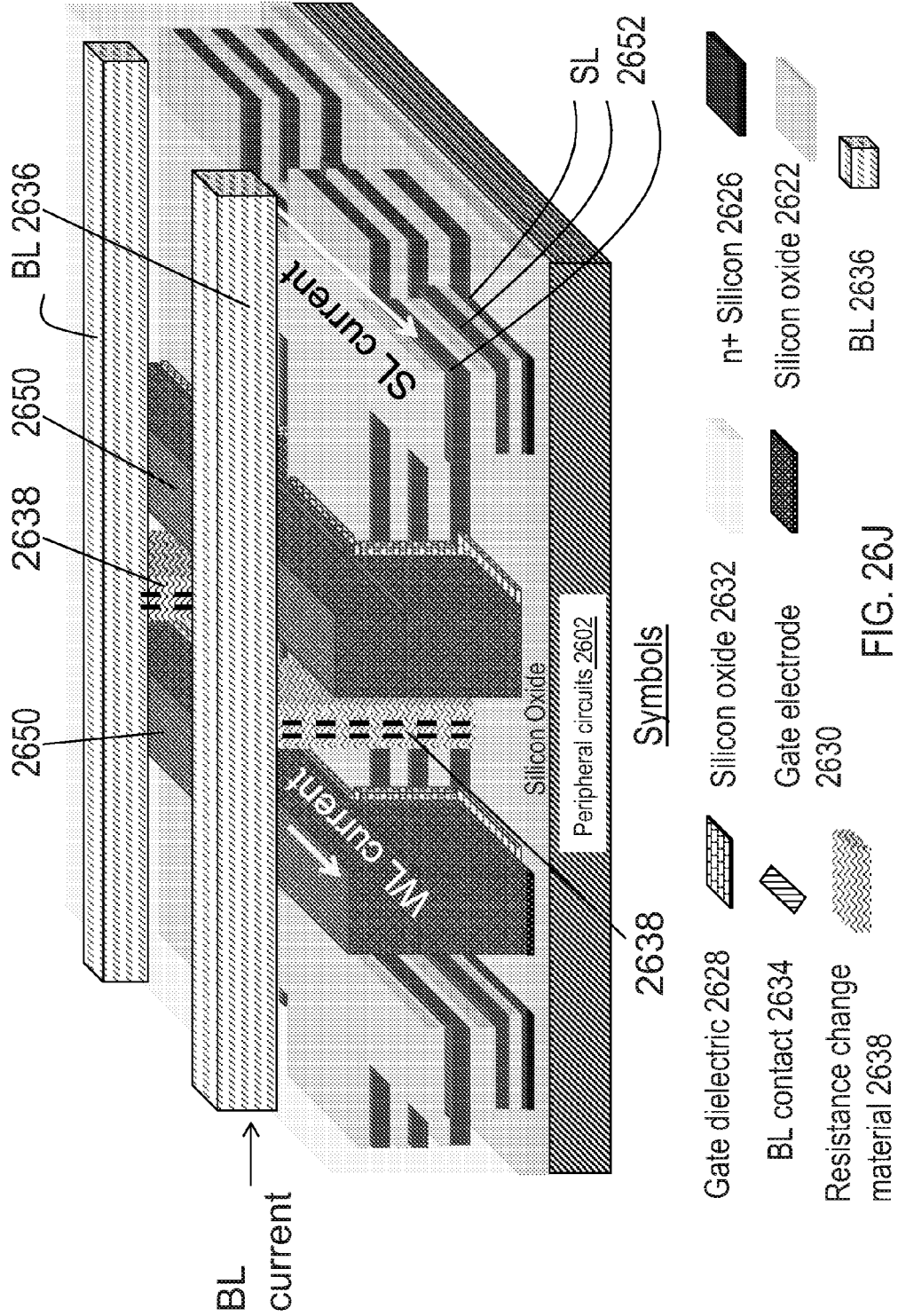


FIG. 26J

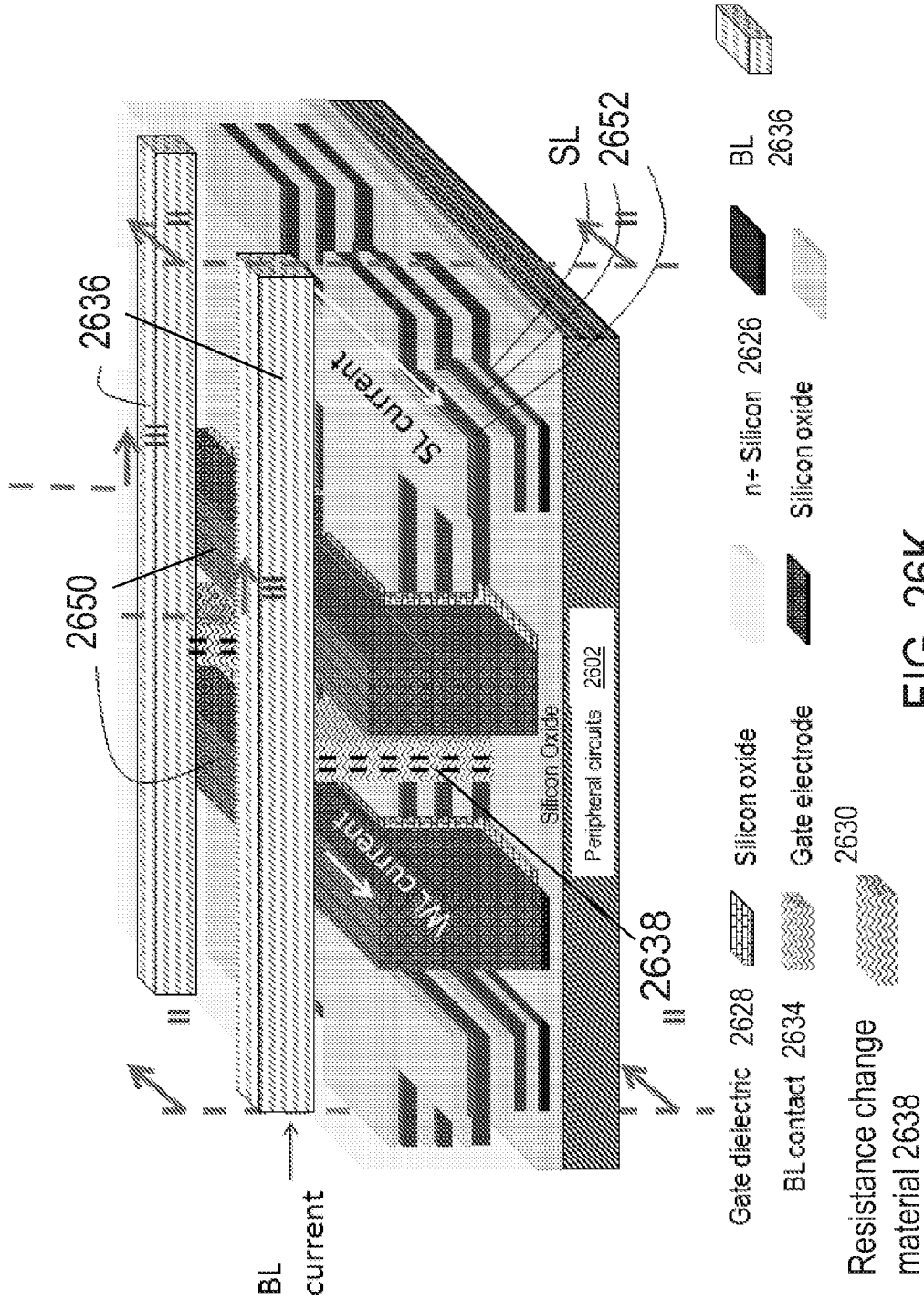
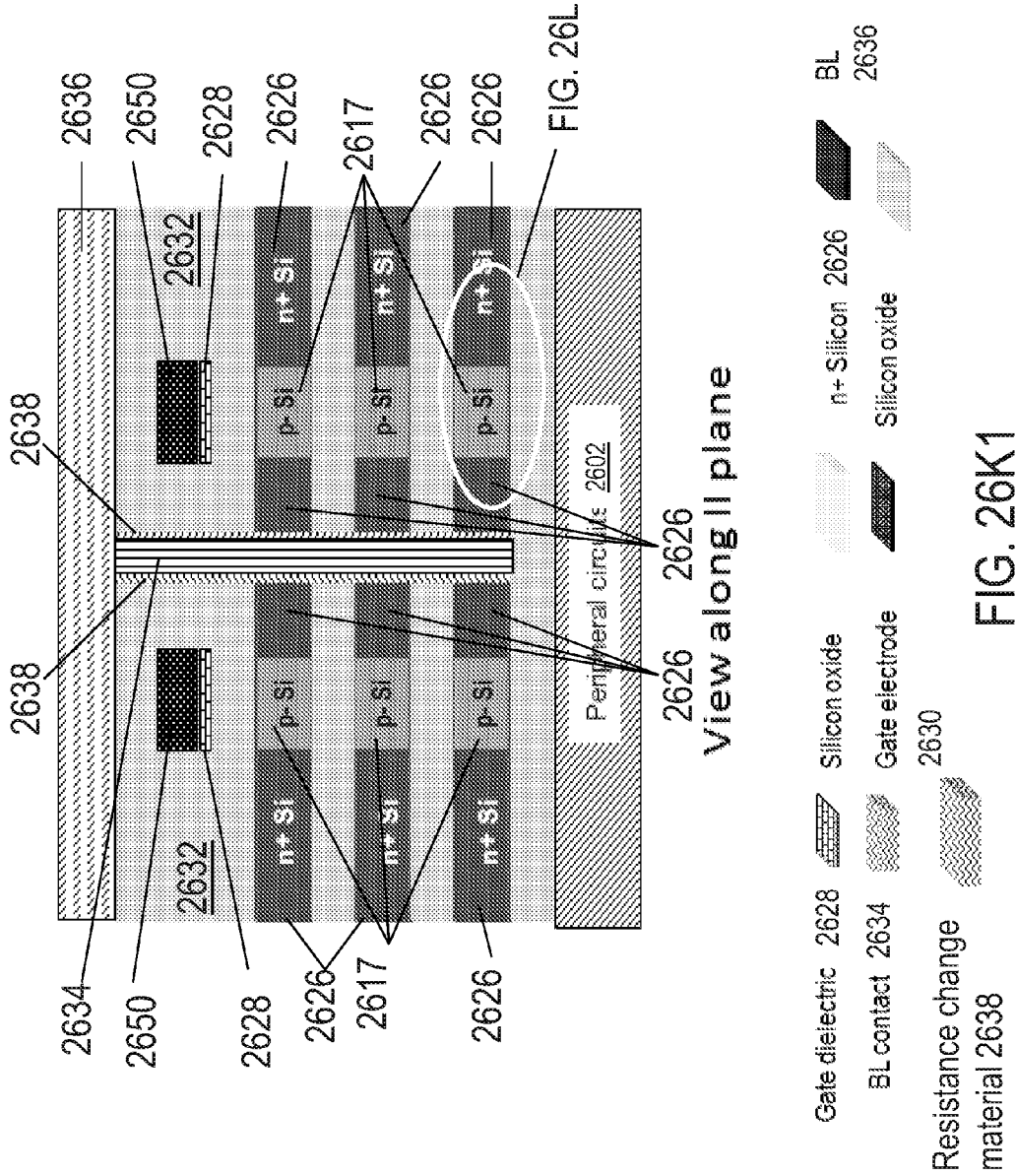


FIG. 26K



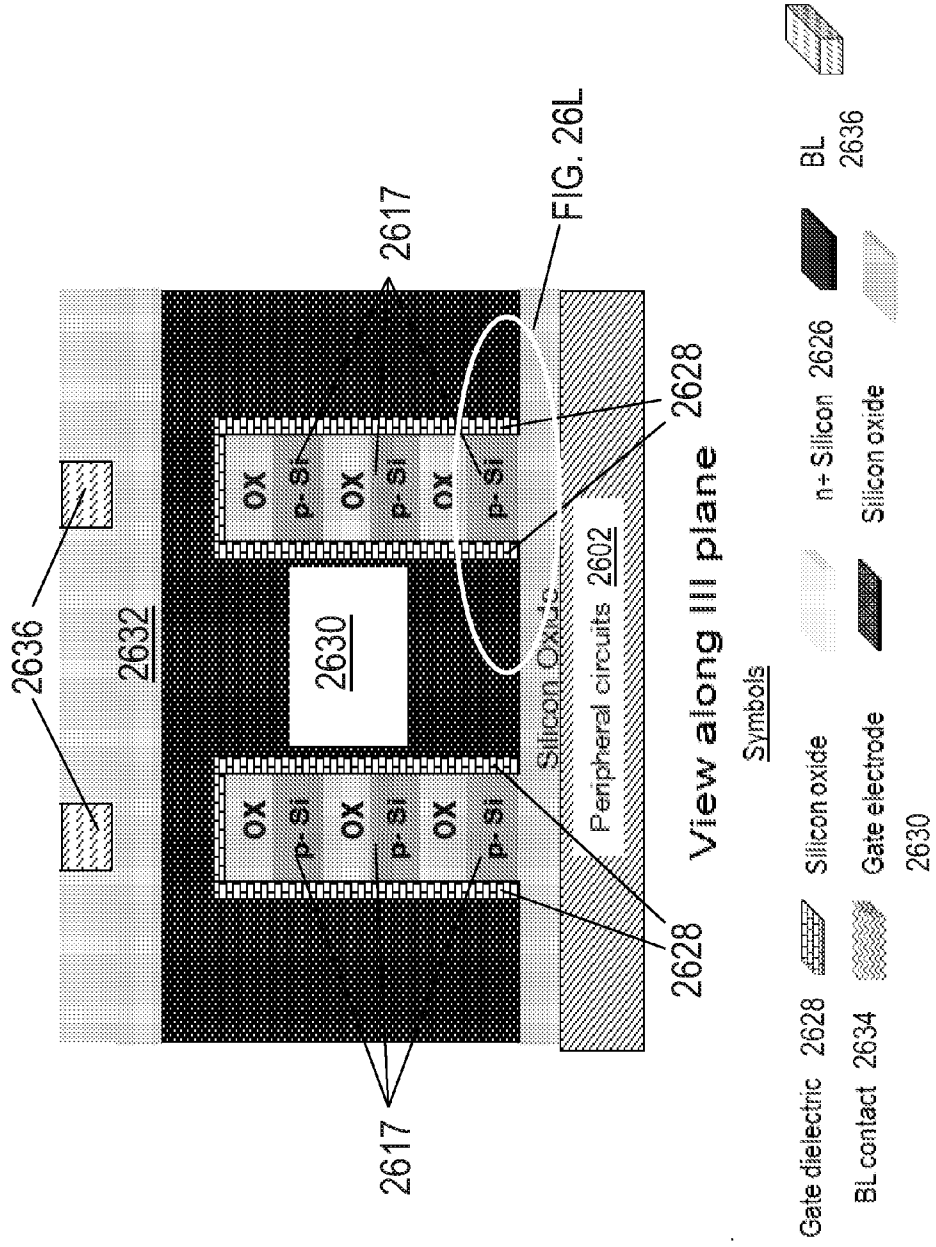


FIG. 26K2

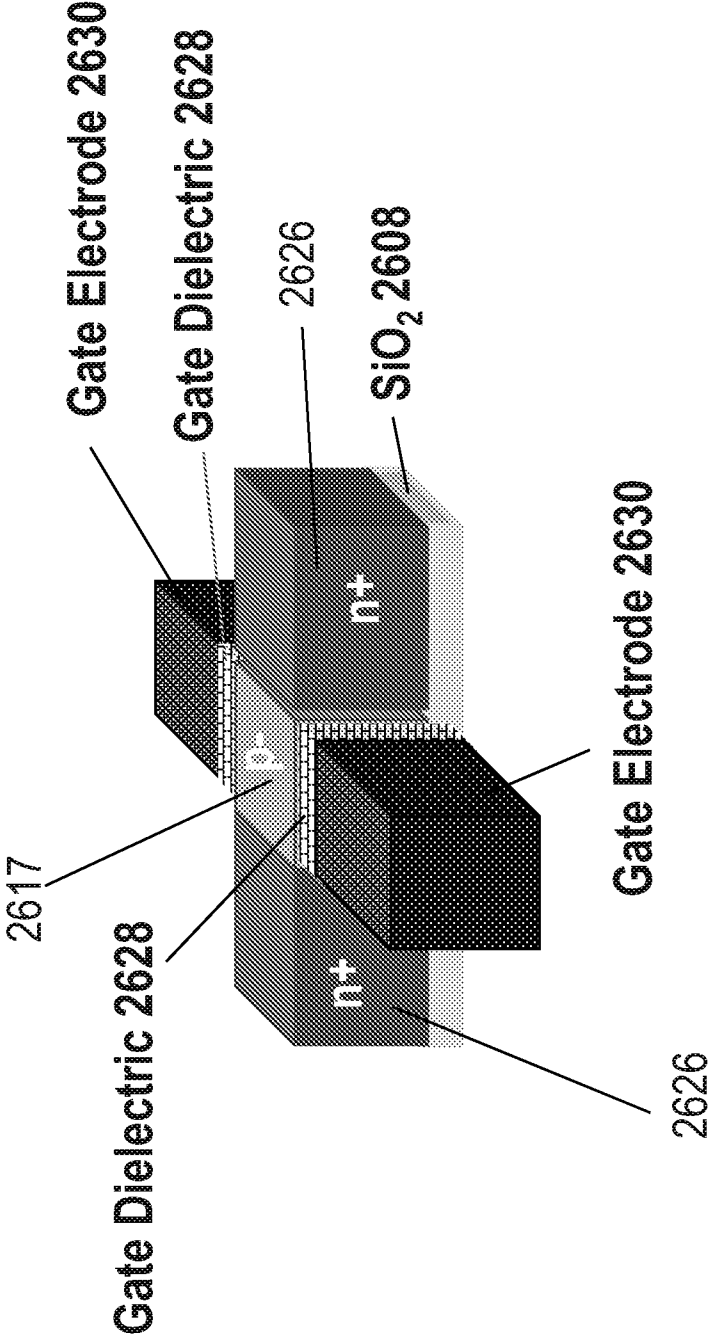


FIG. 26L

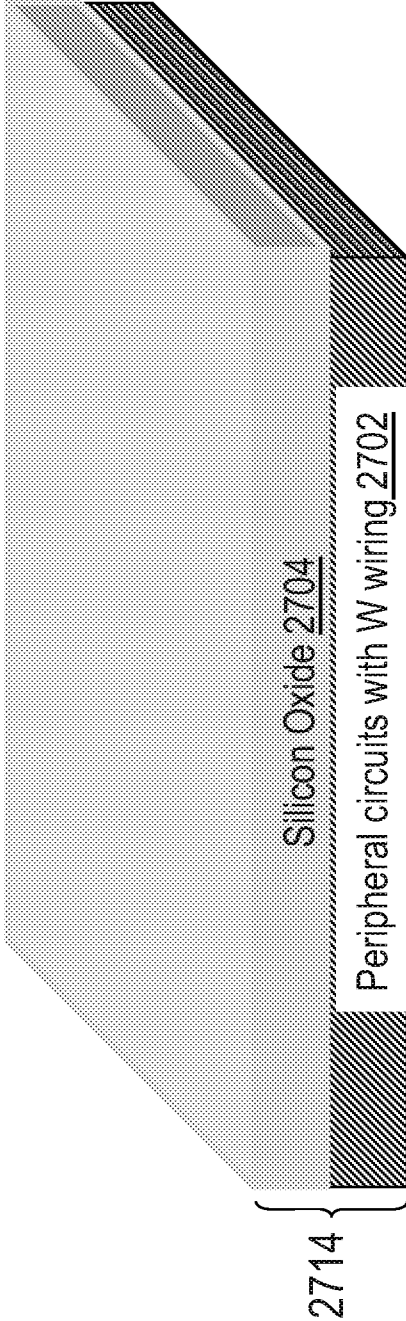


FIG. 27A



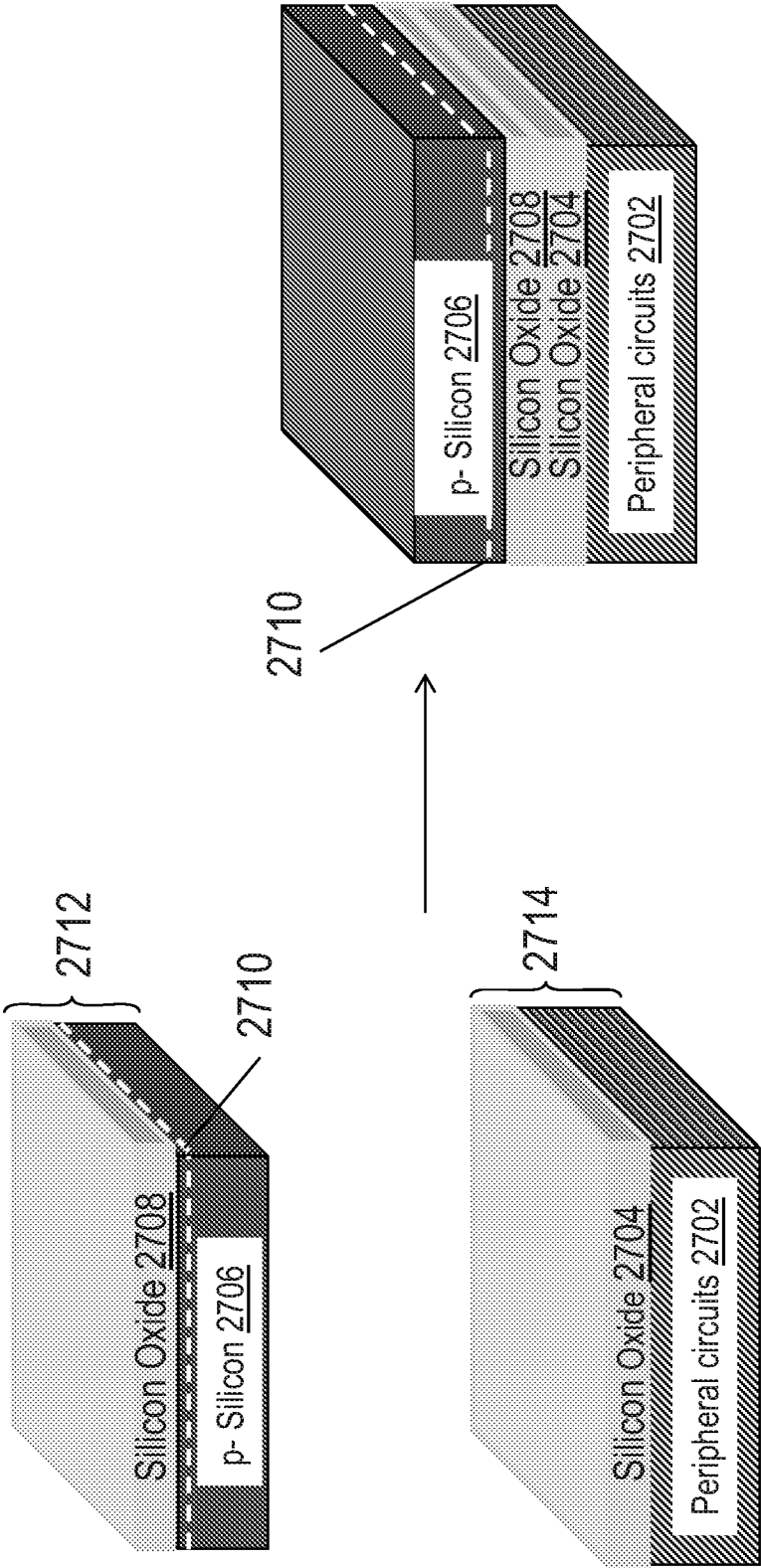


FIG. 27B

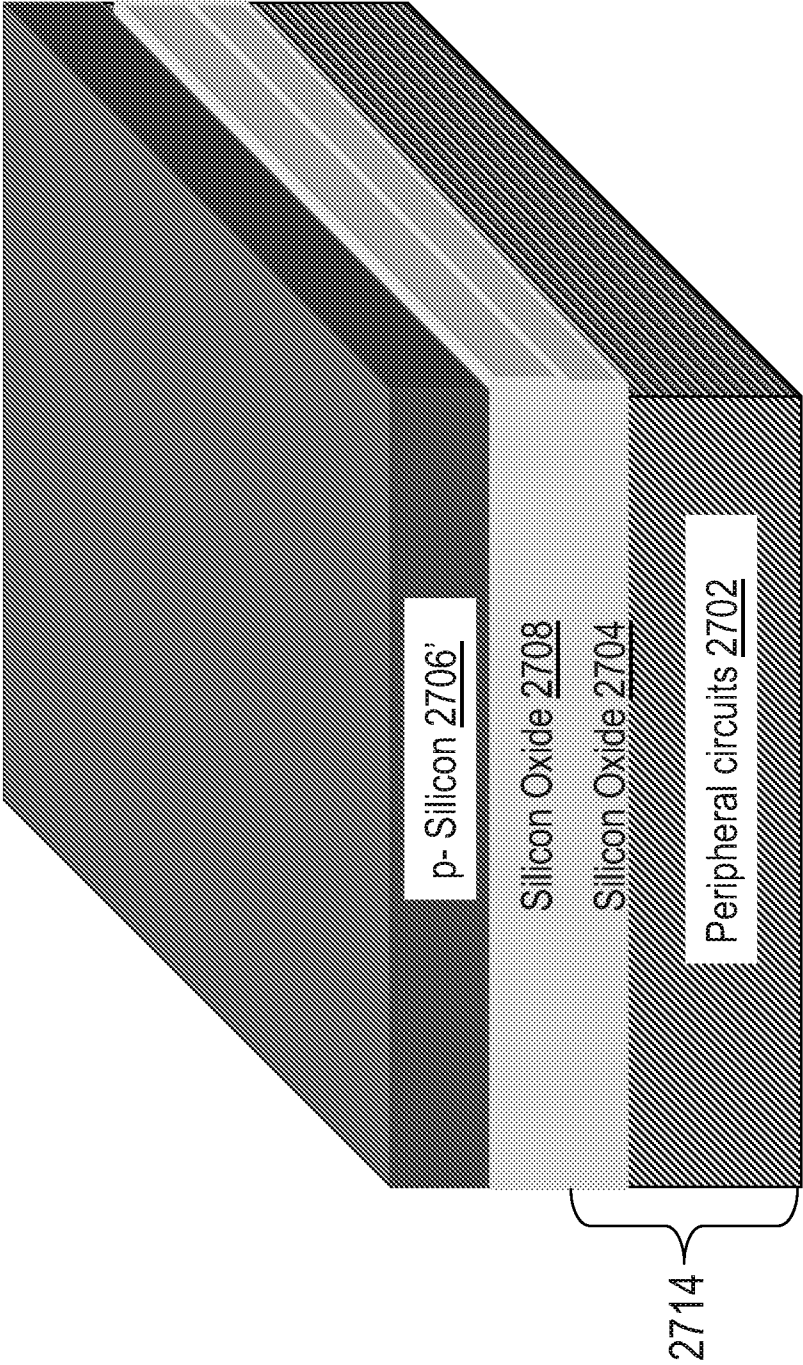


FIG. 27C

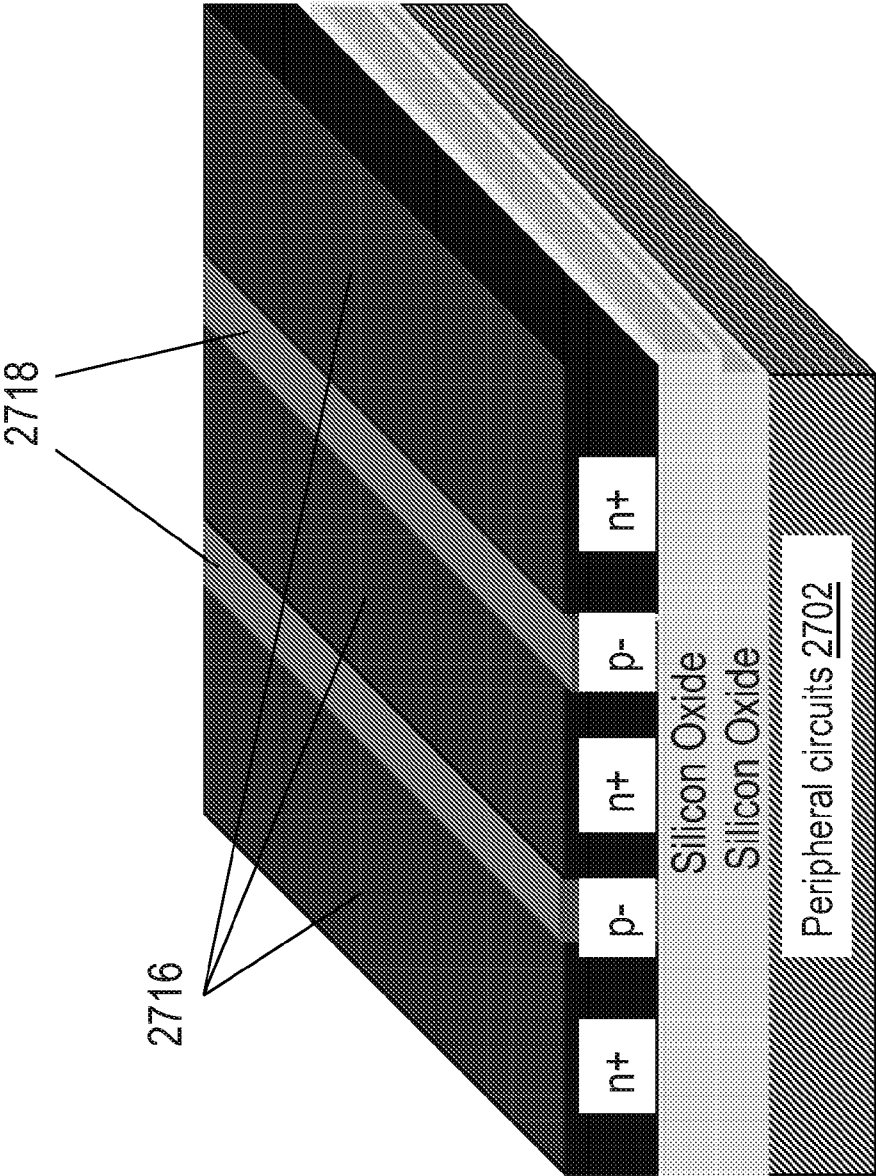


FIG. 27D

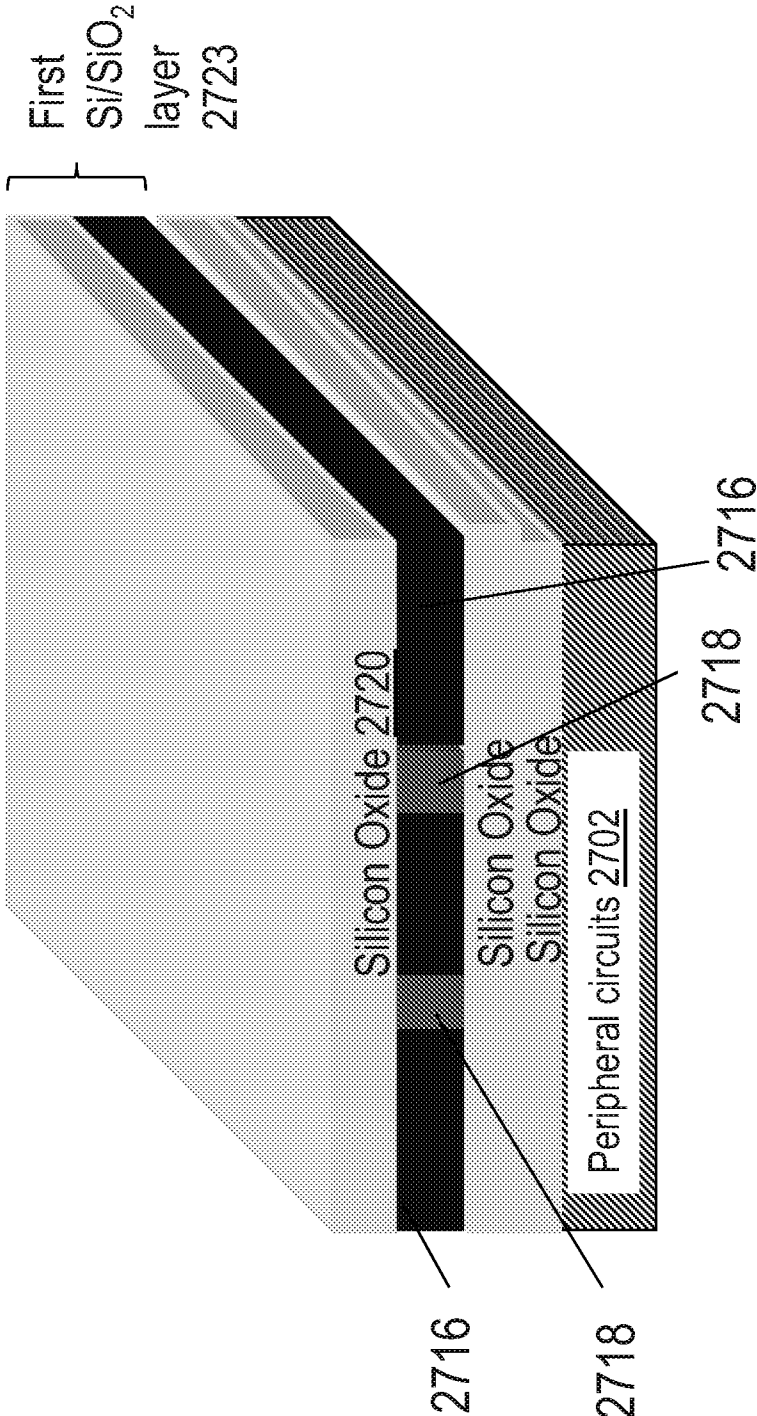


FIG. 27E

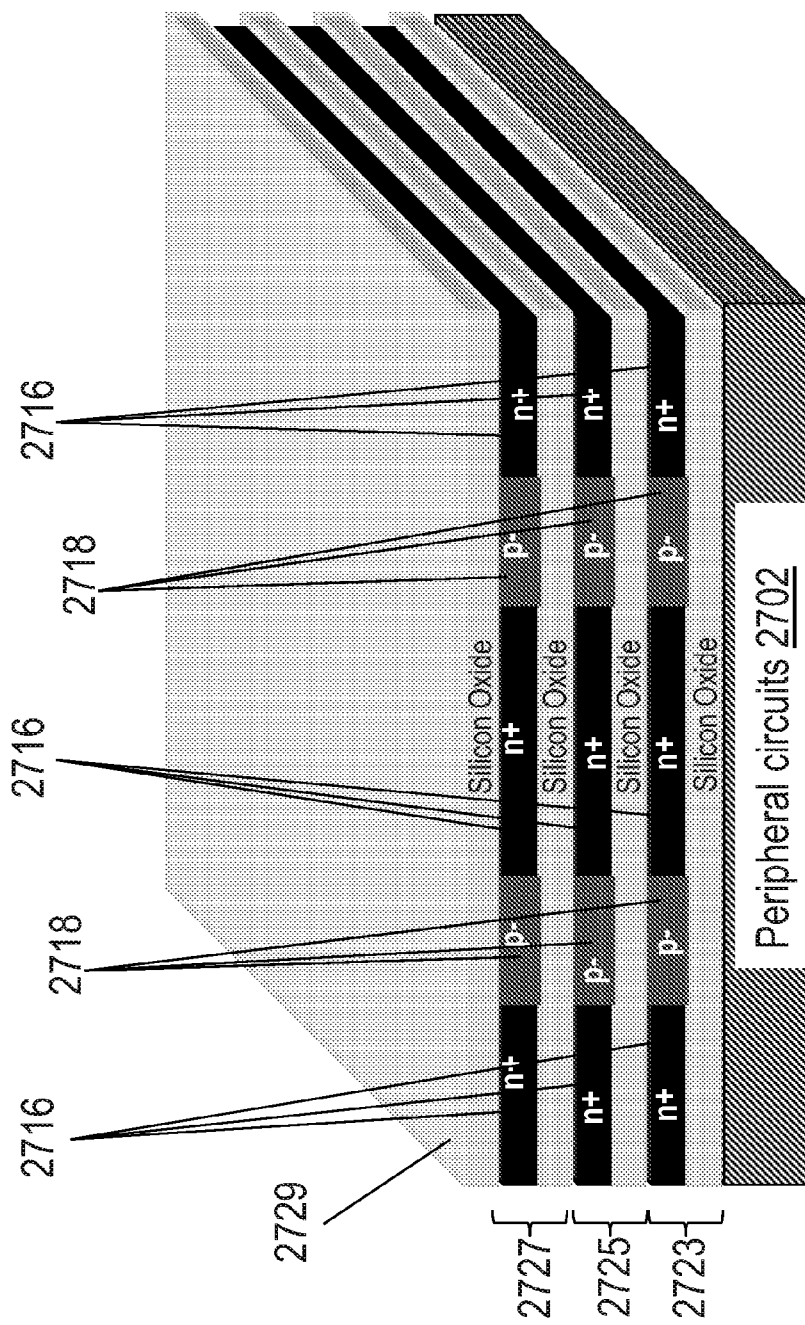
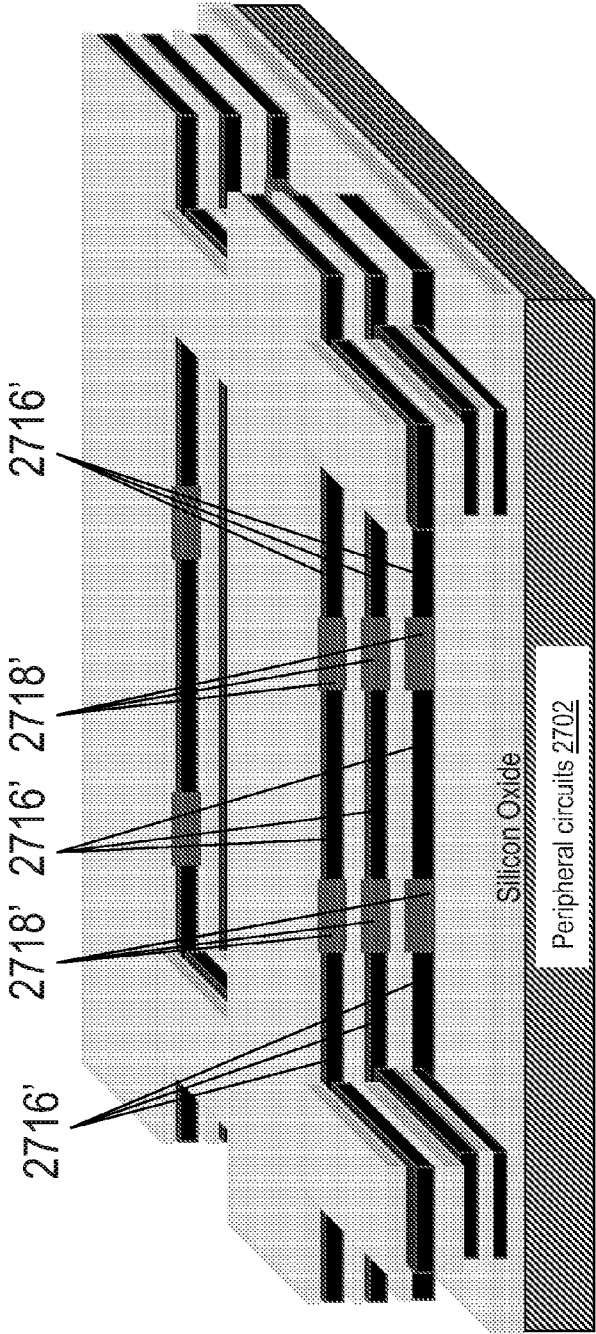


FIG. 27F



Symbols

- p- Silicon 2718' 
- Silicon oxide 
- n+ Silicon 2716' 

FIG. 27G

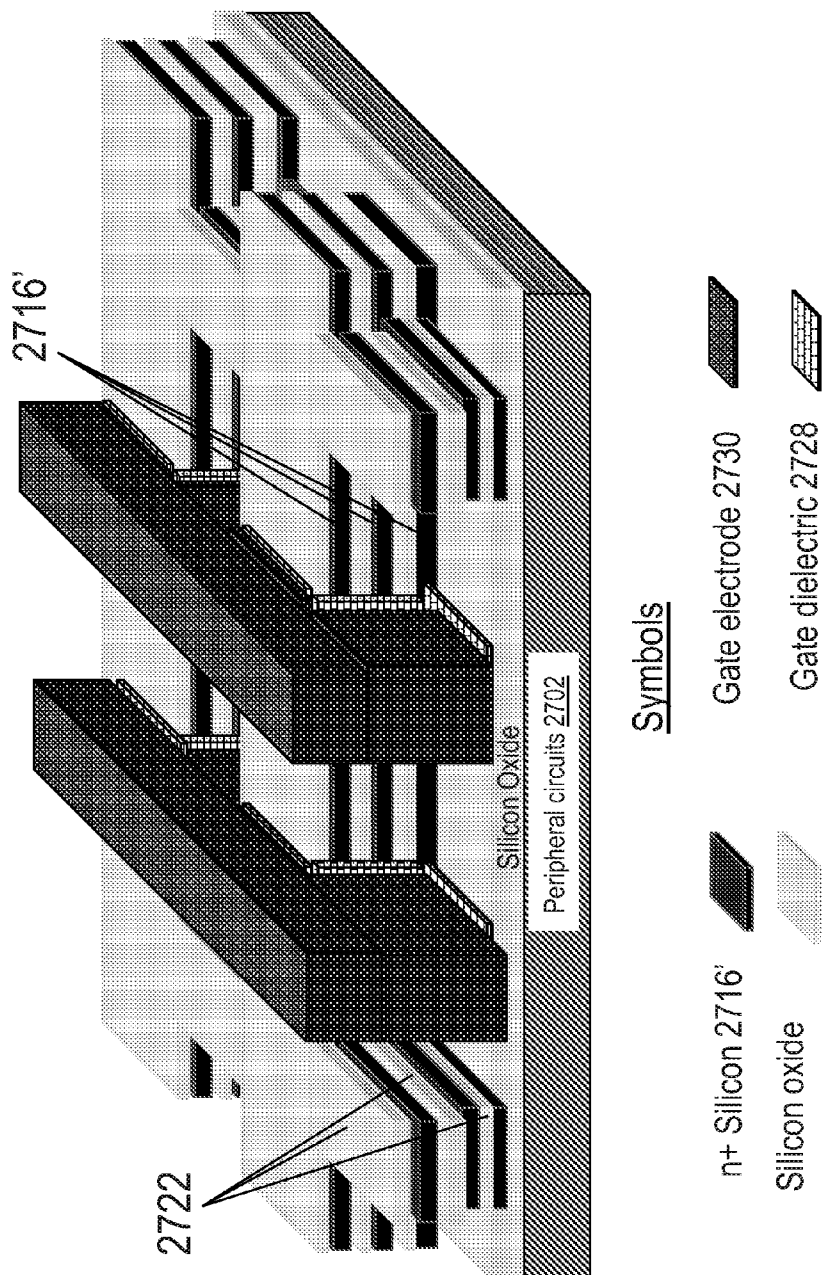


FIG. 27H

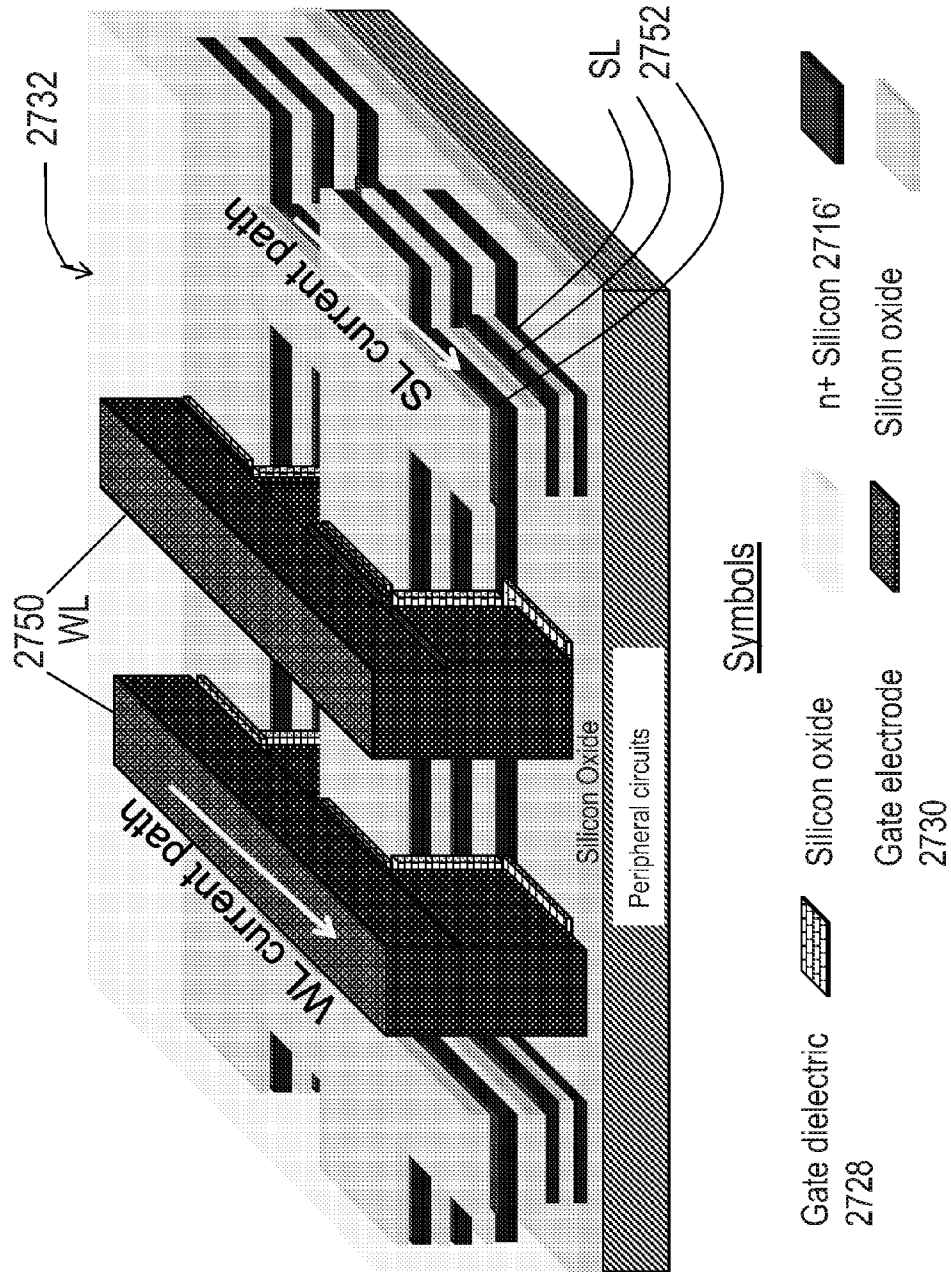
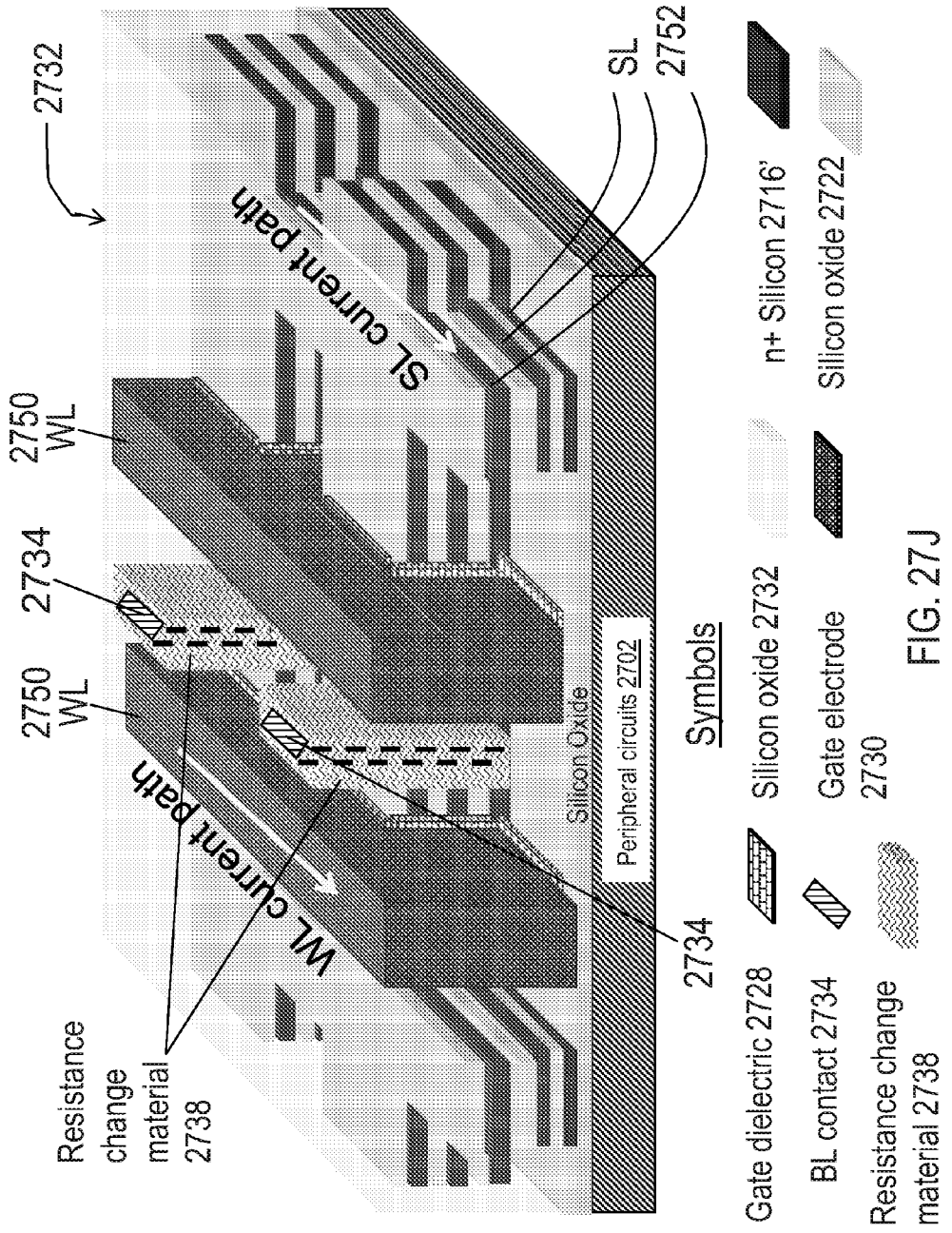
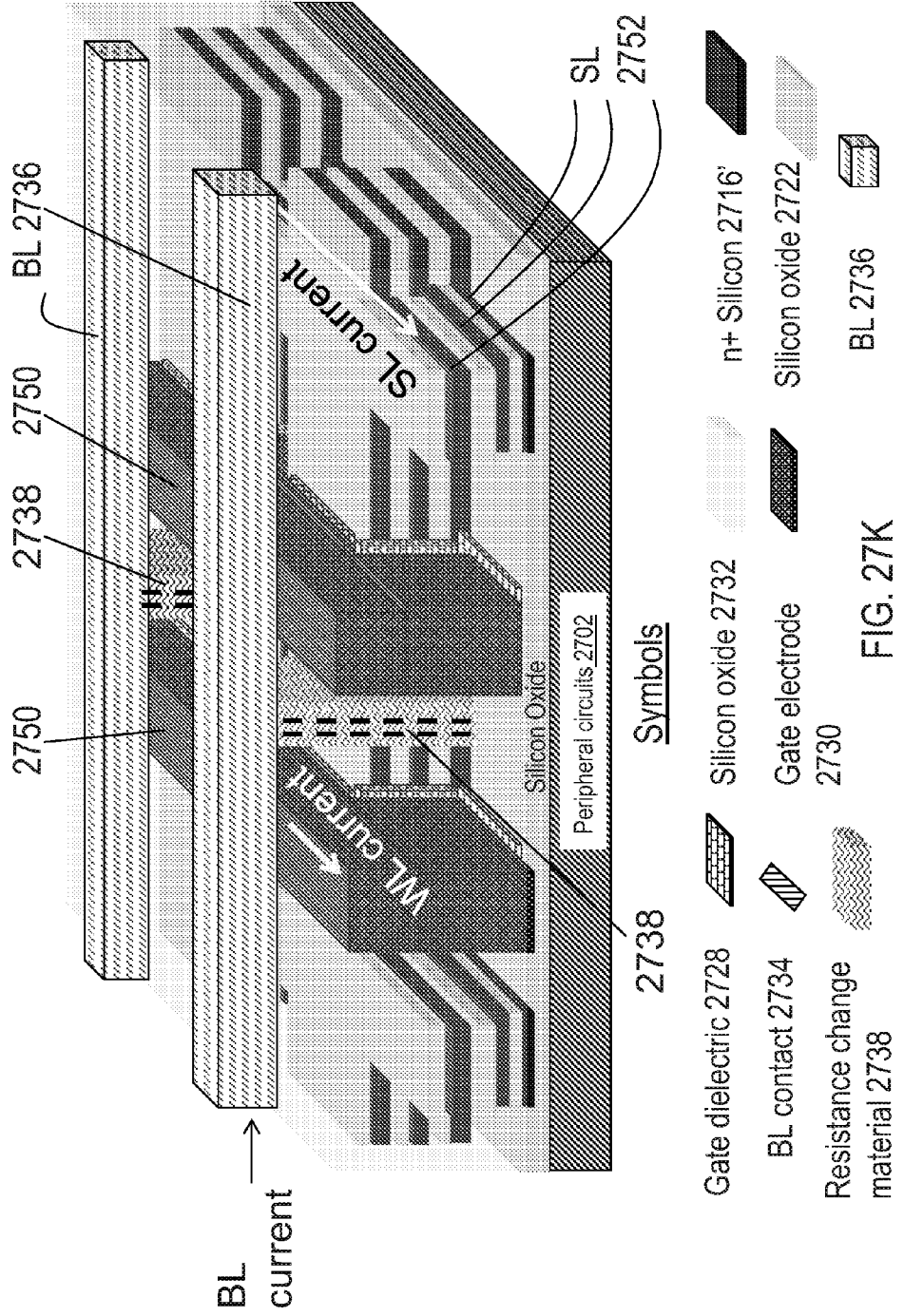


FIG. 271







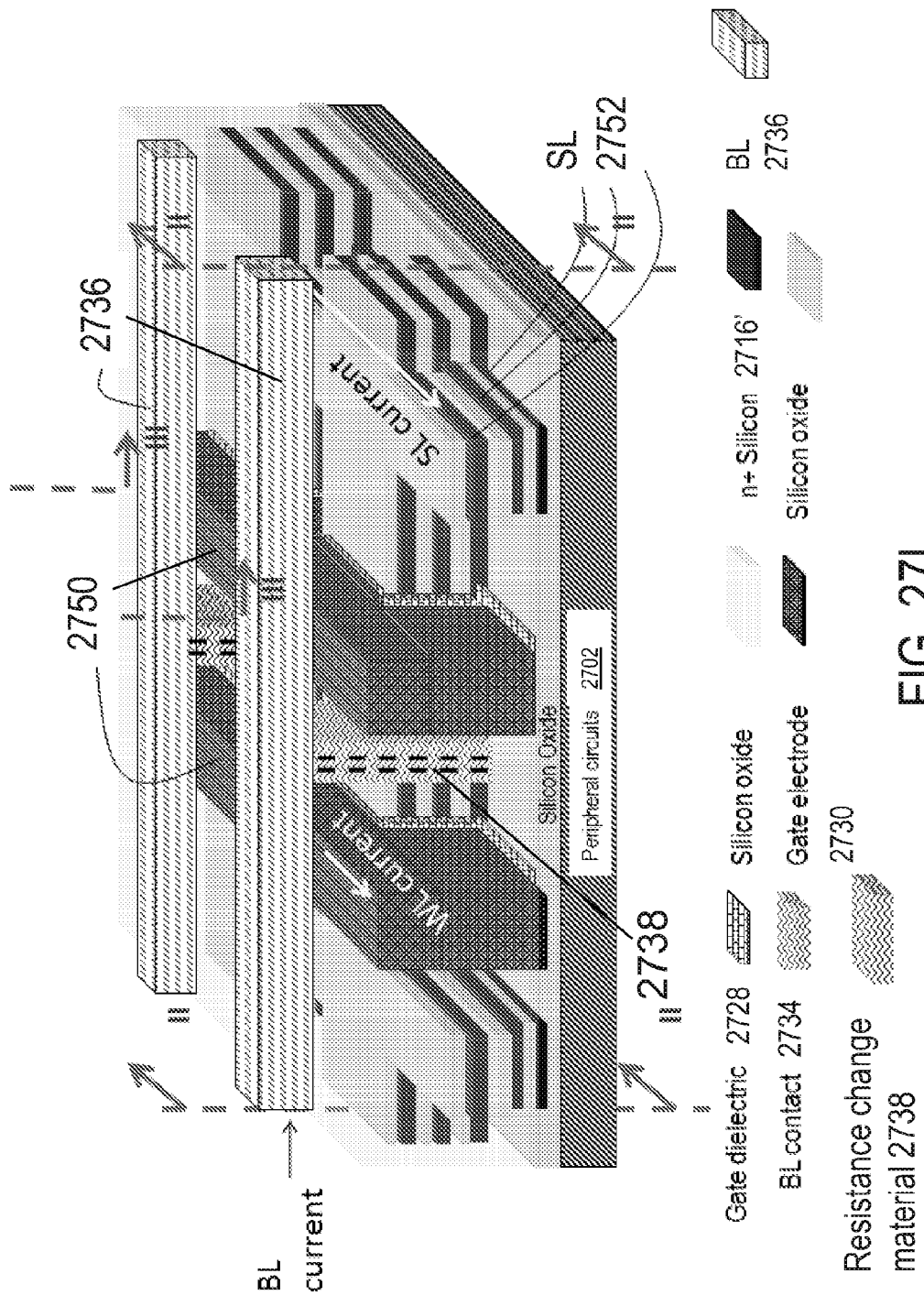


FIG. 27L

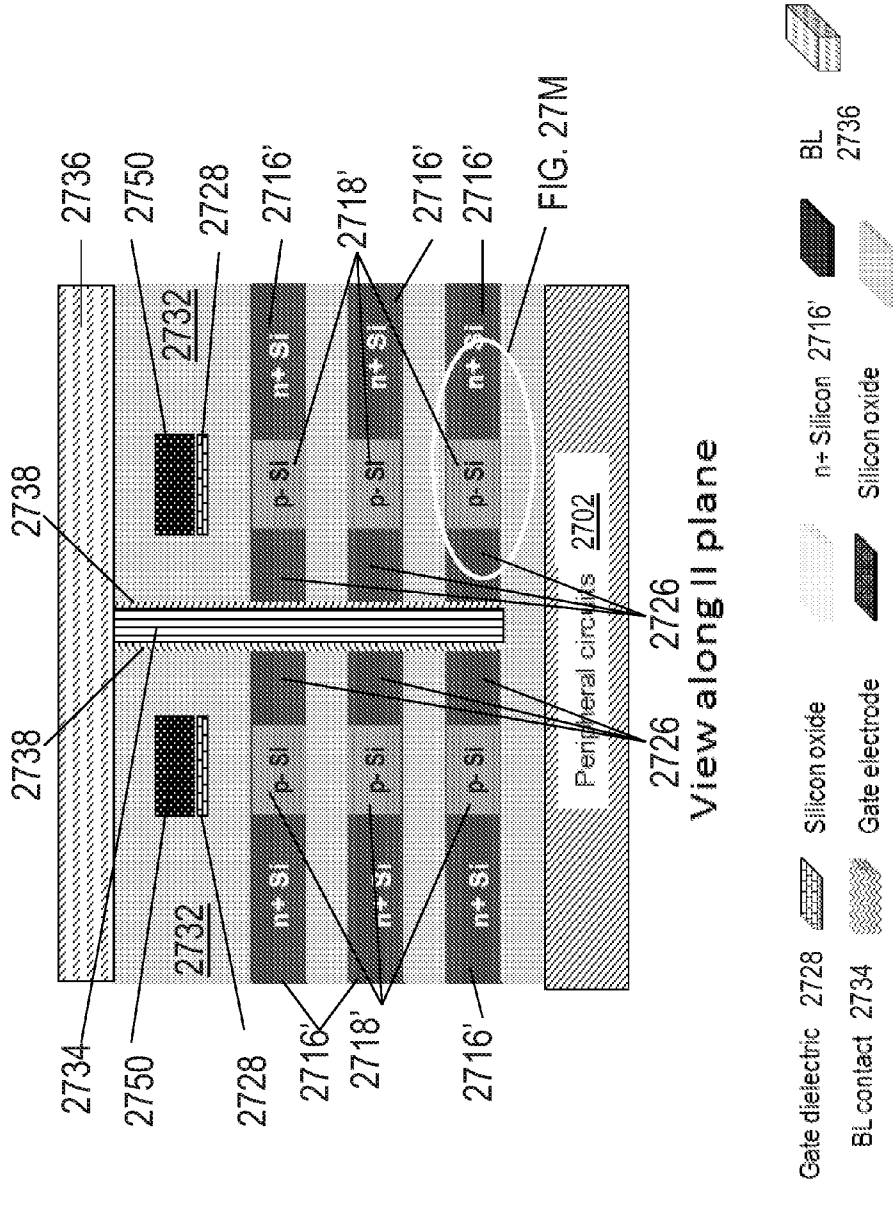


FIG. 27L1

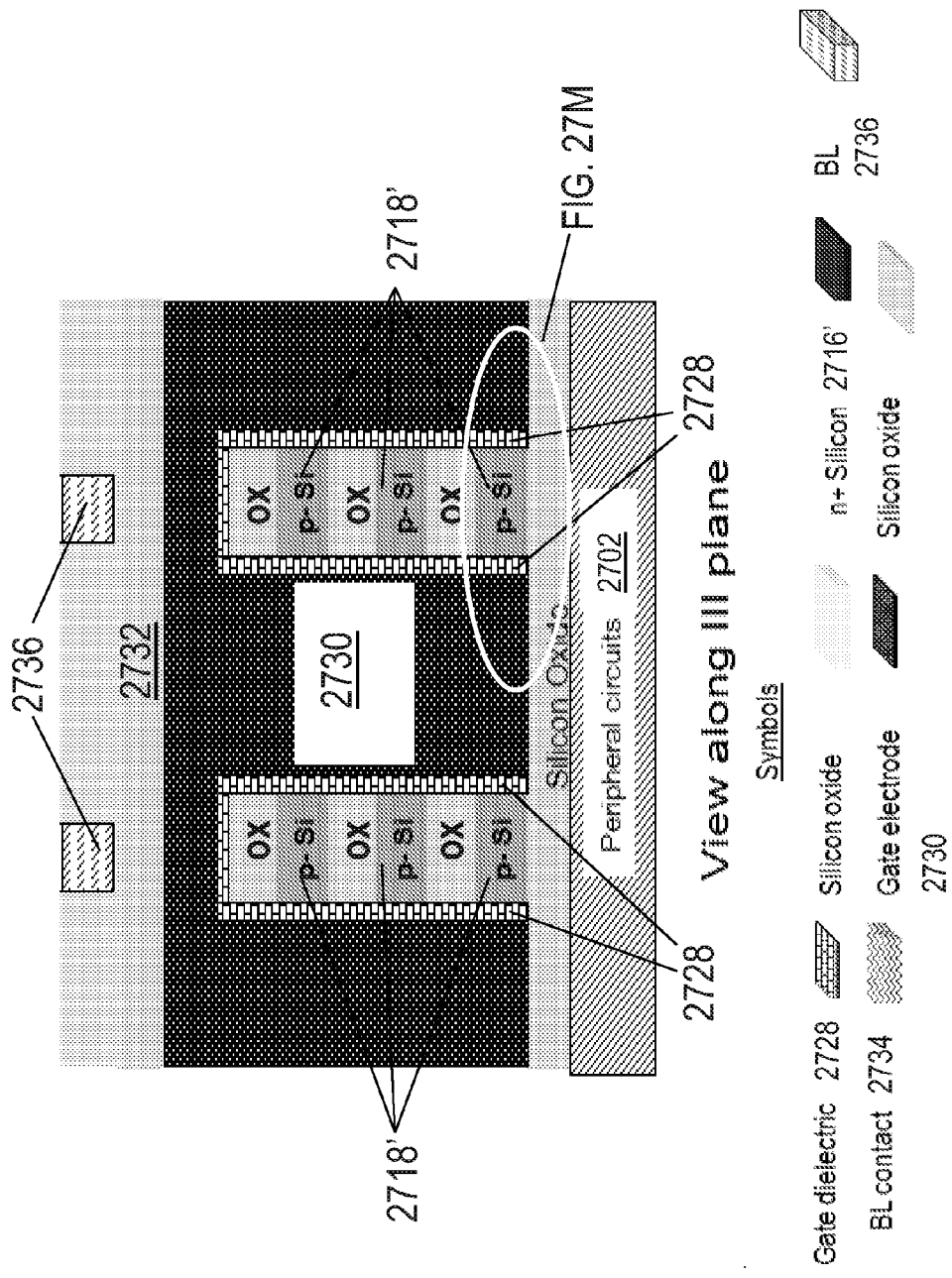


FIG. 27L2

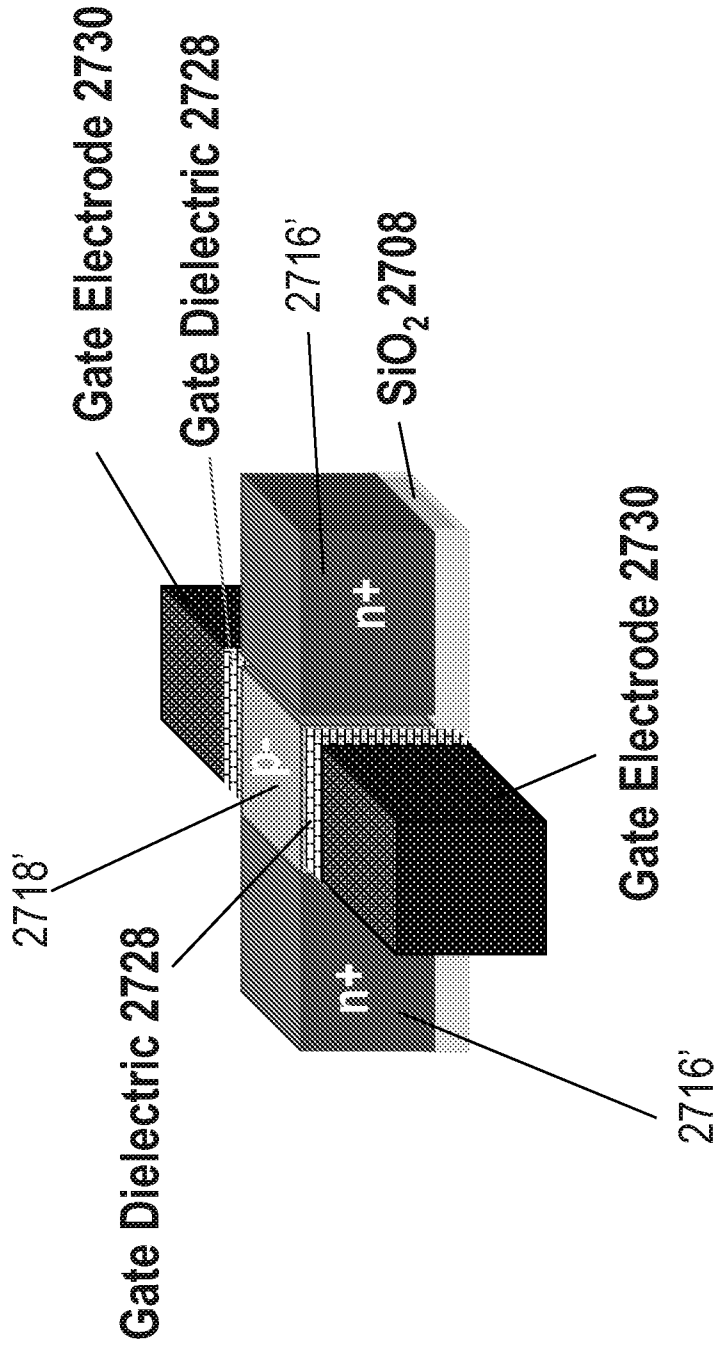


FIG. 27M

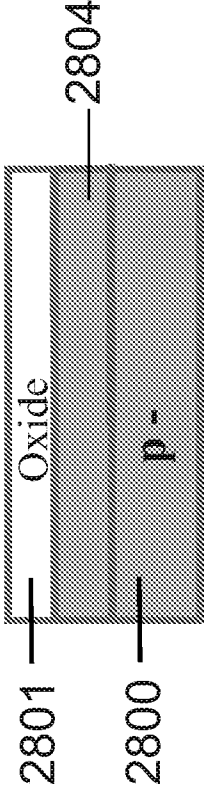


FIG. 28A

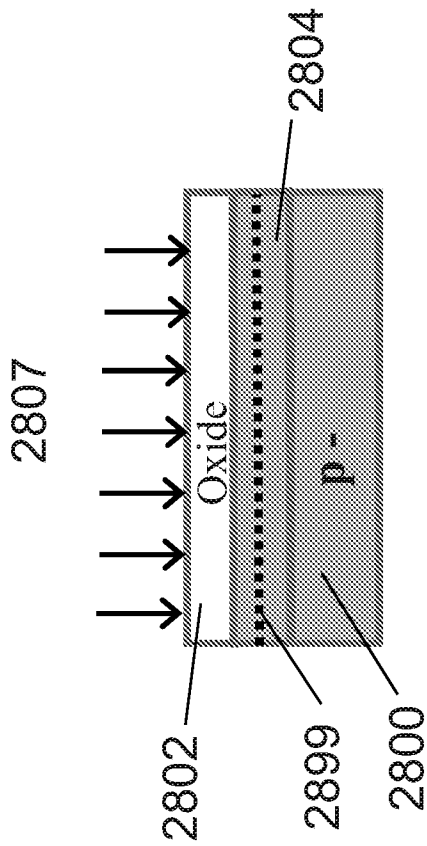


FIG. 28B



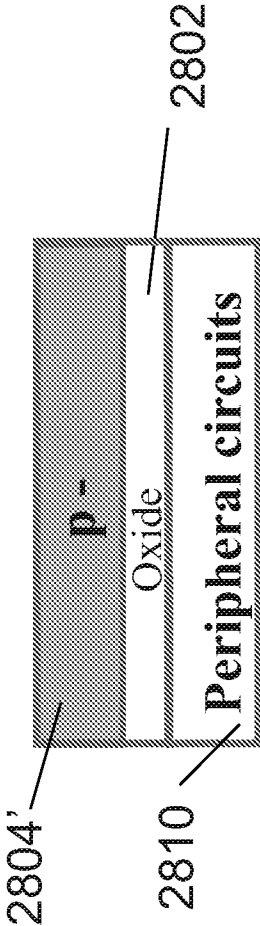


FIG. 28C

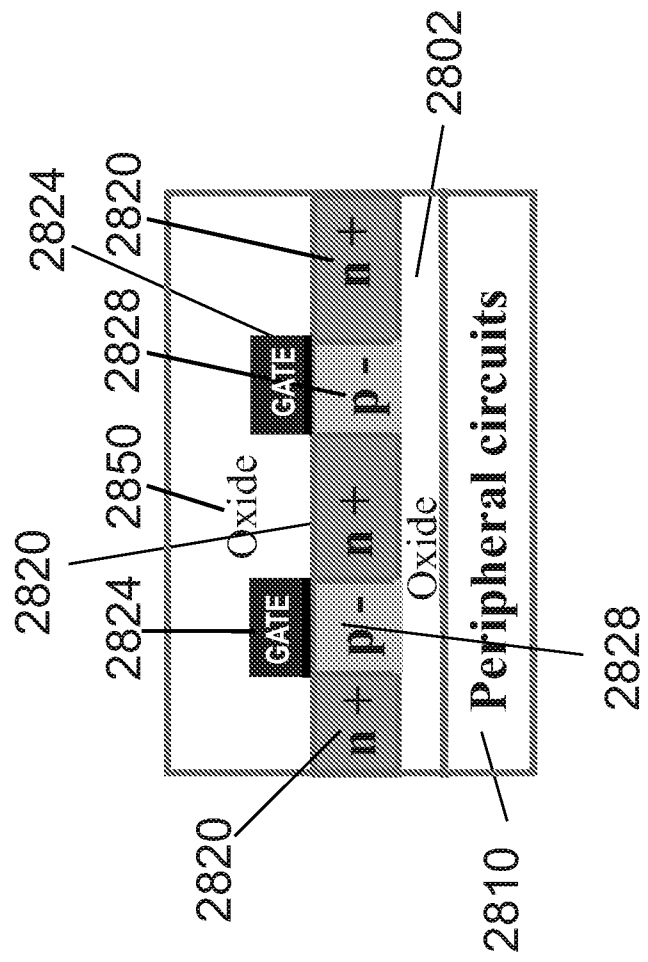


FIG. 28D

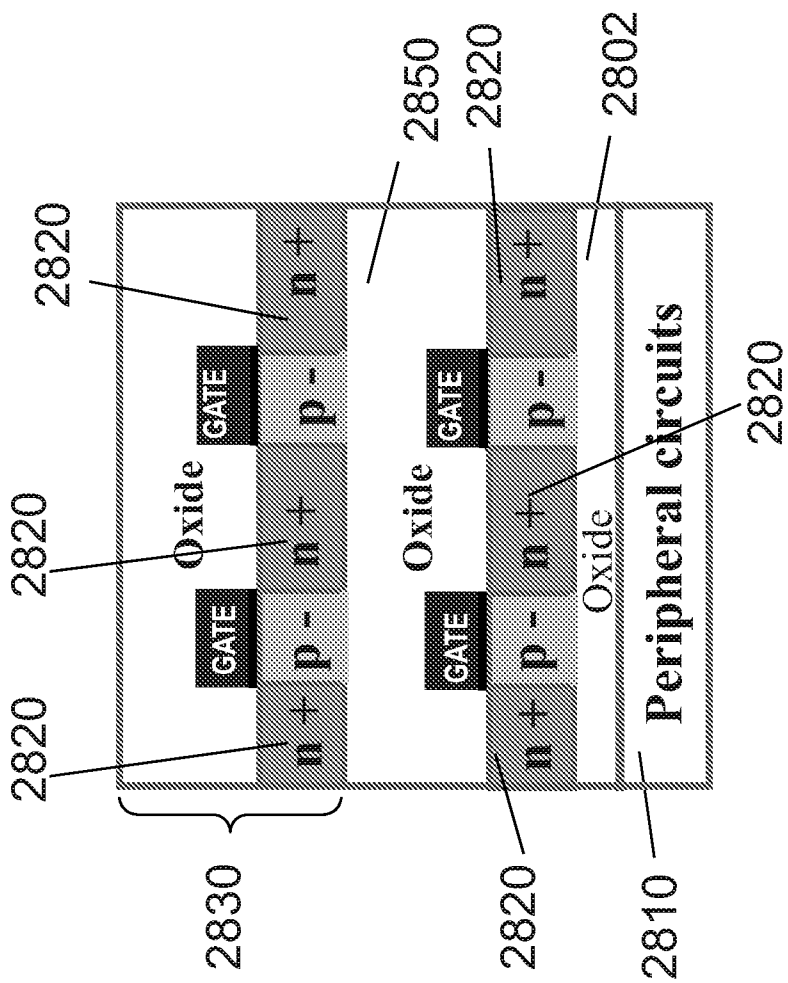


FIG. 28E

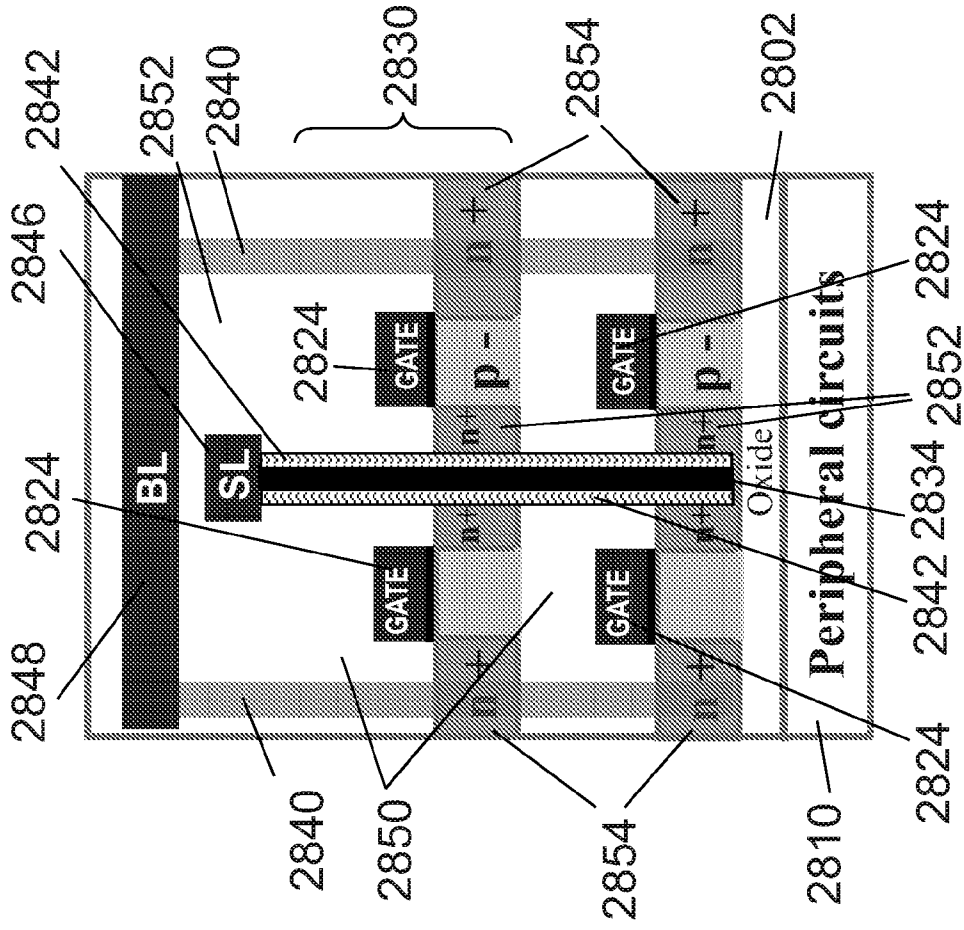


FIG. 28F

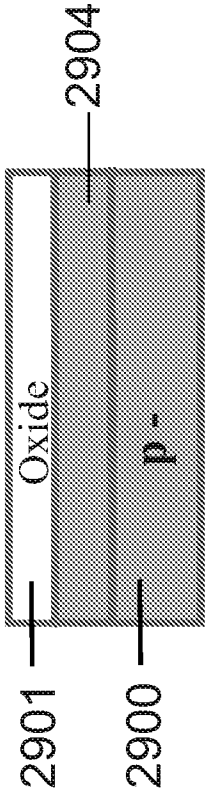


FIG. 29A

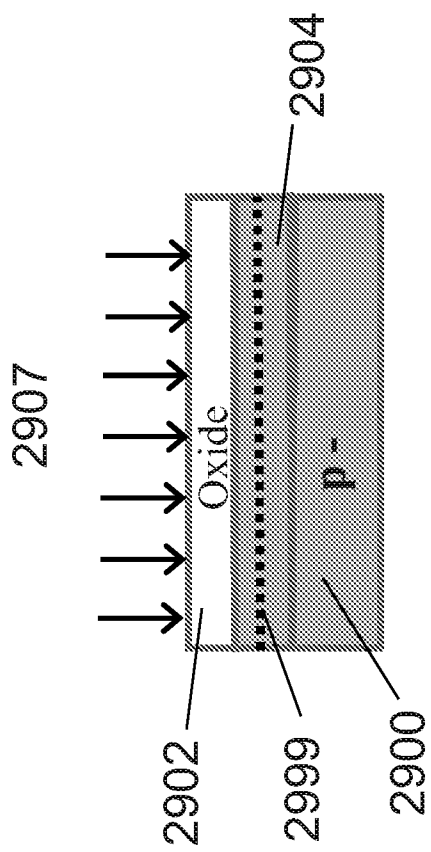


FIG. 29B

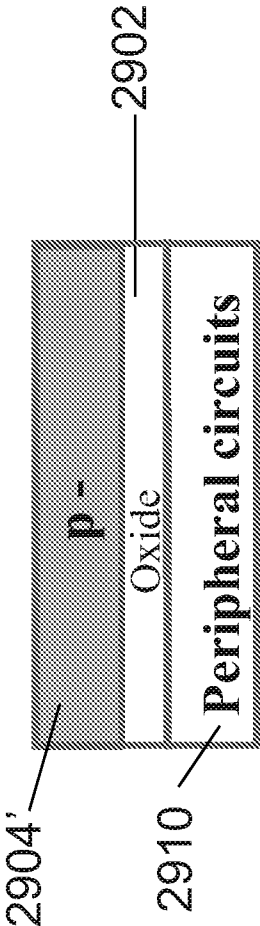


FIG. 29C

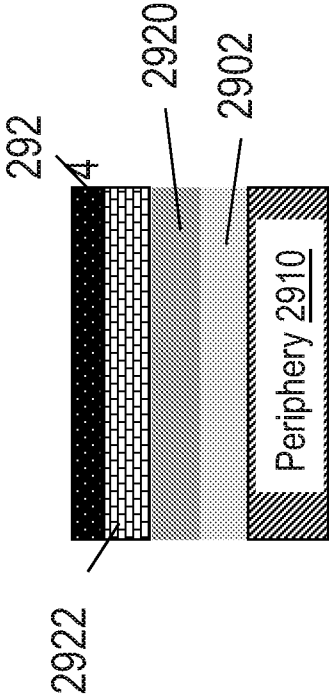


FIG. 29D



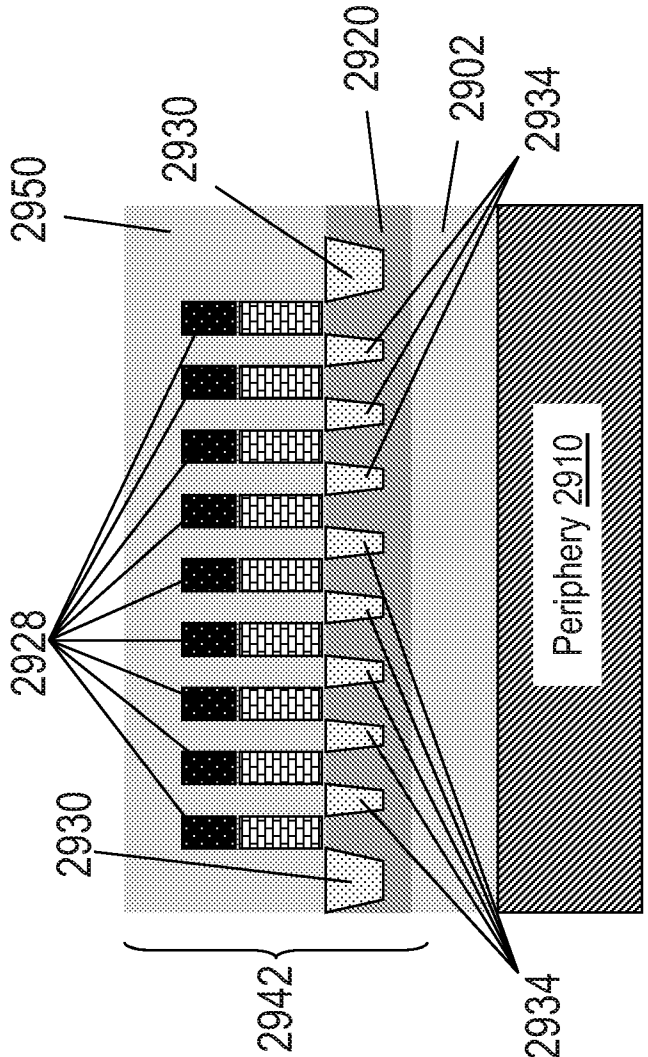


FIG. 29E

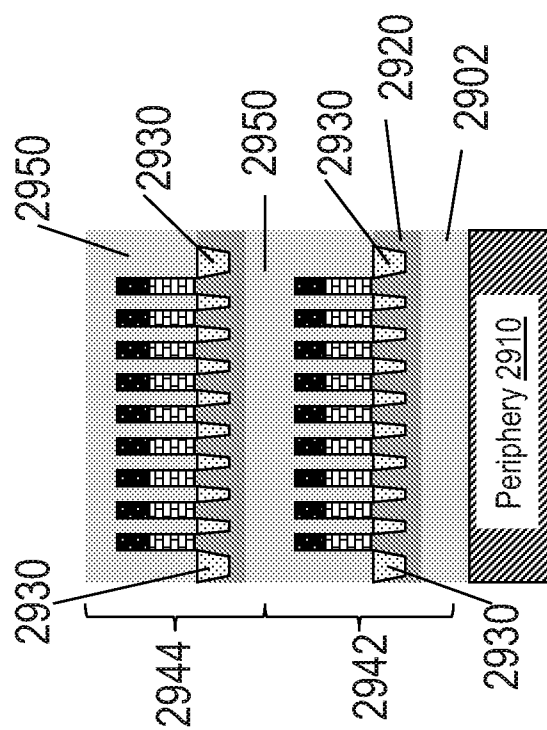


FIG. 29F

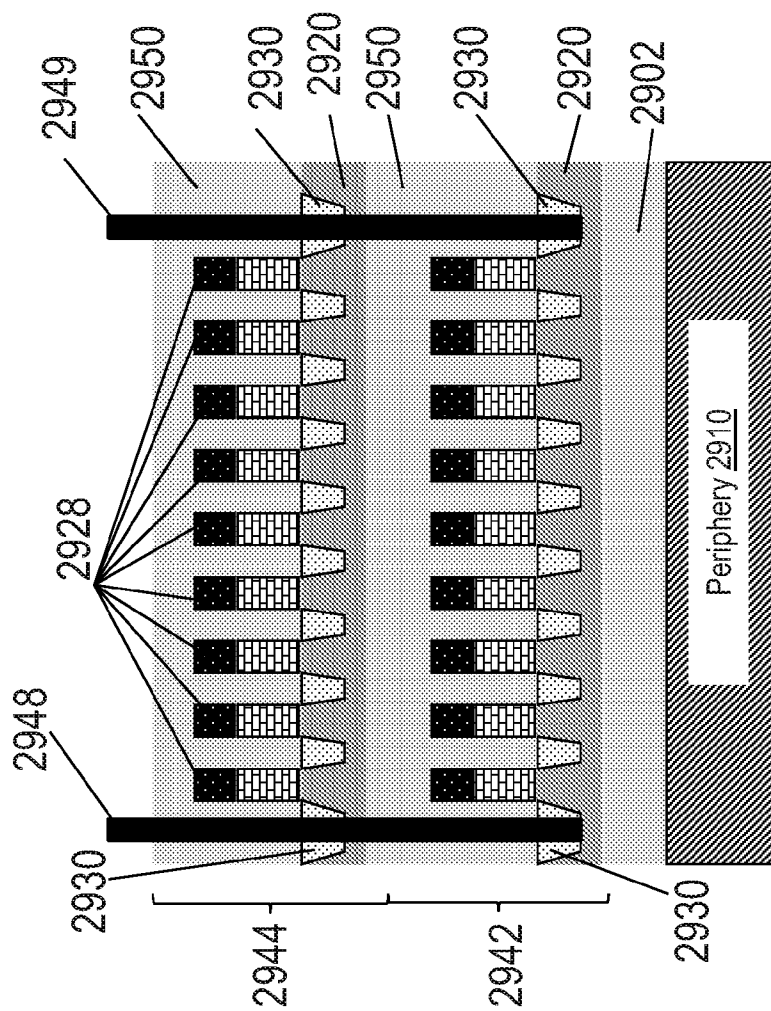


FIG. 29G

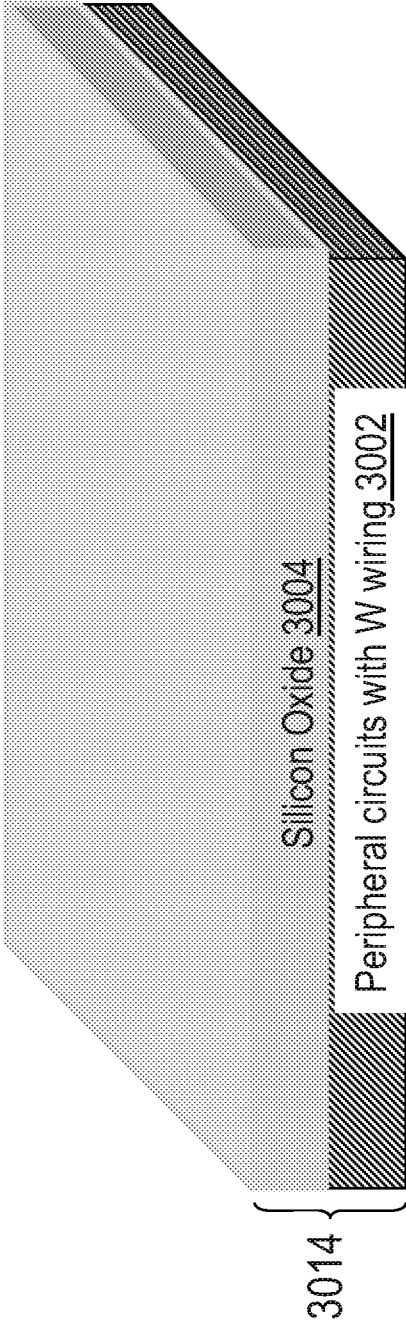


FIG. 30A

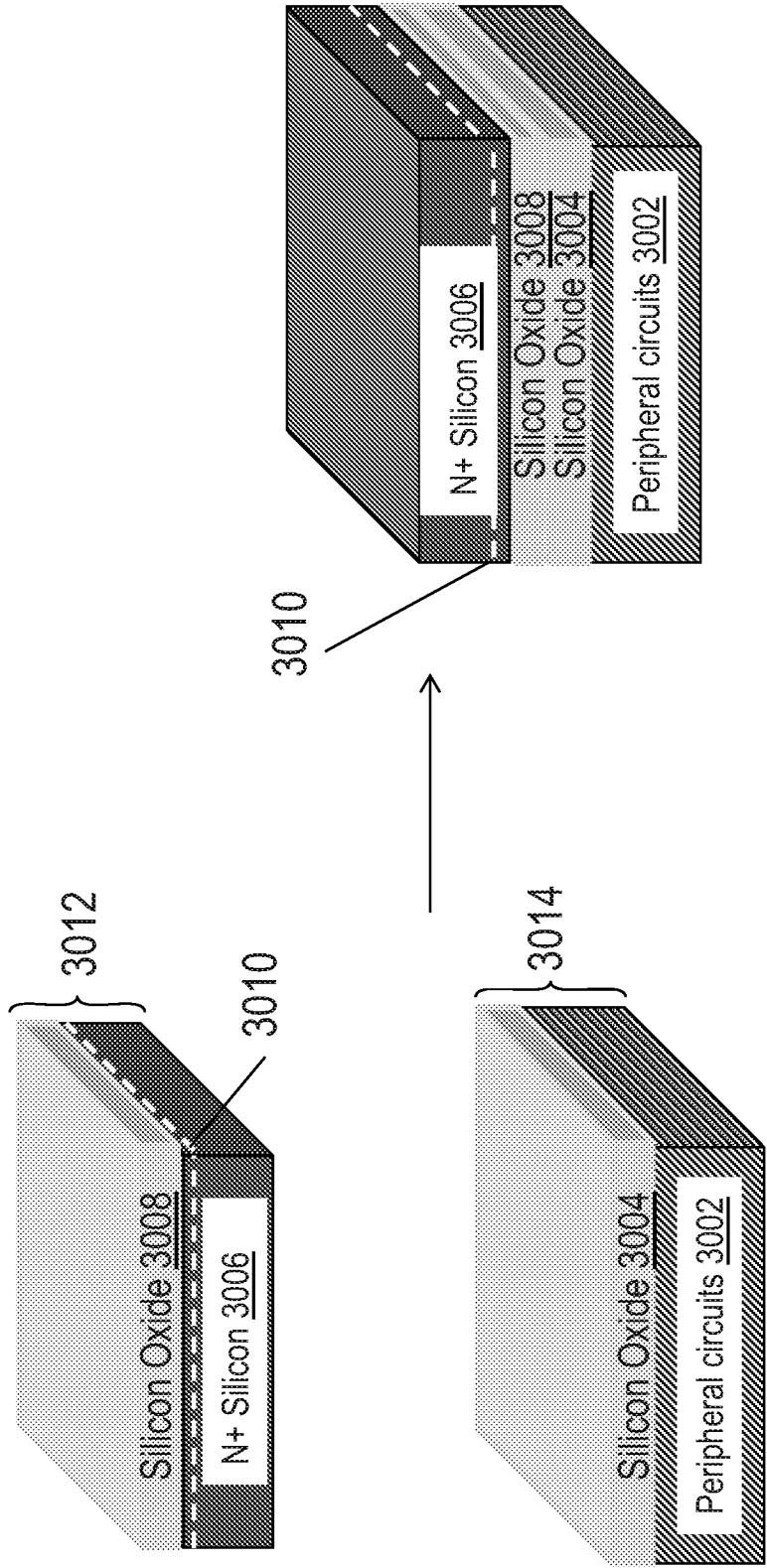


FIG. 30B

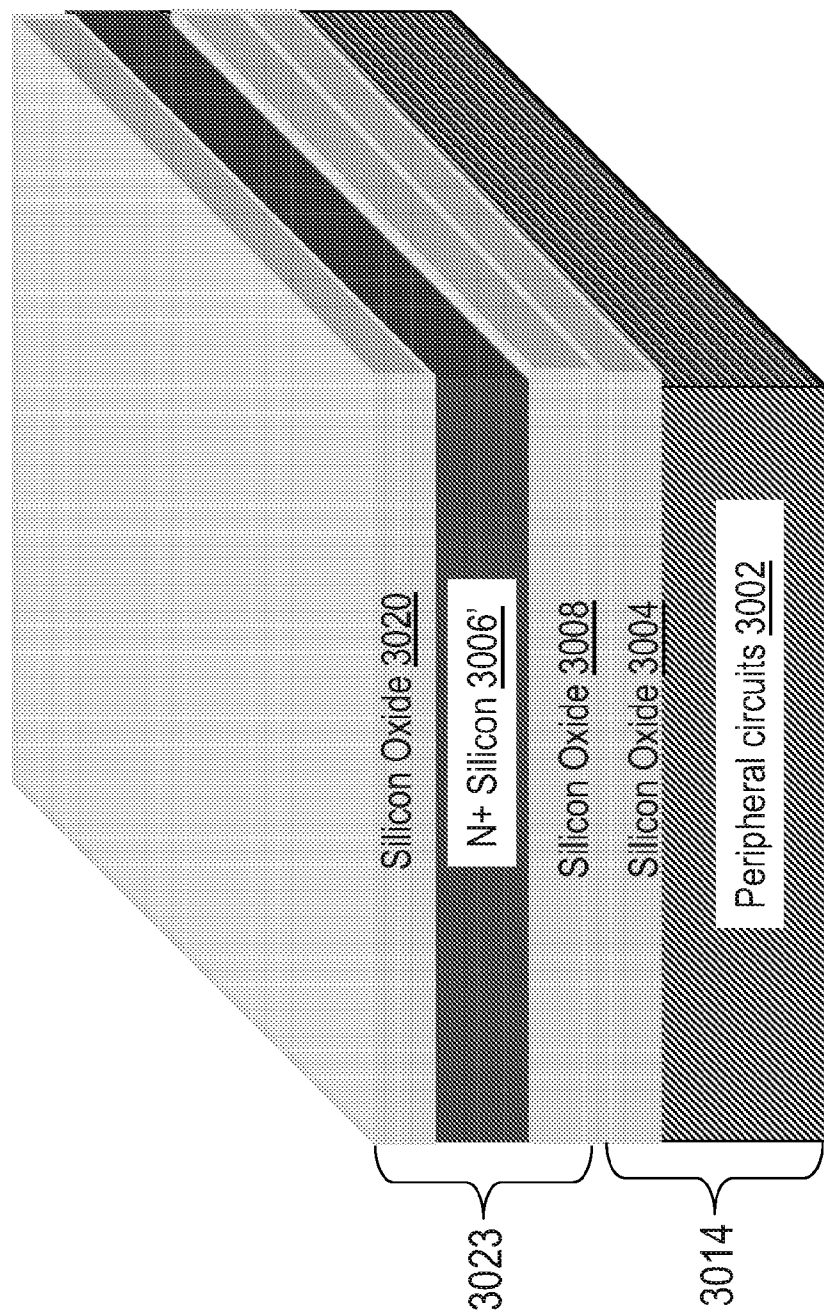


FIG. 30C

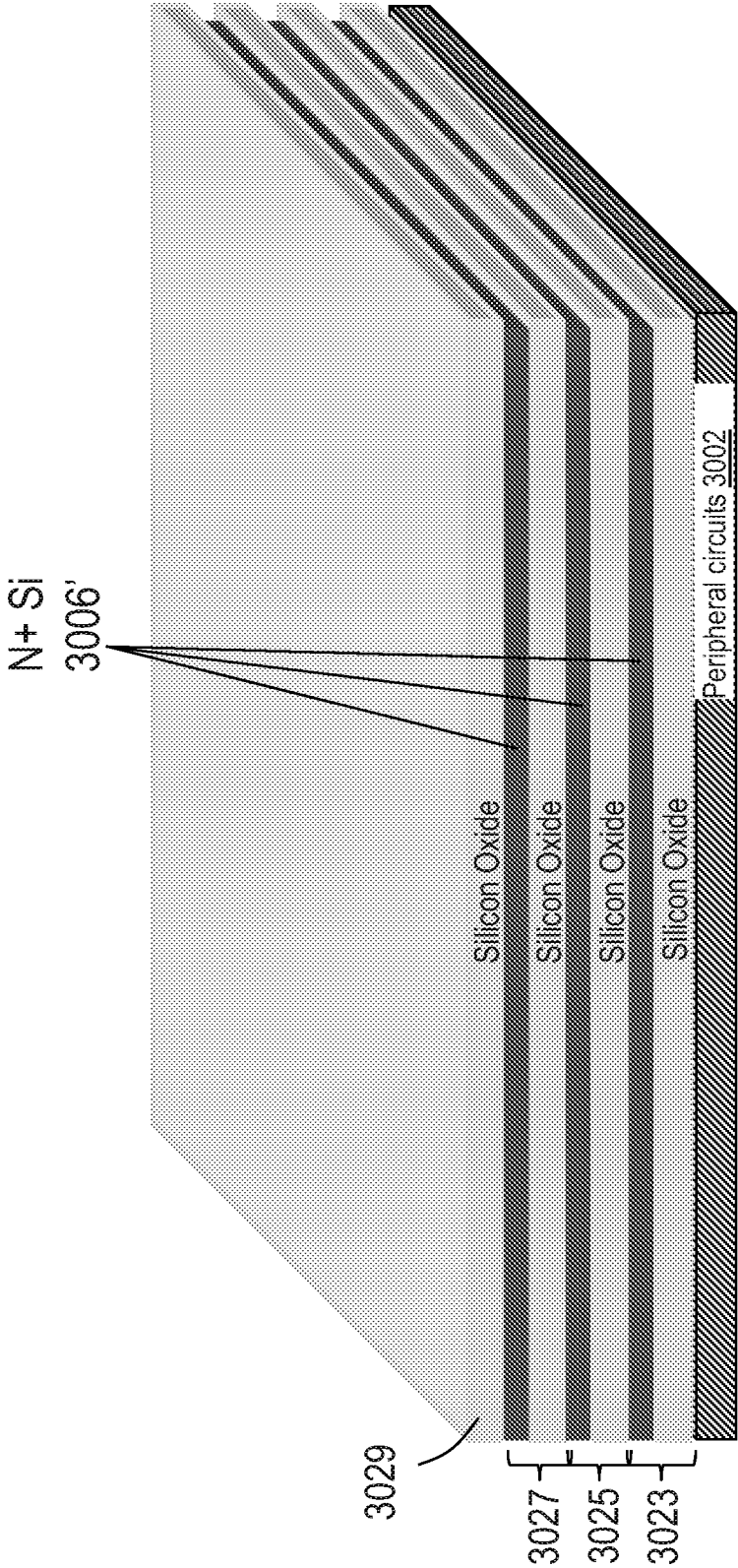


FIG. 30D

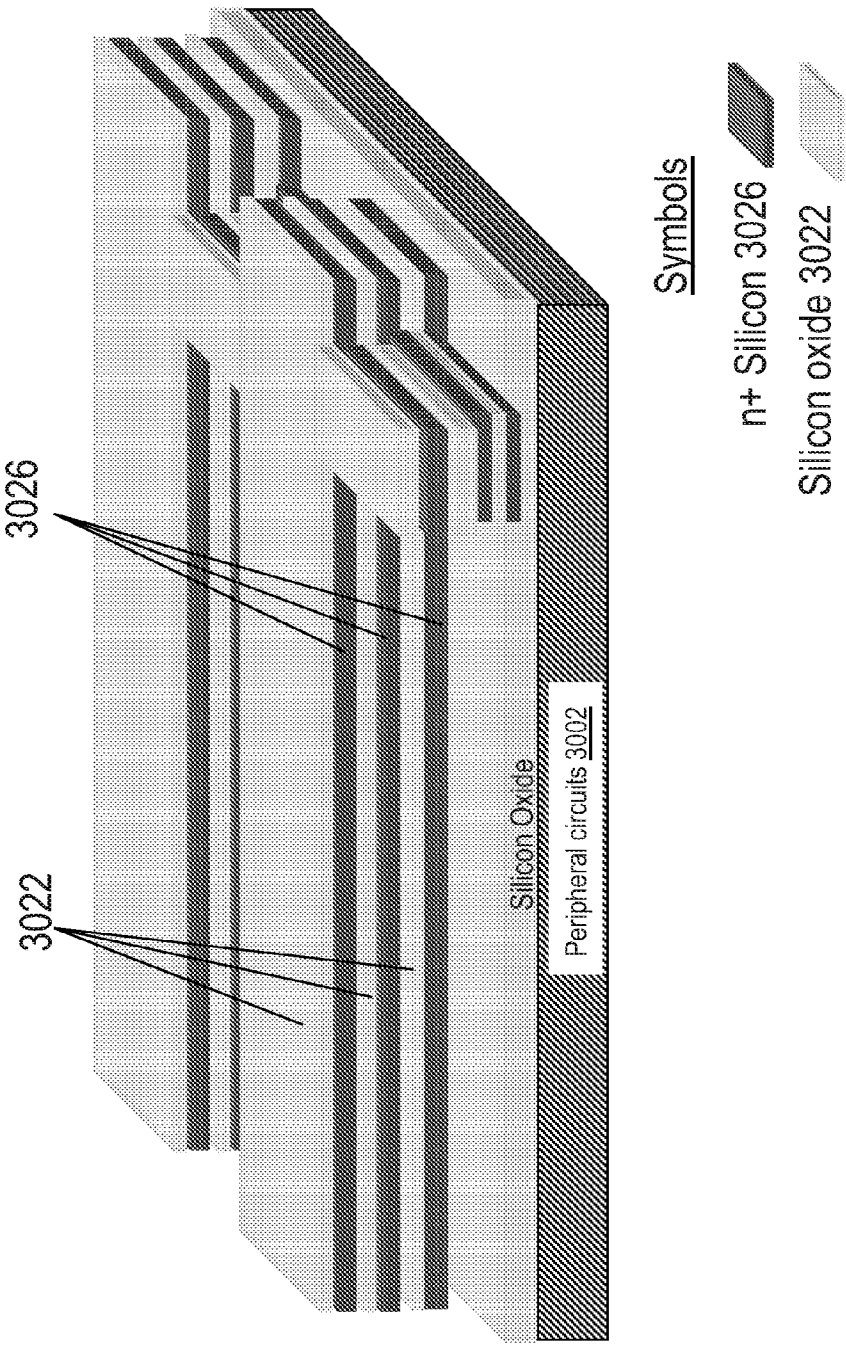


FIG. 30E



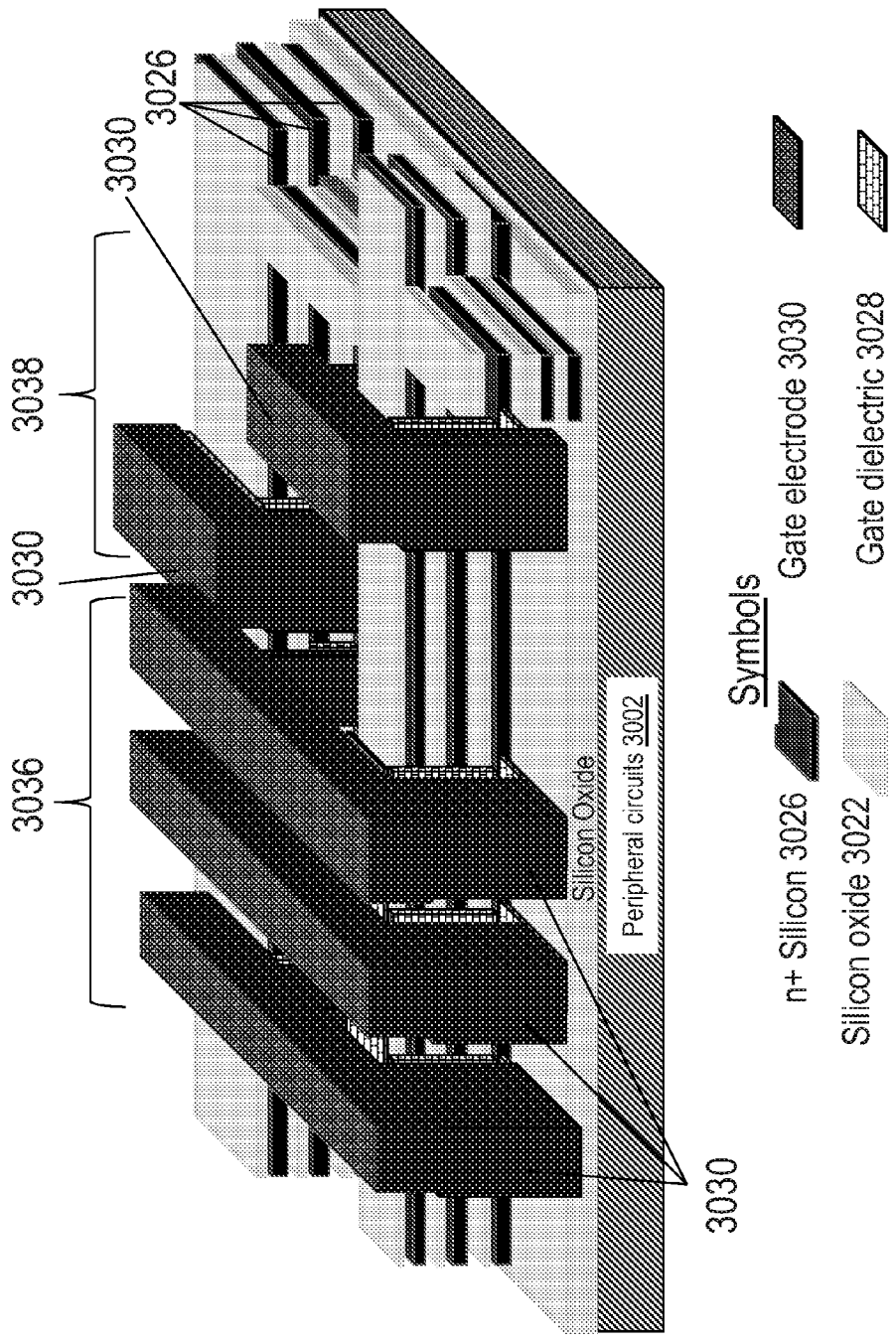


FIG. 30F

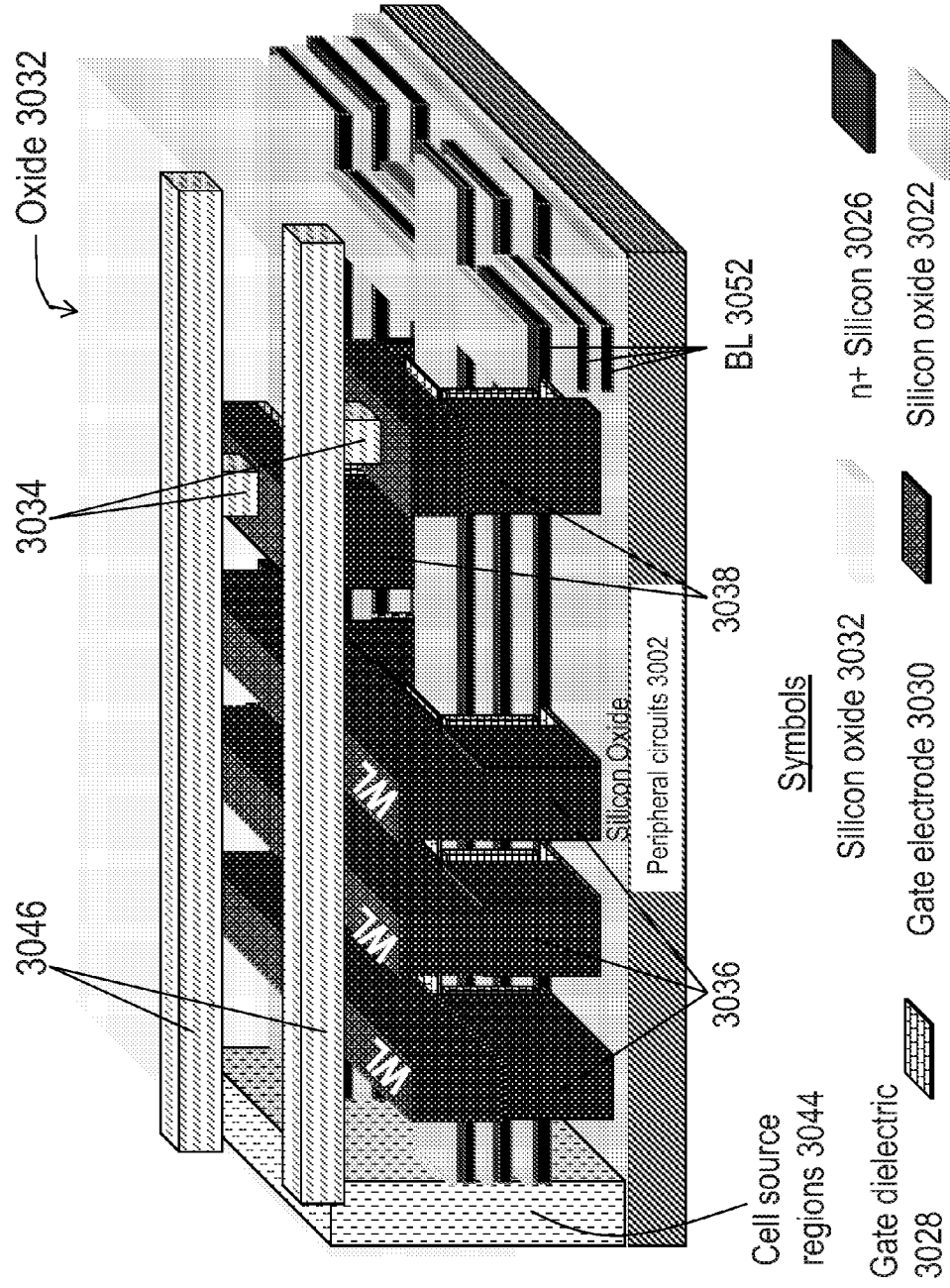


FIG. 30G

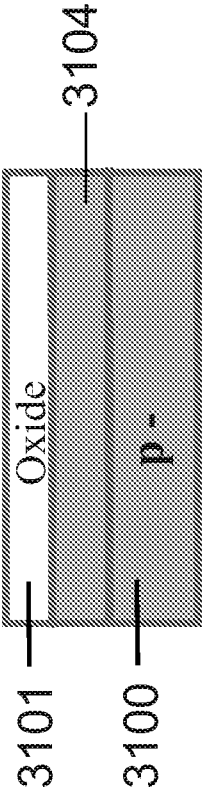


FIG. 31A

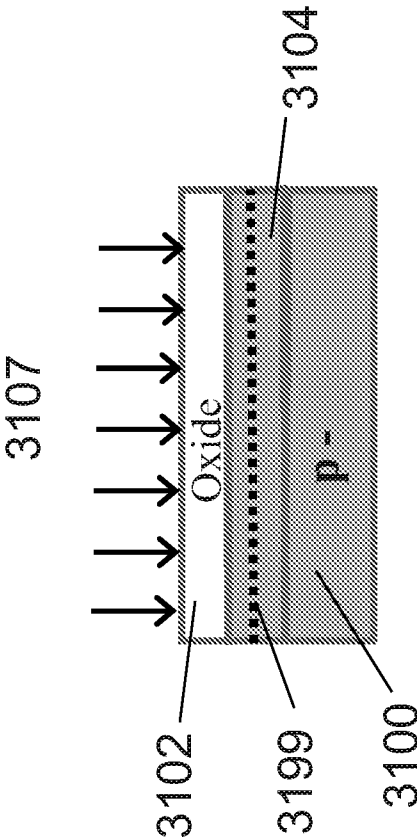


FIG. 31B

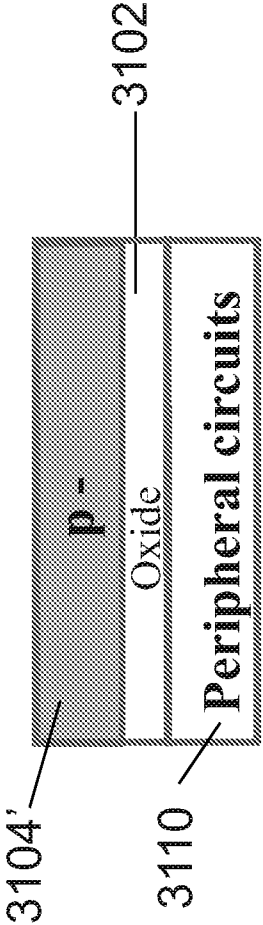


FIG. 31C

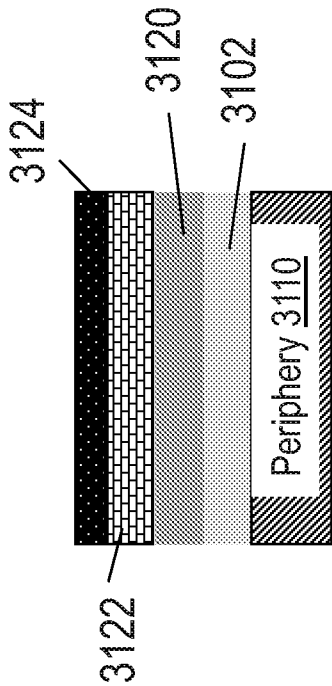


FIG. 31D

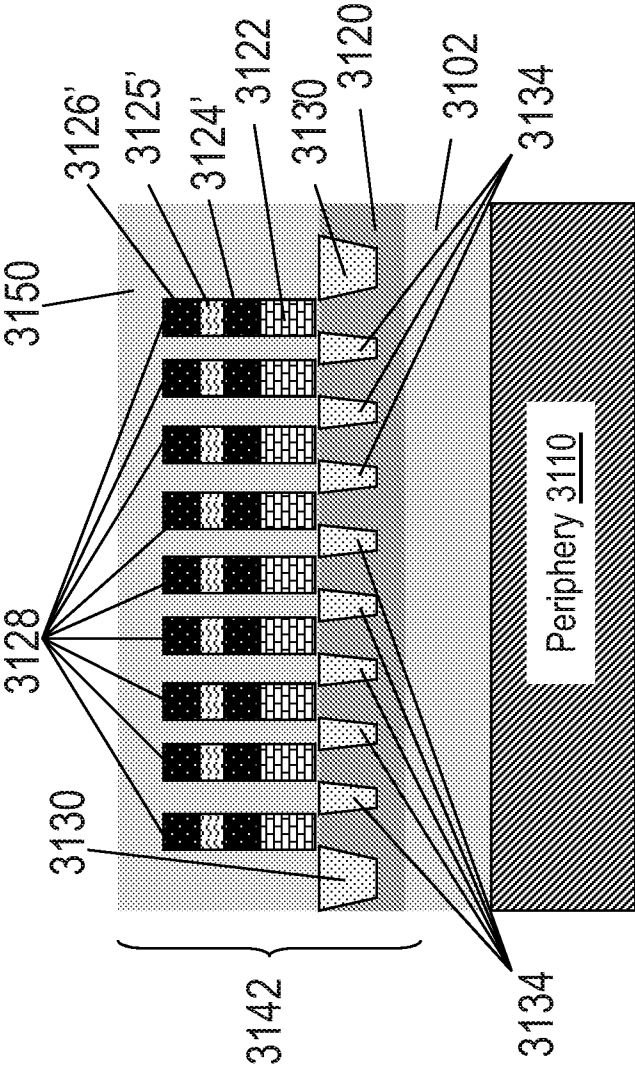


FIG. 31E

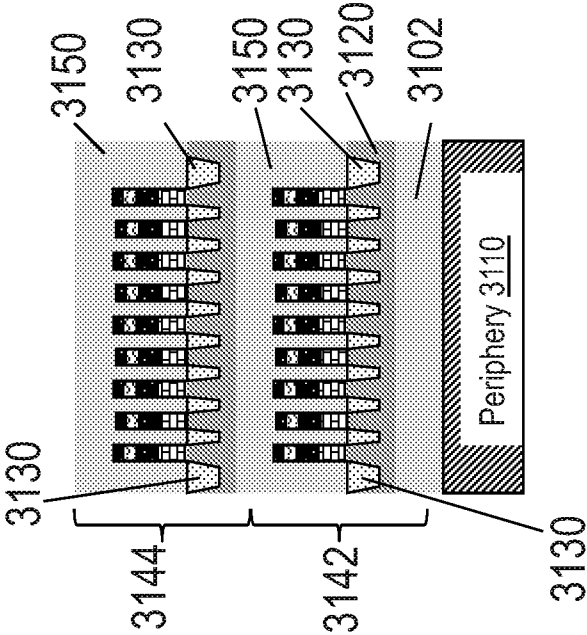


FIG. 31F



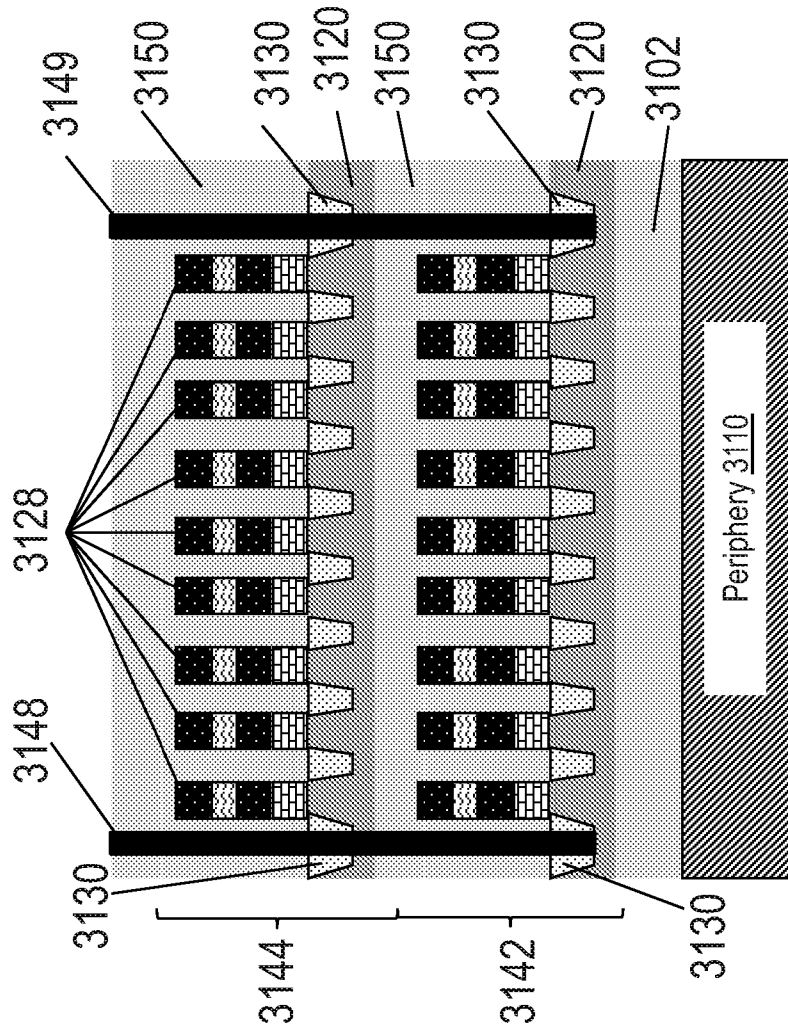


FIG. 31G

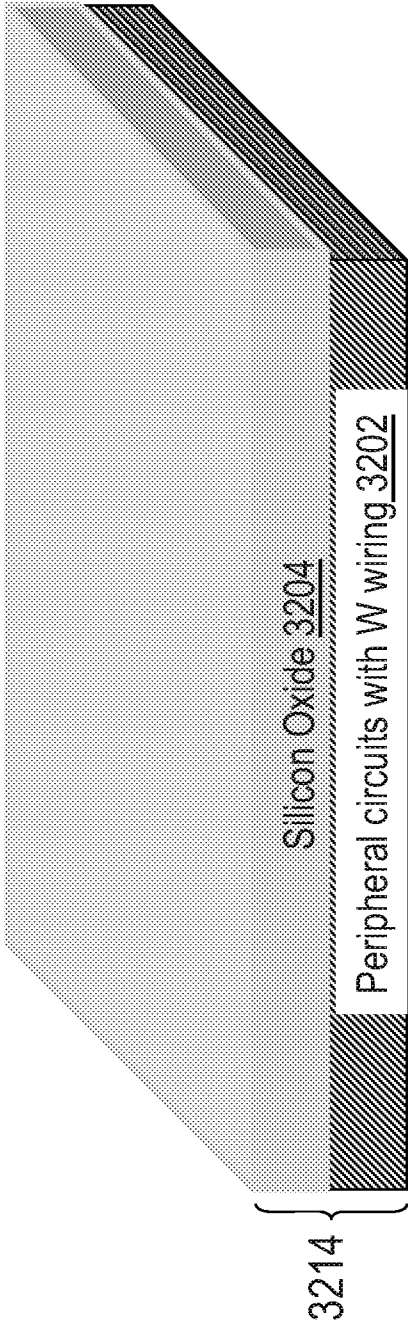


FIG. 32A

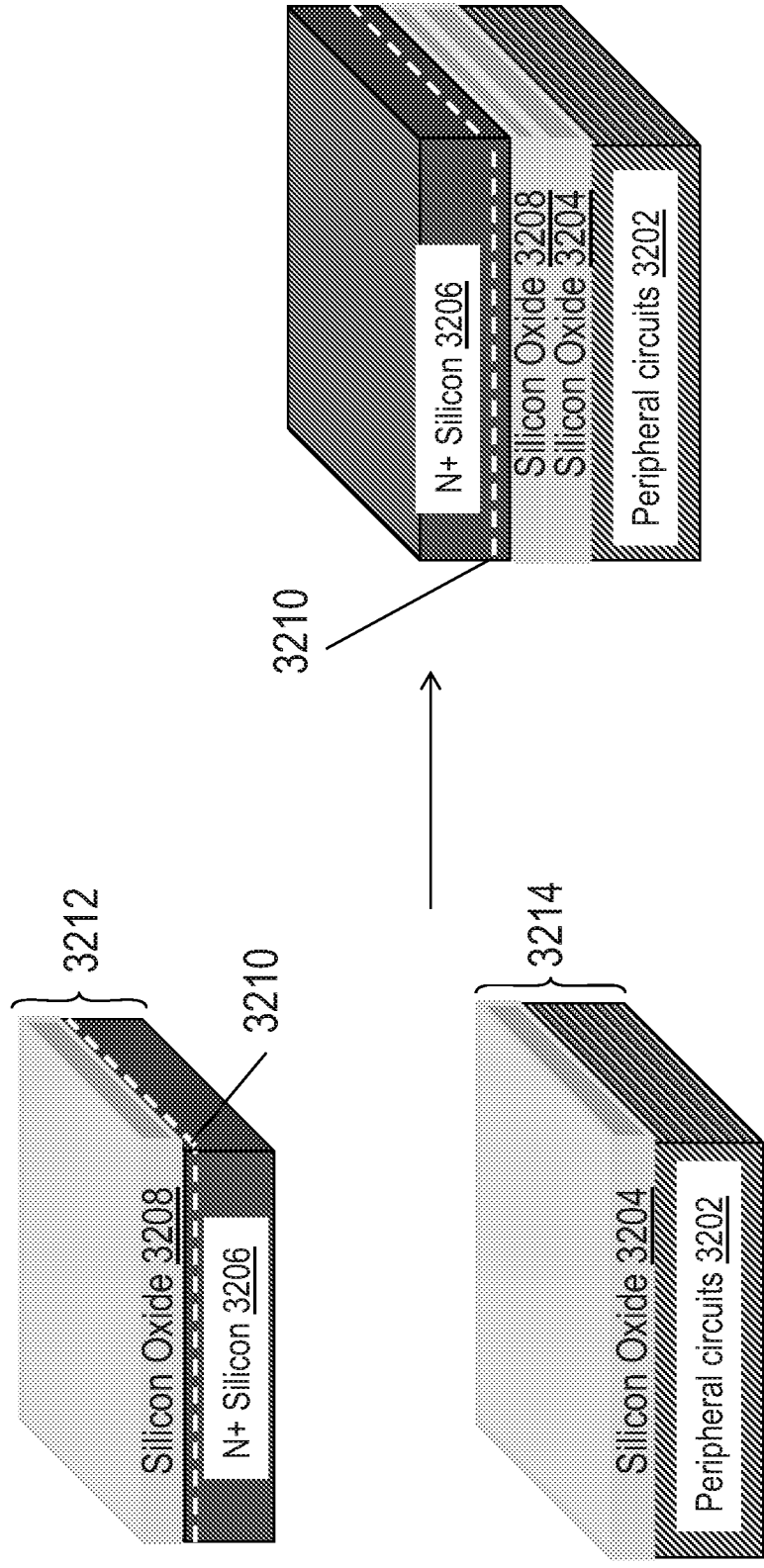


FIG. 32B

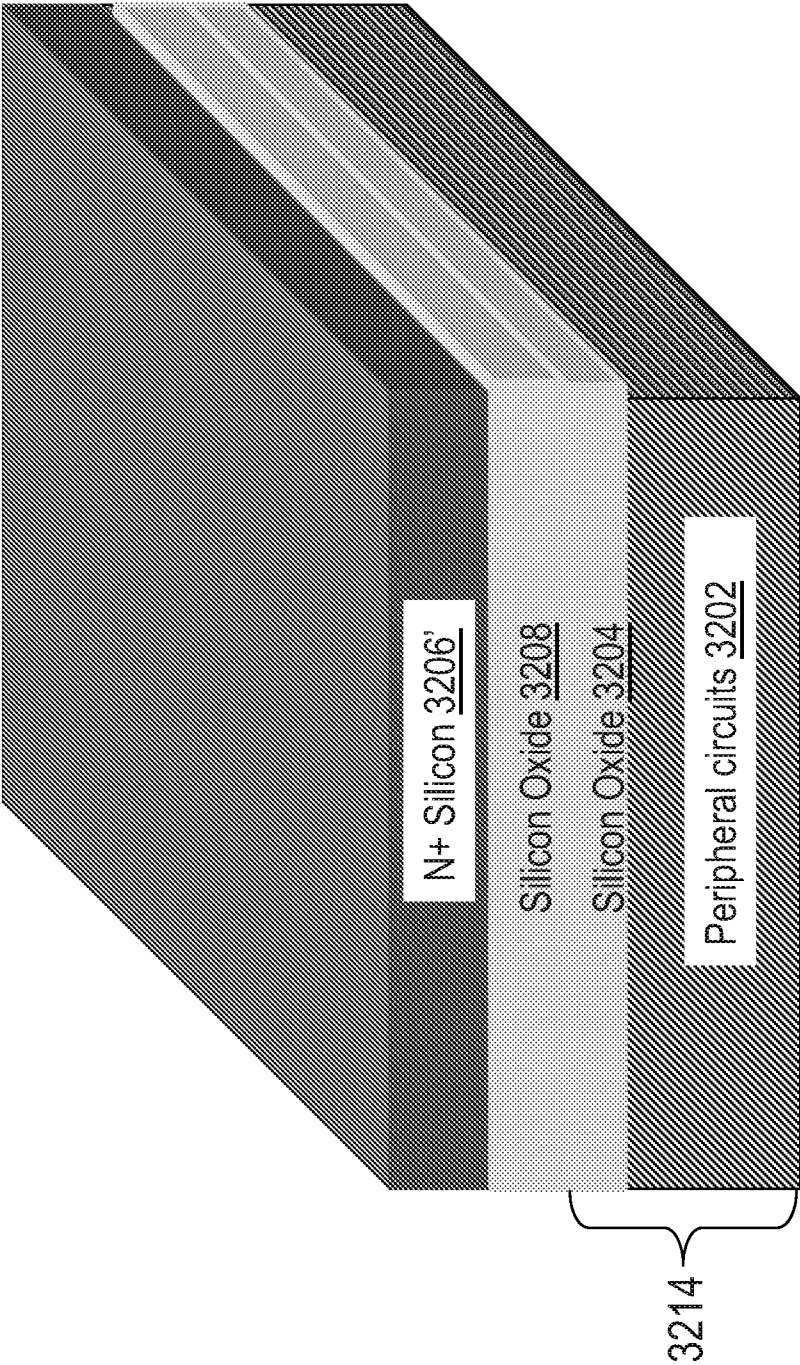


FIG. 32C

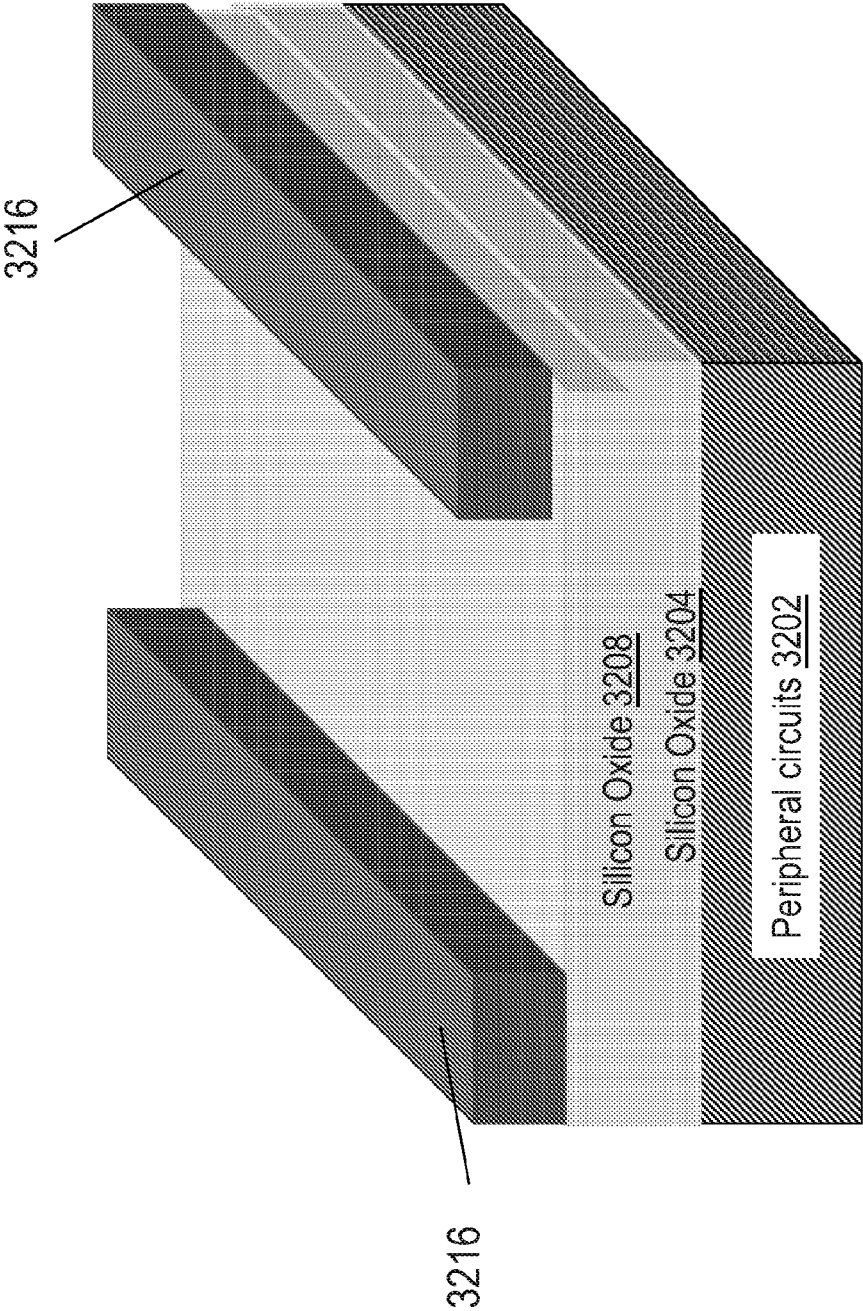


FIG. 32D

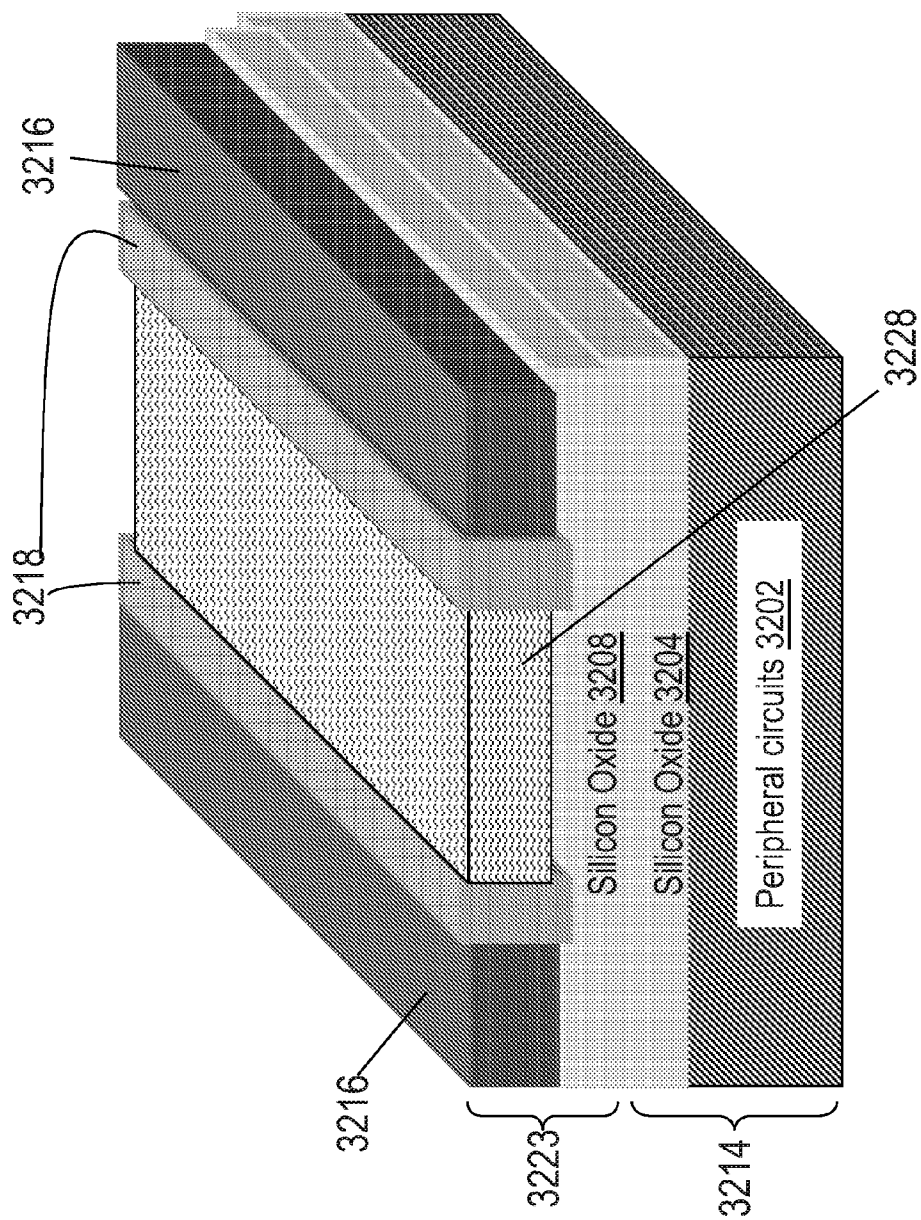


FIG. 32E

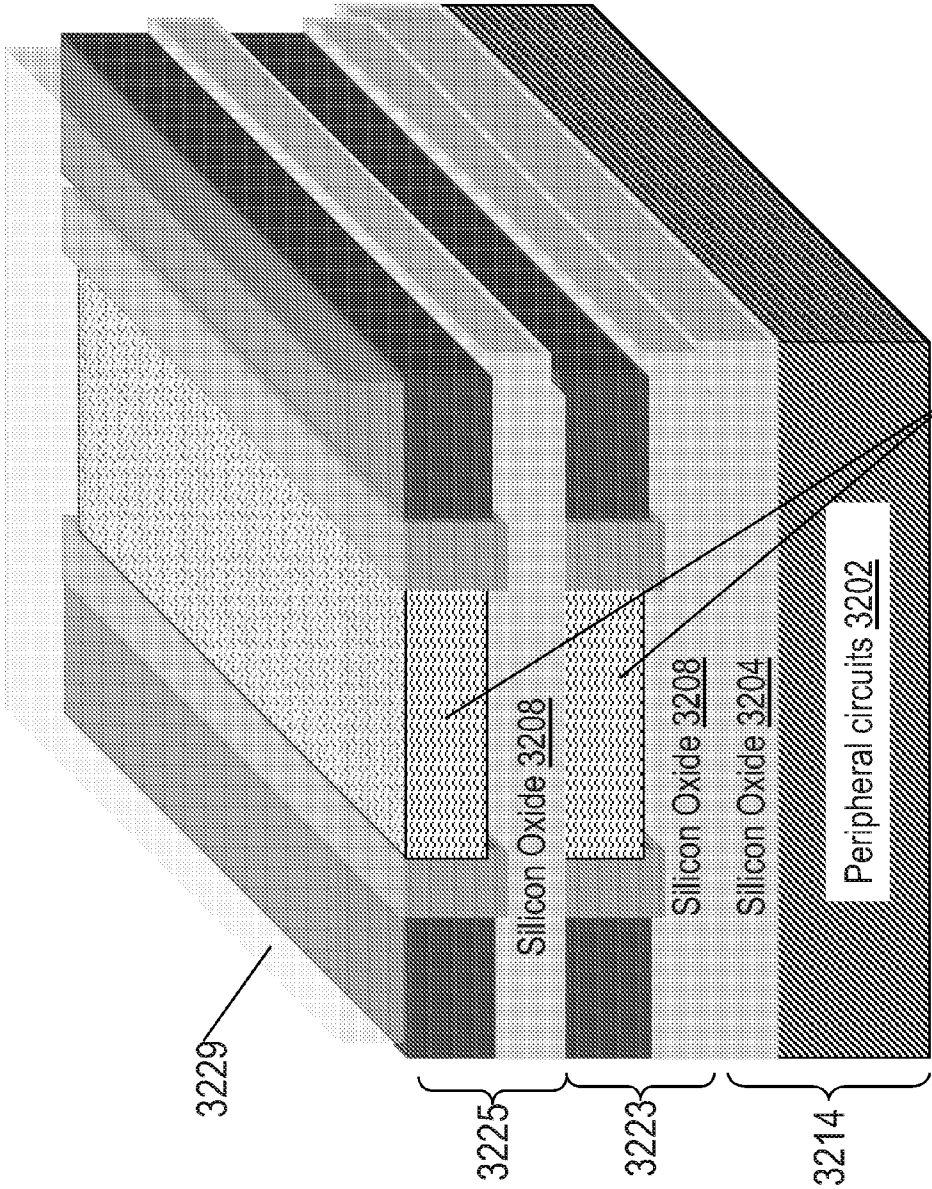


FIG. 32F 3228

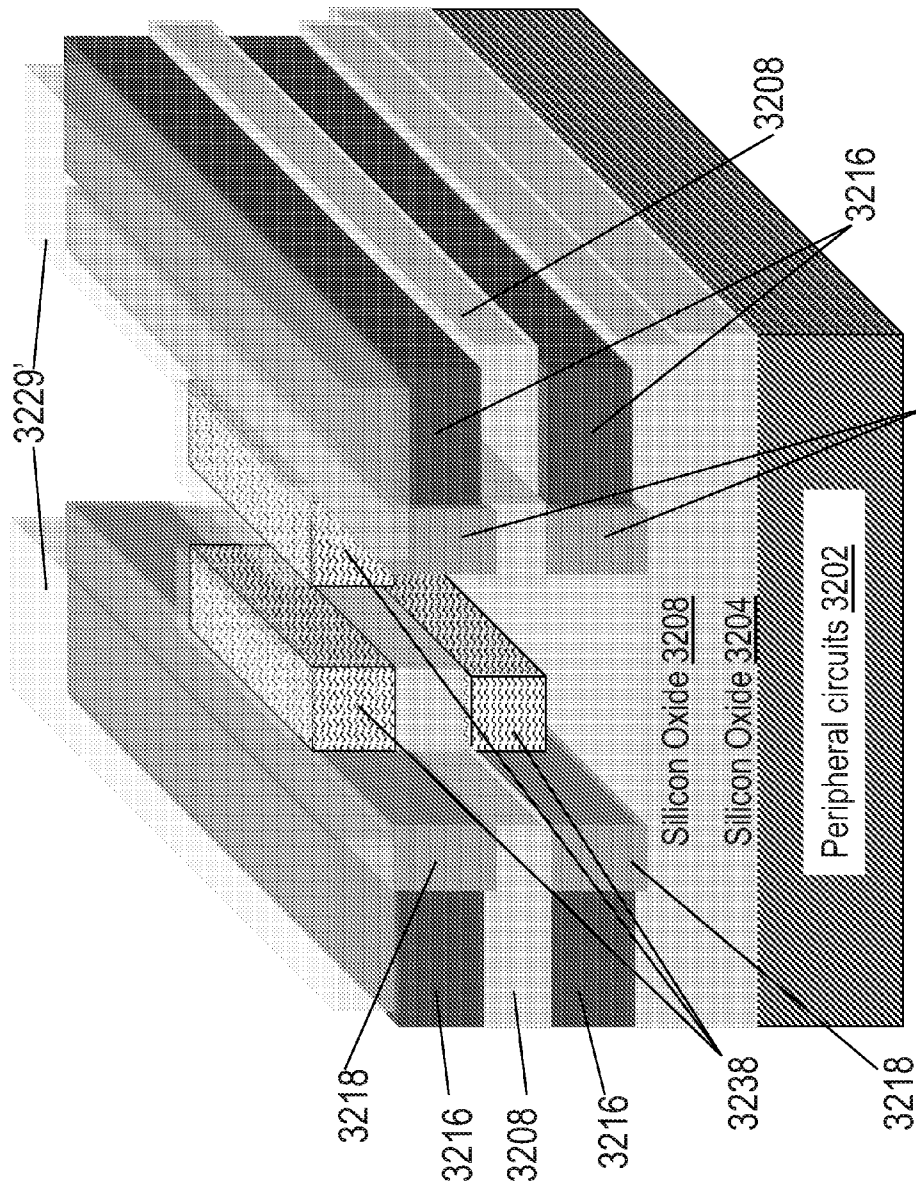


FIG. 32G



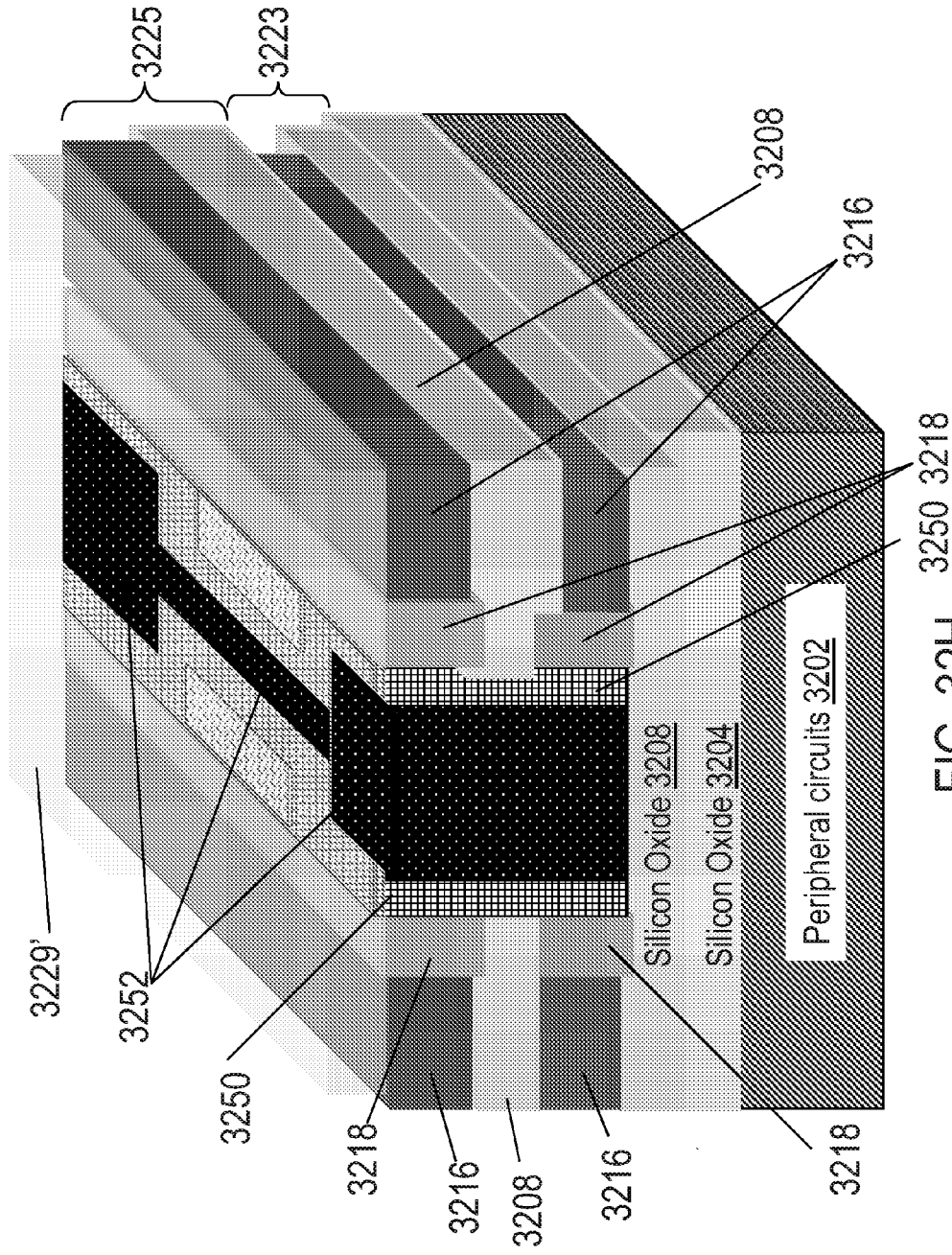
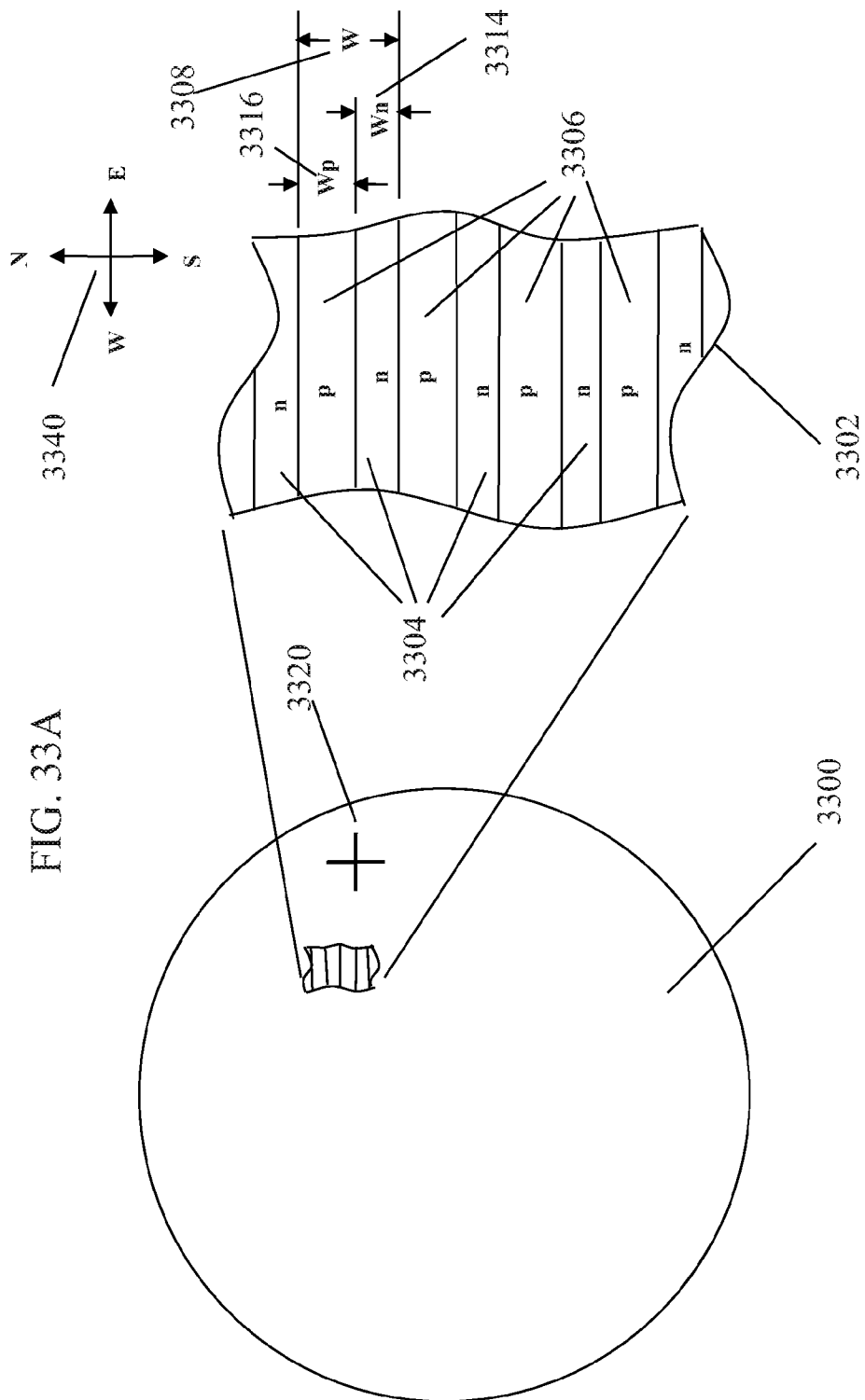


FIG. 32H



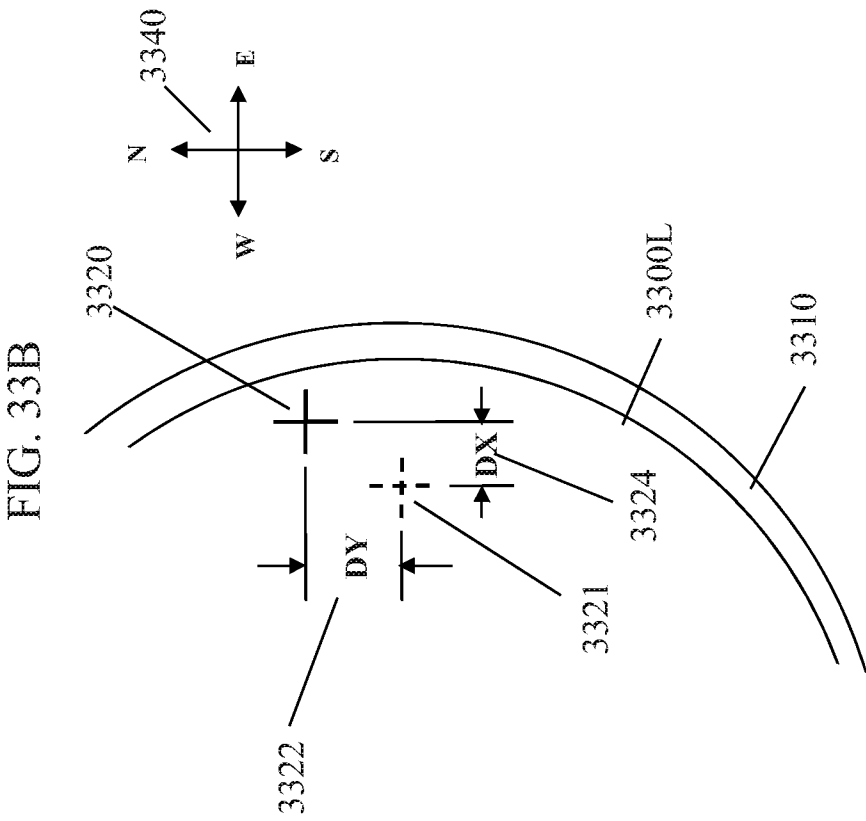


FIG. 33C

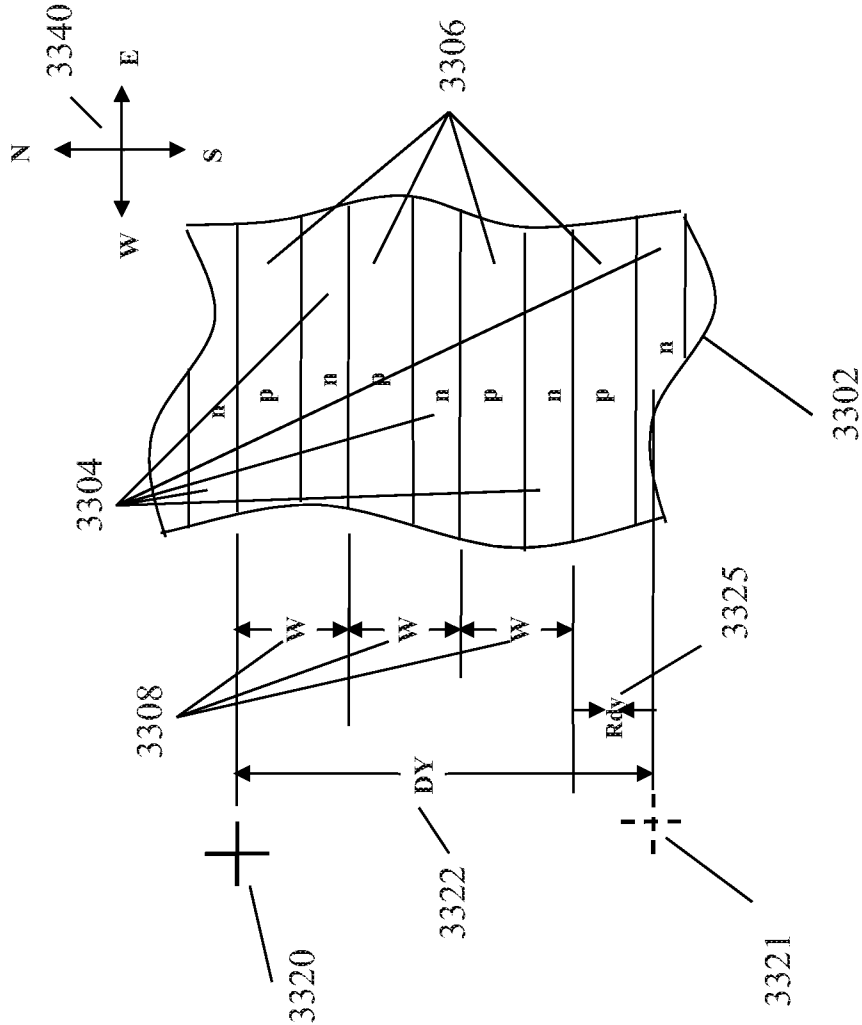
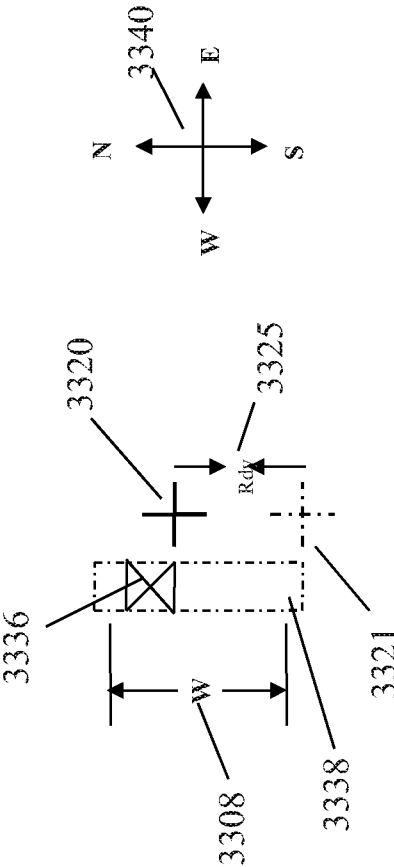


FIG. 33D



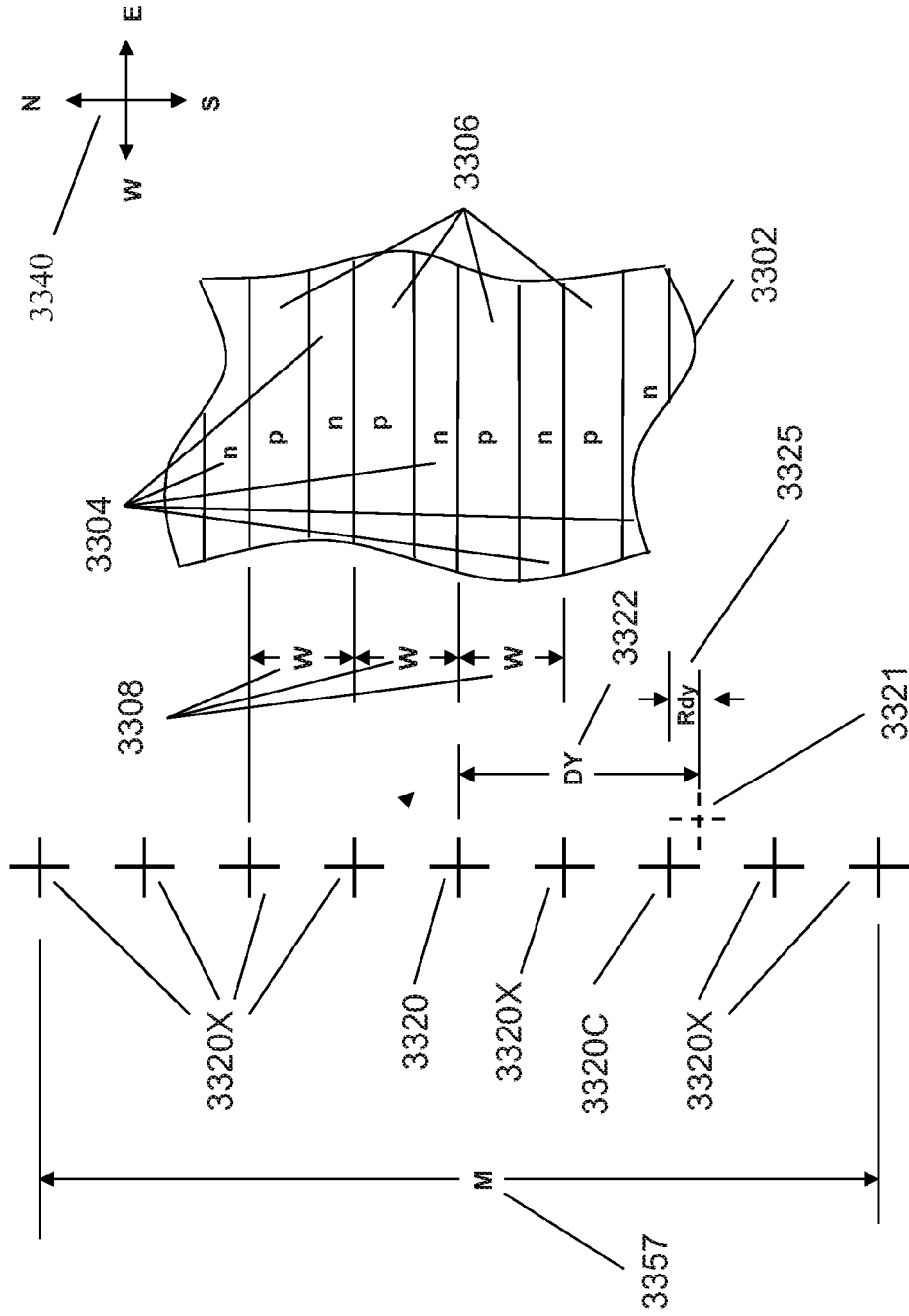
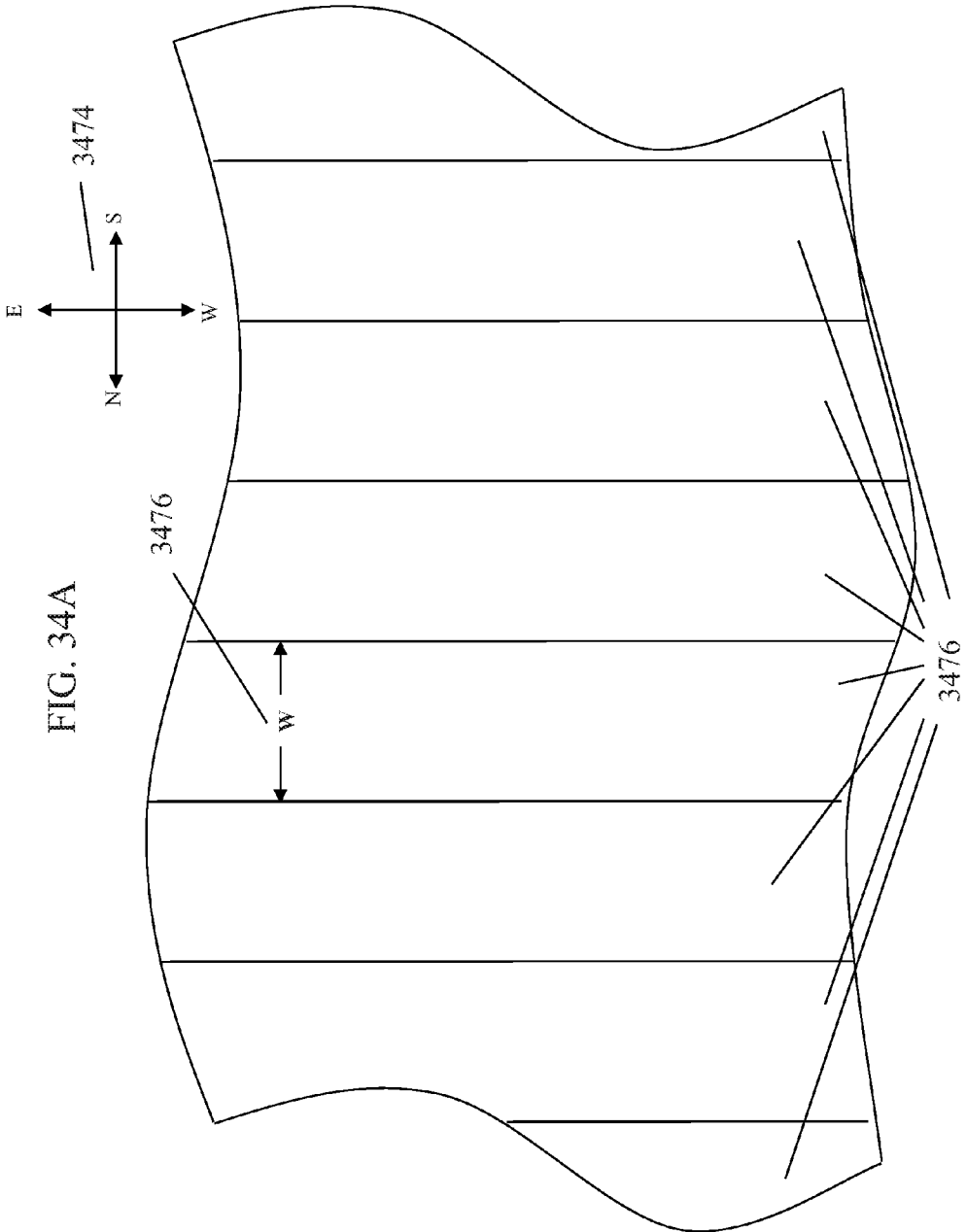


FIG. 33E



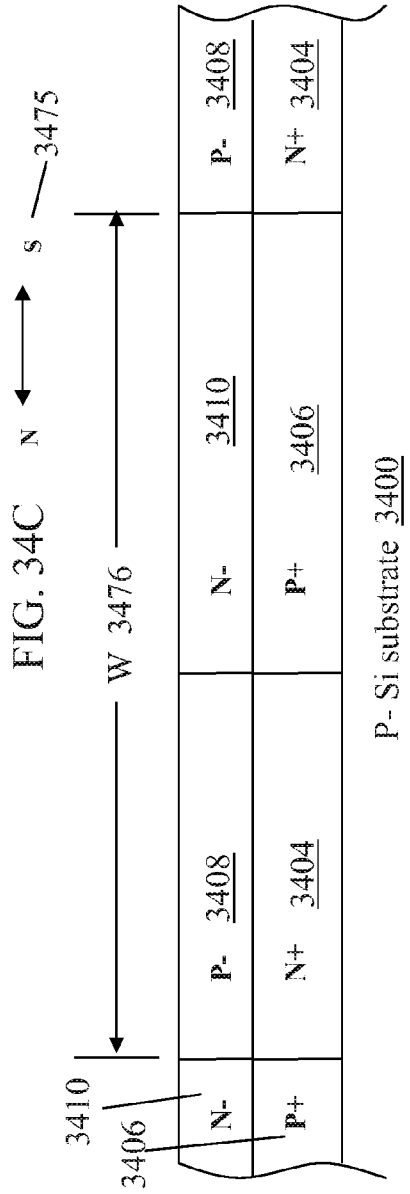
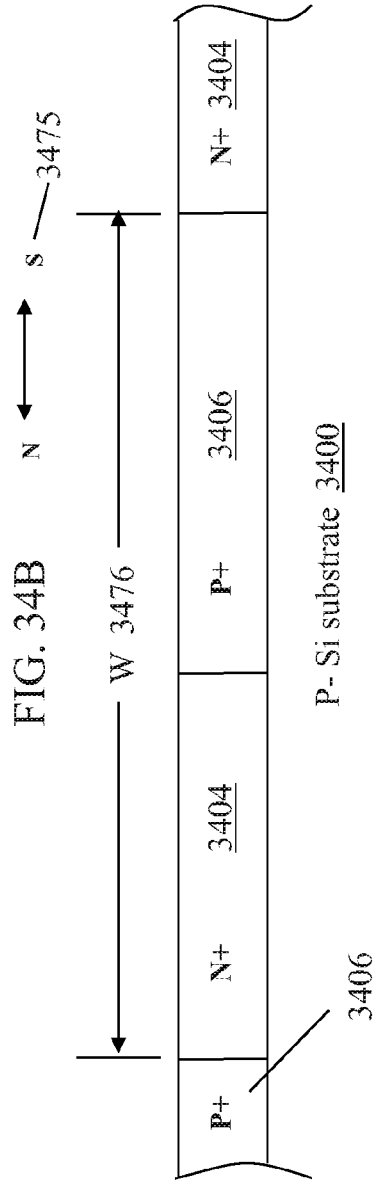




FIG. 34D

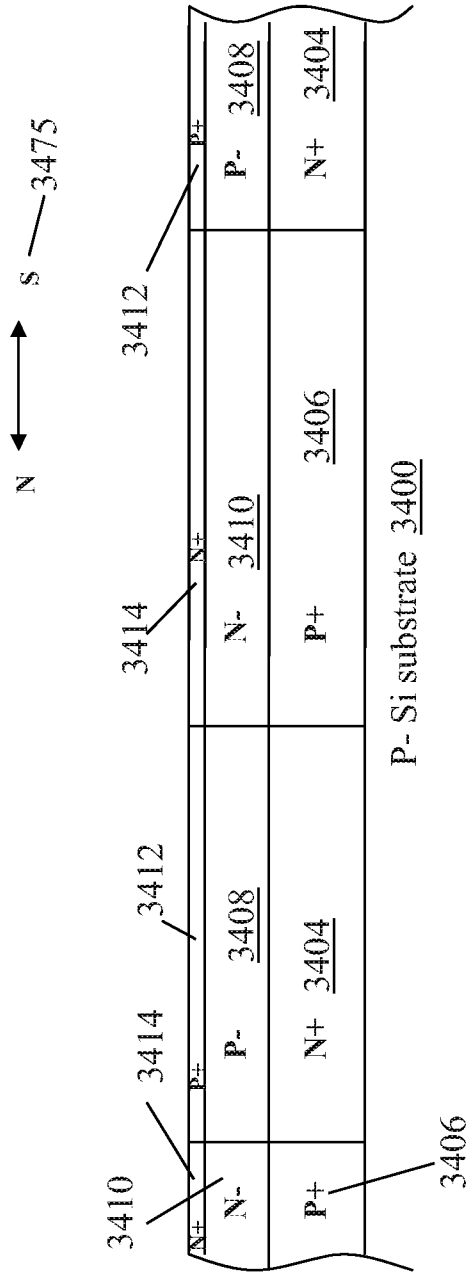


FIG. 34E

N ← → S 3475

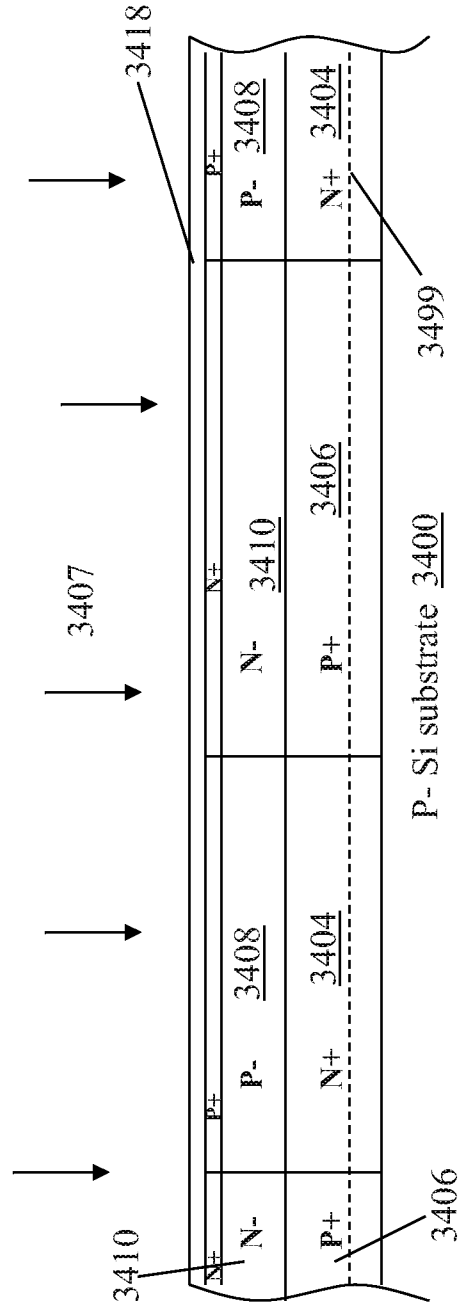


FIG. 34F

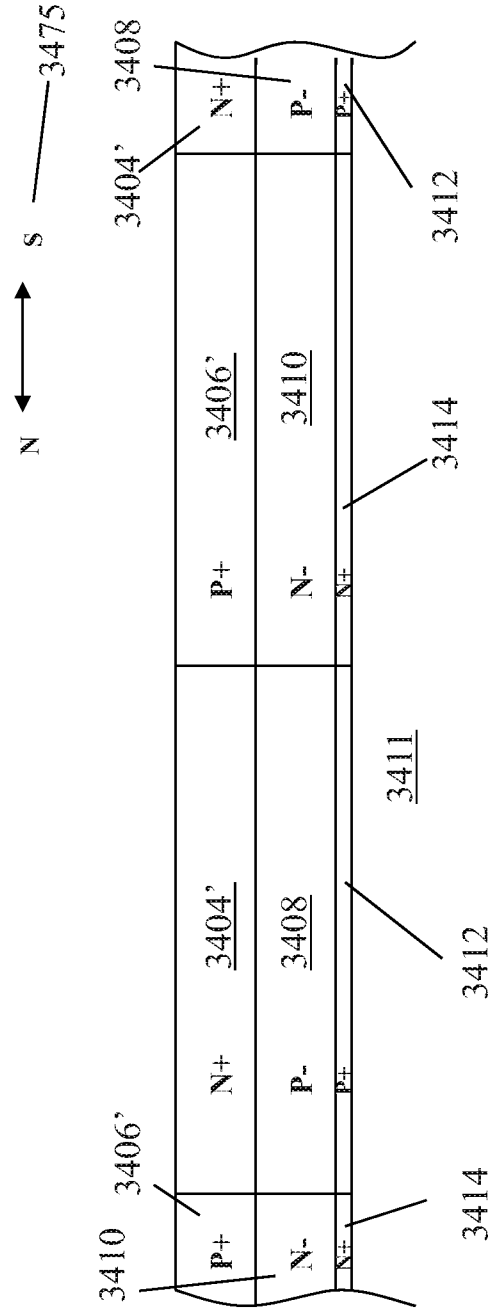


FIG. 34G

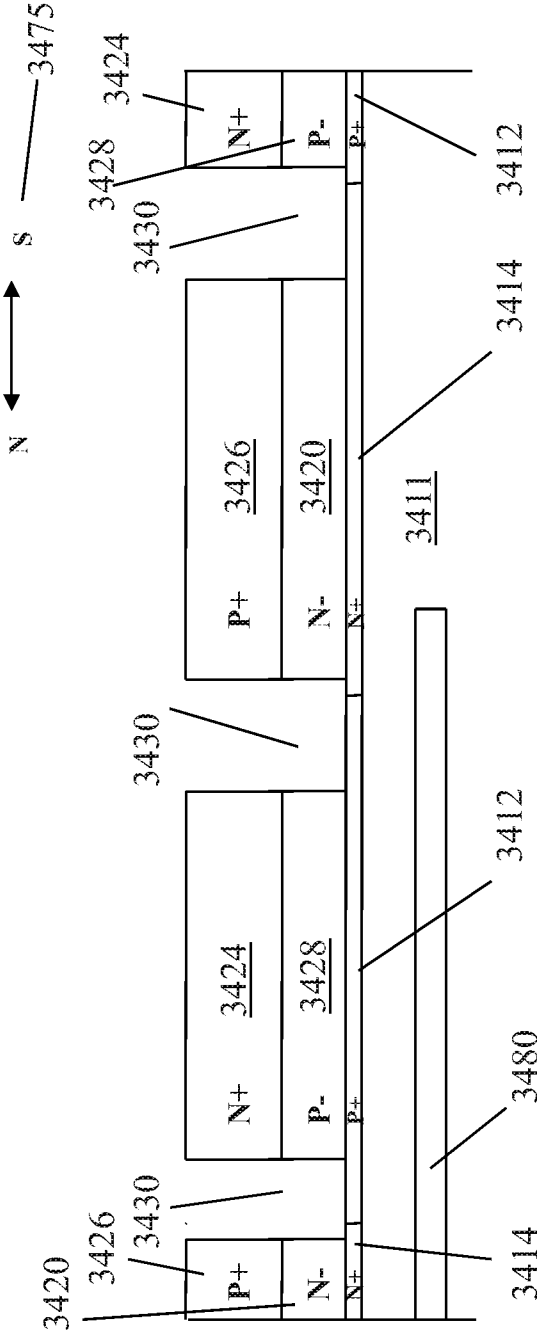


FIG. 34H

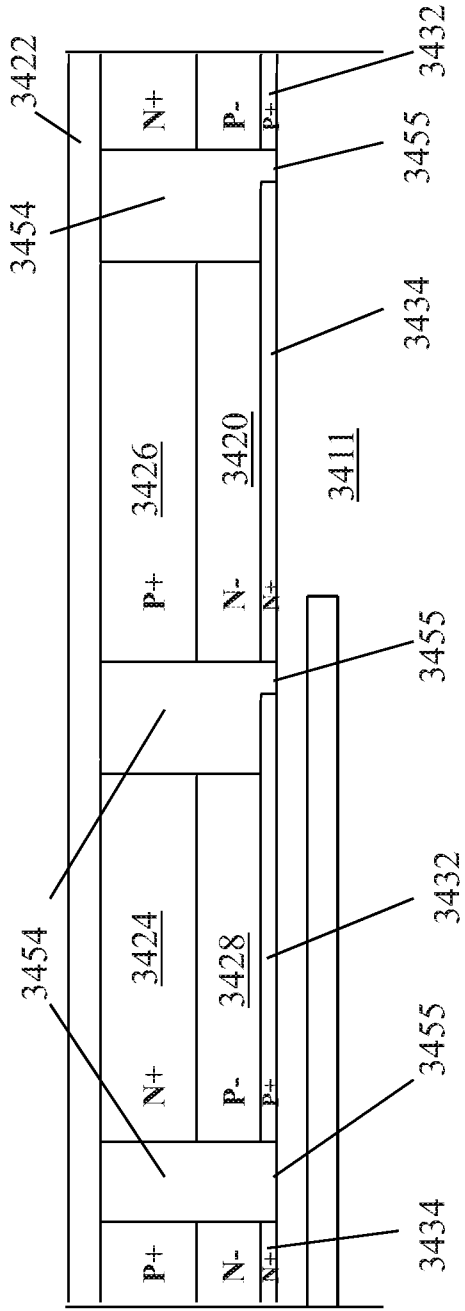


FIG. 34I

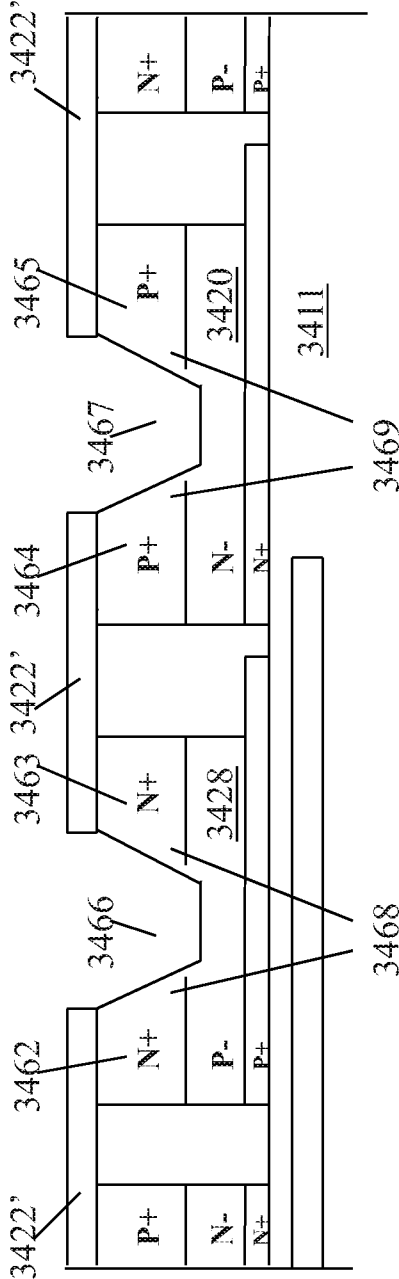


FIG. 34J

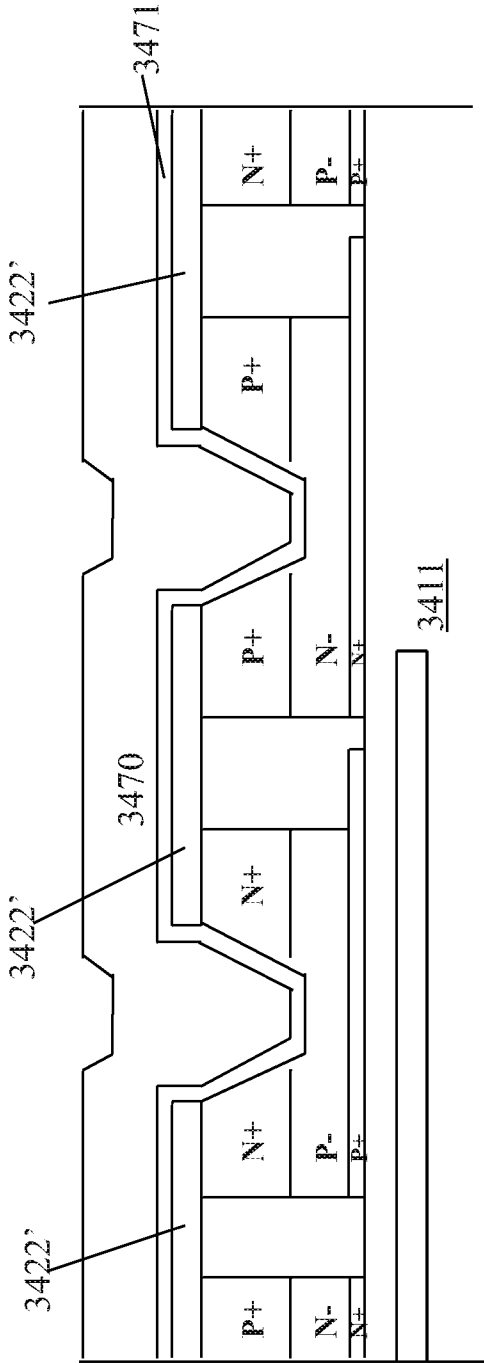


FIG. 34K

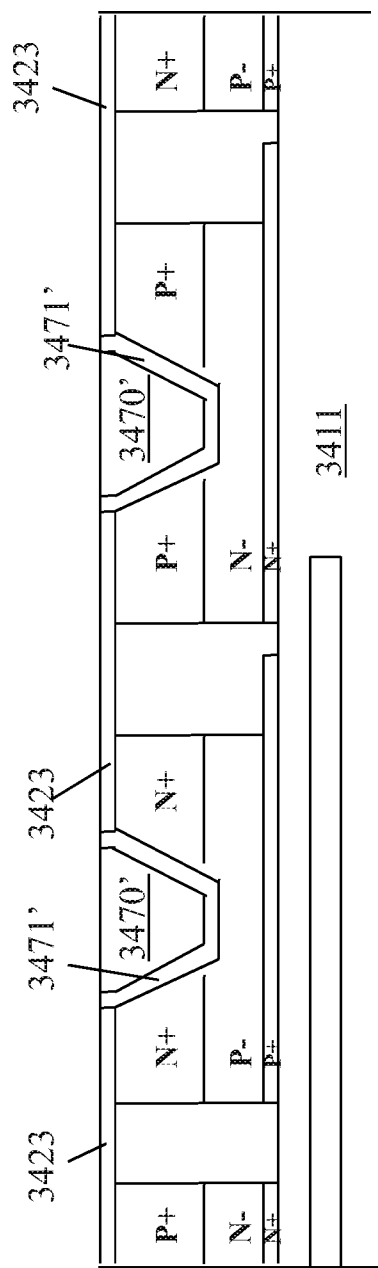
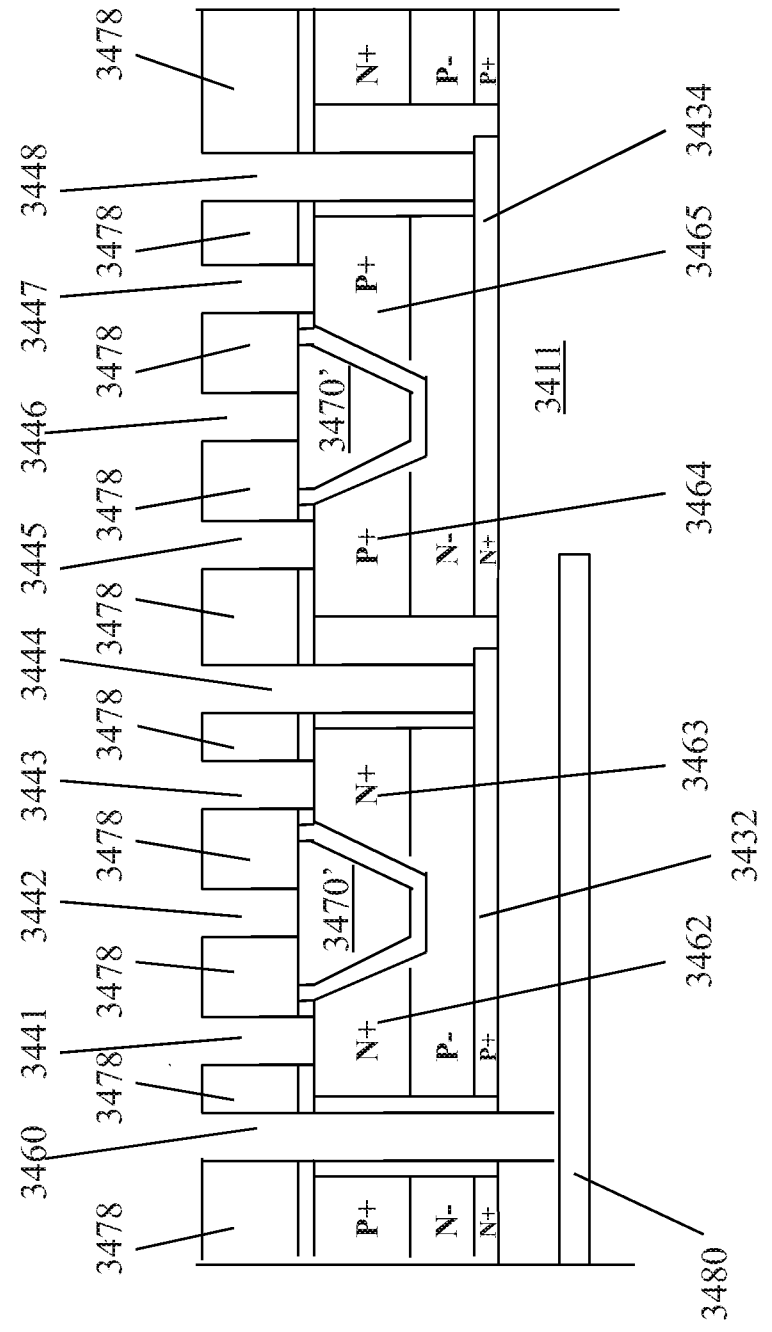




FIG. 34L



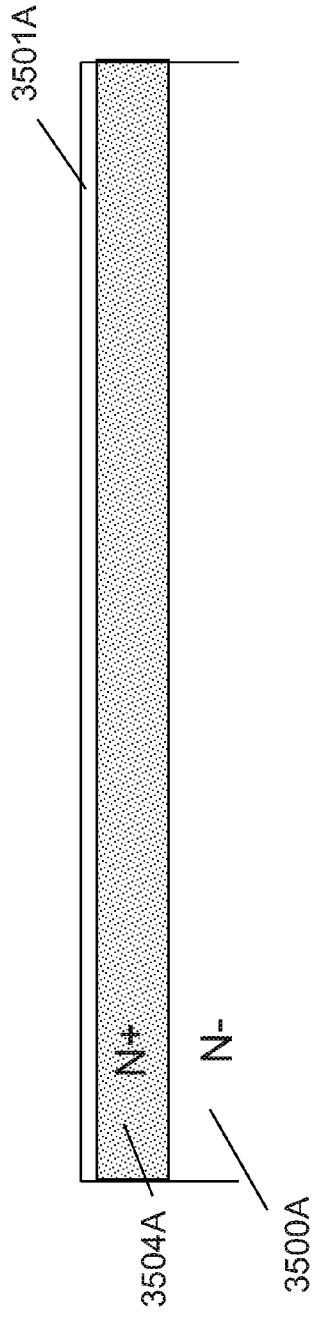


FIG. 35A

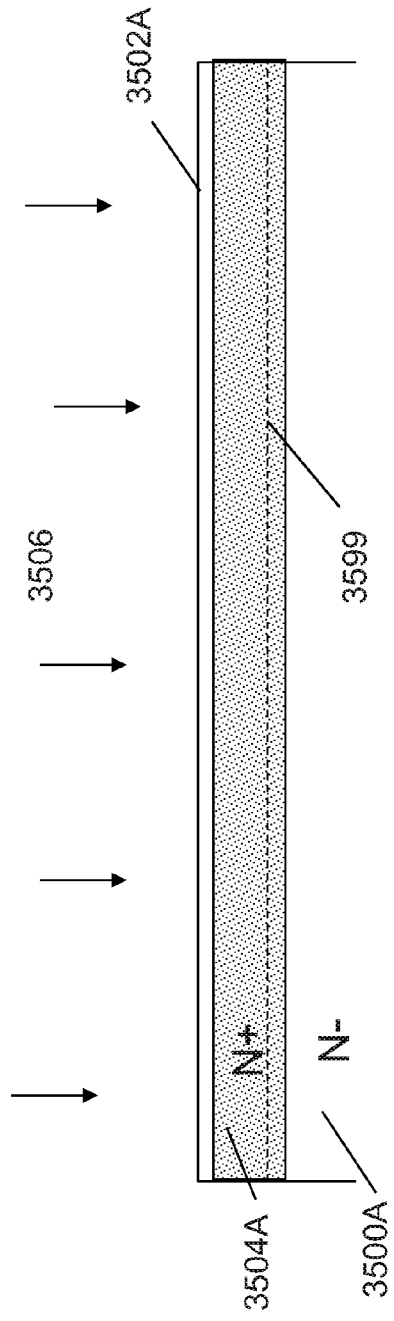


FIG. 35B

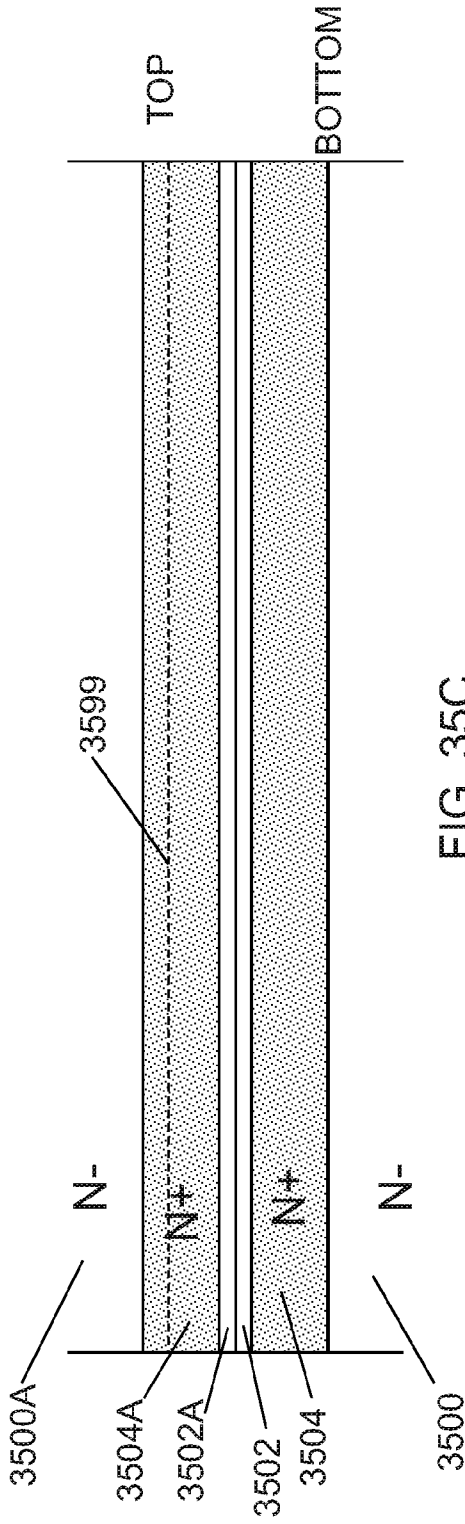


FIG. 35C

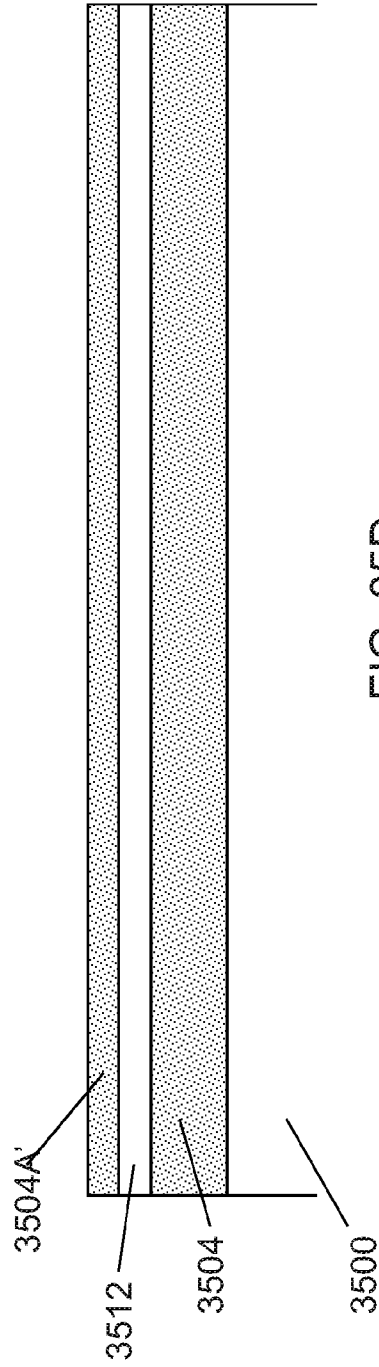


FIG. 35D

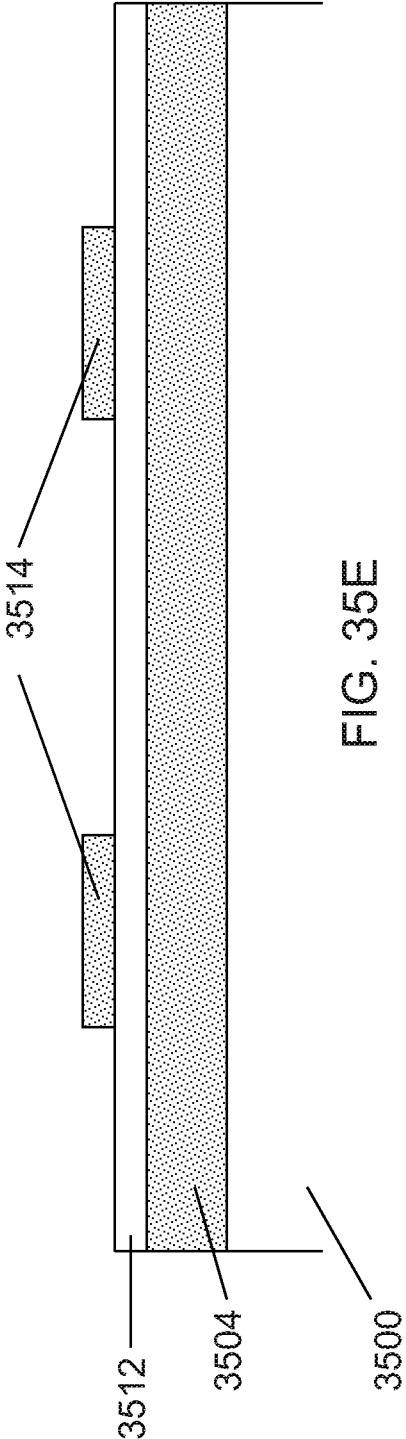


FIG. 35E

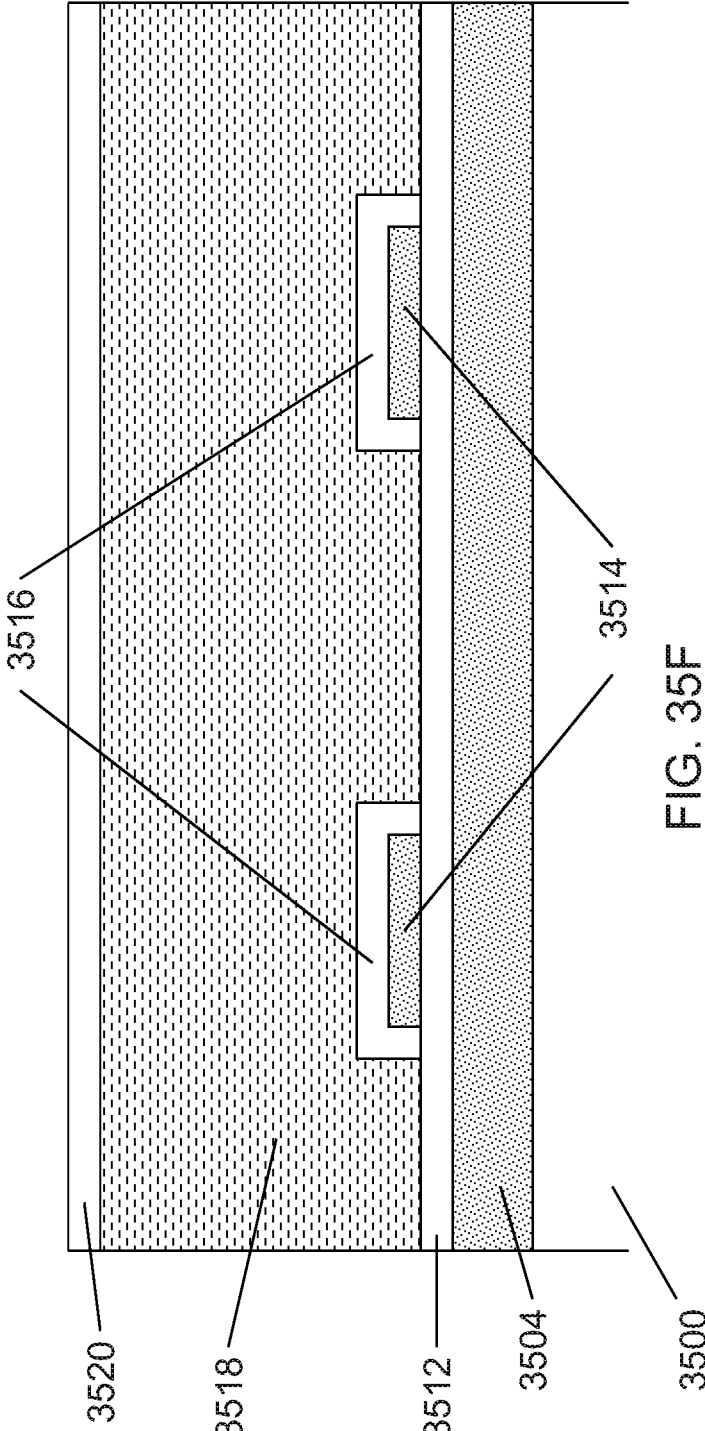


FIG. 35F

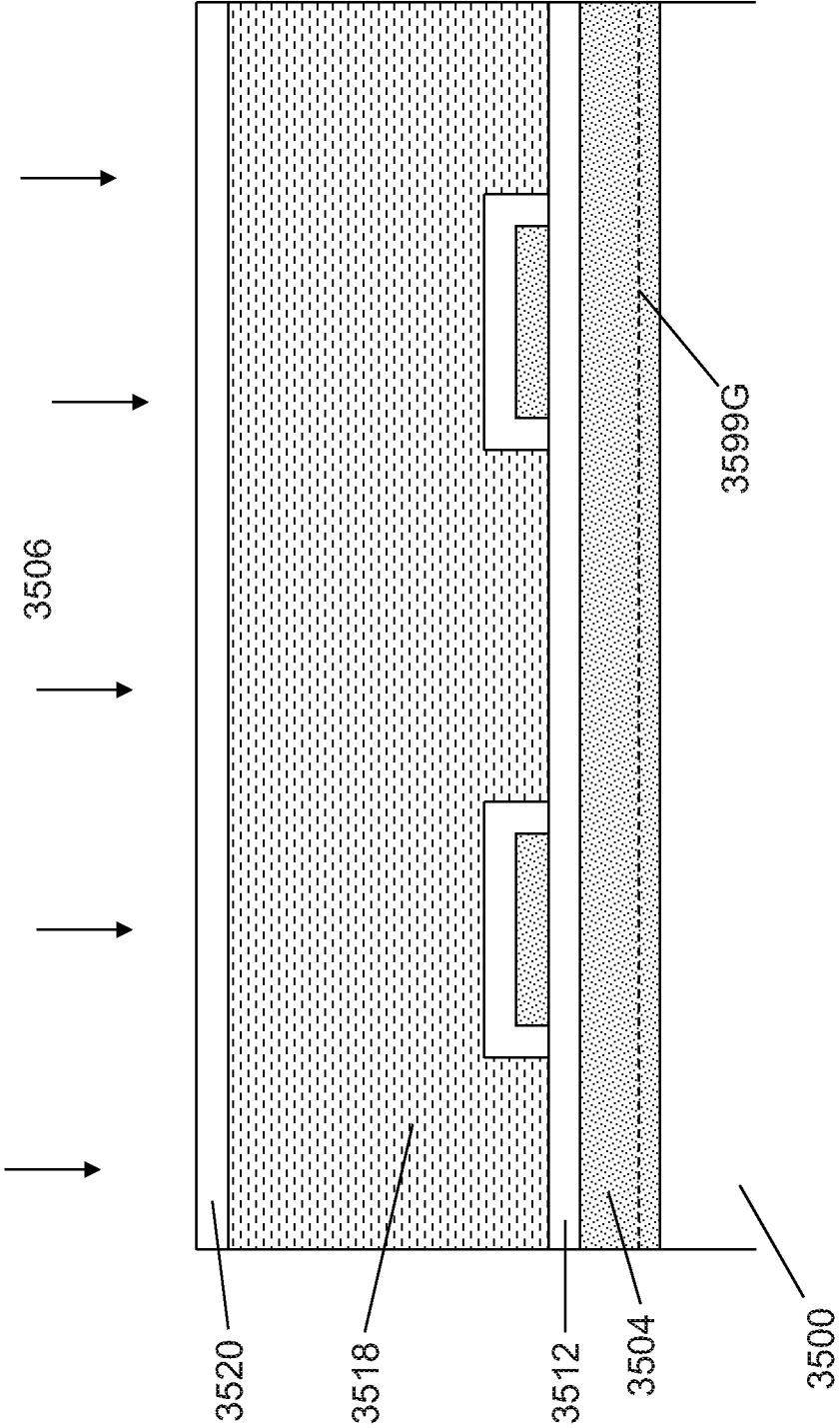


FIG. 35G

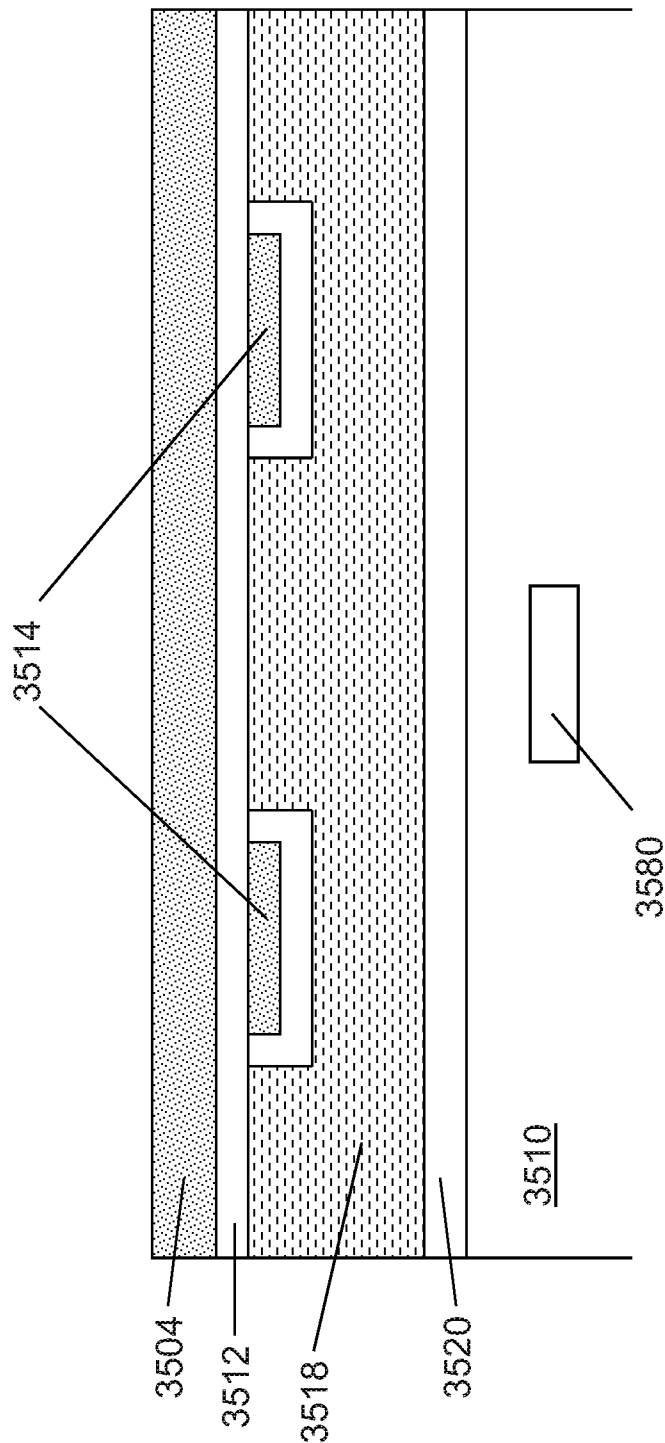


FIG. 35H

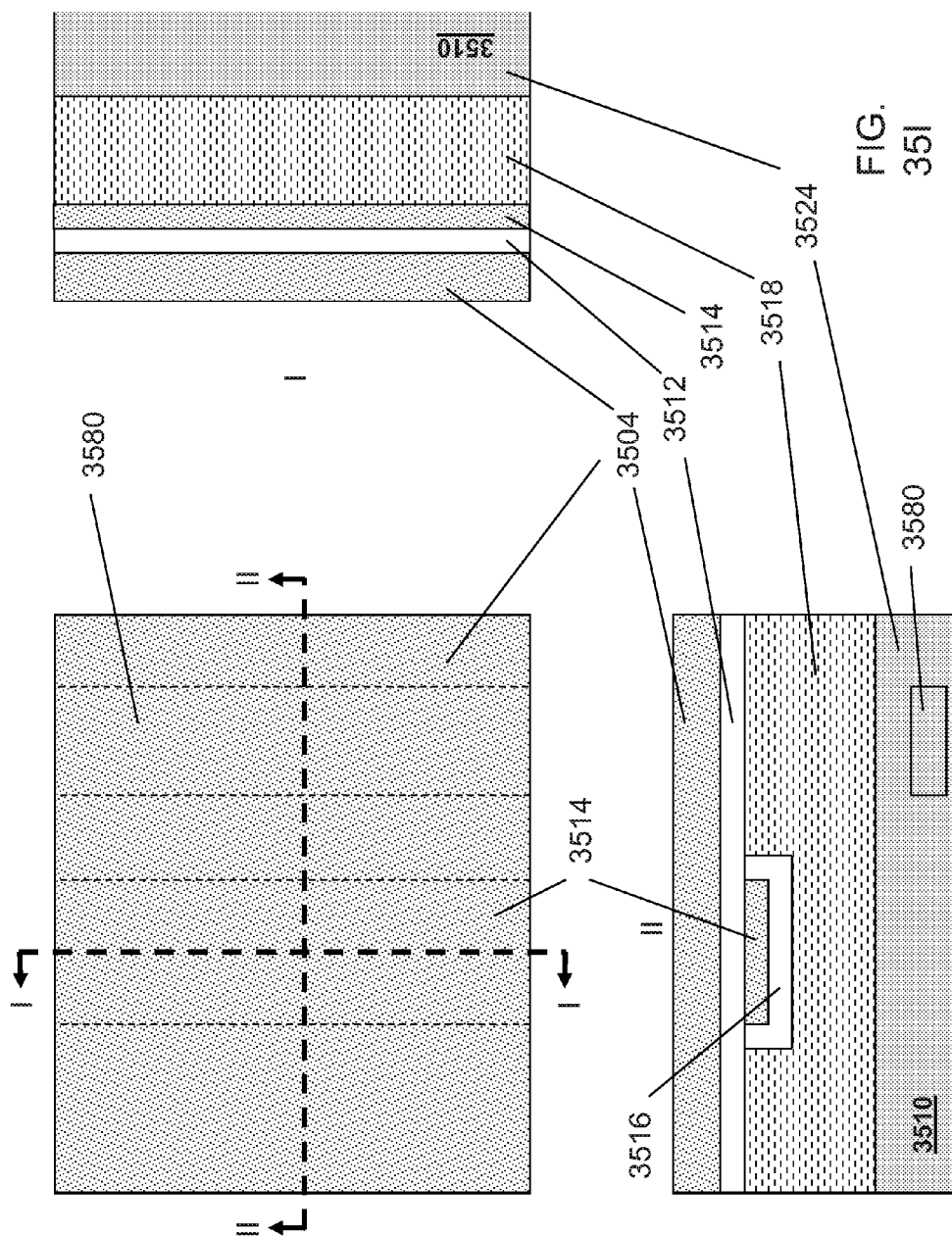
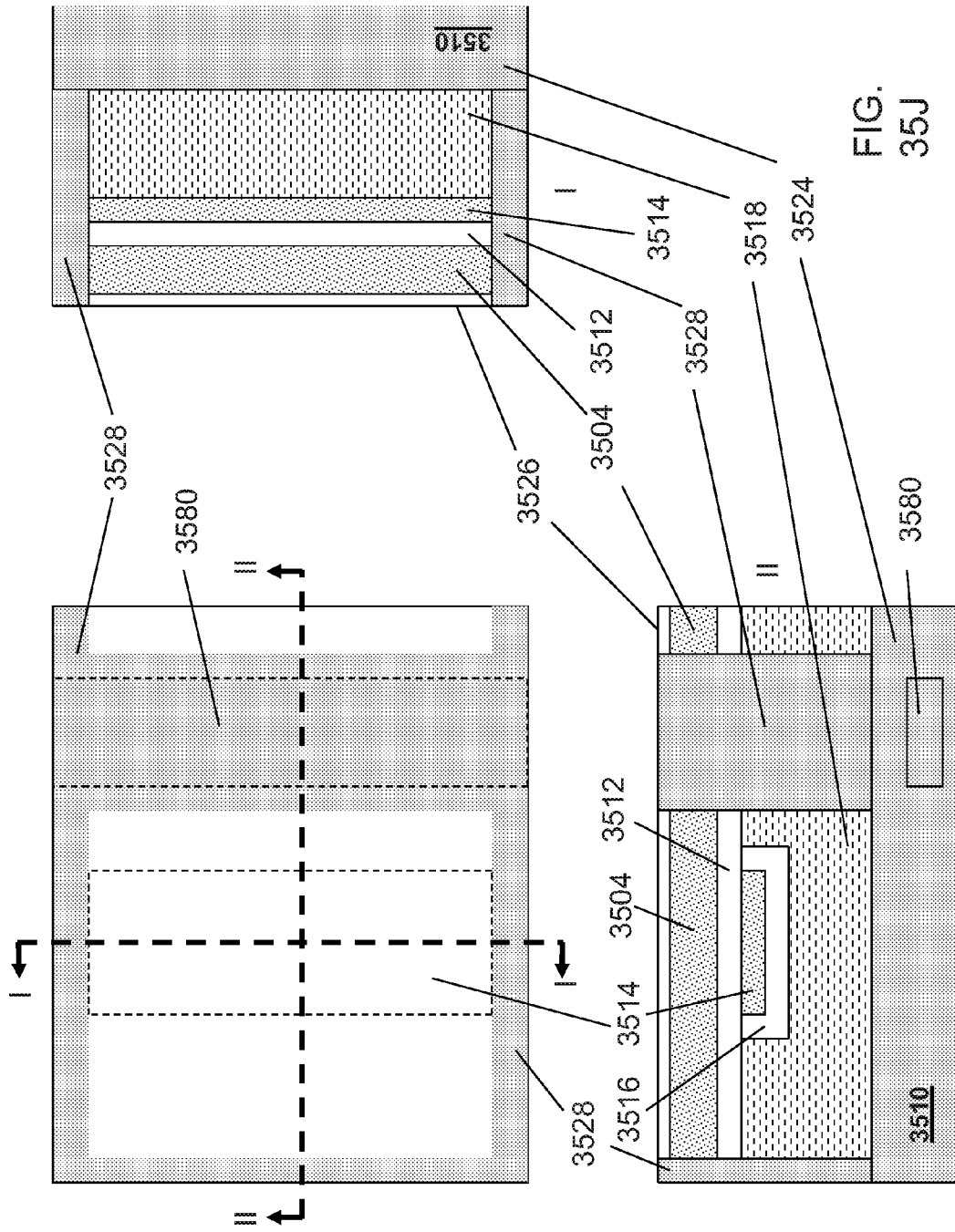


FIG. 351





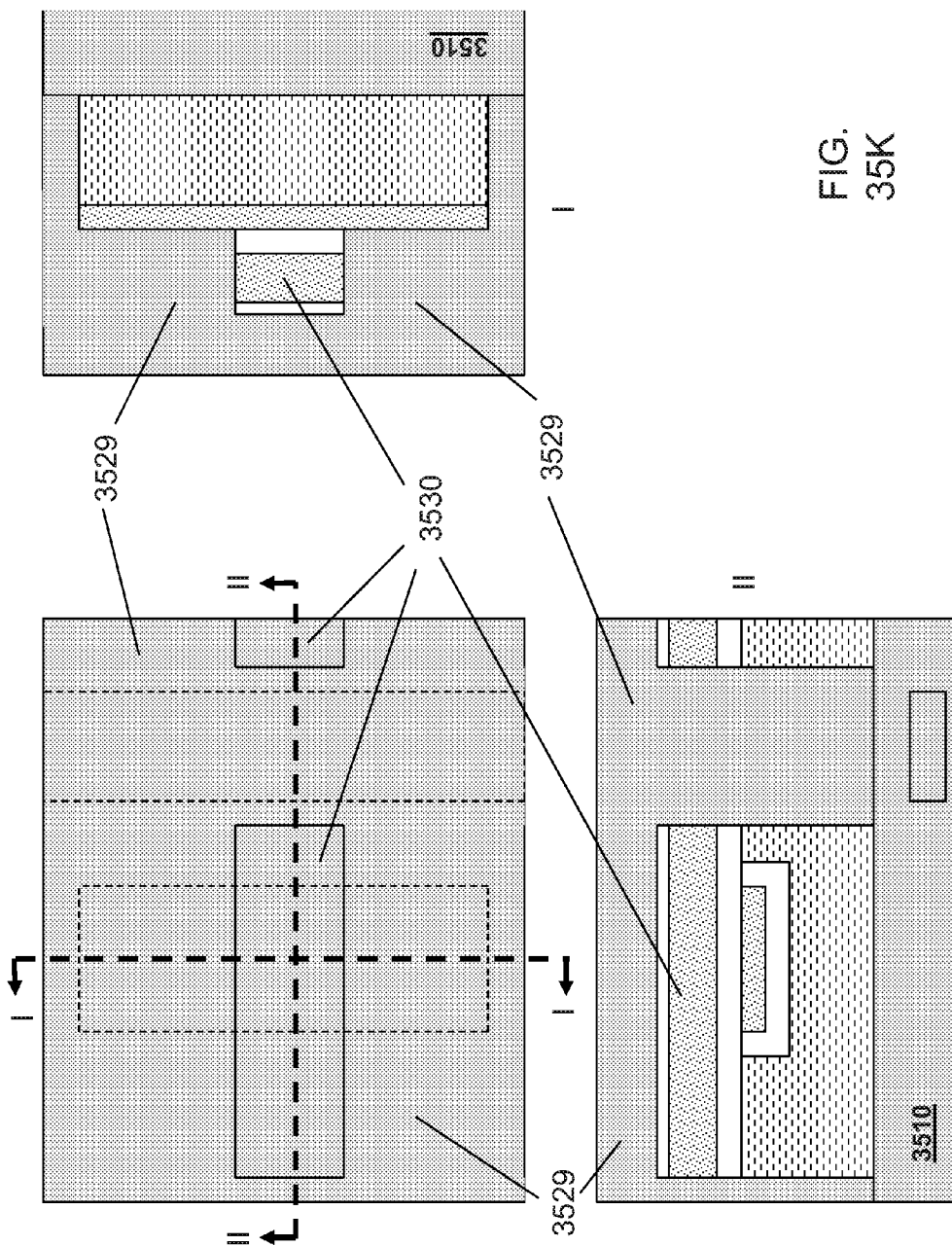


FIG. 35K

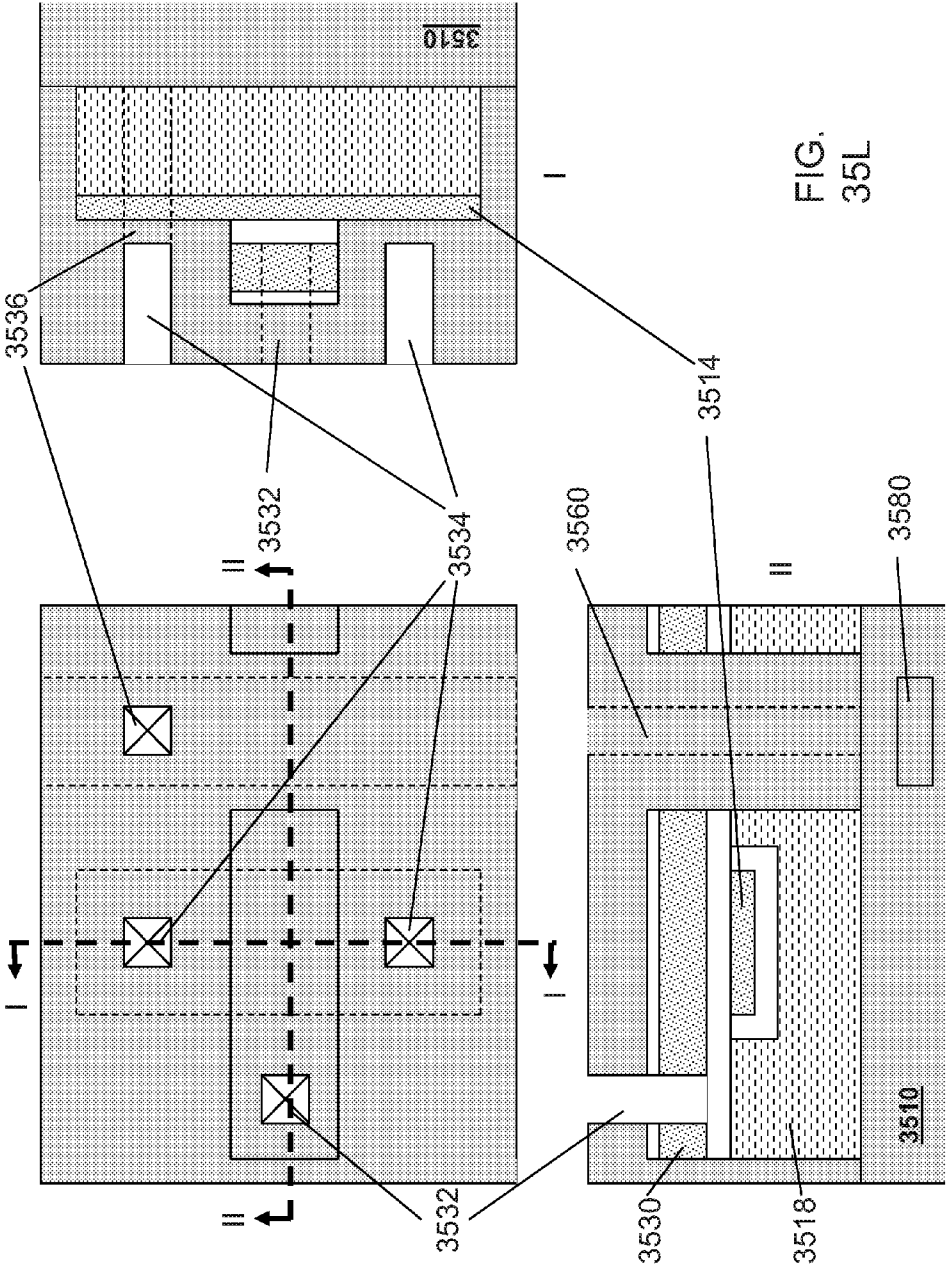


FIG. 35L

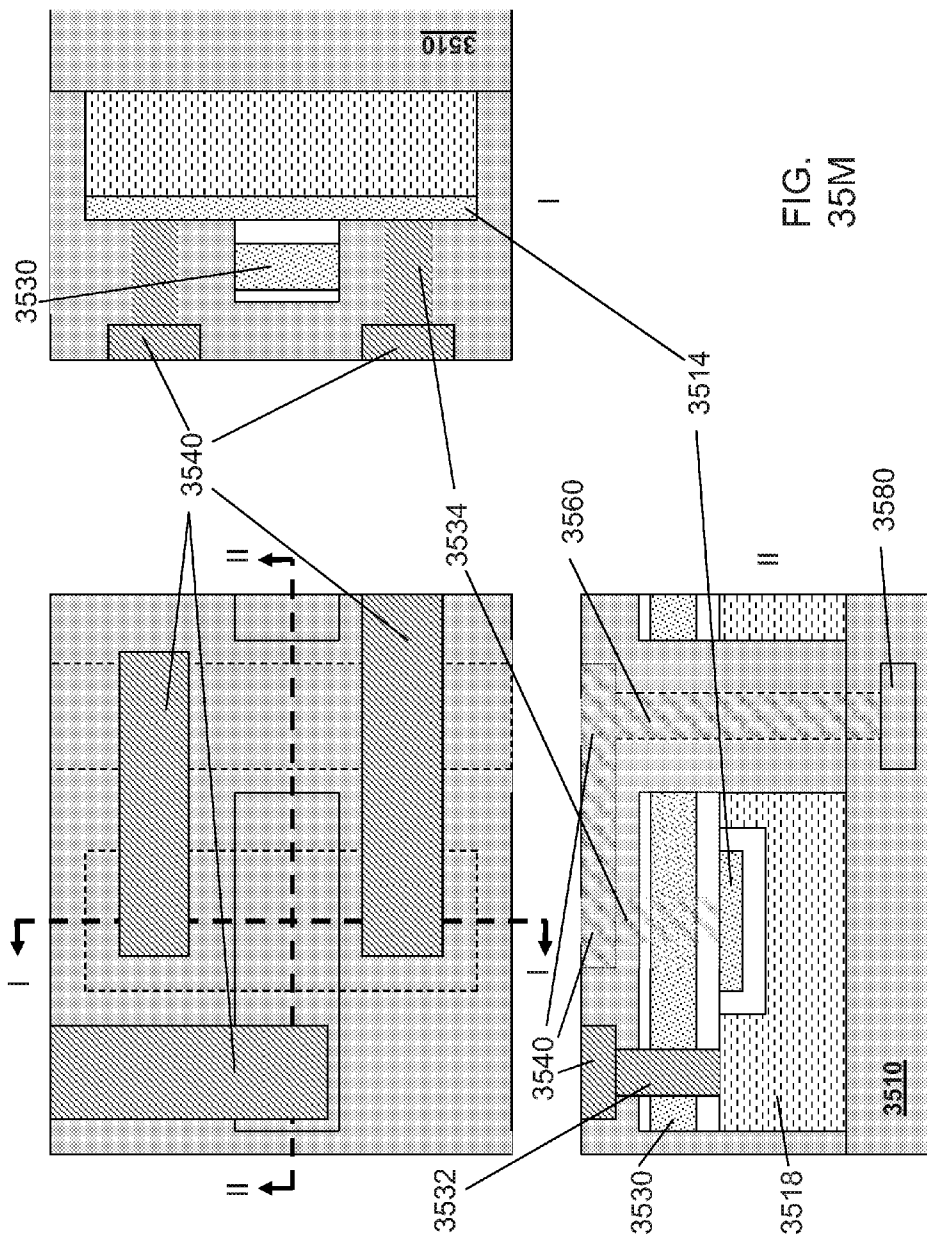


FIG. 35M

FIG. 36A

PMOS

NMOS

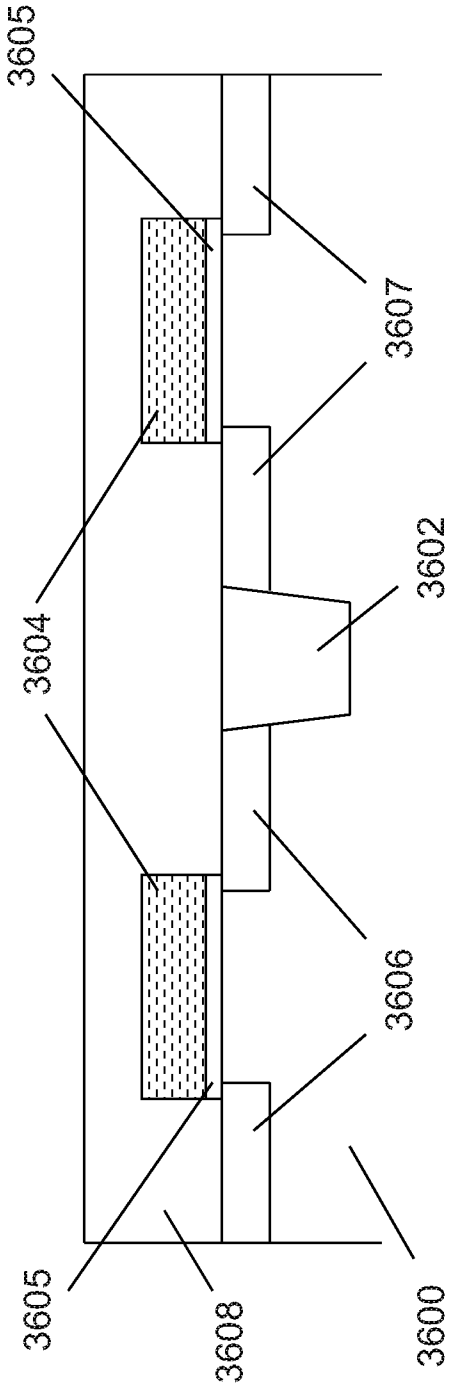


FIG. 36B NMOS PMOS

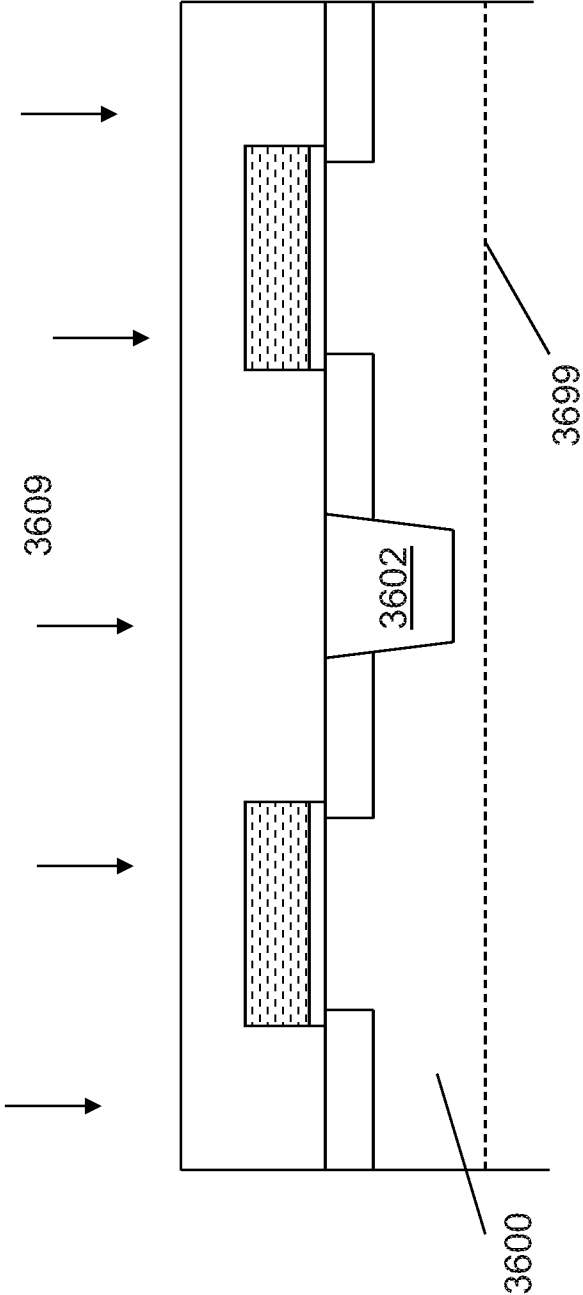
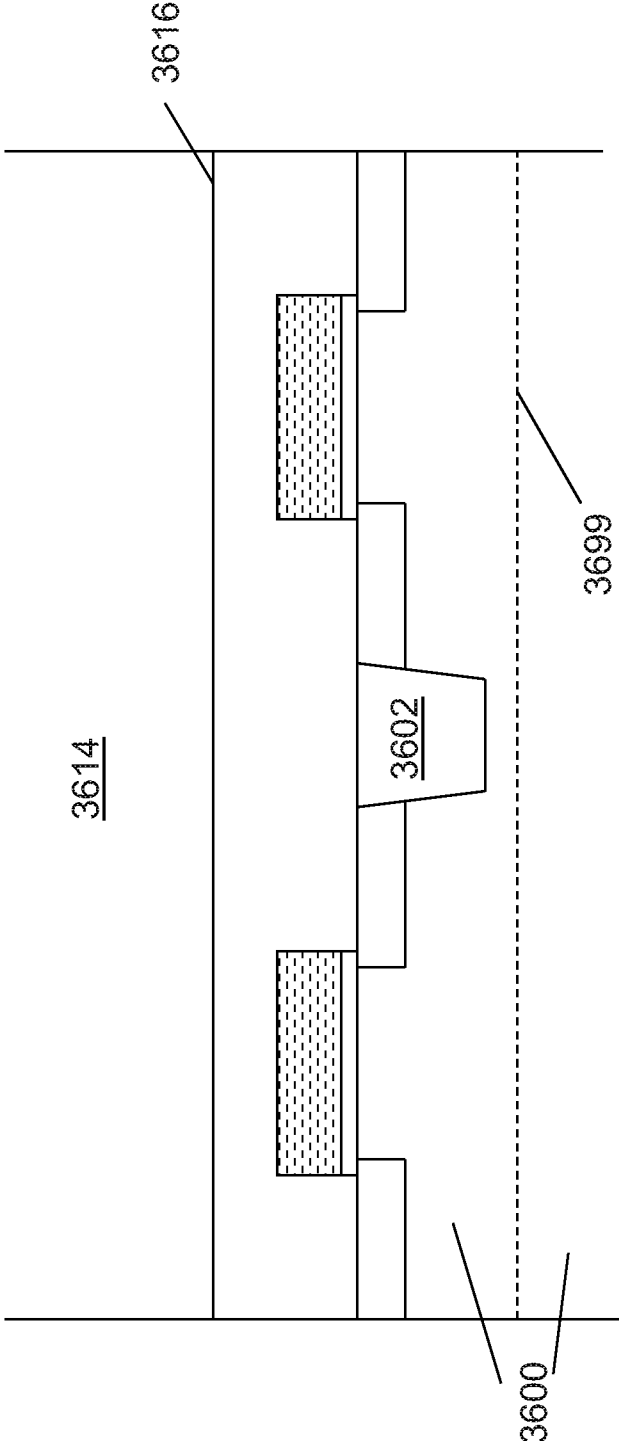


FIG. 36C

NMOS

PMOS



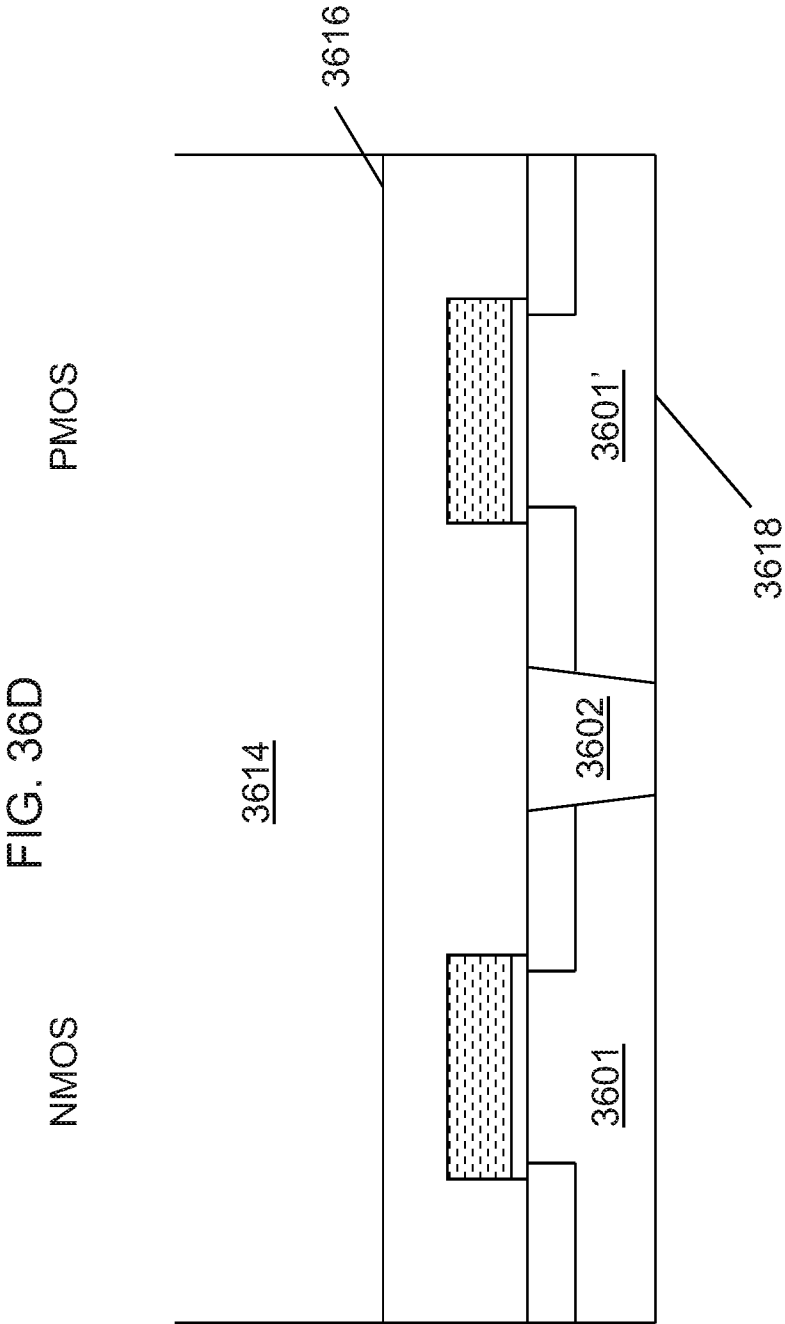




FIG. 36E NMOS PMOS

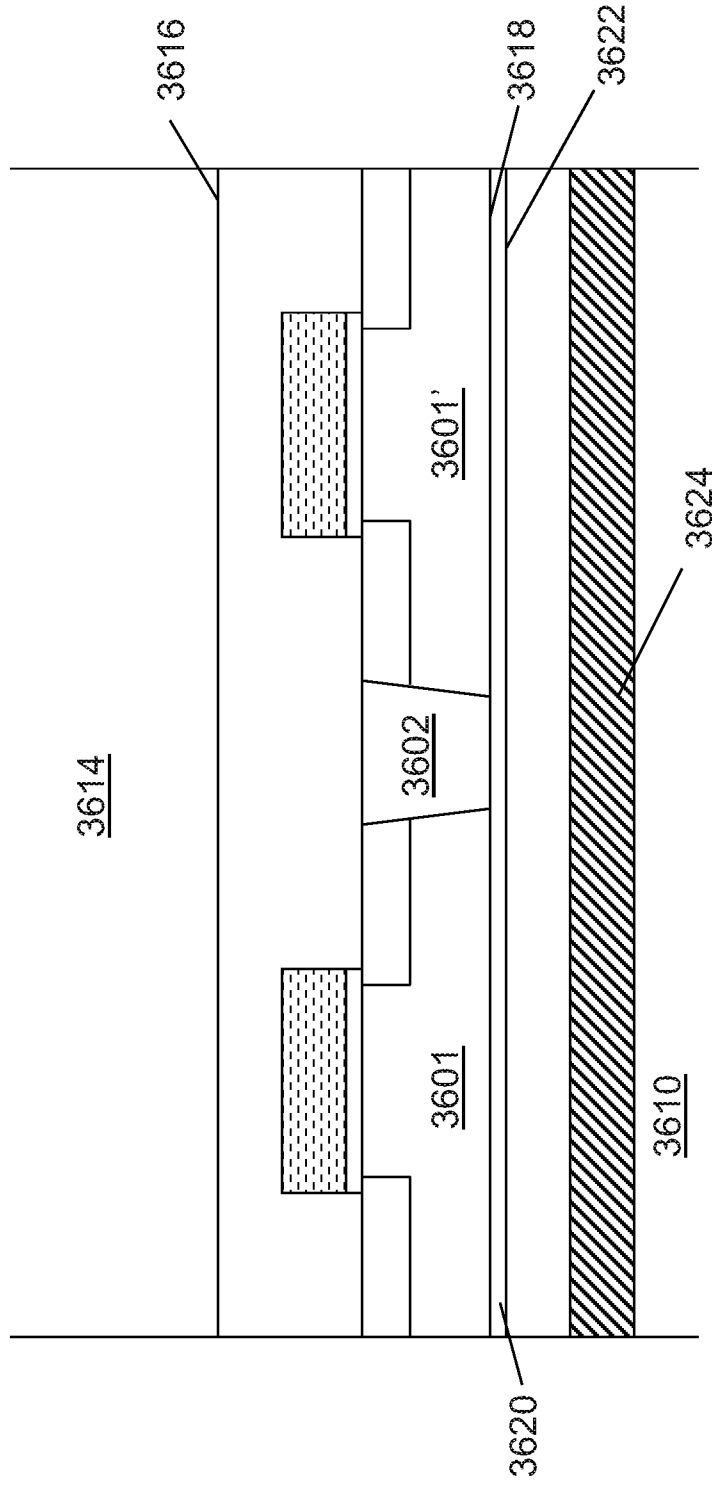
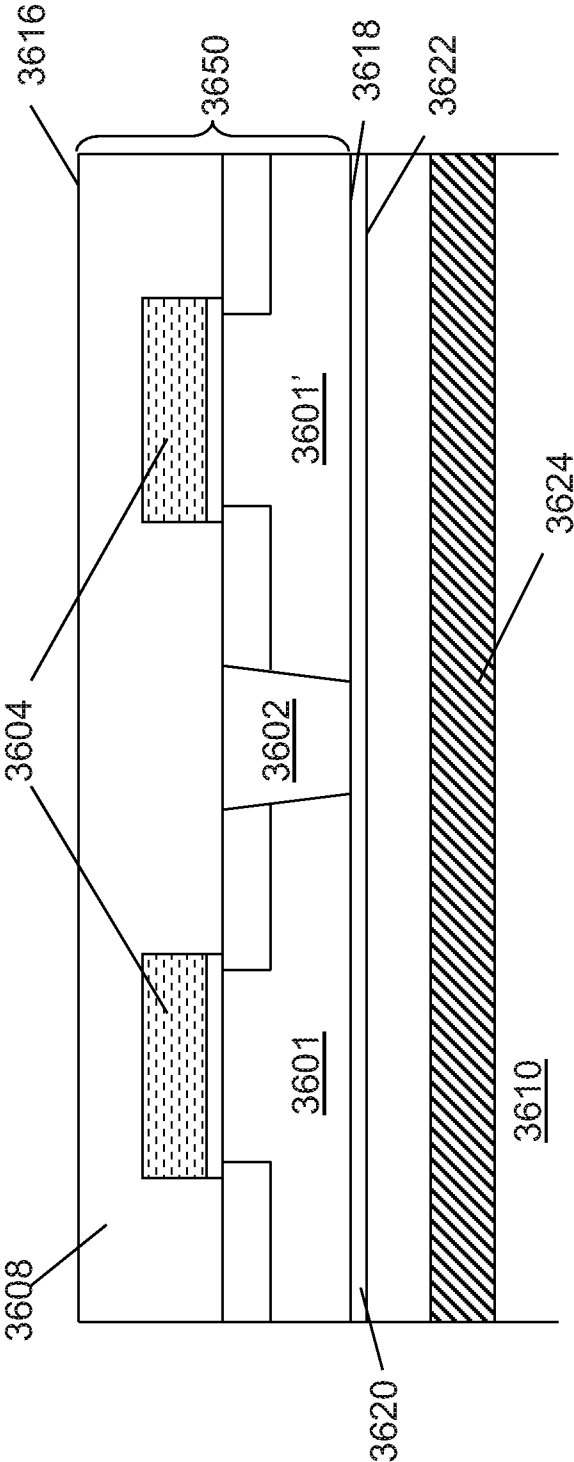


FIG. 36F

NMOS

PMOS



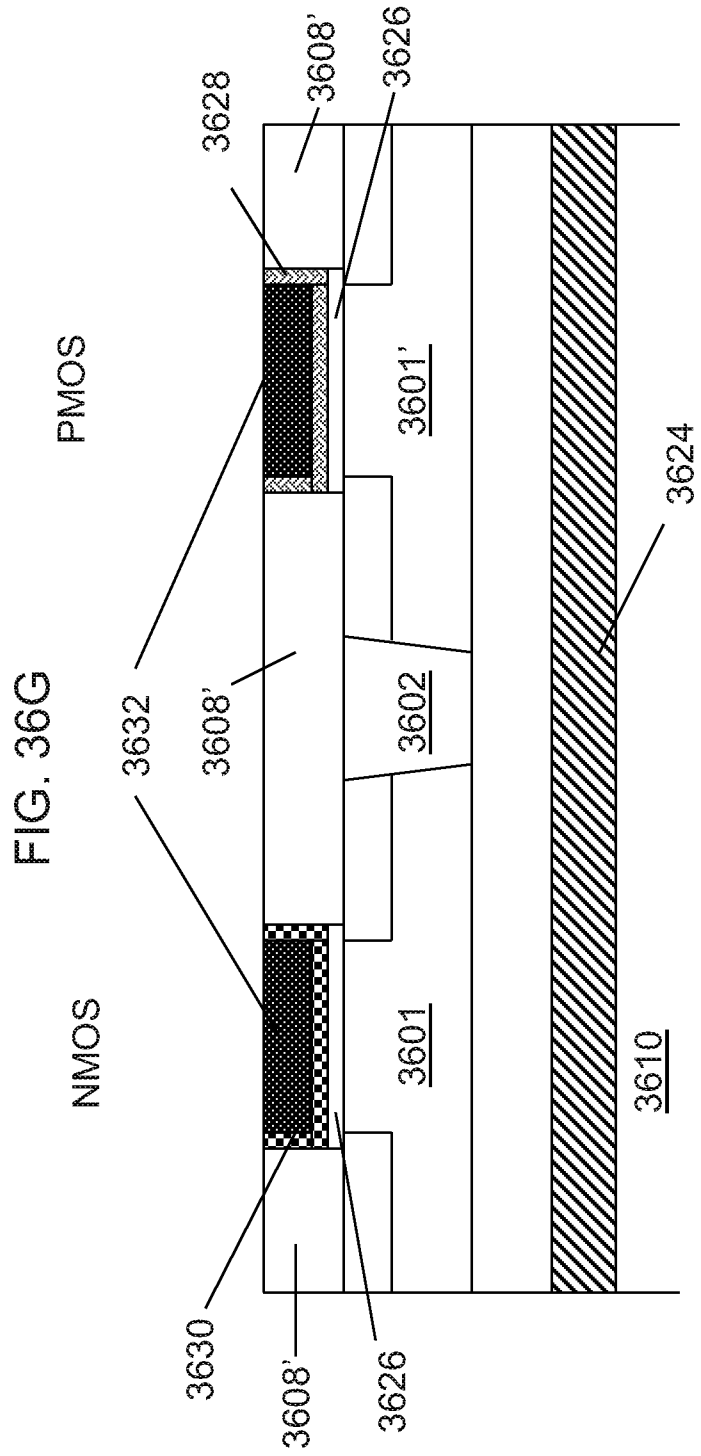
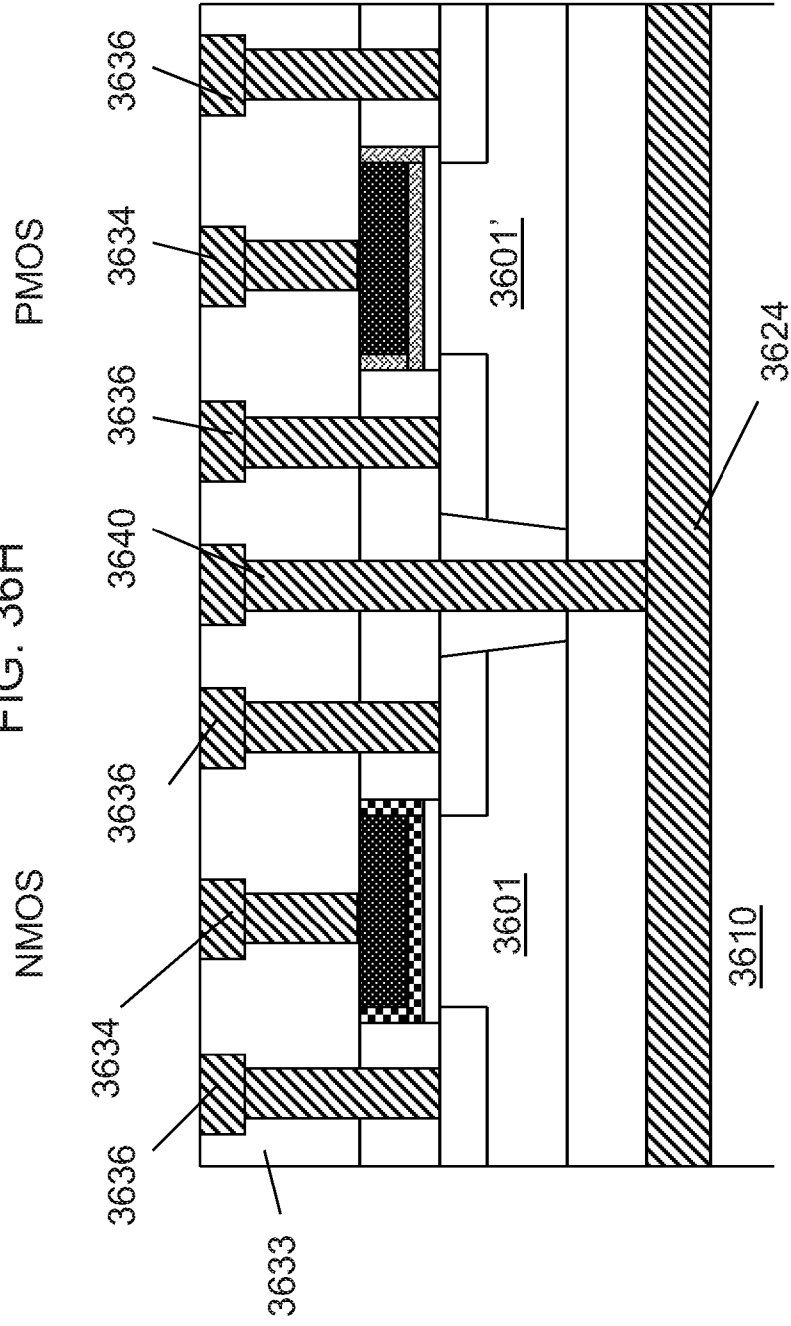


FIG. 36H



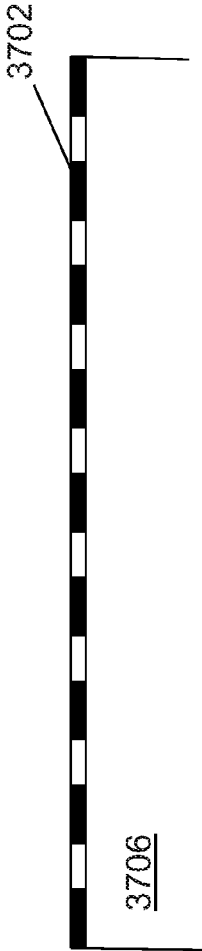


FIG. 37A

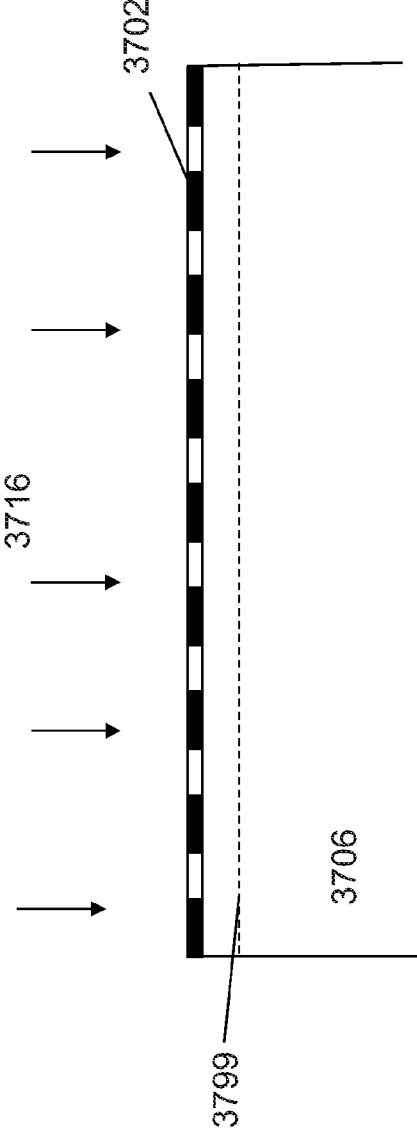


FIG. 37B

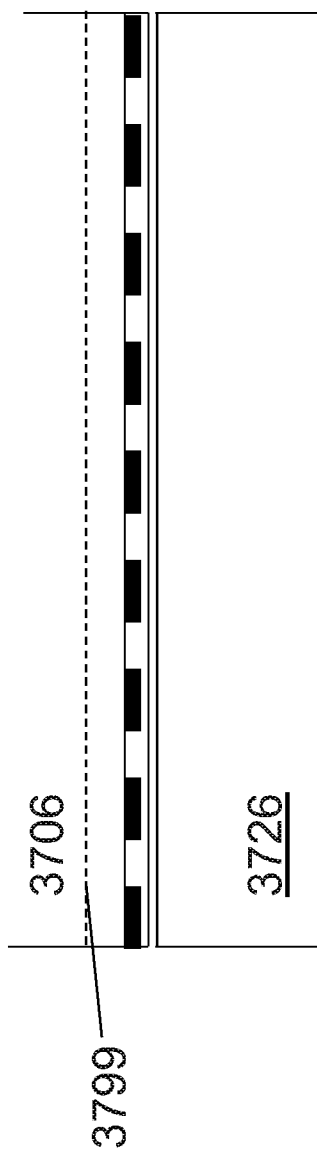


FIG. 37C

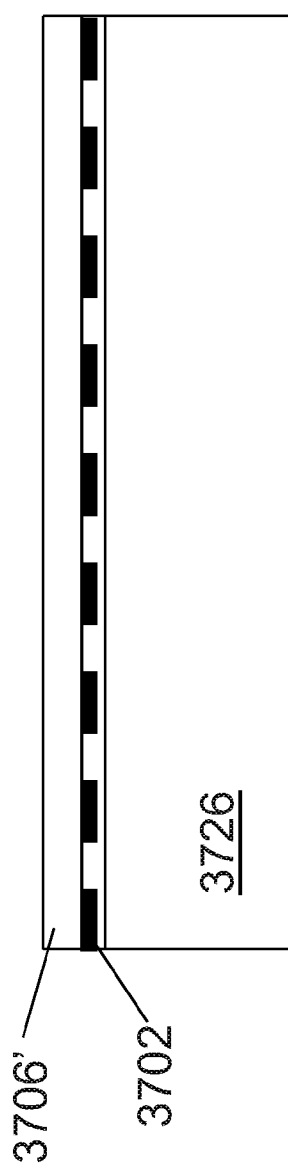


FIG. 37D

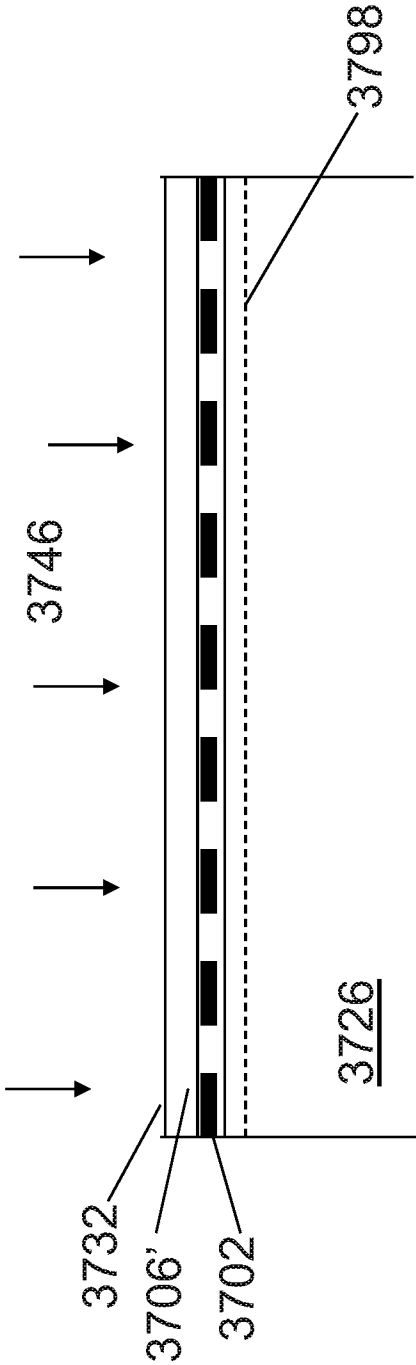


FIG. 37E

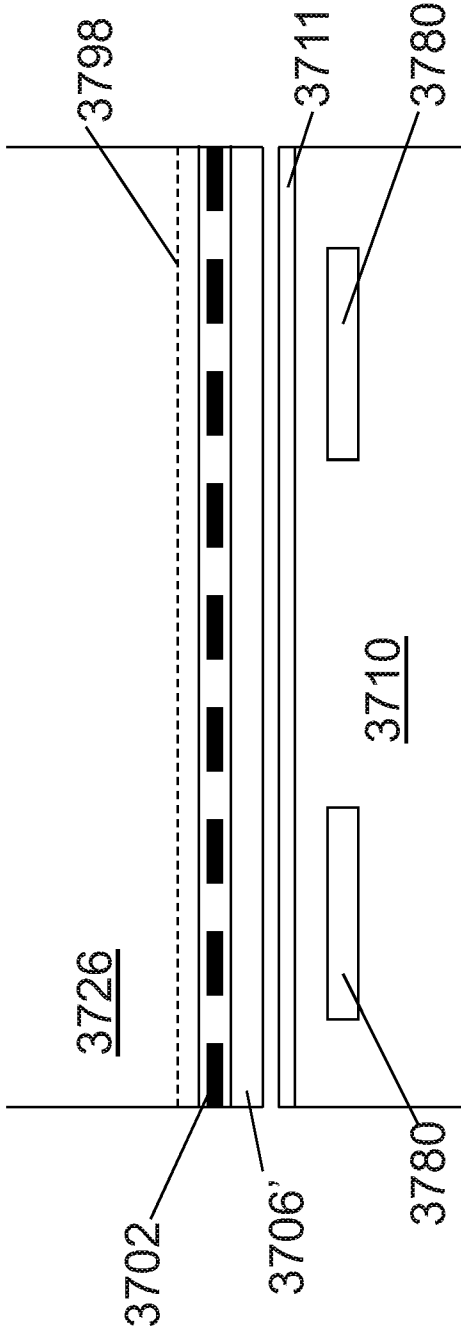


FIG. 37F



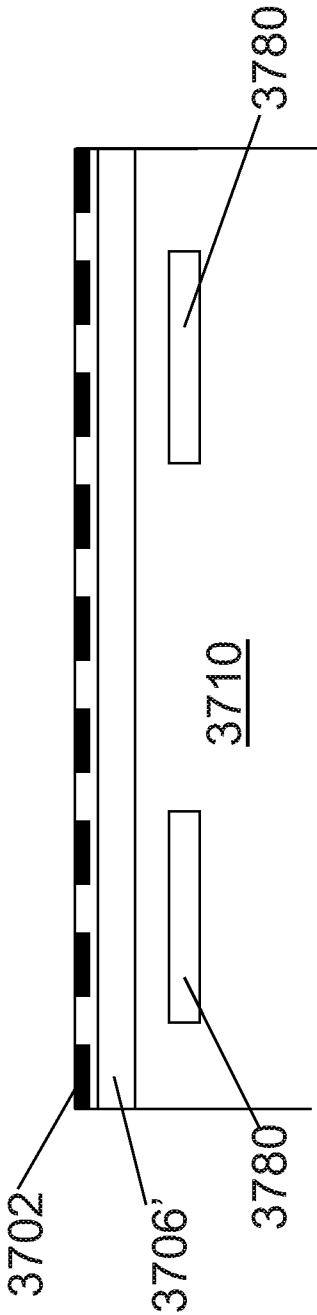


FIG. 37G

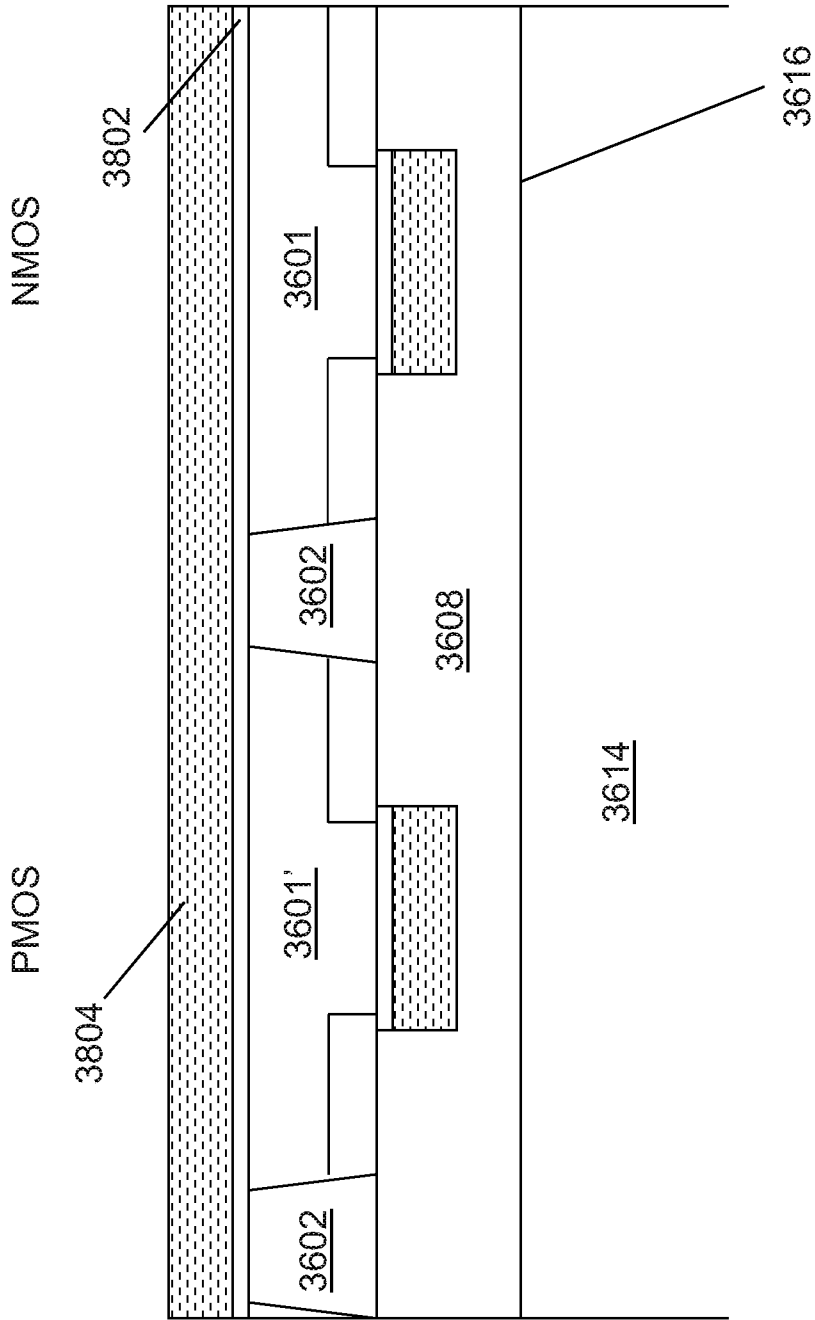


FIG. 38A

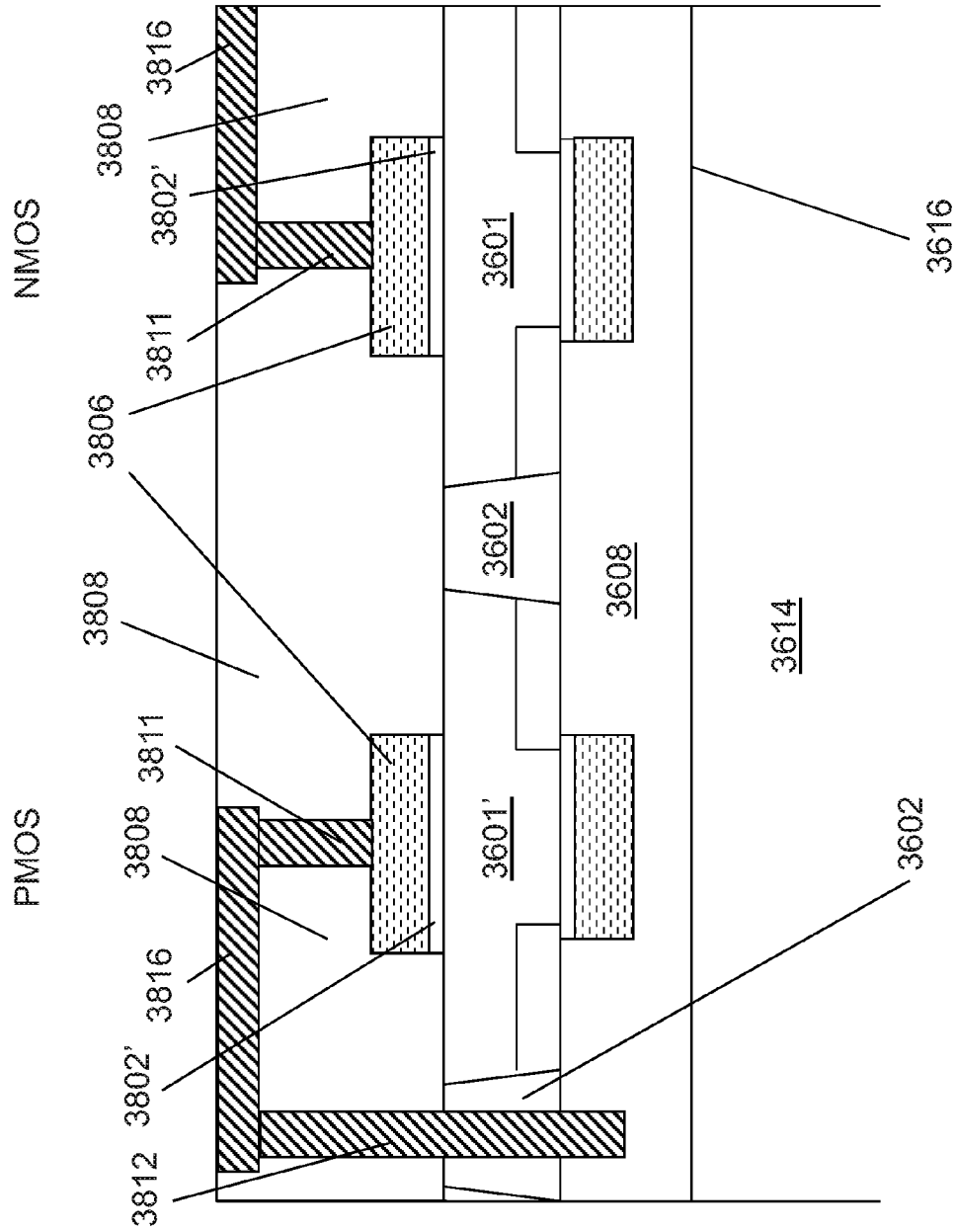


FIG. 38B

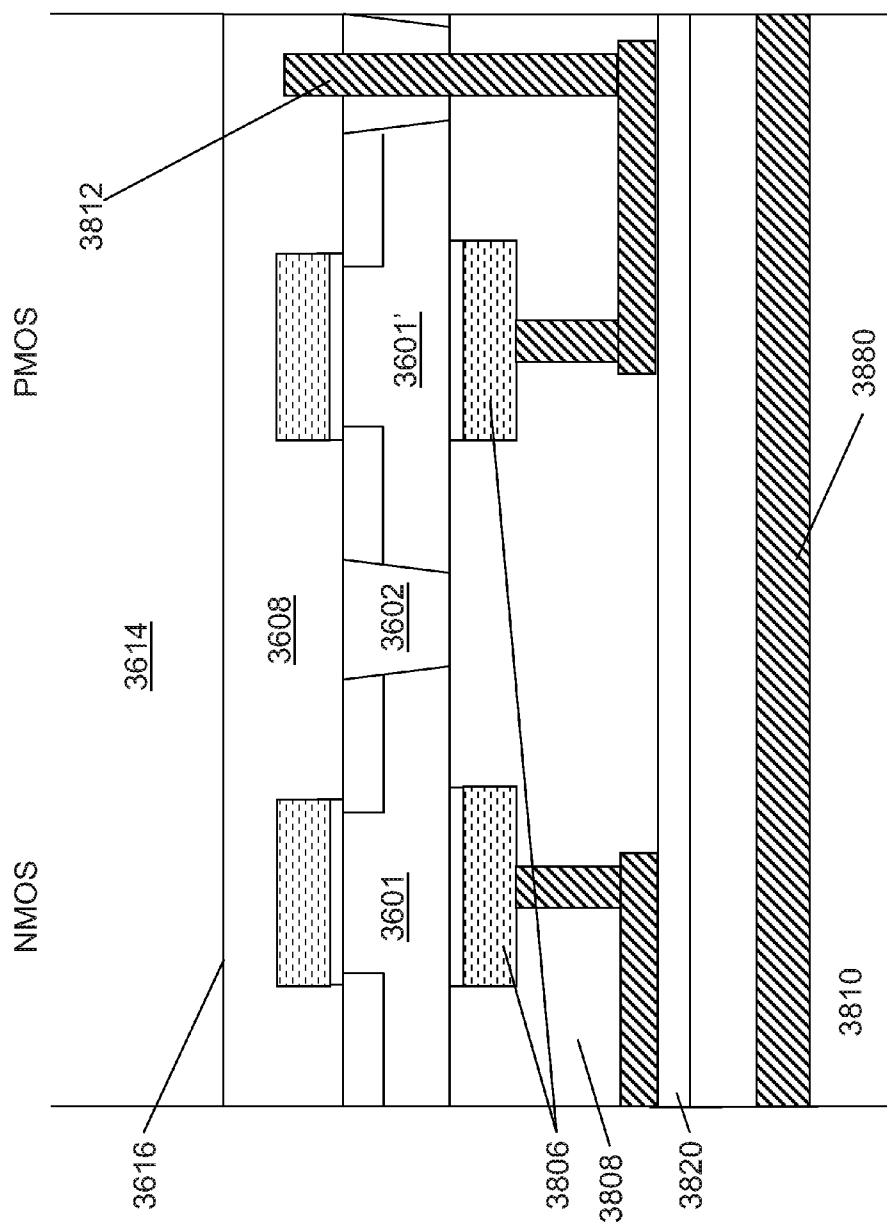


FIG. 38C

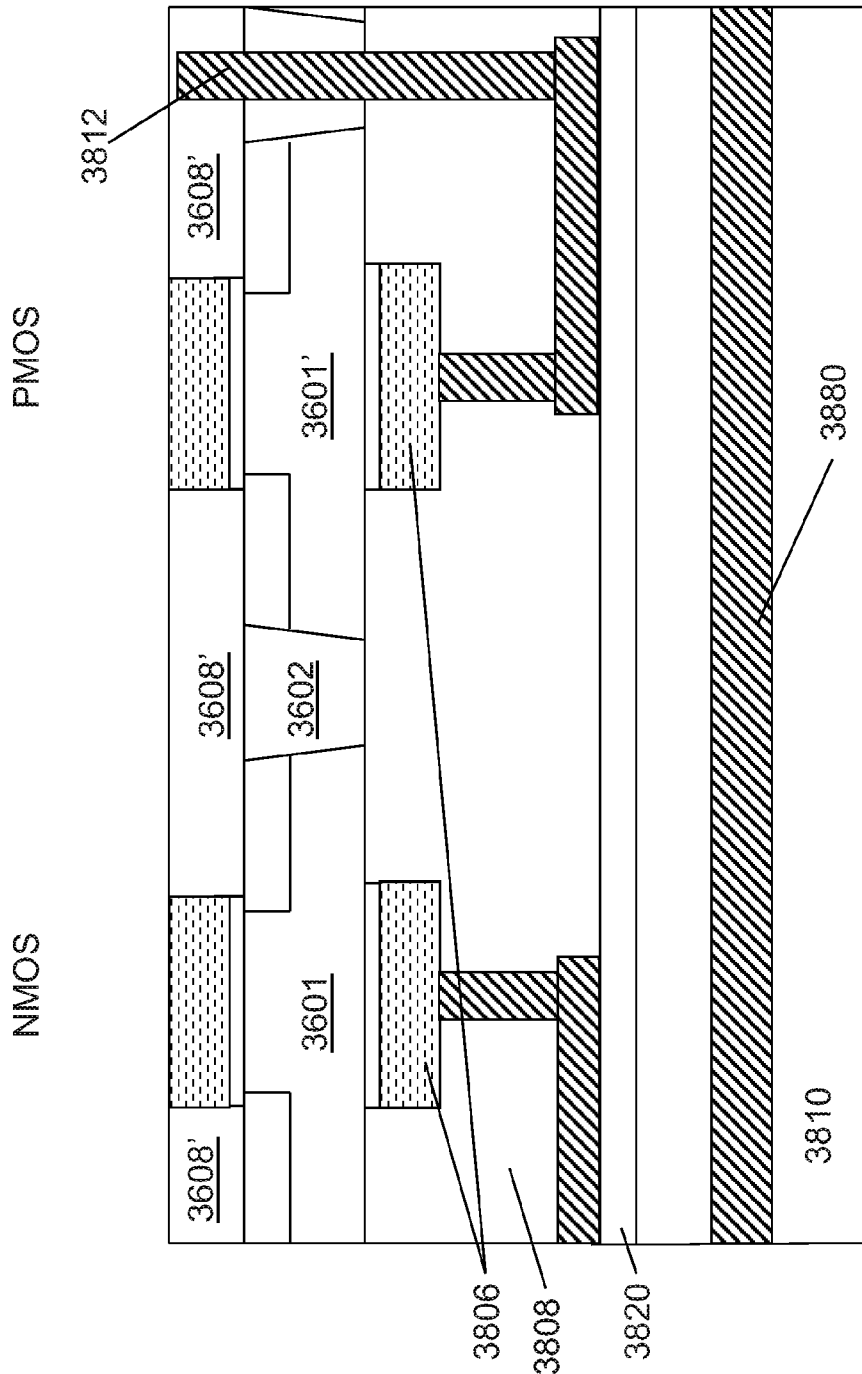


FIG. 38D

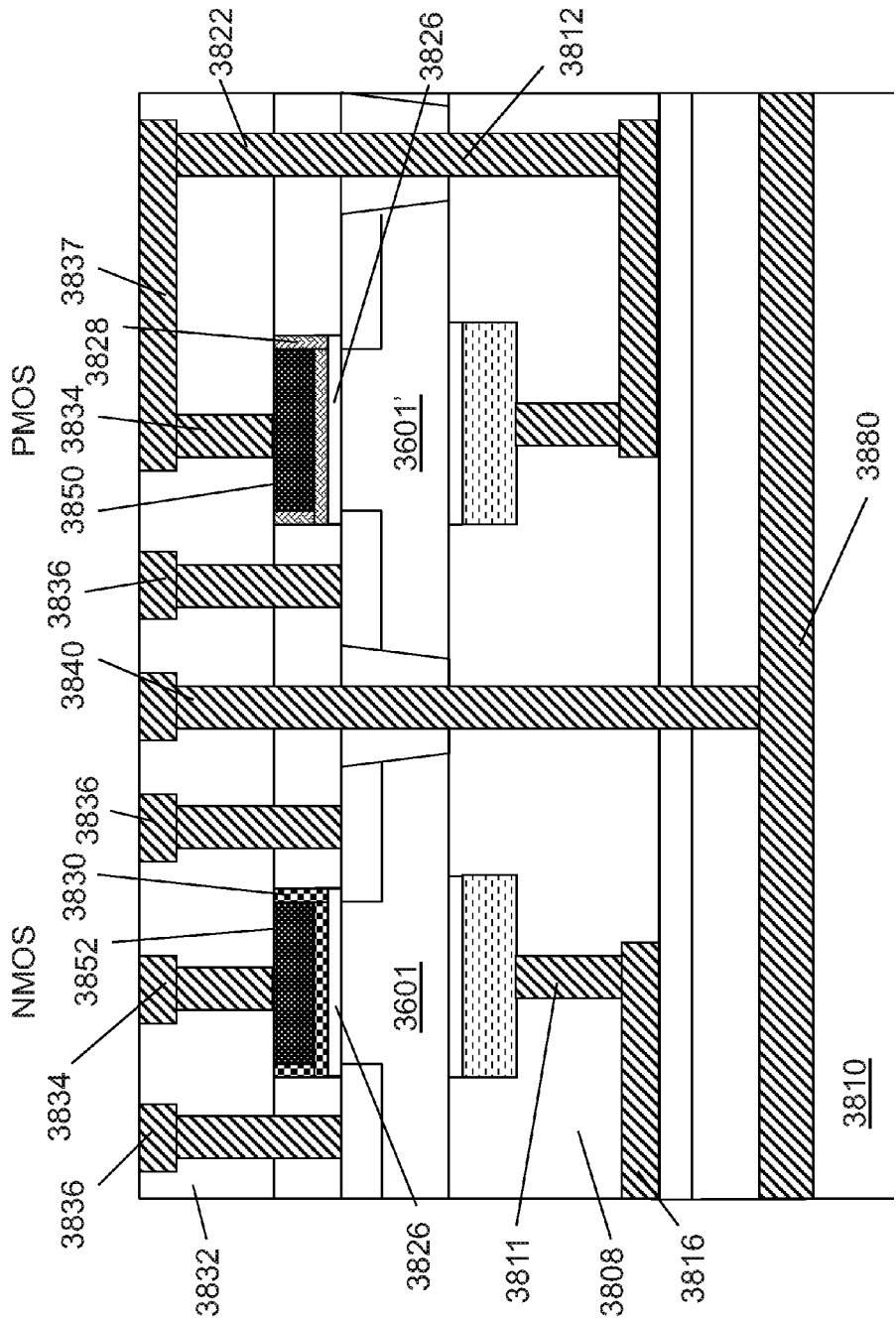


FIG. 38E

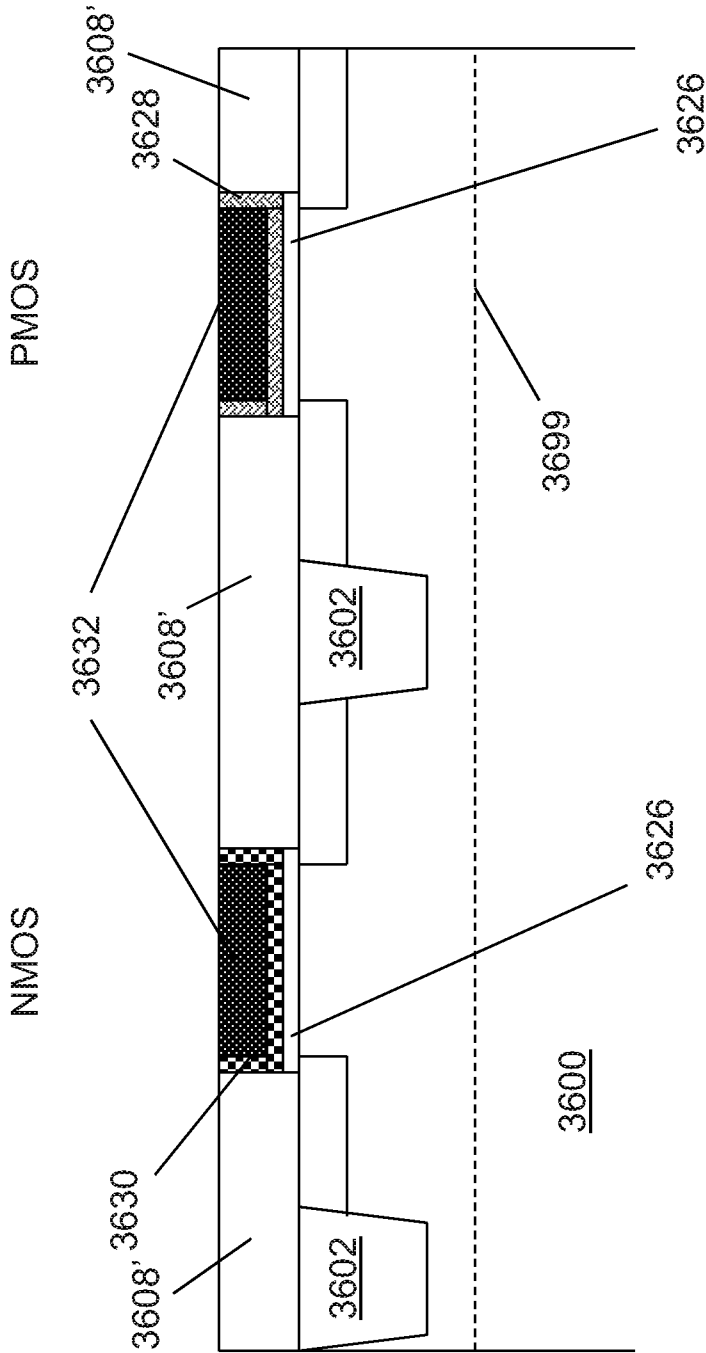


FIG. 39A

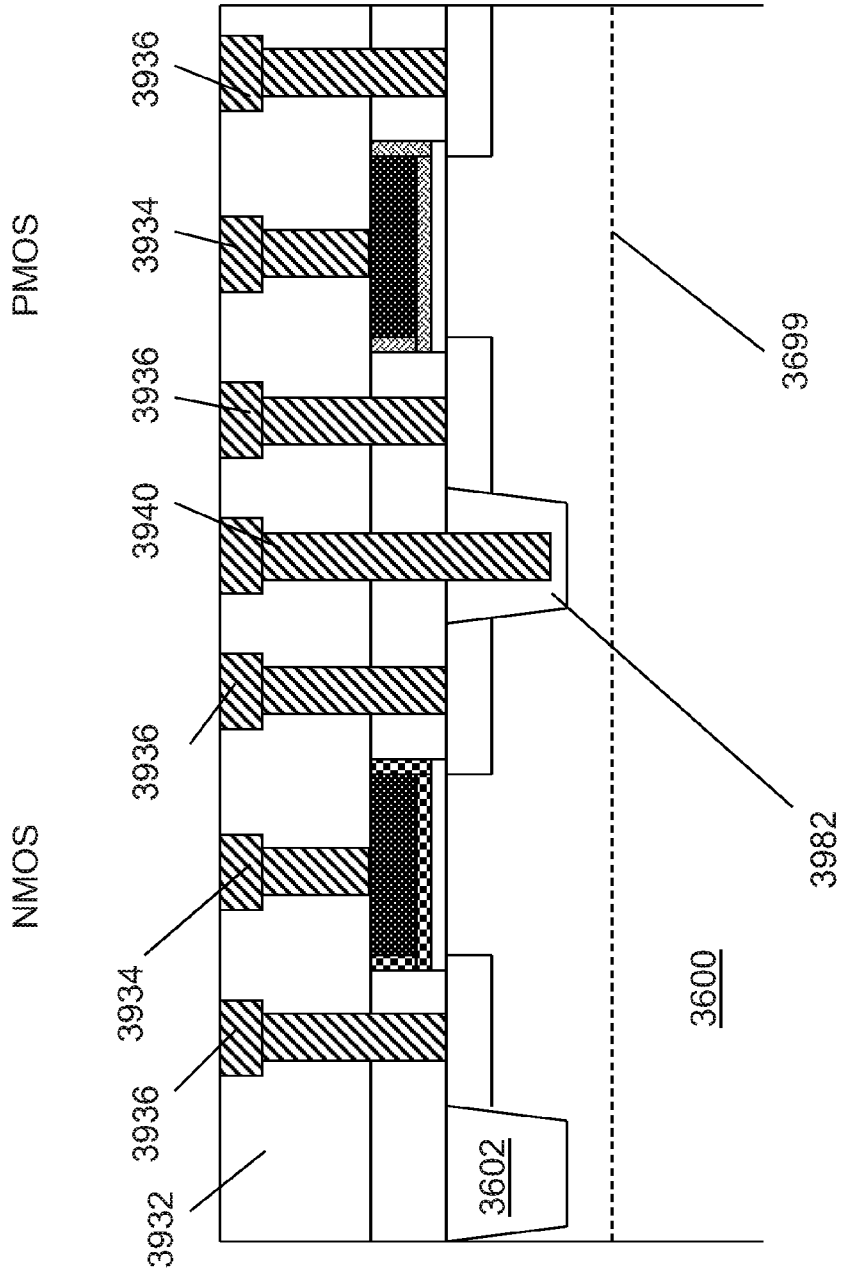


FIG. 39B



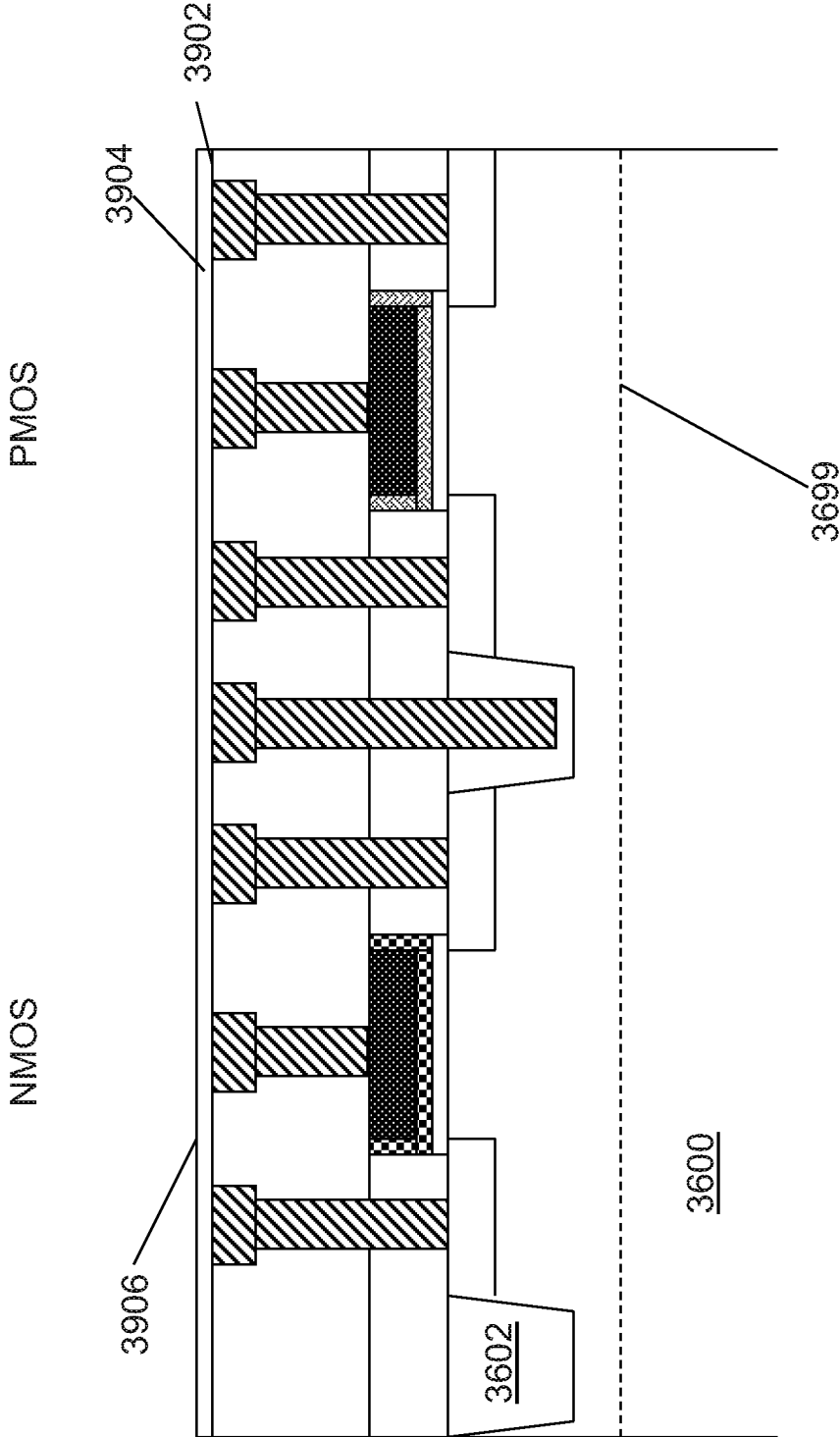


FIG. 39C

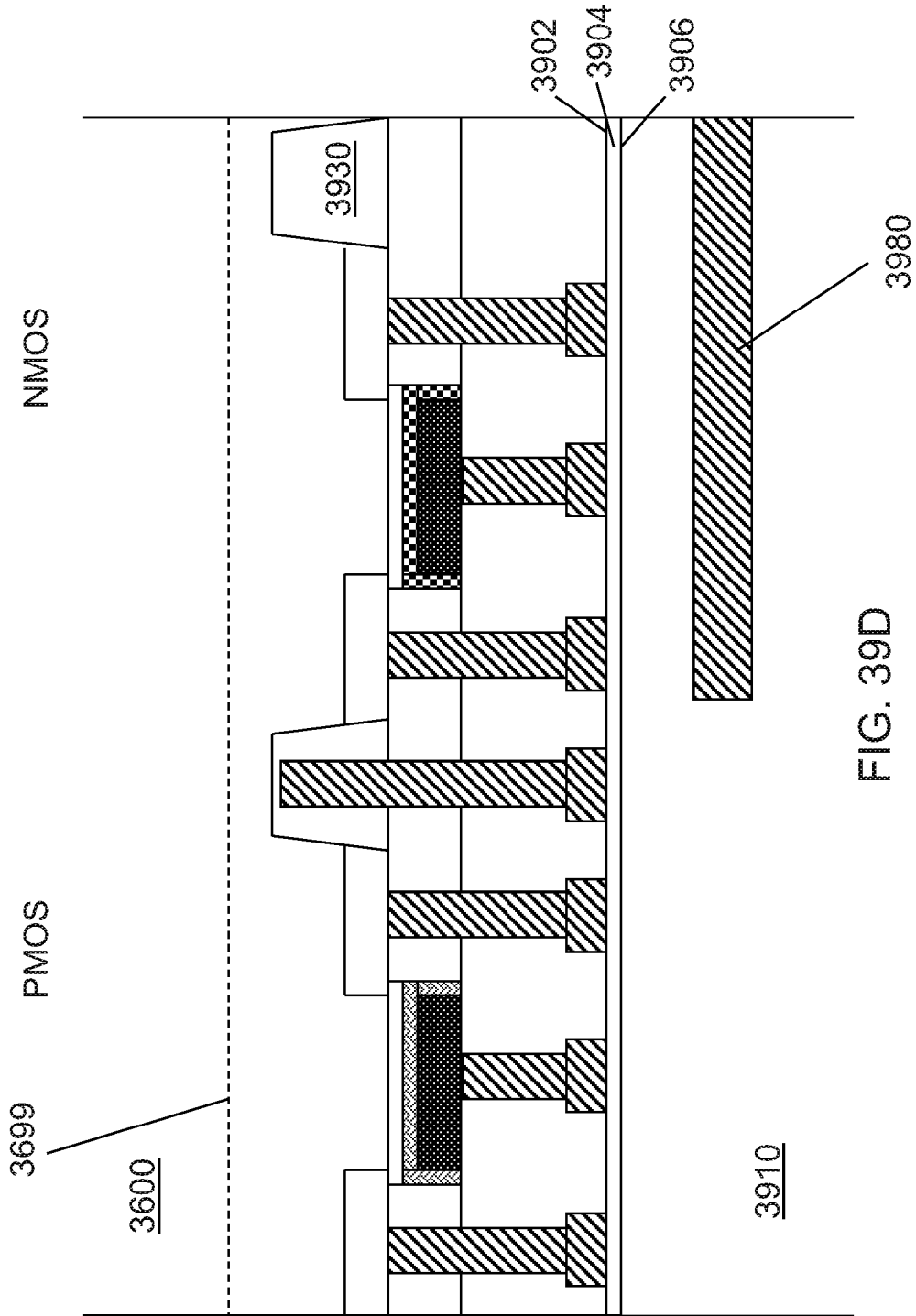


FIG. 39D

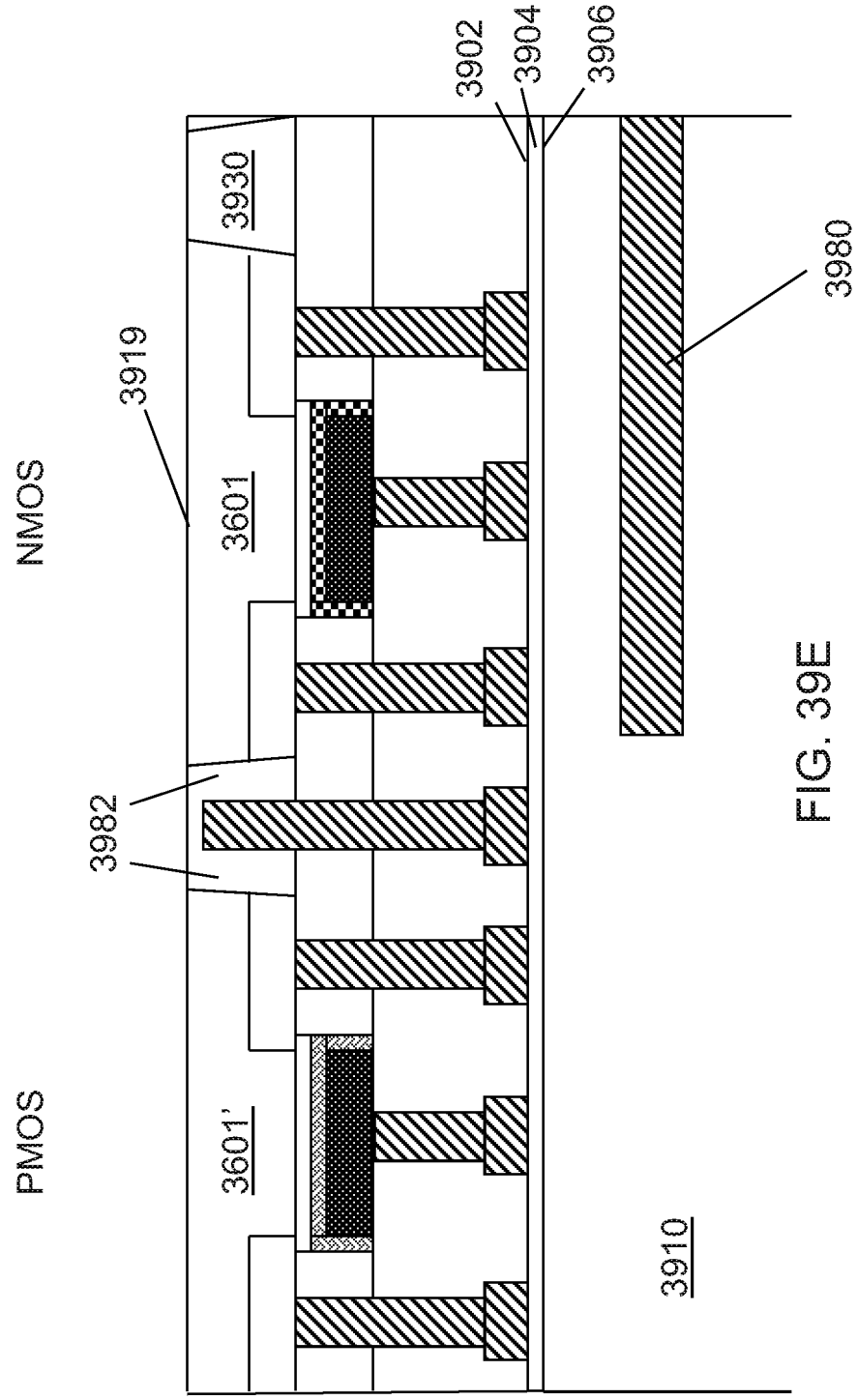


FIG. 39E

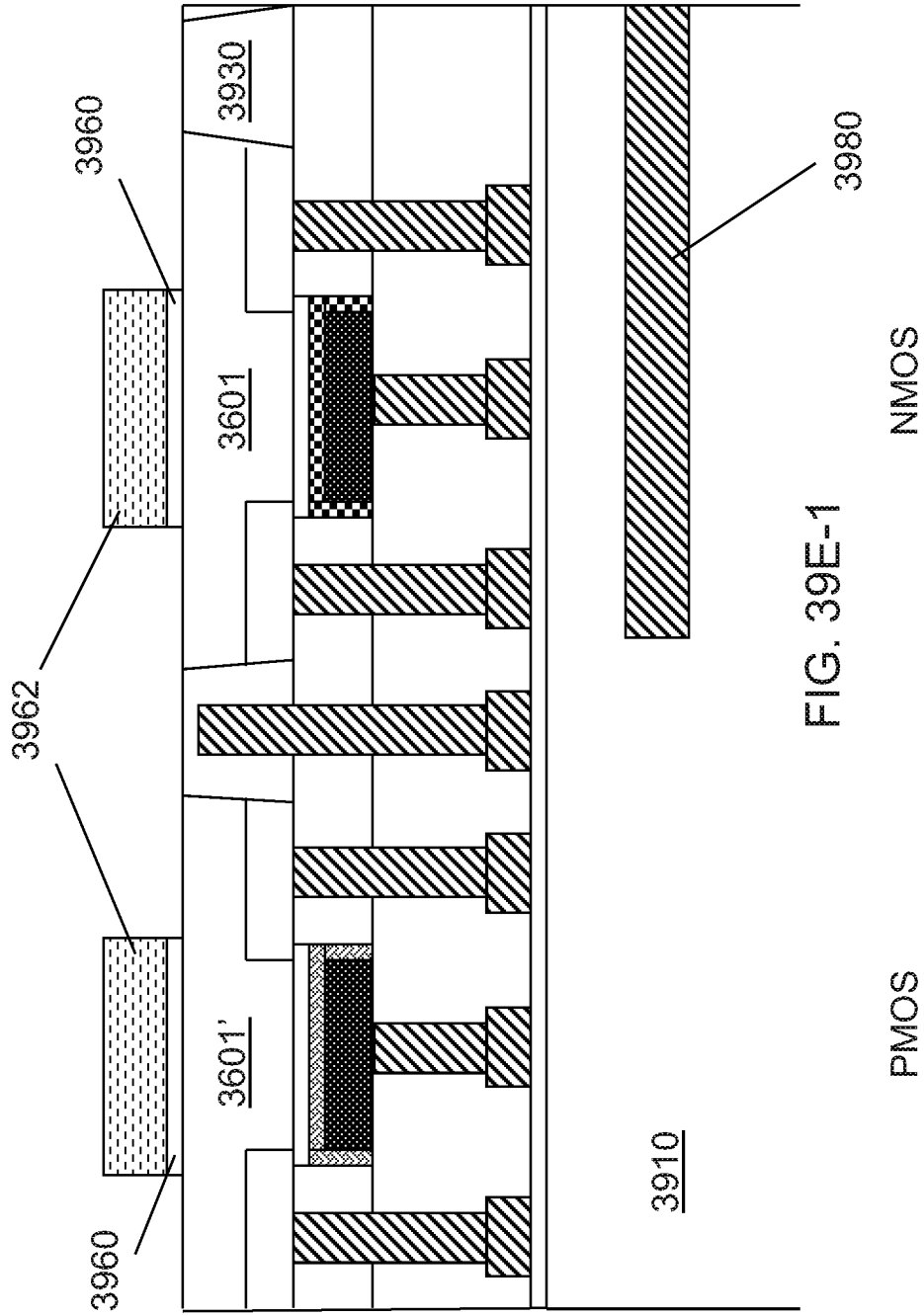


FIG. 39E-1

PMOS

NMOS

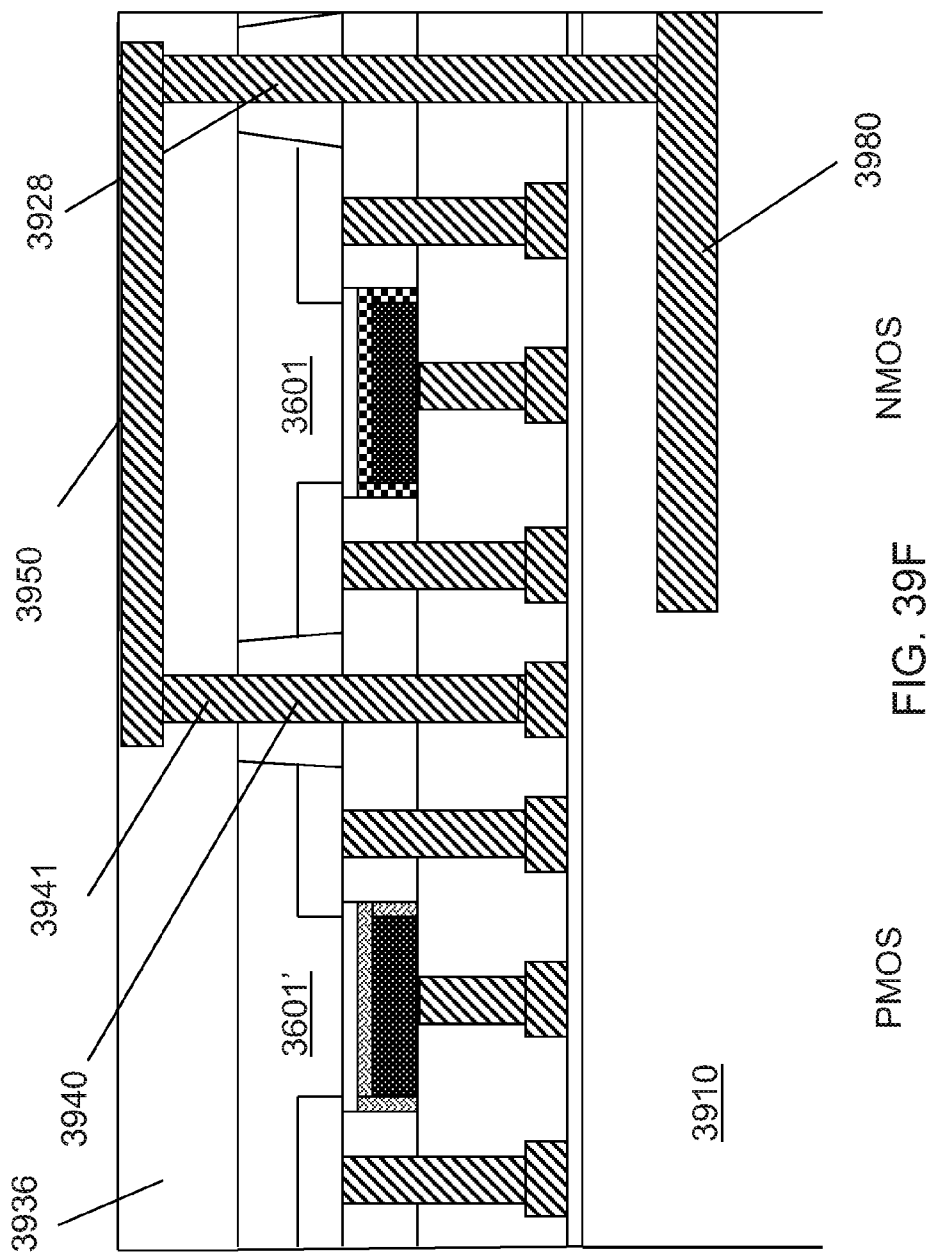


FIG. 39F

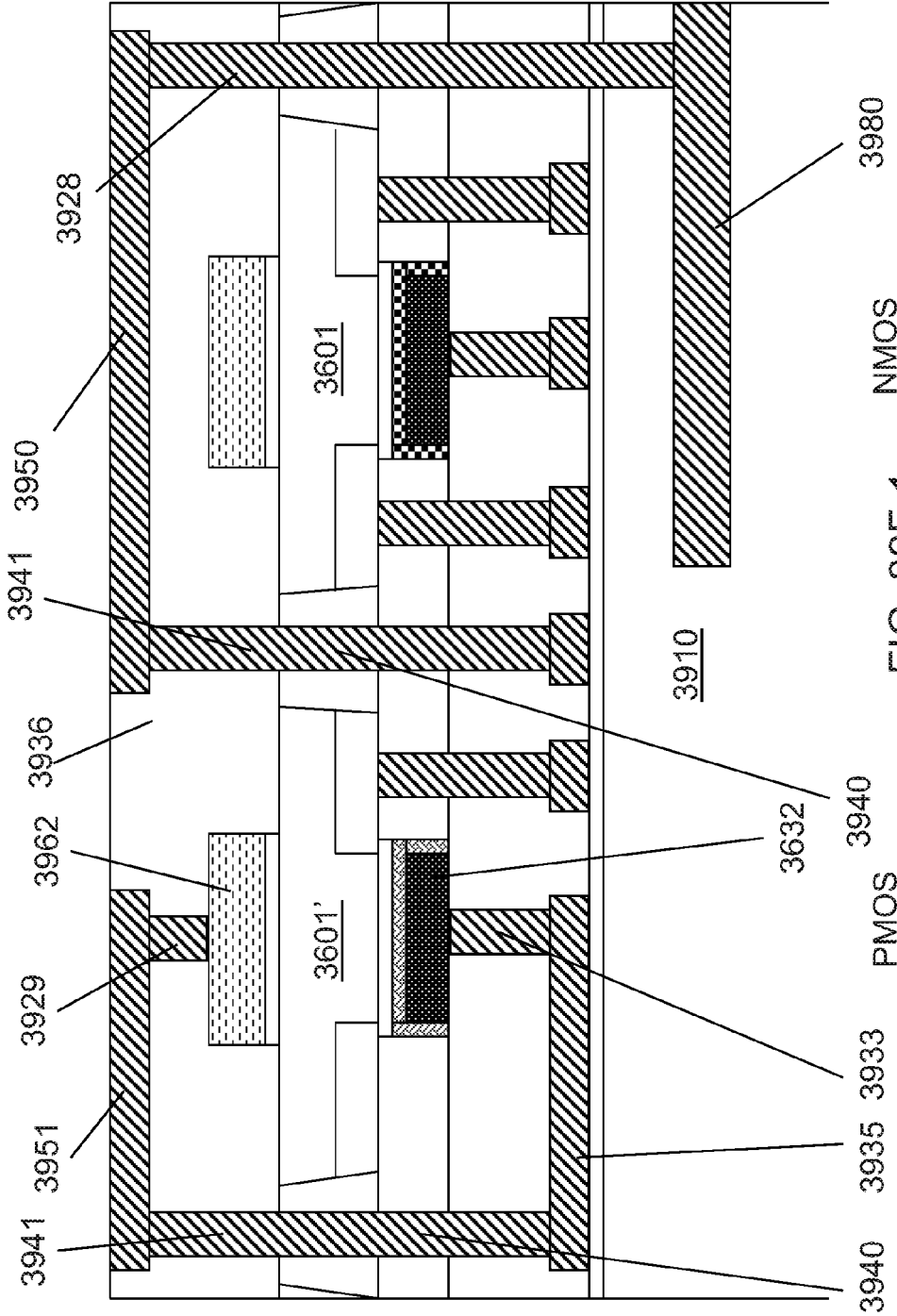


FIG. 39F-1

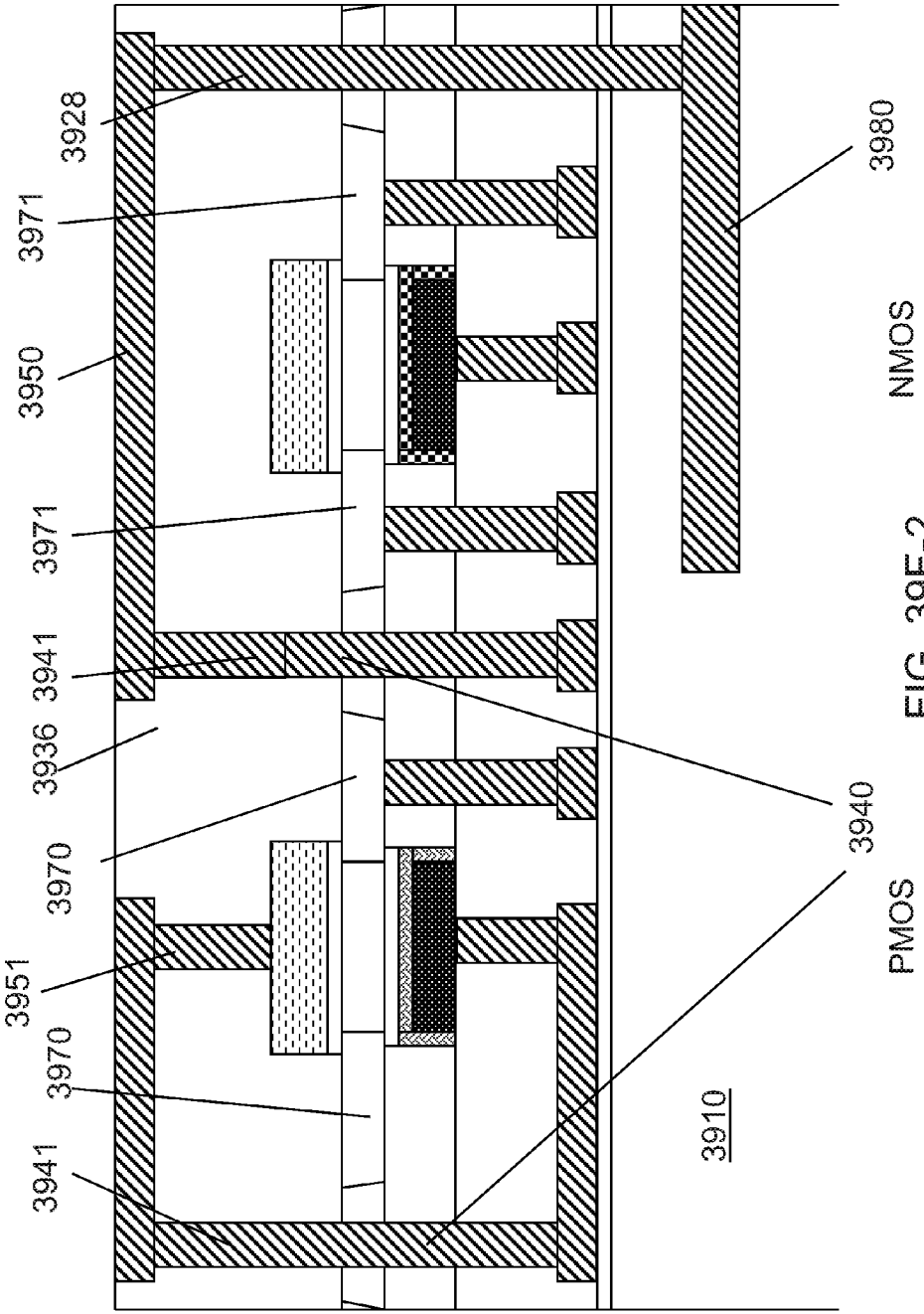


FIG. 39F-2

FIG. 40A

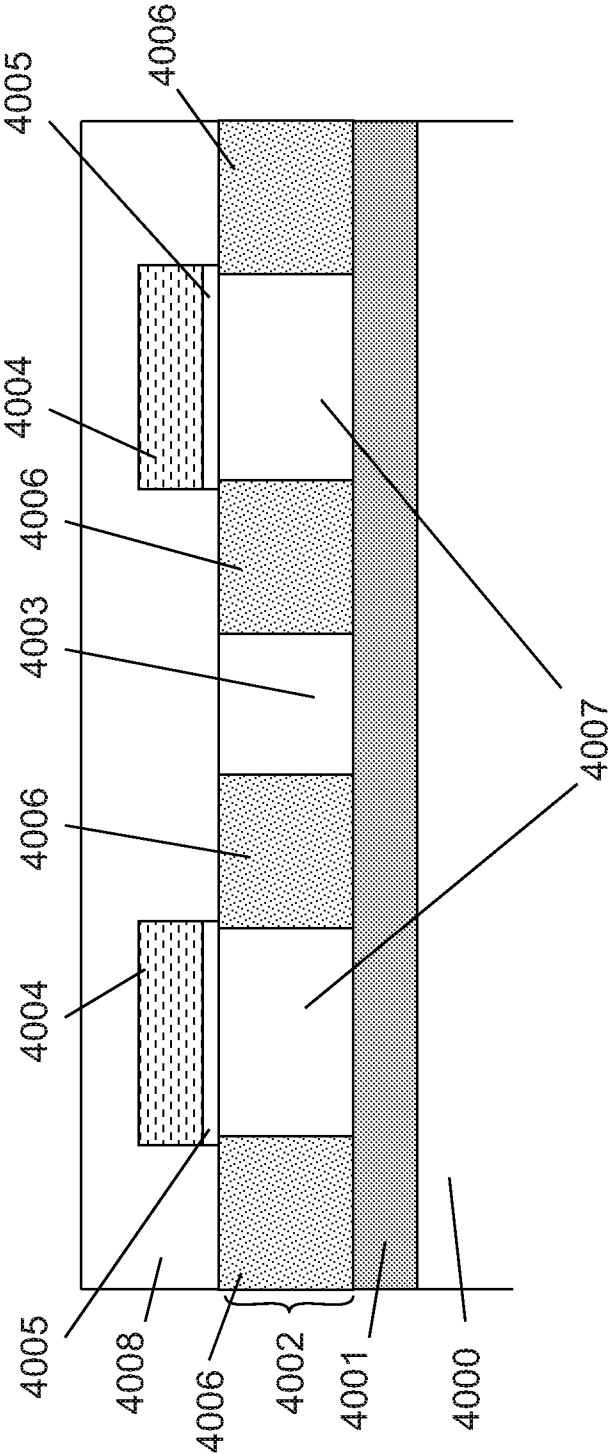




FIG. 40B

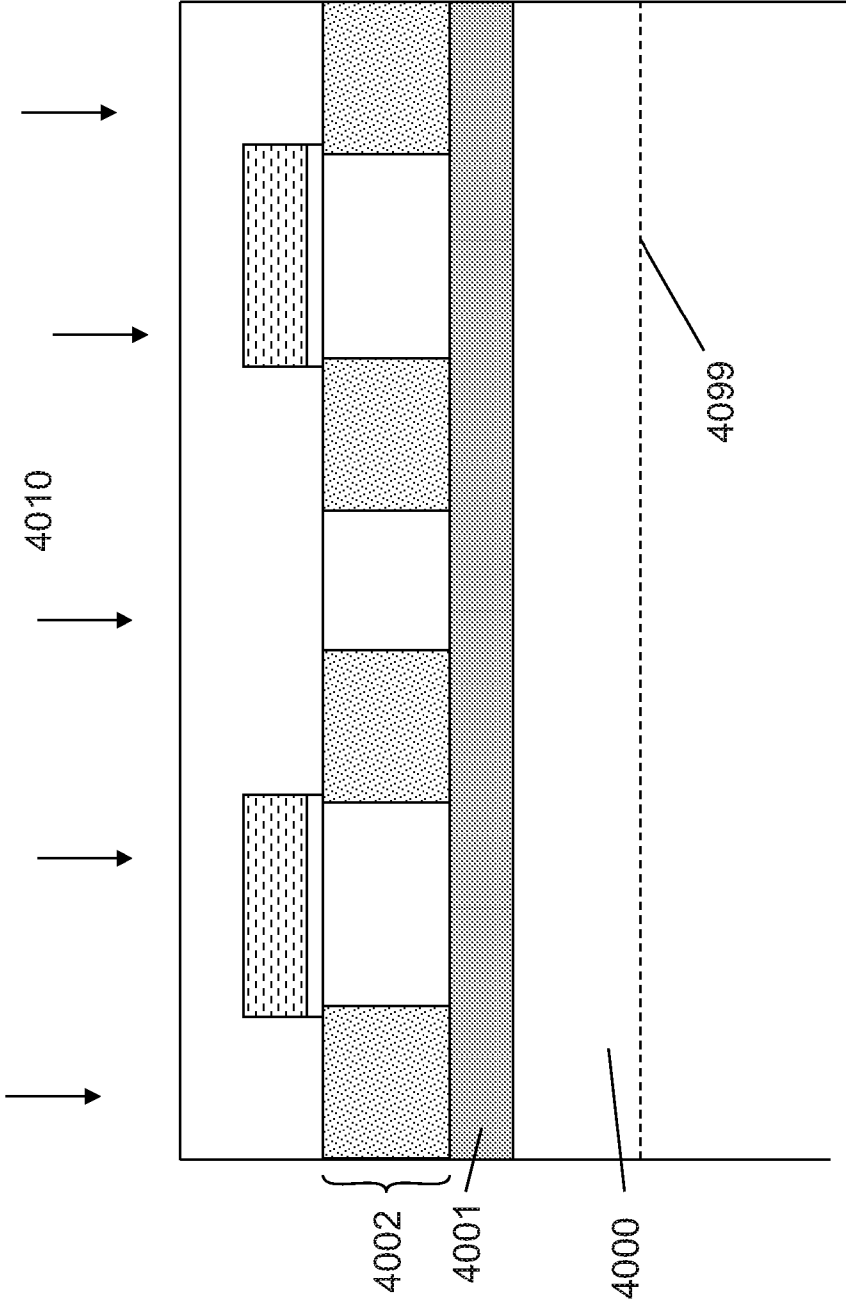


FIG. 400C

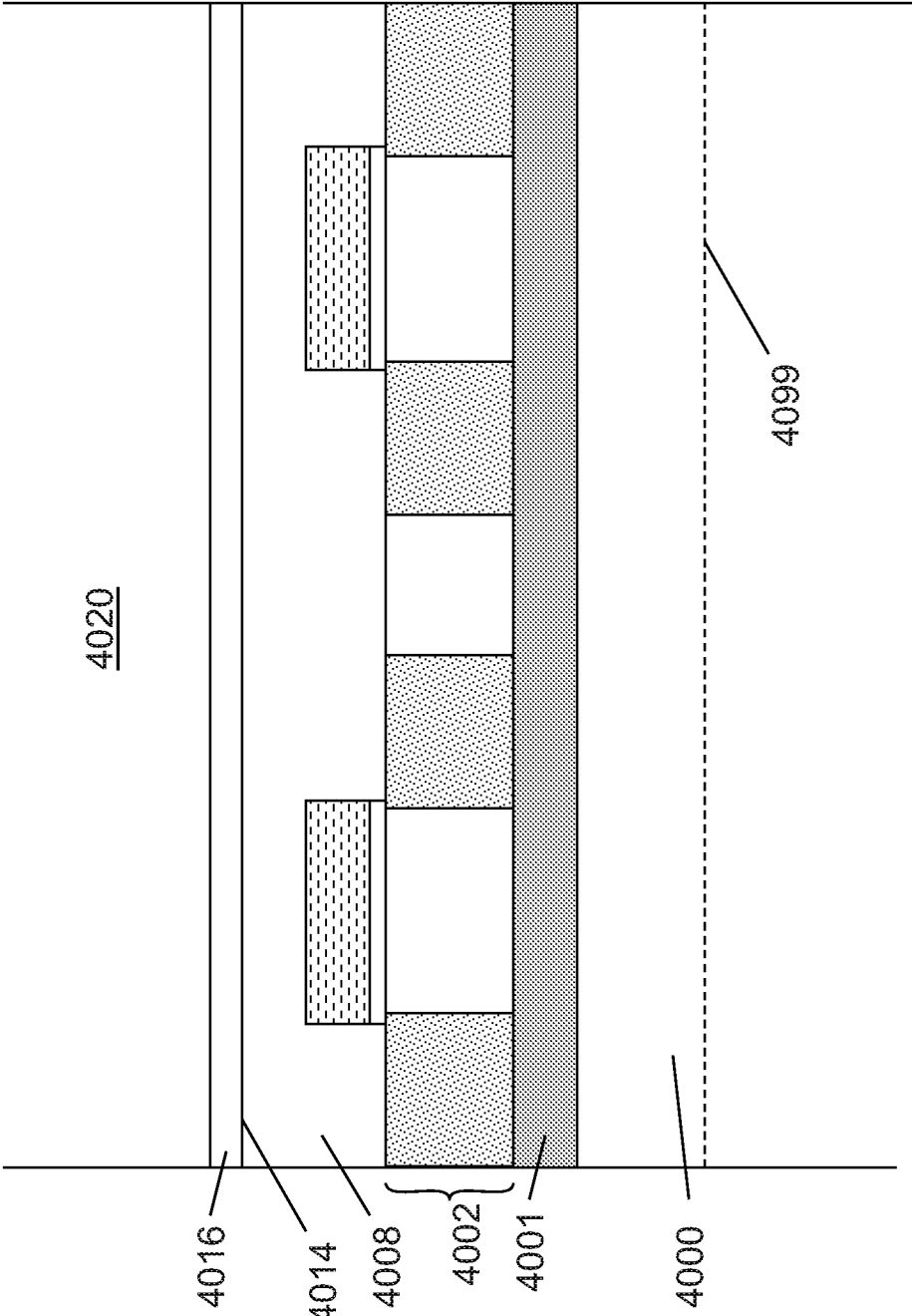
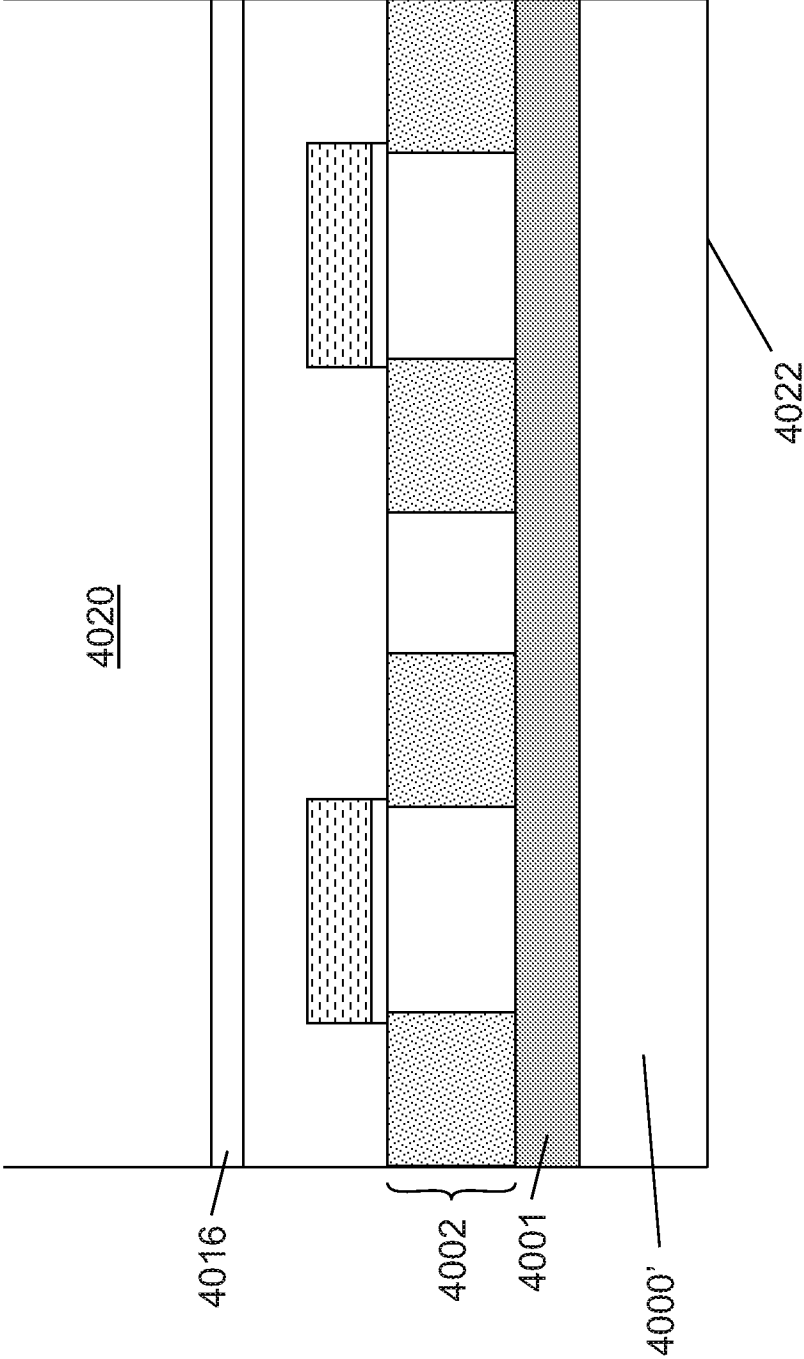


FIG. 40D



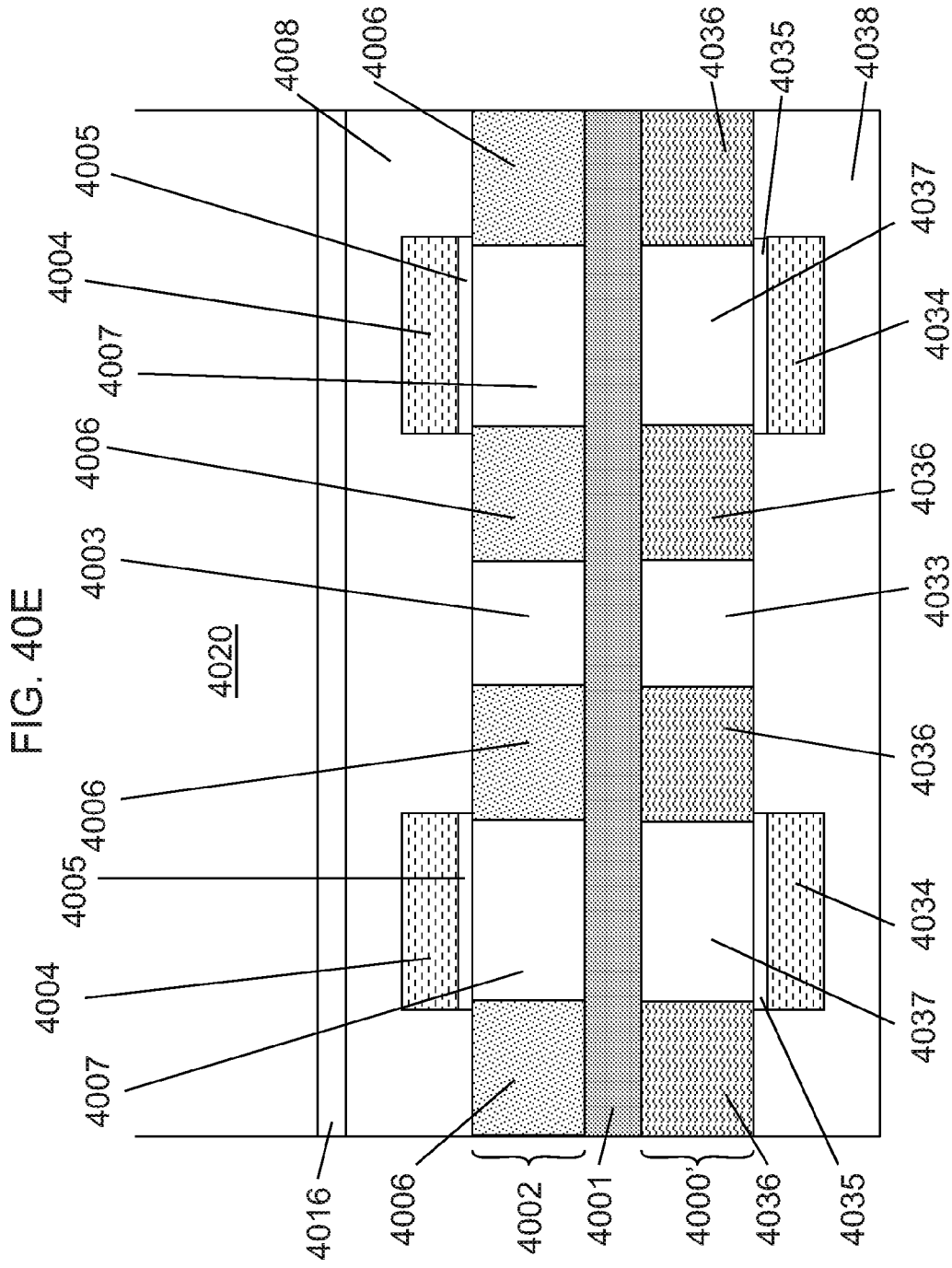


FIG. 40F

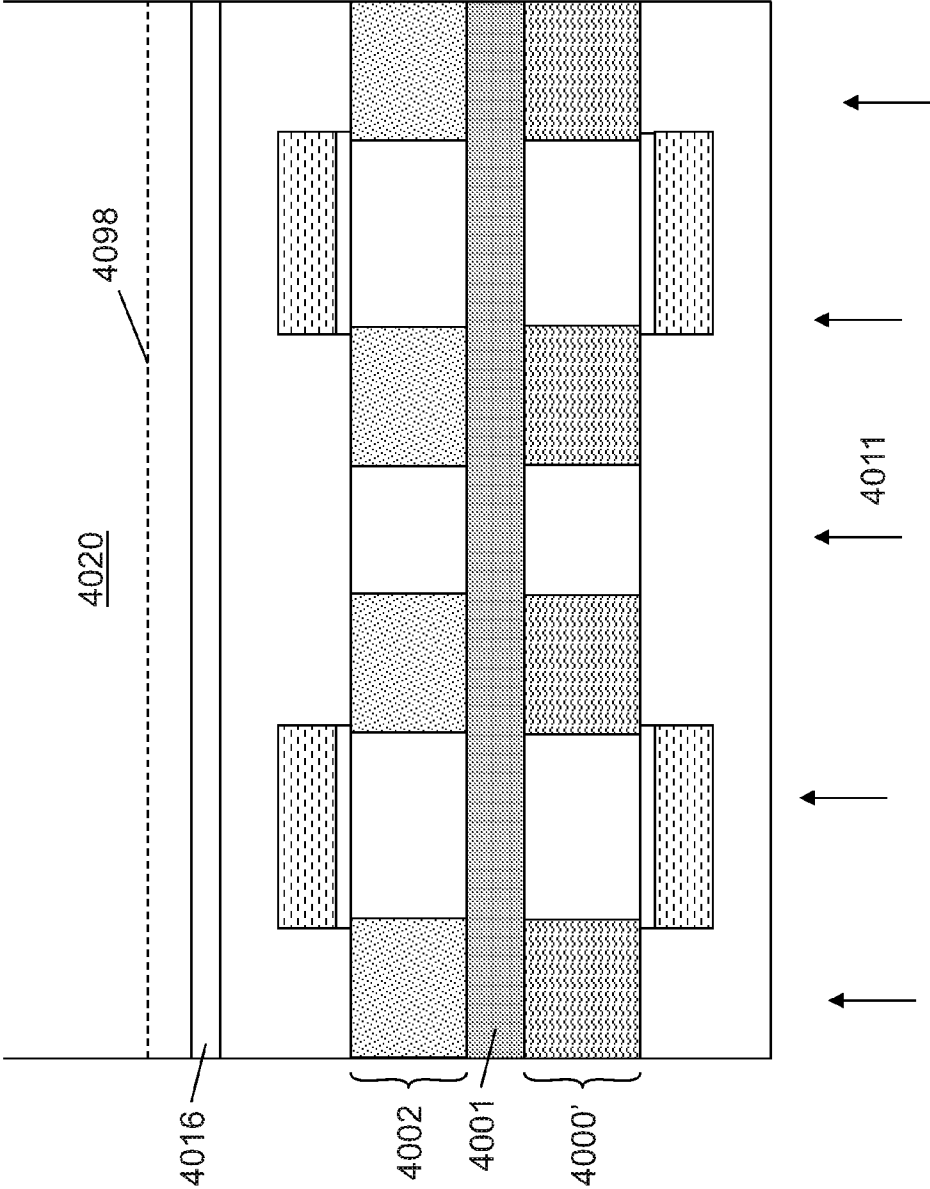
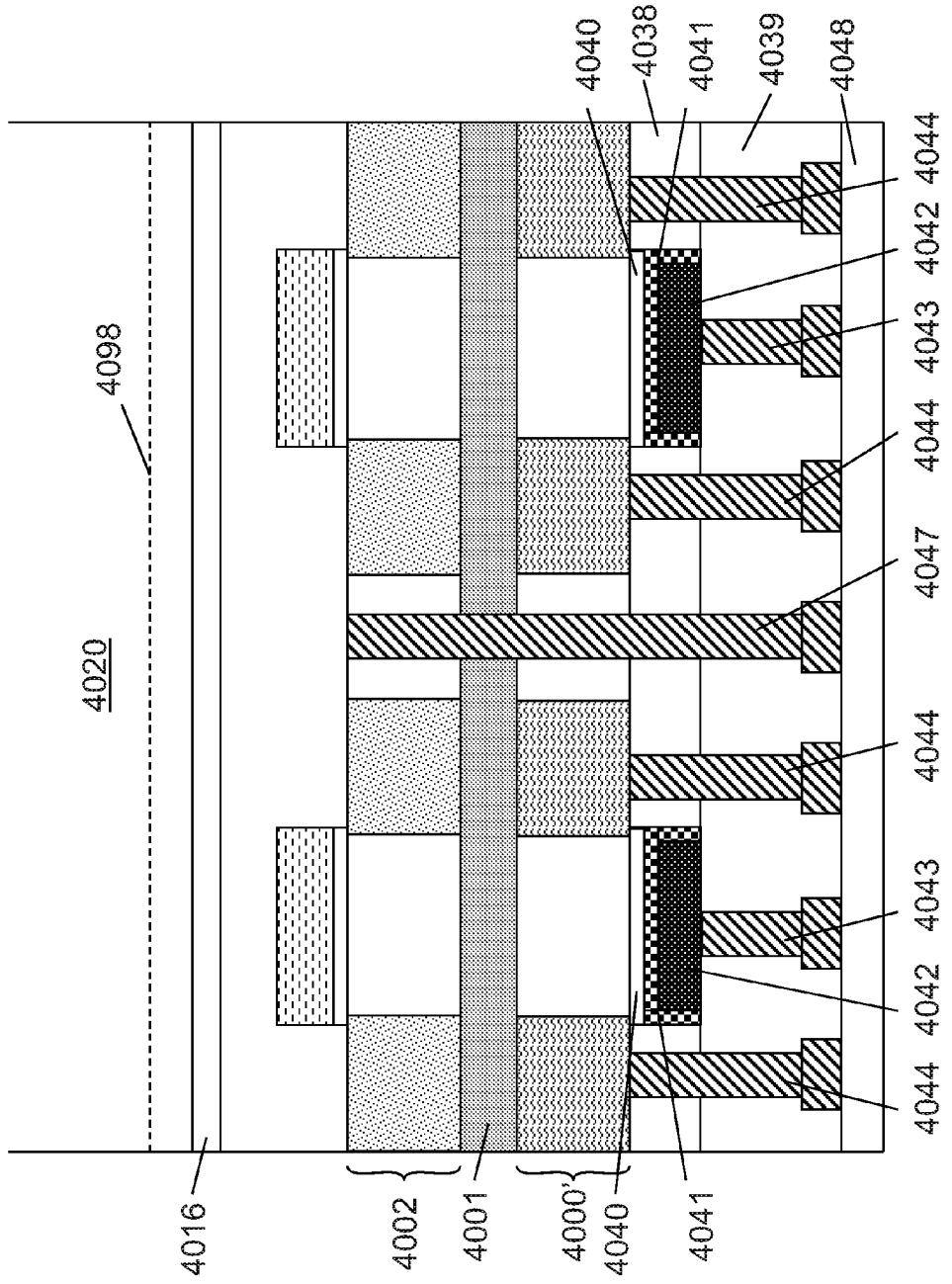


FIG. 40G



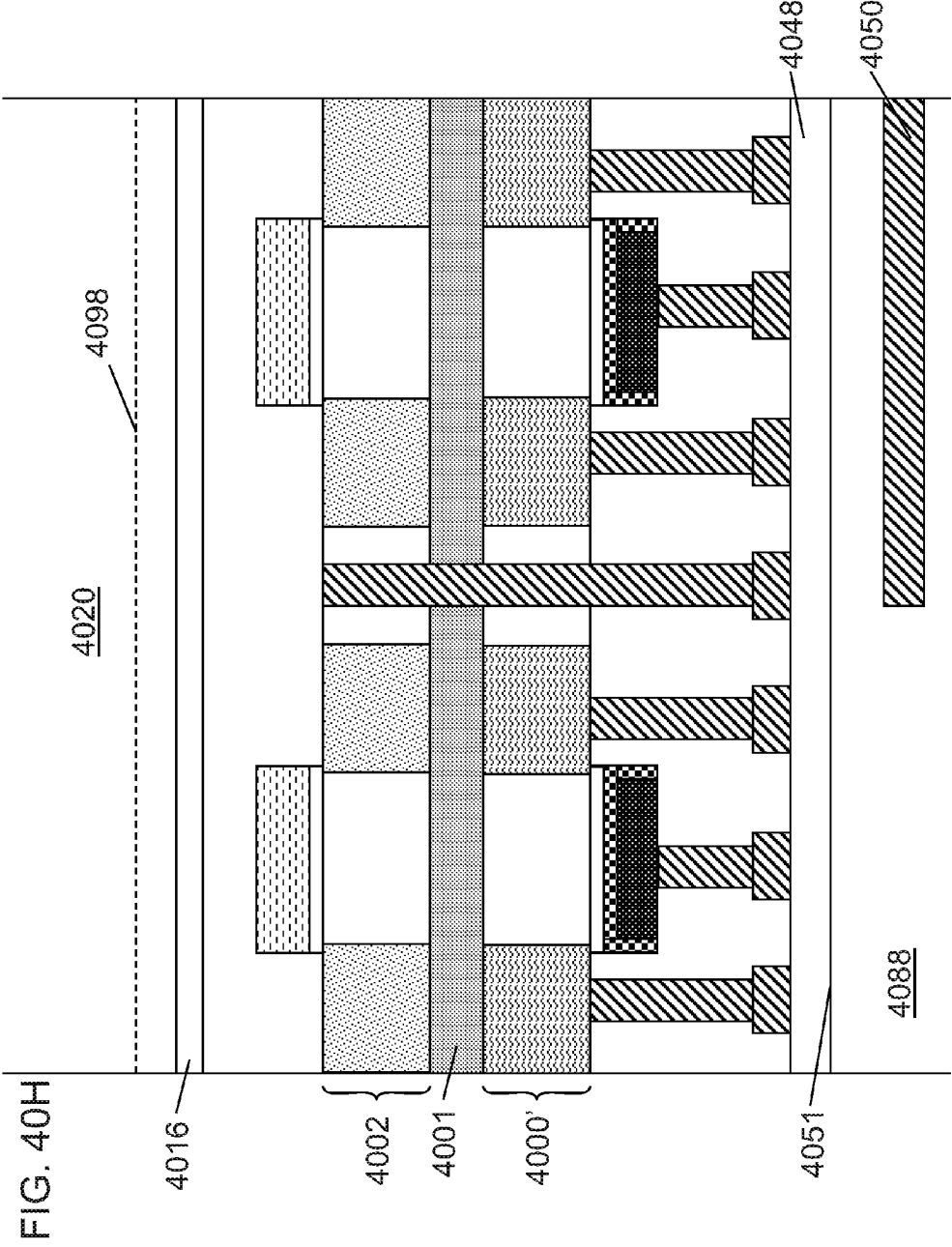
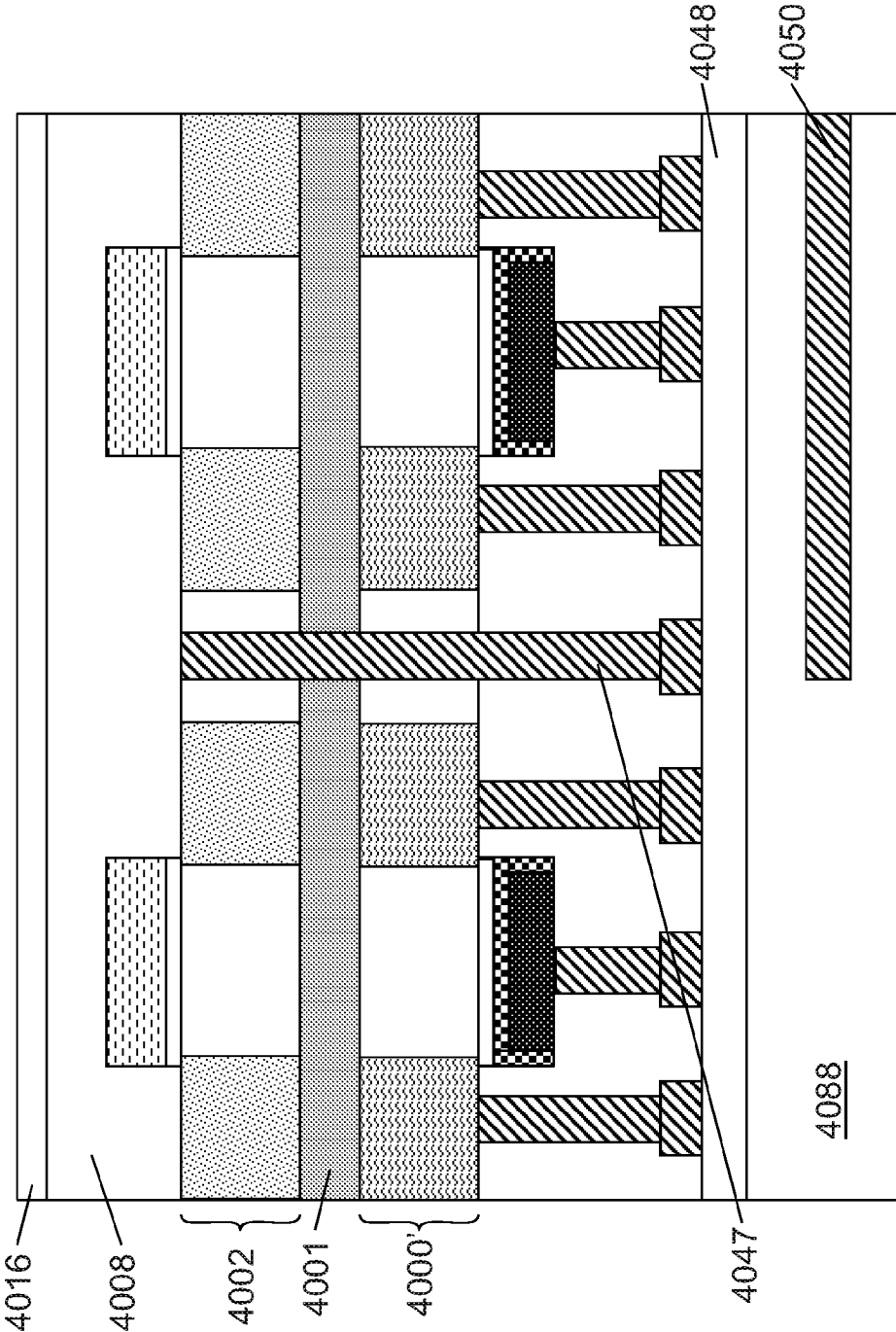
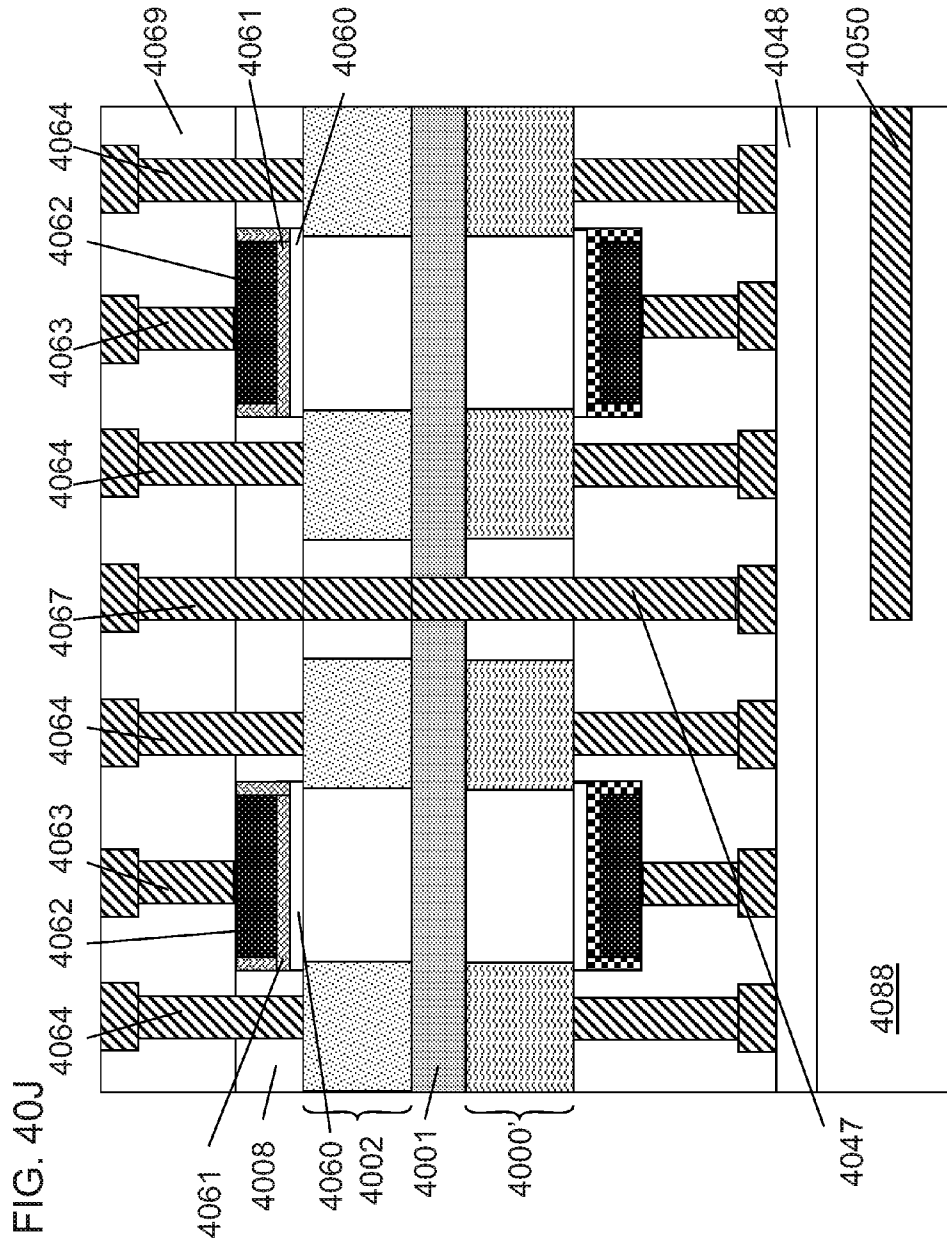


FIG. 40H

FIG. 40I







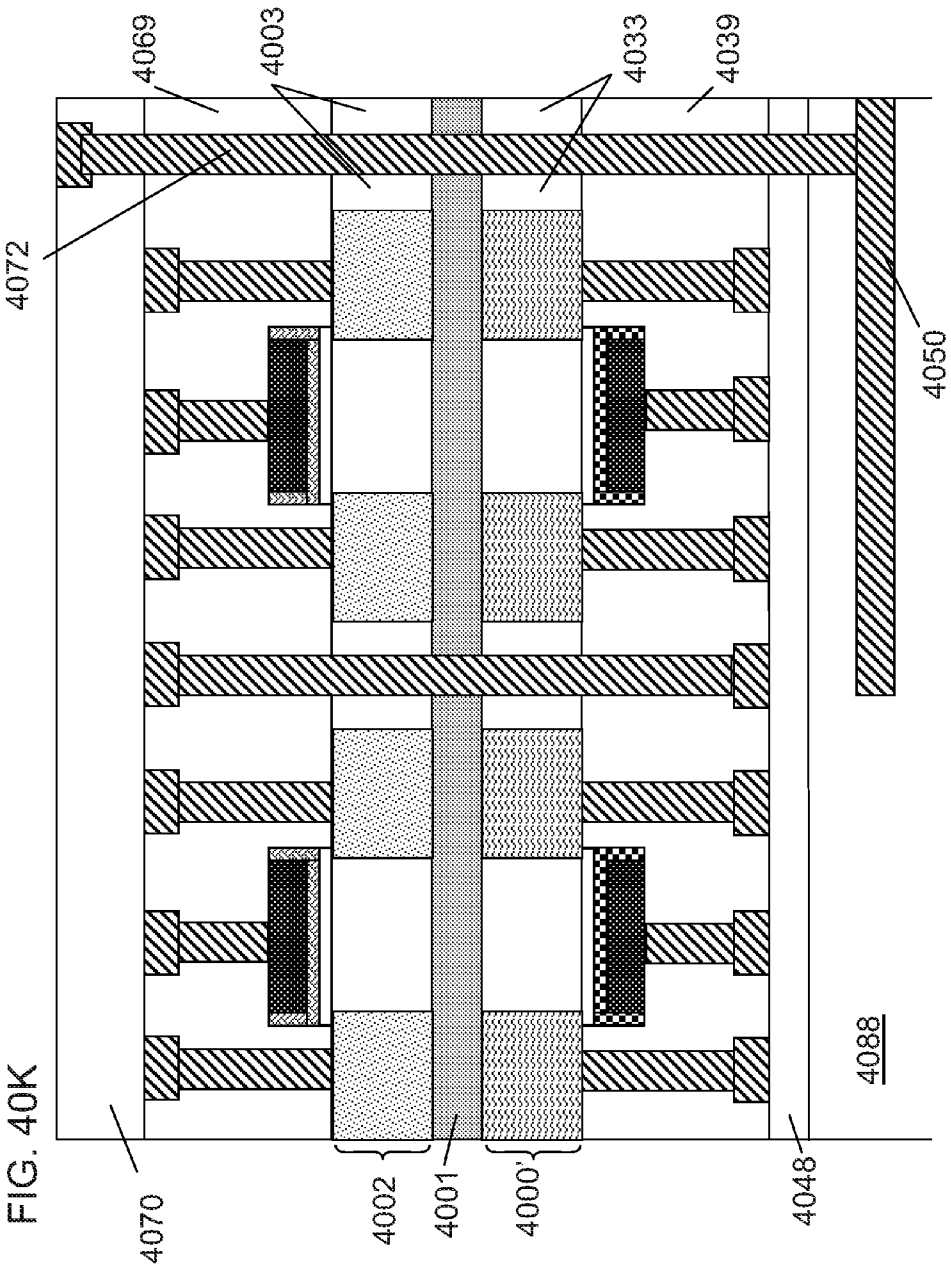


FIG. 40K

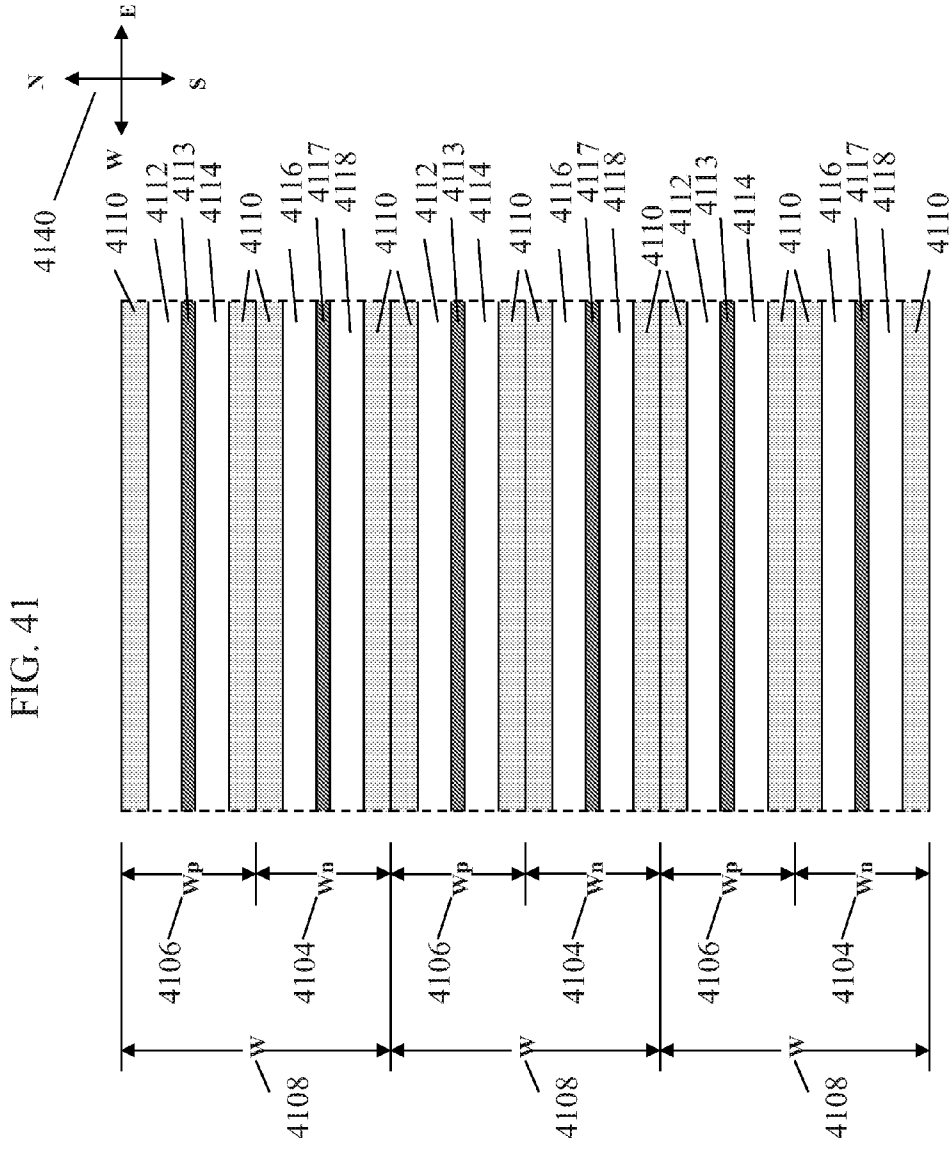
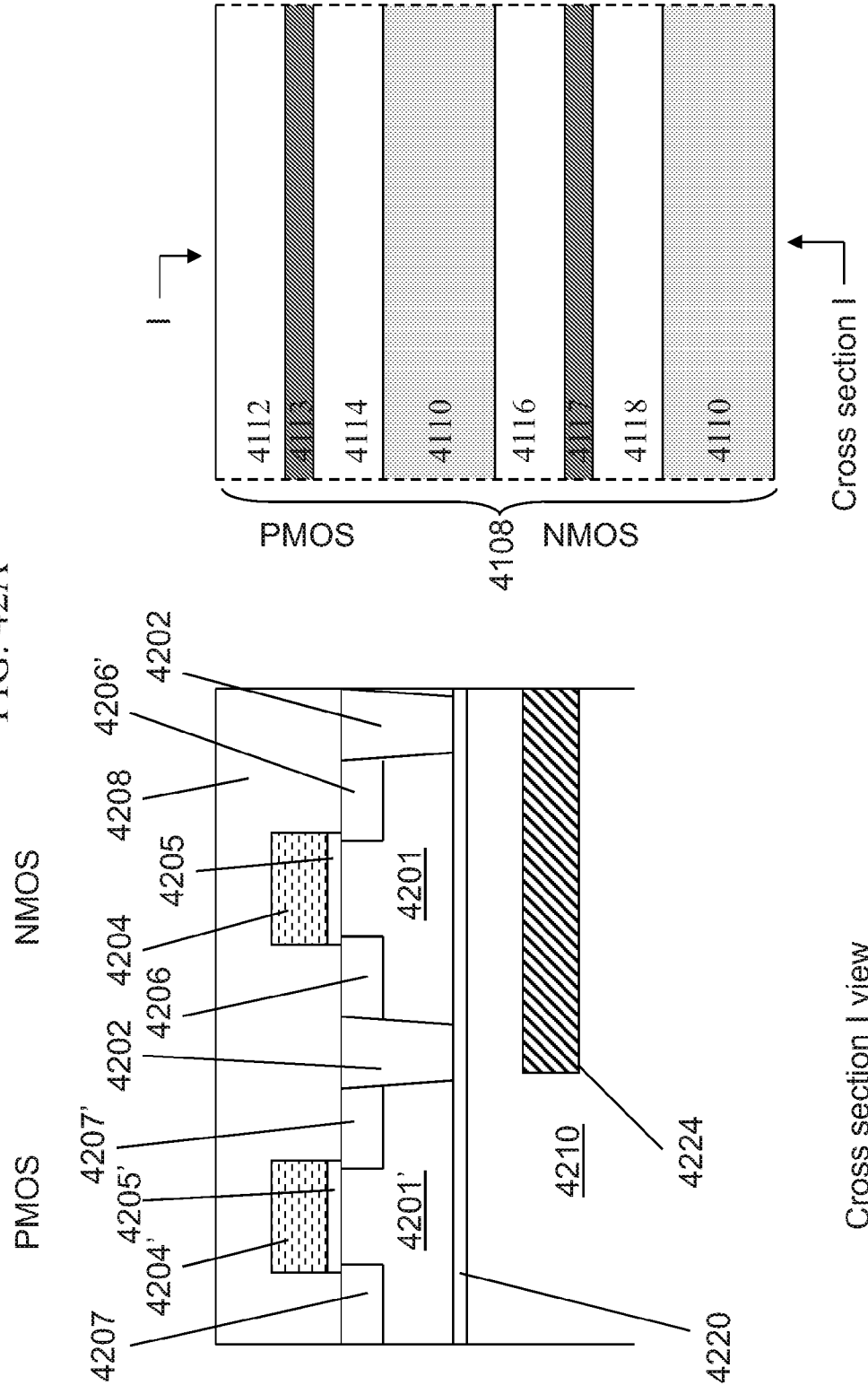


FIG. 42A



Cross section I view

Cross section I

FIG. 42B

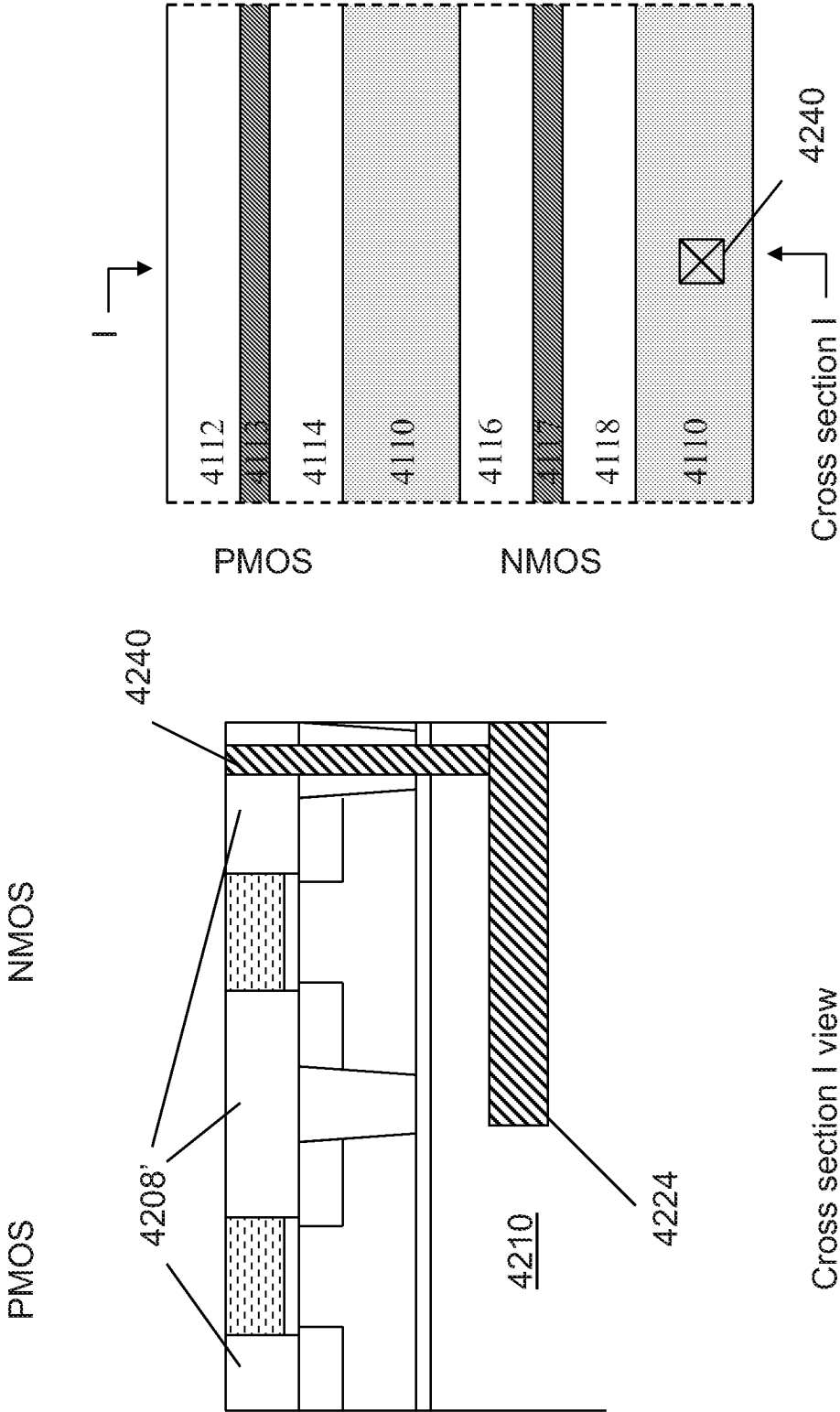


FIG. 42C

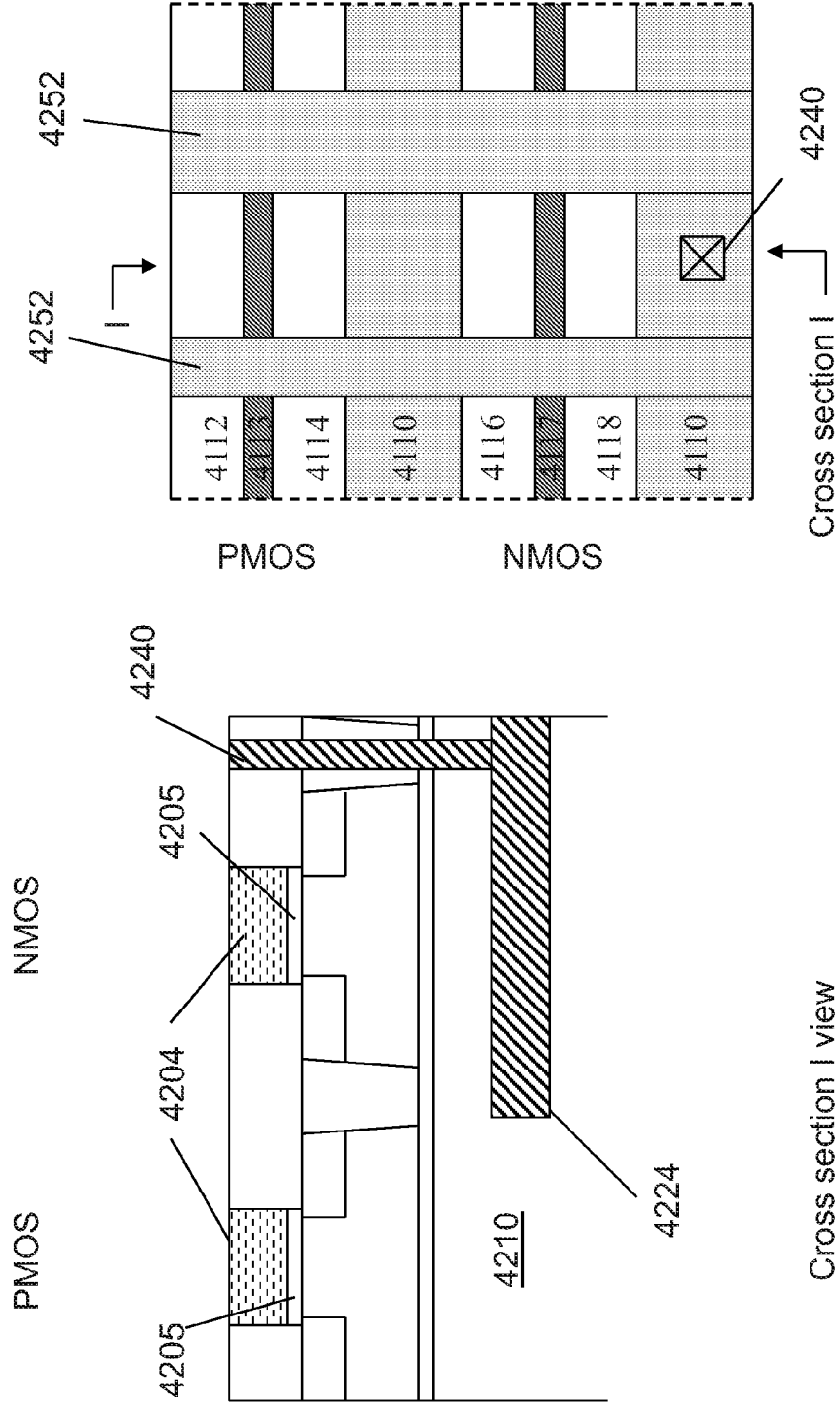
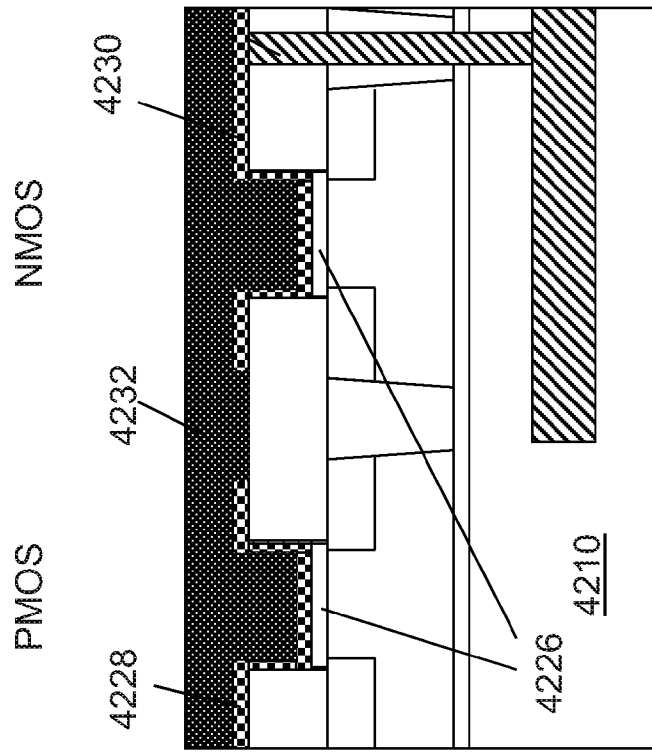
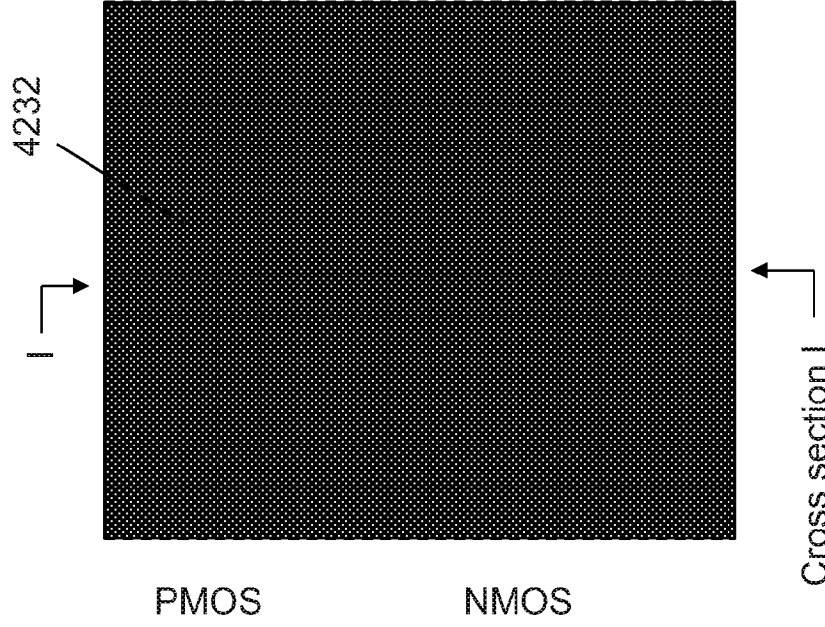


FIG. 42D



Cross section I view



Cross section I

FIG. 42E

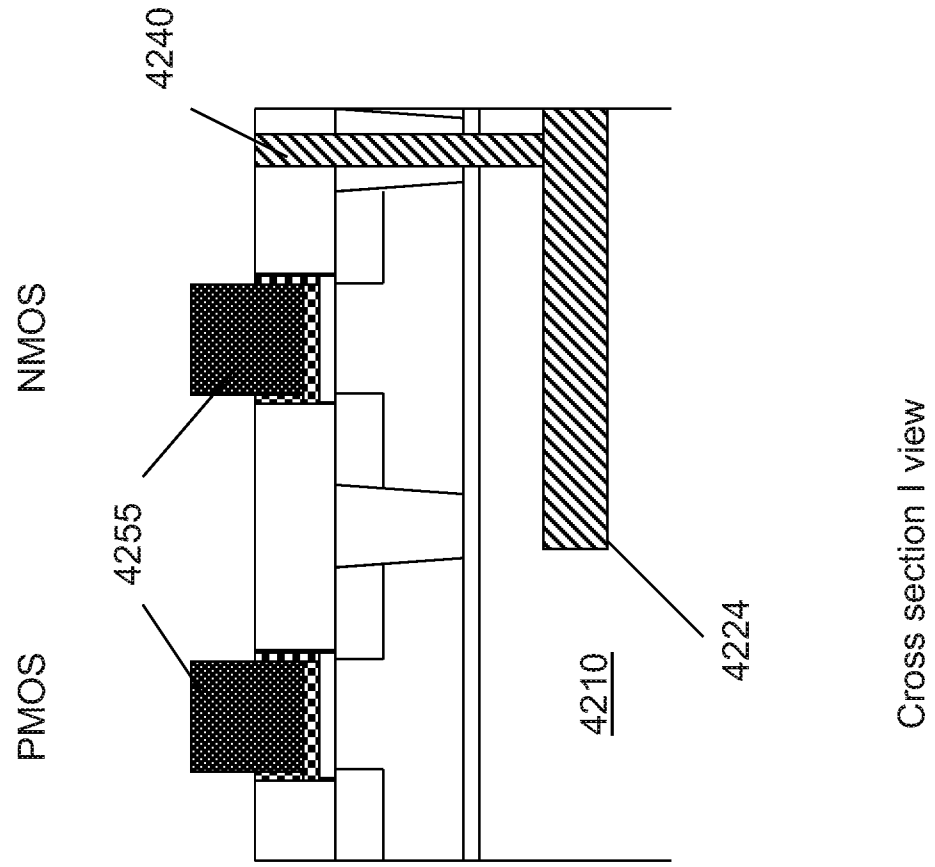
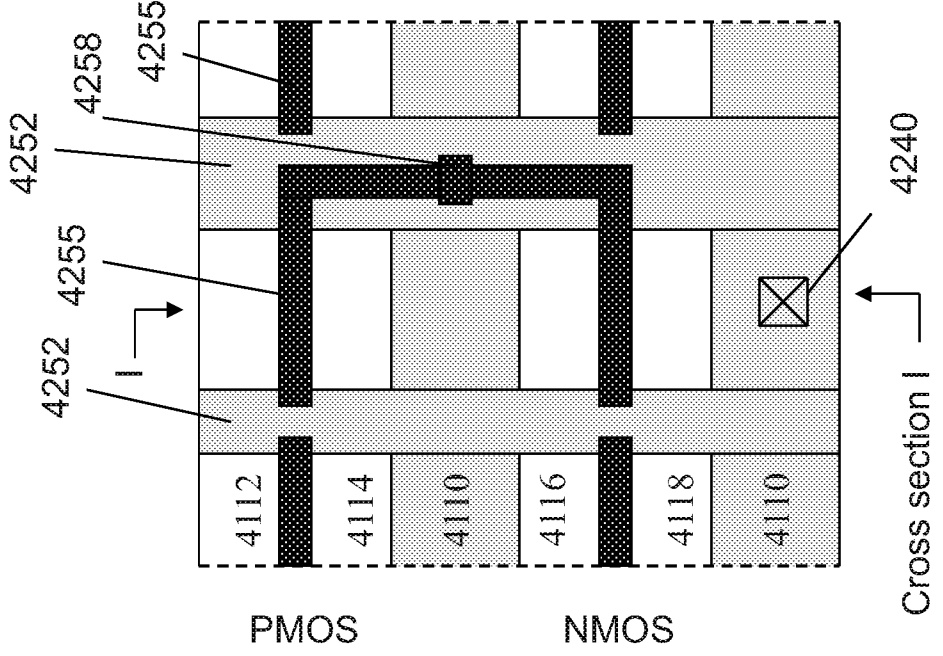
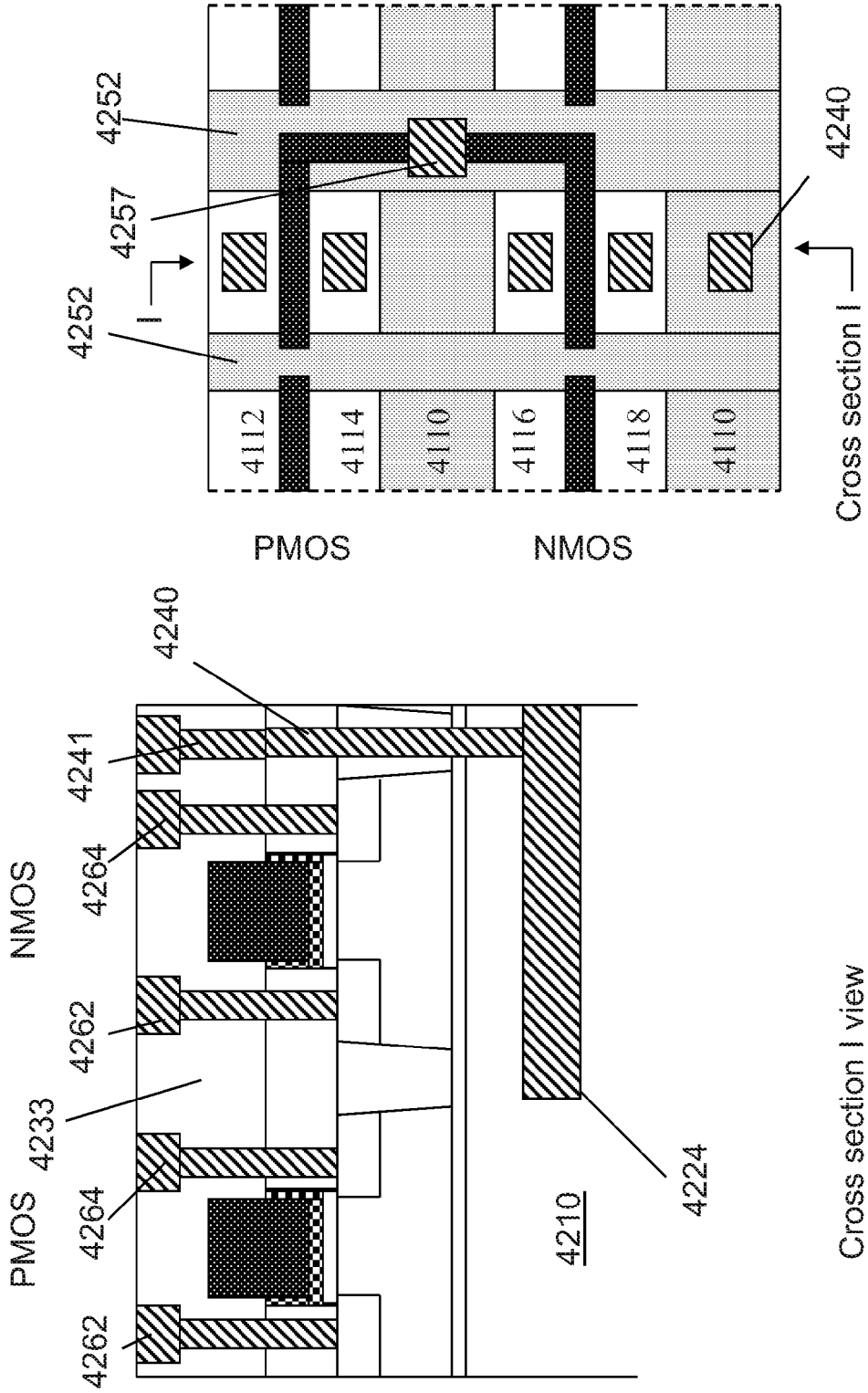
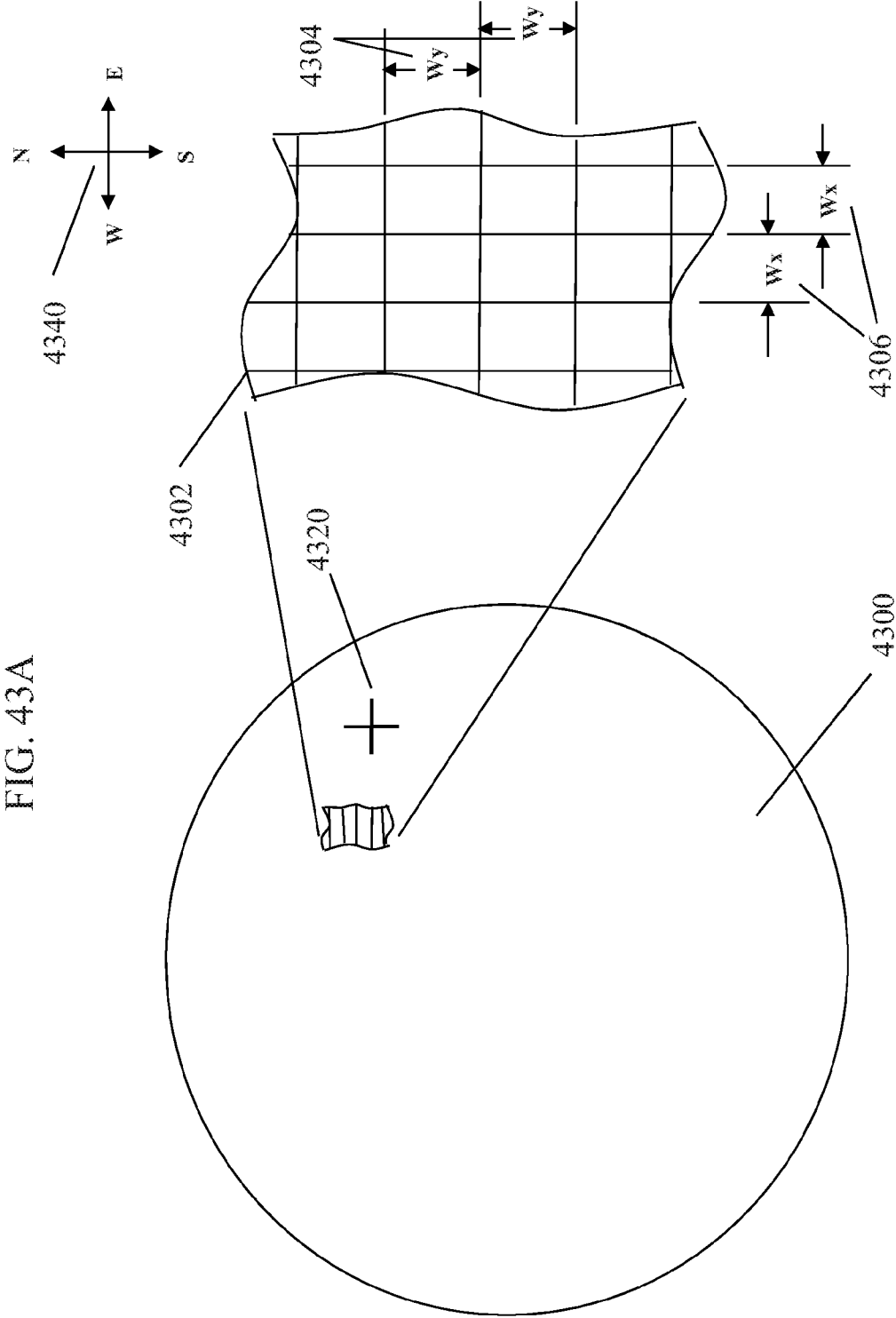




FIG. 42F





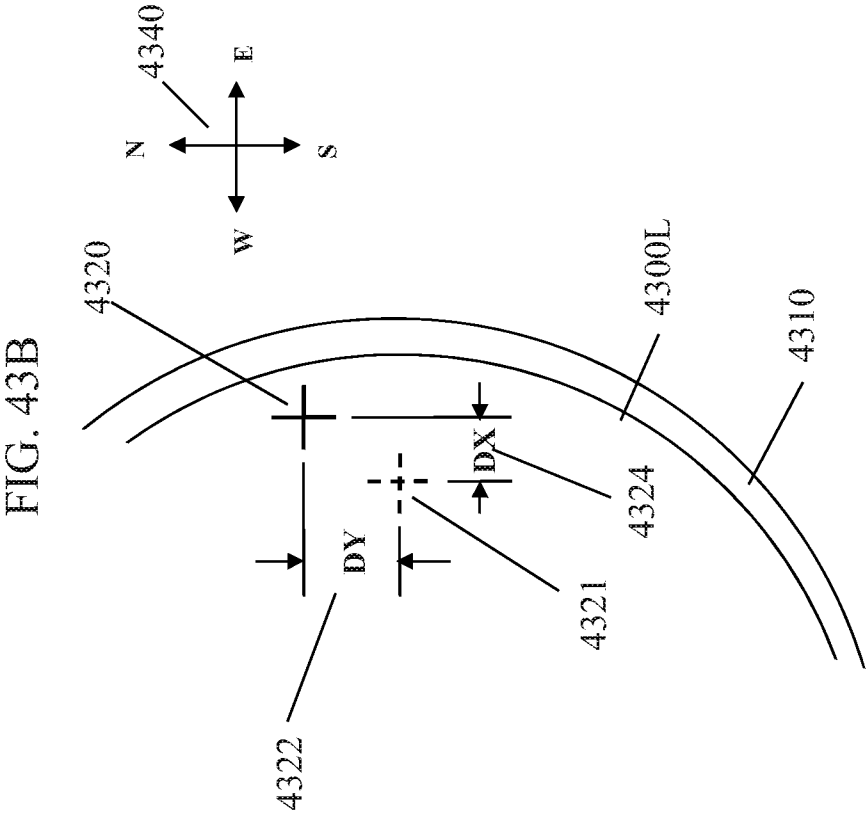




FIG. 43D

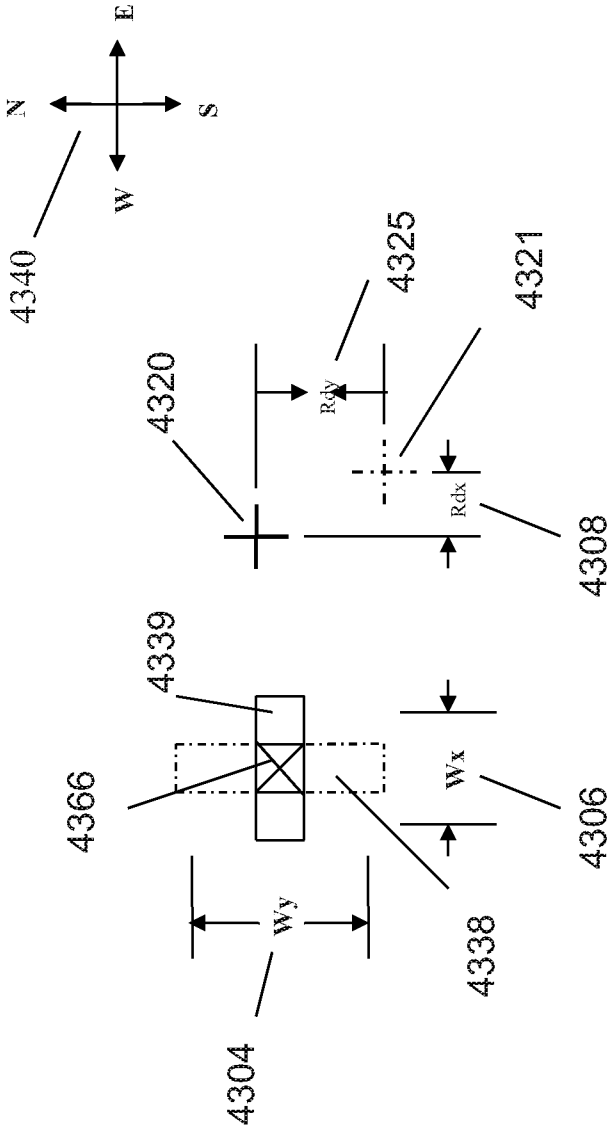


FIG. 43E

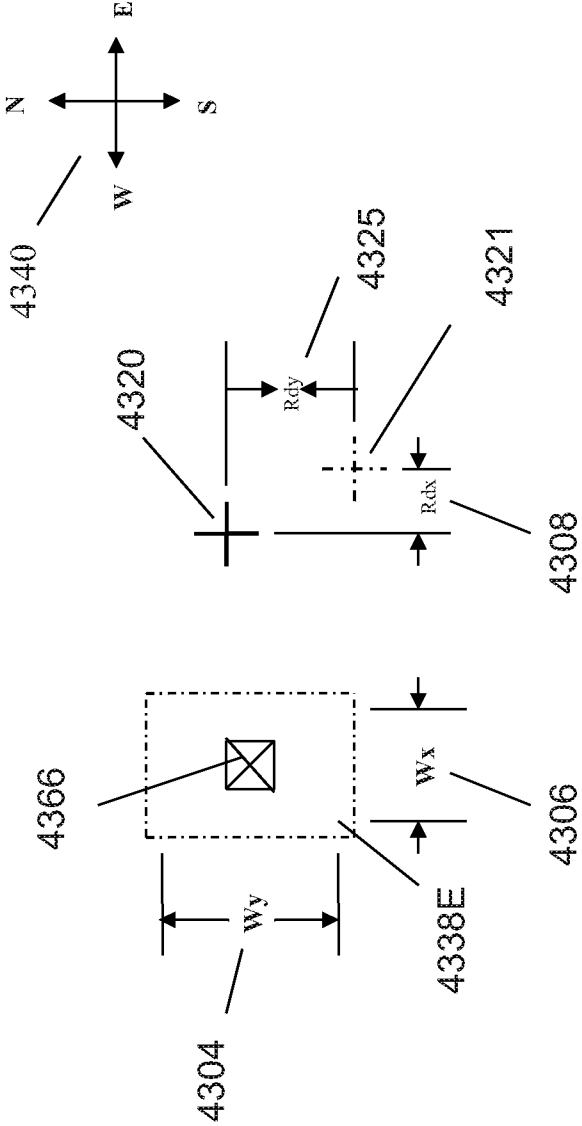
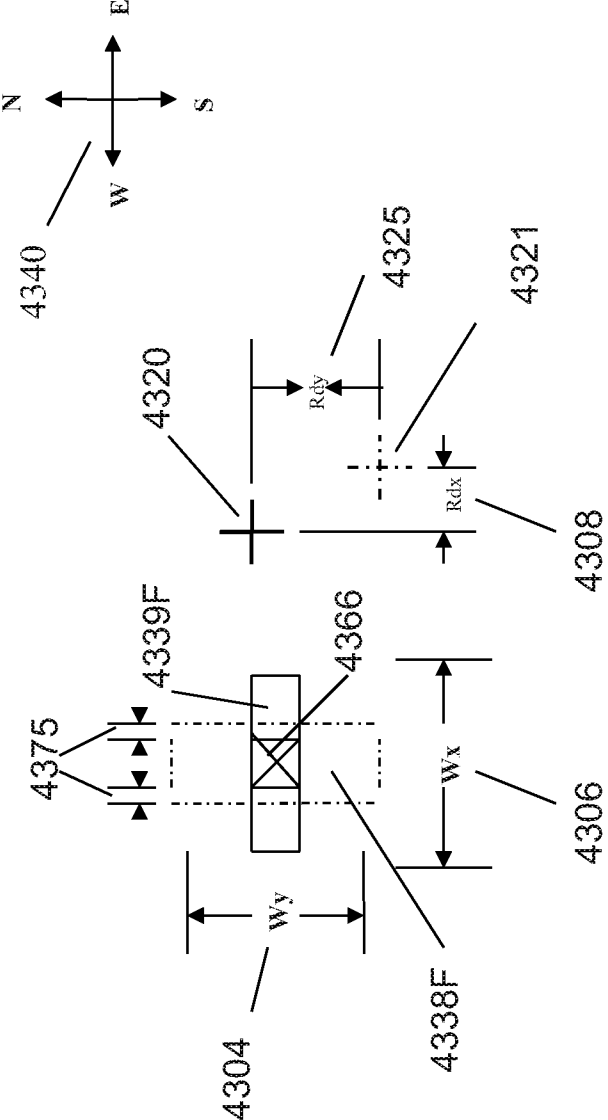
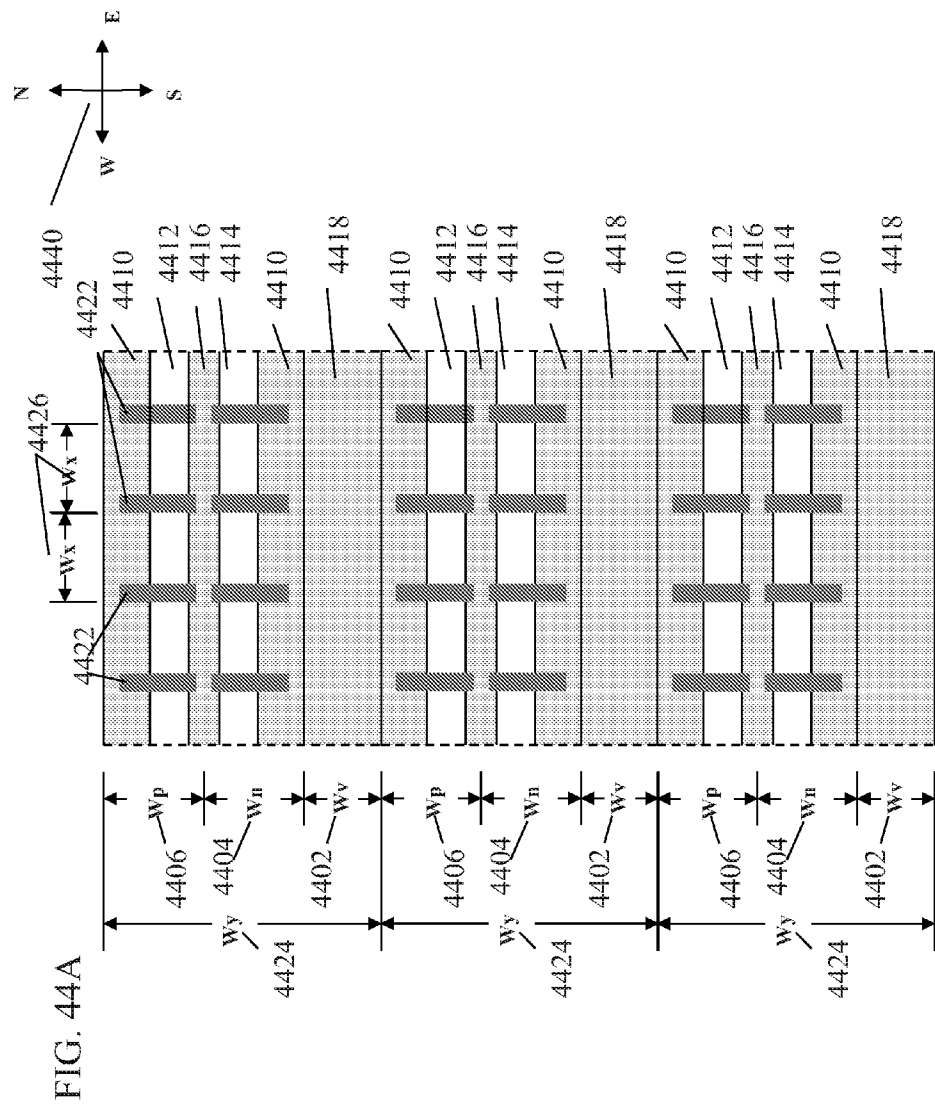


FIG. 43F









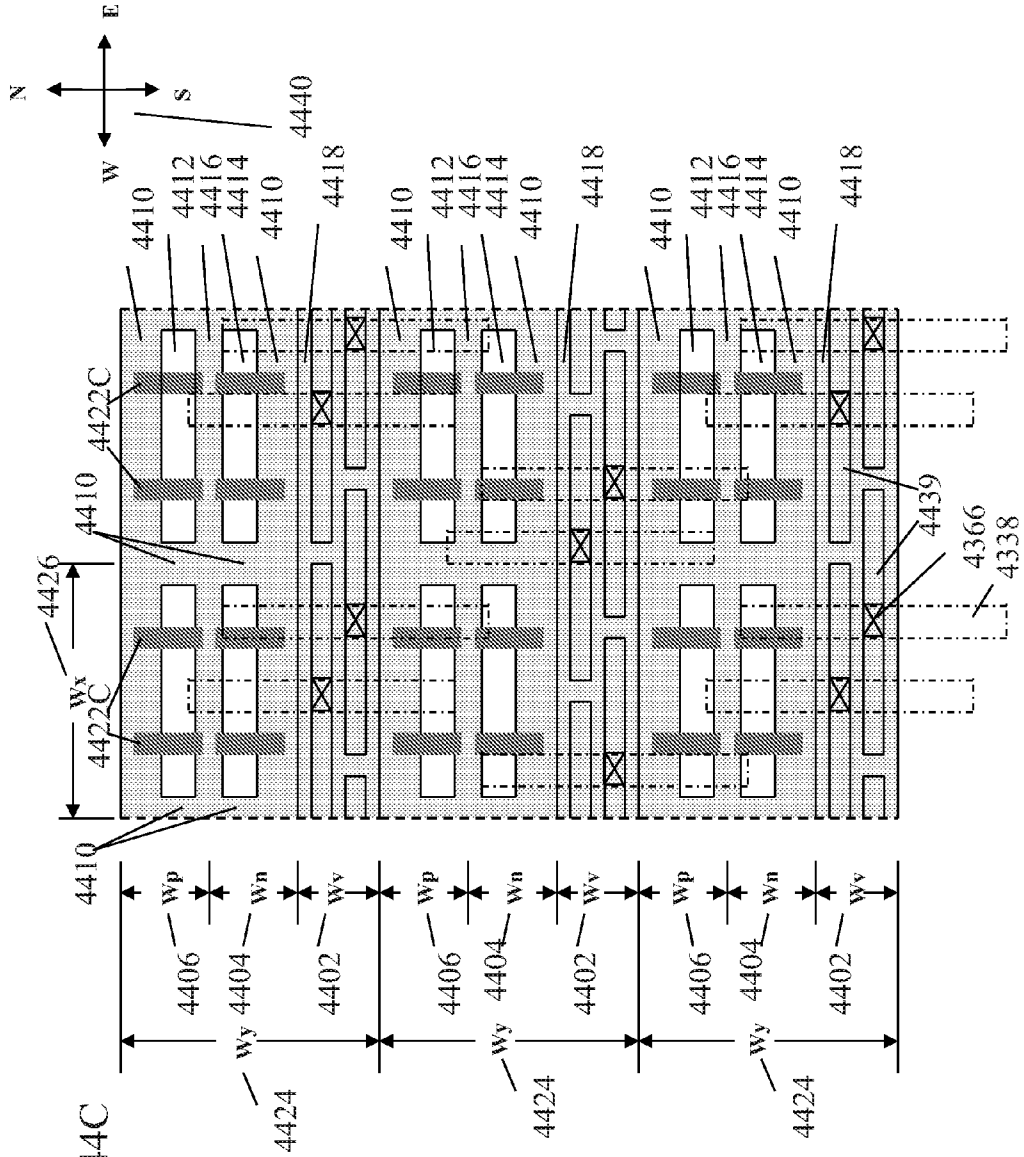




FIG. 46

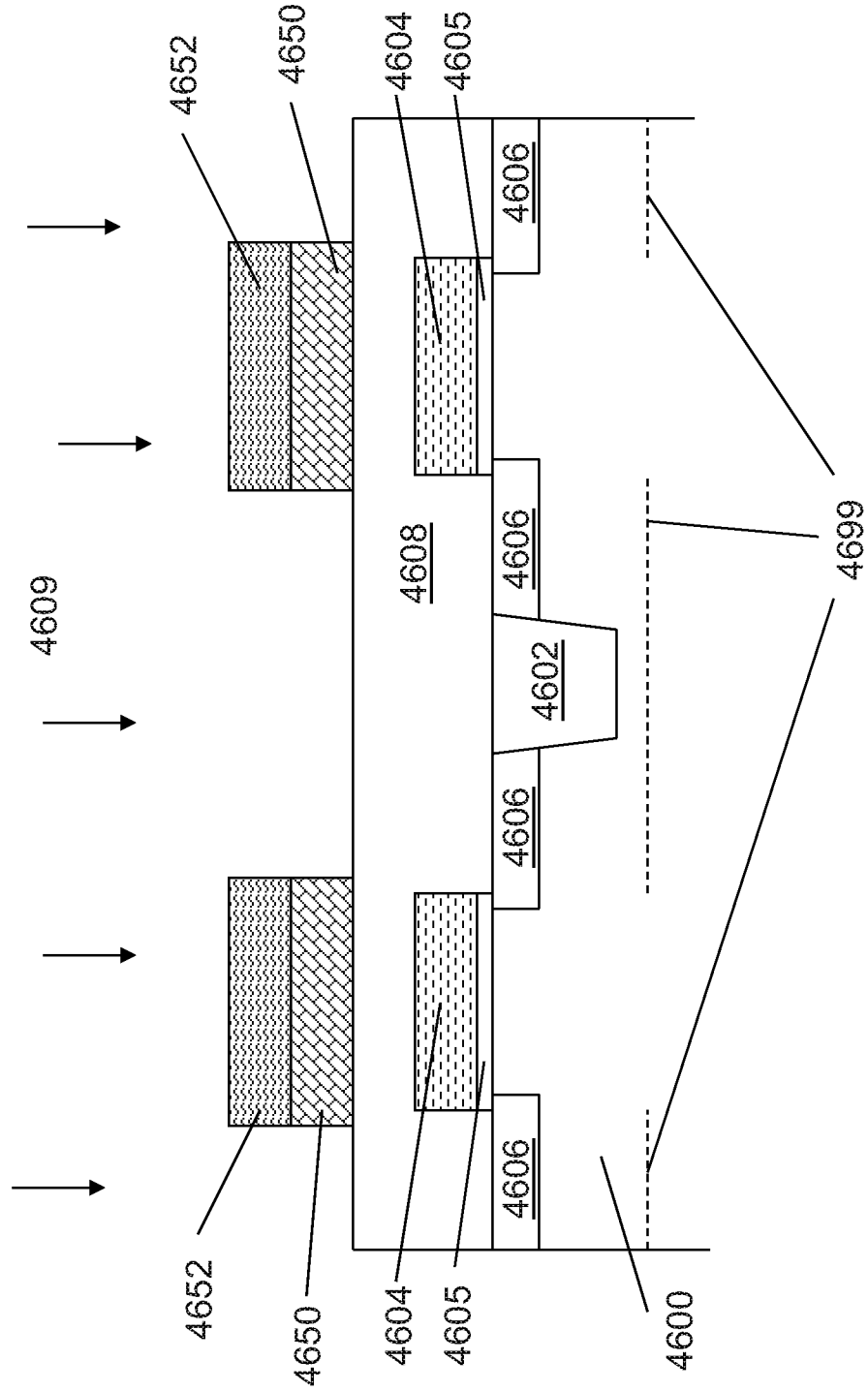
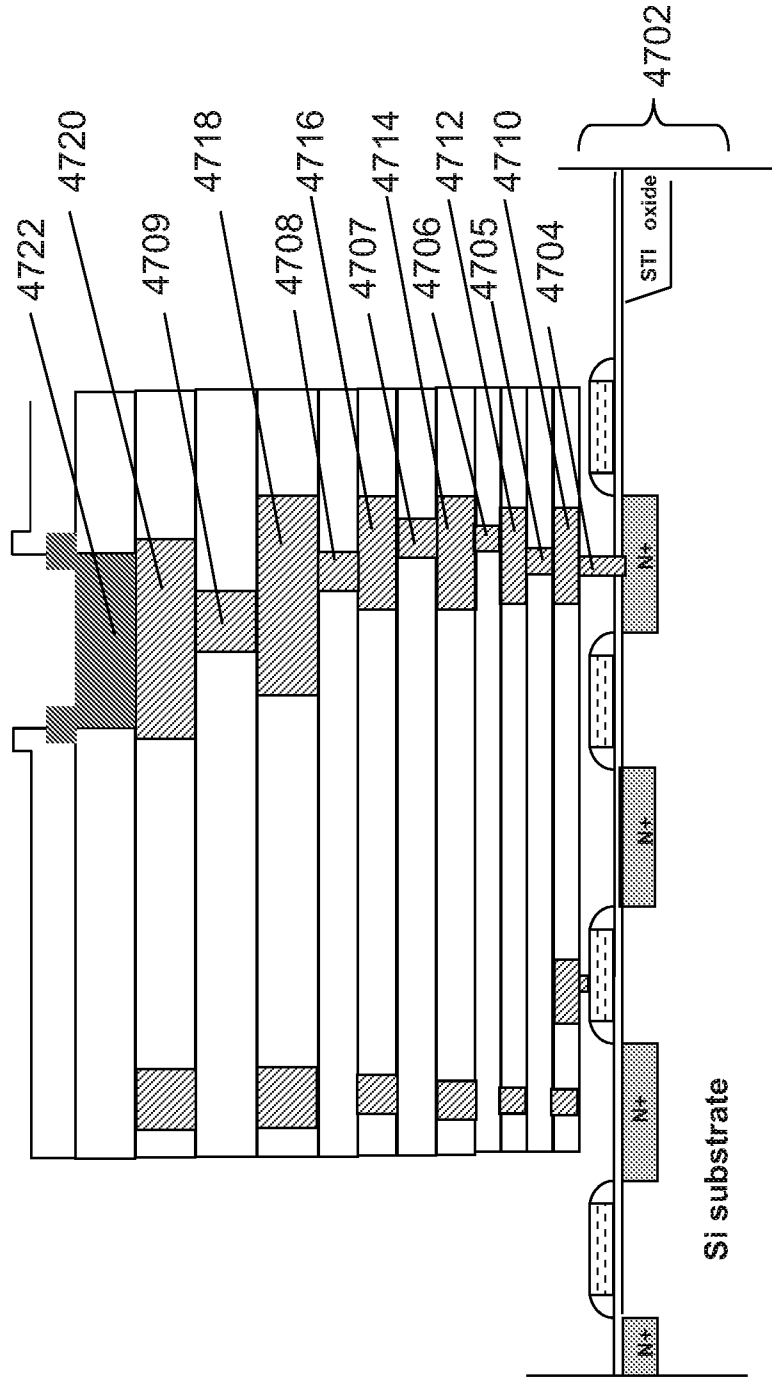


FIG. 47A



Prior Art

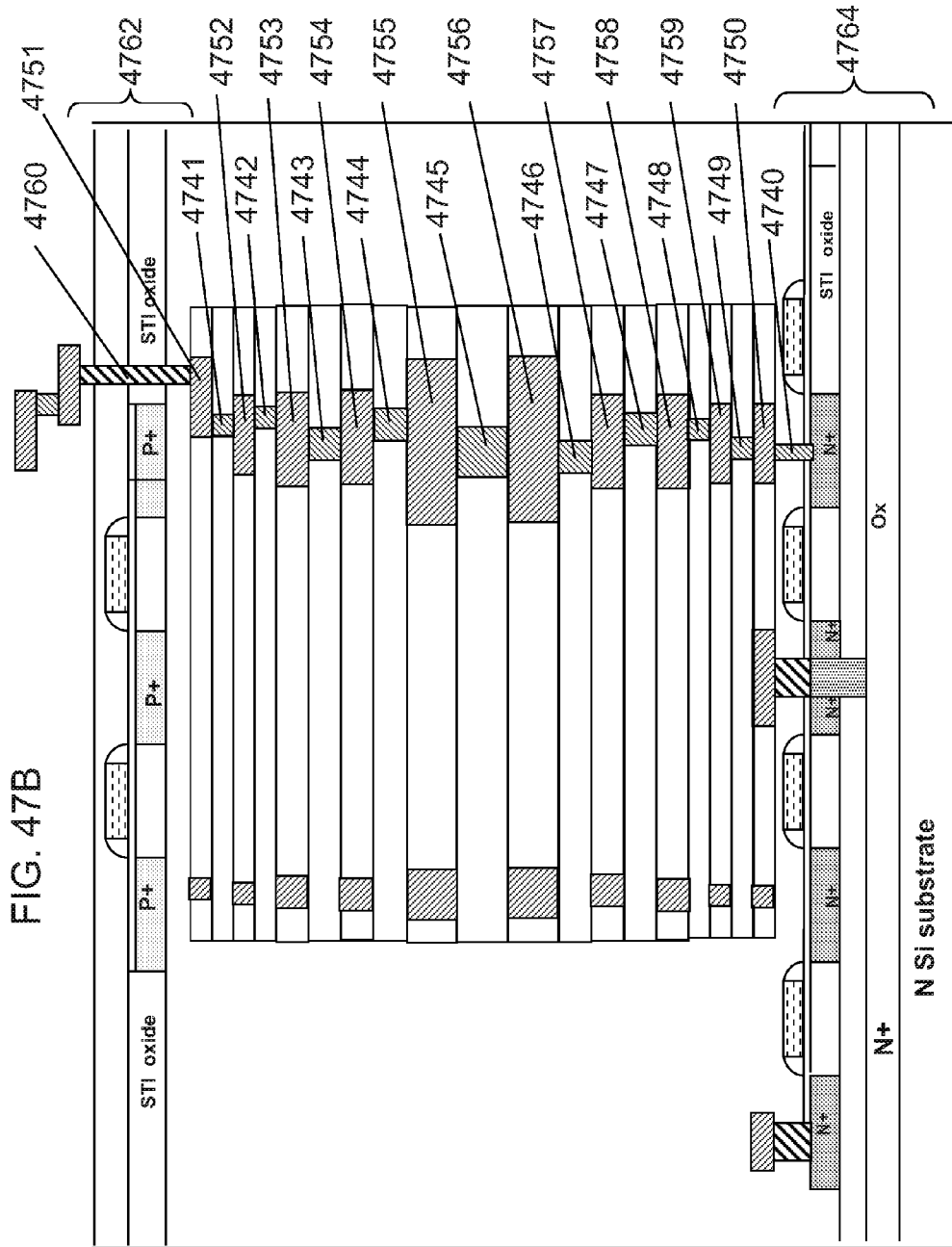


FIG. 47B

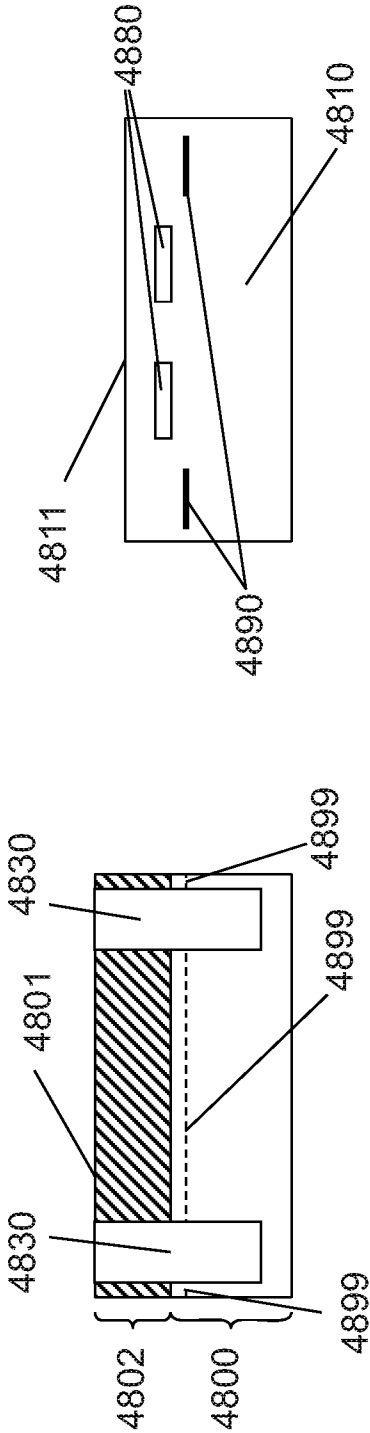


FIG. 48A

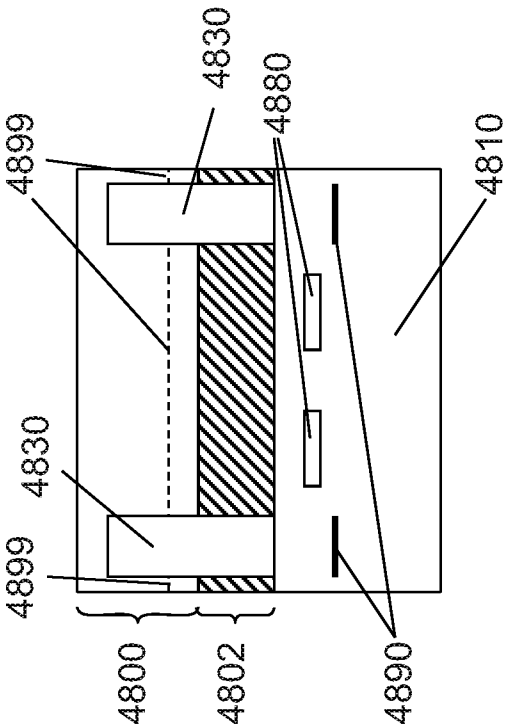


FIG. 48B



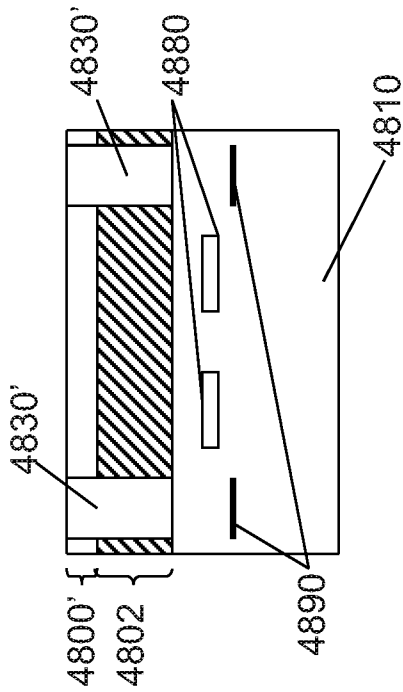


FIG. 48C

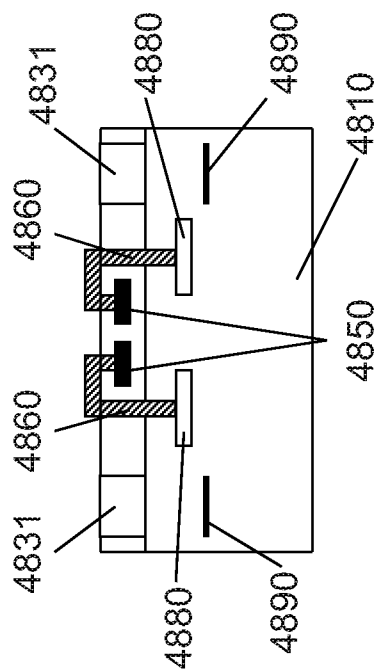


FIG. 48D

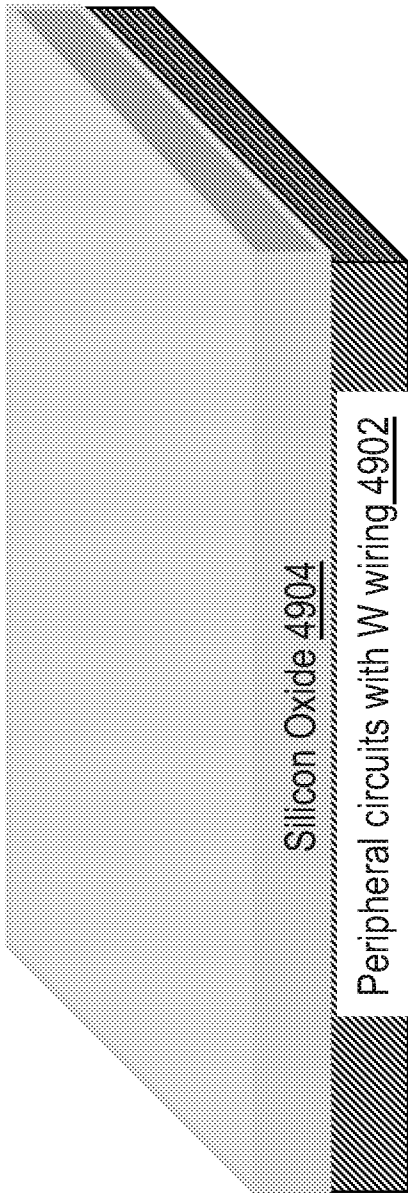


FIG. 49A

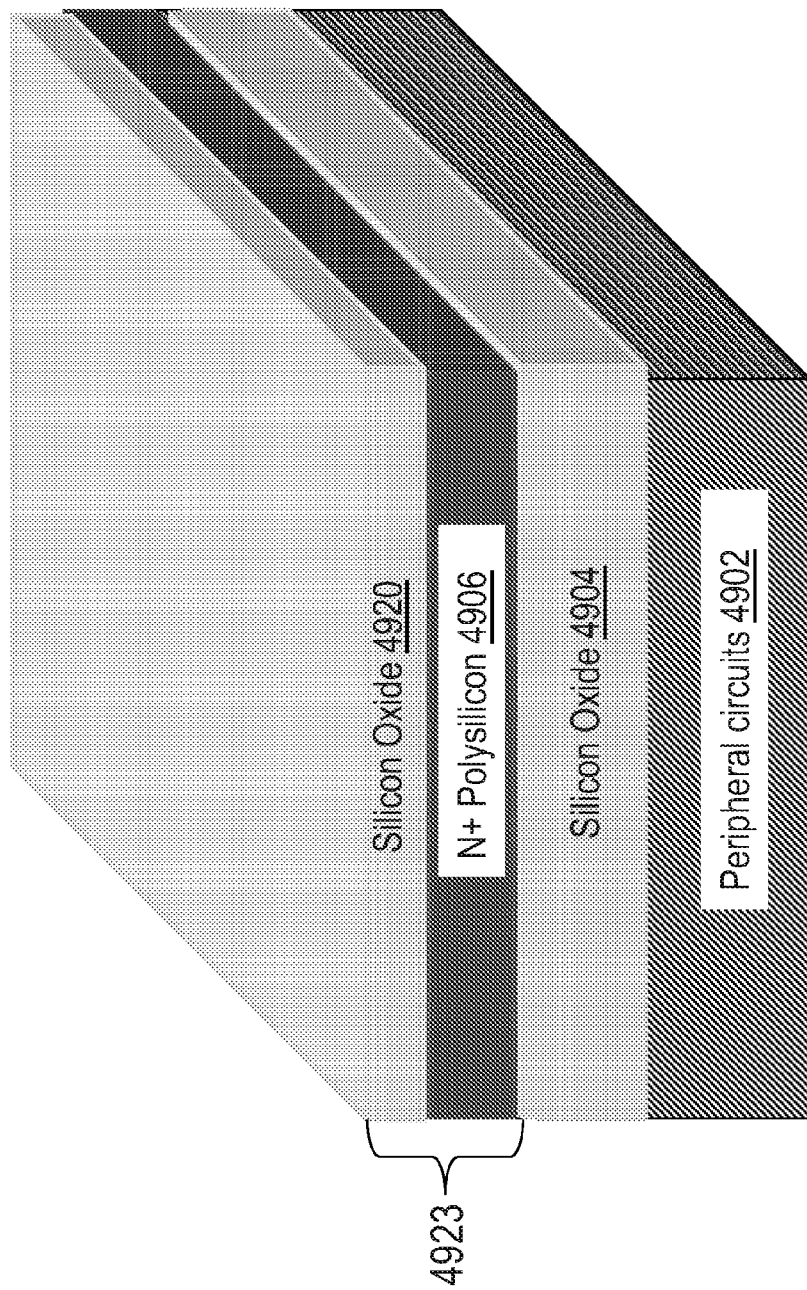


FIG. 49B

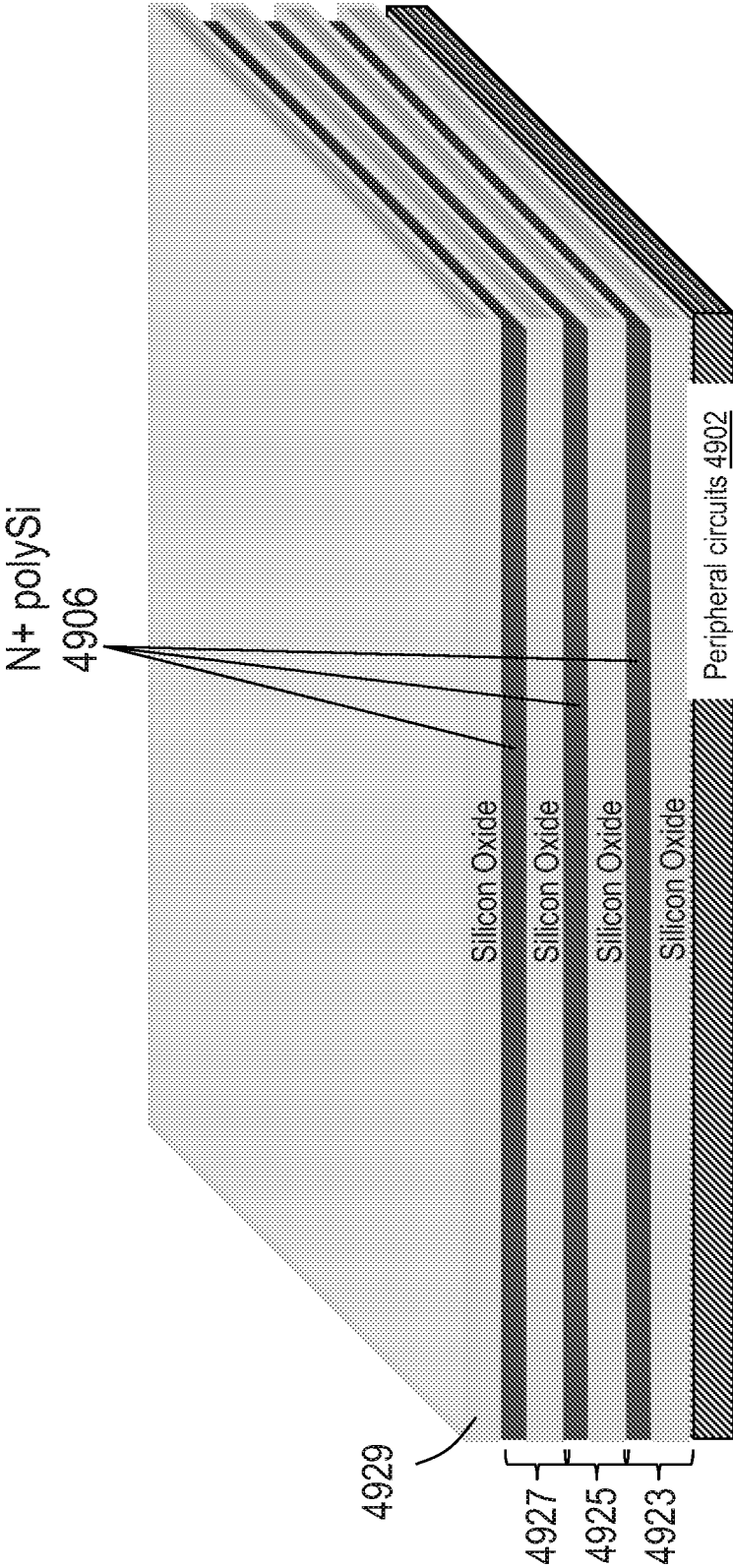


FIG. 49C

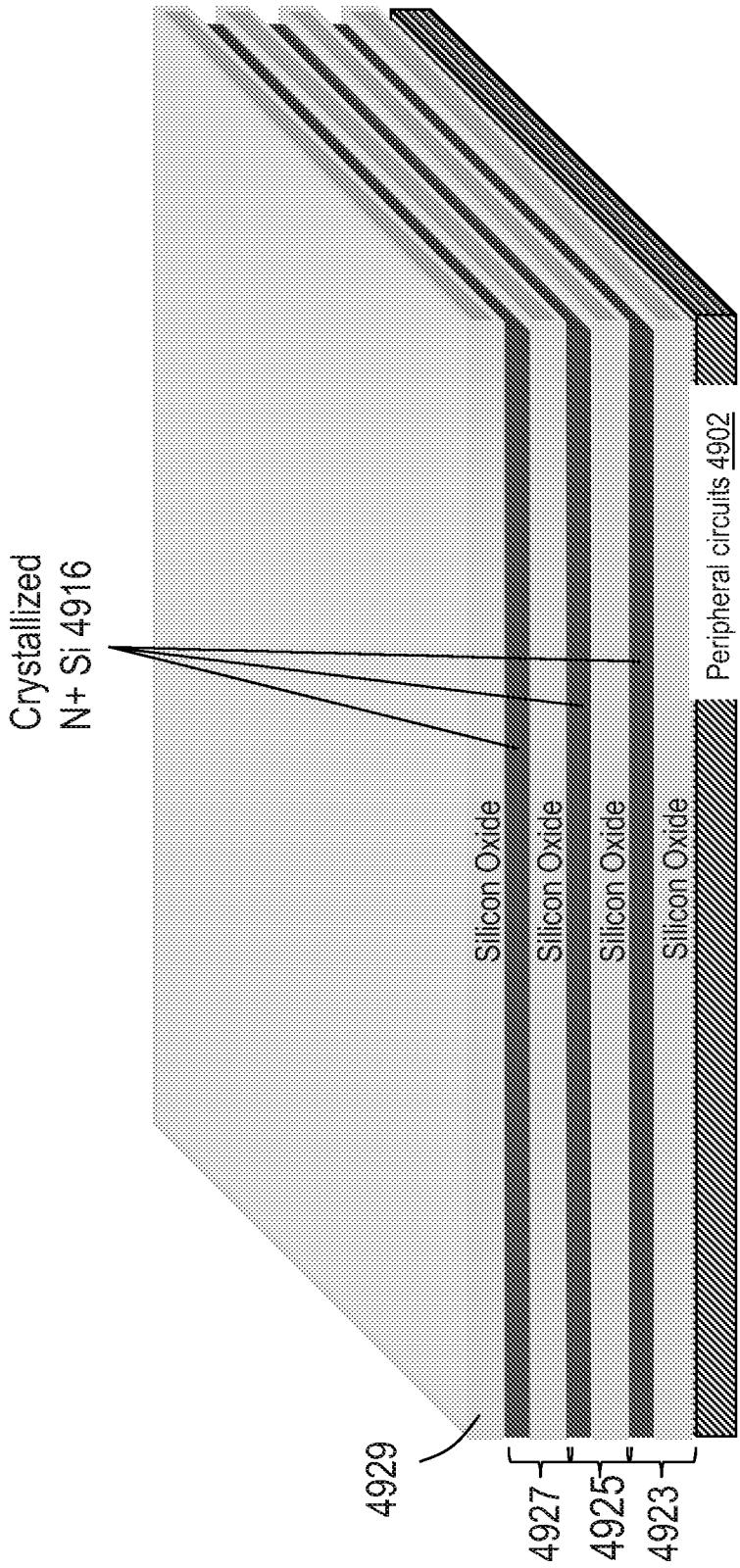


FIG. 49D

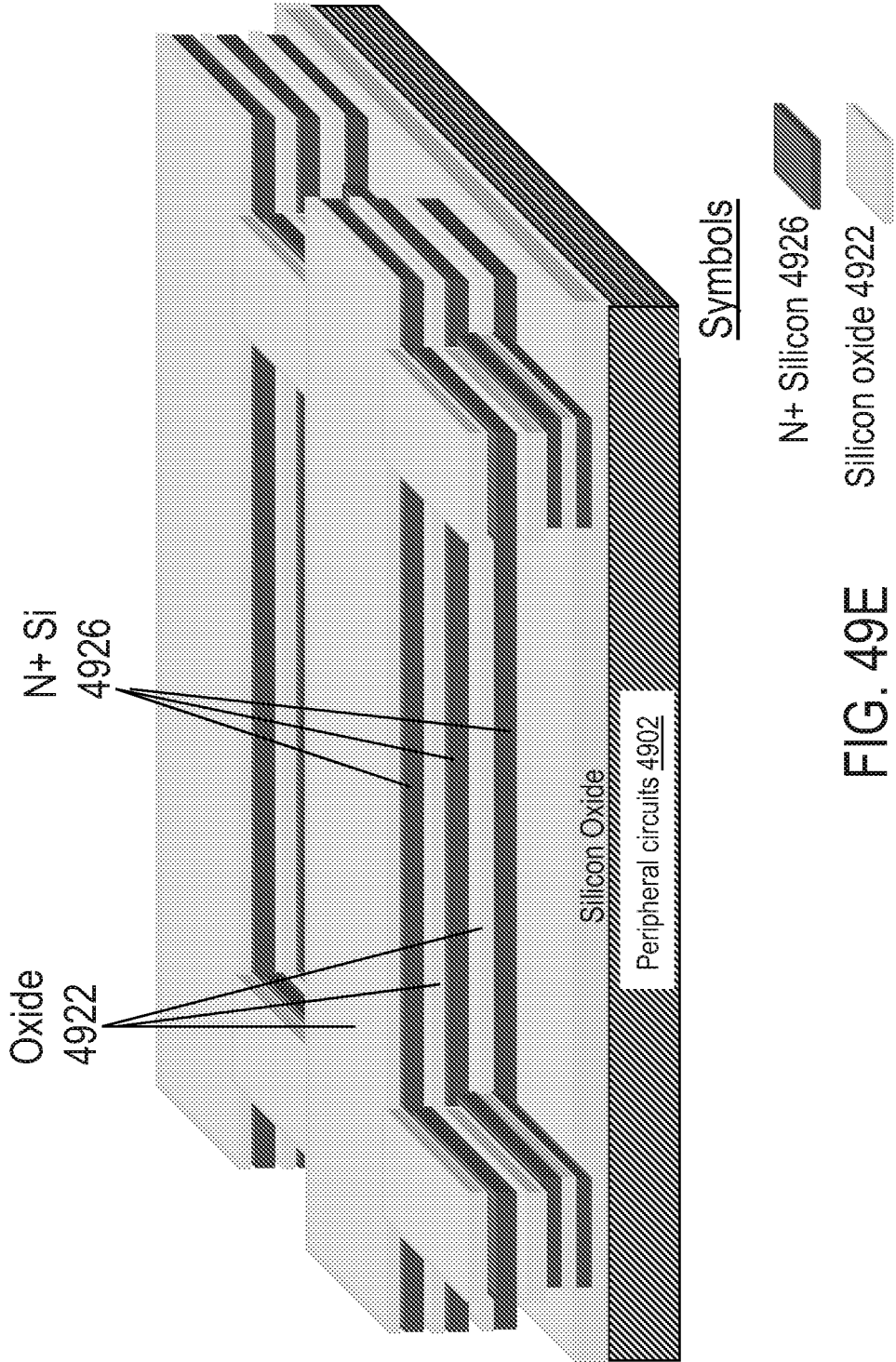


FIG. 49E

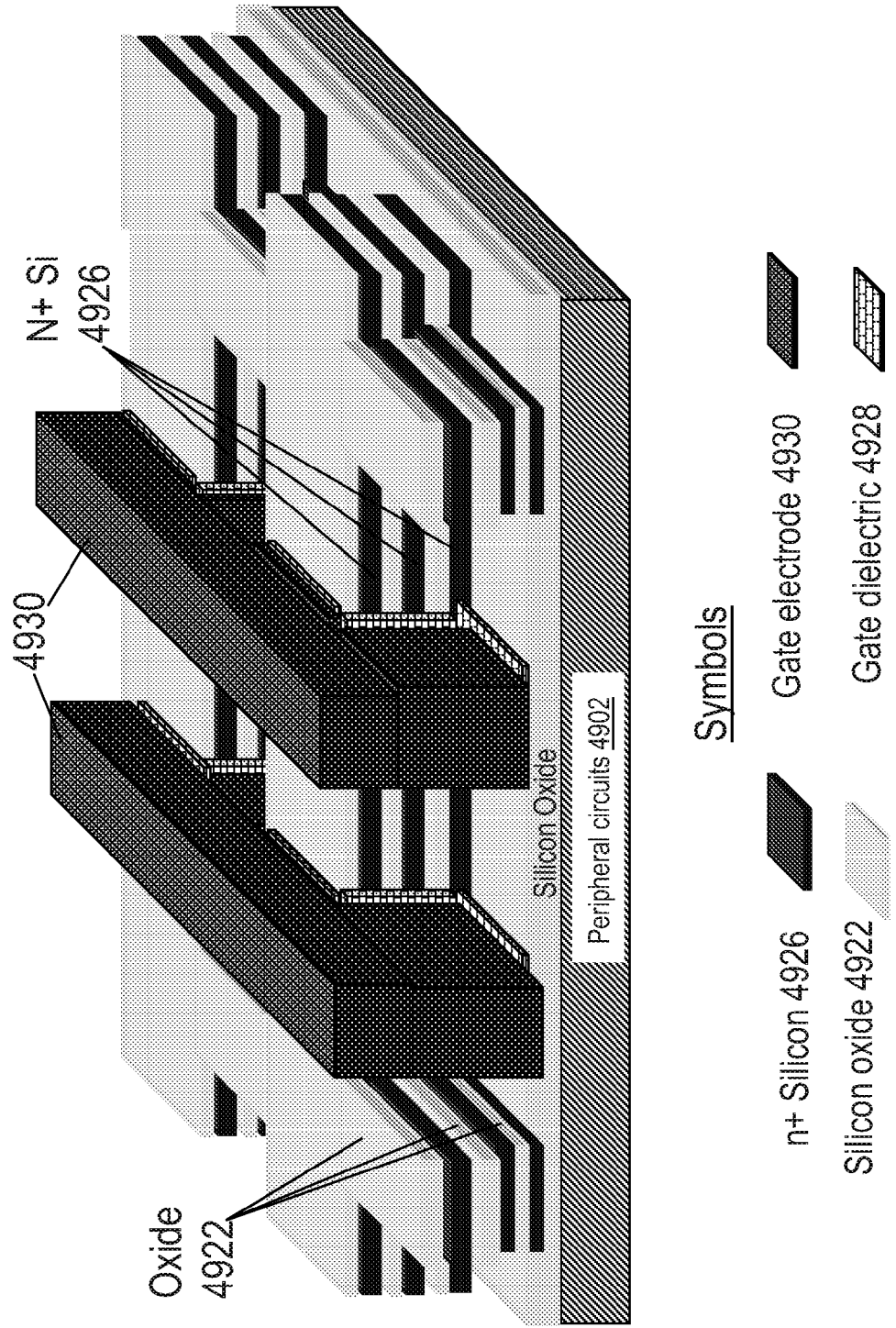
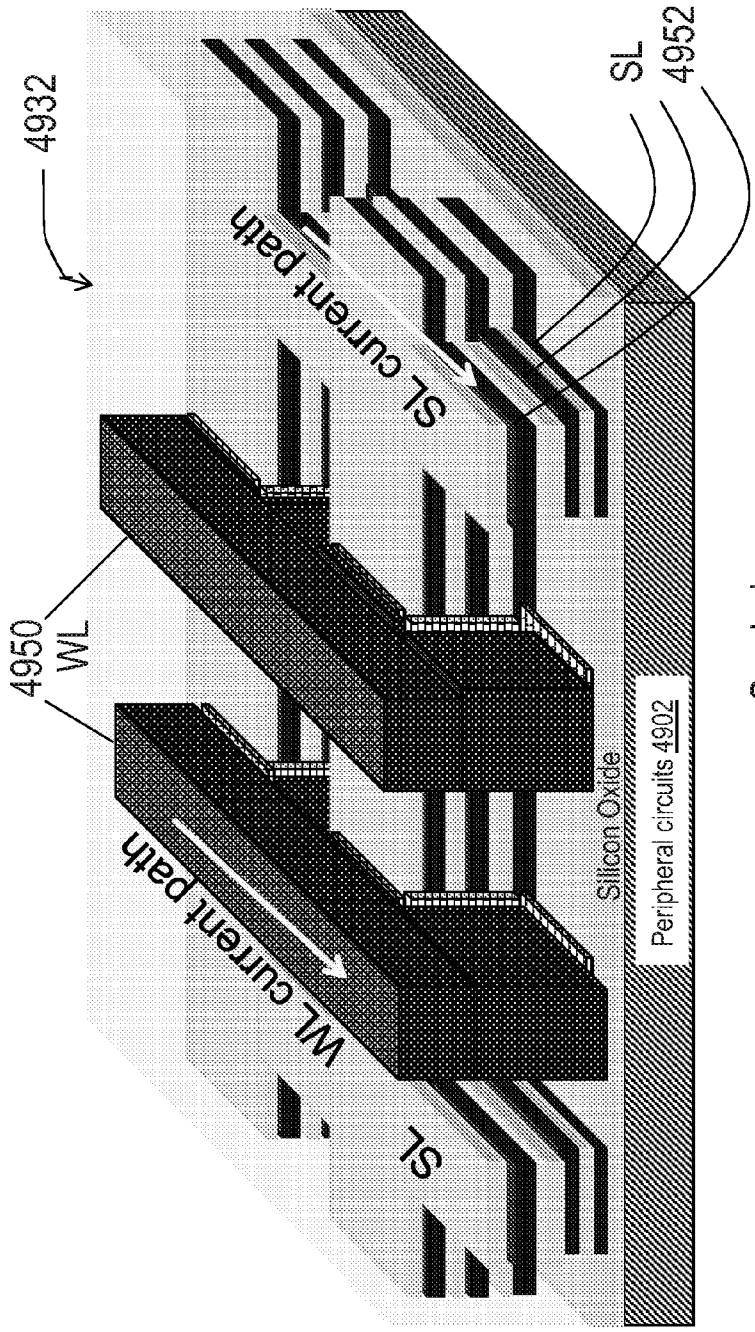


FIG. 49F





Symbols

- Gate dielectric 4928
- Gate electrode 4930
- Silicon oxide 4932
- n+ Silicon 4926
- Silicon oxide 4922

FIG. 49G

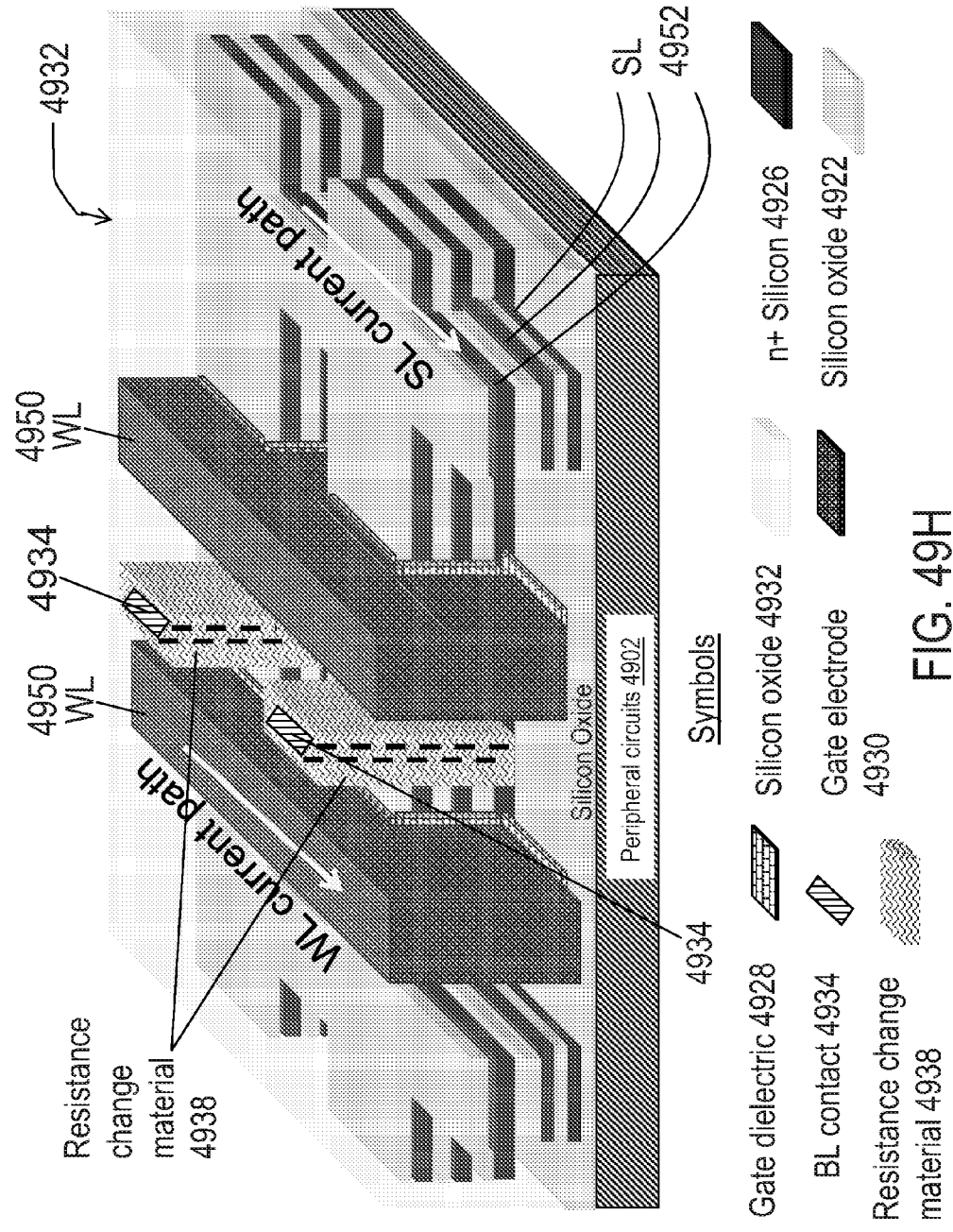
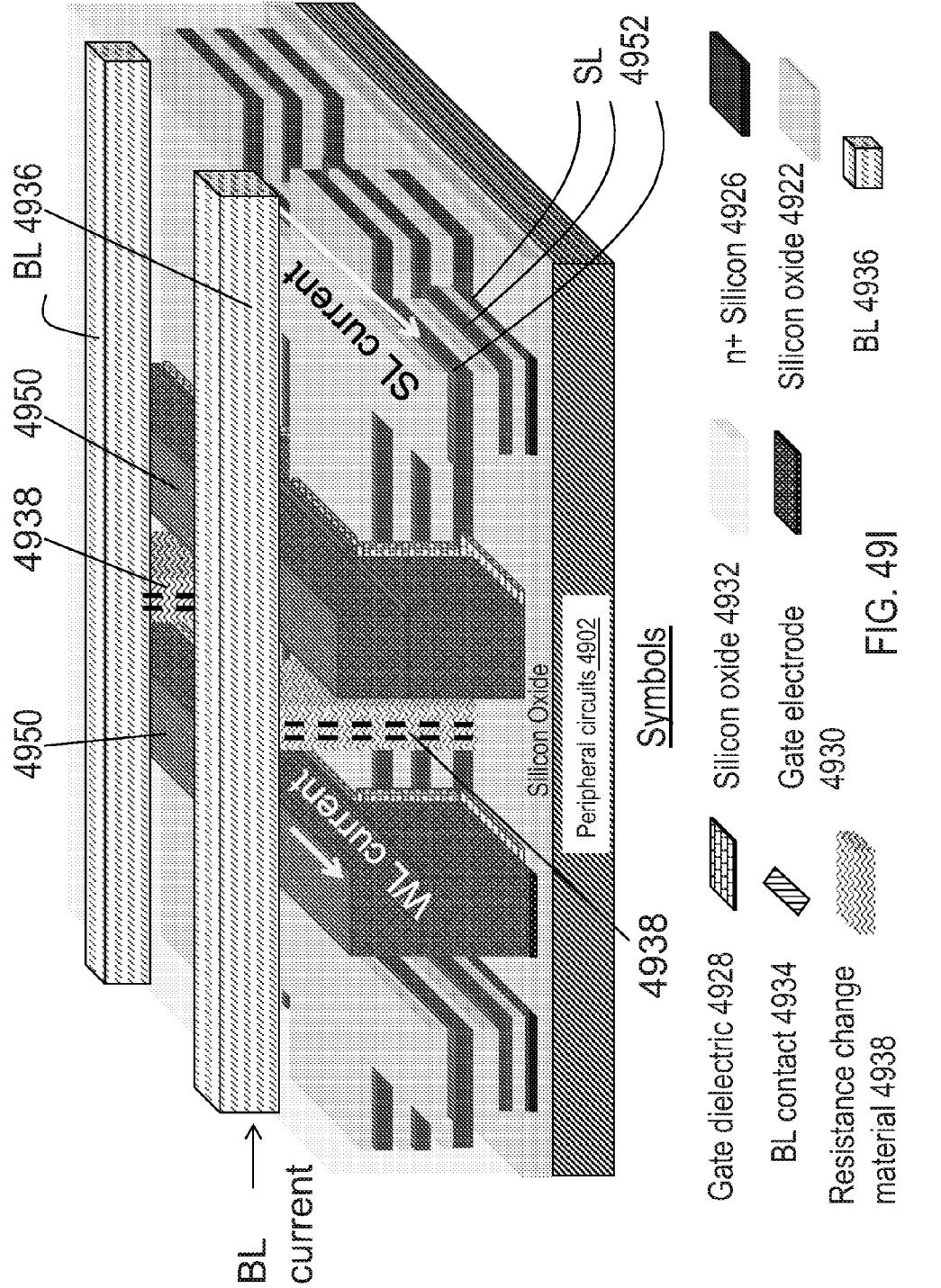


FIG. 49H



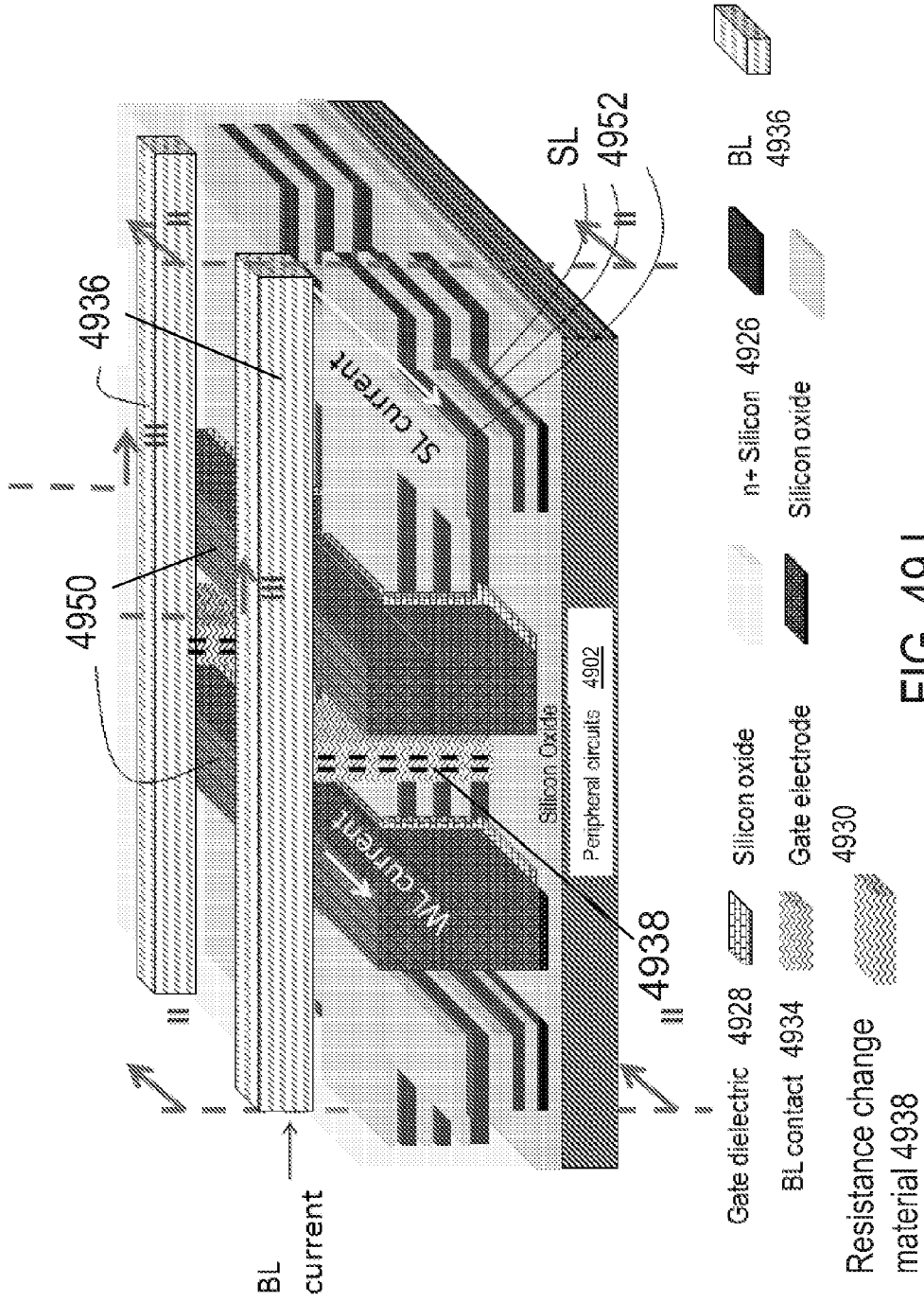
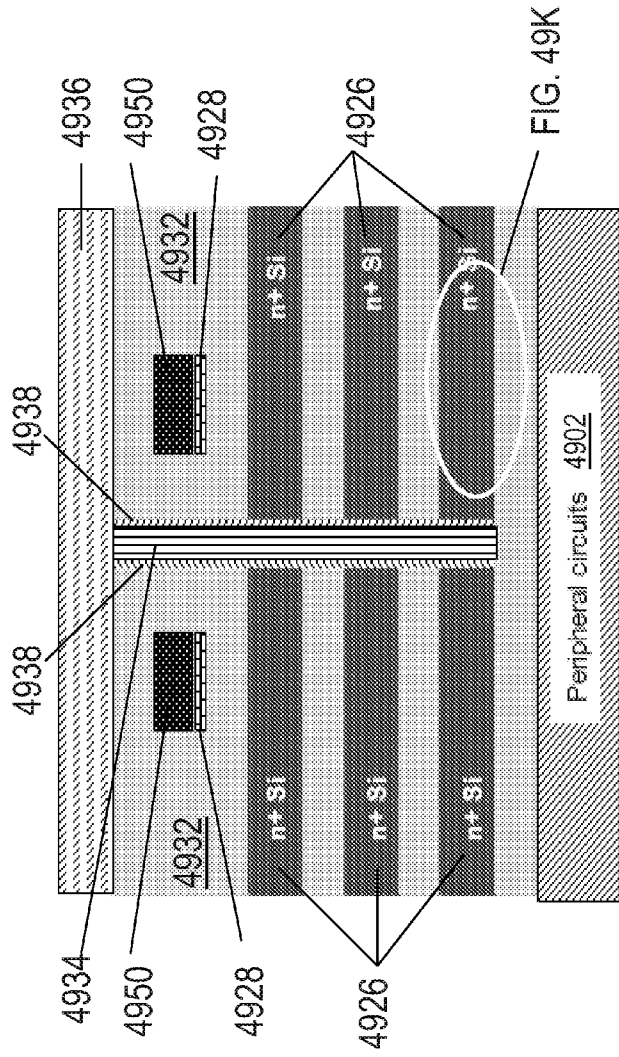


FIG. 49J



View along II plane

**Symbols**

- Gate dielectric 4928
- BL contact 4934
- Resistance change material 4938
- Silicon oxide
- Gate electrode 4930
- n+ Silicon 4926
- Silicon oxide
- BL 4936

FIG. 49J1

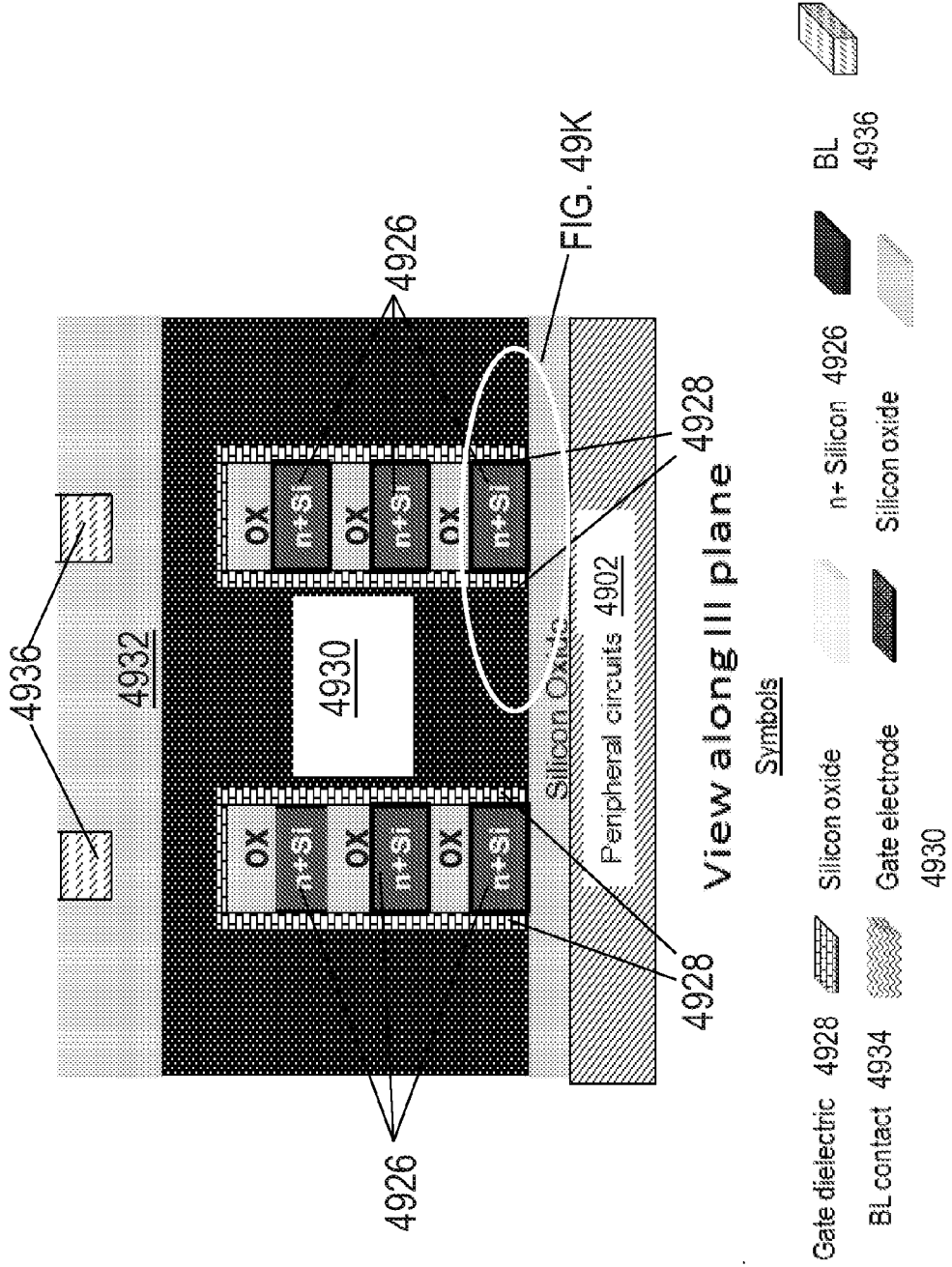


FIG. 49J2

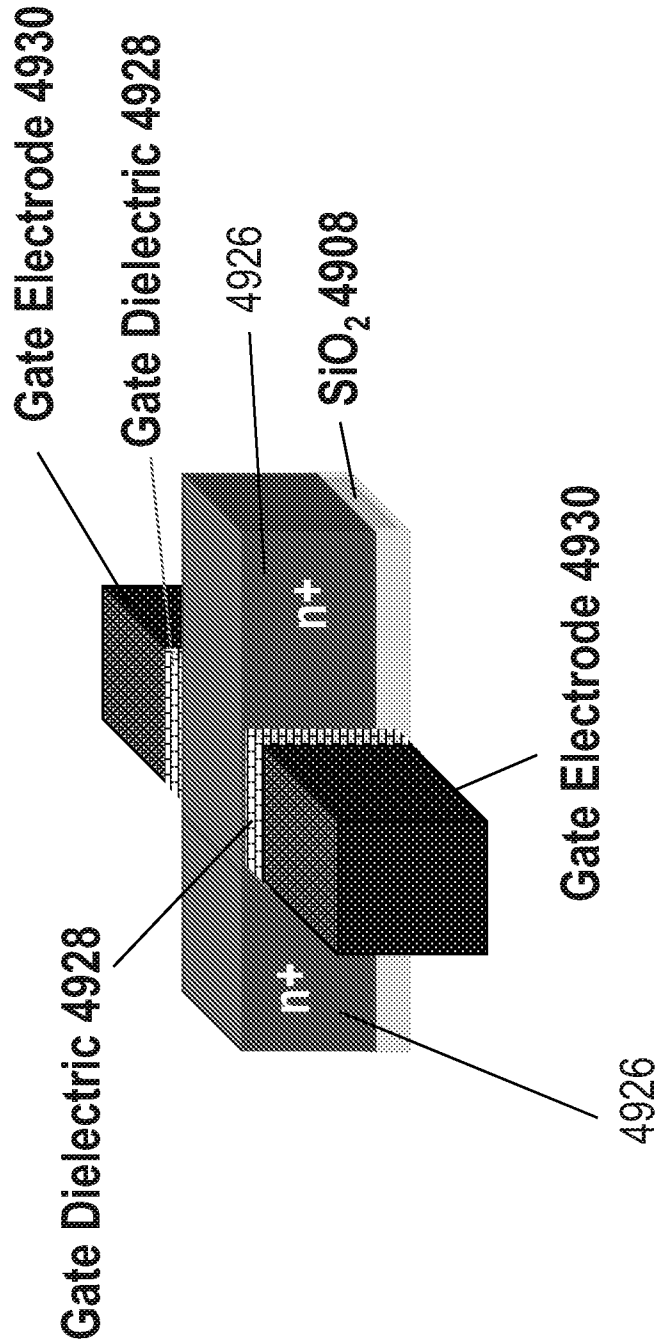


FIG. 49K

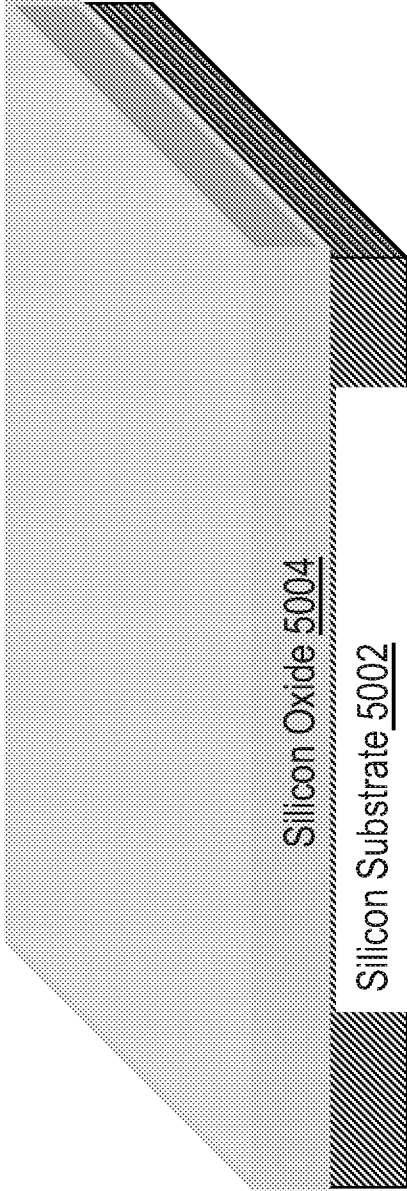


FIG. 50A



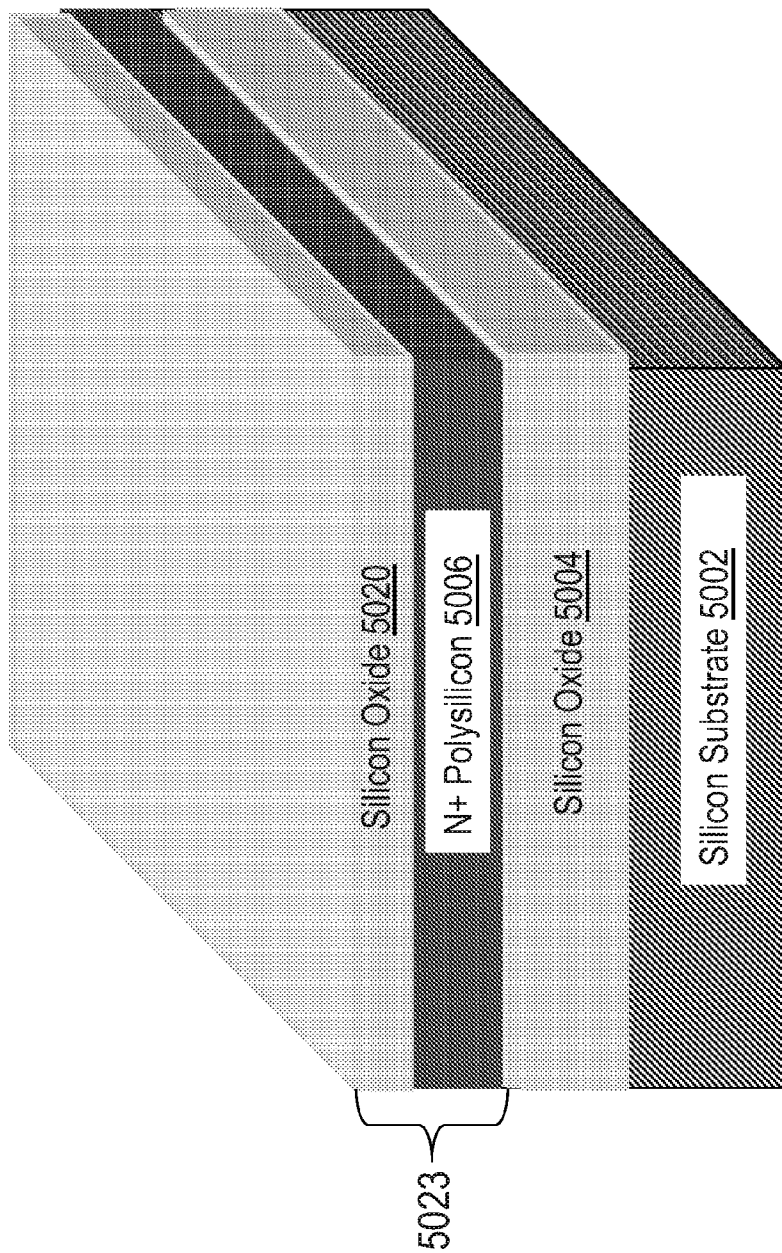


FIG. 50B

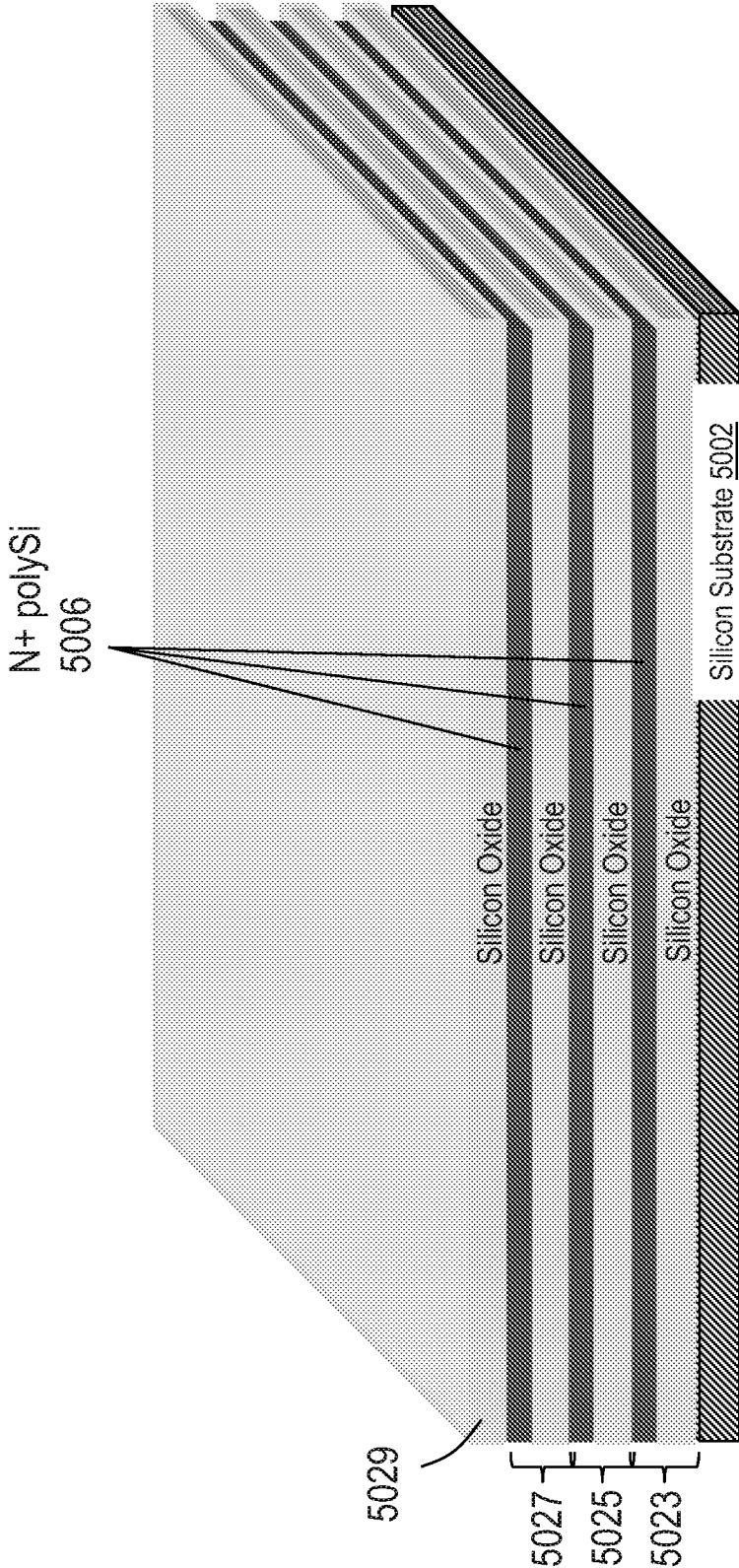


FIG. 500C

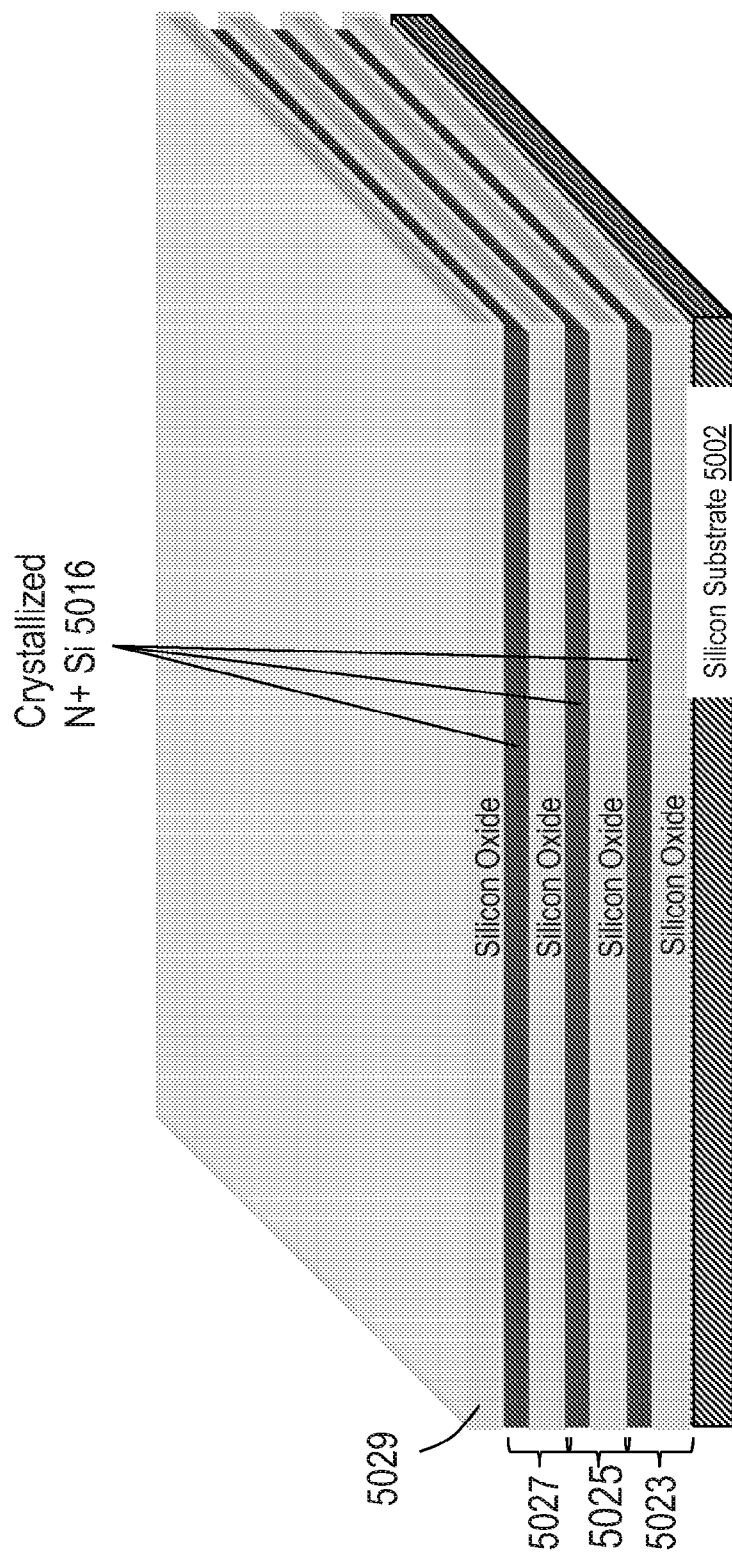


FIG. 50D

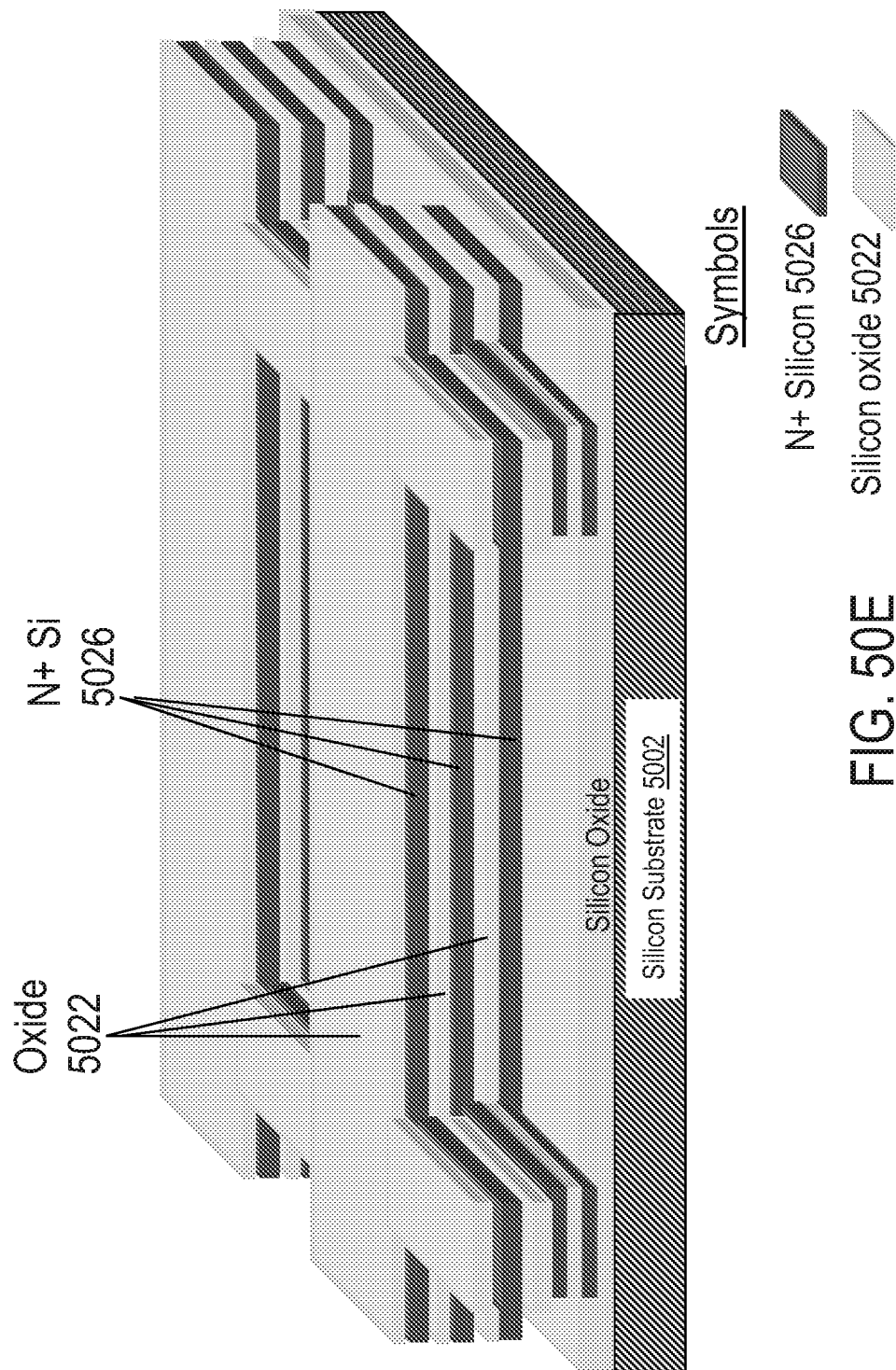


FIG. 50E

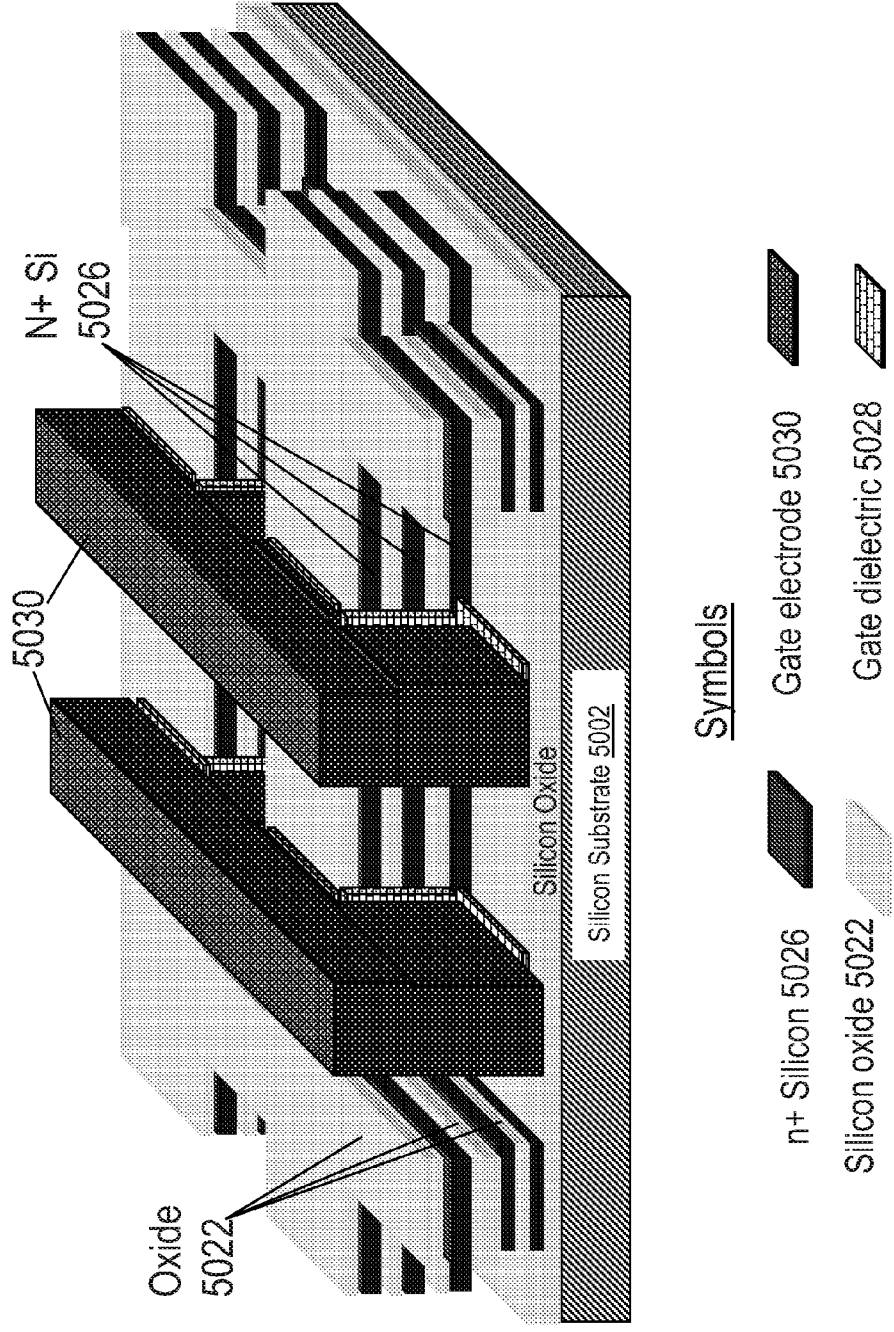


FIG. 50F

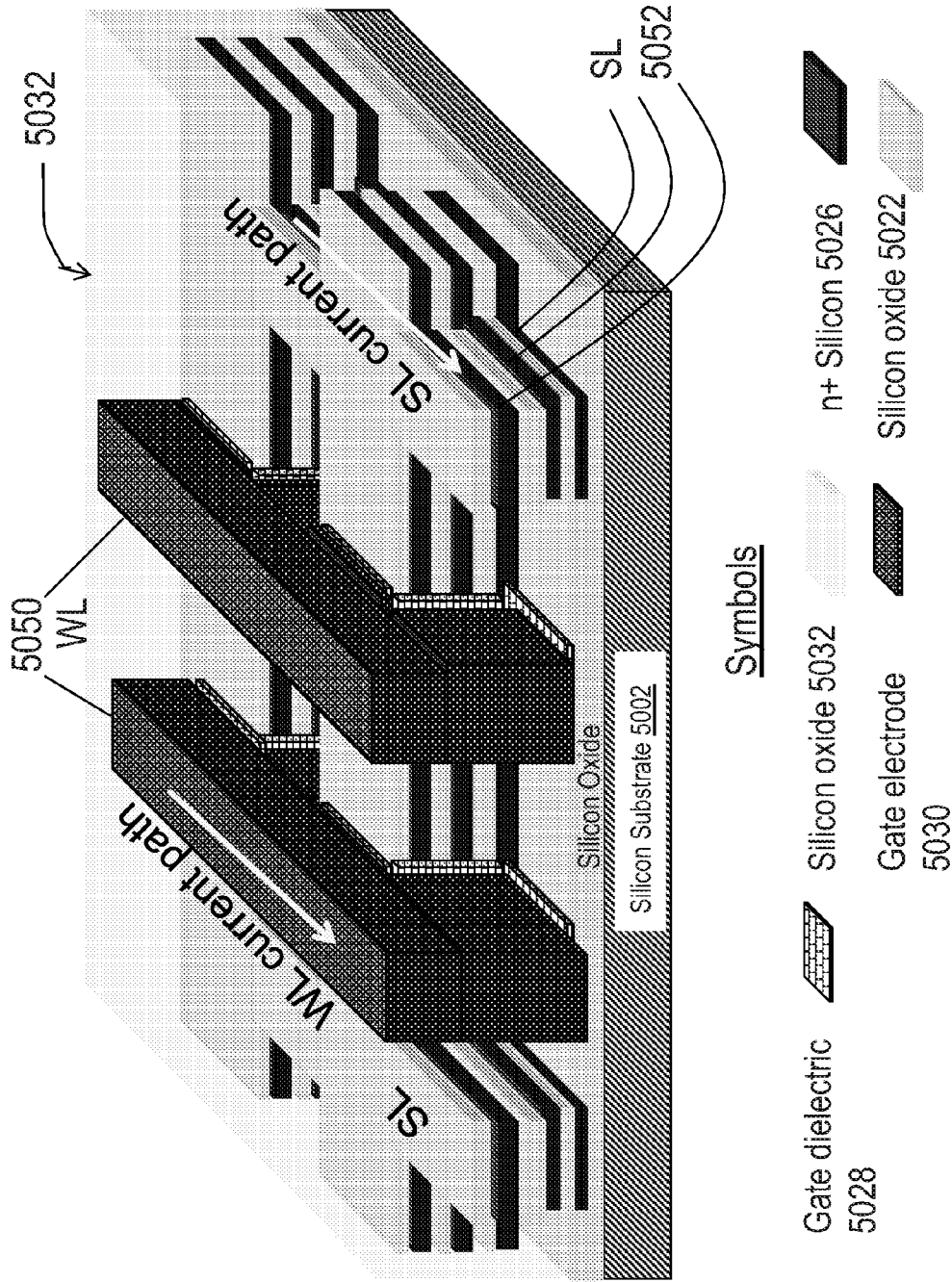


FIG. 50G

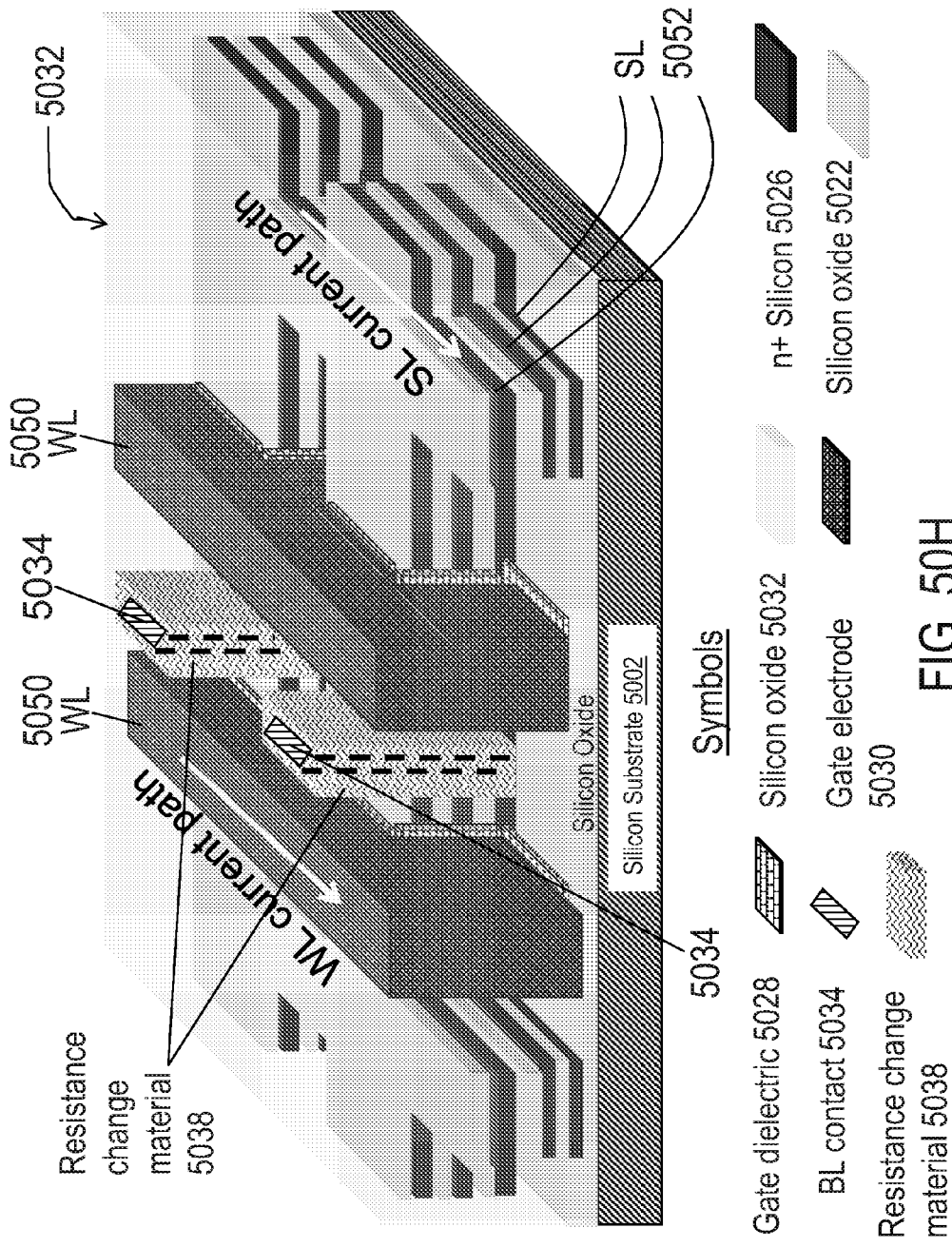


FIG. 50H

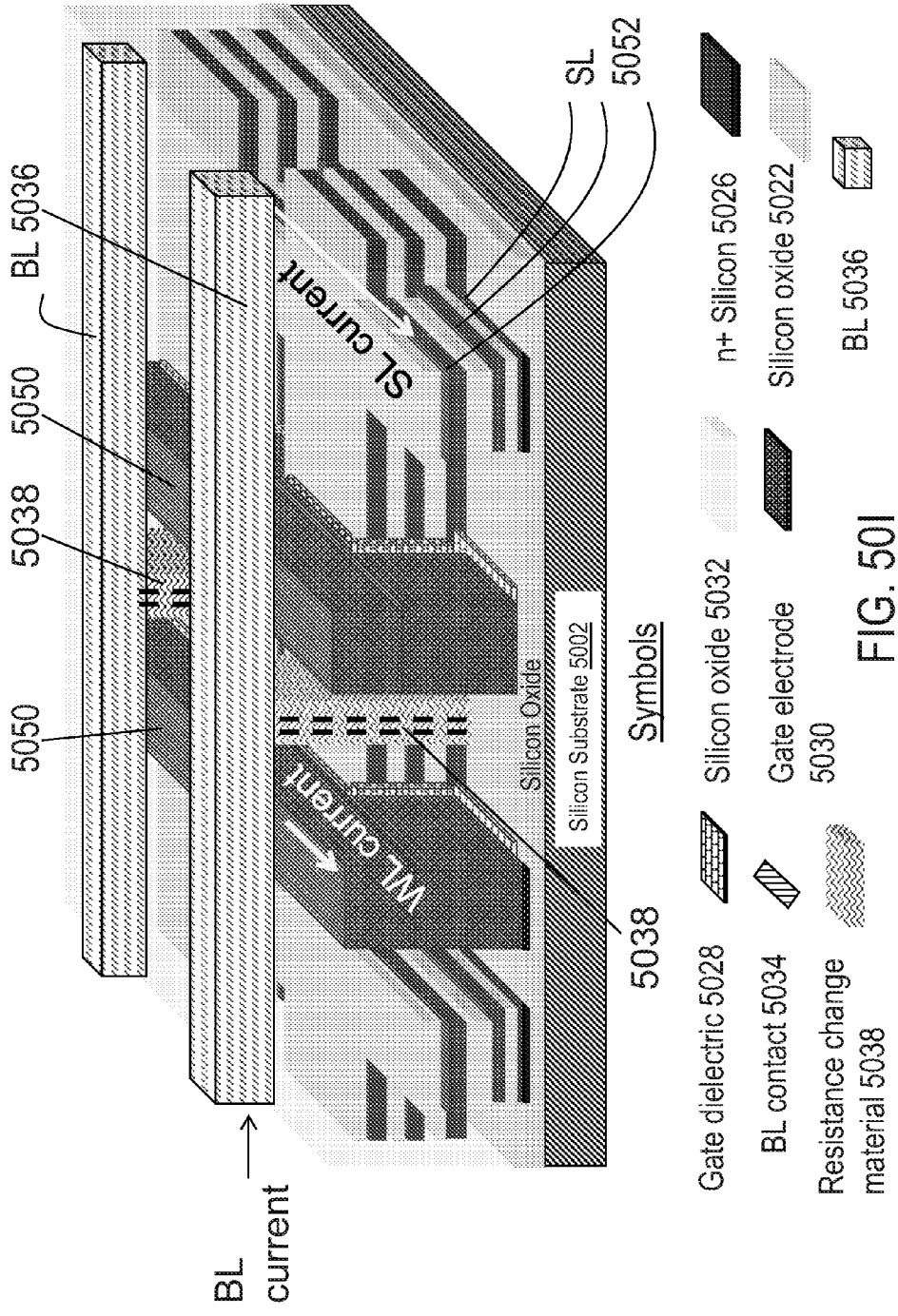


FIG. 50I



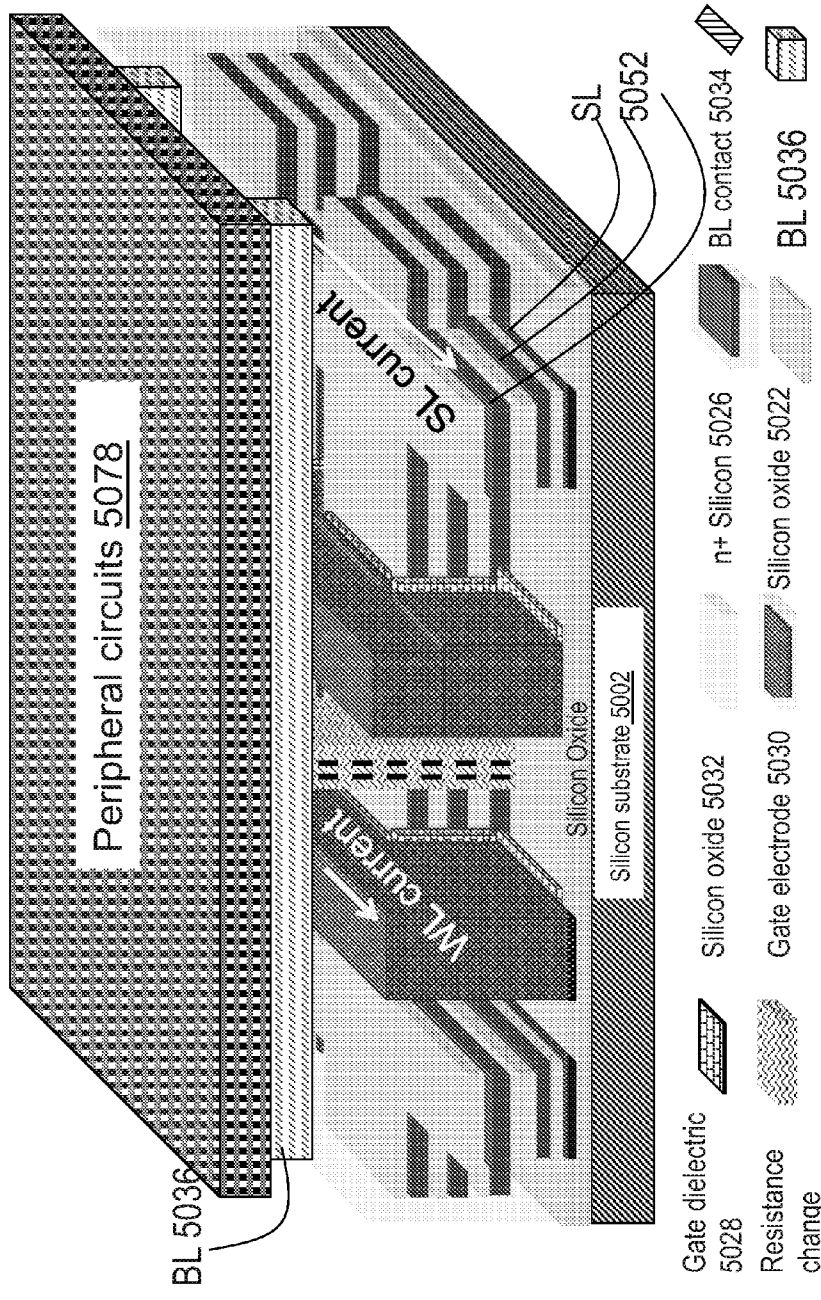


Fig. 50J

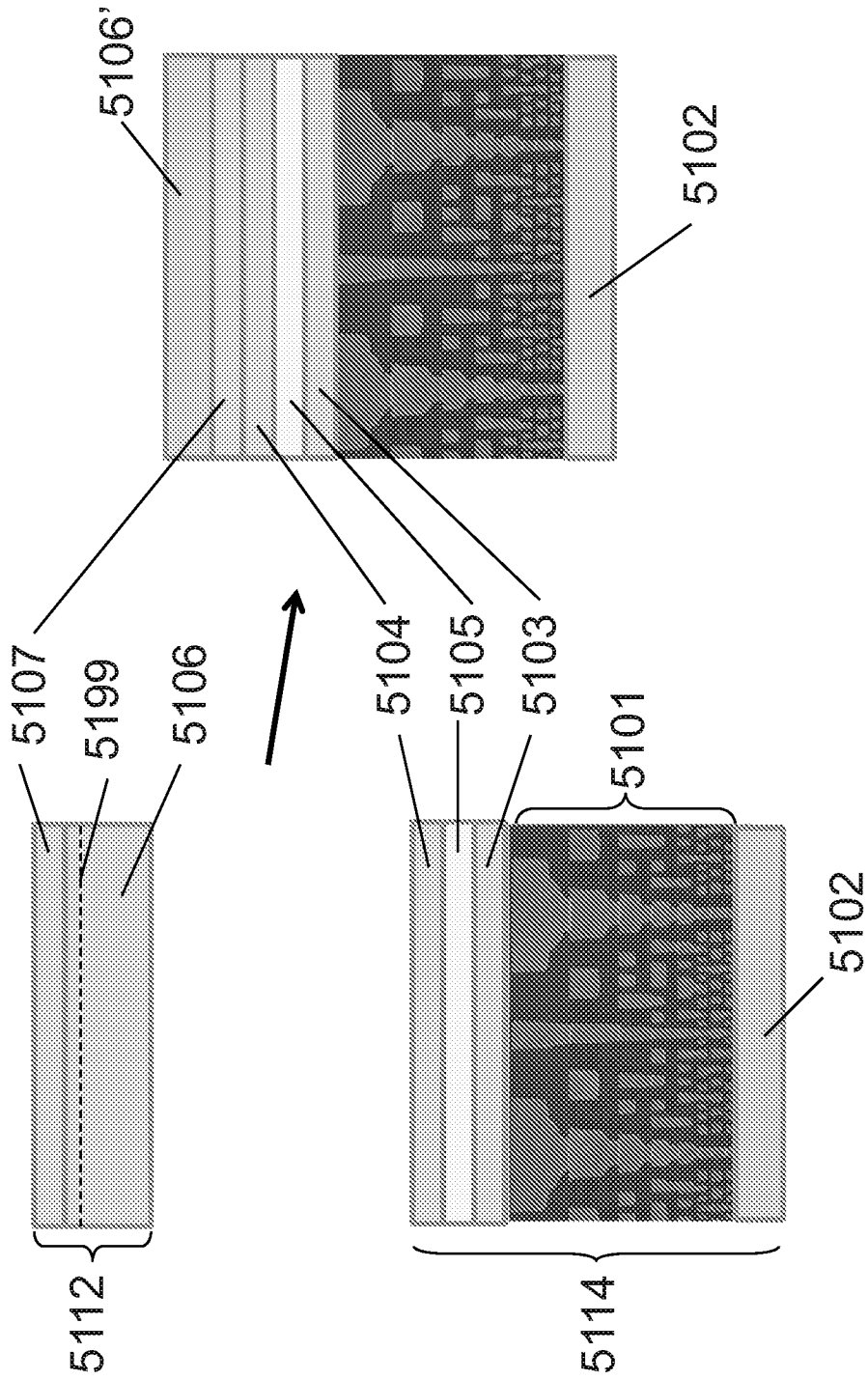


FIG. 51

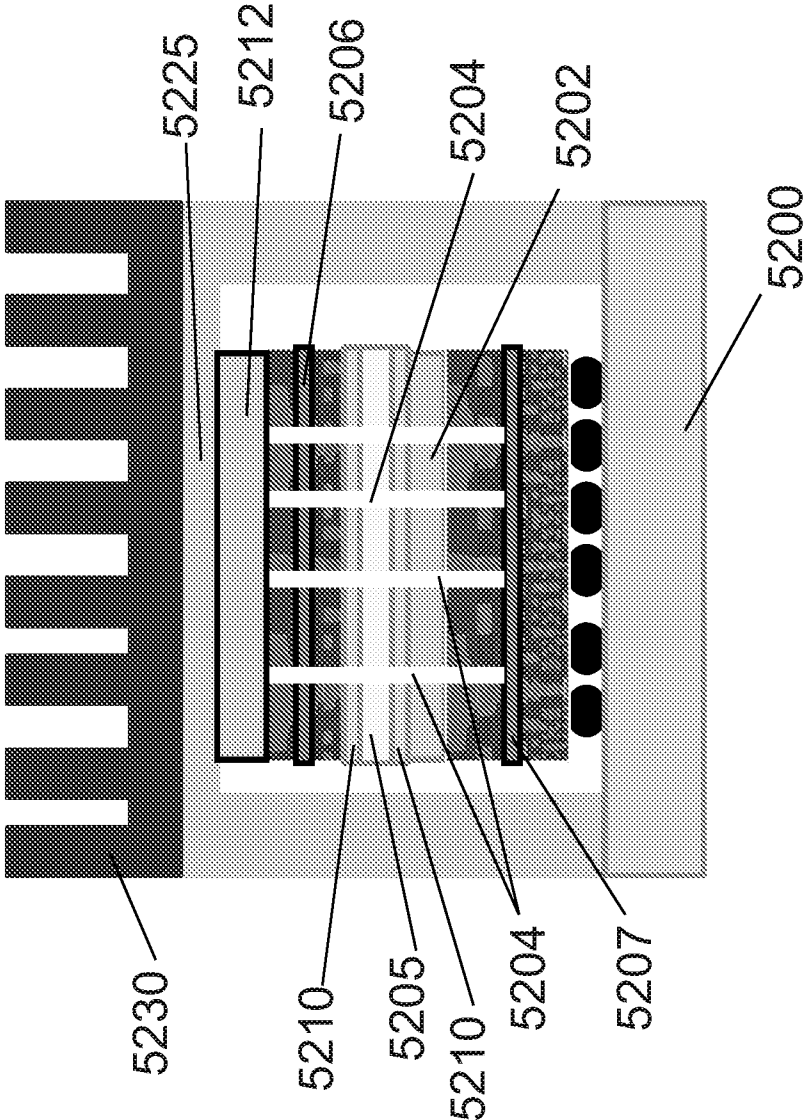


FIG. 52A

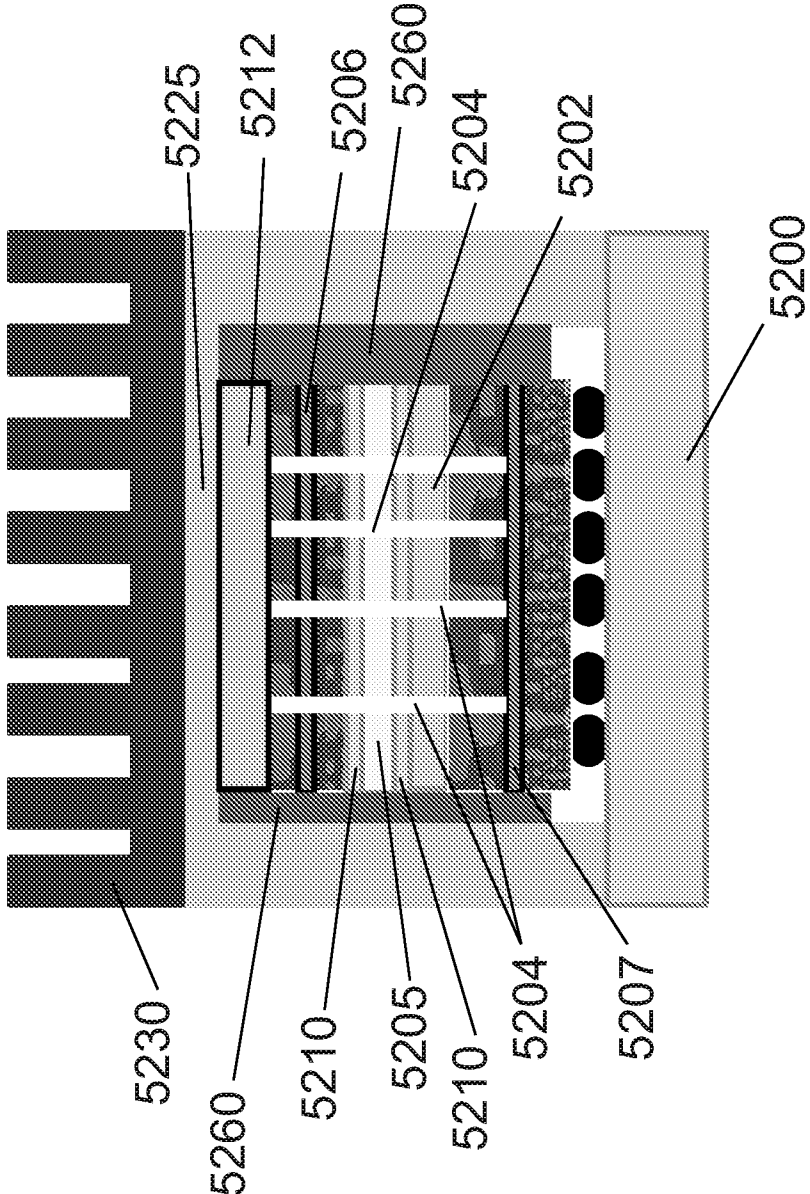


FIG. 52B

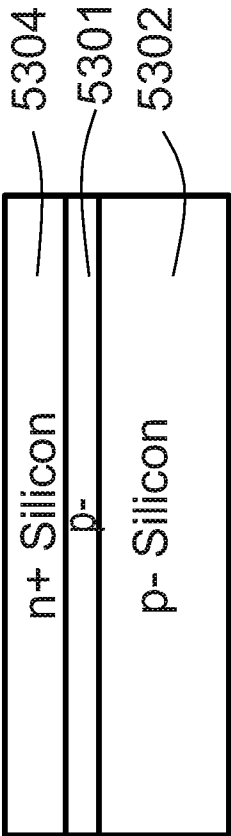


FIG. 53A

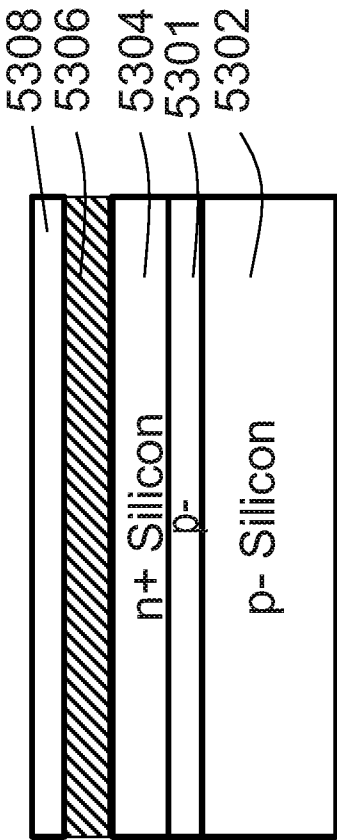


FIG. 53B

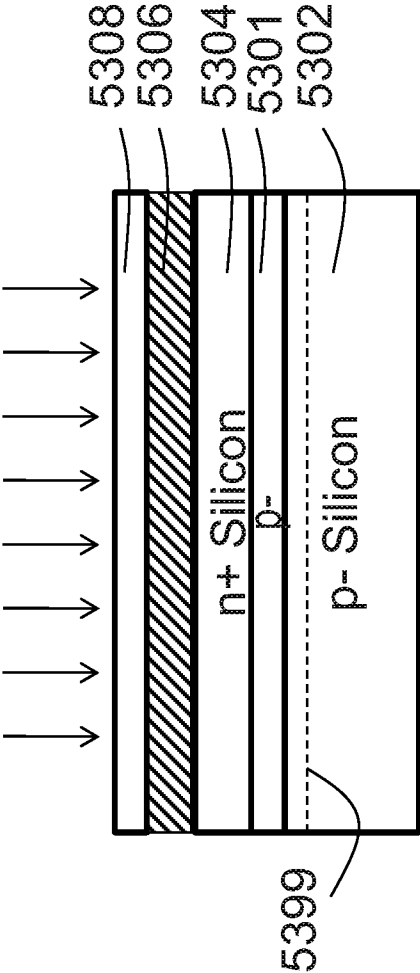


FIG. 53C

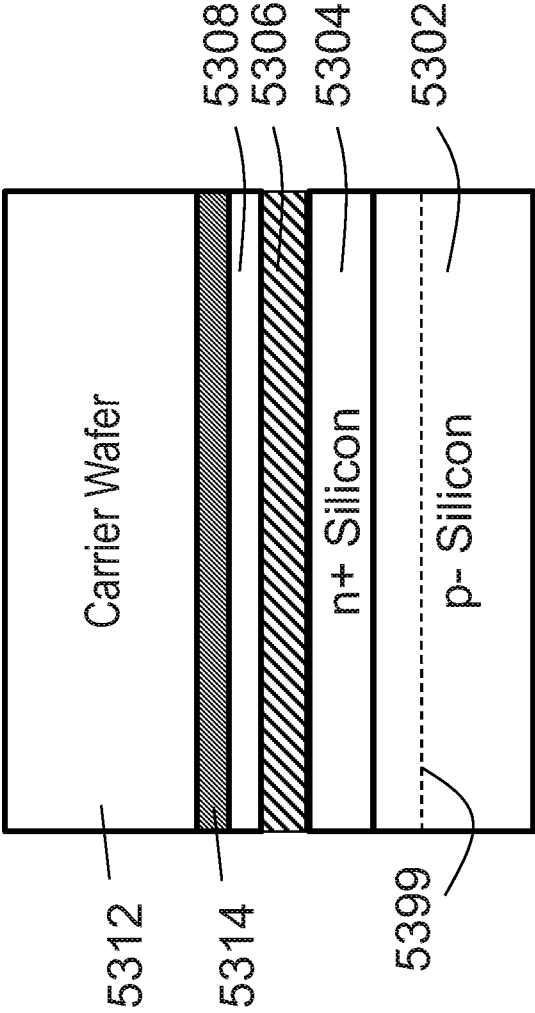


FIG. 53D



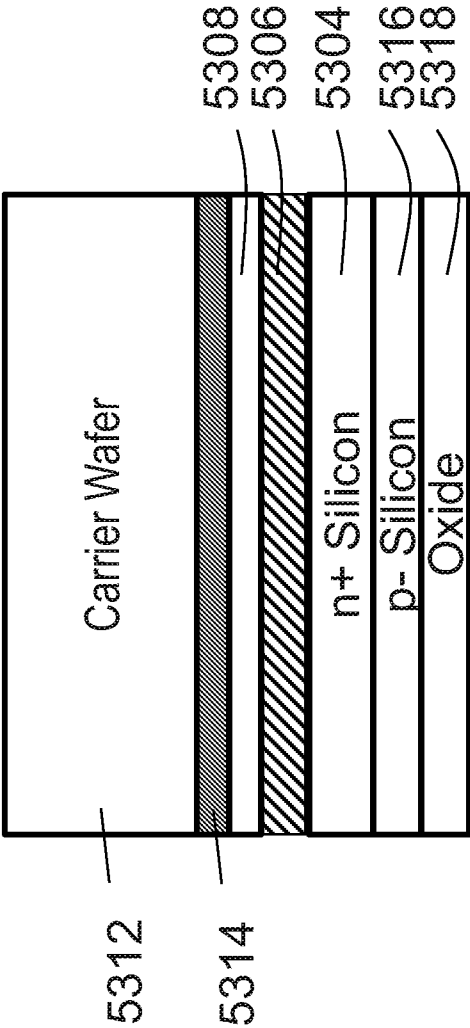


FIG. 53E

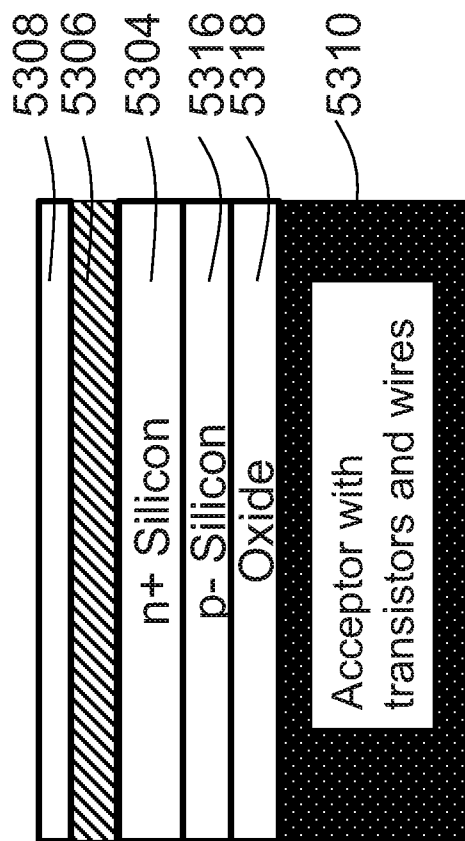


FIG. 53F



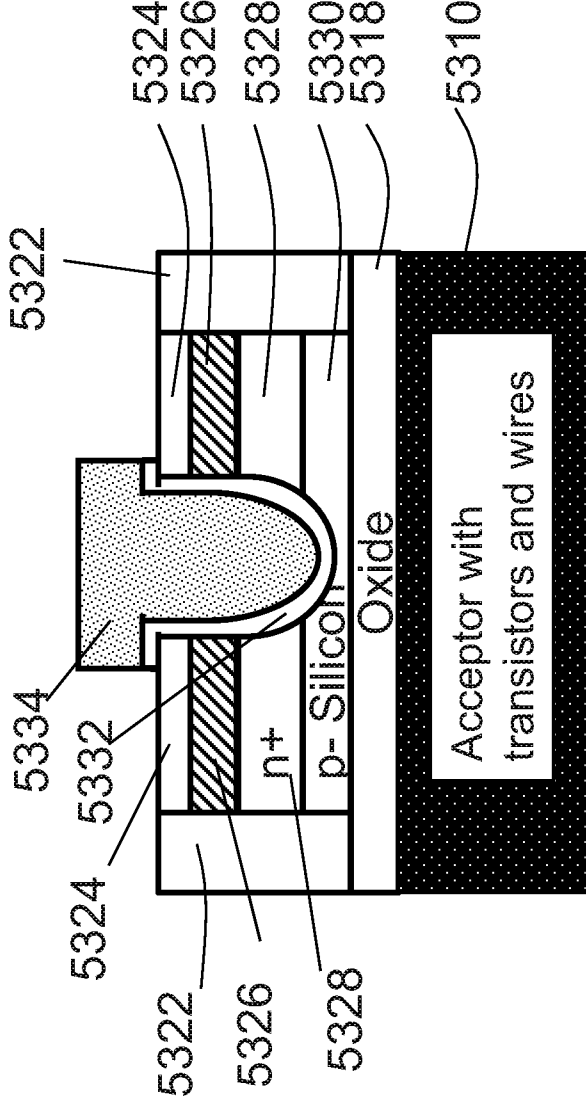


FIG. 53H

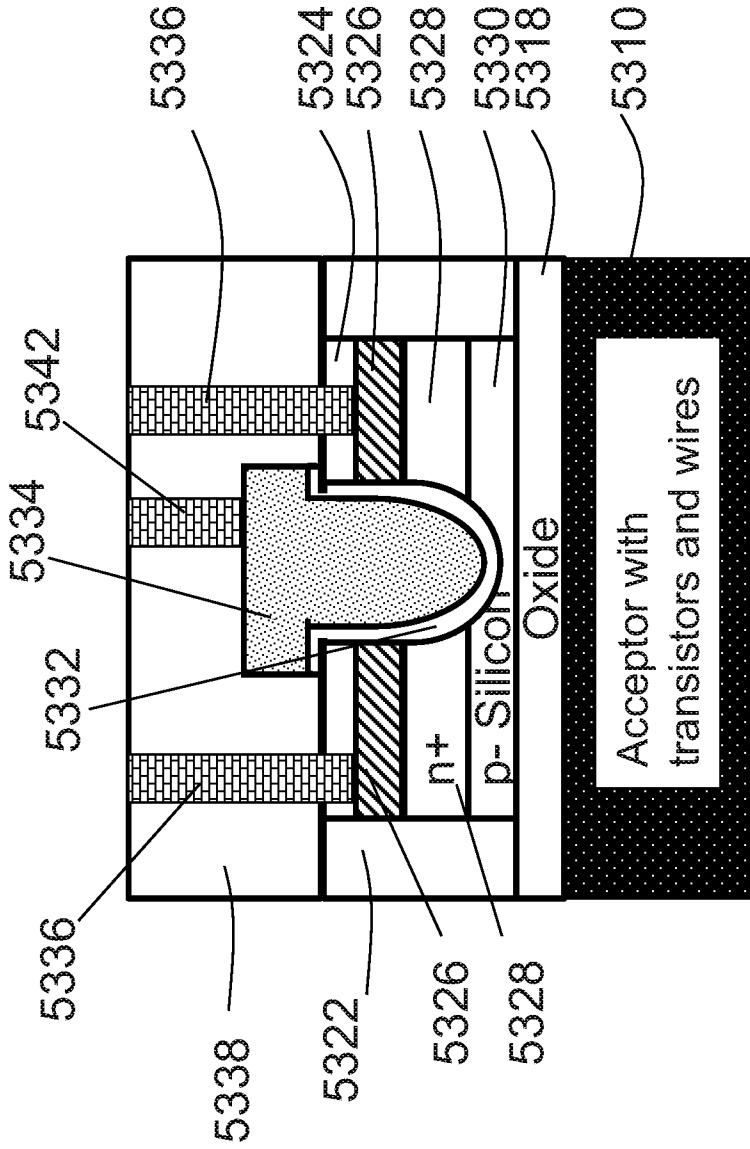
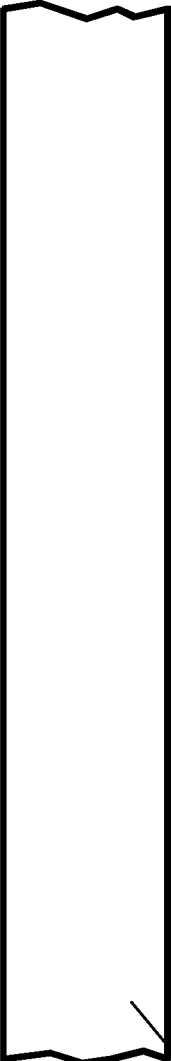


FIG. 531



5400

FIG. 54A

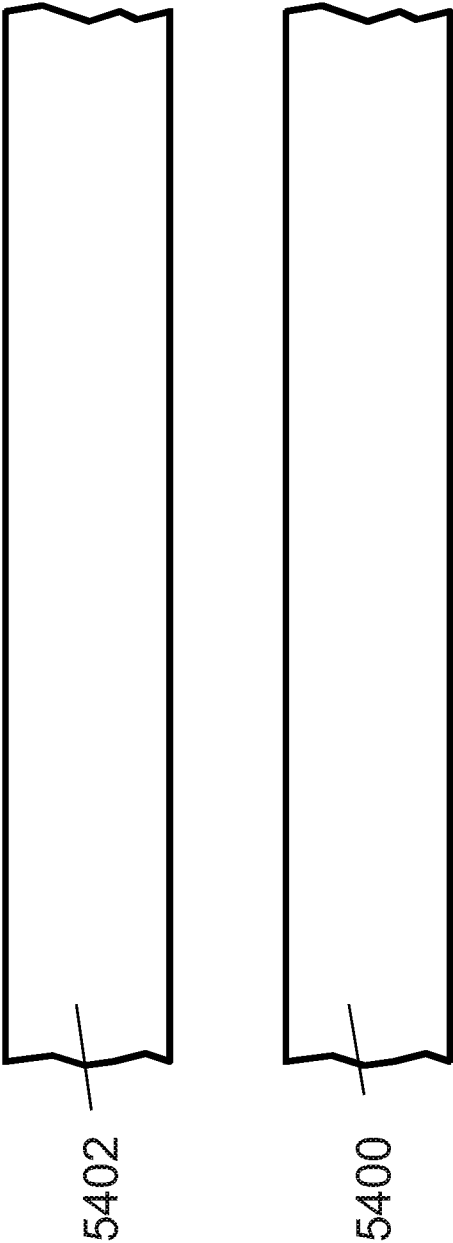


FIG. 54B

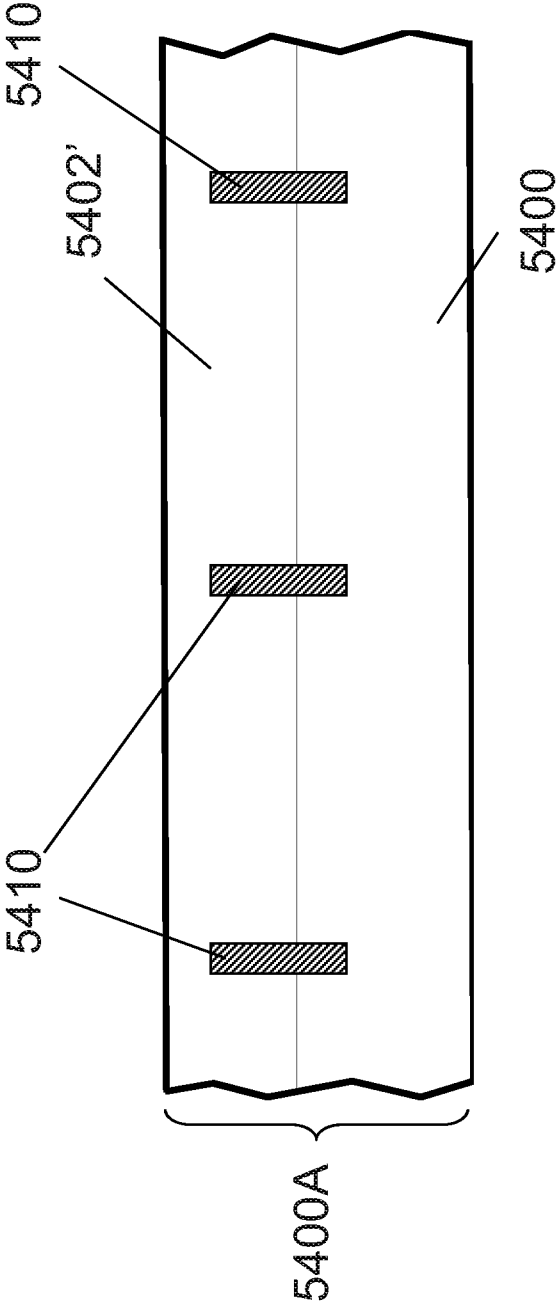


FIG. 54C



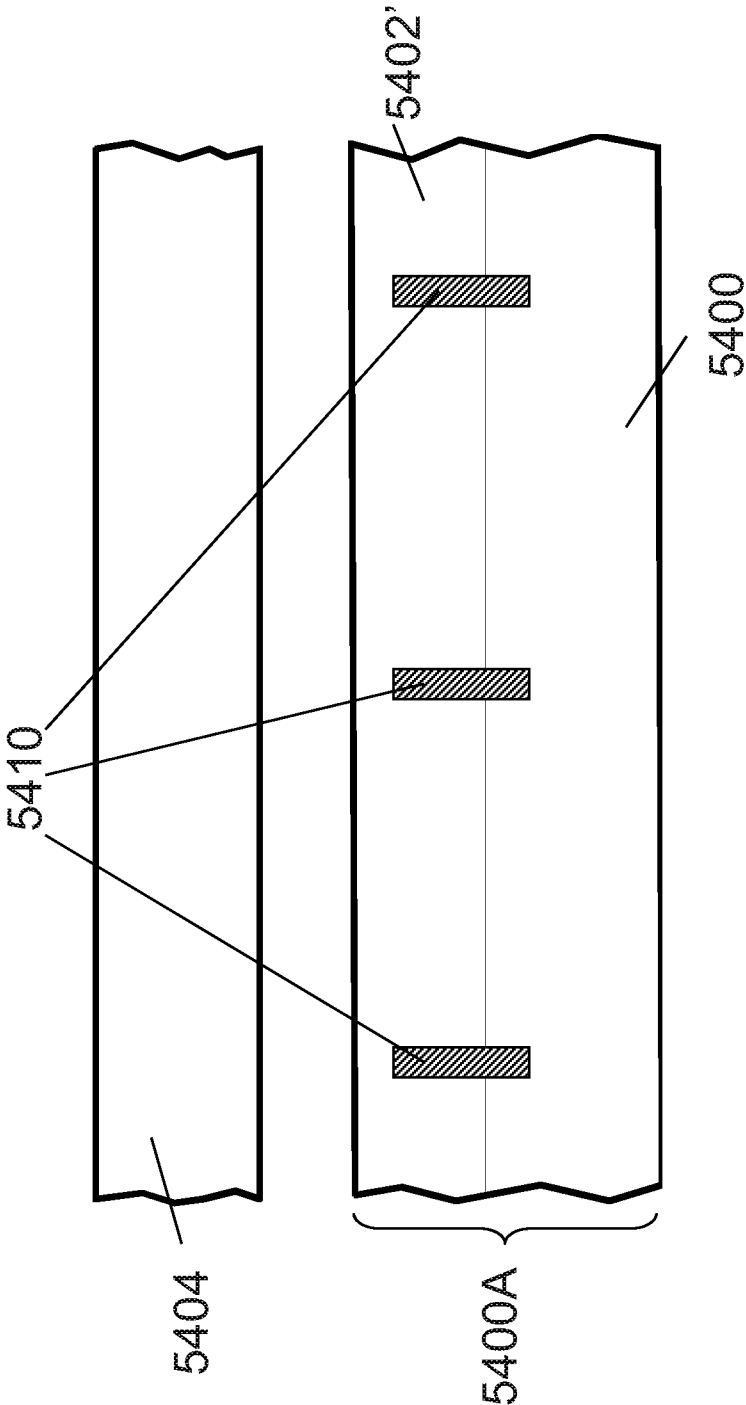


FIG. 54D

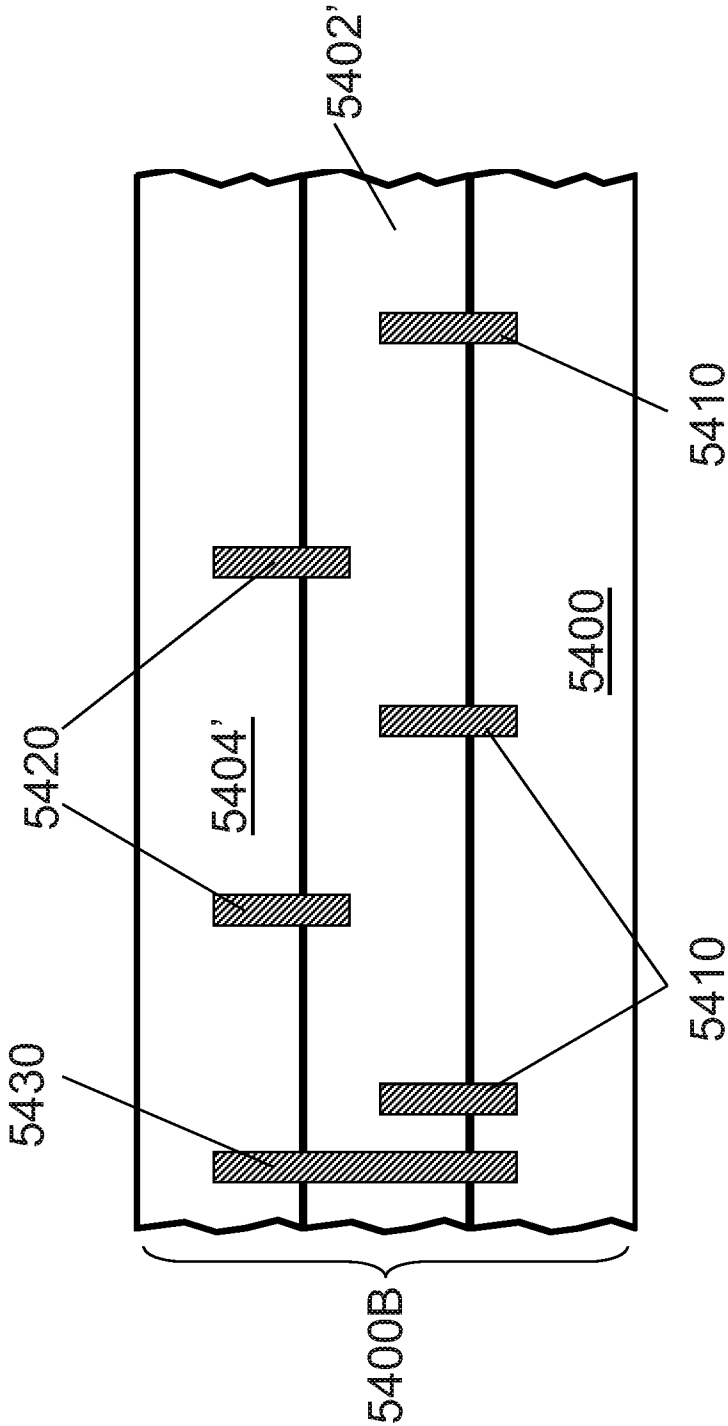
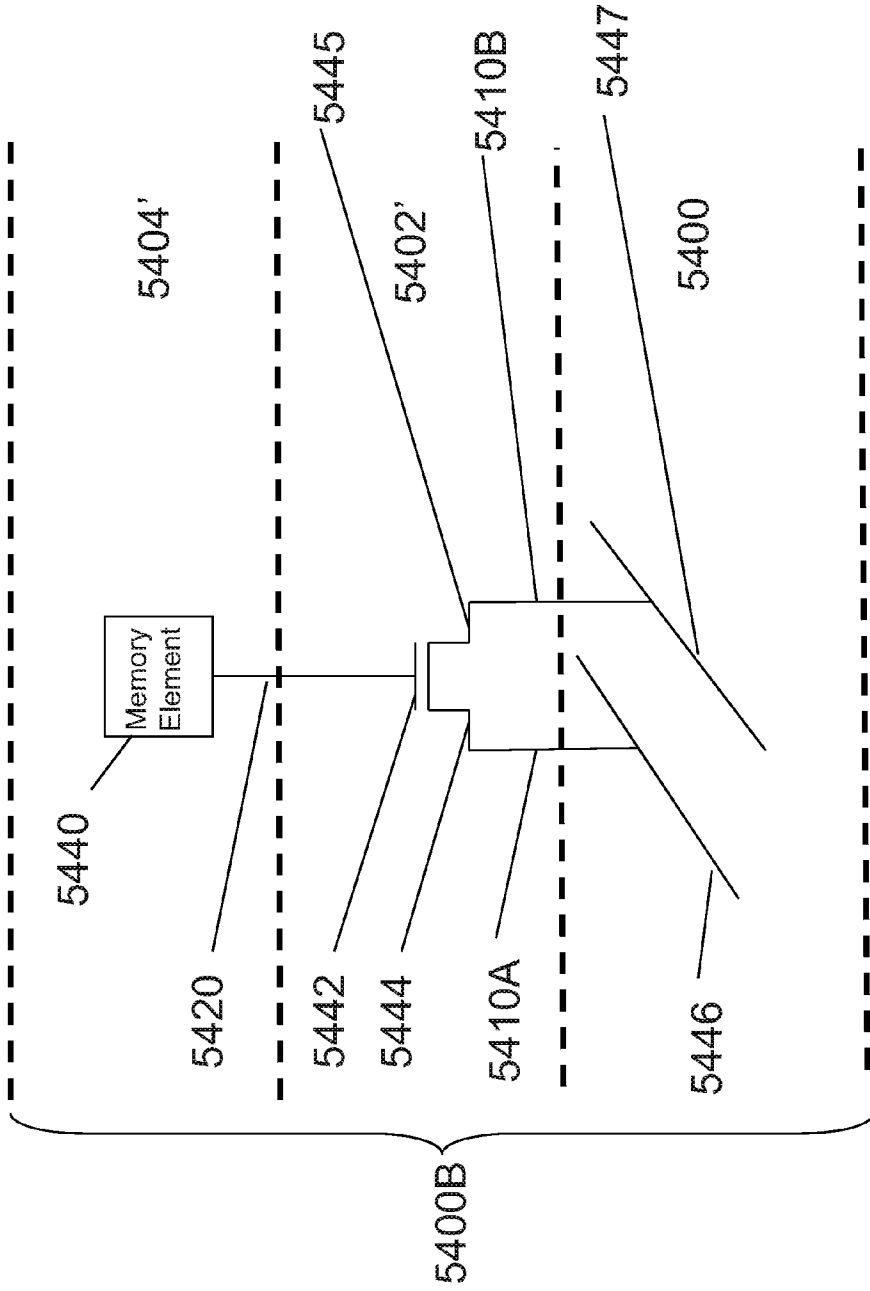
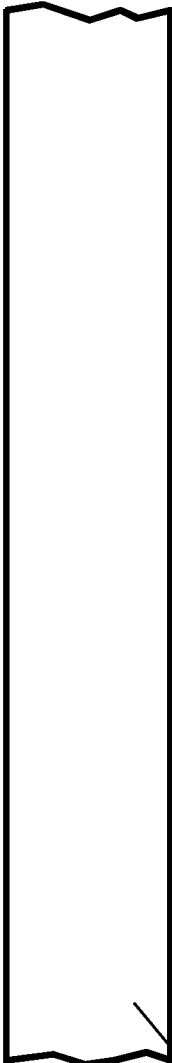


FIG. 54E

FIG. 54F





5500

FIG. 55A

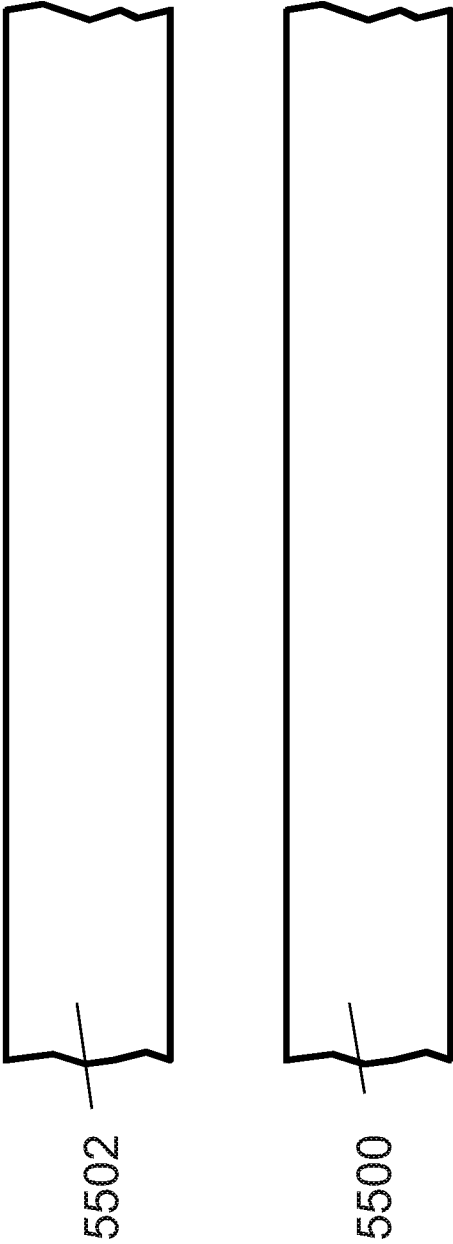


FIG. 55B

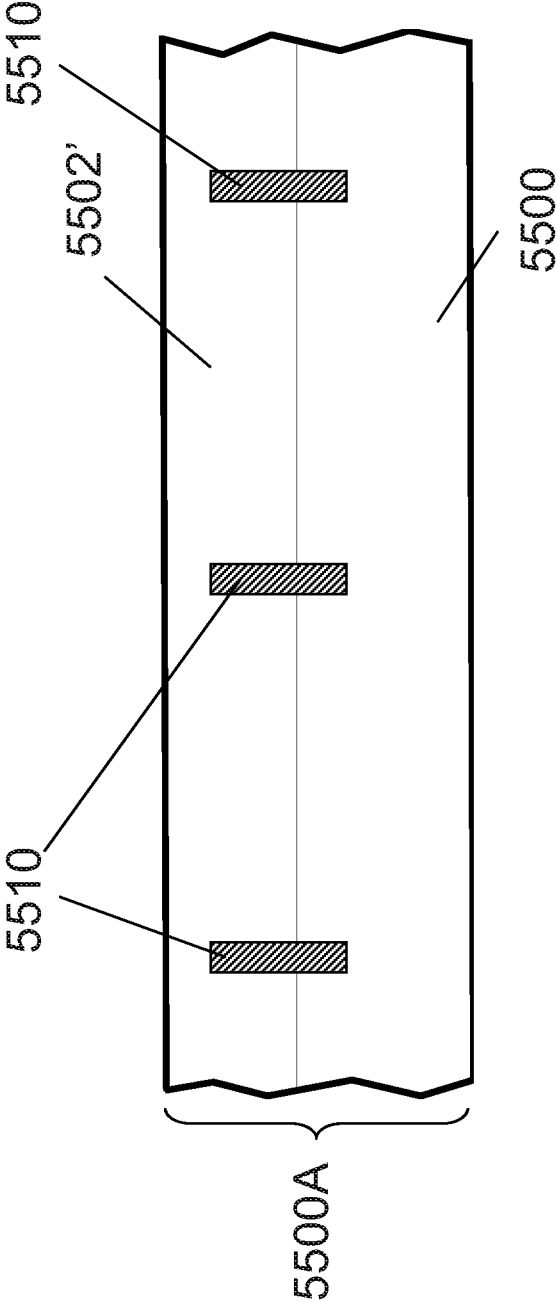
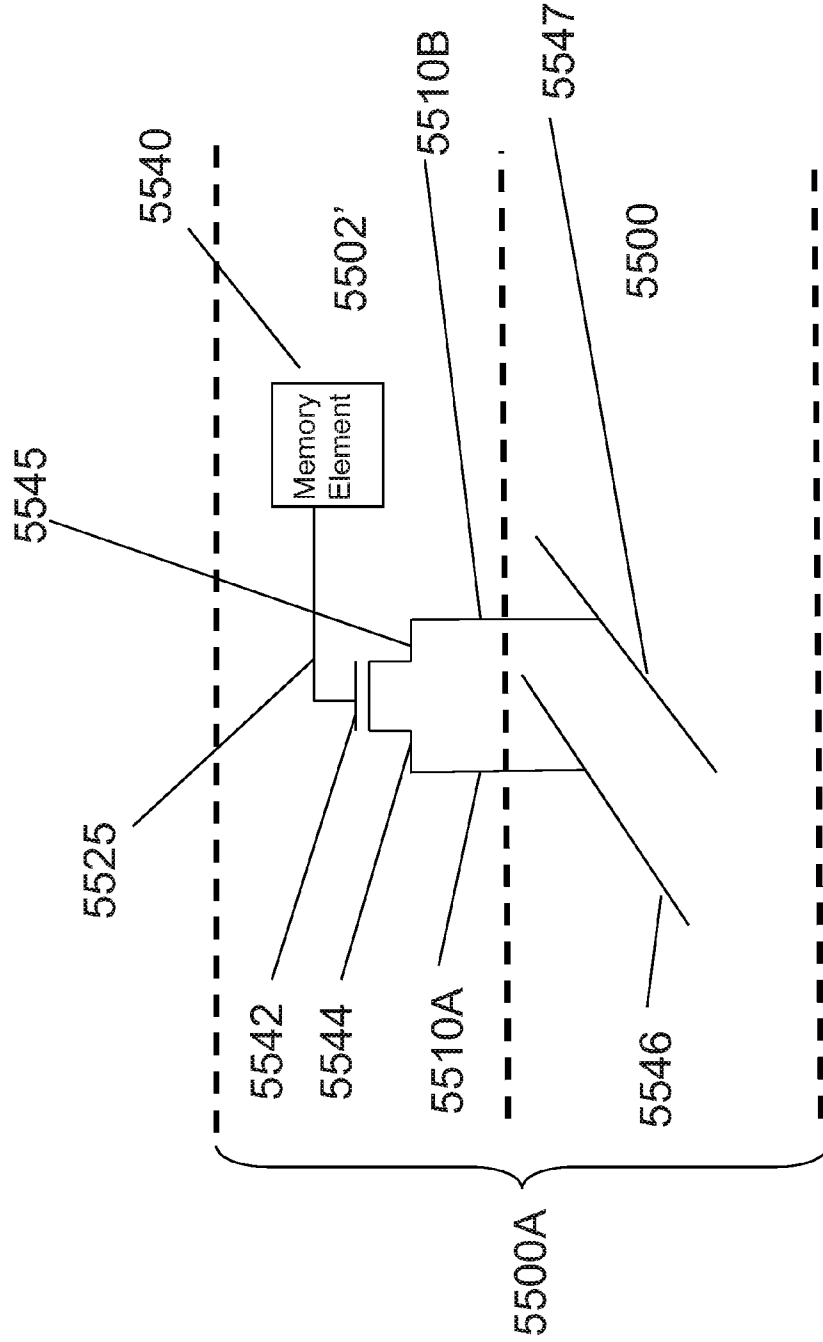


FIG. 55C

FIG. 55D



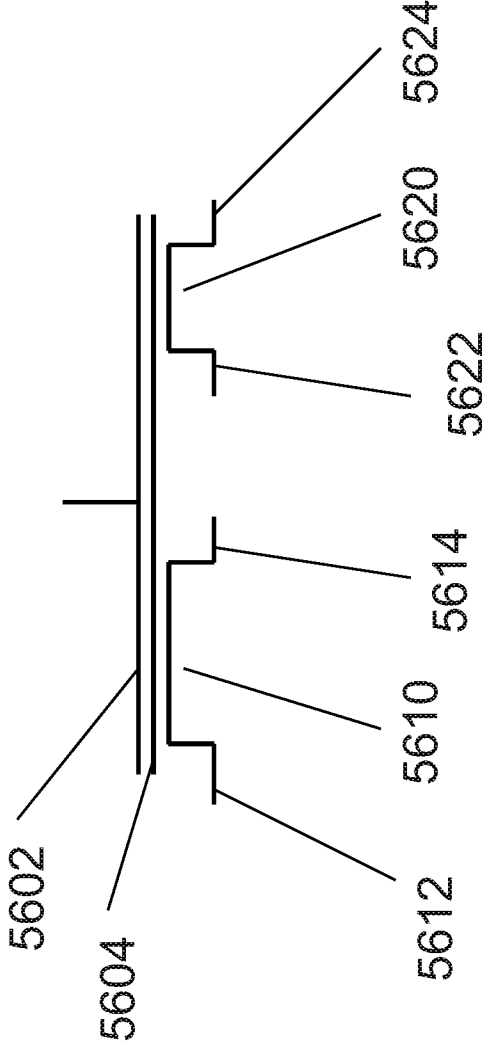


FIG. 56



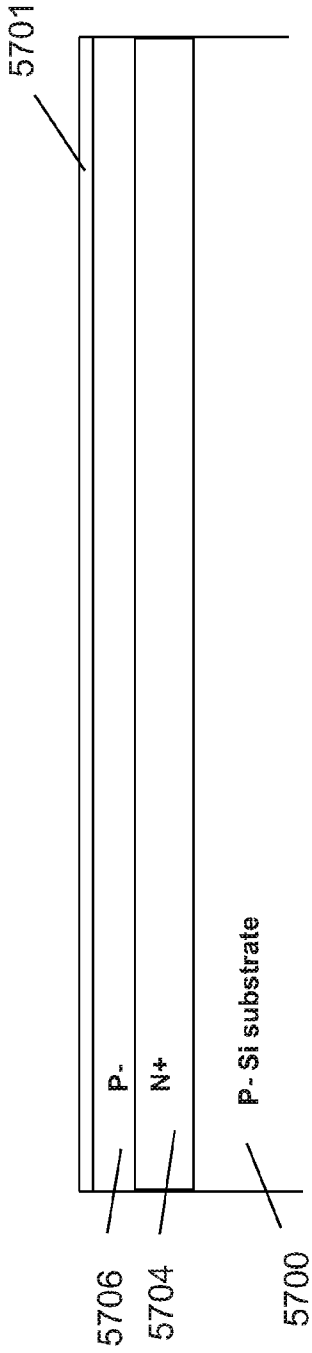


FIG. 57A

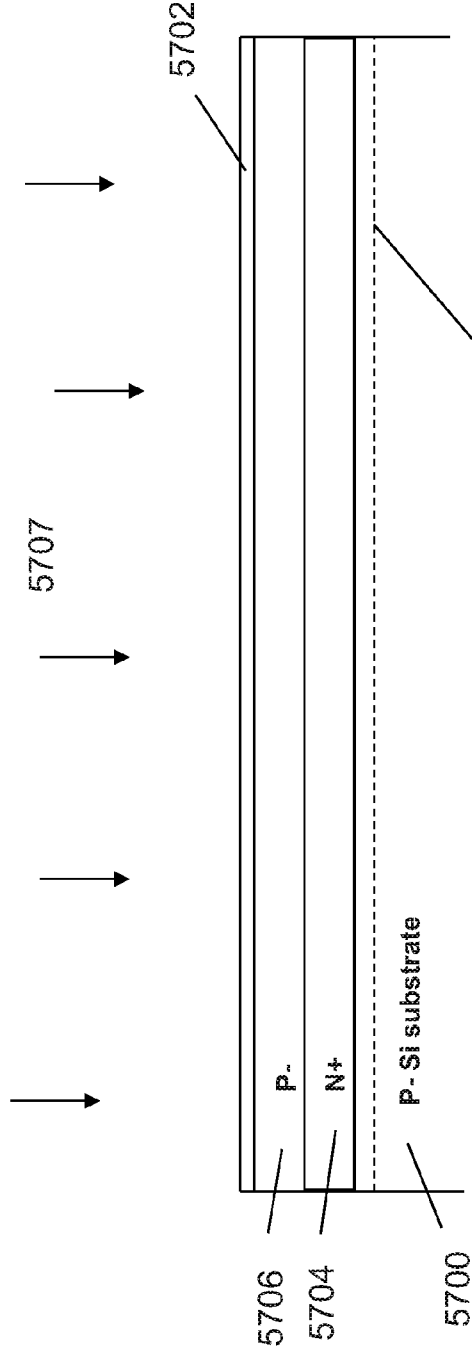


FIG. 57B

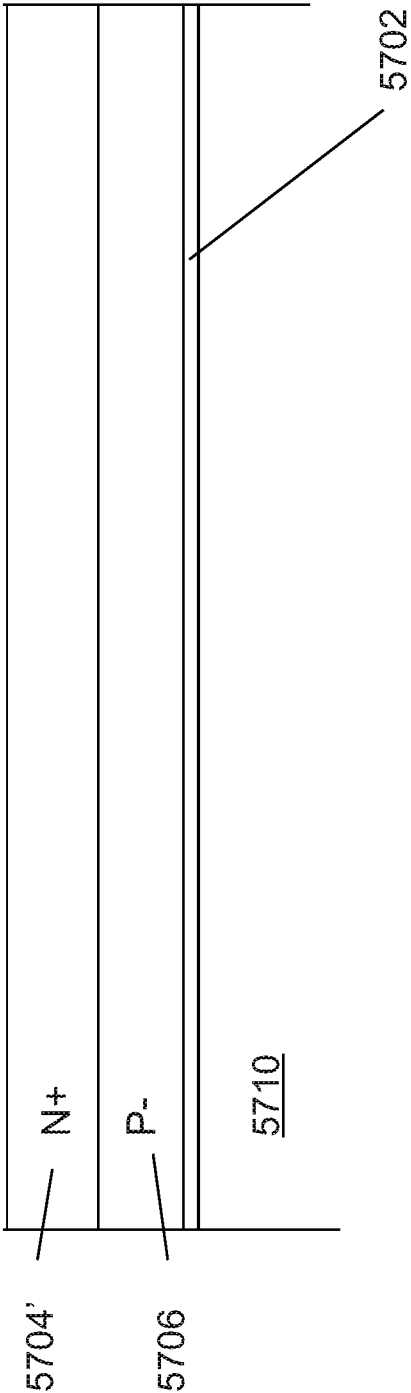
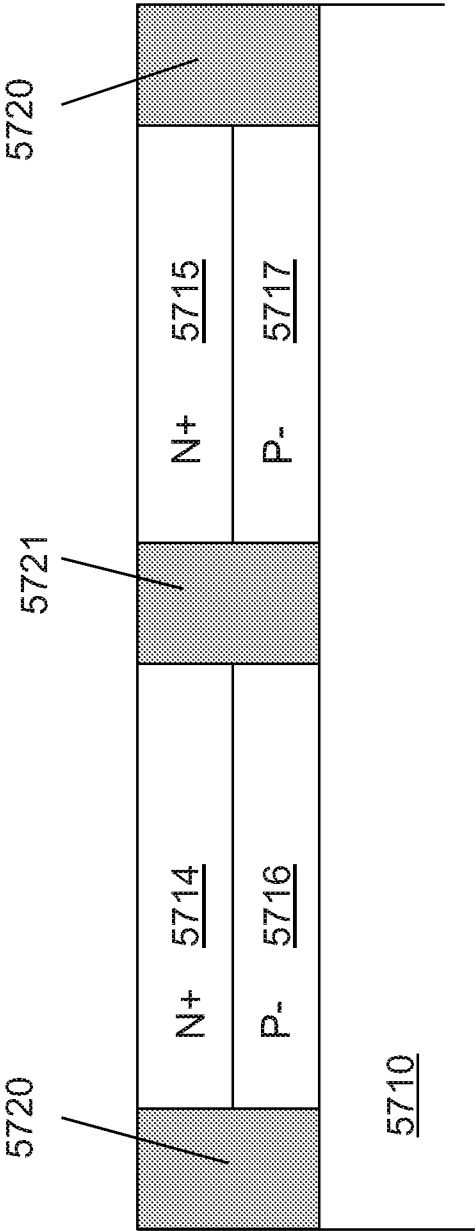


FIG. 57C

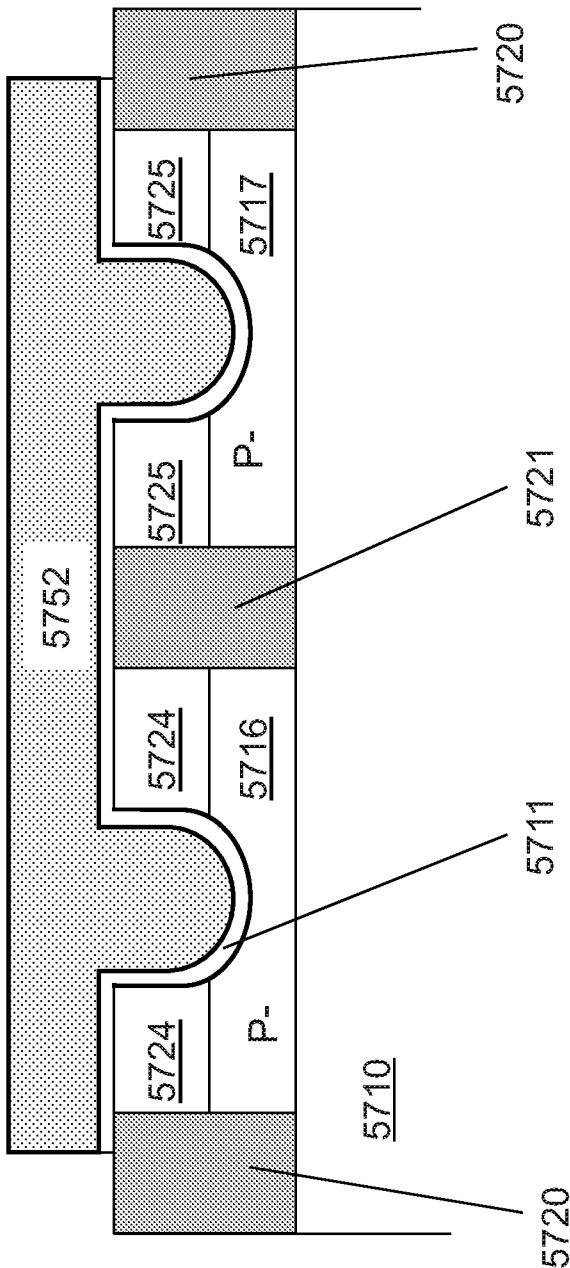


SE

SW

FIG. 57D





SE

FIG. 57F

SW



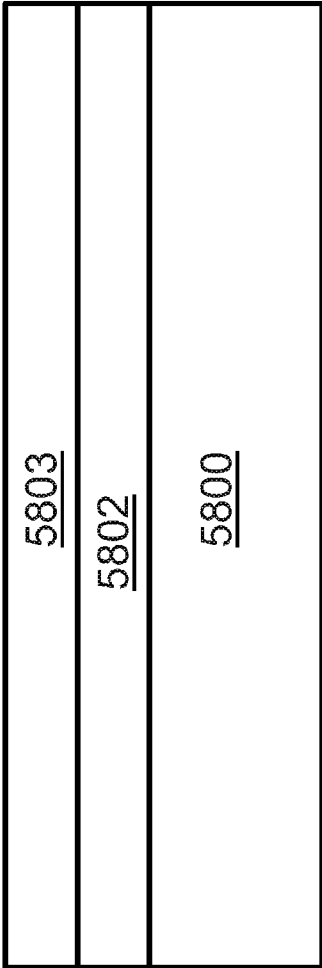


Fig. 58A

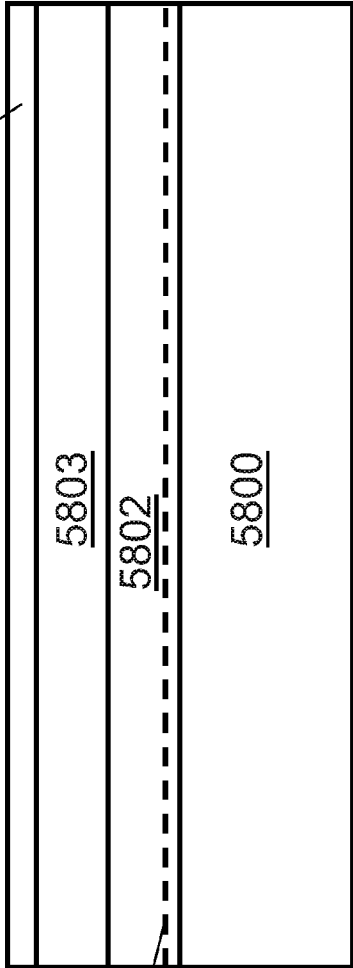


Fig. 58B

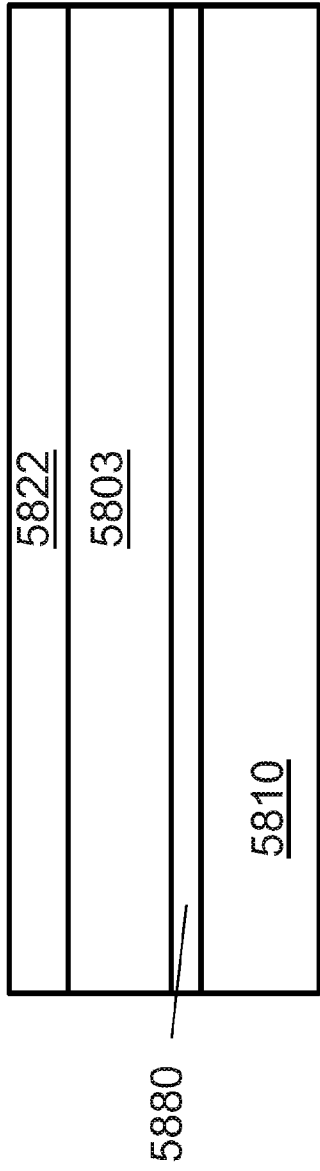


Fig. 58C

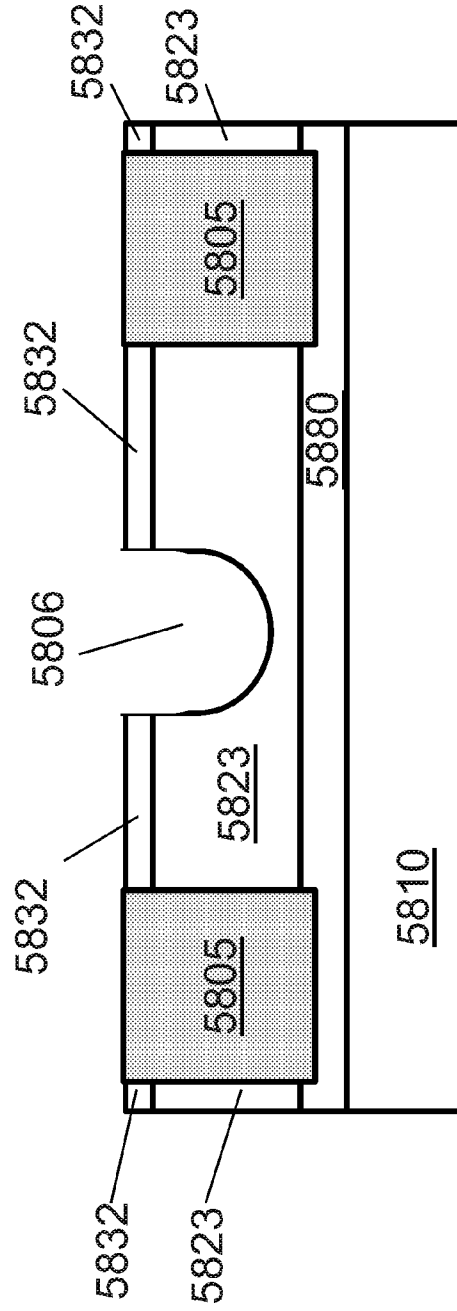


Fig. 58D



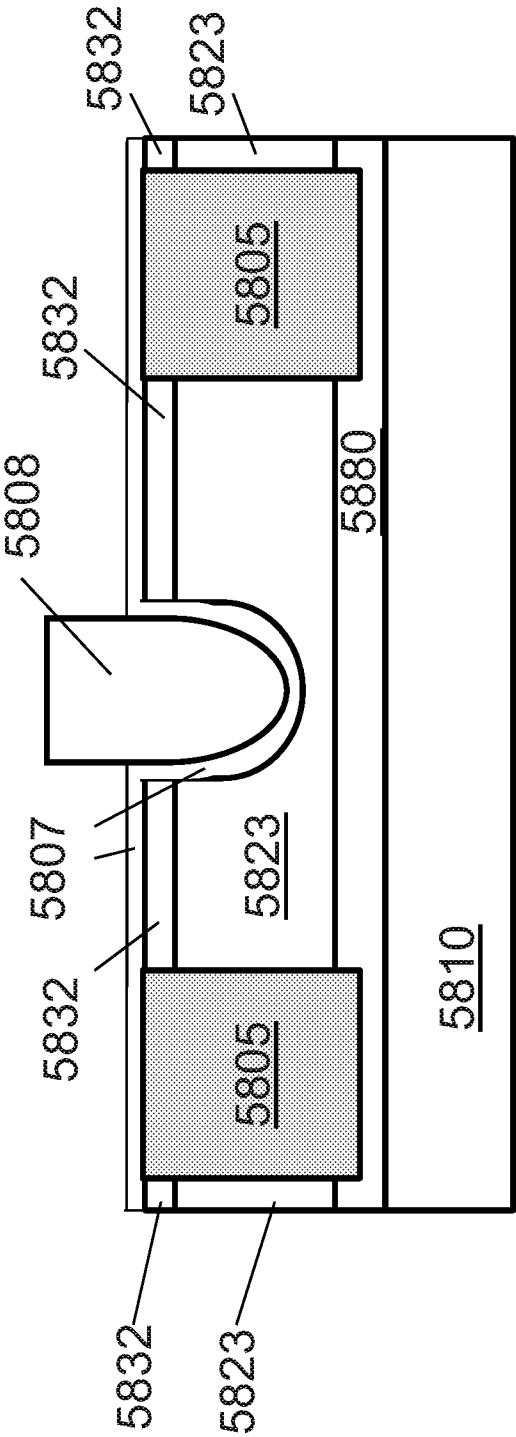


Fig. 58E

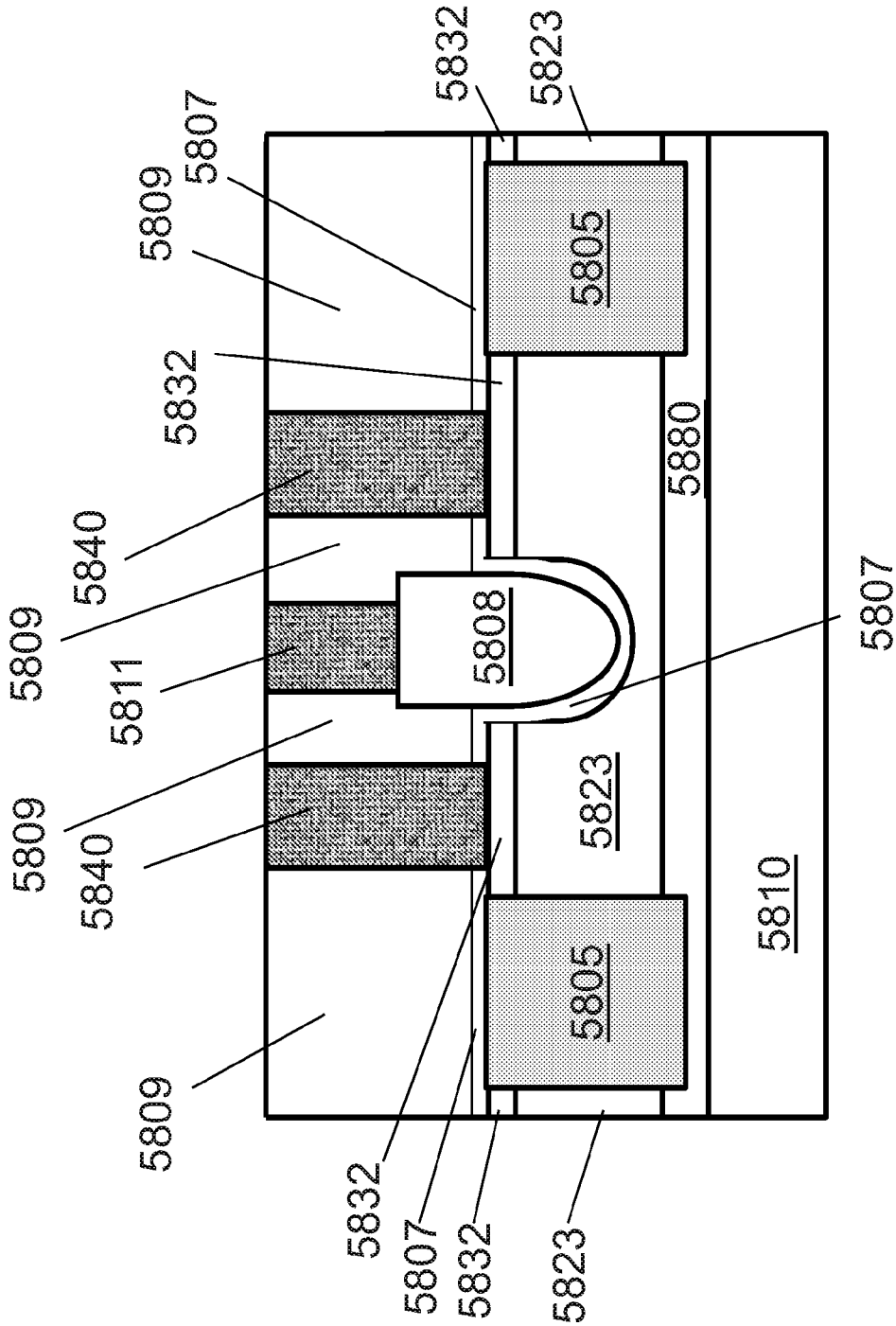


Fig. 58F

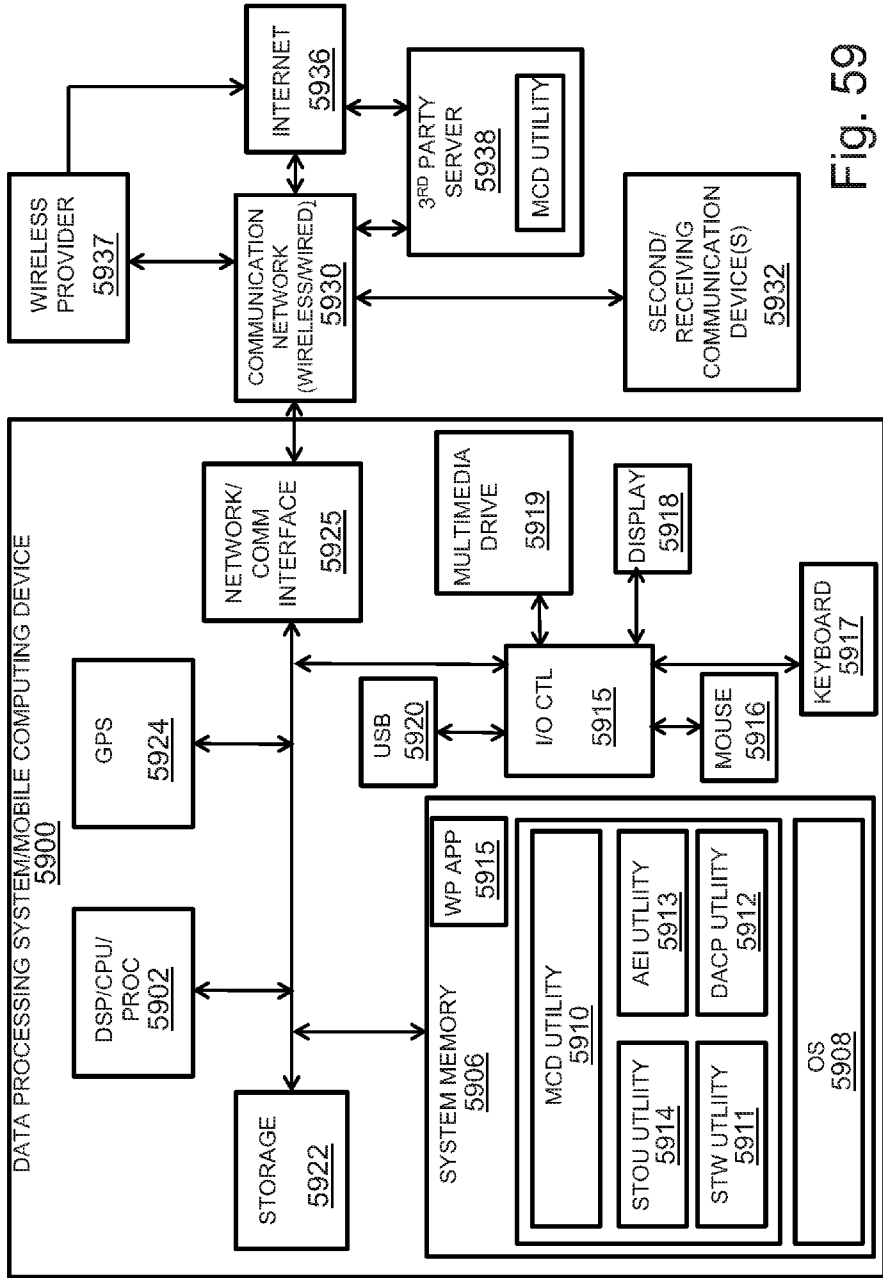


Fig. 59

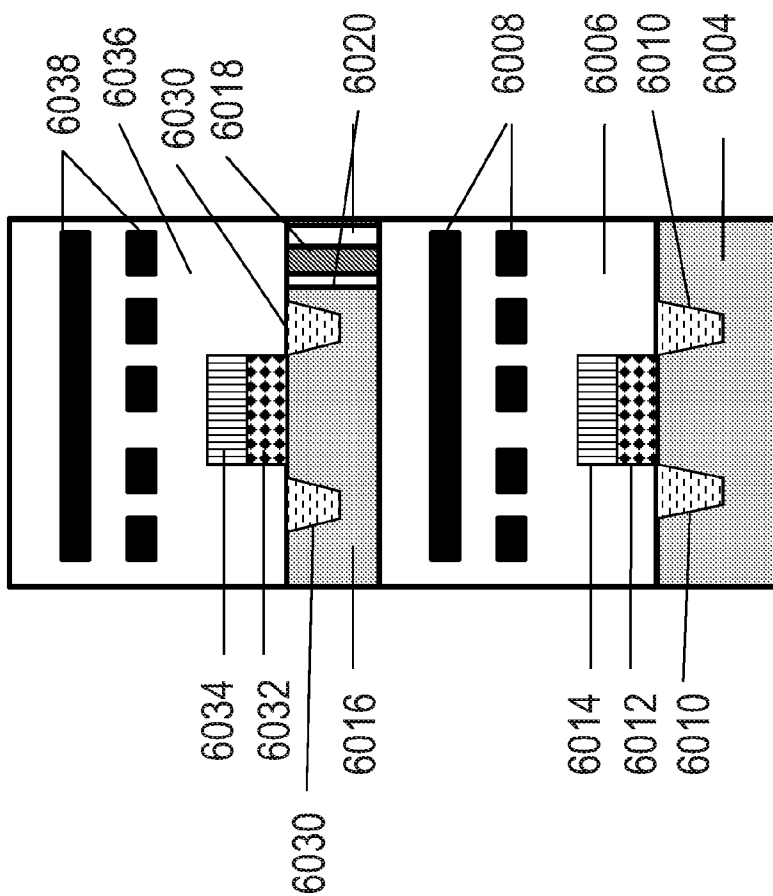


Fig. 60

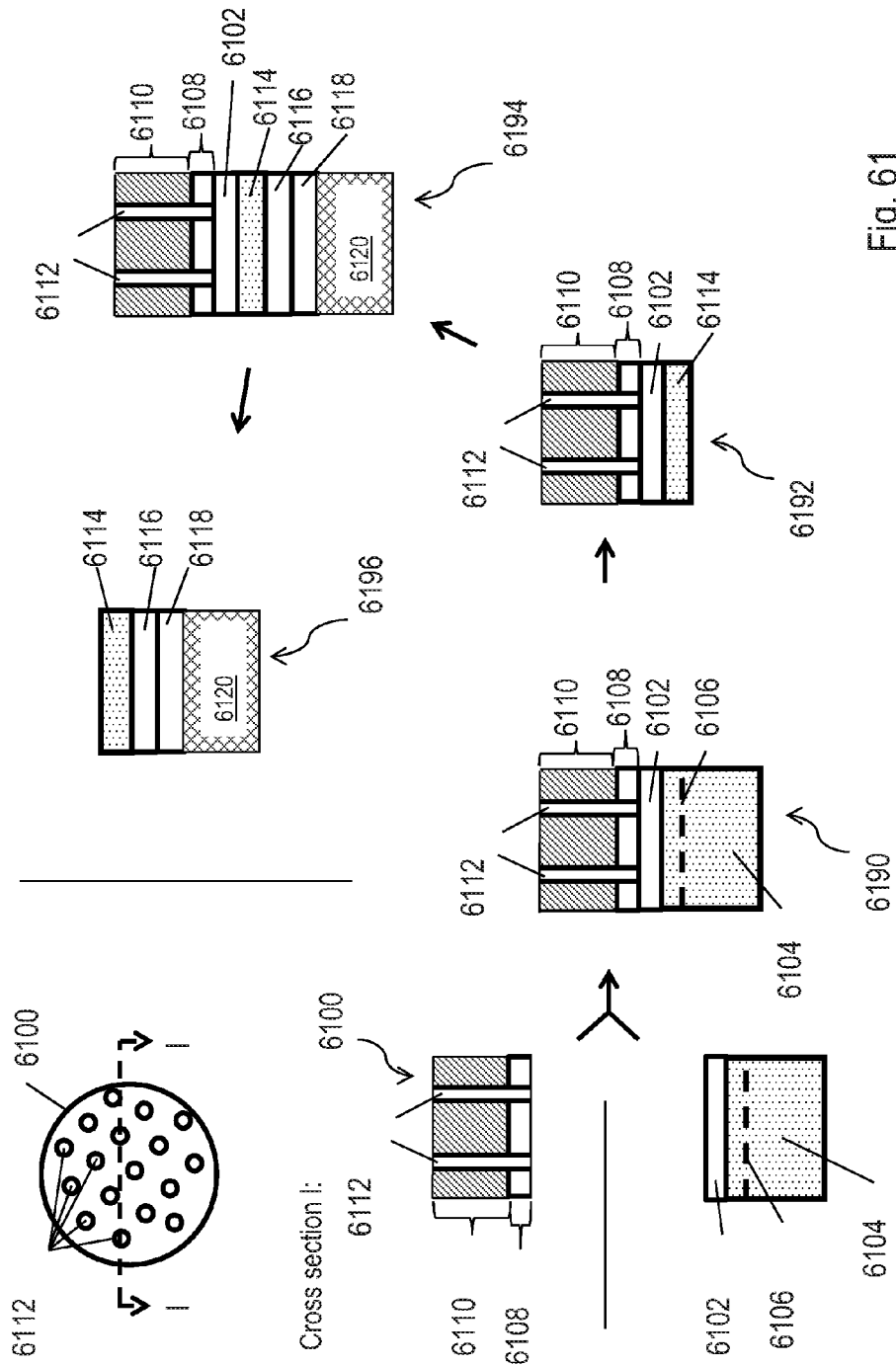


Fig. 61

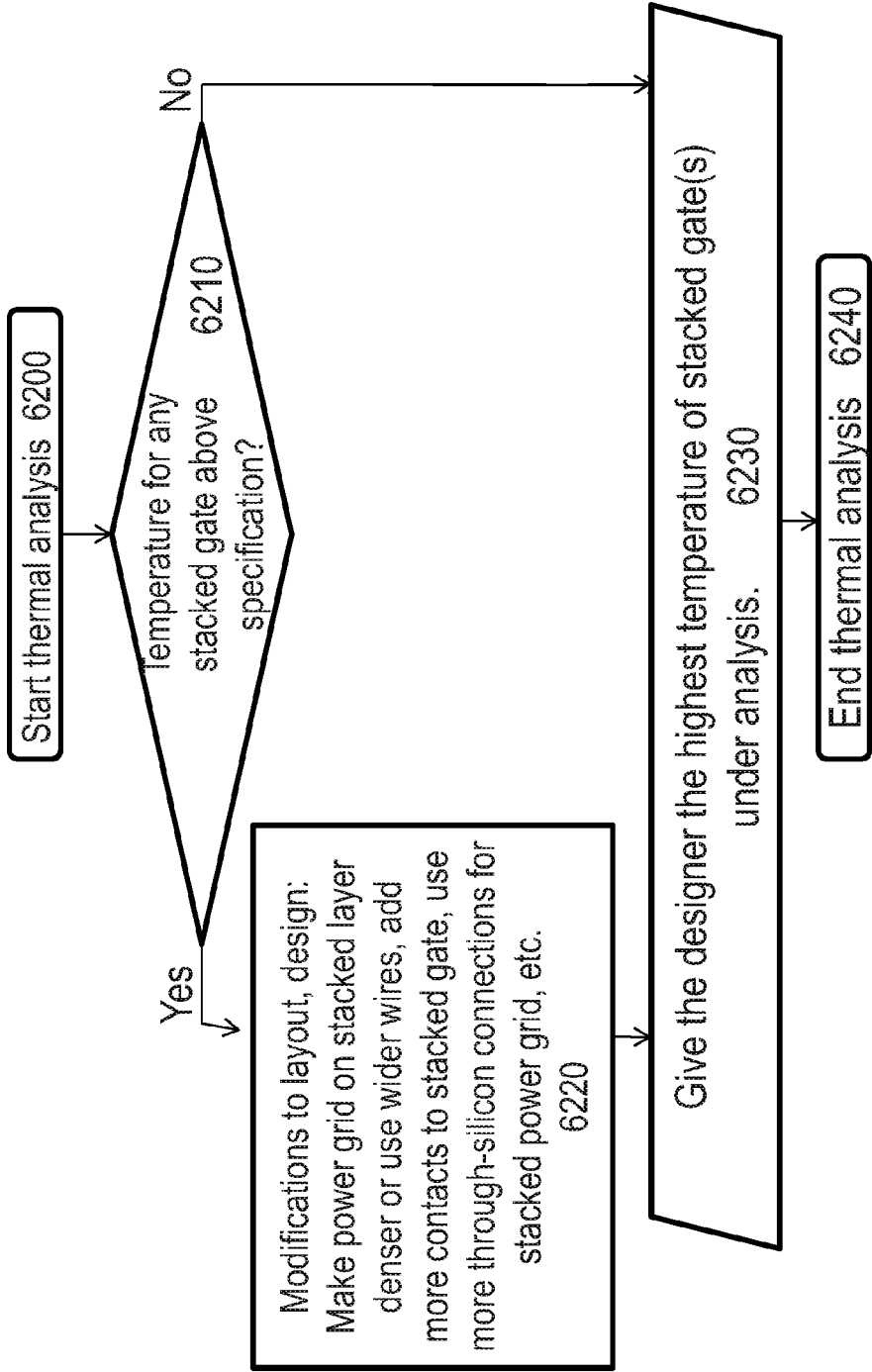


Fig. 62

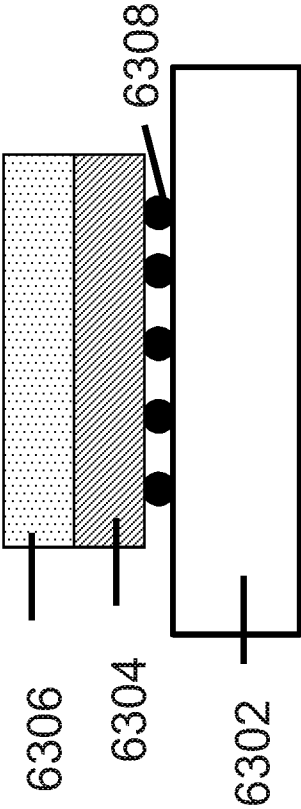


Fig. 63

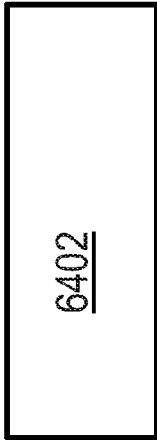


Fig. 64A

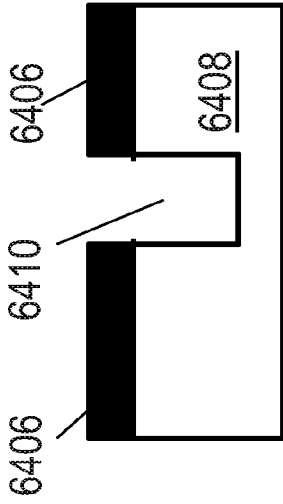


Fig. 64B

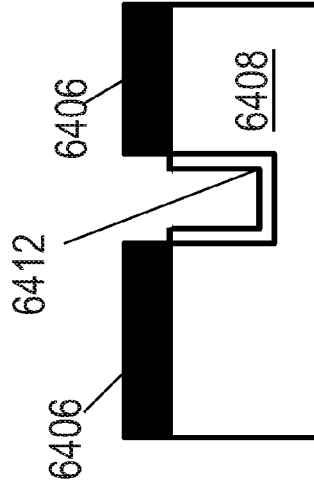


Fig. 64C

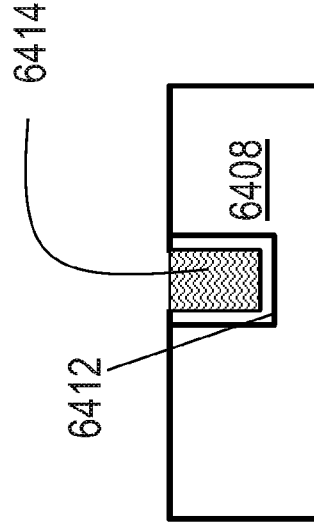


Fig. 64D



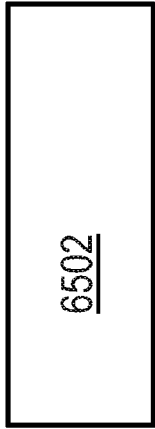


Fig. 65A

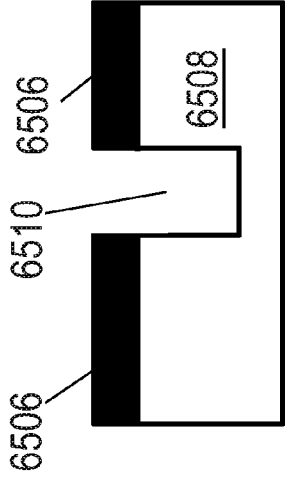


Fig. 65B

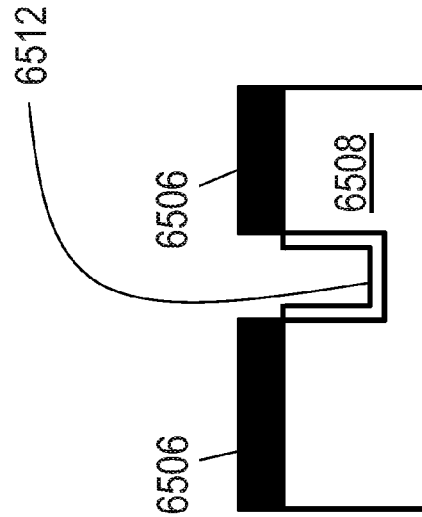


Fig. 65C

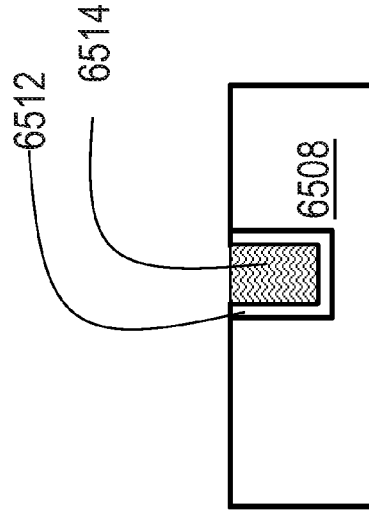


Fig. 65D

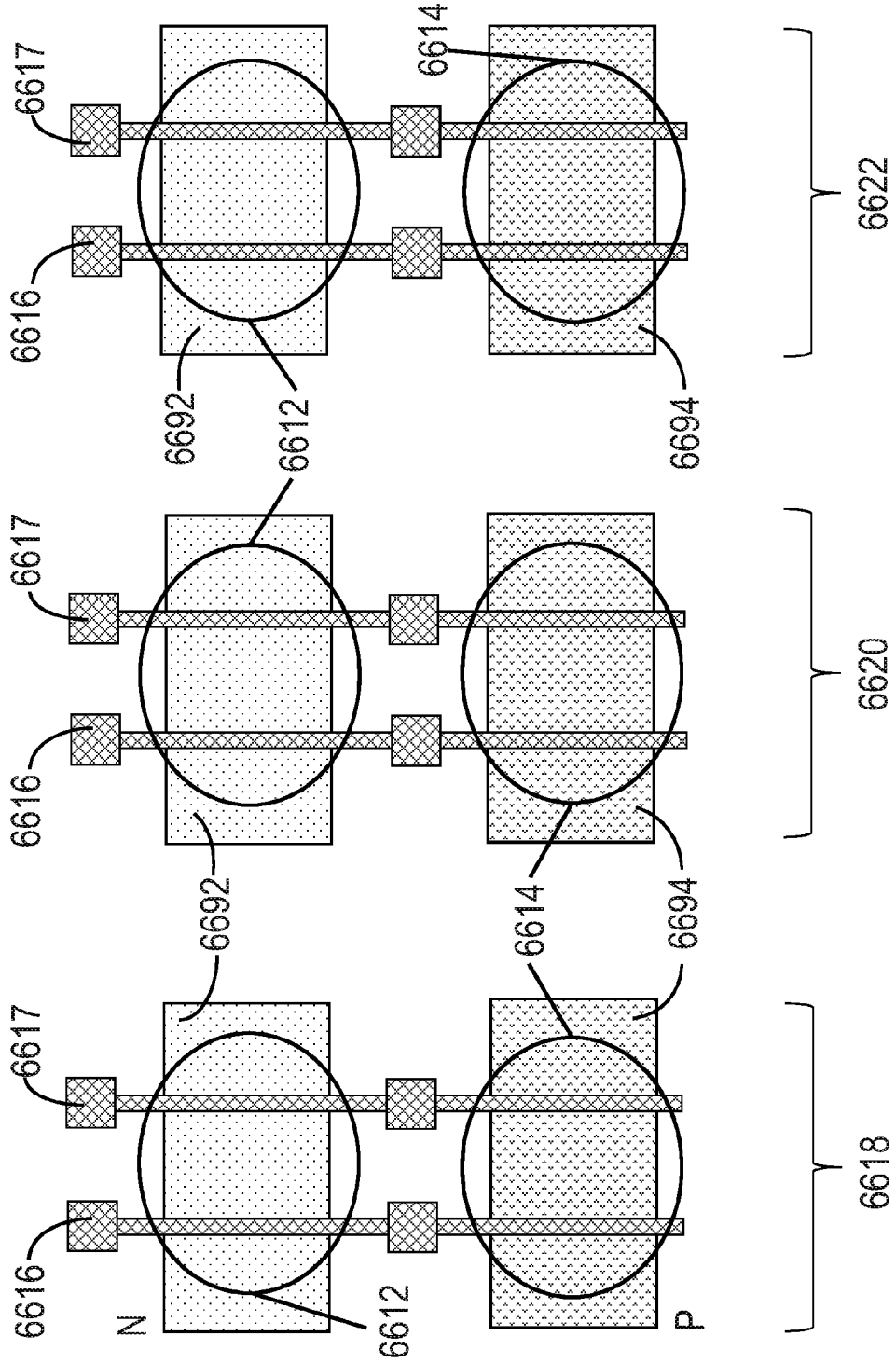


Fig. 66A

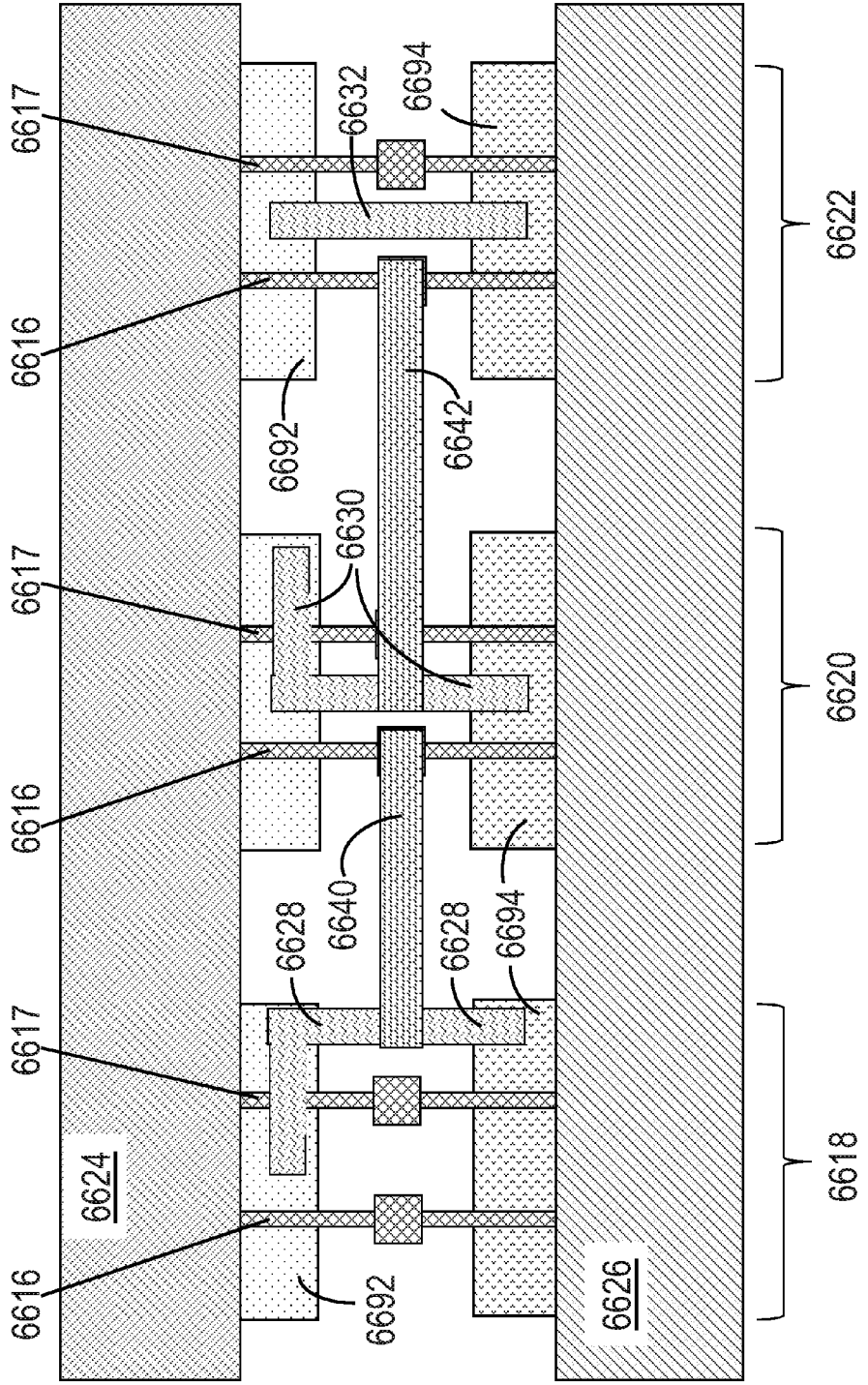


Fig. 66B

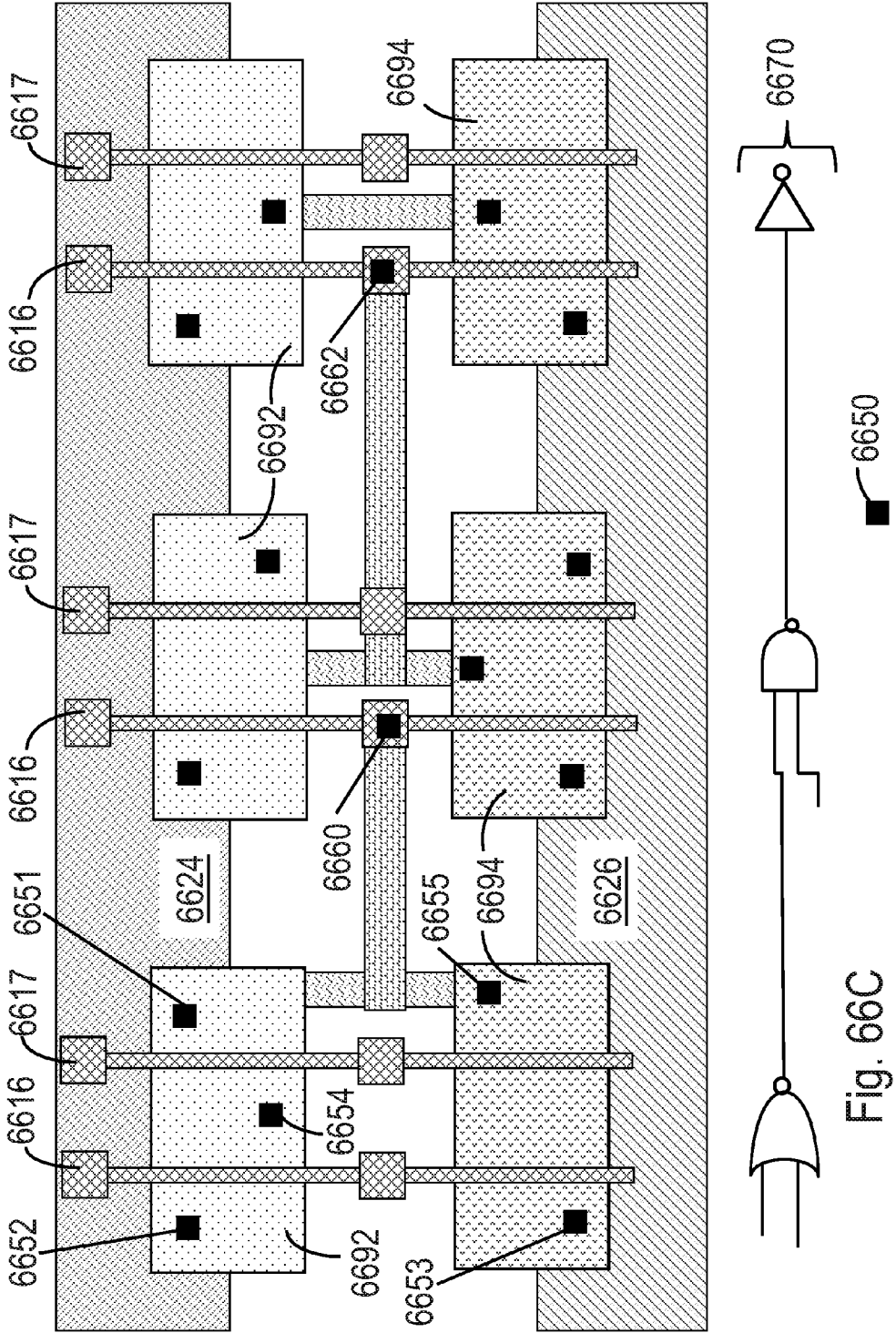


Fig. 66C

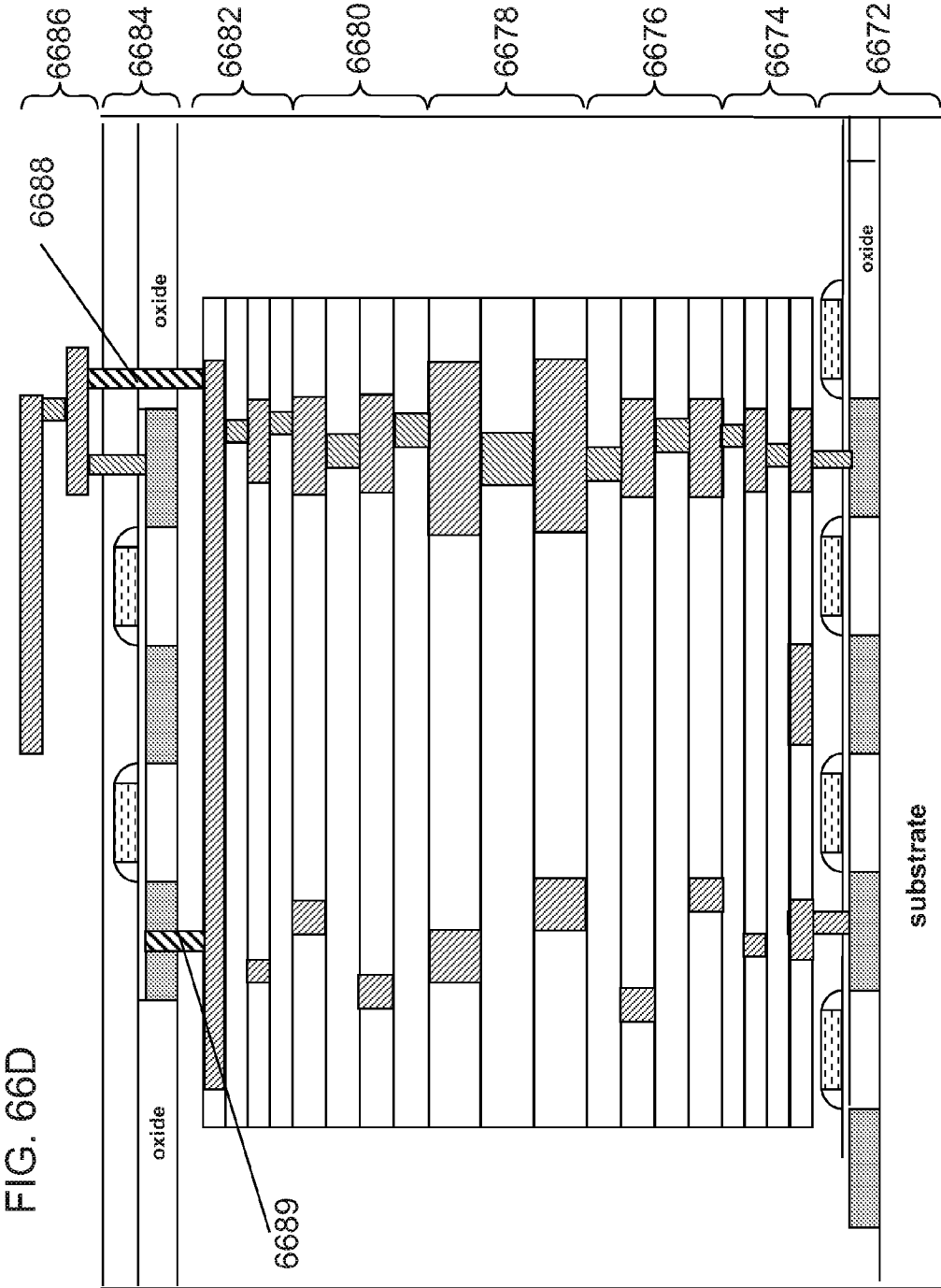


FIG. 66D

## METHOD FOR FABRICATION OF A SEMICONDUCTOR DEVICE AND STRUCTURE

[0001] This application claims priority of co-pending U.S. patent application Ser. Nos. 12/706,520, 12/792,673, 12/847,911, 12/859,665, 12/901,890, 12/894,235, 12/900,379, 12/904,114, 12/963,659, 13/041,404, 13/251,269, 13/423,199, and PCT/US2011/042071, the contents of which are incorporated by reference.

### BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This application relates to the general field of Integrated Circuit (IC) devices and fabrication methods, and more particularly to multilayer or Three Dimensional Integrated Circuit (3D IC) devices and fabrication methods.

[0004] 2. Discussion of Background Art

[0005] Performance enhancements and cost reductions in generations of electronic device technology has generally been achieved by reducing the size of the device, resulting in an enhancement in device speed and a reduction in the area of the device, and hence, its cost. This may be generally referred to as 'device scaling'. The dominant electronic device technology in use today may be the Metal-Oxide-Semiconductor field effect transistor (MOSFET) technology.

[0006] Performance and cost are driven by transistor scaling and the interconnection, or wiring, between those transistors. As the dimensions of the device elements have approached the nanometer scale, the interconnection wiring now dominates the performance, power, and density of integrated circuit devices as described in J. A. Davis, et. al., Proc. IEEE, vol. 89, no. 3, pp. 305-324, March 2001 (Davis).

[0007] Davis further teaches that three dimensional integrated circuits (3D ICs), i.e. electronic chips in which active layers of transistors are stacked one above the other, separated by insulating oxides and connected to each other by metal interconnect wires, may be the best way to continue Moore's Law, especially as device scaling slows, stops, or becomes too costly to continue. 3D integration would provide shorter interconnect wiring and hence improved performance, lower power consumption, and higher density devices.

[0008] One approach to a practical implementation of a 3D IC independently processes two fully interconnected integrated circuits including transistors and wiring, thins one of the wafers, bonds the two wafers together, and then makes electrical connections between the bonded wafers with Thru Silicon Vias (TSV) that may be fabricated prior to or after the bonding. This approach may be less than satisfactory as the density of TSVs may be limited, because they may require large landing pads for the TSVs to overcome the poor wafer to wafer alignment and to allow for the large (about one to ten micron) diameter of the TSVs as a result of the thickness of the wafers bonded together. Additionally, handling and processing thinned silicon wafers may be very difficult and prone to yield loss. Current prototypes of this approach only obtain TSV densities of 10,000s per chip, in comparison to the millions of interconnections currently obtainable within a single chip.

[0009] By utilizing Silicon On Insulator (SOI) wafers and glass handle wafers, A. W. Topol, et. al, in the IEDM Tech Digest, p 363-5 (2005), describe attaining TSVs of tenths of microns. The TSV density may be still limited as a result from misalignment issues resulting from pre-forming the random

circuitry on both wafers prior to wafer bonding. In addition, SOI wafers are more costly than bulk silicon wafers.

[0010] Another approach may be to monolithically build transistors on top of a wafer of interconnected transistors. The utility of this approach may be limited by the requirement to maintain the reliability of the high performance lower layer interconnect metallization, such as, for example, aluminum and copper, and low-k intermetal dielectrics, and hence limits the allowable temperature exposure to below approximately 400° C. Some of the processing steps to create useful transistor elements may require temperatures above about 700° C., such as activating semiconductor doping or crystallization of a previously deposited amorphous material such as silicon to create a poly-crystalline silicon (polysilicon or poly) layer. It may be very difficult to achieve high performance transistors with only low temperature processing and without mono-crystalline silicon channels. However, this approach may be useful to construct memory devices where the transistor performance may not be critical.

[0011] Bakir and Meindl in the textbook "Integrated Interconnect Technologies for 3D Nanosystems", Artech House, 2009, Chapter 13, illustrate a 3D stacked Dynamic Random Access Memory (DRAM) where the silicon for the stacked transistors is produced using selective epitaxy technology or laser recrystallization. This concept may be unsatisfactory as the silicon processed in this manner may have a higher defect density when compared to single crystal silicon and hence may suffer in performance, stability, and control. It may also require higher temperatures than the underlying metallization or low-k intermetal dielectric could be exposed to without reliability concerns.

[0012] Sang-Yun Lee in U.S. Pat. No. 7,052,941 discloses methods to construct vertical transistors by preprocessing a single crystal silicon wafer with doping layers activated at high temperature, layer transferring the wafer to another wafer with preprocessed circuitry and metallization, and then forming vertical transistors from those doping layers with low temperature processing, such as etching silicon. This may be less than satisfactory as the semiconductor devices in the market today utilize horizontal or horizontally oriented transistors and it would be very difficult to convince the industry to move away from the horizontal. Additionally, the transistor performance may be less than satisfactory as a result from large parasitic capacitances and resistances in the vertical structures, and the lack of self-alignment of the transistor gate.

[0013] A key technology for 3D IC construction may be layer transfer, whereby a thin layer of a silicon wafer, called the donor wafer, may be transferred to another wafer, called the acceptor wafer, or target wafer. As described by L. DiCiccio, et. al., at ICICDT 2010 pg 110, the transfer of a thin (about tens of microns to tens of nanometers) layer of mono-crystalline silicon at low temperatures (below approximately 400° C.) may be performed with low temperature direct oxide-oxide bonding, wafer thinning, and surface conditioning. This process is called "Smart Stacking" by Soitec (Crolles, France). In addition, the "SmartCut" process is a well understood technology used for fabrication of SOI wafers. The "SmartCut" process employs a hydrogen implant to enable cleaving of the donor wafer after the layer transfer. These processes with some variations and under different names may be commercially available from SiGen (Silicon Genesis Corporation, San Jose, Calif.). A room temperature wafer bonding process utilizing ion-beam preparation of the

wafer surfaces in a vacuum has been recently demonstrated by Mitsubishi Heavy Industries Ltd., Tokyo, Japan. This process allows room temperature layer transfer.

#### SUMMARY

**[0014]** The invention may be directed to multilayer or Three Dimensional Integrated Circuit (3D IC) devices and fabrication methods.

**[0015]** In one aspect, a method to process an Integrated Circuit device including processing a first layer of first transistors, then processing a first interconnection layer overlaying the first transistors and providing at least one connection to the first transistors, then processing a second interconnection layer overlaying the first interconnection layer, then processing a second layer of second transistors overlaying the second interconnection layer, wherein the second interconnection layer comprises a power grid to provide power to at least one of the second transistors.

**[0016]** In another aspect, a method to process an Integrated Circuit device including processing a first layer of first transistors, then processing a first interconnection layer overlaying the first transistors and providing at least one connection to the first transistors, then processing a second interconnection layer overlaying the first interconnection layer, then processing a second layer of second transistors overlaying the second interconnection layer, then processing the second transistors interconnections forming logic cells, wherein at least one of the logic cells interconnection includes a connection made by the second interconnection layer.

**[0017]** In another aspect, a method for formation of a semiconductor device including a first wafer comprising a first single crystal layer including first transistors and first alignment mark, the method including implanting to form a doped layer within a second wafer; forming a second mono-crystalline layer on top of the first wafer by transferring at least a portion of the doped layer using layer transfer step, and completing the formation of second transistors on the second mono-crystalline layer including a step of forming a gate dielectric followed by second transistors gate formation step, wherein the second transistors are horizontally oriented.

**[0018]** In another aspect, a method to process an Integrated Circuit device including processing a first layer of first transistors, then processing a first interconnection layer overlaying the first transistors and providing at least one connection to the first transistors, then processing a second interconnection layer overlaying the first interconnection layer, then processing a second layer of second transistors overlaying the second interconnection layer, including forming a connection path between the second transistors and the second interconnection layer, wherein the connection path comprises at least one through-layer via, and wherein the through-layer via comprises material whose co-efficient of thermal expansion is within 50 percent of the second layer coefficient of thermal expansion.

**[0019]** Implementations of the above aspects may include one or more of the following. The carrier is a wafer and said performing a transfer comprises performing an ion-cut operation. The method includes forming first transistors and metal layers providing interconnection between said first transistors, wherein said metal layers comprise primarily copper or aluminum covered by an isolating layer. Gates can be replaced. The method includes forming a first mono-crystallized semiconductor layer having first transistors and metal layers providing interconnection between said first transis-

tors, wherein said metal layers comprise primarily copper or aluminum covered by an isolating layer; and forming a second mono-crystallized semiconductor layer above or below the first mono-crystallized semiconductor layer having second transistors, wherein said second transistors comprise horizontally oriented transistors. P type and N type transistors can be formed above or below said target wafer.

**[0020]** Illustrated advantages of the embodiments may include one or more of the following. A 3DIC device with horizontal or horizontally oriented transistors and devices in mono-crystalline silicon can be built at low temperatures. The 3D IC construction of partially preformed layers of transistors provides a high density of layer to layer interconnect.

**[0021]** The 3D ICs offer many significant potential benefits, including a small footprint—more functionality fits into a small space. This extends Moore's Law and enables a new generation of tiny but powerful devices. The 3D ICs have improved speed—The average wire length becomes much shorter. Because propagation delay may be proportional to the square of the wire length, overall performance increases. The 3D ICs consume low power—Keeping a signal on-chip reduces its power consumption by ten to a hundred times. Shorter wires also reduce power consumption by producing less parasitic capacitance. Reducing the power budget leads to less heat generation, extended battery life, and lower cost of operation. The vertical dimension adds a higher order of connectivity and opens a world of new design possibilities. Partitioning a large chip to be multiple smaller dies with 3D stacking could potentially improve the yield and reduce the fabrication cost. Heterogeneous integration—Circuit layers can be built with different processes, or even on different types of wafers. This means that components can be optimized to a much greater degree than if built together on a single wafer. Components with incompatible manufacturing could be combined in a single device. The stacked structure hinders attempts to reverse engineer the circuitry. Sensitive circuits may also be divided among the layers in such a way as to obscure the function of each layer. 3D integration allows large numbers of vertical vias between the layers. This allows construction of wide bandwidth buses between functional blocks in different layers. A typical example would be a processor and memory 3D stack, with the cache memory stacked on top of the processor. This arrangement allows a bus much wider than the typical 128 or 256 bits between the cache and processor. Wide buses in turn alleviate the memory wall problem.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0022]** Various embodiments of the invention will be understood and appreciated more fully from the following detailed description, taken in conjunction with the drawings in which:

**[0023]** FIG. 1 is an exemplary drawing illustration of a layer transfer process flow;

**[0024]** FIG. 2A-2H are exemplary drawing illustrations of the preprocessed wafers and layers and generalized layer transfer;

**[0025]** FIG. 3A-D are exemplary drawing illustrations of a generalized layer transfer process flow;

**[0026]** FIG. 4A-4J are exemplary drawing illustrations of formations of top planar transistors;

**[0027]** FIG. 5 are exemplary drawing illustrations of recessed channel array transistors;

- [0028] FIG. 6A-G are exemplary drawing illustrations of formation of a recessed channel array transistor;
- [0029] FIG. 7A-G are exemplary drawing illustrations of formation of a spherical recessed channel array transistor;
- [0030] FIG. 8 is an exemplary drawing illustration and a transistor characteristic graph of a junction-less transistor (prior art);
- [0031] FIG. 9A-H are exemplary drawing illustrations of the formation of a junction-less transistor;
- [0032] FIG. 10A-H are exemplary drawing illustrations of the formation of a junction-less transistor;
- [0033] FIG. 11A-H are exemplary drawing illustrations of the formation of a junction-less transistor;
- [0034] FIG. 12A-J are exemplary drawing illustrations of the formation of a junction-less transistor;
- [0035] FIG. 13A, 13B are exemplary device simulations of a junction-less transistor;
- [0036] FIG. 14A-I are exemplary drawing illustrations of the formation of a junction-less transistor;
- [0037] FIG. 15A-I are exemplary drawing illustrations of the formation of a JFET transistor;
- [0038] FIG. 16A-G are exemplary drawing illustrations of the formation of a JFET transistor;
- [0039] FIG. 17A-G are exemplary drawing illustrations of the formation of a bipolar transistor;
- [0040] FIG. 18A-J are exemplary drawing illustrations of the formation of a raised source and drain extension transistor;
- [0041] FIG. 19A-J are exemplary drawing illustrations of formation of CMOS recessed channel array transistors;
- [0042] FIG. 20A-P are exemplary drawing illustrations of steps for formation of 3D cells;
- [0043] FIG. 21 is an exemplary drawing illustration of the basics of floating body DRAM;
- [0044] FIG. 22A-H are exemplary drawing illustrations of the formation of a floating body DRAM transistor;
- [0045] FIG. 23A-M are exemplary drawing illustrations of the formation of a floating body DRAM transistor;
- [0046] FIG. 24A-L are exemplary drawing illustrations of the formation of a floating body DRAM transistor;
- [0047] FIG. 25A-K are exemplary drawing illustrations of the formation of a resistive memory transistor;
- [0048] FIG. 26A-L are exemplary drawing illustrations of the formation of a resistive memory transistor;
- [0049] FIG. 27A-M are exemplary drawing illustrations of the formation of a resistive memory transistor;
- [0050] FIG. 28A-F are exemplary drawing illustrations of the formation of a resistive memory transistor;
- [0051] FIG. 29A-G are exemplary drawing illustrations of the formation of a charge trap memory transistor;
- [0052] FIG. 30A-G are exemplary drawing illustrations of the formation of a charge trap memory transistor;
- [0053] FIG. 31A-G are exemplary drawing illustrations of the formation of a floating gate memory transistor;
- [0054] FIG. 32A-H are exemplary drawing illustrations of the formation of a floating gate memory transistor;
- [0055] FIG. 33A is an exemplary drawing illustration of a donor wafer;
- [0056] FIG. 33B is an exemplary drawing illustration of a transferred layer on top of a main wafer;
- [0057] FIG. 33C is an exemplary drawing illustration of a measured alignment offset;
- [0058] FIG. 33D is an exemplary drawing illustration of a connection strip;
- [0059] FIG. 33E is an exemplary drawing illustration of a donor wafer;
- [0060] FIG. 34A-L are exemplary drawing illustrations of the formation of top planar transistors;
- [0061] FIG. 35A-M are exemplary drawing illustrations of the formation of a junction-less transistor;
- [0062] FIG. 36A-H are exemplary drawing illustrations of the formation of top planar transistors;
- [0063] FIG. 37A-G are exemplary drawing illustrations of the formation of top planar transistors;
- [0064] FIG. 38A-E are exemplary drawing illustrations of the formation of top planar transistors;
- [0065] FIG. 39A-F are exemplary drawing illustrations of the formation of top planar transistors;
- [0066] FIG. 40A-K are exemplary drawing illustrations of a formation of top planar transistors;
- [0067] FIG. 41 is an exemplary drawing illustration of a layout for a donor wafer;
- [0068] FIG. 42 A-F are exemplary drawing illustrations of formation of top planar transistors;
- [0069] FIG. 43A is an exemplary drawing illustration of a donor wafer;
- [0070] FIG. 43B is an exemplary drawing illustration of a transferred layer on top of an acceptor wafer;
- [0071] FIG. 43C is an exemplary drawing illustration of a measured alignment offset;
- [0072] FIG. 43D, 43E, 43F are exemplary drawing illustrations of a connection strip;
- [0073] FIG. 44A-C are exemplary drawing illustrations of a layout for a donor wafer;
- [0074] FIG. 45 is an exemplary drawing illustration of a connection strip array structure;
- [0075] FIG. 46 is an exemplary drawing illustration of an implant shield structure;
- [0076] FIG. 47A is an exemplary drawing illustration of a metal interconnect stack prior art;
- [0077] FIG. 47B is an exemplary drawing illustration of a metal interconnect stack;
- [0078] FIG. 48A-D are exemplary drawing illustrations of a generalized layer transfer process flow with alignment windows;
- [0079] FIG. 49A-K are exemplary drawing illustrations of the formation of a resistive memory transistor;
- [0080] FIG. 50A-J are exemplary drawing illustrations of the formation of a resistive memory transistor with periphery on top;
- [0081] FIG. 51 is an exemplary drawing illustration of a heat spreader in a 3D IC;
- [0082] FIG. 52A-B are exemplary drawing illustrations of an integrated heat removal configuration for 3D ICs;
- [0083] FIG. 53A-I are exemplary drawing illustrations of the formation of a recessed channel array transistor with source and drain silicide;
- [0084] FIG. 54A-F are exemplary drawing illustrations of a 3D IC FPGA process flow;
- [0085] FIG. 55A-D are exemplary drawing illustrations of an alternative 3D IC FPGA process flow;
- [0086] FIG. 56 is an exemplary drawing illustration of an NVM FPGA configuration cell;
- [0087] FIG. 57A-G are exemplary drawing illustrations of a 3D IC NVM FPGA configuration cell process flow;
- [0088] FIG. 58A-F are exemplary drawing illustrations of a process flow for manufacturing junction-less recessed channel array transistors;



**[0089]** FIG. 59 is a block diagram representation of an exemplary mobile computing device (MCD);

**[0090]** FIG. 60 is an exemplary drawing illustration of a monolithic 3DIC structure with CTE adjusted through layer connections;

**[0091]** FIG. 61 is an exemplary drawing illustration of a method to repair defects or anneal a transferred layer utilizing a carrier wafer or substrate;

**[0092]** FIG. 62 is an exemplary procedure for a chip designer to ensure a good thermal profile for a design;

**[0093]** FIG. 63 is an exemplary drawing illustration of sub-threshold circuits that may be stacked above or below a logic chip layer;

**[0094]** FIG. 64 A-D are exemplary drawing illustrations of a prior art process to construct shallow trench isolation regions;

**[0095]** FIG. 65 A-D are exemplary drawing illustrations of a sub-400° C. process to construct shallow trench isolation regions; and

**[0096]** FIG. 66 A-D are exemplary drawing illustrations of layers of connections below a layer of transistors and macro-cell formation.

#### DESCRIPTION

**[0097]** Some embodiments of the invention are described herein with reference to the drawing figures. Persons of ordinary skill in the art will appreciate that the description and figures illustrate rather than limit the invention and that in general the figures are not drawn to scale for clarity of presentation. Such skilled persons will also realize that many more embodiments are possible by applying the inventive principles contained herein and that such embodiments fall within the scope of the invention which is not to be limited except by the appended claims.

**[0098]** Many figures may describe process flows for building devices. These process flows, which may be a sequence of steps for building a device, may have many structures, numerals and labels that may be common between two or more adjacent steps. In such cases, some labels, numerals and structures used for a certain step's figure may have been described in the previous steps' figures.

**[0099]** As illustrated in FIG. 1, a generalized single layer transfer procedure that utilizes the above techniques may begin with acceptor substrate 100, which may be a preprocessed CMOS silicon wafer, or a partially processed CMOS, or other prepared silicon or semiconductor substrate. CMOS may include n-type transistors and p-type transistors. Acceptor substrate 100 may include elements such as, for example, transistors, alignment marks, metal layers, and metal connection strips. The metal layers may be utilized to interconnect the transistors. The acceptor substrate may also be called target wafer. The acceptor substrate 100 may be prepared for oxide to oxide wafer bonding by a deposition of an oxide 102, and the acceptor substrate surface 104 may be made ready for low temperature bonding by various surface treatments, such as, for example, an RCA pre-clean that may include dilute ammonium hydroxide or hydrochloric acid, and may include plasma surface preparations, wherein gases such as oxygen, argon, and other gases or combinations of gases and plasma energies that changes the oxide surfaces so to lower the oxide to oxide bonding energy. In addition, polishes may be employed to achieve satisfactory flatness.

**[0100]** A donor wafer or substrate 110 may be prepared for cleaving by an implant or implants of atomic species, such as,

for example, Hydrogen and Helium, to form a layer transfer demarcation plane 199, shown as a dashed line. Layer transfer demarcation plane 199 may be formed before or after other processing on the donor wafer or substrate 110. The donor wafer or substrate 110 may be prepared for oxide to oxide wafer bonding by a deposition of an oxide 112, and the donor wafer surface 114 may be made ready for low temperature bonding by various surface treatments, such as, for example, an RCA pre-clean that may include dilute ammonium hydroxide or hydrochloric acid, and may include plasma surface preparations, wherein gases such as oxygen, argon, and other gases or combinations of gases and plasma energies that change the oxide surfaces so to lower the oxide to oxide bonding energy. In addition, polishes may be employed to achieve satisfactory flatness. The donor wafer or substrate 110 may have prefabricated layers, structures, alignment marks, transistors or circuits.

**[0101]** Donor wafer or substrate 110 may be bonded to acceptor substrate 100, or target wafer, by bringing the donor wafer surface 114 in physical contact with acceptor substrate surface 104, and then applying mechanical force and/or thermal annealing to strengthen the oxide to oxide bond. Alignment of the donor wafer or substrate 110 with the acceptor substrate 100 may be performed immediately prior to the wafer bonding. Acceptable bond strengths may be obtained with bonding thermal cycles that do not exceed approximately 400° C.

**[0102]** The donor wafer or substrate 110 may be cleaved at or near the layer transfer demarcation plane 199 and removed leaving transferred layer 120 bonded and attached to acceptor substrate 100, or target wafer. The cleaving may be accomplished by various applications of energy to the layer transfer demarcation plane, such as, for example, a mechanical strike by a knife, or jet of liquid or jet of air, or by local laser heating, or other suitable cleaving methods that propagate a fracture or separation approximately at the layer transfer demarcation plane 199. The transferred layer 120 may be polished chemically and mechanically to provide a suitable surface for further processing. The transferred layer 120 may be of thickness approximately 200 nm or less to enable formation of nanometer sized thru layer vias and create a high density of interconnects between the donor wafer and acceptor wafer. The thinner the transferred layer 120, the smaller the thru layer via diameter obtainable, as a result of maintaining manufacturable via aspect ratios. Thus, the transferred layer 120 may be, for example, less than about 2 microns thick, less than about 1 micron thick, less than about 0.4 microns thick, less than about 200 nm thick, less than about 150 nm thick, or less than about 100 nm thick. The thickness of the layer or layers transferred according to some embodiments of the invention may be designed as such to match and enable the most suitable lithographic resolution capability of the manufacturing process employed to create the thru layer vias or any other structures on the transferred layer or layers. The donor wafer or substrate 110 may now also be processed and reused for more layer transfers.

**[0103]** Transferred layer 120 may then be further processed to create a monolithic layer of interconnected devices 120' and the formation of thru layer vias (TLVs, or through-layer vias) to electrically couple (connection path) donor wafer circuitry with acceptor wafer circuitry. Alignment marks in acceptor substrate 100 and/or in transferred layer 120 may be utilized to contact transistors and circuitry in transferred layer 120 and electrically couple them to transistors and circuitry in

the acceptor substrate **100**. The use of an implanted atomic species, such as, for example, Hydrogen or Helium or a combination, to create a cleaving plane, such as, for example, layer transfer demarcation plane **199**, and the subsequent cleaving at or near the cleaving plane as described above may be referred to in this document as “ion-cut”, and may be the typically illustrated layer transfer method. As the TLVs are formed through the transferred layer **120**, the thickness of the TLVs may be, for example, less than about 2 microns thick, less than about 1 micron thick, less than about 0.4 microns thick, less than about 200 nm thick, less than about 150 nm thick, or less than about 100 nm thick. TLVs may be constructed mostly out of electrically conductive materials including, for example, copper, aluminum, conductive carbon, or tungsten. Barrier metals, including, for example, TiN and TaN, may be utilized to form TLVs.

[0104] Persons of ordinary skill in the art will appreciate that the illustrations in FIG. 1 are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, a heavily doped (greater than  $1e20$  atoms/cm<sup>3</sup>) boron layer or a silicon germanium (SiGe) layer may be utilized as an etch stop layer either within the ion-cut process flow, wherein the layer transfer demarcation plane may be placed within the etch stop layer or into the substrate material below, or the etch stop layers may be utilized without an implant cleave or ion-cut process and the donor wafer may be preferentially etched away until the etch stop layer may be reached. Such skilled persons will further appreciate that the oxide layer within an SOI or GeOI donor wafer may serve as the etch stop layer. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0105] Alternatively, other technologies and techniques may be utilized for layer transfer as described in, for example, IBM's layer transfer method shown at IEDM 2005 by A. W. Topol, et. al. The IBM's layer transfer method employs a SOI technology and utilizes glass handle wafers. The donor circuit may be high-temperature processed on an SOI wafer, temporarily bonded to a borosilicate glass handle wafer, backside thinned by chemical mechanical polishing of the silicon and then the Buried Oxide (BOX) may be selectively etched off. The now thinned donor wafer may be subsequently aligned and low-temperature oxide-to-oxide bonded to the acceptor wafer topside. A low temperature release of the glass handle wafer from the thinned donor wafer may be next performed, and then thru layer via (or layer to layer) connections may be made.

[0106] Additionally, the inventors contemplate that other technology can be used. For example, an epitaxial liftoff (ELO) technology as shown by P. Demeester, et. al, of IMEC in Semiconductor Science Technology 1993 may be utilized for layer transfer. ELO makes use of the selective removal of a very thin sacrificial layer between the substrate and the layer structure to be transferred. The to-be-transferred layer of GaAs or silicon may be adhesively ‘rolled’ up on a cylinder or removed from the substrate by utilizing a flexible carrier, such as, for example, black wax, to bow up the to-be-transferred layer structure when the selective etch, such as, for example, diluted Hydrofluoric (HF) Acid, etches the exposed release layer, such as, for example, the silicon oxide in SOI or a layer of AlAs. After liftoff, the transferred layer may be then aligned and bonded to the desired acceptor substrate or wafer.

The manufacturability of the ELO process for multilayer layer transfer use was recently improved by J. Yoon, et. al., of the University of Illinois at Urbana-Champaign as described in Nature May 20, 2010.

[0107] Canon developed a layer transfer technology called ELTRAN—Epitaxial Layer TRANSfer from porous silicon. ELTRAN may be utilized as a layer transfer method. The Electrochemical Society Meeting abstract No. 438 from year 2000 and the JSAP International July 2001 paper show a seed wafer being anodized in an HF/ethanol solution to create pores in the top layer of silicon, the pores may be treated with a low temperature oxidation and then high temperature hydrogen annealed to seal the pores. Epitaxial silicon may then be deposited on top of the porous silicon and then oxidized to form the SOI BOX. The seed wafer may be bonded to a handle wafer and the seed wafer may be split off by high pressure water directed at the porous silicon layer. The porous silicon may then be selectively etched off leaving a uniform silicon layer.

[0108] FIG. 2A is a drawing illustration of a generalized preprocessed wafer or layer **200**. The wafer or layer **200** may have preprocessed circuitry, such as, for example, logic circuitry, microprocessors, circuitry including transistors of various types, and other types of digital or analog circuitry including, but not limited to, the various embodiments described herein. Preprocessed wafer or layer **200** may have preprocessed metal interconnects, such as, for example, of copper or aluminum. The preprocessed metal interconnects, such as, for example, metal strips pads, or lines, may be designed and prepared for layer transfer and electrical coupling from preprocessed wafer or layer **200** to the layer or layers to be transferred.

[0109] FIG. 2B is a drawing illustration of a generalized transfer layer **202** prior to being attached to preprocessed wafer or layer **200**. Preprocessed wafer or layer **200** may be called a target wafer or acceptor substrate. Transfer layer **202** may be attached to a carrier wafer or substrate during layer transfer. Transfer layer **202** may have metal interconnects, such as, for example, metal strips, pads, or lines, designed and prepared for layer transfer and electrical coupling to preprocessed wafer or layer **200**. Transfer layer **202**, which may also be called the second semiconductor layer, may include mono-crystalline silicon, or doped mono-crystalline silicon layer or layers, or other semiconductor, metal (including such as aluminum or copper interconnect layers), and insulator materials, layers; or multiple regions of single crystal silicon, or mono-crystalline silicon, or doped mono-crystalline silicon, or other semiconductor, metal, or insulator materials. A preprocessed wafer that can withstand subsequent processing of transistors on top at high temperatures may be called the “Foundation” or a foundation wafer, layer or circuitry. The terms ‘mono-crystalline silicon’ and ‘single crystal silicon’ may be used interchangeably.

[0110] FIG. 2C is a drawing illustration of a preprocessed wafer or layer **200A** created by the layer transfer of transfer layer **202** on top of preprocessed wafer or layer **200**. The top of preprocessed wafer or layer **200A** may be further processed with metal interconnects, such as, for example, metal strips, pads, or lines, designed and prepared for layer transfer and electrical coupling from preprocessed wafer or layer **200A** to the next layer or layers to be transferred.

[0111] FIG. 2D is a drawing illustration of a generalized transfer layer **202A** prior to being attached to preprocessed wafer or layer **200A**. Transfer layer **202A** may be attached to

a carrier wafer or substrate during layer transfer. Transfer layer 202A may have metal interconnects, such as, for example, metal strips, pads, or lines, designed and prepared for layer transfer and electrical coupling to preprocessed wafer or layer 200A. Transfer layer 202A may include mono-crystalline silicon, or doped mono-crystalline silicon layer or layers, or other semiconductor, metal, and insulator materials, layers; or multiple regions of single crystal silicon, or mono-crystalline silicon, or dope mono-crystalline silicon, or other semiconductor, metal, or insulator materials.

[0112] FIG. 2E is a drawing illustration of a preprocessed wafer or layer 200B created by the layer transfer of transfer layer 202A on top of preprocessed wafer or layer 200A. Transfer layer 202A may also be called the third semiconductor layer. The top of preprocessed wafer or layer 200B may be further processed with metal interconnects, such as, for example, metal strips, pads, or lines, designed and prepared for layer transfer and electrical coupling from preprocessed wafer or layer 200B to the next layer or layers to be transferred.

[0113] FIG. 2F is a drawing illustration of a generalized transfer layer 202B prior to being attached to preprocessed wafer or layer 200B. Transfer layer 202B may be attached to a carrier wafer or substrate during layer transfer. Transfer layer 202B may have metal interconnects, such as, for example, metal strips, pads, or lines, designed and prepared for layer transfer and electrical coupling to preprocessed wafer or layer 200B. Transfer layer 202B may include mono-crystalline silicon, or doped mono-crystalline silicon layer or layers, or other semiconductor, metal, and insulator materials, layers; or multiple regions of single crystal silicon, or mono-crystalline silicon, or dope mono-crystalline silicon, or other semiconductor, metal, or insulator materials.

[0114] FIG. 2G is a drawing illustration of preprocessed wafer or layer 200C created by the layer transfer of transfer layer 202B on top of preprocessed wafer or layer 200B. The top of preprocessed wafer or layer 200C may be further processed with metal interconnect, such as, for example, metal strips, pads, or lines, designed and prepared for layer transfer and electrical coupling from preprocessed wafer or layer 200C to the next layer or layers to be transferred.

[0115] FIG. 2H is a drawing illustration of preprocessed wafer or layer 200C, a 3D IC stack, which may include transferred layers 202A and 202B on top of the original preprocessed wafer or layer 200. Transferred layers 202A and 202B and the original preprocessed wafer or layer 200 may include transistors of one or more types in one or more layers, metallization such as, for example, copper or aluminum in one or more layers, interconnections to and among layers above and below (connection paths, such as TLVs or TSVs), and interconnections within the layer. The transistors may be of various types that may be different from layer to layer or within the same layer. The transistors may be in various organized patterns. The transistors may be in various pattern repeats or bands. The transistors may be in multiple layers involved in the transfer layer. The transistors may be, for example, junction-less transistors or recessed channel transistors or other types of transistors described in this document. Transferred layers 202A and 202B and the original preprocessed wafer or layer 200 may further include semiconductor devices such as, for example, resistors and capacitors and inductors, one or more programmable interconnects, memory structures and devices, sensors, radio frequency devices, or optical interconnect with associated transceivers.

The terms carrier wafer or carrier substrate may also be called holder wafer or holder substrate.

[0116] This layer transfer process can be repeated many times, thereby creating preprocessed wafers that may include many different transferred layers which, when combined, can then become preprocessed wafers or layers for future transfers. This layer transfer process may be sufficiently flexible that preprocessed wafers and transfer layers, if properly prepared, can be flipped over and processed on either side with further transfers in either direction as a matter of design choice.

[0117] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 2A through 2H are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the preprocessed wafer or layer 200 may act as a base or substrate layer in a wafer transfer flow, or as a preprocessed or partially preprocessed circuitry acceptor wafer in a wafer transfer process flow. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0118] One industry method to form a low temperature gate stack may be called a high-k metal gate (HKMG) and may be referred to in later discussions. The high-k metal gate structure may be formed as follows. Following an industry standard HF/SC1/SC2 cleaning to create an atomically smooth surface, a high-k dielectric may be deposited. The semiconductor industry has chosen Hafnium-based dielectrics as the leading material of choice to replace SiO<sub>2</sub> and Silicon oxynitride. The Hafnium-based family of dielectrics includes hafnium oxide and hafnium silicate/hafnium silicon oxynitride. Hafnium oxide, HfO<sub>2</sub>, may have a dielectric constant twice as much as that of hafnium silicate/hafnium silicon oxynitride (HfSiO/HfSiON k~15). The choice of the metal may be critical for the device to perform properly. A metal replacing N<sup>+</sup> poly as the gate electrode may need to have a work function of approximately 4.2 eV for the device to operate properly and at the right threshold voltage. Alternatively, a metal replacing P<sup>+</sup> poly as the gate electrode may need to have a work function of approximately 5.2 eV to operate properly. The TiAl and TiAlN based family of metals, for example, could be used to tune the work function of the metal from 4.2 eV to 5.2 eV.

[0119] Alternatively, a low temperature gate stack may be formed with a gate oxide formed by a microwave oxidation technique, such as, for example, the TEL SPA (Tokyo Electron Limited Slot Plane Antenna) oxygen radical plasma, that grows or deposits a low temperature Gate Dielectric to serve as the MOSFET gate oxide, or an atomic layer deposition (ALD) deposition technique may be utilized. A metal gate of proper work function, such as, for example, aluminum or tungsten, or low temperature doped amorphous silicon gate electrode, may then be deposited.

[0120] Transistors constructed in this document can be considered "planar transistors" when the current flow in the transistor channel may be substantially in the horizontal direction. The horizontal direction may be defined as the direction being parallel to the largest area of surface of the substrate or wafer that the transistor may be built or layer transferred onto. These transistors can also be referred to as horizontal transistors, horizontally oriented transistors, or lateral transistors. In some embodiments of the invention the

horizontal transistor may be constructed in a two-dimensional plane where the source and the drain are in the same two dimensional horizontal plane.

[0121] The following sections discuss some embodiments of the invention wherein wafer sized doped layers may be transferred and then may be processed to create 3D ICs.

[0122] An embodiment of the invention is to pre-process a donor wafer by forming wafer sized layers of various materials without a process temperature restriction, then layer transferring the pre-processed donor wafer to the acceptor wafer, and processing at either low temperature (below approximately 400° C.) or high temperature (greater than approximately 400° C.) after the layer transfer to form device structures, such as, for example, transistors and metal interconnect, on or in the donor wafer that may be physically aligned and may be electrically coupled or connected to the acceptor wafer. A wafer sized layer denotes a continuous layer of material or combination of materials that may extend across the wafer to substantially the full extent of the wafer edges and may be approximately uniform in thickness. If the wafer sized layer compromises dopants, then the dopant concentration may be substantially the same in the x and y direction across the wafer, but can vary in the z direction perpendicular to the wafer surface.

[0123] As illustrated in FIG. 3A, a generalized process flow may begin with a donor wafer 300 that may be preprocessed with wafer sized layers 302 of conducting, semi-conducting or insulating materials that may be formed by deposition, ion implantation and anneal, oxidation, epitaxial growth, combinations of above, or other semiconductor processing steps and methods. The donor wafer 300 may be preprocessed with a layer transfer demarcation plane (shown as dashed line) 399, such as, for example, a hydrogen implant cleave plane, before or after layers 302 are formed. Acceptor wafer 310 may be a preprocessed wafer that may have fully functional circuitry including metal layers (including aluminum or copper metal interconnect layers that may connect acceptor wafer 310 transistors) or may be a wafer with previously transferred layers, or may be a blank carrier or holder wafer, or other kinds of substrates suitable for layer transfer processing. Acceptor wafer 310 may have alignment marks 390 and metal connect pads or strips 380. Acceptor wafer 310 and the donor wafer 300 may be a bulk mono-crystalline silicon wafer or a Silicon On Insulator (SOI) wafer or a Germanium on Insulator (GeOI) wafer.

[0124] Both bonding surfaces 301 and 311 may be prepared for wafer bonding by depositions, polishes, plasma, or wet chemistry treatments to facilitate successful wafer to wafer bonding.

[0125] As illustrated in FIG. 3B, the donor wafer 300 with layers 302 and layer transfer demarcation plane 399 may then be flipped over, aligned, and bonded to the acceptor wafer 310. The donor wafer 300 with layers 302 may have alignment marks (not shown).

[0126] As illustrated in FIG. 3C, the donor wafer 300 may be cleaved at or thinned to the layer transfer demarcation plane 399, leaving a portion of the donor wafer 300' and the pre-processed layers 302 bonded to the acceptor wafer 310, by methods such as, for example, ion-cut or other layer transfer methods.

[0127] As illustrated in FIG. 3D, the remaining donor wafer portion 300' may be removed by polishing or etching and the transferred layers 302 may be further processed to create donor wafer device structures 350 that may be precisely

aligned to the acceptor wafer alignment marks 390. Donor wafer device structures 350 may include, for example, CMOS transistors such as N type and P type transistors, or any of the other transistor or device types discussed herein this document. These donor wafer device structures 350 may utilize thru layer vias (TLVs) 360 to electrically couple (connection paths) the donor wafer device structures 350 to the acceptor wafer metal connect pads or strips 380. TLVs 360 may be formed through the transferred layers 302. As the transferred layers 302 may be thin, on the order of about 200 nm or less in thickness, the TLVs may be easily manufactured as a typical metal to metal via may be, and said TLV may have state of the art diameters such as nanometers or tens to a few hundreds of nanometers, such as, for example about 150 nm or about 100 nm or about 50 nm. The thinner the transferred layers 302, the smaller the thru layer via diameter obtainable, which may result from maintaining manufacturable via aspect ratios. Thus, the transferred layers 302 (and hence, TLVs 360) may be, for example, less than about 2 microns thick, less than about 1 micron thick, less than about 0.4 microns thick, less than about 200 nm thick, less than about 150 nm thick, or less than about 100 nm thick. The thickness of the layer or layers transferred according to some embodiments of the invention may be designed as such to match and enable the most suitable obtainable lithographic resolution, such as, for example, less than about 10 nm, 14 nm, 22 nm or 28 nm linewidth resolution and alignment capability, such as, for example, less than about 5 nm, 10 nm, 20 nm, or 40 nm alignment accuracy/precision/error, of the manufacturing process employed to create the thru layer vias or any other structures on the transferred layer or layers. Transferred layers 302 may be considered to be overlying the metal layer or layers of acceptor wafer 310. Alignment marks in acceptor substrate 310 and/or in transferred layers 302 may be utilized to enable reliable contact to transistors and circuitry in transferred layers 302 and donor wafer device structures 350 and electrically couple them to the transistors and circuitry in the acceptor substrate 310. The donor wafer 300 may now also be processed and reused for more layer transfers.

[0128] There may be multiple methods by which a transistor or other devices may be formed to enable a 3D IC.

[0129] A planar V-groove NMOS transistor may be formed as follows. As illustrated in FIG. 4A, a P- substrate donor wafer 400 may be processed to include wafer sized layers of N+ doping 402, P- doping 404, and P+ doping 406. The N+ doping layer 402 and P+ doping layer 406 may be formed by ion implantation and thermal anneal. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ 402, P- 404, and P+ 406 or by a combination of epitaxy and implantation. The shallow P+ doped layer 406 may be doped by Plasma Assisted Doping (PLAD) techniques. In addition, P- layer 404 may have additional ion implantation and anneal processing to provide a different dopant level than P- substrate 400. P- layer 404 may have a graded or various layers of P- doping to mitigate transistor performance issues, such as, for example, short channel effects, after the NMOS transistor is formed.

[0130] As illustrated in FIG. 4B, the top surface of P- substrate donor wafer 400 may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of P+ layer 406 to form oxide layer 408. A layer transfer demarcation plane (shown as dashed line) 499 may be formed by hydrogen implantation or other methods as previously described. Both the P- substrate donor wafer 400 and accep-

tor wafer **410** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer **402** and the P- substrate donor wafer **400** that may be above the layer transfer demarcation plane **499** may be removed by cleaving or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0131] As illustrated in FIG. 4C, the P+ layer **406**, P- layer **404**, and remaining N+ layer **402'** have been layer transferred to acceptor wafer **410**. The top surface **403** of N+ layer **402'** may be chemically or mechanically polished. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer **410** alignment marks (not shown). For illustration clarity, the oxide layers used to facilitate the wafer to wafer bond are not shown.

[0132] As illustrated in FIG. 4D, the substrate P+ body tie **412** contact opening and transistor isolation **414** may be soft or hard mask defined and then etched. Thus N+ **403** and P- **405** doped regions may be formed.

[0133] As illustrated in FIG. 4E, the transistor isolation **414** may be formed by mask defining and then etching P+ layer **406** to the top of acceptor wafer **410**, forming P+ regions **407**. Then a low-temperature gap fill oxide **420** may be deposited and chemically mechanically polished. A thin polish stop layer **422** such as, for example, low temperature silicon nitride, may then be deposited.

[0134] As illustrated in FIG. 4F, source **432**, drain **434** and self-aligned gate **436** may be defined by masking and etching the thin polish stop layer **422** and then followed by a sloped N+ etch of N+ region **403** and may continue into P- region **405**. The sloped (30-90 degrees, 45 is shown) etch or etches may be accomplished with wet chemistry or plasma or Reactive Ion Etching (RIE) techniques. This process forms angular source and drain extensions **438**.

[0135] As illustrated in FIG. 4G, a gate oxide **442** may be formed and a gate electrode material **444** may be deposited. The gate oxide **442** may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate electrode material **444** in the industry standard high k metal gate process schemes described previously. Or the gate oxide **442** may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode material **444** with proper work function and less than approximately 400° C. deposition temperature such as, for example, tungsten or aluminum may be deposited.

[0136] As illustrated in FIG. 4H, the gate electrode material **444** and gate oxide **442** may be chemically mechanically polished with the polish stop in the polish stop layer **422**. The gate electrode material **444** and gate oxide **442** may be thus remaining in the intended V-groove. Alternatively, the gate could be defined by a photolithography masking and etching process with minimum overlaps outside the V-groove.

[0137] As illustrated in FIG. 4I, a low temperature thick oxide **450** may be deposited and source contact **452**, gate contact **454**, drain contact **456**, substrate P+ body tie **458**, and thru layer via **460** openings may be masked and etched preparing the transistors to be connected via metallization. The thru layer via **460** provides electrical coupling among the donor wafer transistors and the acceptor wafer metal connect pads or strips **480**.

[0138] A planar V-groove PMOS transistor may be constructed via the above process flow by changing the initial P-

substrate donor wafer **400** or epi-formed P- on N+ layer **402** to an N-wafer or an N- on P+ epi layer; and the N+ layer **402** to a P+ layer. Similarly, layer **406** would change from P+ to N+ if the substrate body tie was utilized. Proper work function gate electrode materials **444** would be employed.

[0139] Additionally, a planar accumulation mode V-groove MOSFET transistor may be constructed via the above process flow by changing the initial P- substrate donor wafer **400** or epi-formed P- on N+ layer **402** to an N- wafer or an N- epi layer on N+. Proper work function gate electrode materials **444** would be employed.

[0140] Additionally, a planar double gate V-groove MOSFET transistor may be constructed as illustrated in FIG. 4J. Acceptor wafer metal **481** may be positioned beneath the top gate **444** and electrically coupled through top gate contact **454**, donor wafer metal interconnect, TLV **460** to acceptor wafer metal connect pads or strips **480**, which may be coupled to acceptor wafer metal **481** forming a bottom gate. The acceptor and donor wafer bonding oxides may be constructed of thin layers to allow the bottom gate acceptor wafer metal **481** control over a portion of the transistor channel. Note that the P+ regions **407** and substrate P+ body tie **458** of FIG. 4I, the body tie example, may not be a part of the double-gate construction illustrated in FIG. 4J.

[0141] Recessed Channel Array Transistors (RCATs) may be another transistor family which may utilize layer transfer and the definition-by-etch process to construct a low-temperature monolithic 3D IC. Two types of RCAT (RCAT and SRCAT) device structures are shown in FIG. 5. These were described by J. Kim, et al. at the Symposium on VLSI Technology, in 2003 and 2005. Kim, et al. teaches construction of a single layer of transistors and did not utilize any layer transfer techniques. Their work also used high-temperature anneals, wherein the temperatures were above about 400° C.

[0142] A planar n-channel Recessed Channel Array Transistor (RCAT) suitable for a 3D IC may be constructed as follows. As illustrated in FIG. 6A, a P- substrate donor wafer **600** may be processed to include wafer sized layers of N+ doping **602**, and P- doping **603** across the wafer. The N+ doping layer **602** may be formed by ion implantation and thermal anneal. In addition, P-layer **603** may have additional ion implantation and anneal processing to provide a different dopant level than P- substrate **600**. P-layer **603** may have graded or various layers of P- doping to mitigate transistor performance issues, such as, for example, short channel effects, after the RCAT is formed. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ **602** and P- **603**, or by a combination of epitaxy and implantation.

[0143] As illustrated in FIG. 6B, the top surface of P- substrate donor wafer **600** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of P- layer **603** to form oxide layer **680**. A layer transfer demarcation plane (shown as dashed line) **699** may be formed by hydrogen implantation or other methods as previously described. Both the P- substrate donor wafer **600** and acceptor wafer **610** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer **602** and the P- substrate donor wafer **600** that may be above the layer transfer demarcation plane **699** may be removed by cleaving or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0144] As illustrated in FIG. 6C, P- layer 603, and remaining N+ layer 602' have been layer transferred to acceptor wafer 610. The top surface of N+ layer 602' may be chemically or mechanically polished. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer 610 alignment marks (not shown). For illustration clarity, the oxide layers used to facilitate the wafer to wafer bond are not shown.

[0145] As illustrated in FIG. 6D, the transistor isolation regions 605 may be formed by mask defining and then etching N+ layer 602' and P- layer 603 to the top of acceptor wafer 610. Then a low-temperature gap fill oxide may be deposited and chemically mechanically polished, the oxide remaining in isolation regions 605. Then the recessed channel 606 may be mask defined and etched. The recessed channel surfaces and edges may be smoothed by wet chemical or plasma/RIE etching techniques to mitigate high field effects. The etch formation of recessed channel 606 may define the transistor channel length. These process steps form N+ source and drain regions 622 and P- channel region 623, which may form the transistor body. The doping concentration of the P- channel region 623 may include gradients of concentration or layers of differing doping concentrations.

[0146] As illustrated in FIG. 6E, a gate dielectric 607 may be formed and a gate electrode 608 may be deposited. The gate dielectric 607 may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate electrode 608 in the industry standard high k metal gate process schemes described previously. Or the gate dielectric 607 may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode 608 with proper work function and less than approximately 400° C. deposition temperature such as, for example, tungsten or aluminum may be deposited. Then the gate electrode 608 may be chemically mechanically polished, and the gate area defined by masking and etching.

[0147] As illustrated in FIG. 6F, a low temperature thick oxide 609 may be deposited and source, gate, and drain contacts 615, and thru layer via 660 openings may be masked and etched preparing the transistors to be connected via metallization. The thru layer via 660 provides electrical coupling among the donor wafer transistors and the acceptor wafer metal interconnect pads 683.

[0148] A planar PMOS RCAT transistor may be constructed via the above process flow by changing the initial P- substrate donor wafer 600 or epi-formed P- layer 603 to an N- wafer or an N- on P+ epi layer; and the N+ layer 602 to a P+ layer. Proper work function gate electrode 608 would be employed.

[0149] Additionally, a planar accumulation mode RCAT transistor may be constructed via the above process flow by changing the initial P- substrate donor wafer 600 or epi-formed P- layer 603 to an N- wafer or an N- epi layer on N+. Proper work function gate electrode 608 would be employed.

[0150] Additionally, a planar partial double gate RCAT transistor may be constructed as illustrated in FIG. 6G. Acceptor wafer metal 681 may be positioned beneath the top gate electrode 608 and electrically coupled through the top gate contact 654, donor wafer metal interconnect, TLV 660 to acceptor wafer metal interconnect pads 683, which may be coupled to acceptor wafer metal 681 forming a bottom gate. The acceptor and donor wafer bonding oxides may be constructed of thin layers to allow bottom gate, via acceptor

wafer metal 681, control over a portion of the transistor channel. Further, efficient heat removal and transistor body biasing may be accomplished on the RCAT by adding an appropriately doped buried layer (N- in the case of an n-RCAT) and then forming a buried layer region underneath the P- channel region 623 for junction isolation and connecting that buried region to a thermal and electrical contact, similar to what is described for layer 1606 and region 1646 in FIGS. 16A-G.

[0151] A planar n-channel Spherical Recessed Channel Array Transistor (S-RCAT) may be constructed as follows. As illustrated in FIG. 7A, a P- substrate donor wafer 700 may be processed to include wafer sized layers of N+ doping 702, and P- doping 703. The N+ doped layer 702 may be formed by ion implantation and thermal anneal. In addition, P- layer 703 may have additional ion implantation and anneal processing to provide a different dopant level than P- substrate donor wafer 700. P-layer 703 may have graded or various layers of P- doping to mitigate transistor performance issues, such as, for example, short channel effects, after the S-RCAT is formed. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ doped layer 702 and P- layer 703, or by a combination of epitaxy and implantation.

[0152] As illustrated in FIG. 7B, the top surface of P- substrate donor wafer 700 may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of P- layer 703 to form oxide layer 780. A layer transfer demarcation plane (shown as a dashed line) 799 may be formed by hydrogen implantation or other methods as previously described. Both the P- substrate donor wafer 700 and acceptor wafer 710 may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ doped layer 702 and the P- substrate donor wafer 700 that may be above the layer transfer demarcation plane 799 may be removed by cleaving or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0153] As illustrated in FIG. 7C, P- layer 703, and remaining N+ layer 702' have been layer transferred to acceptor wafer 710. The top surface of N+ layer 702' may be chemically or mechanically polished. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer 710 alignment marks (not shown). For illustration clarity, the oxide layers used to facilitate the wafer to wafer bond are not shown.

[0154] As illustrated in FIG. 7D, the transistor isolation areas 705 may be formed by mask defining and then etching N+ layer 702' and P- layer 703 to the top of acceptor wafer 710. Then a low-temperature gap fill oxide may be deposited and chemically mechanically polished, remaining in isolation areas 705. Then the spherical recessed channel 706 may be mask defined and etched. In the first step, the eventual gate electrode recessed channel may be partially etched, and a spacer deposition may be performed with a conformal low temperature deposition of materials such as, for example, silicon oxide or silicon nitride or in combination.

[0155] In the second step, an anisotropic etch of the spacer may be performed to leave the spacer material only on the vertical sidewalls of the recessed gate channel opening. In the third step, an isotropic silicon etch may be conducted to form the spherical recessed channel 706. In the fourth step, the spacer on the sidewall may be removed with a selective etch. The recessed channel surfaces and edges may be smoothed by

wet chemical or plasma/RIE etching techniques to mitigate high field effects. These process steps form N+ source and drain regions **722** and P-channel region **723**, which may form the transistor body. The doping concentration of the P-channel region **723** may include gradients of concentration or layers of differing doping concentrations. The etch formation of spherical recessed channel **706** may define the transistor channel length.

**[0156]** As illustrated in FIG. 7E, a gate oxide **707** may be formed and a gate electrode **708** may be deposited. The gate oxide **707** may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate electrode **708** in the industry standard high k metal gate process schemes described previously. Or the gate oxide **707** may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode **708** with proper work function and less than approximately 400° C. deposition temperature such as, for example, tungsten or aluminum may be deposited. Then the gate electrode **708** may be chemically mechanically polished, and the gate area defined by masking and etching.

**[0157]** As illustrated in FIG. 7F, a low temperature thick oxide **709** may be deposited and source, gate, and drain contacts **715**, and thru layer vias **760** may be masked and etched preparing the transistors to be connected. The thru layer via **760** provides electrical coupling among the donor wafer transistors or signal wiring and the acceptor wafer metal connect pads **783**.

**[0158]** A planar PMOS S-RCAT transistor may be constructed via the above process flow by changing the initial P-substrate donor wafer **700** or epi-formed P-layer **703** to an N- wafer or an N- on P+ epi layer; and the N+ layer **702** to a P+ layer. Proper work function gate electrodes **708** would be employed.

**[0159]** Additionally, a planar accumulation mode S-RCAT transistor may be constructed via the above process flow by changing the initial P- substrate donor wafer **700** or epi-formed P-layer **703** to an N- wafer or an N- epi layer on N+. Proper work function gate electrodes **708** would be employed.

**[0160]** Additionally, a planar partial double gate S-RCAT transistor may be constructed as illustrated in FIG. 7G. Acceptor wafer metal **781** may be positioned beneath the top gate, gate electrode **708**, and electrically coupled through the top gate contact **754**, donor wafer metal interconnect, thru layer via **760** to acceptor wafer metal interconnect pads **783**, which may be coupled to acceptor wafer metal **781** forming a bottom gate. The acceptor and donor wafer bonding oxides may be constructed of thin layers to allow bottom gate control over a portion of the transistor channel. Further, efficient heat removal and transistor body biasing may be accomplished on the S-RCAT by adding an appropriately doped buried layer (N- in the case of an NMOS S-RCAT) and then forming a buried layer region underneath the P- channel region **723** for junction isolation and connecting that buried region to a thermal and electrical contact, similar to what is described for layer **1606** and region **1646** in FIGS. 16A-G.

**[0161]** SRAM, DRAM or other memory circuits may be constructed with RCAT or S-RCAT devices and may have different trench depths compared to logic circuits. The RCAT and S-RCAT devices may be utilized to form BiCMOS inverters and other mixed circuitry when the acceptor wafer

includes conventional Bipolar Junction Transistors and the transferred layer or layers may be utilized to form the RCAT devices.

**[0162]** Junction-less Transistors (JLTs) are another transistor family that may utilize layer transfer and etch definition to construct a low-temperature monolithic 3D IC. The junction-less transistor structure avoids the increasingly sharply graded junctions necessary for sufficient separation between source and drain regions as silicon technology scales. This allows the JLT to have a thicker gate oxide than a conventional MOSFET for an equivalent performance. The junction-less transistor may also be known as a nanowire transistor without junctions, or gated resistor, or nanowire transistor as described in a paper by Jean-Pierre Colinge, et. al., (Colinge) published in Nature Nanotechnology on Feb. 21, 2010.

**[0163]** As illustrated in FIG. 8 the junction-less transistor may be constructed whereby the transistor channel may be a thin solid piece of evenly and heavily doped single crystal silicon. Single crystal silicon may also be referred to as monocrystalline silicon. The doping concentration of the channel underneath the gate **806** and gate dielectric **808** may be identical to that of the source **804** and drain **802**. As a result of the high channel doping, the channel must be thin and narrow enough to allow for full depletion of the carriers when the device may be turned off. Additionally, the channel doping must be high enough to allow a reasonable current to flow when the device may be on. A multi-sided gate may provide increased control of the channel. The JLT may have a very small channel area (typically less than about 20 nm on one or more sides), so the gate can deplete the channel of charge carriers at approximately 0V and turn the source to drain current substantially off. I-V curves from Colinge of n channel and p channel junction-less transistors are shown in FIG. 8. This illustrates that the JLT can obtain comparable performance to the tri-gate transistor (junction-ed) that may be commonly researched and reported by transistor developers.

**[0164]** As illustrated in FIGS. 9A to 9G, an n-channel 3-sided gated junction-less transistor (JLT) may be constructed that may be suitable for 3D IC manufacturing. As illustrated in FIG. 9A, an N- substrate donor wafer **900** may be processed to include a wafer sized layer of N+ doping **904**. The N+ doping layer **904** may be formed by ion implantation and thermal anneal. The N+ doping layer **904** may have a doping concentration that may be more than 10x the doping concentration of N- substrate donor wafer **900**. A screen oxide **901** may be grown before the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. The N+ layer **904** may alternatively be formed by epitaxial growth of a doped silicon layer of N+ or may be a deposited layer of heavily N+ doped polysilicon that may be optically annealed to form large grains. The N+ doped layer **904** may be formed by doping the N-substrate donor wafer **900** by Plasma Assisted Doping (PLAD) techniques. These processes may be done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done.

**[0165]** As illustrated in FIG. 9B, the top surface of N-substrate donor wafer **900** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the N+ layer **904** to form oxide layer **902**, or a re-oxidation of implant screen oxide **901**. A layer transfer demarcation plane **999** (shown as a dashed line) may be formed in N-substrate donor wafer **900** or N+ layer **904** (shown) by hydro-

gen implantation **907** or other methods as previously described. Both the N- substrate donor wafer **900** and acceptor wafer **910** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer **904** and the N- substrate donor wafer **900** that may be above the layer transfer demarcation plane **999** may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0166] As illustrated in FIG. 9C, the remaining N+ layer **904'** may be layer transferred to acceptor wafer **910**. The top surface **906** of N+ layer **904'** may be chemically or mechanically polished. Now junction-less transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer **910** alignment marks (not shown). The acceptor wafer metal connect pad **980** is illustrated. For illustration clarity, the oxide layers used to facilitate the wafer to wafer bond are not shown.

[0167] As illustrated in FIG. 9D a low temperature thin oxide (not shown) may be grown or deposited, or formed by liquid oxidants such as, for example, 120° C. sulfuric peroxide, to protect the thin transistor N+ silicon layer **904'** top from contamination, and then the N+ layer **904'** may be masked and etched and the photoresist subsequently removed. Thus the transistor channel elements **908** may be formed. The thin protective oxide may be striped in a dilute HF solution.

[0168] As illustrated in FIG. 9E a low temperature based Gate Dielectric may be deposited and densified to serve as the junction-less transistor gate dielectric **911**. Alternatively, a low temperature microwave plasma oxidation of the transistor channel element **908** silicon surfaces may serve as the JLT gate dielectric **911** or an atomic layer deposition (ALD) technique may be utilized to form the HKMG gate oxide as previously described. Then deposition of a low temperature gate electrode material **912** with proper work function and less than approximately 400° C. deposition temperature, such as, for example, P+ doped amorphous silicon, may be performed. Alternatively, a HKMG gate structure may be formed as described previously.

[0169] As illustrated in FIG. 9F the gate electrode material **912** may be masked and etched to define the three sided (top and two side) gate electrode **914** that may be in an overlapping crossing manner, generally orthogonal, with respect to the transistor channel element **908**.

[0170] As illustrated in 3D projection FIG. 9G, the entire structure may be substantially covered with a Low Temperature Oxide **916**, which may be planarized with chemical mechanical polishing. The gate electrode **914**, N+ transistor channel **908**, gate dielectric **911**, and acceptor wafer **910** are shown.

[0171] As illustrated in FIG. 9H, then the contacts and thru layer vias may be formed. The gate contact **920** connects to the gate electrode **914**. The two transistor channel terminal contacts (source and drain) **922** independently connect to the transistor channel element **908** on each side of the gate electrode **914**. The thru layer via **960** electrically couples the transistor layer metallization on the donor wafer to the acceptor wafer metal connect pad **980** in acceptor wafer **910**. This process flow enables the formation of a mono-crystalline silicon channel 3-sided gated junction-less transistor which may be formed and connected to the underlying multi-metal

layer semiconductor device without exposing the underlying devices to a high temperature.

[0172] A p channel 3-sided gated JLT may be constructed as above with the N+ layer **904** formed as P+ doped, and the gate electrode material **912** may be of appropriate work function to shutoff the p channel at a gate voltage of approximately zero. N- substrate donor wafer **900** may be of other doping, for example, a P-, P+, N+ doped substrate.

[0173] As illustrated in FIGS. 10A to 10H, an n-channel 2-sided gated junction-less transistor (JLT) may be constructed that may be suitable for 3D IC manufacturing. As illustrated in FIG. 10A, an N- (shown) or P- substrate donor wafer **1000** may be processed to include a wafer sized layer of N+ doping **1004**. The N+ doping layer **1004** may be formed by ion implantation and thermal anneal. The N+ doping layer **1004** may have a doping concentration that may be more than 10x the doping concentration of N- substrate donor wafer **1000**. A screen oxide **1001** may be grown before the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. The N+ layer **1004** may alternatively be formed by epitaxial growth of a doped silicon layer of N+ or may be a deposited layer of heavily N+ doped amorphous or poly-crystalline silicon that may be optically annealed to form large grains. The N+ doped layer **1004** may be formed by doping the N- substrate donor wafer **1000** by Plasma Assisted Doping (PLAD) techniques. These processes may be done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done.

[0174] As illustrated in FIG. 10B, the top surface of N- donor substrate wafer **1000** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the N+ layer **1004** to form oxide layer **1002**, or a re-oxidation of implant screen oxide **1001** to form oxide layer **1002**. A layer transfer demarcation plane **1099** (shown as a dashed line) may be formed in N- donor substrate wafer **1000** or N+ layer **1004** (shown) by hydrogen implantation **1007** or other methods as previously described. Both the N- donor substrate wafer **1000** and acceptor substrate **1010** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer **1004** and the N- donor wafer substrate **1000** that may be above the layer transfer demarcation plane **1099** may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods. For example, if the layer transfer demarcation plane **1099** is placed below the N+ layer **1004** and into the N- donor substrate **1000**, the remaining N- or P- layer may be removed by etch or mechanical polishing after the cleaving process. This could be done selectively to the N+ layer **1004**.

[0175] As illustrated in FIG. 10C, the remaining N+ layer **1004'** may have been layer transferred to acceptor substrate **1010**. The top surface of N+ layer **1004'** may be chemically or mechanically polished or etched to the desired thickness. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor substrate **1010** alignment marks (not shown). A low temperature CMP and plasma/RIE etch stop layer **1005**, such as, for example, low temperature silicon nitride (SiN) on silicon oxide, may be deposited on top of N+ layer **1004'**. The acceptor wafer metal connect pad **1080** is illustrated. For illustration clarity, the oxide layers used to facilitate the wafer to wafer bond are not shown.



[0176] As illustrated in FIG. 10D the CMP & plasma/RIE etch stop layer 1005 and N+ layer 1004' may be masked and etched, and the photoresist subsequently removed. The transistor channel elements 1008 with associated CMP & plasma/RIE etch stop layer 1005' may be formed.

[0177] As illustrated in FIG. 10E a low temperature based Gate Dielectric may be deposited and densified to serve as the junction-less transistor gate dielectric 1011. Alternatively, a low temperature microwave plasma oxidation of the transistor channel element 1008 silicon surfaces may serve as the JLT gate dielectric 1011 or an atomic layer deposition (ALD) technique may be utilized to form the HKMG gate oxide as previously described. Then deposition of a low temperature gate material 1012 with proper work function and less than approximately 400° C. deposition temperature, such as, for example, P+ doped amorphous silicon, may be performed. Alternatively, a HKMG gate structure may be formed as described previously.

[0178] As illustrated in FIG. 10F the gate material 1012 may be masked and etched to define the three sided gate electrodes 1014 that may be in an overlapping crossing manner, generally orthogonal, with respect to the transistor channel element 1008.

[0179] As illustrated in 3D projection FIG. 10G, the entire structure may be substantially covered with a Low Temperature Oxide 1016, which may be planarized with chemical mechanical polishing. The three sided gate electrode 1014, N+ transistor channel element 1008, gate dielectric 1011, and acceptor substrate 1010 are shown.

[0180] As illustrated in FIG. 10H, then the contacts and metal interconnects may be formed. The gate contact 1020 connects to the three sided gate electrodes 1014. The two transistor channel terminal contacts (source and drain) 1022 independently connect to the transistor channel element 1008 on each side of the three sided gate electrodes 1014. The thru layer via 1060 electrically couples the transistor layer metalization to the acceptor substrate 1010 at acceptor wafer metal connect pad 1080. This flow enables the formation of a monocrystalline silicon channel 2-sided gated junction-less transistor which may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

[0181] A p channel 2-sided gated JLT may be constructed as above with the N+ layer 1004 formed as P+ doped, and the gate material 1012 may be of appropriate work function to shutoff the p channel at a gate voltage of zero.

[0182] FIG. 10 is drawn to illustrate a thin-side-up junction-less transistor (JLT). A thin-side-up JLT may have the thinnest dimension of the channel cross-section facing up (oriented horizontally), with that face being parallel to the silicon base substrate surface. Previously and subsequently described junction-less transistors may have the thinnest dimension of the channel cross section oriented vertically and perpendicular to the silicon base substrate surface, or may be constructed in the thin-side-up manner.

[0183] As illustrated in FIGS. 11A to 11H, an n-channel 1-sided gated junction-less transistor (JLT) may be constructed that may be suitable for 3D IC manufacturing. As illustrated in FIG. 11A, an N- substrate donor wafer 1100 may be processed to include a wafer sized layer of N+ doping 1104. The N+ doping layer 1104 may be formed by ion implantation and thermal anneal. The N+ doping layer 1104 may have a doping concentration that may be more than 10x the doping concentration of N- substrate donor wafer 1100. A

screen oxide 1101 may be grown before the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. The N+ layer 1104 may alternatively be formed by epitaxial growth of a doped silicon layer of N+ or may be a deposited layer of heavily N+ doped amorphous or poly-crystalline silicon that may be optically annealed to form large grains. The N+ doped layer 1104 may be formed by doping the N- substrate donor wafer 1100 by Plasma Assisted Doping (PLAD) techniques. These processes may be done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done.

[0184] As illustrated in FIG. 11B, the top surface of N- substrate donor wafer 1100 may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the N+ layer 1104 to form oxide layer 1102, or a re-oxidation of implant screen oxide 1101 to form oxide layer 1102. A layer transfer demarcation plane 1199 (shown as a dashed line) may be formed in N- substrate donor wafer 1100 or N+ layer 1104 (shown) by hydrogen implantation 1107 or other methods as previously described. Both the N- substrate donor wafer 1100 and acceptor substrate 1110 may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer 1104 and the N- donor wafer substrate 1100 that may be above the layer transfer demarcation plane 1199 may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0185] As illustrated in FIG. 11C, the remaining N+ layer 1104' may have been layer transferred to acceptor substrate 1110. The top surface of N+ layer 1104' may be chemically or mechanically polished or etched to the desired thickness. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor substrate 1110 alignment marks (not shown). A low temperature CMP and plasma/RIE etch stop layer 1105, such as, for example, low temperature silicon nitride (SiN) on silicon oxide, may be deposited on top of N+ layer 1104'. The acceptor wafer metal connect pad 1180 is illustrated. For illustration clarity, the oxide layers used to facilitate the wafer to wafer bond are not shown.

[0186] As illustrated in FIG. 11D the CMP & plasma/RIE etch stop layer 1105 and N+ layer 1104' may be masked and etched, and the photoresist subsequently removed. The transistor channel elements 1108 with associated CMP & plasma/RIE etch stop layer 1105' may be formed. A low temperature oxide layer 1109 may be deposited.

[0187] As illustrated in FIG. 11E a chemical mechanical polish (CMP) step may be performed to polish the oxide layer 1109 to the level of the CMP stop layer 1105'. Then the CMP stop layer 1105' may be removed with selective wet or dry chemistry to not harm the top surface of transistor channel elements 1108. A low temperature based Gate Dielectric may be deposited and densified to serve as the junction-less transistor gate dielectric 1111. Alternatively, a low temperature microwave plasma oxidation of the transistor channel element 1108 silicon surfaces may serve as the JLT gate dielectric 1111 or an atomic layer deposition (ALD) technique may be utilized to form the HKMG gate oxide as previously described. Then deposition of a low temperature gate material 1112, such as, for example, P+ doped amorphous silicon, may be performed. Alternatively, a HKMG gate structure may be formed as described previously.

[0188] As illustrated in FIG. 11F the gate material 1112 may be masked and etched to define the gate electrode 1114 that may be in an overlapping crossing manner, generally orthogonal, with respect to the transistor channel elements 1108.

[0189] As illustrated in 3D projection FIG. 11G, the entire structure may be substantially covered with a Low Temperature Oxide 1116, which may be planarized with chemical mechanical polishing. The three sided gate electrode 1114, transistor channel elements 1108, gate dielectric 1111, and acceptor substrate 1110 are shown.

[0190] As illustrated in FIG. 11H, then the contacts and metal interconnects may be formed. The gate contact 1120 connects to the gate electrode 1114. The two transistor channel terminal contacts (source and drain) 1122 independently connect to the transistor channel element 1108 on each side of the gate electrode 1114. The thru layer via 1160 electrically couples the transistor layer metallization to the acceptor substrate 1110 at acceptor wafer metal connect pad 1180. This flow enables the formation of a mono-crystalline silicon channel 1-sided gated junction-less transistor that may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

[0191] A p channel 1-sided gated JLT may be constructed as above with the N+ layer 1104 formed as P+ doped, and the gate material 1112 may be of appropriate work function to substantially shutoff the p channel at a gate voltage of approximately zero.

[0192] As illustrated in FIGS. 12A to 12J, an n-channel 4-sided gated junction-less transistor (JLT) may be constructed that may be suitable for 3D IC manufacturing. 4-sided gated JLTs can also be referred to as gate-all around JLTs or silicon nanowire JLTs.

[0193] As illustrated in FIG. 12A, a P- (shown) or N- substrate donor wafer 1200 may be processed to include wafer sized layers of N+ doped silicon 1202 and 1206, and wafer sized layers of n+ SiGe 1204 and 1208. Layers 1202, 1204, 1206, and 1208 may be grown epitaxially and may be carefully engineered in terms of thickness and stoichiometry to keep the defect density that may result from the lattice mismatch between Si and SiGe low. The stoichiometry of the SiGe may be unique to each SiGe layer to provide for different etch rates as may be described later. Some techniques for achieving this include keeping the thickness of the SiGe layers below the critical thickness for forming defects. The top surface of P- substrate donor wafer 1200 may be prepared for oxide wafer bonding with a deposition of an oxide 1213. These processes may be done at temperatures above approximately 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done. The N+ doping layers 1202 and 1206 may have a doping concentration that may be more than 10x the doping concentration of P-substrate donor wafer 1200.

[0194] As illustrated in FIG. 12B, a layer transfer demarcation plane 1299 (shown as a dashed line) may be formed in P- substrate donor wafer 1200 by hydrogen implantation or other methods as previously described.

[0195] As illustrated in FIG. 12C, both the P- substrate donor wafer 1200 and acceptor wafer 1210 top layers and surfaces may be prepared for wafer bonding as previously described and then P- substrate donor wafer donor wafer 1200 may be flipped over, aligned to the acceptor wafer 1210 alignment marks (not shown) and bonded together at a low

temperature (less than approximately 400° C.). Oxide 1213 from the donor wafer and the oxide of the surface of the acceptor wafer 1210 may thus be atomically bonded together are designated as oxide 1214.

[0196] As illustrated in FIG. 12D, the portion of the P-donor wafer substrate 1200 that is above the layer transfer demarcation plane 1299 may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods. A CMP process may be used to remove the remaining P- layer until the N+ silicon layer 1202 may be reached.

[0197] As illustrated in FIG. 12E, stacks of N+ silicon and n+ SiGe regions that may become transistor channels and gate areas may be formed by lithographic definition and plasma/RIE etching of N+ silicon layers 1202 & 1206 and n+ SiGe layers 1204 & 1208. The result may be stacks of n+ SiGe 1216 and N+ silicon 1218 regions. The isolation among stacks may be filled with a low temperature gap fill oxide 1220 and chemically and mechanically polished (CMP'ed) flat. This may fully isolate the transistors from each other. The stack ends are exposed in the illustration for clarity of understanding.

[0198] As illustrated in FIG. 12F, eventual ganged or common gate area 1230 may be lithographically defined and oxide etched. This may expose the transistor channels and gate area stack sidewalls of alternating N+ silicon 1218 and n+ SiGe 1216 regions to the eventual ganged or common gate area 1230. The stack ends are exposed in the illustration for clarity of understanding.

[0199] As illustrated in FIG. 12G, the exposed n+ SiGe regions 1216 may be removed by a selective etch recipe that does not attack the N+ silicon regions 1218. This creates air gaps among the N+ silicon regions 1218 in the eventual ganged or common gate area 1230. Such etching recipes are described in "High performance 5 nm radius twin silicon nanowire MOSFET(TSNWFET): Fabrication on bulk Si wafer, characteristics, and reliability," in *Proc. IEDMTech. Dig.*, 2005, pp. 717-720 by S. D. Suk, et. al. The n+ SiGe layers farthest from the top edge may be stoichiometrically crafted such that the etch rate of the layer (now region) farthest from the top (such as n+ SiGe layer 1208) may etch slightly faster than the layer (now region) closer to the top (such as n+ SiGe layer 1204), thereby equalizing the eventual gate lengths of the two stacked transistors. The stack ends are exposed in the illustration for clarity of understanding.

[0200] As illustrated in FIG. 12H, a step of reducing the surface roughness, rounding the edges, and thinning the diameter of the N+ silicon regions 1218 that may be exposed in the ganged or common gate area may utilize a low temperature oxidation and subsequent HF etch removal of the oxide just formed. This step may be repeated multiple times. Hydrogen may be added to the oxidation or separately utilized as a plasma treatment to the exposed N+ silicon surfaces. The result may be a rounded silicon nanowire-like structure to form the eventual transistor gated channel 1236. The stack ends are exposed in the illustration for clarity of understanding.

[0201] As illustrated in FIG. 12I a low temperature based Gate Dielectric (not shown in this Fig.) may be deposited and densified to serve as the junction-less transistor gate oxide. Alternatively, a low temperature microwave plasma oxidation of the eventual transistor gated channel 1236 silicon surfaces may serve as the JLT gate oxide or an atomic layer deposition (ALD) technique may be utilized to form the HKMG gate

oxide as previously described. Then deposition of a low temperature gate material with proper work function and less than approximately 400° C. deposition temperature, such as, for example, P+ doped amorphous silicon, may be performed, to form gate 1212. Alternatively, a HKMG gate structure may be formed as described previously. A CMP may be performed after the gate material deposition. The stack ends are exposed in the illustration for clarity of understanding.

[0202] FIG. 12J illustrates the JLT transistor stack formed in FIG. 12I with the oxide removed for clarity of viewing, and a cross-sectional cut I of FIG. 12I. Gate 1212 and gate dielectric 1211 surrounds the transistor gated channel 1236 and each ganged or common transistor stack may be isolated from one another by oxide 1222. The source and drain connections of the transistor stacks can be made to the N+Silicon 1218 and n+ SiGe 1216 regions that may not be covered by the gate 1212.

[0203] Contacts to the 4-sided gated JLT source, drain, and gate may be made with conventional Back end of Line (BEOL) processing as described previously and coupling from the formed JLTs to the acceptor wafer may be accomplished with formation of a thru layer via connection to an acceptor wafer metal interconnect pad also described previously. This flow enables the formation of a mono-crystalline silicon channel 4-sided gated junction-less transistor that may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

[0204] A p channel 4-sided gated JLT may be constructed as above with the N+ silicon layers 1202 and 1208 formed as P+ doped, and the gate metals of gate 1212 may be of appropriate work function to shutoff the p channel at a gate voltage of zero.

[0205] While the process flow shown in FIG. 12A-J illustrates the key steps involved in forming a four-sided gated JLT with 3D stacked components, it is conceivable to one skilled in the art that changes to the process can be made. For example, process steps and additional materials/regions, such as a stressed oxide within the transistor isolation regions, to add strain to JLTs may be added. Additionally, N+SiGe layers 1204 and 1208 may instead include p+SiGe or undoped SiGe and the selective etchant formula adjusted. Furthermore, more than two layers of chips or circuits can be 3D stacked. Moreover there may be many methods to construct silicon nanowire transistors. These are described in "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," *Electron Devices Meeting (IEDM)*, 2009 *IEEE International*, vol., no., pp. 1-4, 7-9 Dec. 2009 by Bangsaruntip, S.; Cohen, G. M.; Majumdar, A.; et al. ("Bangsaruntip") and in "High performance 5 nm radius twin silicon nanowire MOSFET (TSN-WFET): Fabrication on bulk Si wafer, characteristics, and reliability," in *Proc. IEDM Tech. Dig.*, 2005, pp. 717-720 by S. D. Suk, S.-Y. Lee, S.-M. Kim, et al. ("Suk"). Contents of these publications are incorporated in this document by reference. The techniques described in these publications can be utilized for fabricating four-sided gated JLTs.

[0206] Turning the channel off with minimal leakage at an approximately zero gate bias may be a major challenge for a junction-less transistor device. To enhance gate control over the transistor channel, the channel may be doped unevenly; whereby the heaviest doping may be closest to the gate or gates and the channel doping may be lighter farther away from the gate electrode. For example, the cross-sectional

center of a 2, 3, or 4 gate sided junction-less transistor channel may be more lightly doped than the edges. This may enable much lower transistor off currents for the same gate work function and control.

[0207] As illustrated in FIGS. 13A and 13B, drain to source current ( $I_{ds}$ ) as a function of the gate voltage ( $V_g$ ) for various junction-less transistor channel doping levels may be simulated where the total thickness of the n-type channel may be about 20 nm. The y-axis of FIG. 13A is plotted as logarithmic and FIG. 13B as linear. Two of the four curves in each figure correspond to evenly doping the 20 nm channel thickness to  $1E17$  and  $1E18$  atoms/cm<sup>3</sup>, respectively. The remaining two curves show simulation results where the 20 nm channel has two layers of 10 nm thickness each. In the legend denotations for the remaining two curves, the first number corresponds to the 10 nm portion of the channel that is the closest to the gate electrode. For example, the curve  $D=1E18/1E17$  illustrates the simulated results where the 10 nm channel portion doped at  $1E18$  is closest to the gate electrode while the 10 nm channel portion doped at  $1E17$  is farthest away from the gate electrode. In FIG. 13A, curves 1302 and 1304 correspond to doping patterns of  $D=1E18/1E17$  and  $D=1E17/1E18$ , respectively. According to FIG. 13A, at a  $V_g$  of 0 volts, the off current for the doping pattern of  $D=1E18/1E17$  is approximately 50 times lower than that of the reversed doping pattern of  $D=1E17/1E18$ . Likewise, in FIG. 13B, curves 1306 and 1308 correspond to doping patterns of  $D=1E18/1E17$  and  $D=1E17/1E18$ , respectively. FIG. 13B illustrates that at a  $V_g$  of 1 volt, the  $I_{ds}$  of both doping patterns are within a few percent of each other.

[0208] The junction-less transistor channel may be constructed with even, graded, or discrete layers of doping. The channel may be constructed with materials other than doped mono-crystalline silicon, such as, for example, poly-crystalline silicon, or other semi-conducting, insulating, or conducting material, such as, for example, graphene or other graphitic material, and may be in combination with other layers of similar or different material. For example, the center of the channel may include a layer of oxide, or of lightly doped silicon, and the edges more heavily doped single crystal silicon. This may enhance the gate control effectiveness of the off state of the resistor, and may increase the on-current as a result of strain effects on the other layer or layers in the channel. Strain techniques may be employed from covering and insulator material above, below, and surrounding the transistor channel and gate. Lattice modifiers may be employed to strain the silicon, such as, for example, an embedded SiGe implantation and anneal. The cross section of the transistor channel may be rectangular, circular, or oval shaped, to enhance the gate control of the channel. Alternatively, to optimize the mobility of the P-channel junction-less transistor in the 3D layer transfer method, the donor wafer may be rotated with respect to the acceptor wafer prior to bonding to facilitate the creation of the P-channel in the <110> silicon plane direction or may include other silicon crystal orientations such as <511>.

[0209] As illustrated in FIGS. 14A to 14I, an n-channel 3-sided gated junction-less transistor (JLT) may be constructed that may be suitable for 3D IC manufacturing. This structure may improve the source and drain contact resistance by providing for a higher doping at the metal contact surface than in the transistor channel. Additionally, this structure may be utilized to create a two layer channel wherein the layer closest to the gate may be more highly doped.

[0210] As illustrated in FIG. 14A, an N- substrate donor wafer 1400 may be processed to include two wafer sized layers of N+ doping 1403 and 1404. The top N+ layer 1404 may have a lower doping concentration than the bottom N+ doping layer 1403. The bottom N+ doping layer 1403 may have a doping concentration that may be more than 10x the doping concentration of top N+ layer 1404. The N+ doping layers 1403 and 1404 may be formed by ion implantation and thermal anneal. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ silicon with differing dopant concentrations or by a combination of epitaxy and implantation. A screen oxide 1401 may be grown or deposited before the implants to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. The N+ layer 1404 may alternatively be a deposited layer of heavily N+ doped polysilicon that may be optically annealed to form large grains, or the structures may be formed by one or more depositions of in-situ doped amorphous silicon to create the various dopant layers or gradients. The N+ doped layer 1404 may be formed by doping the N- substrate donor wafer 1400 by Plasma Assisted Doping (PLAD) techniques. These processes may be done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done.

[0211] As illustrated in FIG. 14B, the top surface of N- substrate donor wafer 1400 may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the N+ layer 1404 to form oxide layer 1402, or a re-oxidation of implant screen oxide 1401. A layer transfer demarcation plane 1499 (shown as a dashed line) may be formed in N- substrate donor wafer 1400 or in the N+ layer 1404 (as shown) by hydrogen implantation 1407 or other methods as previously described. Both the N- substrate donor wafer 1400 and acceptor wafer 1410 may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer 1403 and the N- substrate donor wafer 1400 that may be above the layer transfer demarcation plane 1499 may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0212] As illustrated in FIG. 14C, the remaining N+ layer 1403', lighter N+ doped layer 1404, and oxide layer 1402 have been layer transferred to acceptor wafer 1410. The top surface of N+ layer 1403' may be chemically or mechanically polished and an etch hard mask layer of low temperature silicon nitride may be deposited on the surface of N+ layer 1403', including a thin oxide stress buffer layer, thus forming silicon nitride etch hard mask layer 1405. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer 1410 alignment marks (not shown). The acceptor wafer metal connect pad 1480 is illustrated. For illustration clarity, the oxide layers used to facilitate the wafer to wafer bond are not shown in subsequent drawings.

[0213] As illustrated in FIG. 14D the source and drain connection areas may be lithographically defined, the silicon nitride etch hard mask layer 1405 may be etched, and the photoresist may be removed, leaving etch hard mask regions 1415. A partial or full silicon plasma/RIE etch may be performed to thin or remove N+ layer 1403'. Alternatively, one or more a low temperature oxidations coupled with a Hydrofluoric Acid etch of the formed oxide may be utilized to thin

N+ layer 1403'. This results in a two-layer channel, as described and simulated above in conjunction with FIGS. 13A and 13B, formed by thinning N+ layer 1403' with the above etch process to almost complete removal, leaving some of N+ layer 1403' remaining (now labeled 1413) on top of the lighter N+ doped 1404 layer and the full thickness of N+ layer 1403' (now labeled 1414) still remaining underneath the etch hard mask regions 1415. A substantially complete removal of the top channel N+ layer 1403' in the areas not underneath etch hard mask regions 1415 may be performed. This etch process may be utilized to adjust for post layer transfer cleave wafer-to-wafer CMP variations of the remaining donor wafer layers, such as N- substrate donor wafer 1400 and N+ layer 1403' and provide less variability in the final channel thickness.

[0214] As illustrated in FIG. 14E photoresist 1450 may be lithographically defined to substantially cover the source and drain connection areas 1414 and the heavier N+ doped transistor channel layer region 1453, previously a portion of thinned N+ doped layer 1413.

[0215] As illustrated in FIG. 14F the exposed portions of thinned N+ doped layer 1413 and the lighter N+ doped layer 1404 may be plasma/RIE etched and the photoresist 1450 removed. The etch forms source connection region 1451 and drain connection region 1452, provides isolation among transistors, and defines the width of the JLT channel which may include lighter doped N+ region 1408 and thinned heavier N+ doped layer region 1453.

[0216] As illustrated in FIG. 14G, a low temperature based Gate Dielectric may be deposited and densified to serve as the gate dielectric 1411 for the junction-less transistor. Alternatively, a low temperature microwave plasma oxidation of the lighter doped N+ region 1408 silicon surfaces may serve as the JLT gate dielectric 1411 or an atomic layer deposition (ALD) technique may be utilized to form the HKMG gate oxide as previously described. Then deposition of a low temperature gate material with proper work function and less than approximately 400° C. deposition temperature, such as, for example, P+ doped amorphous silicon, may be performed to form gate 1412. Alternatively, a HKMG gate structure may be formed as described previously.

[0217] As illustrated in FIG. 14H, the gate material of gate 1412 may be masked and etched to define the three sided (top and two side) gate electrode 1464 that may be in an overlapping crossing manner, generally orthogonal, with respect to the transistor channel lighter doped N+ region 1408.

[0218] As illustrated in 14I, the entire structure may be substantially covered with a Low Temperature Oxide 1416, which may be planarized with chemical mechanical polishing. The three sided gate electrode 1464, N+ transistor channel composed of lighter N+ doped region 1408 and heavier doped N+ silicon region 1453, gate dielectric 1411, source connection region 1451, and drain connection region 1452 are shown. Contacts and metal interconnects may be formed. The gate contact 1420 connects to the gate electrode 1464. The two transistor channel terminal contacts (source and drain) 1422 independently connect to the heavier doped N+ silicon region 1453 on each side of the gate electrode 1464. The layer via 1460 electrically couples the transistor layer metallization to the acceptor wafer 1410 at acceptor wafer metal connect pad 1480. This flow enables the formation of a mono-crystalline silicon channel with 1, 2, or 3-sided gated junction-less transistor with uniform, graded, or multiple layers of dopant levels in the transistor channel, which may be

formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature processing step.

[0219] A p channel 1, 2, or 3-sided gated JLT may be constructed as above with the N+ layers 1404 and 1403 formed as P+ doped, and the gate material of gate 1412 may be of appropriate work function to shutoff the p channel at a gate voltage of approximately zero.

[0220] A junction-less FinFet may also be constructed similarly, wherein heavier doped N+ silicon region 1453 may be substantially etched away leaving behind source connection region 1451 and drain connection region 1452, and the thickness of lighter N+ doped region 1408 may be greater than its width (forming the fin), and three sided (top and two side) gate electrode 1464 with gate dielectric 1411 may control the electrostatic properties (such as on and off transistor states) of the fin. Thus, the heavier doped N+ silicon region 1453 may provide good contact resistance to the eventual source and drain contacts (for example, the two transistor channel terminal contacts (source and drain) 1422), while the lighter N+ doped region 1408 (or "fin") may be undoped or of light doping such that it can be electrostatically controlled by the three sided (top and two side) gate electrode 1464. A junctioned FinFet may be constructed similarly to the junction-less FinFet wherein the dopant type, such as n or p type dopant, of source connection region 1451 and drain connection region 1452 may be different than the dopant type of the transistor channel, for example, the lighter N+ doped region 1408.

[0221] A planar n-channel Junction-Less Recessed Channel Array Transistor (JLRCAT) suitable for a monolithic 3D IC may be constructed as follows. The JLRCAT may provide an improved source and drain contact resistance, thereby allowing for lower channel doping, and the recessed channel may provide for more flexibility in the engineering of channel lengths and transistor characteristics, and increased immunity from process variations.

[0222] As illustrated in FIG. 58A, a N- substrate donor wafer 5800 may be processed to include wafer sized layers of N+ doping 5802, and N- doping 5803 across the wafer. The N+ doped layer 5802 may be formed by ion implantation and thermal anneal. N- doped layer 5803 may have additional ion implantation and anneal processing to provide a different dopant level than N-substrate donor wafer 5800. N- doped layer 5803 may have graded or various layers of N-doping to mitigate transistor performance issues, such as, for example, short channel effects, after the JLRCAT is formed. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ 5802 and N-5803, or by a combination of epitaxy and implantation Annealing of implants and doping may utilize optical annealing techniques or types of Rapid Thermal Anneal (RTA or spike). The N+ doped layer 5802 may have a doping concentration that may be more than 10x the doping concentration of N- doped layer 5803.

[0223] As illustrated in FIG. 58B, the top surface of N-substrate donor wafer 5800 may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of N-doped layer 5803 to form oxide layer 5880. A layer transfer demarcation plane (shown as dashed line) 5899 may be formed by hydrogen implantation or other methods as previously described. Both the N- substrate donor wafer 5800 and acceptor wafer 5810 may be prepared for wafer bonding as previously described and then low temperature

(less than approximately 400° C.) bonded. Acceptor wafer 5810, as described previously, may include, for example, transistors, circuitry, and metal, such as, for example, aluminum or copper, interconnect wiring, and thru layer via metal interconnect strips or pads. The portion of the N+ doped layer 5802 and the N-substrate donor wafer 5800 that may be above the layer transfer demarcation plane 5899 may be removed by cleaving or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0224] As illustrated in FIG. 58C, oxide layer 5880, N-doped layer 5803, and remaining N+ layer 5822 have been layer transferred to acceptor wafer 5810. The top surface of N+ layer 5822 may be chemically or mechanically polished. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer 5810 alignment marks (not shown).

[0225] As illustrated in FIG. 58D, the transistor isolation regions 5805 may be formed by mask defining and then plasma/RIE etching N+ layer 5822 and N- doped layer 5803 substantially to the top of oxide layer 5880, substantially into oxide layer 5880, or into a portion of the upper oxide layer of acceptor wafer 5810. Then a low-temperature gap fill oxide may be deposited and chemically mechanically polished, the oxide remaining in isolation regions 5805. Then the recessed channel 5806 may be mask defined and etched thru N+ doped layer 5822 and partially into N- doped layer 5803. The recessed channel surfaces and edges may be smoothed by processes, such as, for example, wet chemical, plasma/RIE etching, low temperature hydrogen plasma, or low temperature oxidation and strip techniques, to mitigate high field effects. The low temperature smoothing process may employ, for example, a plasma produced in a TEL (Tokyo Electron Labs) SPA (Slot Plane Antenna) machine. These process steps may form N+ source and drain regions 5832 and N-channel region 5823, which may form the transistor body. The doping concentration of N+ source and drain regions 5832 may be more than 10x the concentration of N- channel region 5823. The doping concentration of the N- channel region 5823 may include gradients of concentration or layers of differing doping concentrations. The etch formation of recessed channel 5806 may define the transistor channel length.

[0226] As illustrated in FIG. 58E, a gate dielectric 5807 may be formed and a gate metal material may be deposited. The gate dielectric 5807 may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Alternatively, the gate dielectric 5807 may be formed with a low temperature processes including, for example, oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate material with proper work function and less than approximately 400° C. deposition temperature such as, for example, tungsten or aluminum may be deposited. Then the gate material may be chemically mechanically polished, and the gate area defined by masking and etching, thus forming the gate electrode 5808.

[0227] As illustrated in FIG. 58F, a low temperature thick oxide 5809 may be deposited and planarized, and source, gate, and drain contacts, and thru layer via (not shown) openings may be masked and etched preparing the transistors to be connected via metallization. Thus gate contact 5811 connects to gate electrode 5808, and source & drain contacts 5840

connect to N+ source and drain regions **5832**. The thru layer via (not shown) provides electrical coupling among the donor wafer transistors and the acceptor wafer metal connect pads or strips (not shown) as previously described.

[0228] The formation procedures of and use of the N+ source and drain regions **5832** that may have more than 10× the concentration of N- channel region **5823** may enable low contact resistance in a FinFet type transistor, where the thickness of the transistor channel is greater than the width of the channel, the transistor channel width being perpendicular to a line formed between the source and drain.

[0229] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **58A** through **58F** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, a p-channel JLRCAT may be formed with changing the types of dopings appropriately. Moreover, the N- substrate donor wafer **5800** may be p type. Further, N-doped layer **5803** may include multiple layers of different doping concentrations and gradients to fine tune the eventual JLRCAT channel for electrical performance and reliability characteristics, such as, for example, off-state leakage current and on-state current. Furthermore, isolation regions **5805** may be formed by a hard mask defined process flow, wherein a hard mask stack, such as, for example, silicon oxide and silicon nitride layers, or silicon oxide and amorphous carbon layers, may be utilized. Moreover, CMOS JLRCATs may be constructed with n-JLRCATs in one mono-crystalline silicon layer and p-JLRCATs in a second mono-crystalline layer, which may include different crystalline orientations of the mono-crystalline silicon layers, such as for example, <100>, <111> or <551>, and may include different contact silicides for optimum contact resistance to p or n type source, drains, and gates. Furthermore, a back-gate or double gate structure may be formed for the JLRCAT and may utilize techniques described elsewhere in this document. Further, efficient heat removal and transistor body biasing may be accomplished on a JLRCAT by adding an appropriately doped buried layer (P- in the case of a n-JLRCAT) and then forming a buried layer region underneath the N- channel region **5823** for junction isolation and connecting that buried region to a thermal and electrical contact, similar to what is described for layer **1606** and region **1646** in FIGS. **16A-G**. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0230] As illustrated in FIGS. **15A** to **15I**, an n-channel planar Junction Field Effect Transistor (JFET) may be constructed that may be suitable for 3D IC manufacturing.

[0231] As illustrated in FIG. **15A**, an N- substrate donor wafer **1500** may be processed to include two wafer sized layers of N+ layer **1503** and N- doped layer **1504**. The N-doped layer **1504** may have the same or different dopant concentration than the N- substrate donor wafer **1500**. The N+ layer **1503** and N- doped layer **1504** may be formed by ion implantation and thermal anneal. The N+ layer **1503** may have a doping concentration that may be more than 10× the doping concentration of N- doped layer **1504**. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ silicon then N- silicon or by a combination of epitaxy and implantation. A screen oxide **1501** may be grown before an implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. These processes may be

done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done.

[0232] As illustrated in FIG. **15B**, the top surface of N- substrate donor wafer **1500** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the N-doped layer **1504** to form oxide layer **1502**, or a re-oxidation of implant screen oxide **1501**. A layer transfer demarcation plane **1599** (shown as a dashed line) may be formed in N- substrate donor wafer **1500** or N+ layer **1503** (shown) by hydrogen implantation **1507** or other methods as previously described. Both the N- substrate donor wafer **1500** and acceptor wafer **1510** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer **1503** and the N- substrate donor wafer **1500** that may be above the layer transfer demarcation plane **1599** may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0233] As illustrated in FIG. **15C**, the remaining N+ doped silicon layer **1503'**, N- doped layer **1504**, and oxide layer **1502** have been layer transferred to acceptor wafer **1510**. The top surface of N+ doped silicon layer **1503'** may be chemically or mechanically polished smooth and flat. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer **1510** alignment marks (not shown). For illustration clarity, the oxide layers, such as, for example, oxide layer **1502**, used to facilitate the wafer to wafer bond, are not shown in subsequent drawings.

[0234] As illustrated in FIG. **15D** the source and drain regions **1520** may be lithographically defined and then formed by etching away portions of N+ doped silicon layer **1503'** down to at least the level of the N- doped layer **1504**.

[0235] As illustrated in FIG. **15E** transistor to transistor isolation regions **1526** may be lithographically defined and the N- doped layer **1504** plasma/RIE etched to form regions of JFET transistor channel **1544**. The doping concentration of the JFET transistor channel N- region **1544** may include gradients of concentration or sub-layers of doping concentration.

[0236] As illustrated in FIG. **15F**, formation of a shallow P+ region **1530** may be performed to create a JFET gate by utilizing a mask defined implant of P+ type dopant, such as, for example, Boron. In this example a laser or other method of optical annealing may be utilized to activate the P+ implanted dopant.

[0237] As illustrated in FIG. **15G**, after a deposition and planarization of thick oxide **1542**, a layer of a laser light or optical anneal radiation reflecting material, such as, for example, aluminum or copper, may be deposited if the P+ gate implant is utilized. An opening **1554** in the reflective layer may be masked and etched, thus forming reflective regions **1550** and allowing the laser light or optical anneal energy **1560** to heat the shallow P+ region **1530**, and reflecting the majority of the laser or optical anneal energy **1560** away from acceptor wafer **1510**. Typically, the opening **1554** area may be less than 10% of the total wafer area, thus greatly reducing the thermal stress on the underlying metal layers contained in acceptor wafer **1510**. Additionally, a barrier metal clad copper region **1582**, or, alternatively, a reflective Aluminum layer or other laser light or optical anneal radiation reflective material, may be formed in the acceptor wafer

**1510** pre-processing and positioned under the reflective layer opening **1554** such that it may reflect any of the unwanted laser or optical anneal energy **1560** that might travel to the acceptor wafer **1510**. Acceptor substrate metal layer copper region **1582** may be utilized as a back-gate or back-bias source for the JFET transistor above it. In addition, absorptive materials may, alone or in combination with reflective materials, be utilized in the above laser or other methods of optical annealing techniques.

[0238] As illustrated in FIG. 15H, an optical energy absorptive region **1556** of, for example, amorphous carbon, may be formed by low temperature deposition or sputtering and subsequent lithographic definition and plasma/RIE etching. This allows the minimum laser or other optical energy to be employed that effectively heats the implanted area to be activated, and thereby minimizes the heat stress on the reflective regions **1550** and **1582** and the acceptor wafer **1510** metallization.

[0239] As illustrated in FIG. 15I, the reflective material, such as reflective regions **1550**, if utilized, may be removed, and the gate contact **1561** may be masked and etched open thru thick oxide **1542** to shallow P+ region **1530** or transistor channel N- region **1544**. Then deposition and partial etch-back (or Chemical Mechanical Polishing (CMP)) of aluminum (or other metal to obtain an optimal Schottky or ohmic gate contact **1561** to either transistor channel N- region **1544** or shallow P+ gate region **1530** respectively) may be performed. N+ contacts **1562** may be masked and etched open and metal may be deposited to create ohmic connections to the N+ regions **1520**. Interconnect metallization may then be conventionally formed. The thru layer via (not shown) may be formed to electrically couple the JFET transistor layer metallization to the acceptor wafer **1510** at acceptor wafer metal connect pad (not shown). This flow enables the formation of a mono-crystalline silicon channel JFET that may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

[0240] A p channel JFET may be constructed as above with the N- doped layer **1504** and N+ layer **1503** formed as P- and P+ doped respectively, and the shallow P+ gate region **1530** formed as N+, and gate metal may be of appropriate work function to create a proper Schottky barrier.

[0241] As illustrated in FIGS. 16A to 16G, an n-channel planar Junction Field Effect Transistor (JFET) with integrated bottom gate junction may be constructed that may be suitable for 3D IC manufacturing.

[0242] As illustrated in FIG. 16A, an N- substrate donor wafer **1600** may be processed to include three wafer sized layers of N+ doping **1603**, N- doping **1604**, and P+ doping **1606**. The N- doped layer **1604** may have the same or a different dopant concentration than the N- substrate donor wafer **1600**. The N+ doping layer **1603**, N- doped layer **1604**, and P+ doping layer **1606** may be formed by ion implantation and thermal anneal. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ silicon then N- silicon then P+ silicon or by a combination of epitaxy and implantation. The P+ doped layer **1606** may be formed by doping the top layer by Plasma Assisted Doping (PLAD) techniques. A screen oxide **1601** may be grown before an implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. These processes may be done at temperatures above about 400° C. as the layer transfer to the

processed substrate with metal interconnects has yet to be done. The N+ doping layer **1603** may have a doping concentration that may be more than 10× the doping concentration of N- doped layer **1604**.

[0243] As illustrated in FIG. 16B, the top surface of N- substrate donor wafer **1600** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the P+ layer **1606** to form oxide layer **1602**, or a re-oxidation of implant screen oxide **1601**. A layer transfer demarcation plane **1699** (shown as a dashed line) may be formed in N- substrate donor wafer **1600** or N+ doping layer **1603** (shown) by hydrogen implantation **1607** or other methods as previously described. Both the N- substrate donor wafer **1600** and acceptor wafer **1610** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ doping layer **1603** and the N- substrate donor wafer **1600** that may be above the layer transfer demarcation plane **1699** may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0244] As illustrated in FIG. 16C, the remaining N+ doped layer **1603'**, N- doped layer **1604**, P+ doped layer **1606**, and oxide layer **1602** have been layer transferred to acceptor wafer **1610**. The top surface of N+ doped layer **1603'** may be chemically or mechanically polished smooth and flat. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer **1610** alignment marks (not shown). For illustration clarity, the oxide layers, such as **1602**, used to facilitate the wafer to wafer bond are not shown in subsequent drawings.

[0245] As illustrated in FIG. 16D the source and drain regions **1643** may be lithographically defined and then formed by etching away portions of N+ doped layer **1603'** down to at least the level of the N- doped layer **1604**.

[0246] As illustrated in FIG. 16E transistor channel regions may be lithographically defined and the N- doped layer **1604** plasma/RIE etched to form regions of JFET transistor channel **1644**. The doping concentration of the JFET transistor channel region **1644** may include gradients of concentration or discrete sub-layers of doping concentration. Then transistor to transistor isolation **1626** may be lithographically defined and the P+ doped layer **1606** plasma/RIE etched to form the P+ bottom gate junction regions **1646**.

[0247] As illustrated in FIG. 16F, formation of a shallow P+ region **1630** may be performed to create a JFET gate junction by utilizing a mask defined implant of P+ dopant, such as, for example, Boron. Laser or other method of optical annealing may be utilized to activate the P+ implanted dopant without damaging the underlying layers using reflective and/or absorbing layers as described previously.

[0248] As illustrated in FIG. 16G, after the deposition and planarization of thick oxide **1642** the gate contact **1660** may be masked and etched open thru thick oxide **1642** to shallow P+ region **1630** (if utilized) or transistor channel region **1644**. Then deposition and partial etch-back (or Chemical Mechanical Polishing (CMP)) of aluminum (or other metal to obtain an optimal Schottky or ohmic gate contact **1660** to either transistor channel region **1644** or shallow P+ gate region **1630** respectively) may be performed. N+ contacts **1662** may be masked and etched open and metal may be deposited to create ohmic connections to the N+ regions **1643**. P+ bottom gate junction contacts **1666** may be masked and etched open and metal may be deposited to create ohmic connections to the P+

bottom gate junction regions **1646**. Interconnect metallization may then be conventionally formed. The layer via (not shown) may be formed to electrically couple the JFET transistor layer metallization to the acceptor wafer **1610** at acceptor wafer metal connect pad (not shown). This flow enables the formation of a mono-crystalline silicon channel JFET with integrated bottom gate junction that may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

**[0249]** A p channel JFET with integrated bottom gate junction may be constructed as above with the N- doped layer **1604** and N+ doping layer **1603** formed as P- and P+ doped respectively, the P+ bottom gate junction layer **1060** formed as N+ doped, and the shallow P+ gate region **1630** formed as N+, and gate metal may be of appropriate work function to create a proper Schottky barrier.

**[0250]** As illustrated in FIGS. **17A** to **17G**, an NPN bipolar junction transistor may be constructed that may be suitable for 3D IC manufacturing.

**[0251]** As illustrated in FIG. **17A**, an N- substrate donor wafer **1700** may be processed to include four wafer sized layers of N+ doping **1703**, P- doping **1704**, N- doping **1706**, and N+ doping **1708**. The N- doped layer **1706** may have the same or different dopant concentration than the N-substrate donor wafer **1700**. The four doped layers **1703**, **1704**, **1706**, and **1708** may be formed by ion implantation and thermal anneal. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers or by a combination of epitaxy and implantation and anneals. A screen oxide **1701** may be grown before an implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. These processes may be done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done. N+ doping layer **1703** may have a doping concentration that may be more than 10x the doping concentration of N-doped layer **1706** and P- doped layer **1704**.

**[0252]** As illustrated in FIG. **17B**, the top surface of N- substrate donor wafer **1700** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the N+ layer **1708** to form oxide layer **1702**, or a re-oxidation of implant screen oxide **1701**. A layer transfer demarcation plane **1799** (shown as a dashed line) may be formed in N- substrate donor wafer **1700** or N+ layer **1703** (shown) by hydrogen implantation **1707** or other methods as previously described. Both the N- substrate donor wafer **1700** and acceptor wafer **1710** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer **1703** and the N- substrate donor wafer **1700** that may be above the layer transfer demarcation plane **1799** may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods. Effectively at this point there may be a giant npn or bipolar transistor overlaying the entire wafer.

**[0253]** As illustrated in FIG. **17C**, the remaining N+ doped layer **1703'**, P- doped layer **1704**, N-doped layer **1706**, N+ doped layer **1708**, and oxide layer **1702** have been layer transferred to acceptor wafer **1710**. The top surface of N+ doped layer **1703'** may be chemically or mechanically polished smooth and flat. Now multiple transistors may be

formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer **1710** alignment marks (not shown). For illustration clarity, the oxide layers, such as **1702**, used to facilitate the wafer to wafer bond are not shown in subsequent drawings.

**[0254]** As illustrated in FIG. **17D** the emitter regions **1733** may be lithographically defined and then formed by plasma/RIE etch removal of portions of N+ doped layer **1703'** down to at least the level of the P- doped layer **1704**.

**[0255]** As illustrated in FIG. **17E** the base **1734** and collector **1736** regions may be lithographically defined and formed by plasma/RIE etch removal of portions of P- doped layer **1704** and N- doped layer **1706** down to at least the level of the N+ layer **1708**.

**[0256]** As illustrated in FIG. **17F** the collector connection region **1738** may be lithographically defined and formed by plasma/RIE etch removal of portions of N+ doped layer **1708** down to at least the level of the top oxide of acceptor wafer **1710**. This may create electrical isolation among transistors.

**[0257]** As illustrated in FIG. **17G**, the entire structure may be substantially covered with a Low Temperature Oxide **1762**, which may be planarized with chemical mechanical polishing. The emitter regions **1733**, the base region **1734**, the collector region **1736**, the collector connection region **1738**, and the acceptor wafer **1710** are shown. Contacts and metal interconnects may be formed by lithography and plasma/RIE etch. The emitter contact **1742** connects to the emitter regions **1733**. The base contact **1740** connects to the base region **1734**, and the collector contact **1744** connects to the collector connection region **1738**. Interconnect metallization may then be conventionally formed. The thru layer via (not shown) may be formed to electrically couple the NPN bipolar transistor layer metallization to the acceptor wafer **1710** at acceptor wafer metal connect pad (not shown). This flow enables the formation of a mono-crystalline silicon NPN bipolar junction transistor that may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

**[0258]** A PNP bipolar junction transistor may be constructed as above with the N- doped layer **1706** and N+ layers **1703** and **1708** formed as P- and P+ doped respectively, and the P- doped layer **1704** formed as N-.

**[0259]** The bipolar transistors formed with reference to FIG. **17** may be utilized to form analog or digital BiCMOS circuits where the CMOS transistors may be on the acceptor wafer **1710** and the bipolar transistors may be formed in the transferred top layers.

**[0260]** As illustrated in FIGS. **18A** to **18J**, an n-channel raised source and drain extension transistor may be constructed that may be suitable for 3D IC manufacturing.

**[0261]** As illustrated in FIG. **18A**, a P- substrate donor wafer **1800** may be processed to include two wafer sized layers of N+ doping **1803** and P- doping **1804**. The P- doped layer **1804** may have the same or a different dopant concentration than the P- substrate donor wafer **1800**. The N+ doped layer **1803** and P- doped layer **1804** may be formed by ion implantation and thermal anneal. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of N+ silicon then P- silicon or by a combination of epitaxy and implantation. The N+ doped layer **1803** may have a doping concentration that may be more than 10x the doping concentration of P- doped layer **1804**. The doping concentration of the P- doped layer **1804** may include gradients of concentration or sub-layers of doping concentration. A



screen oxide **1801** may be grown before an implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. These processes may be done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done.

[0262] As illustrated in FIG. 18B, the top surface of P-substrate donor wafer **1800** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the P-layer **1804** to form oxide layer **1802**, or a re-oxidation of implant screen oxide **1801**. A layer transfer demarcation plane **1899** (shown as a dashed line) may be formed in P-substrate donor wafer **1800** or N+ doped layer **1803** (shown) by hydrogen implantation **1807** or other methods as previously described. Both the P-substrate donor wafer **1800** and acceptor wafer **1810** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ doped layer **1803** and the P-substrate donor wafer **1800** that may be above the layer transfer demarcation plane **1899** may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0263] As illustrated in FIG. 18C, the remaining N+ layer **1803'**, P-doped layer **1804**, and oxide layer **1802** have been layer transferred to acceptor wafer **1810**. The top surface of N+ layer **1803'** may be chemically or mechanically polished smooth and flat. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer **1810** alignment marks (not shown). For illustration clarity, the oxide layers, such as **1802**, used to facilitate the wafer to wafer bond are not shown in subsequent drawings.

[0264] As illustrated in FIG. 18D the raised source and drain regions **1833** may be lithographically defined and then formed by etching away portions of N+ layer **1803'** to form a thin more lightly doped N+ layer **1836** for the future source and drain extensions. Then transistor to transistor isolation regions **1820** may be lithographically defined and the thin more lightly doped N+ layer **1836** and the P-doped layer **1804** may be plasma/RIE etched down to at least the level of the top oxide of acceptor wafer **1810** and thus form electrically isolated regions of P-doped transistor channels **1834**.

[0265] As illustrated in FIG. 18E a highly conformal low-temperature oxide or Oxide/Nitride stack may be deposited and plasma/RIE etched to form N+ sidewall spacers **1824** and P-sidewalls spacers **1825**.

[0266] As illustrated in FIG. 18F, a self-aligned plasma/RIE silicon etch may be performed to create source drain extensions **1844** from the thin lightly doped N+ layer **1836**, thus forming eventual gate area **1840**.

[0267] As illustrated in FIG. 18G, a low temperature based Gate Dielectric may be deposited and densified to serve as the gate oxide **1811**. Alternatively, a low temperature microwave plasma oxidation of the exposed transistor P-doped channel **1834** silicon surfaces may serve as the gate oxide **1811** or an atomic layer deposition (ALD) technique may be utilized to form the HKMG gate oxide as previously described.

[0268] As illustrated in FIG. 18H, a deposition of a low temperature gate material with proper work function and less than approximately 400° C. deposition temperature, such as, for example, N+ doped amorphous silicon, may be per-

formed, and etched back to form self-aligned transistor gate **1814**. Alternatively, a HKMG gate structure may be formed as described previously.

[0269] As illustrated in FIG. 18I, the entire structure may be substantially covered with a Low Temperature Oxide **1850**, which may be planarized with chemical mechanical polishing. The raised source and drain regions **1833**, source drain extensions **1844**, P-doped transistor channels **1834**, gate oxide **1811**, transistor gate **1814**, and acceptor wafer **1810** are shown. Contacts and metal interconnects may be formed with lithography and plasma/RIE etch. The gate contact **1854** connects to the gate **1814**. The two transistor channel terminal contacts (source **1852** and drain **1856**) independently connect to the raised N+ source and drain regions **1833**. Interconnect metallization may then be conventionally formed. The thru layer via (not shown) electrically couples the transistor layer metallization to the acceptor wafer **1810** at acceptor wafer metal connect pad (not shown). This flow enables the formation of a mono-crystalline n-channel transistor with raised source and drain extensions, which may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

[0270] As illustrated in FIG. 18J, the top layer of the acceptor wafer **1810** may include a 'back-gate' **1882** whereby gate **1814** may be aligned & formed directly on top of the back-gate **1882**. The back-gate **1882** may be formed from the top metal layer of the acceptor wafer **1810**, or alternatively be composed of doped amorphous silicon, and may utilize the oxide layer deposited on top of the metal layer for the wafer bonding (not shown) to act as a gate oxide for the back-gate **1882**.

[0271] A p-channel raised source and drain extension transistor may be constructed as above with the P-layer **1804** and N+ layer **1803** formed as N- and P+ doped respectively, and gate metal may be of appropriate work function to shutoff the p channel at the desired gate voltage.

[0272] A single type (n or p) of transistor formed in the transferred prefabricated layers could be sufficient for some uses, such as, for example, programming transistors for a Field Programmable Gate Array (FPGA). However, for logic circuitry two complementing (n and p) transistors would be helpful to create CMOS type logic. Accordingly the above described various single- or mono-type transistor flows could be performed twice (with reference to the FIG. 2 discussion). First perform substantially all the steps to build the 'n-channel' type, and then perform an additional layer transfer to build the 'p-channel' type on top of it. Subsequently, the mono-type devices of one layer may be electrically coupled together with the other layer utilizing the available dense interconnects as the layers transferred may be less than approximately 200 nm in thickness.

[0273] Alternatively, full CMOS devices may be constructed with a single layer transfer of wafer sized doped layers. CMOS may include n-type transistors and p-type transistors. This process flow may be described below for the case of n-RCATs and p-RCATs, but may apply to any of the above devices constructed out of wafer sized transferred doped layers.

[0274] As illustrated in FIGS. 19A to 19I, an n-RCAT and p-RCAT may be constructed in a single layer transfer of wafer sized doped layers with a process flow that may be suitable for 3D IC manufacturing.

[0275] As illustrated in FIG. 19A, a P- substrate donor wafer 1900 may be processed to include four wafer sized layers of N+ doping 1903, P- doping 1904, P+ doping 1906, and N- doping 1908. The P- doped layer 1904 may have the same or a different dopant concentration than the P-substrate donor wafer 1900. The four doped layers 1903, 1904, 1906, and 1908 may be formed by ion implantation and thermal anneal. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers or by a combination of epitaxy and implantation and anneals. P- doped layer 1904 and N- doped layer 1908 may have graded or various layers of doping to mitigate transistor performance issues, such as, for example, short channel effects. The N+ doping layer 1903 may have a doping concentration that may be more than 10x the doping concentration of P- doped layer 1904. The P+ doping layer 1906 may have a doping concentration that may be more than 10x the doping concentration of N- doped layer 1908. A screen oxide 1901 may be grown before an implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. These processes may be done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done.

[0276] As illustrated in FIG. 19B, the top surface of P- substrate donor wafer 1900 may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the N-doped layer 1908 to form oxide layer 1902, or a re-oxidation of implant screen oxide 1901. A layer transfer demarcation plane 1999 (shown as a dashed line) may be formed in P- substrate donor wafer 1900 or N+ layer 1903 (shown) by hydrogen implantation 1907 or other methods as previously described. Both the P- substrate donor wafer 1900 and acceptor wafer 1910 may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer 1903 and the P- substrate donor wafer 1900 that may be above the layer transfer demarcation plane 1999 may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[0277] As illustrated in FIG. 19C, the remaining N+ layer 1903', P- doped layer 1904, P+ doped layer 1906, N- doped layer 1908, and oxide layer 1902 have been layer transferred to acceptor wafer 1910. The top surface of N+ layer 1903' may be chemically or mechanically polished smooth and flat. Now multiple transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer 1910 alignment marks (not shown). For illustration clarity, the oxide layers, such as 1902, used to facilitate the wafer to wafer bond are not shown in subsequent drawings.

[0278] As illustrated in FIG. 19D the transistor isolation region may be lithographically defined and then formed by plasma/RIE etch removal of portions of N+ doped layer 1903', P- doped layer 1904, P+ doped layer 1906, and N- doped layer 1908 to at least the top oxide of acceptor wafer 1910. Then a low-temperature gap fill oxide may be deposited and chemically mechanically polished, remaining in transistor isolation region 1920. Thus formed may be future RCAT transistor regions N+ doped 1913, P- doped 1914, P+ doped 1916, and N- doped 1918.

[0279] As illustrated in FIG. 19E the N+ doped region 1913 and P- doped region 1914 of the p-RCAT portion of the wafer may be lithographically defined and removed by either

plasma/RIE etch or a selective wet etch. Then the p-RCAT recessed channel 1942 may be mask defined and etched. The recessed channel surfaces and edges may be smoothed by wet chemical or plasma/RIE etching techniques to mitigate high field effects. These process steps form P+ source and drain regions 1926 and N- transistor channel region 1928, which may form the transistor body. The doping concentration of the N- transistor channel region 1928 may include gradients of concentration or layers of differing doping concentrations. The etch formation of p-RCAT recessed channel 1942 may define the transistor channel length.

[0280] As illustrated in FIG. 19F, a gate dielectric 1911 may be formed and a gate metal material may be deposited. The gate dielectric 1911 may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal material in the industry standard high k metal gate process schemes described previously and targeted for an p-channel RCAT utility. Or the gate dielectric 1911 may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate material with proper work function and less than approximately 400° C. deposition temperature such as, for example, platinum or aluminum may be deposited. Then the gate metal material may be chemically mechanically polished, and the p-RCAT gate electrode 1954' defined by masking and etching.

[0281] As illustrated in FIG. 19G, a low temperature oxide 1950 may be deposited and planarized, substantially covering the formed p-RCAT so that processing to form the n-RCAT may proceed.

[0282] As illustrated in FIG. 19H the n-RCAT recessed channel 1944 may be mask defined and etched. The recessed channel surfaces and edges may be smoothed by wet chemical or plasma/RIE etching techniques to mitigate high field effects. These process steps form N+ source and drain regions 1933 and P- transistor channel region 1934, which may form the transistor body. The doping concentration of the P- transistor channel region 1934 may include gradients of concentration or layers of differing doping concentrations. The etch formation of n-RCAT recessed channel 1944 may define the transistor channel length.

[0283] As illustrated in FIG. 19I, a gate dielectric 1912 may be formed and a gate metal material may be deposited. The gate dielectric 1912 may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal material in the industry standard high k metal gate process schemes described previously and targeted for use in a re-channel RCAT. Or the gate dielectric 1912 may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate material with proper work function and less than approximately 400° C. deposition temperature such as, for example, tungsten or aluminum may be deposited. Then the gate metal material may be chemically mechanically polished, and the gate electrode 1956' defined by masking and etching.

[0284] As illustrated in FIG. 19J, the entire structure may be substantially covered with a Low Temperature Oxide 1952, which may be planarized with chemical mechanical polishing. Contacts and metal interconnects may be formed by lithography and plasma/RIE etch. The n-RCAT N+ source and drain regions 1933, P- transistor channel region 1934, gate dielectric 1912 and gate electrode 1956' are shown. The p-RCAT P+ source and drain regions 1926, N-transistor chan-

nel region **1928**, gate dielectric **1911** and gate electrode **1954'** are shown. Transistor isolation region **1920**, low temperature oxide **1952**, n-RCAT source contact **1962**, gate contact **1964**, and drain contact **1966** are shown. p-RCAT source contact **1972**, gate contact **1974**, and drain contact **1976** are shown. The n-RCAT source contact **1962** and drain contact **1966** provide electrical coupling to their respective N<sup>+</sup> regions **1933**. The n-RCAT gate contact **1964** provides electrical coupling to gate electrode **1956'**. The p-RCAT source contact **1972** and drain contact **1976** provide electrical coupling their respective N<sup>+</sup> region **1926**. The p-RCAT gate contact **1974** provides electrical coupling to gate electrode **1954'**. Contacts (not shown) to P<sup>+</sup> doped region **1916**, and N<sup>-</sup> doped region **1918** may be made to allow biasing for noise suppression and back-gate/substrate biasing.

[**0285**] Interconnect metallization may then be conventionally formed. The thru layer via (not shown) may be formed to electrically couple the complementary RCAT layer metallization to the acceptor wafer **1910** at acceptor wafer metal connect pad (not shown). This flow enables the formation of a mono-crystalline silicon n-RCAT and p-RCAT constructed in a single layer transfer of prefabricated wafer sized doped layers, which may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

[**0286**] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **19A** through **19J** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the n-RCAT may be processed prior to the p-RCAT, or that various etch hard masks may be employed. Such skilled persons will further appreciate that devices other than a complementary RCAT may be created with minor variations of the process flow, such as, for example, complementary bipolar junction transistors, or complementary raised source drain extension transistors, or complementary junction-less transistors, or complementary V-groove transistors. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[**0287**] An alternative process flow to create devices and interconnect to enable building a 3D IC and a 3D IC cell library is illustrated in FIGS. **20A** to **20P**.

[**0288**] As illustrated in FIG. **20A**, a heavily doped N type mono-crystalline acceptor wafer **2010** may be processed to include a wafer sized layer of N<sup>+</sup> doping **2003**. Doped N<sup>+</sup> layer **2003** may be formed by ion implantation and thermal anneal or may alternatively be formed by epitaxially depositing a doped N<sup>+</sup> silicon layer or by a combination of epitaxy and implantation and anneals. A screen oxide layer **2001** may be grown or deposited before the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. Alternatively, a high temperature (greater than approximately 400° C.) resistant metal such as, for example, Tungsten may be added as a low resistance interconnect layer, as a uniform wafer sized sheet layer across the wafer or as a defined geometry metallization, and oxide layer **2001** may be deposited to provide an oxide surface for later wafer to wafer bonding. The doped N<sup>+</sup> layer **2003** or the high temperature resistant metal in the acceptor wafer may function as the ground plane or ground lines for the source connections of the NMOS transistors manufactured in the donor wafer above it.

[**0289**] As illustrated in FIG. **20B**, the top surface of a P-mono-crystalline silicon donor wafer **2000** may be prepared for oxide wafer bonding with a deposition of an oxide **2092** or by thermal oxidation of the P- donor wafer to form oxide layer **2001**. A layer transfer demarcation plane **2099** (shown as a dashed line) may be formed in donor wafer **2000** by hydrogen implantation **2007** or other methods as previously described. Both the donor wafer **2000** and acceptor wafer **2010** may be prepared for wafer bonding as previously described and then bonded. The portion of the P- donor wafer **2000** that is above the layer transfer demarcation plane **2099** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other layer transfer methods.

[**0290**] As illustrated in FIG. **20C**, the remaining P- layer **2000'** and oxide layer **2092** may have been layer transferred to acceptor wafer **2010**. The top surface of P- layer **2000'** may be chemically or mechanically polished smooth and flat and epitaxial (EPI) smoothing techniques may be employed. For illustration clarity, the oxide layers, such as **2001** and **2092**, used to facilitate the wafer to wafer bond, may be combined and shown as oxide layer **2013**.

[**0291**] As illustrated in FIG. **20D** a CMP polish stop layer **2018**, such as, for example, silicon nitride or amorphous carbon, may be deposited after oxide layer **2015**. A contact opening may be lithographically defined and plasma/RIE etched removing regions of P- layer **2000'** and oxide layer **2013** to form the NMOS source to ground contact opening **2006**.

[**0292**] As illustrated in FIG. **20E**, the NMOS source to ground contact opening **2006** may be filled by a deposition of heavily doped polysilicon or amorphous silicon, or a high melting point (greater than approximately 400° C.) metal such as, for example, tungsten, and then chemically mechanically polished to the level of the oxide layer **2015**. This forms the NMOS source to ground contact **2008**. Alternatively, these contacts could be used to connect the drain or source of the NMOS to any signal line in the high temperature resistant metal in the acceptor wafer.

[**0293**] Next, a standard NMOS transistor formation process flow may be performed with two exceptions. First, no lithographic masking steps may be used for an implant step that differentiates NMOS and PMOS devices, as only the NMOS devices may be being formed in this layer. Second, high temperature anneal steps may or may not be done during the NMOS formation, as some or substantially all of the necessary anneals can be done after the PMOS formation described later.

[**0294**] As illustrated in FIG. **20F** a shallow trench oxide region may be lithographically defined and plasma/RIE etched to at least the top level of oxide layer **2013** removing regions of mono-crystalline silicon P- layer **2000'**. A gap-fill oxide may be deposited and CMP'ed flat to form conventional STI oxide isolation region **2040** and P- doped mono-crystalline silicon regions **2020**. Threshold adjust implants may or may not be performed at this time. The silicon surface may be cleaned of remaining oxide with a short HF (Hydrofluoric Acid) etch or other method.

[**0295**] As illustrated in FIG. **20G**, a gate dielectric **2011** may be formed and a gate metal material with proper work function, such as, for example, doped or undoped poly-crystalline silicon, may be deposited. The gate dielectric **2011** may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal in the

industry standard high k metal gate process schemes described previously. Or the gate dielectric **2011** may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate material with proper work function such as, for example, tungsten or aluminum may be deposited. Then the NMOS gate electrodes **2012** and poly on STI interconnect **2014** may be defined by masking and etching. Gate stack self-aligned LDD (Lightly Doped Drain) and halo punch-thru implants may be performed at this time to adjust junction and transistor breakdown characteristics.

**[0296]** As illustrated in FIG. **20H** a conventional spacer deposition of oxide and/or nitride and a subsequent etchback may be done to form NMOS implant offset spacers **2016** on the NMOS gate electrodes **2012** and the poly on STI interconnect **2014**. Then a self-aligned N+ source and drain implant may be performed to create NMOS transistor source and drains **2038** and remaining P- silicon NMOS transistor channels **2030**. High temperature anneal steps may or may not be done at this time to activate the implants and set initial junction depths. A self-aligned silicide may be formed.

**[0297]** As illustrated in FIG. **20I** the entire structure may be substantially covered with a gap fill oxide **2050**, which may be planarized with chemical mechanical polishing. The oxide surface **2051** may be prepared for oxide to oxide wafer bonding as previously described.

**[0298]** Additionally, one or more metal interconnect layers (not shown) with associated contacts and vias (not shown) may be constructed utilizing standard semiconductor manufacturing processes. The metal layer may be constructed at lower temperature using such metals as Copper or Aluminum, or may be constructed with refractory metals such as, for example, Tungsten to provide high temperature utility at greater than approximately 400° C.

**[0299]** As illustrated in FIG. **20J**, an N- mono-crystalline silicon donor wafer **2054** may be prepared for oxide wafer bonding with a deposition of an oxide **2052** or by thermal oxidation of the N- donor wafer to form oxide layer **2052**. A layer transfer demarcation plane **2098** (shown as a dashed line) may be formed in donor wafer **2054** by hydrogen implantation **2007** or other methods as previously described. Both the donor wafer **2054** and the now acceptor wafer **2010** may be prepared for wafer bonding as previously described, and then bonded. To optimize the PMOS mobility, the donor wafer **2054** may be rotated with respect to the acceptor wafer **2010** as part of the bonding process to facilitate creation of the PMOS channel in the <110> silicon plane direction. The portion of the N- donor wafer substrate **2054** that may be above the layer transfer demarcation plane **2098** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other layer transfer methods.

**[0300]** As illustrated in FIG. **20K**, the remaining N- layer **2054'** and oxide layer **2052** may have been layer transferred to acceptor wafer **2010**. Oxide layer **2052** may be bonded to oxide layer **2050**. The top surface of N- layer **2054'** may be chemically or mechanically polished smooth and flat and epitaxial (EPI) smoothing techniques may be employed. For illustration clarity oxide layer **2052** used to facilitate the wafer to wafer bond is not shown in subsequent illustrations.

**[0301]** As illustrated in FIG. **20L** a polishing stop layer **2061**, such as, for example, silicon nitride or amorphous carbon with a protecting oxide layer may be deposited. Then a shallow trench region may be lithographically defined and

plasma/RIE etched to at least the top level of oxide layer **2050** removing regions of N- mono-crystalline silicon layer **2054'**. A gap-fill oxide may be deposited and CMP'ed flat to form conventional STI oxide isolation region **2064** and N- doped mono-crystalline silicon regions **2056**. Transistor threshold adjust implants may or may not be performed at this time. The silicon surface may be cleaned of remaining oxide with a short HF (Hydrofluoric Acid) etch or other method.

**[0302]** As illustrated in FIG. **20M**, a gate oxide **2062** may be formed and a gate metal material with proper work function, such as, for example, doped or undoped poly-crystalline silicon, may be deposited. The gate oxide **2062** may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Or the gate oxide **2062** may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate material with proper work function such as, for example, tungsten or aluminum may be deposited. Then the PMOS gate electrodes **2066** and poly on STI interconnect **2068** may be defined by masking and etching. Gate stack self-aligned LDD (Lightly Doped Drain) and halo punch-thru implants may be performed at this time to adjust junction and transistor breakdown characteristics.

**[0303]** As illustrated in FIG. **20N** a conventional spacer deposition of oxide and/or nitride and a subsequent etchback may be done to form PMOS implant offset spacers **2067** on the PMOS gate electrodes **2066** and the poly on STI interconnect **2068**. Then a self-aligned N+ source and drain implant may be performed to create PMOS transistor source and drains **2057** and remaining N-silicon PMOS transistor channels **2058**. Thermal anneals to activate implants and set junctions in both the PMOS and NMOS devices may be performed with RTA (Rapid Thermal Anneal) or furnace thermal exposures. Alternatively, laser annealing may be utilized to activate implants and set the junctions. Optically absorptive and reflective layers as described previously may be employed to anneal implants and activate junctions. A self-aligned silicide may be formed.

**[0304]** As illustrated in FIG. **20O** the entire structure may be substantially covered with a Low Temperature Oxide **2082**, which may be planarized with chemical mechanical polishing.

**[0305]** Additionally, one or more metal interconnect layers (not shown) with associated contacts and vias (not shown) may be constructed utilizing standard semiconductor manufacturing processes. The metal layer may be constructed at lower temperature using such metals as Copper or Aluminum, or may be constructed with refractory metals such as, for example, Tungsten to provide high temperature utility at greater than approximately 400° C.

**[0306]** As illustrated in FIG. **20P**, contacts and metal interconnects may be formed by lithography and plasma/RIE etch. The N mono-crystalline silicon acceptor wafer **2010**, ground plane N+ layer **2003**, oxide regions **2013**, NMOS source to ground contact **2008**, N+NMOS source and drain regions **2038**, NMOS channel regions **2030**, NMOS STI oxide regions **2040**, NMOS gate dielectric **2011**, NMOS gate electrodes **2012**, NMOS gates over STI **2014**, gap fill oxide **2050**, PMOS STI oxide regions **2064**, P+PMOS source and drain regions **2057**, PMOS channel regions **2058**, PMOS gate dielectric **2062**, PMOS gate electrodes **2066**, PMOS gates over STI **2068**, and gap fill oxide **2082** are shown. Three

groupings of the eight interlayer contacts may be lithographically defined and plasma/RIE etched. First, the contact **2078** to the ground plane N+ layer **2003**, as well as the NMOS drain only contact **2070** and the NMOS only gate on STI contact **2076** may be masked and etched in a first contact step, which may be a deep oxide etch stopping on silicon (**2038** and **2003**) or poly-crystalline silicon **2014**. Then the NMOS & PMOS gate on STI interconnect contact **2072** and the NMOS & PMOS drain contact **2074** may be masked and etched in a second contact step, which may be an oxide/silicon/oxide etch stopping on silicon **2038** and poly-crystalline silicon **2014**. These contacts may make an electrical connection to the sides of silicon **2057** and poly-crystalline silicon **2068**. Then the PMOS gate interconnect on STI contact **2082**, the PMOS only source contact **2084**, and the PMOS only drain contact **2086** may be masked and etched in a third contact step, which may be a shallow oxide etch stopping on silicon **2057** or poly-crystalline silicon **2068**. Alternatively, the shallowest contacts may be masked and etched first, followed by the mid-level, and then the deepest contacts. The metal lines may be mask defined and etched, contacts and metal line filled with barrier metals and copper interconnect, and CMP'ed in a typical Dual Damascene interconnect scheme, thereby substantially completing the eight types of contact connections.

[0307] An illustrated advantage of this 3D cell structure may be the independent formation of the PMOS transistors and the NMOS transistors. Therefore, each transistor formation may be optimized independently. This may be accomplished by the independent selection of the crystal orientation, various stress materials and techniques, such as, for example, doping profiles, material thicknesses and compositions, temperature cycles, and so forth.

[0308] This process flow enables the manufacturing of a 3D IC library of cells that can be created from the devices and interconnect constructed by layer transferring prefabricated wafer sized doped layers. In addition, with reference to the FIG. 2 discussions, these devices and interconnect may be formed and then layer transferred and electrically coupled to an underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

[0309] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 20A through 20P are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the PMOS may be built first and the NMOS stacked on top, or one or more layers of interconnect metallization may be constructed between the NMOS and PMOS transistor layers, or one or more layers interconnect metallization may be constructed on top of the PMOS devices, or more than one NMOS or PMOS device layers may be stacked such that the resulting number of mono-crystalline silicon device layers may be greater than two, backside TSVs may be employed to connect to the ground plane, or devices other than CMOS MOSFETS may be created with minor variations of the process flow, such as, for example, complementary bipolar junction transistors, or complementary raised source drain extension transistors, or complementary junction-less transistors. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0310] 3D memory device structures may also be constructed in layers of mono-crystalline silicon and utilize pre-

processing a donor wafer by forming wafer sized layers of various materials without a process temperature restriction, then layer transferring the pre-processed donor wafer to the acceptor wafer, followed by some processing steps, and repeating this procedure multiple times, and then processing with either low temperature (below approximately 400° C.) or high temperature (greater than approximately 400° C.) after the final layer transfer to form memory device structures, such as, for example, transistors, capacitors, resistors, or memristors, on or in the multiple transferred layers that may be physically aligned and may be electrically coupled to the acceptor wafer.

[0311] Novel monolithic 3D Dynamic Random Access Memories (DRAMs) may be constructed in the above manner. Some embodiments of the invention utilize the floating body DRAM type.

[0312] Further details of a floating body DRAM and its operation modes can be found in U.S. Pat. Nos. 7,541,616, 7,514,748, 7,499,358, 7,499,352, 7,492,632, 7,486,563, 7,477,540, and 7476939. Background information on floating body DRAM and its operation is given in "Floating Body RAM Technology and its Scalability to 32 nm Node and Beyond," *Electron Devices Meeting, 2006. IEDM '06. International*, vol., no., pp. 1-4, 11-13 Dec. 2006 by T. Shino, et. al.; "Overview and future challenges of floating body RAM (FBRAM) technology for 32 nm technology node and beyond", *Solid-State Electronics*, Volume 53, Issue 7; "Papers Selected from the 38th European Solid-State Device Research Conference"—*ESSDERC '08*, July 2009, pages 676-683, ISSN 0038-1101, DOI: 10.1016/j.sse.2009.03.010 by Takeshi Hamamoto, et al.; "New Generation of Z-RAM," *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, vol., no., pp. 925-928, 10-12 Dec. 2007 by Okhonin, S., et al. Prior art for constructing monolithic 3D DRAMs used planar transistors where crystalline silicon layers were formed with either selective epitaxy technology or laser recrystallization. Both selective epitaxy technology and laser recrystallization may not provide perfectly mono-crystalline silicon and often may require a high thermal budget. A description of these processes is given in the book entitled "Integrated Interconnect Technologies for 3D Nanoelectronic Systems" by Bakir and Meindl. The contents of these documents are incorporated in this specification by reference.

[0313] As illustrated in FIG. 21 the fundamentals of operating a floating body DRAM may be described. In order to store a '1' bit, excess holes **2102** may exist in the floating body region **2120** and change the threshold voltage of the memory cell transistor including source **2104**, gate **2106**, drain **2108**, floating body region **2120**, and buried oxide (BOX) **2118**. This is shown in FIG. 21(a). The '0' bit corresponds to no charge being stored in the floating body region **2120** and affects the threshold voltage of the memory cell transistor including source **2110**, gate **2112**, drain **2114**, floating body region **2120**, and buried oxide (BOX) **2116**. This is shown in FIG. 21(b). The difference in threshold voltage between the memory cell transistor depicted in FIG. 21(a) and FIG. 21(b) manifests itself as a change in the drain current **2134** of the transistor at a particular gate voltage **2136**. This is described in FIG. 21(c). This current differential **2130** may be sensed by a sense amplifier circuit to differentiate between '0' and '1' states and thus function as a memory bit.

[0314] As illustrated in FIGS. 22A to 22H, a horizontally-oriented monolithic 3D DRAM that utilizes two masking

steps per memory layer may be constructed that may be suitable for 3D IC manufacturing.

[0315] As illustrated in FIG. 22A, a P- substrate donor wafer 2200 may be processed to include a wafer sized layer of P- doping 2204. The P- layer 2204 may have the same or a different dopant concentration than the P- substrate donor wafer 2200. The P- layer 2204 may be formed by ion implantation and thermal anneal. A screen oxide 2201 may be grown before the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding.

[0316] As illustrated in FIG. 22B, the top surface of donor wafer 2200 may be prepared for oxide to oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the P- layer 2204 to form oxide layer 2202, or a re-oxidation of implant screen oxide 2201. A layer transfer demarcation plane 2299 (shown as a dashed line) may be formed in donor wafer 2200 or P- layer 2204 (shown) by hydrogen implantation 2207 or other methods as previously described. Both the donor wafer 2200 and acceptor wafer 2210 may be prepared for wafer bonding as previously described and then bonded, for example, at a low temperature (less than approximately 400° C.) to minimize stresses. The portion of the P- layer 2204 and the P- substrate donor wafer 2200 that may be above the layer transfer demarcation plane 2299 may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods.

[0317] As illustrated in FIG. 22C, the remaining P- doped layer 2204', and oxide layer 2202 have been layer transferred to acceptor wafer 2210. Acceptor wafer 2210 may include peripheral circuits designed and processed such that the peripheral circuits can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The peripheral circuits may utilize a refractory metal such as, for example, tungsten that can withstand high temperatures greater than approximately 400° C. The top surface of P- doped layer 2204' may be chemically or mechanically polished smooth and flat. Now transistors may be formed and aligned to the acceptor wafer 2210 alignment marks (not shown).

[0318] As illustrated in FIG. 22D shallow trench isolation (STI) oxide regions (not shown) may be lithographically defined and plasma/RIE etched to at least the top level of oxide layer 2202 removing regions of mono-crystalline silicon P- doped layer 2204'. A gap-fill oxide may be deposited and CMP'ed flat to form conventional STI oxide regions and P- doped mono-crystalline silicon regions (not shown) for forming the transistors. Threshold adjust implants may or may not be performed at this time. A gate stack 2224 may be formed with a gate dielectric, such as, for example, thermal oxide, and a gate metal material, such as, for example, polycrystalline silicon. Alternatively, the gate oxide may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Further, the gate oxide may be formed with a rapid thermal oxidation (RTO), a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate material such as, for example, tungsten or aluminum may be deposited. Gate stack self-aligned

LDD (Lightly Doped Drain) and halo punch-thru implants may be performed at this time to adjust junction and transistor breakdown characteristics. A conventional spacer deposition of oxide and/or nitride and a subsequent etchback may be done to form implant offset spacers (not shown) on the gate stacks 2224. Then a self-aligned N+ source and drain implant may be performed to create transistor source and drains 2220 and remaining P- silicon NMOS transistor channels 2228. High temperature anneal steps may or may not be done at this time to activate the implants and set initial junction depths. Finally, the entire structure may be substantially covered with a gap fill oxide 2250, which may be planarized with chemical mechanical polishing. The oxide surface may be prepared for oxide to oxide wafer bonding as previously described.

[0319] As illustrated in FIG. 22E, the transistor layer formation, bonding to acceptor wafer 2210 oxide 2250, and subsequent transistor formation as described in FIGS. 22A to 22D may be repeated to form the second tier 2230 of memory transistors. After substantially all of the desired memory layers are constructed, a rapid thermal anneal (RTA) may be conducted to activate the dopants in substantially all of the memory layers and in the acceptor wafer 2210 peripheral circuits. Alternatively, optical anneals, such as, for example, a laser based anneal, may be performed.

[0320] As illustrated in FIG. 22F, contacts and metal interconnects may be formed by lithography and plasma/RIE etch. Bit line (BL) contacts 2240 electrically couple the memory layers' transistor N+ regions on the transistor drain side 2254, and the source line contact 2242 electrically couples the memory layers' transistor N+ regions on the transistors source side 2252. The bit-line (BL) wiring 2248 and source-line (SL) wiring 2246 electrically couples the bit-line contacts 2240 and source-line contacts 2242 respectively. The gate stacks, such as, for example, 2234, may be connected with a contact and metallization (not shown) to form the word-lines (WLs). A thru layer via (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor wafer 2210 peripheral circuitry via an acceptor wafer metal connect pad (not shown).

[0321] As illustrated in FIG. 22G, a top-view layout a section of the top of the memory array is shown where WL wiring 2264 and SL wiring 2265 may be perpendicular to the BL wiring 2266.

[0322] As illustrated in FIG. 22H, a schematic of each single layer of the DRAM array illustrates the connections for WLs, BLs and SLs at the array level. The multiple layers of the array share BL and SL contacts, but each layer may have its own unique set of WL connections to allow each bit to be accessed independently of the others.

[0323] This flow enables the formation of a horizontally-oriented monolithic 3D DRAM array that utilizes two masking steps per memory layer and may be constructed by layer transfers of wafer sized doped mono-crystalline silicon layers and this 3D DRAM array may be connected to an underlying multi-metal layer semiconductor device, which may or may not contain the peripheral circuits, used to control the DRAM's read and write functions.

[0324] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 22A through 22H are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the transistors may be of another type such as RCATs, or junction-less. Additionally, the contacts may utilize doped poly-crystalline silicon, or other conductive mate-

rials. Moreover, the stacked memory layer may be connected to a periphery circuit that may be above the memory stack. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0325] As illustrated in FIGS. 23A to 23M, a horizontally-oriented monolithic 3D DRAM that utilizes one masking step per memory layer may be constructed that may be suitable for 3D IC.

[0326] As illustrated in FIG. 23A, a silicon substrate with peripheral circuitry 2302 may be constructed with high temperature (greater than approximately 400° C.) resistant wiring, such as, for example, Tungsten. The peripheral circuitry substrate 2302 may include memory control circuits as well as circuitry for other purposes and of various types, such as, for example, analog, digital, radio frequency (RF), or memory. The peripheral circuitry substrate 2302 may include peripheral circuits that can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The top surface of the peripheral circuitry substrate 2302 may be prepared for oxide wafer bonding with a deposition of a silicon oxide layer 2304, thus forming acceptor wafer 2414.

[0327] As illustrated in FIG. 23B, a mono-crystalline silicon donor wafer 2312 may be processed to include a wafer sized layer of P- doping (not shown) which may have a different dopant concentration than the P- substrate 2306. The P- doping layer may be formed by ion implantation and thermal anneal. A screen oxide layer 2308 may be grown or deposited prior to the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. A layer transfer demarcation plane 2310 (shown as a dashed line) may be formed in donor wafer 2312 within the P- substrate 2306 or the P- doping layer (not shown) by hydrogen implantation or other methods as previously described. Both the donor wafer 2312 and acceptor wafer 2314 may be prepared for wafer bonding as previously described and then bonded at the surfaces of oxide layer 2304 and oxide layer 2308, for example, at a low temperature (less than approximately 400° C.) for lowest stresses, or a moderate temperature (less than approximately 900° C.).

[0328] As illustrated in FIG. 23C, the portion of the P- layer (not shown) and the P- substrate 2306 that may be above the layer transfer demarcation plane 2310 may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining mono-crystalline silicon P- layer 2306'. Remaining P- layer 2306' and oxide layer 2308 have been layer transferred to acceptor wafer 2314. The top surface of P- layer 2306' may be chemically or mechanically polished smooth and flat. Now transistors or portions of transistors may be formed and aligned to the acceptor wafer 2314 alignment marks (not shown).

[0329] As illustrated in FIG. 23D, N+ silicon regions 2316 may be lithographically defined and N type species, such as, for example, Arsenic, may be ion implanted into P- layer 2306'. This forms remaining regions of P- silicon 2318. The

N+ silicon regions 2316 may have a doping concentration that may be more than 10x the doping concentration of P- silicon regions 2318.

[0330] As illustrated in FIG. 23E, oxide layer 2320 may be deposited to prepare the surface for later oxide to oxide bonding. This now forms the first Si/SiO<sub>2</sub> layer 2322 which includes silicon oxide layer 2320, N+ silicon regions 2316, and P- silicon regions 2318.

[0331] As illustrated in FIG. 23F, additional Si/SiO<sub>2</sub> layers, such as, for example, second Si/SiO<sub>2</sub> layer 2324 and third Si/SiO<sub>2</sub> layer 2326, may each be formed as described in FIGS. 23A to 23E. Oxide layer 2329 may be deposited. After substantially all of the desired memory layers are constructed, a rapid thermal anneal (RTA) may be conducted to activate the dopants in substantially all of the memory layers 2322, 2324, 2326 and in the peripheral circuitry substrate 2302. Alternatively, optical anneals, such as, for example, a laser based anneal, may be performed.

[0332] As illustrated in FIG. 23G, oxide layer 2329, third Si/SiO<sub>2</sub> layer 2326, second Si/SiO<sub>2</sub> layer 2324 and first Si/SiO<sub>2</sub> layer 2322 may be lithographically defined and plasma/RIE etched to form a portion of the memory cell structure. Regions of P- silicon 2318', which may form the floating body transistor channels, and N+ silicon regions 2316', which may form the source, drain and local source lines, result from the etch.

[0333] As illustrated in FIG. 23H, a gate dielectric and gate electrode material may be deposited, planarized with a chemical mechanical polish (CMP), and then lithographically defined and plasma/RIE etched to form gate dielectric regions 2328 which may be self-aligned to and substantially covered by gate electrodes 2330 (shown), or substantially cover the entire silicon/oxide multi-layer structure. The gate electrode 2330 and gate dielectric 2328 stack may be sized and aligned such that P- silicon regions 2318' may be substantially covered. The gate stack including gate electrode 2330 and gate dielectric 2328 may be formed with a gate dielectric, such as, for example, thermal oxide, and a gate electrode material, such as, for example, polycrystalline silicon. Alternatively, the gate dielectric may be an atomic layer deposited (ALD) material that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Further, the gate dielectric may be formed with a rapid thermal oxidation (RTO), a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode such as, for example, tungsten or aluminum may be deposited.

[0334] As illustrated in FIG. 23I, the entire structure may be substantially covered with a gap fill oxide 2332, which may be planarized with chemical mechanical polishing. The oxide 2332 is shown transparent in the figure for clarity. Word-line regions (WL) 2350, coupled with and composed of gate electrodes 2330, and source-line regions (SL) 2352, composed of indicated N+ silicon regions 2316', are shown.

[0335] As illustrated in FIG. 23J, bit-line (BL) contacts 2334 may be lithographically defined, etched with plasma/RIE, photoresist removed, and then metal, such as, for example, copper, aluminum, or tungsten, may be deposited to fill the contact and etched or polished to the top of oxide 2332. Each BL contact 2334 may be shared among substantially all layers of memory, shown as three layers of memory in FIG. 23J. A thru layer via (not shown) may be formed to electri-

cally couple the BL, SL, and WL metallization to the acceptor wafer **2314** peripheral circuitry via an acceptor wafer metal connect pad (not shown).

[0336] As illustrated in FIG. **23K**, BL metal lines **2336** may be formed and connect to the associated BL contacts **2334**. Contacts and associated metal interconnect lines (not shown) may be formed for the WL and SL at the memory array edges. SL contacts can be made into stair-like structures using techniques described in "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory," VLSI Technology, 2007 IEEE Symposium on, vol., no., pp. 14-15, 12-14 Jun. 2007 by Tanaka, H.; Kido, M.; Yahashi, K.; Oomura, M.; et al.

[0337] As illustrated in FIGS. **23L**, **23L1** and **23L2**, cross section cut II of FIG. **23L** is shown in FIG. **23L1**, and cross section cut III of FIG. **23L** is shown in FIG. **23L2**. BL metal line **2336**, oxide **2332**, BL contact **2334**, WL regions **2350**, gate dielectric **2328**, P- silicon regions **2318'**, and peripheral circuitry substrate **2302** are shown in FIG. **23L1**. The BL contact **2334** may connect to one side of the three levels of floating body transistors that may include two N+ silicon regions **2316'** in each level with their associated P- silicon region **2318'**. BL metal lines **2336**, oxide **2332**, gate electrode **2330**, gate dielectric **2328**, P- silicon regions **2318'**, inter-layer oxide region ('ox'), and peripheral circuitry substrate **2302** are shown in FIG. **23L2**. The gate electrode **2330** may be common to substantially all six P- silicon regions **2318'** and forms six two-sided gated floating body transistors.

[0338] As illustrated in FIG. **23M**, a single exemplary floating body transistor with two gates on the first Si/SiO<sub>2</sub> layer **2322** may include P- silicon region **2318'** (functioning as the floating body transistor channel), N+ silicon regions **2316'** (functioning as source and drain), and two gate electrodes **2330** with associated gate dielectrics **2328**. The transistor may be electrically isolated from beneath by oxide layer **2308**.

[0339] This flow enables the formation of a horizontally-oriented monolithic 3D DRAM that utilizes one masking step per memory layer constructed by layer transfers of wafer sized doped mono-crystalline silicon layers and this 3D DRAM may be connected to an underlying multi-metal layer semiconductor device.

[0340] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **23A** through **23M** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the transistors may be of another type such as RCATs, or junction-less. Additionally, the contacts may utilize doped poly-crystalline silicon, or other conductive materials. Moreover, the stacked memory layers may be connected to a periphery circuit that may be above the memory stack. Further, the Si/SiO<sub>2</sub> layers **2322**, **2324** and **2326** may be annealed layer-by-layer after their associated implantations by using a laser anneal system. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0341] As illustrated in FIGS. **24A** to **24L**, a horizontally-oriented monolithic 3D DRAM that utilizes zero additional masking steps per memory layer by sharing mask steps after substantially all the layers have been transferred may be constructed that may be suitable for 3D IC manufacturing.

[0342] As illustrated in FIG. **24A**, a silicon substrate with peripheral circuitry **2402** may be constructed with high tem-

perature (greater than approximately 400° C.) resistant wiring, such as, for example, Tungsten. The peripheral circuitry substrate **2402** may include memory control circuits as well as circuitry for other purposes and of various types, such as, for example, analog, digital, RF, or memory. The peripheral circuitry substrate **2402** may include peripheral circuits that can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The top surface of the peripheral circuitry substrate **2402** may be prepared for oxide wafer bonding with a deposition of a silicon oxide layer **2404**, thus forming acceptor wafer **2414**.

[0343] As illustrated in FIG. **24B**, a mono-crystalline silicon donor wafer **2412** may be processed to include a wafer sized layer of P- doping (not shown) which may have a different dopant concentration than the P- substrate **2406**. The P- doping layer may be formed by ion implantation and thermal anneal. A screen oxide layer **2408** may be grown or deposited prior to the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. A layer transfer demarcation plane **2410** (shown as a dashed line) may be formed in donor wafer **2412** within the P- substrate **2406** or the P- doping layer (not shown) by hydrogen implantation or other methods as previously described. Both the donor wafer **2412** and acceptor wafer **2414** may be prepared for wafer bonding as previously described and then bonded at the surfaces of oxide layer **2404** and oxide layer **2408**, for example, at a low temperature (less than approximately 400° C.) for lowest stresses, or a moderate temperature (less than approximately 900° C.).

[0344] As illustrated in FIG. **24C**, the portion of the P- layer (not shown) and the P- substrate **2406** that may be above the layer transfer demarcation plane **2410** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining mono-crystalline silicon P- layer **2406'**. Remaining P- layer **2406'** and oxide layer **2408** have been layer transferred to acceptor wafer **2414**. The top surface of P- layer **2406'** may be chemically or mechanically polished smooth and flat. Now transistors or portions of transistors may be formed and aligned to the acceptor wafer **2414** alignment marks (not shown). Oxide layer **2420** may be deposited to prepare the surface for later oxide to oxide bonding. This now forms the first Si/SiO<sub>2</sub> layer **2423** which includes silicon oxide layer **2420**, P-layer **2406'**, and oxide layer **2408**.

[0345] As illustrated in FIG. **24D**, additional Si/SiO<sub>2</sub> layers, such as, for example, second Si/SiO<sub>2</sub> layer **2425** and third Si/SiO<sub>2</sub> layer **2427**, may each be formed as described in FIGS. **24A** to **24C**. Oxide layer **2429** may be deposited to electrically isolate the top silicon layer.

[0346] As illustrated in FIG. **24E**, oxide layer **2429**, third Si/SiO<sub>2</sub> layer **2427**, second Si/SiO<sub>2</sub> layer **2425** and first Si/SiO<sub>2</sub> layer **2423** may be lithographically defined and plasma/RIE etched to form a portion of the memory cell structure, which may include regions of P- silicon **2416** and oxide **2422**.

[0347] As illustrated in FIG. **24F**, a gate dielectric and gate electrode material may be deposited, planarized with a chemical mechanical polish (CMP), and then lithographi-



cally defined and plasma/RIE etched to form gate dielectric regions **2428** which may either be self-aligned to and substantially covered by gate electrodes **2430** (shown), or substantially cover the entire silicon/oxide multi-layer structure. The gate stack including gate electrode **2430** and gate dielectric regions **2428** may be formed with a gate dielectric, such as, for example, thermal oxide, and a gate electrode material, such as, for example, poly-crystalline silicon. Alternatively, the gate dielectric may be an atomic layer deposited (ALD) material that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Further, the gate dielectric may be formed with a rapid thermal oxidation (RTO), a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode such as, for example, tungsten or aluminum may be deposited.

**[0348]** As illustrated in FIG. **24G**, N+ silicon regions **2426** may be formed in a self-aligned manner to the gate electrodes **2430** by ion implantation of an N type species, such as, for example, Arsenic, into the portions of P- silicon regions **2416** that may not be blocked by the gate electrodes **2430**. This forms remaining regions of P- silicon **2417** (not shown) in the gate electrode **2430** blocked areas. Different implant energies or angles, or multiples of each, may be utilized to place the N type species into each layer of P- silicon regions **2416**. Spacers (not shown) may be utilized during this multi-step implantation process and layers of silicon present in different layers of the stack may have different spacer widths to account for the differing lateral straggle of N type species implants. Bottom layers, such as, for example, first Si/SiO<sub>2</sub> layer **2423**, could have larger spacer widths than top layers, such as, for example, third Si/SiO<sub>2</sub> layer **2427**. Alternatively, angular ion implantation with substrate rotation may be utilized to compensate for the differing implant straggle. The top layer implantation may have a steeper angle than perpendicular to the wafer surface and hence land ions slightly underneath the gate electrode **2430** edges and closely match a more perpendicular lower layer implantation which may land ions slightly underneath the gate electrode **2430** edge as a result of the straggle effects of the greater implant energy necessary to reach the lower layer. A rapid thermal anneal (RTA) may be conducted to activate the dopants in substantially all of the memory layers **2423**, **2425**, **2427** and in the peripheral circuitry substrate **2402**. Alternatively, optical anneals, such as, for example, a laser based anneal, may be performed.

**[0349]** As illustrated in FIG. **24H**, the entire structure may be substantially covered with a gap fill oxide **2432**, which be planarized with chemical mechanical polishing. The oxide **2432** is shown transparent in the figure for clarity. Word-line regions (WL) **2450**, coupled with and composed of gate electrodes **2430**, and source-line regions (SL) **2452**, composed of indicated N+ silicon regions **2426**, are shown.

**[0350]** As illustrated in FIG. **24I**, bit-line (BL) contacts **2434** may be lithographically defined, etched with plasma/RIE, photoresist removed, and then metal, such as, for example, copper, aluminum, or tungsten, may be deposited to fill the contact and etched or polished to the top of oxide **2432**. Each BL contact **2434** may be shared among substantially all layers of memory, shown as three layers of memory in FIG. **24I**. A thru layer via (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor wafer **2414** peripheral circuitry via an acceptor wafer metal connect pad (not shown).

**[0351]** As illustrated in FIG. **24J**, BL metal lines **2436** may be formed and connect to the associated BL contacts **2434**. Contacts and associated metal interconnect lines (not shown) may be formed for the WL and SL at the memory array edges.

**[0352]** As illustrated in FIGS. **24K**, **24K1** and **24K2**, cross section cut II of FIG. **24K** is shown in FIG. **24K1**, and cross section cut III of FIG. **24K** is shown in FIG. **24K2**. BL metal lines **2436**, oxide **2432**, BL contact **2434**, WL regions **2450**, gate dielectric regions **2428**, N+ silicon regions **2426**, P- silicon regions **2417**, and peripheral circuitry substrate **2402** are shown in FIG. **24K1**. The BL contact **2434** couples to one side of the three levels of floating body transistors that may include two N+ silicon regions **2426** in each level with their associated P- silicon region **2417**. BL metal lines **2436**, oxide **2432**, gate electrode **2430**, gate dielectric regions **2428**, P- silicon regions **2417**, interlayer oxide region ('ox'), and peripheral circuitry substrate **2402** are shown in FIG. **24K2**. The gate electrode **2430** may be common to substantially all six P- silicon regions **2417** and forms six two-sided gated floating body transistors.

**[0353]** As illustrated in FIG. **24L**, a single exemplary floating body two gate transistor on the first Si/SiO<sub>2</sub> layer **2423** may include P- silicon region **2417** (functioning as the floating body transistor channel), N+ silicon regions **2426** (functioning as source and drain), and two gate electrodes **2430** with associated gate dielectric regions **2428**. The transistor may be electrically isolated from beneath by oxide layer **2408**.

**[0354]** This flow enables the formation of a horizontally-oriented monolithic 3D DRAM that utilizes zero additional masking steps per memory layer and may be constructed by layer transfers of wafer sized doped mono-crystalline silicon layers and may be connected to an underlying multi-metal layer semiconductor device.

**[0355]** Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **24A** through **24L** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the transistors may be of another type such as RCATs, or junction-less. Additionally, the contacts may utilize doped poly-crystalline silicon, or other conductive materials. Moreover, the stacked memory layer may be connected to a periphery circuit that may be above the memory stack. Further, each gate of the double gate 3D DRAM can be independently controlled for increased control of the memory cell. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

**[0356]** Novel monolithic 3D memory technologies utilizing material resistance changes may be constructed in a similar manner. There are many types of resistance-based memories including phase change memory, Metal Oxide memory, resistive RAM (RRAM), memristors, solid-electrolyte memory, ferroelectric RAM, and MRAM. Background information on these resistive-memory types is given in "Overview of candidate device technologies for storage-class memory," *IBM Journal of Research and Development*, vol. 52, no. 4.5, pp. 449-464, July 2008 by Burr, G. W., et al. The contents of this document are incorporated in this specification by reference.

**[0357]** As illustrated in FIGS. **25A** to **25K**, a resistance-based zero additional masking steps per memory layer 3D memory may be constructed that may be suitable for 3D IC

manufacturing. This 3D memory utilizes junction-less transistors and may have a resistance-based memory element in series with a select or access transistor.

**[0358]** As illustrated in FIG. 25A, a silicon substrate with peripheral circuitry **2502** may be constructed with high temperature (greater than approximately 400° C.) resistant wiring, such as, for example, Tungsten. The peripheral circuitry substrate **2502** may include memory control circuits as well as circuitry for other purposes and of various types, such as, for example, analog, digital, RF, or memory. The peripheral circuitry substrate **2502** may include peripheral circuits that can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The top surface of the peripheral circuitry substrate **2502** may be prepared for oxide wafer bonding with a deposition of a silicon oxide layer **2504**, thus forming acceptor wafer **2514**.

**[0359]** As illustrated in FIG. 25B, a mono-crystalline silicon donor wafer **2512** may be processed to include a wafer sized layer of N+ doping (not shown) which may have a different dopant concentration than the N+ substrate **2506**. The N+ doping layer may be formed by ion implantation and thermal anneal. A screen oxide layer **2508** may be grown or deposited prior to the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. A layer transfer demarcation plane **2510** (shown as a dashed line) may be formed in donor wafer **2512** within the N+ substrate **2506** or the N+ doping layer (not shown) by hydrogen implantation or other methods as previously described. Both the donor wafer **2512** and acceptor wafer **2514** may be prepared for wafer bonding as previously described and then bonded at the surfaces of oxide layer **2504** and oxide layer **2508**, for example, at a low temperature (less than approximately 400° C.) for lowest stresses, or a moderate temperature (less than approximately 900° C.).

**[0360]** As illustrated in FIG. 25C, the portion of the N+ layer (not shown) and the N+ wafer substrate **2506** that may be above the layer transfer demarcation plane **2510** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining mono-crystalline silicon N+ layer **2506'**. Remaining N+ layer **2506'** and oxide layer **2508** have been layer transferred to acceptor wafer **2514**. The top surface of N+ layer **2506'** may be chemically or mechanically polished smooth and flat. Now transistors or portions of transistors may be formed and aligned to the acceptor wafer **2514** alignment marks (not shown). Oxide layer **2520** may be deposited to prepare the surface for later oxide to oxide bonding. This now forms the first Si/SiO<sub>2</sub> layer **2523** which includes silicon oxide layer **2520**, N+ silicon layer **2506'**, and oxide layer **2508**.

**[0361]** As illustrated in FIG. 25D, additional Si/SiO<sub>2</sub> layers, such as, for example, second Si/SiO<sub>2</sub> layer **2525** and third Si/SiO<sub>2</sub> layer **2527**, may each be formed as described in FIGS. 25A to 25C. Oxide layer **2529** may be deposited to electrically isolate the top N+ silicon layer.

**[0362]** As illustrated in FIG. 25E, oxide layer **2529**, third Si/SiO<sub>2</sub> layer **2527**, second Si/SiO<sub>2</sub> layer **2525** and first Si/SiO<sub>2</sub> layer **2523** may be lithographically defined and

plasma/RIE etched to form a portion of the memory cell structure, which now includes regions of N+ silicon **2526** and oxide **2522**.

**[0363]** As illustrated in FIG. 25F, a gate dielectric and gate electrode material may be deposited, planarized with a chemical mechanical polish (CMP), and then lithographically defined and plasma/RIE etched to form gate dielectric regions **2528** which may either be self-aligned to and substantially covered by gate electrodes **2530** (shown), or substantially cover the entire N+ silicon **2526** and oxide **2522** multi-layer structure. The gate stack including gate electrodes **2530** and gate dielectric regions **2528** may be formed with a gate dielectric, such as, for example, thermal oxide, and a gate electrode material, such as, for example, poly-crystalline silicon. Alternatively, the gate dielectric may be an atomic layer deposited (ALD) material that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Further, the gate dielectric may be formed with a rapid thermal oxidation (RTO), a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode such as, for example, tungsten or aluminum may be deposited.

**[0364]** As illustrated in FIG. 25G, the entire structure may be substantially covered with a gap fill oxide **2532**, which may be planarized with chemical mechanical polishing. The oxide **2532** is shown transparent in the figure for clarity. Word-line regions (WL) **2550**, coupled with and composed of gate electrodes **2530**, and source-line regions (SL) **2552**, composed of N+ silicon regions **2526**, are shown.

**[0365]** As illustrated in FIG. 25H, bit-line (BL) contacts **2534** may be lithographically defined, etched with plasma/RIE through oxide **2532**, the three N+ silicon regions **2526**, and associated oxide vertical isolation regions to connect substantially all memory layers vertically, and photoresist removed. Resistance change material **2538**, such as, for example, hafnium oxide, may then be deposited, for example, with atomic layer deposition (ALD). The electrode for the resistance change memory element may then be deposited by ALD to form the electrode/BL contact **2534**. The excess deposited material may be polished to planarity at or below the top of oxide **2532**. Each BL contact **2534** with resistive change material **2538** may be shared among substantially all layers of memory, shown as three layers of memory in FIG. 25H.

**[0366]** As illustrated in FIG. 25I, BL metal lines **2536** may be formed and connect to the associated BL contacts **2534** with resistive change material **2538**. Contacts and associated metal interconnect lines (not shown) may be formed for the WL and SL at the memory array edges. A thru layer via (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor wafer **2514** peripheral circuitry via an acceptor wafer metal connect pad (not shown).

**[0367]** As illustrated in FIGS. 25J, **25J1** and **25J2**, cross section cut II of FIG. 25J is shown in FIG. 25J1, and cross section cut III of FIG. 25J is shown in FIG. 25J2. BL metal lines **2536**, oxide **2532**, BL contact/electrode **2534**, resistive change material **2538**, WL regions **2550**, gate dielectric regions **2528**, N+ silicon regions **2526**, and peripheral circuitry substrate **2502** are shown in FIG. 25J1. The BL contact/electrode **2534** couples to one side of the three levels of resistive change material **2538**. The other side of the resistive change material **2538** may be coupled to N+ regions **2526**. BL metal lines **2536**, oxide **2532**, gate electrodes **2530**, gate

dielectric regions **2528**, N+ silicon regions **2526**, interlayer oxide region ('ox'), and peripheral circuitry substrate **2502** are shown in FIG. **25J2**. The gate electrode **2530** may be common to substantially all six N+ silicon regions **2526** and forms six two-sided gated junction-less transistors as memory select transistors.

[**0368**] As illustrated in FIG. **25K**, a single exemplary two-sided gated junction-less transistor on the first Si/SiO<sub>2</sub> layer **2523** may include N+ silicon region **2526** (functioning as the source, drain, and transistor channel), and two gate electrodes **2530** with associated gate dielectric regions **2528**. The transistor may be electrically isolated from beneath by oxide layer **2508**.

[**0369**] This flow enables the formation of a resistance-based multi-layer or 3D memory array with zero additional masking steps per memory layer, which utilizes junction-less transistors and may have a resistance-based memory element in series with a select transistor, and may be constructed by layer transfers of wafer sized doped mono-crystalline silicon layers, and this 3D memory array may be connected to an underlying multi-metal layer semiconductor device.

[**0370**] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **25A** through **25K** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the transistors may be of another type such as RCATs. Additionally, doping of each N+ layer may be slightly different to compensate for interconnect resistances. Moreover, the stacked memory layer may be connected to a periphery circuit that may be above the memory stack. Further, each gate of the double gate 3D resistance based memory can be independently controlled for increased control of the memory cell. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[**0371**] As illustrated in FIGS. **26A** to **26L**, a resistance-based 3D memory may be constructed with zero additional masking steps per memory layer, which may be suitable for 3D IC manufacturing. This 3D memory utilizes double gated MOSFET transistors and may have a resistance-based memory element in series with a select transistor.

[**0372**] As illustrated in FIG. **26A**, a silicon substrate with peripheral circuitry **2602** may be constructed with high temperature (greater than approximately 400° C.) resistant wiring, such as, for example, Tungsten. The peripheral circuitry substrate **2602** may include memory control circuits as well as circuitry for other purposes and of various types, such as, for example, analog, digital, RF, or memory. The peripheral circuitry substrate **2602** may include peripheral circuits that can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The top surface of the peripheral circuitry substrate **2602** may be prepared for oxide wafer bonding with a deposition of a silicon oxide layer **2604**, thus forming acceptor wafer **2614**.

[**0373**] As illustrated in FIG. **26B**, a mono-crystalline silicon donor wafer **2612** may be processed to include a wafer sized layer of P- doping (not shown) which may have a different dopant concentration than the P- substrate **2606**. The P- doping layer may be formed by ion implantation and

thermal anneal. A screen oxide layer **2608** may be grown or deposited prior to the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. A layer transfer demarcation plane **2610** (shown as a dashed line) may be formed in donor wafer **2612** within the P- substrate **2606** or the P- doping layer (not shown) by hydrogen implantation or other methods as previously described. Both the donor wafer **2612** and acceptor wafer **2614** may be prepared for wafer bonding as previously described and then bonded at the surfaces of oxide layer **2604** and oxide layer **2608**, for example, at a low temperature (less than approximately 400° C.) for lowest stresses, or a moderate temperature (less than approximately 900° C.).

[**0374**] As illustrated in FIG. **26C**, the portion of the P- layer (not shown) and the P- substrate **2606** that may be above the layer transfer demarcation plane **2610** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining mono-crystalline silicon P- layer **2606'**. Remaining P- layer **2606'** and oxide layer **2608** have been layer transferred to acceptor wafer **2614**. The top surface of P- layer **2606'** may be chemically or mechanically polished smooth and flat. Now transistors or portions of transistors may be formed and aligned to the acceptor wafer **2614** alignment marks (not shown). Oxide layer **2620** may be deposited to prepare the surface for later oxide to oxide bonding. This now forms the first Si/SiO<sub>2</sub> layer **2623** which includes silicon oxide layer **2620**, P-layer **2606'**, and oxide layer **2608**.

[**0375**] As illustrated in FIG. **26D**, additional Si/SiO<sub>2</sub> layers, such as, for example, second Si/SiO<sub>2</sub> layer **2625** and third Si/SiO<sub>2</sub> layer **2627**, may each be formed as described in FIGS. **26A** to **26C**. Oxide layer **2629** may be deposited to electrically isolate the top silicon layer.

[**0376**] As illustrated in FIG. **26E**, oxide layer **2629**, third Si/SiO<sub>2</sub> layer **2627**, second Si/SiO<sub>2</sub> layer **2625** and first Si/SiO<sub>2</sub> layer **2623** may be lithographically defined and plasma/RIE etched to form a portion of the memory cell structure, which now includes P- silicon regions **2616** and oxide **2622**.

[**0377**] As illustrated in FIG. **26F**, a gate dielectric and gate electrode material may be deposited, planarized with a chemical mechanical polish (CMP), and then lithographically defined and plasma/RIE etched to form gate dielectric regions **2628** which may either be self-aligned to and substantially covered by gate electrodes **2630** (shown), or may substantially cover the entire silicon/oxide multi-layer structure. The gate stack including gate electrodes **2630** and gate dielectric regions **2628** may be formed with a gate dielectric, such as, for example, thermal oxide, and a gate electrode material, such as, for example, polycrystalline silicon. Alternatively, the gate dielectric may be an atomic layer deposited (ALD) material that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Further, the gate dielectric may be formed with a rapid thermal oxidation (RTO), a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode such as, for example, tungsten or aluminum may be deposited.

[**0378**] As illustrated in FIG. **26G**, N+ silicon regions **2626** may be formed in a self-aligned manner to the gate electrodes **2630** by ion implantation of an N type species, such as, for

example, Arsenic, into the P- silicon regions 2616 that may not be blocked by the gate electrodes 2630. This may form remaining regions of P- silicon 2617 (not shown) in the gate electrode 2630 blocked areas. Different implant energies or angles, or multiples of each, may be utilized to place the N type species into each layer of P- silicon regions 2616. Spacers (not shown) may be utilized during this multi-step implantation process and layers of silicon present in different layers of the stack may have different spacer widths to account for the differing lateral straggle of N type species implants. Bottom layers, such as, for example, first Si/SiO<sub>2</sub> layer 2623, could have larger spacer widths than top layers, such as, for example, third Si/SiO<sub>2</sub> layer 2627. Alternatively, angular ion implantation with substrate rotation may be utilized to compensate for the differing implant straggle. The top layer implantation may have a steeper angle than perpendicular to the wafer surface and hence land ions slightly underneath the gate electrode 2630 edges and closely match a more perpendicular lower layer implantation which may land ions slightly underneath the gate electrode 2630 edge as a result of the straggle effects of the greater implant energy necessary to reach the lower layer. A rapid thermal anneal (RTA) may be conducted to activate the dopants in substantially all of the memory layers 2623, 2625, 2627 and in the peripheral circuitry substrate 2602. Alternatively, optical anneals, such as, for example, a laser based anneal, may be performed.

[0379] As illustrated in FIG. 26H, the entire structure may be substantially covered with a gap fill oxide 2632, which may be planarized with chemical mechanical polishing. The oxide 2632 is shown transparent in the figure for clarity. Word-line regions (WL) 2650, coupled with and composed of gate electrodes 2630, and source-line regions (SL) 2652, composed of indicated N+ silicon regions 2626, are shown.

[0380] As illustrated in FIG. 26I, bit-line (BL) contacts 2634 may be lithographically defined, etched with plasma/RIE through oxide 2632, the three N+ silicon regions 2626, and associated oxide vertical isolation regions to connect substantially all memory layers vertically, and photoresist removed. Resistance change material 2638, such as, for example, hafnium oxide, may then be deposited, for example, with atomic layer deposition (ALD). The electrode for the resistance change memory element may then be deposited by ALD to form the electrode/BL contact 2634. The excess deposited material may be polished to planarity at or below the top of oxide 2632. Each BL contact 2634 with resistive change material 2638 may be shared among substantially all layers of memory, shown as three layers of memory in FIG. 26I.

[0381] As illustrated in FIG. 26J, BL metal lines 2636 may be formed and connect to the associated BL contacts 2634 with resistive change material 2638. Contacts and associated metal interconnect lines (not shown) may be formed for the WL and SL at the memory array edges. A thru layer via (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor wafer 2614 peripheral circuitry via an acceptor wafer metal connect pad (not shown).

[0382] As illustrated in FIGS. 26K, 26K1 and 26K2, cross section cut II of FIG. 26K is shown in FIG. 26K1, and cross section cut III of FIG. 26K is shown in FIG. 26K2. BL metal lines 2636, oxide 2632, BL contact/electrode 2634, resistive change material 2638, WL regions 2650, gate dielectric regions 2628, P- silicon regions 2617, N+ silicon regions 2626, and peripheral circuitry substrate 2602 are shown in FIG. 26K1. The BL contact/electrode 2634 couples to one

side of the three levels of resistive change material 2638. The other side of the resistive change material 2638 may be coupled to N+ silicon regions 2626. The P- silicon regions 2617 with associated N+ regions 2626 on each side form the source, channel, and drain of the select transistor. BL metal lines 2636, oxide 2632, gate electrode 2630, gate dielectric regions 2628, P- silicon regions 2617, interlayer oxide regions ('ox'), and peripheral circuitry substrate 2602 are shown in FIG. 26K2. The gate electrode 2630 may be common to substantially all six P- silicon regions 2617 and controls the six double gated MOSFET select transistors.

[0383] As illustrated in FIG. 26L, a single exemplary double gated MOSFET select transistor on the first Si/SiO<sub>2</sub> layer 2623 may include P- silicon region 2617 (functioning as the transistor channel), N+ silicon regions 2626 (functioning as source and drain), and two gate electrodes 2630 with associated gate dielectric regions 2628. The transistor may be electrically isolated from beneath by oxide layer 2608.

[0384] The above flow enables the formation of a resistance-based 3D memory with zero additional masking steps per memory layer constructed by layer transfers of wafer sized doped mono-crystalline silicon layers and may be connected to an underlying multi-metal layer semiconductor device.

[0385] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 26A through 26L are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the transistors may be of another type such as RCATs. The MOSFET selectors may utilize lightly doped drain and halo implants for channel engineering. Additionally, the contacts may utilize doped poly-crystalline silicon, or other conductive materials. Moreover, the stacked memory layer may be connected to a periphery circuit that may be above the memory stack. Further, each gate of the double gate 3D DRAM can be independently controlled for increased control of the memory cell. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0386] As illustrated in FIGS. 27A to 27M, a resistance-based 3D memory with one additional masking step per memory layer may be constructed that may be suitable for 3D IC manufacturing. This 3D memory utilizes double gated MOSFET select transistors and may have a resistance-based memory element in series with the select transistor.

[0387] As illustrated in FIG. 27A, a silicon substrate with peripheral circuitry 2702 may be constructed with high temperature (greater than approximately 400° C.) resistant wiring, such as, for example, Tungsten. The peripheral circuitry substrate 2702 may include memory control circuits as well as circuitry for other purposes and of various types, such as, for example, analog, digital, RF, or memory. The peripheral circuitry substrate 2702 may include circuits that can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The top surface of the peripheral circuitry substrate 2702 may be prepared for oxide wafer bonding with a deposition of a silicon oxide layer 2704, thus forming acceptor wafer 2414.

[0388] As illustrated in FIG. 27B, a mono-crystalline silicon donor wafer 2712 may be processed to include a wafer sized layer of P- doping (not shown) which may have a different dopant concentration than the P- substrate 2706. The P- doping layer may be formed by ion implantation and thermal anneal. A screen oxide layer 2708 may be grown or deposited prior to the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. A layer transfer demarcation plane 2710 (shown as a dashed line) may be formed in donor wafer 2712 within the P- substrate 2706 or the P- doping layer (not shown) by hydrogen implantation or other methods as previously described. Both the donor wafer 2712 and acceptor wafer 2714 may be prepared for wafer bonding as previously described and then bonded at the surfaces of oxide layer 2704 and oxide layer 2708, for example, at a low temperature (less than approximately 400° C.) for lowest stresses, or a moderate temperature (less than approximately 900° C.).

[0389] As illustrated in FIG. 27C, the portion of the P- layer (not shown) and the P- substrate 2706 that may be above the layer transfer demarcation plane 2710 may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining mono-crystalline silicon P- layer 2706'. Remaining P- layer 2706' and oxide layer 2708 have been layer transferred to acceptor wafer 2714. The top surface of P- layer 2706' may be chemically or mechanically polished smooth and flat. Now transistors or portions of transistors may be formed and aligned to the acceptor wafer 2714 alignment marks (not shown).

[0390] As illustrated in FIG. 27D, N+ silicon regions 2716 may be lithographically defined and N type species, such as, for example, Arsenic, may be ion implanted into P- layer 2706'. This forms remaining regions of P- silicon regions 2718. The N+ silicon regions 2716 may have a doping concentration that may be more than 10× the doping concentration of P- silicon regions 2718.

[0391] As illustrated in FIG. 27E, oxide layer 2720 may be deposited to prepare the surface for later oxide to oxide bonding. This now forms the first Si/SiO<sub>2</sub> layer 2723 which includes silicon oxide layer 2720, N+ silicon regions 2716, and P- silicon regions 2718.

[0392] As illustrated in FIG. 27F, additional Si/SiO<sub>2</sub> layers, such as, for example, second Si/SiO<sub>2</sub> layer 2725 and third Si/SiO<sub>2</sub> layer 2727, may each be formed as described in FIGS. 27A to 27E. Oxide layer 2729 may be deposited. After substantially all the desired numbers of memory layers are constructed, a rapid thermal anneal (RTA) may be conducted to activate the dopants in substantially all of the memory layers 2723, 2725, 2727 and in the peripheral circuitry substrate 2702. Alternatively, optical anneals, such as, for example, a laser based anneal, may be performed.

[0393] As illustrated in FIG. 27G, oxide layer 2729, third Si/SiO<sub>2</sub> layer 2727 second Si/SiO<sub>2</sub> layer 2725 and first Si/SiO<sub>2</sub> layer 2723 may be lithographically defined and plasma/RIE etched to form a portion of the memory cell structure. P- regions 2718', which may form the transistor channels, and N+ silicon regions 2716', which form the source, drain and local source lines, may result from the etch, as well as oxide regions 2722.

[0394] As illustrated in FIG. 27H, a gate dielectric and gate electrode material may be deposited, planarized with a chemical mechanical polish (CMP), and then lithographi-

cally defined and plasma/RIE etched to form gate dielectric regions 2728 which may be either self-aligned to and substantially covered by gate electrodes 2730 (shown), or substantially cover the entire silicon/oxide multi-layer structure. The gate electrodes 2730 and gate dielectric regions 2728 stack may be sized and aligned such that P- regions 2718' may be substantially covered. The gate stack including gate electrodes 2730 and gate dielectric regions 2728 may be formed with a gate dielectric, such as, for example, thermal oxide, and a gate electrode material, such as, for example, poly-crystalline silicon. Alternatively, the gate dielectric may be an atomic layer deposited (ALD) material that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Further, the gate dielectric may be formed with a rapid thermal oxidation (RTO), a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode such as, for example, tungsten or aluminum may be deposited.

[0395] As illustrated in FIG. 27I, the entire structure may be substantially covered with a gap fill oxide 2732, which may be planarized with chemical mechanical polishing. The oxide 2732 is shown transparent in the figure for clarity. Word-line regions (WL) 2750, coupled with and composed of gate electrodes 2730, and source-line regions (SL) 2752, composed of indicated N+ silicon regions 2716', are shown.

[0396] As illustrated in FIG. 27J, bit-line (BL) contacts 2734 may be lithographically defined, etched with plasma/RIE through oxide 2732, the three N+ silicon regions 2716', and associated oxide vertical isolation regions to connect substantially all memory layers vertically, and photoresist removed. Resistance change material 2738, such as, for example, hafnium oxide, may then be deposited, for example, with atomic layer deposition (ALD). The electrode for the resistance change memory element may then be deposited by ALD to form the BL contact/electrode 2734. The excess deposited material may be polished to planarity at or below the top of oxide 2732. Each BL contact/electrode 2734 with resistive change material 2738 may be shared among substantially all layers of memory, shown as three layers of memory in FIG. 27J.

[0397] As illustrated in FIG. 27K, BL metal lines 2736 may be formed and connect to the associated BL contacts 2734 with resistive change material 2738. Contacts and associated metal interconnect lines (not shown) may be formed for the WL and SL at the memory array edges. A thru layer via (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor wafer 2714 peripheral circuitry via an acceptor wafer metal connect pad (not shown).

[0398] As illustrated in FIGS. 27L, 27L1 and 27L2, cross section cut II of FIG. 27L is shown in FIG. 27L1, and cross section cut III of FIG. 27L is shown in FIG. 27L2. BL metal lines 2736, oxide 2732, BL contact/electrode 2734, resistive change material 2738, WL regions 2750, gate dielectric regions 2728, P- regions 2718', N+ silicon regions 2716', and peripheral circuitry substrate 2702 are shown in FIG. 27L1. The BL contact/electrode 2734 couples to one side of the three levels of resistive change material 2738. The other side of the resistive change material 2738 may be coupled to N+ silicon regions 2726. The P- regions 2718' with associated N+ regions 2716' on each side form the source, channel, and drain of the select transistor. BL metal lines 2736, oxide 2732, gate electrodes 2730, gate dielectric regions 2728, P- regions 2718', interlayer oxide regions ('ox'), and peripheral circuitry

substrate **2702** are shown in FIG. **27L2**. The gate electrode **2730** may be common to substantially all six P- regions **2718'** and controls the six double gated MOSFET select transistors. **[0399]** As illustrated in FIG. **27L**, a single exemplary double gated MOSFET select transistor on the first Si/SiO<sub>2</sub> layer **2723** may include P- region **2718'** (functioning as the transistor channel), N+ silicon regions **2716'** (functioning as source and drain), and two gate electrodes **2730** with associated gate dielectrics regions **2728**. The transistor may be electrically isolated from beneath by oxide layer **2708**.

**[0400]** The above flow enables the formation of a resistance-based 3D memory with one additional masking step per memory layer constructed by layer transfers of wafer sized doped mono-crystalline silicon layers and may be connected to an underlying multi-metal layer semiconductor device

**[0401]** Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **27A** through **27M** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the transistors may be of another type, such as RCATs. Additionally, the contacts may utilize doped polycrystalline silicon, or other conductive materials. Moreover, the stacked memory layer may be connected to a periphery circuit that may be above the memory stack. Further, the Si/SiO<sub>2</sub> layers **2723**, **2725** and **2727** may be annealed layer-by-layer after their associated implantations by using a laser anneal system. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

**[0402]** As illustrated in FIGS. **28A** to **28F**, a resistance-based 3D memory with two additional masking steps per memory layer may be constructed that may be suitable for 3D IC manufacturing. This 3D memory utilizes single gate MOSFET select transistors and may have a resistance-based memory element in series with the select transistor.

**[0403]** As illustrated in FIG. **28A**, a P- substrate donor wafer **2800** may be processed to include a wafer sized layer of P- doping **2804**. The P- doped layer **2804** may have the same or different dopant concentration than the P- substrate donor wafer **2800**. The P- doped layer **2804** may be formed by ion implantation and thermal anneal. A screen oxide **2801** may be grown before the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding.

**[0404]** As illustrated in FIG. **28B**, the top surface of P-substrate donor wafer **2800** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the P-doped layer **2804** to form oxide layer **2802**, or a re-oxidation of implant screen oxide **2801**. A layer transfer demarcation plane **2899** (shown as a dashed line) may be formed in P- substrate donor wafer **2800** or P- doped layer **2804** (shown) by hydrogen implantation **2807** or other methods as previously described. Both the P- substrate donor wafer **2800** and acceptor wafer **2810** may be prepared for wafer bonding as previously described and then bonded, for example, at a low temperature (less than approximately 400° C.) to minimize stresses. The portion of the P-layer **2804** and the P- substrate donor wafer **2800** that may be above the layer transfer demarcation plane **2899** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods.

**[0405]** As illustrated in FIG. **28C**, the remaining P- doped layer **2804'**, and oxide layer **2802** have been layer transferred

to acceptor wafer **2810**. Acceptor wafer **2810** may include peripheral circuits such that they can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The peripheral circuits may utilize a refractory metal such as, for example, tungsten that can withstand high temperatures greater than approximately 400° C. The top surface of P- doped layer **2804'** may be chemically or mechanically polished smooth and flat. Now transistors may be formed and aligned to the acceptor wafer **2810** alignment marks (not shown).

**[0406]** As illustrated in FIG. **28D** shallow trench isolation (STI) oxide regions (not shown) may be lithographically defined and plasma/RIE etched to at least the top level of oxide layer **2802** removing regions of mono-crystalline silicon P- doped layer **2804'**. A gap-fill oxide may be deposited and CMP'ed flat to form conventional STI oxide regions and P- doped mono-crystalline silicon regions (not shown) for forming the transistors. Threshold adjust implants may or may not be performed at this time. A gate stack **2824** may be formed with a gate dielectric, such as, for example, thermal oxide, and a gate metal material, such as, for example, polycrystalline silicon. Alternatively, the gate oxide may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Further, the gate oxide may be formed with a rapid thermal oxidation (RTO), a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate material such as, for example, tungsten or aluminum may be deposited. Gate stack self-aligned LDD (Lightly Doped Drain) and halo punch-thru implants may be performed at this time to adjust junction and transistor breakdown characteristics. A conventional spacer deposition of oxide and nitride and a subsequent etch-back may be done to form implant offset spacers (not shown) on the gate stacks **2824**. Then a self-aligned N+ source and drain implant may be performed to create transistor source and drains **2820** and remaining P- silicon NMOS transistor channels **2828**. High temperature anneal steps may or may not be done at this time to activate the implants and set initial junction depths. Finally, the entire structure may be substantially covered with a gap fill oxide **2850**, which may be planarized with chemical mechanical polishing. The oxide surface may be prepared for oxide to oxide wafer bonding as previously described.

**[0407]** As illustrated in FIG. **28E**, the transistor layer formation, bonding to acceptor wafer **2810** oxide **2850**, and subsequent transistor formation as described in FIGS. **28A** to **28D** may be repeated to form the second tier **2830** of memory transistors. After substantially all the desired memory layers are constructed, a rapid thermal anneal (RTA) may be conducted to activate the dopants in substantially all of the memory layers and in the acceptor wafer **2810** peripheral circuits. Alternatively, optical anneals, such as, for example, a laser based anneal, may be performed.

**[0408]** As illustrated in FIG. **28F**, source-line (SL) contacts/electrode **2834** may be lithographically defined, etched with plasma/RIE through the oxide **2850** and N+ silicon regions **2820** of each memory tier, and associated oxide vertical isolation regions to connect substantially all memory layers vertically, and photoresist removed. Resistance change material **2842**, such as, for example, hafnium oxide, may then

be deposited, for example, with atomic layer deposition (ALD). The electrode for the resistance change memory element may then be deposited by ALD to form the SL contact/electrode **2834**. The excess deposited material may be polished to planarity at or below the top of oxide **2850**. Each SL contact/electrode **2834** with resistive change material **2842** may be shared among substantially all layers of memory, shown as two layers of memory in FIG. **28F**. The SL contact/electrode **2834** electrically couples the memory layers' transistor N+ regions on the transistor source side **2852**. SL metal lines **2846** may be formed and connect to the associated SL contact/electrode **2834** with resistive change material **2842**. Oxide layer **2853** may be deposited and planarized. Bit-line (BL) contacts **2840** may be lithographically defined, etched with plasma/RIE through oxide layer **2853**, the oxide **2850** and N+ silicon regions **2820** of each memory tier, and associated oxide vertical isolation regions to connect substantially all memory layers vertically, and photoresist removed. BL contacts **2840** electrically couple the memory layers' transistor N+ regions on the transistor drain side **2854**. BL metal lines **2848** may be formed and connect to the associated BL contacts **2840**. The gate stacks, such as, for example, gate stacks **2824**, may be connected with a contact and metallization (not shown) to form the word-lines (WLs). A thru layer via (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor wafer **2810** peripheral circuitry via an acceptor wafer metal connect pad (not shown).

[**0409**] This flow enables the formation of a resistance-based 3D memory with two additional masking steps per memory layer constructed by layer transfers of wafer sized doped layers and this 3D memory may be connected to an underlying multi-metal layer semiconductor device.

[**0410**] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **28A** through **28F** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the transistors may be of another type such as PMOS or RCATs. Additionally, the stacked memory layer may be connected to a periphery circuit that may be above the memory stack. Moreover, each tier of memory could be configured with a slightly different donor wafer P- layer doping profile. Further, the memory could be organized in a different manner, such as BL and SL interchanged, or where there are buried wiring whereby wiring for the memory array may be below the memory layers but above the periphery. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[**0411**] Charge trap NAND (Negated AND) memory devices are another form of popular commercial non-volatile memories. Charge trap device store their charge in a charge trap layer, wherein this charge trap layer then influences the channel of a transistor. Background information on charge-trap memory can be found in "*Integrated Interconnect Technologies for 3D Nanoelectronic Systems*", Artech House, 2009 by Bakir and Meindl ("Bakir"), "A Highly Scalable 8-Layer 3D Vertical-Gate (VG) TFT NAND Flash Using Junction-Free Buried Channel BE-SONOS Device," Symposium on VLSI Technology, 2010 by Hang-Ting Lue, et al., and "Introduction to Flash memory", Proc. IEEE91, 489-502 (2003) by R. Bez, et al. Work described in Bakir utilized selective epitaxy, laser recrystallization, or polysilicon to

form the transistor channel, which results in less than satisfactory transistor performance. The architectures shown in FIGS. **29** and **30** may be relevant for any type of charge-trap memory.

[**0412**] As illustrated in FIGS. **29A** to **29G**, a charge trap based two additional masking steps per memory layer 3D memory may be constructed that may be suitable for 3D IC. This 3D memory utilizes NAND strings of charge trap transistors constructed in mono-crystalline silicon.

[**0413**] As illustrated in FIG. **29A**, a P- substrate donor wafer **2900** may be processed to include a wafer sized layer of P- doping **2904**. The P-doped layer **2904** may have the same or different dopant concentration than the P- substrate donor wafer **2900**. The P- doped layer **2904** may have a vertical dopant gradient. The P- doped layer **2904** may be formed by ion implantation and thermal anneal. A screen oxide **2901** may be grown before the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding.

[**0414**] As illustrated in FIG. **29B**, the top surface of P-substrate donor wafer **2900** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the P-doped layer **2904** to form oxide layer **2902**, or a re-oxidation of implant screen oxide **2901**. A layer transfer demarcation plane **2999** (shown as a dashed line) may be formed in P- substrate donor wafer **2900** or P- doped layer **2904** (shown) by hydrogen implantation **2907** or other methods as previously described. Both the P- substrate donor wafer **2900** and acceptor wafer **2910** may be prepared for wafer bonding as previously described and then bonded, for example, at a low temperature (less than approximately 400° C.) to minimize stresses. The portion of the P-doped layer **2904** and the P- substrate donor wafer **2900** that may be above the layer transfer demarcation plane **2999** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods.

[**0415**] As illustrated in FIG. **29C**, the remaining P- layer **2904'**, and oxide layer **2902** have been layer transferred to acceptor wafer **2910**. Acceptor wafer **2910** may include peripheral circuits such that they can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The peripheral circuits may utilize a refractory metal such as, for example, tungsten that can withstand high temperatures greater than approximately 400° C. The top surface of P- layer **2904'** may be chemically or mechanically polished smooth and flat. Now transistors may be formed and aligned to the acceptor wafer **2910** alignment marks (not shown).

[**0416**] As illustrated in FIG. **29D** shallow trench isolation (STI) oxide regions (not shown) may be lithographically defined and plasma/RIE etched to at least the top level of oxide layer **2902** removing regions of mono-crystalline silicon P- layer **2904'**, thus forming P- doped regions **2920**. A gap-fill oxide may be deposited and CMP'ed flat to form conventional STI oxide regions and P- doped mono-crystalline silicon regions (not shown) for forming the transistors. Threshold adjust implants may or may not be performed at this time. A gate stack may be formed with growth or deposition of a charge trap gate dielectric **2922**, such as, for example, thermal oxide and silicon nitride layers (ONO:

Oxide-Nitride-Oxide), and a gate metal material **2924**, such as, for example, doped or undoped poly-crystalline silicon. Alternatively, the charge trap gate dielectric may include silicon or III-V nano-crystals encased in an oxide.

[0417] As illustrated in FIG. 29E, gate stacks **2928** may be lithographically defined and plasma/RIE etched removing regions of gate metal material **2924** and charge trap gate dielectric **2922**. A self aligned N+ source and drain implant may be performed to create inter-transistor source and drains **2934** and end of NAND string source and drains **2930**. Finally, the entire structure may be substantially covered with a gap fill oxide layer **2950** and the oxide planarized with chemical mechanical polishing. The oxide surface may be prepared for oxide to oxide wafer bonding as previously described. This now forms the first tier of memory transistors **2942** which includes silicon oxide layer **2950**, gate stacks **2928**, inter-transistor source and drains **2934**, end of NAND string source and drains **2930**, P- doped regions **2920**, and oxide layer **2902**.

[0418] As illustrated in FIG. 29F, the transistor layer formation, bonding to acceptor wafer **2910** oxide layer **2950**, and subsequent transistor formation as described in FIGS. 29A to 29D may be repeated to form the second tier **2944** of memory transistors on top of the first tier of memory transistors **2942**. After substantially all the desired memory layers are constructed, a rapid thermal anneal (RTA) may be conducted to activate the dopants in substantially all of the memory layers and in the acceptor wafer **2910** peripheral circuits. Alternatively, optical anneals, such as, for example, a laser based anneal, may be performed.

[0419] As illustrated in FIG. 29G, source line (SL) ground contact **2948** and bit line contact **2949** may be lithographically defined, etched with plasma/RIE through oxide layer **2950**, end of NAND string source and drains **2930**, and P-doped regions **2920** of each memory tier, and associated oxide vertical isolation regions to connect substantially all memory layers vertically, and photoresist removed. Metal or heavily doped poly-crystalline silicon may be utilized to fill the contacts and metallization utilized to form BL and SL wiring (not shown). The gate stacks **2928** may be connected with a contact and metallization to form the word-lines (WLs) and WL wiring (not shown). A thru layer via (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor wafer **2910** peripheral circuitry via an acceptor wafer metal connect pad (not shown).

[0420] This flow enables the formation of a charge trap based 3D memory with two additional masking steps per memory layer constructed by layer transfers of wafer sized doped layers of mono-crystalline silicon and this 3D memory may be connected to an underlying multi-metal layer semiconductor device.

[0421] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 29A through 29G are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, BL or SL select transistors may be constructed within the process flow. Additionally, the stacked memory layer may be connected to a periphery circuit that may be above the memory stack. Moreover, each tier of memory could be configured with a slightly different donor wafer P-layer doping profile. Further, the memory could be organized in a different manner, such as BL and SL interchanged, or these architectures can be modified into a NOR flash memory style, or where buried wiring for the memory array may be

below the memory layers but above the periphery. Additionally, the charge trap dielectric and gate layer may be deposited before the layer transfer and temporarily bonded to a carrier or holder wafer or substrate and then transferred to the acceptor substrate with periphery. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0422] As illustrated in FIGS. 30A to 30G, a charge trap based 3D memory with zero additional masking steps per memory layer 3D memory may be constructed that may be suitable for 3D IC manufacturing. This 3D memory utilizes NAND strings of charge trap junction-less transistors with junction-less select transistors constructed in mono-crystalline silicon.

[0423] As illustrated in FIG. 30A, a silicon substrate with peripheral circuitry **3002** may be constructed with high temperature (greater than approximately 400° C.) resistant wiring, such as, for example, Tungsten. The peripheral circuitry substrate **3002** may include memory control circuits as well as circuitry for other purposes and of various types, such as, for example, analog, digital, RF, or memory. The peripheral circuitry substrate **3002** may include peripheral circuits that can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The top surface of the peripheral circuitry substrate **3002** may be prepared for oxide wafer bonding with a deposition of a silicon oxide layer **3004**, thus forming acceptor wafer **3014**.

[0424] As illustrated in FIG. 30B, a mono-crystalline silicon donor wafer **3012** may be processed to include a wafer sized layer of N+ doping (not shown) which may have a different dopant concentration than the N+ substrate **3006**. The N+ doping layer may be formed by ion implantation and thermal anneal. A screen oxide layer **3008** may be grown or deposited prior to the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. A layer transfer demarcation plane **3010** (shown as a dashed line) may be formed in donor wafer **3012** within the N+ substrate **3006** or the N+ doping layer (not shown) by hydrogen implantation or other methods as previously described. Both the donor wafer **3012** and acceptor wafer **3014** may be prepared for wafer bonding as previously described and then bonded at the surfaces of oxide layer **3004** and oxide layer **3008**, for example, at a low temperature (less than approximately 400° C.) for lowest stresses, or a moderate temperature (less than approximately 900° C.).

[0425] As illustrated in FIG. 30C, the portion of the N+ layer (not shown) and the N+ wafer substrate **3006** that may be above the layer transfer demarcation plane **3010** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining mono-crystalline silicon N+ layer **3006'**. Remaining N+ layer **3006'** and oxide layer **3008** have been layer transferred to acceptor wafer **3014**. The top surface of N+ layer **3006'** may be chemically or mechanically polished smooth and flat. Oxide layer **3020** may be deposited to prepare the surface for later oxide to oxide



bonding. This now forms the first Si/SiO<sub>2</sub> layer **3023** which includes silicon oxide layer **3020**, N<sup>+</sup> silicon layer **3006'**, and oxide layer **3008**.

**[0426]** As illustrated in FIG. **30D**, additional Si/SiO<sub>2</sub> layers, such as, for example, second Si/SiO<sub>2</sub> layer **3025** and third Si/SiO<sub>2</sub> layer **3027**, may each be formed as described in FIGS. **30A** to **30C**. Oxide layer **3029** may be deposited to electrically isolate the top N<sup>+</sup> silicon layer.

**[0427]** As illustrated in FIG. **30E**, oxide layer **3029**, third Si/SiO<sub>2</sub> layer **3027**, second Si/SiO<sub>2</sub> layer **3025** and first Si/SiO<sub>2</sub> layer **3023** may be lithographically defined and plasma/RIE etched to form a portion of the memory cell structure, which now includes regions of N<sup>+</sup> silicon **3026** and oxide **3022**.

**[0428]** As illustrated in FIG. **30F**, a gate stack may be formed with growth or deposition of a charge trap gate dielectric layer, such as, for example, thermal oxide and silicon nitride layers (ONO: Oxide-Nitride-Oxide), and a gate metal electrode layer, such as, for example, doped or undoped polycrystalline silicon. The gate metal electrode layer may then be planarized with chemical mechanical polishing. Alternatively, the charge trap gate dielectric layer may include silicon or III-V nano-crystals encased in an oxide. The select transistor gate area **3038** may include a non-charge trap dielectric. The gate metal electrode regions **3030** and gate dielectric regions **3028** of both the NAND string area **3036** and select transistor gate area **3038** may be lithographically defined and plasma/RIE etched.

**[0429]** As illustrated in FIG. **30G**, the entire structure may be substantially covered with a gap fill oxide **3032**, which may be planarized with chemical mechanical polishing. The oxide **3032** is shown transparent in the figure for clarity. Select metal lines **3046** may be formed and connect to the associated select gate contacts **3034**. Contacts and associated metal interconnect lines (not shown) may be formed for the WL and SL at the memory array edges. Word-line regions (WL) **3036**, coupled with and composed of gate metal electrode regions **3030**, and bit-line regions (BL) **3052**, composed of indicated N<sup>+</sup> silicon regions **3026**, are shown. Source regions **3044** may be formed by trench contact etch and fill to couple to the N<sup>+</sup> silicon regions on the source end of the NAND string. A thru layer via (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor wafer **3014** peripheral circuitry via an acceptor wafer metal connect pad (not shown).

**[0430]** This flow enables the formation of a charge trap based 3D memory with zero additional masking steps per memory layer constructed by layer transfers of wafer sized doped layers of mono-crystalline silicon and this 3D memory may be connected to an underlying multi-metal layer semiconductor device.

**[0431]** Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **30A** through **30G** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, BL or SL contacts may be constructed in a staircase manner as described previously. Additionally, the stacked memory layer may be connected to a periphery circuit that may be above the memory stack. Moreover, each tier of memory could be configured with a slightly different donor wafer N<sup>+</sup> layer doping profile. Further, the memory could be organized in a different manner, such as BL and SL interchanged, or where buried wiring for the memory array may be below the memory layers but above the periphery. Additional

types of 3D charge trap memories may be constructed by layer transfer of mono-crystalline silicon; for example, those found in "A Highly Scalable 8-Layer 3D Vertical-Gate (VG) TFT NAND Flash Using Junction-Free Buried Channel BE-SONOS Device," Symposium on VLSI Technology, 2010 by Hang-Ting Lue, et al. and "Multi-layered Vertical Gate NAND Flash overcoming stacking limit for terabit density storage", Symposium on VLSI Technology, 2009 by W. Kim, S. Choi, et al. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

**[0432]** Floating gate (FG) memory devices are another form of popular commercial non-volatile memories. Floating gate devices store their charge in a conductive gate (FG) that may typically be isolated from unintentional electric fields, wherein the charge on the FG may then influence the channel of a transistor. Background information on floating gate flash memory can be found in "Introduction to Flash memory", Proc. IEEE91, 489-502 (2003) by R. Bez, et al. The architectures shown in FIGS. **31** and **32** may be relevant for any type of floating gate memory.

**[0433]** As illustrated in FIGS. **31A** to **31G**, a floating gate based 3D memory with two additional masking steps per memory layer may be constructed that may be suitable for 3D IC manufacturing. This 3D memory utilizes NAND strings of floating gate transistors constructed in mono-crystalline silicon.

**[0434]** As illustrated in FIG. **31A**, a P<sup>-</sup> substrate donor wafer **3100** may be processed to include a wafer sized layer of P<sup>-</sup> doping **3104**. The P-doped layer **3104** may have the same or a different dopant concentration than the P<sup>-</sup> substrate donor wafer **3100**. The P<sup>-</sup> doped layer **3104** may have a vertical dopant gradient. The P<sup>-</sup> doped layer **3104** may be formed by ion implantation and thermal anneal. A screen oxide **3101** may be grown before the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding.

**[0435]** As illustrated in FIG. **31B**, the top surface of P<sup>-</sup> substrate donor wafer **3100** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the P-doped layer **3104** to form oxide layer **3102**, or a re-oxidation of implant screen oxide **3101**. A layer transfer demarcation plane **3199** (shown as a dashed line) may be formed in P<sup>-</sup> substrate donor wafer **3100** or P<sup>-</sup> doped layer **3104** (shown) by hydrogen implantation **3107** or other methods as previously described. Both the P<sup>-</sup> substrate donor wafer **3100** and acceptor wafer **3110** may be prepared for wafer bonding as previously described and then bonded, for example, at a low temperature (less than approximately 400° C.) to minimize stresses. The portion of the P-doped layer **3104** and the P<sup>-</sup> substrate donor wafer **3100** that may be above the layer transfer demarcation plane **3199** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods.

**[0436]** As illustrated in FIG. **31C**, the remaining P<sup>-</sup> layer **3104'**, and oxide layer **3102** have been layer transferred to acceptor wafer **3110**. Acceptor wafer **3110** may include peripheral circuits such that they can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants in antipa-

tion of anneals later in the process flow. The peripheral circuits may utilize a refractory metal such as, for example, tungsten that can withstand high temperatures greater than approximately 400° C. The top surface of P-layer 3104' may be chemically or mechanically polished smooth and flat. Now transistors may be formed and aligned to the acceptor wafer 3110 alignment marks (not shown).

[0437] As illustrated in FIG. 31D a partial gate stack may be formed with growth or deposition of a tunnel oxide 3122, such as, for example, thermal oxide, and a FG gate metal material 3124, such as, for example, doped or undoped polycrystalline silicon. Shallow trench isolation (STI) oxide regions (not shown) may be lithographically defined and plasma/RIE etched to at least the top level of oxide layer 3102 removing regions of mono-crystalline silicon P-layer 3104', thus forming P-doped silicon regions 3120. A gap-fill oxide may be deposited and CMP'ed flat to form conventional STI oxide regions (not shown).

[0438] As illustrated in FIG. 31E, an inter-poly oxide layer, such as, for example, silicon oxide and silicon nitride layers (ONO: Oxide-Nitride-Oxide), and then a Control Gate (CG) gate metal material, such as, for example, doped or undoped polycrystalline silicon, may be deposited. The gate stacks 3128 may be lithographically defined and plasma/RIE etched removing regions of CG gate metal material, inter-poly oxide layer, FG gate metal material 3124, and tunnel oxide 3122. This results in the gate stacks 3128 including CG gate metal regions 3126', inter-poly oxide regions 3125', FG gate metal regions 3124', and tunnel oxide regions 3122'. Only one gate stack 3128 may be annotated with region tie lines for clarity. A self-aligned N+ source and drain implant may be performed to create inter-transistor source and drains 3134 and end of NAND string source and drains 3130. Finally, the entire structure may be substantially covered with a gap fill oxide 3150, which may be planarized with chemical mechanical polishing. The oxide surface may be prepared for oxide to oxide wafer bonding as previously described. This now forms the first tier of memory transistors 3142 which includes silicon oxide 3150, gate stacks 3128, inter-transistor source and drains 3134, end of NAND string source and drains 3130, P-doped silicon regions 3120, and oxide layer 3102.

[0439] As illustrated in FIG. 31F, the transistor layer formation, bonding to acceptor wafer 3110 oxide 3150, and subsequent transistor formation as described in FIGS. 31A to 31D may be repeated to form the second tier 3144 of memory transistors on top of the first tier of memory transistors 3142. After substantially all the desired memory layers are constructed, a rapid thermal anneal (RTA) may be conducted to activate the dopants in substantially all of the memory layers and in the acceptor wafer 3110 peripheral circuits. Alternatively, optical anneals, such as, for example, a laser based anneal, may be performed.

[0440] As illustrated in FIG. 31G, source line (SL) ground contact 3148 and bit line contact 3149 may be lithographically defined, etched with plasma/RIE through oxide 3150, end of NAND string source and drains 3130, and P-doped silicon regions 3120 of each memory tier, and associated oxide vertical isolation regions to connect substantially all memory layers vertically, and photoresist removed. Metal or heavily doped poly-crystalline silicon may be utilized to fill the contacts and metallization utilized to form BL and SL wiring (not shown). The gate stacks 3128 may be connected with a contact and metallization to form the word-lines (WLs)

and WL wiring (not shown). A thru layer via (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor wafer 3110 peripheral circuitry via an acceptor wafer metal connect pad (not shown).

[0441] This flow enables the formation of a floating gate based 3D memory with two additional masking steps per memory layer constructed by layer transfers of wafer sized doped layers of mono-crystalline silicon and this 3D memory may be connected to an underlying multi-metal layer semiconductor device.

[0442] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 31A through 31G are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, BL or SL select transistors may be constructed within the process flow. Additionally, the stacked memory layer may be connected to a periphery circuit that may be above the memory stack. Moreover, each tier of memory could be configured with a slightly different donor wafer P-layer doping profile. Further, the memory could be organized in a different manner, such as BL and SL interchanged, or where buried wiring for the memory array may be below the memory layers but above the periphery. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0443] As illustrated in FIGS. 32A to 32H, a floating gate based 3D memory with one additional masking step per memory layer 3D memory may be constructed that may be suitable for 3D IC manufacturing. This 3D memory utilizes 3D floating gate junction-less transistors constructed in mono-crystalline silicon.

[0444] As illustrated in FIG. 32A, a silicon substrate with peripheral circuitry 3202 may be constructed with high temperature (greater than approximately 400° C.) resistant wiring, such as, for example, Tungsten. The peripheral circuitry substrate 3202 may include memory control circuits as well as circuitry for other purposes and of various types, such as, for example, analog, digital, RF, or memory. The peripheral circuitry substrate 3202 may include peripheral circuits that can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants in anticipation of anneals later in the process flow. The top surface of the peripheral circuitry substrate 3202 may be prepared for oxide wafer bonding with a deposition of a silicon oxide layer 3204, thus forming acceptor wafer 3214.

[0445] As illustrated in FIG. 32B, a mono-crystalline N+ doped silicon donor wafer 3212 may be processed to include a wafer sized layer of N+ doping (not shown) which may have a different dopant concentration than the N+ substrate 3206. The N+ doping layer may be formed by ion implantation and thermal anneal. A screen oxide layer 3208 may be grown or deposited prior to the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. A layer transfer demarcation plane 3210 (shown as a dashed line) may be formed in donor wafer 3212 within the N+ substrate 3206 or the N+ doping layer (not shown) by hydrogen implantation or other methods as previously described. Both the donor wafer 3212 and acceptor wafer 3214 may be prepared for wafer bonding as

previously described and then bonded at the surfaces of oxide layer 3204 and oxide layer 3208, for example, at a low temperature (less than approximately 400° C.) for lowest stresses, or a moderate temperature (less than approximately 900° C.).

[0446] As illustrated in FIG. 32C, the portion of the N+ layer (not shown) and the N+ wafer substrate 3206 that may be above the layer transfer demarcation plane 3210 may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining mono-crystalline silicon N+ layer 3206'. Remaining N+ layer 3206' and oxide layer 3208 have been layer transferred to acceptor wafer 3214. The top surface of N+ layer 3206' may be chemically or mechanically polished smooth and flat. Now transistors or portions of transistors may be formed and aligned to the acceptor wafer 3214 alignment marks (not shown).

[0447] As illustrated in FIG. 32D N+ regions 3216 may be lithographically defined and then etched with plasma/RIE removing regions of N+ layer 3206' and stopping on or partially within oxide layer 3208.

[0448] As illustrated in FIG. 32E a tunneling dielectric 3218 may be grown or deposited, such as, for example, thermal silicon oxide, and a floating gate (FG) material 3228, such as, for example, doped or undoped poly-crystalline silicon, may be deposited. The structure may be planarized by chemical mechanical polishing to approximately the level of the N+ regions 3216. The surface may be prepared for oxide to oxide wafer bonding as previously described, such as, for example, a deposition of a thin oxide. This now forms the first memory layer 3223 which includes future FG regions 3228, tunneling dielectric 3218, N+ regions 3216 and oxide layer 3208.

[0449] As illustrated in FIG. 32F, the N+ layer formation, bonding to an acceptor wafer, and subsequent memory layer formation as described in FIGS. 32A to 32E may be repeated to form the second layer of memory 3225 on top of the first memory layer 3223. Oxide layer 3229 may then be deposited.

[0450] As illustrated in FIG. 32G, FG regions 3238 may be lithographically defined and then etched with plasma/RIE removing portions of oxide layer 3229, future FG regions 3228 and oxide layer 3208 on the second layer of memory 3225 and future FG regions 3228 on the first memory layer 3223, stopping on or partially within oxide layer 3208 of the first memory layer 3223.

[0451] As illustrated in FIG. 32H, an inter-poly oxide layer 3250, such as, for example, silicon oxide and silicon nitride layers (ONO: Oxide-Nitride-Oxide), and a Control Gate (CG) gate material 3252, such as, for example, doped or undoped poly-crystalline silicon, may be deposited. The surface may be planarized by chemical mechanical polishing leaving a thinned oxide layer 3229'. As shown in the illustration, this results in the formation of 4 horizontally oriented floating gate memory cells with N+ junction-less transistors. Contacts and metal wiring to form well-known memory access/decoding schemes may be processed and a thru layer via may be formed to electrically couple the memory access decoding to the acceptor substrate peripheral circuitry via an acceptor wafer metal connect pad.

[0452] This flow enables the formation of a floating gate based 3D memory with one additional masking step per memory layer constructed by layer transfers of wafer sized

doped layers of mono-crystalline silicon and this 3D memory may be connected to an underlying multi-metal layer semiconductor device.

[0453] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 32A through 32H are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, memory cell control lines could be built in a different layer rather than the same layer. Additionally, the stacked memory layers may be connected to a periphery circuit that may be above the memory stack. Moreover, each tier of memory could be configured with a slightly different donor wafer N+ layer doping profile. Further, the memory could be organized in a different manner, such as BL and SL interchanged, or these architectures could be modified into a NOR flash memory style, or where buried wiring for the memory array may be below the memory layers but above the periphery. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0454] The following sections discuss some embodiments of the invention wherein wafer or die-sized pre-formed repeating strips of layers in a donor wafer may be transferred onto an acceptor wafer and then may be processed to create 3D ICs.

[0455] An embodiment of the invention is to pre-process a donor wafer by forming repeating wafer-sized or die-sized strips of layers of various materials without a forming process temperature restriction, then layer transferring the pre-processed donor wafer to the acceptor wafer, and processing with either low temperature (below approximately 400° C.) or high temperature (greater than approximately 400° C.) after the layer transfer to form device structures, such as, for example, transistors, on or in the donor wafer that may be physically aligned and may be electrically coupled to the acceptor wafer. The donor wafer and acceptor wafer in these discussions may include the compositions, such as metal layers and TLVs, referred to for donor wafers and acceptor wafers in the FIGS. 1, 2 and 3 layer transfer discussions.

[0456] As illustrated in FIG. 33A, a generalized process flow may begin with a donor wafer 3300 that may be preprocessed with repeating strips across the wafer or die of conducting, semi-conducting or insulating materials that may be formed by deposition, ion implantation and anneal, oxidation, epitaxial growth, combinations of above, or other semiconductor processing steps and methods. For example, a repeating pattern of n-type strips 3304 and p-type strips 3306 may be constructed on donor wafer 3300 and are drawn in illustration blow-up area 3302. The width of the n-type strips 3304 may be  $W_n$  3314 and the width of the p-type strips 3306 may be  $W_p$  3316. Their sum  $W$  3308 may be the width of the repeating pattern. A four cardinal directions indicator 3340 may be used to assist the explanation. The strips traverse from East to West and the alternating repeats from North to South. The donor wafer n-type strips 3304 and p-type strips 3306 may extend in length from East to West by the acceptor die width plus the maximum donor wafer to acceptor wafer misalignment, or alternatively, may extend the entire length of a donor wafer from East to West. Donor wafer 3300 may have one or more donor alignment marks 3320. The donor wafer 3300 may be preprocessed with a layer transfer demarcation plane, such as, for example, a hydrogen implant cleave plane.

[0457] As illustrated in FIG. 33B, the donor wafer 3300 with a layer transfer demarcation plane may be flipped over, aligned, and bonded to the acceptor wafer 3310. Typically the donor wafer 3300 to acceptor wafer 3310 maximum misalignment that may result from the bonding processing may be approximately 1 micron. The acceptor wafer 3310 may be a preprocessed wafer that may have fully functional circuitry or may be a wafer with previously transferred layers, or may be a blank carrier or holder wafer, or other kinds of substrates. The acceptor wafer 3310 and the donor wafer 3300 may be a bulk mono-crystalline silicon wafer or a Silicon On Insulator (SOI) wafer or a Germanium on Insulator (GeOI) wafer. Both the donor wafer 3300 and the acceptor wafer 3310 bonding surfaces may be prepared for wafer bonding by oxide depositions, polishes, plasma, or wet chemistry treatments to facilitate successful wafer to wafer bonding. The donor wafer 3300 may be cleaved at or thinned to the layer transfer demarcation plane, leaving donor wafer portion 3300L and the pre-processed strips and layers such as, for example, n-type strips 3304 and p-type strips 3306. The donor wafer 3300 may now also be processed and reused for more layer transfers.

[0458] As further illustrated in FIG. 33B, the remaining donor wafer portion 3300L may be further processed to create device structures and thru layer connections to landing strips or pads 3338 on the acceptor wafer. The landing strips or pads 3338 may be formed with metals, such as, for example, copper or aluminum, and may include barrier metals, such as, for example, TiN or WCo. A four cardinal directions indicator 3340 may be used to assist the explanation. By making the landing strips or pads 3338 in FIG. 33D somewhat wider than the width W 3308 of the repeating strips, the alignment of the device structures on the donor wafer can be shifted up or down (North or South) in steps of distance W until the thru layer connections may be within a W distance to being on top of the appropriate landing pad. Since there's no pattern in the other direction, the alignment can be left or right (East or West) as much as needed until the thru layer connections may be on top of the appropriate landing pad. This mask alignment scheme is further explained below. The misalignment in the East-West direction may be DX 3324 and the misalignment in the North-South direction may be DY 3322. For simplicity of the following explanations, the donor wafer alignment mark 3320 and acceptor wafer alignment mark 3321 may be assumed to be placed such that the donor wafer alignment mark 3320 is always north of the acceptor wafer alignment mark 3321. The cases where donor wafer alignment mark 3320 may be either perfectly aligned with or aligned south of acceptor alignment mark 3321 may be handled in a similar manner. In addition, these alignment marks may be placed in only a few locations on each wafer, within each step field, within each die, within each repeating pattern W, or in other locations as a matter of design choice. As a result of the die-sized or wafer-sized donor wafer strips, such as, for example, n-type strips 3304 and p-type strips 3306, extending in the East-West direction, proper East-West alignment to those prefabricated strips may be achieved regardless of misalignment DX 3324. Alignment of images for further processing of donor wafer structures in the East-West direction may be accomplished by utilizing the East-West co-ordinate of the acceptor wafer alignment mark 3321. If die-sized donor wafer strips are utilized, the repeating strips may overlap into the die scribeline the distance of the maximum donor wafer to acceptor wafer misalignment.

[0459] As illustrated in FIG. 33C, donor wafer alignment mark 3320 may land DY 3322 distance in the North-South direction away from acceptor alignment mark 3321. N-type strips 3304 and p-type strips 3306 of repeat width sum W 3308 may be drawn in illustration blow-up area 3302. A four cardinal directions indicator 3340 may be used to assist the explanation. In this illustration, misalignment DY 3322 may include three repeat sum distances W 3308 and a residual Rdy 3325. In the generalized case, residual Rdy 3325 may be the remainder of DY 3322 modulo W 3308,  $0 \leq \text{Rdy } 3325 < W 3308$ . Proper alignment of images for further processing of donor wafer structures may be accomplished by utilizing the East-West coordinate of acceptor wafer alignment mark 3321 for the image's East-West alignment mark position, and by shifting Rdy 3325 from the acceptor wafer alignment mark 3321 in the North-South direction for the image's North-South alignment mark position.

[0460] As illustrated in FIG. 33D acceptor metal connect strip or landing pad 3338 may be designed with length W 3308 plus an extension for via design rules and for angular misalignment across the die. Acceptor metal connect strip 3338 may be oriented length-wise in the North-South direction. The acceptor metal connect strip 3338 may be formed with metals, such as, for example, copper or aluminum, and may include barrier metals, such as, for example, TiN or WCo. A four cardinal directions indicator 3340 may be used to assist the explanation. The acceptor metal connect strip 3338 extension, in length and/or width, may include compensation for via design rules and for angular (rotational) misalignment between the donor and acceptor wafer as a result of being bonded together, and may include uncompensated donor wafer bow and warp. The acceptor metal connect strip 3338 may be aligned to the acceptor wafer alignment mark 3321. Thru layer via (TLV) 3336 may be aligned as described above in a similar manner as other donor wafer structure definition images. The TLV's 3336 East-West alignment mark position may be the East-West coordinate of acceptor wafer alignment mark 3321, and the TLV's North-South alignment mark position may be Rdy 3325 from the acceptor wafer alignment mark 3321 in the North-South direction.

[0461] As illustrated in FIG. 33E, the donor wafer alignment mark 3320 may be replicated precisely every repeat W 3308 in the North to South direction, including alignment marks 3320X, and 3320C, for a distance to substantially cover the full extent of potential North to South donor wafer to acceptor wafer misalignment M 3357. The donor wafer alignment mark 3320 may land DY 3322 distance in the North-South direction away from acceptor alignment mark 3321. N-type strips 3304 and p-type strips 3306 of repeat width sum W 3308 are drawn in illustration blow-up area 3302. A four cardinal directions indicator 3340 may be used to assist the explanation. The residue Rdy 3325 may therefore be the North to South misalignment between the closest donor wafer alignment mark 3320C and the acceptor wafer alignment mark 3321. Proper alignment of images for further processing of donor wafer structures may be accomplished by utilizing the East-West coordinate of acceptor wafer alignment mark 3321 for the image's East-West alignment mark position, and by shifting Rdy 3325 from the acceptor wafer alignment mark 3321 in the North-South direction for the image's North-South alignment mark position.

[0462] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 33A through 33E are exemplary only and are not drawn to scale. Such skilled persons will

further appreciate that many variations are possible such as, for example,  $W_n$  3314 and  $W_p$  3316 could be set for the minimum width of the corresponding transistor plus its isolation in the selected process node. Additionally, the North-South direction could become the East-West direction (and vice versa) by merely rotating the wafer 90° and that the strips of n-type transistors 3304 and strips of p-type transistors 3306 could also run North-South as a matter of design choice with corresponding adjustments to the rest of the fabrication process. Such skilled persons will further appreciate that the strips of n-type transistors 3304 and strips of p-type transistors 3306 can have many different organizations as a matter of design choice. For example, the strips of n-type transistors 3304 and strips of p-type transistors 3306 can each include a single row of transistors in parallel, multiple rows of transistors in parallel, multiple groups of transistors of different dimensions and orientations and types (either individually or in groups), and different ratios of transistor sizes or numbers among the strips of n-type transistors 3304 and strips of p-type transistors 3306. Moreover, TLV 3336 may be drawn in the database (not shown) so that it may be positioned approximately at the center of the acceptor metal connect strip 3338, and, hence, may be away from the ends of the acceptor metal connect strip 3338 at distances greater than approximately the nominal layer to layer misalignment margin. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the scope of the invention is to be limited only by the appended claims.

[0463] There may be multiple methods by which a transistor or other devices may be formed to enable the manufacturing of a 3D IC. Two examples may be described.

[0464] As illustrated in FIGS. 34A to 34L, planar V-groove NMOS and PMOS transistors may be formed with a single layer transfer as follows. As illustrated in FIG. 34A of a top view blow-up section of a donor wafer (with reference to the FIG. 33A discussion), repeating strips of repeat width  $W$  3476 may be created in the East-West direction. A four cardinal directions indicator 3474 may be used to assist the explanation. Repeating strips of repeat width  $W$  3476 may be as long as the length of the acceptor die plus a margin for the maximum donor wafer to acceptor wafer misalignment, or alternatively, these repeating strips of repeat width  $W$  3476 may extend the entire length of a donor wafer. The remaining FIGS. 34B to 34L illustrate a cross sectional view.

[0465] As illustrated in FIG. 34B, a P- substrate donor wafer 3400 may be processed to include East to West strips of N+ doping 3404 and P+ doping 3406 of combined repeating strips of repeat width  $W$  3476 in the North to South direction. A two cardinal directions indicator 3475 may be used to assist the explanation. The N+ strip 3404 and P+ strip 3406 may be formed by masked ion implantation and a thermal anneal.

[0466] As illustrated in FIG. 34C, a P-epitaxial growth may be performed and then followed by masking, ion implantation, and anneal to form East to West strips of N- doping 3410 and P-doping 3408 of combined repeating strips of repeat width  $W$  3476 in the North to South direction and in alignment with previously formed N+ strips 3404 and P+ strips 3406. N-strip 3410 may be stacked on top of P+ strip 3406, and P- strip 3408 may be stacked on top of N+ strip 3404. N+ strips 3404, P+ strips 3406, P- strip 3408, and N-strip 3410 may have graded or various layers of doping to mitigate transistor performance issues, such as, for example, short channel effects, or lower contact resistance after the NMOS

and PMOS transistors are formed. N+ strip 3404 may have a doping concentration that may be more than 10× the doping concentration of P- strip 3408. P+ strip 3406 may have a doping concentration that may be more than 10× the doping concentration of N- strip 3410. As illustrated in FIG. 34D shallow P+ strips 3412 and N+ strips 3414 may be formed by masking, shallow ion implantation, and RTA activation to form East to West strips of P+ doping 3412 and N+ doping 3414 of combined repeating strips of repeat width  $W$  3476 in the North to South direction and in alignment with previously formed N+ strips 3404, P+ strips 3406, N- strips 3410 and P- strips 3408. N+ strip 3414 may be stacked on top of N-strip 3410, and P+ strip 3412 may be stacked on top of P- strip 3408. The shallow P+ strips 3412 and N+ strips 3414 may be doped by Plasma Assisted Doping (PLAD) techniques.

[0467] As illustrated in FIG. 34E, the top surface of processed P- substrate donor wafer 3400 may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of shallow P+ strips 3412 and N+ strips 3414 to form oxide layer 3418. A layer transfer demarcation plane 3499 (shown as dashed line) may be formed by hydrogen implantation 3407 or other methods as previously described. Oxide layer 3418 may be deposited or grown before the H+ implant, and may include differing thicknesses over the P+ strips 3412 and N+ strips 3414 to allow an even H+ implant range stopping and facilitate a level and continuous layer transfer demarcation plane 3499 (shown as dashed line). Both the P- substrate donor wafer 3400 and acceptor wafer 3411 may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the N+ strips 3404, P+ strips 3406, and the P- substrate donor wafer 3400 that may be above the layer transfer demarcation plane 3499 may be removed by cleaving or other low temperature processes as previously described, such as, for example, ion-cut or other methods.

[0468] As illustrated in FIG. 34F, P+ strip 3412, N+ strip 3414, P- strip 3408, N- strip 3410, remaining N+ strip 3404', and remaining P+ strip 3406' have been layer transferred to acceptor wafer 3411. The top surface of N+ strip 3404' and P+ strip 3406' may be chemically or mechanically polished. Now transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer 3411 alignment marks (not shown). For illustration clarity, the oxide layers, such as, for example, oxide layer 3418, used to facilitate the wafer to wafer bond are not shown.

[0469] As illustrated in FIG. 34G, the substrate P+ body tie 3412 and substrate N+ body tie 3414 contact opening 3430 and partial transistor isolation may be soft or hard mask defined and then etched thru N+ strips 3404', P- strips 3408, P+ strips 3406', and N- strips 3410. This forms N+ regions 3424, P+ regions 3426, P- regions 3428, and N- regions 3420. The acceptor metal connect strip 3480 as previously discussed in FIG. 33D is shown. The doping concentration of the N- regions 3420 and P- regions 3428 may include gradients of concentration or layers of differing doping concentrations.

[0470] As illustrated in FIG. 34H, the transistor isolation may be formed by mask defining and then etching shallow P+ strips 3412 and N+ strips 3414 to substantially the top of acceptor wafer 3411, forming P+ substrate tie regions 3432, N+ substrate tie regions 3434, and transistor isolation regions 3455. Then a low-temperature gap fill oxide 3454 may be deposited and chemically mechanically polished. A thin pol-

ish stop layer 3422, such as, for example, low temperature silicon nitride with a thin oxide buffer layer, may then be deposited.

[0471] As illustrated in FIG. 34I, NMOS source region 3462, NMOS drain region 3463, and NMOS self-aligned gate opening region 3466 may be defined by masking and etching the thin polish stop layer 3422 and then followed by a sloped N+ etch of N+ region 3424 and may continue into P- region 3428. The sloped (30-90 degrees, 45 is shown) etch or etches may be accomplished with wet chemistry or plasma/RIE etching techniques. This process forms NMOS sloped source and drain extensions 3468. Then PMOS source region 3464, PMOS drain region 3465, PMOS self-aligned gate opening region 3467 may be defined by masking and etching the thin polish stop layer 3422 and then followed by a sloped P+ etch of P+ region 3426 and may continue into N- region 3420. The sloped (30-90 degrees, 45 is shown) etch or etches may be accomplished with wet chemistry or plasma/RIE etching techniques. This process forms PMOS sloped source and drain extensions 3469. The above two masked etches may form thin polish stop layer regions 3422'.

[0472] As illustrated in FIG. 34J, a gate dielectric 3471 may be formed and a gate electrode material 3470 may be deposited. The gate dielectric 3471 may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate electrode material 3470 in the industry standard high k metal gate process schemes described previously. Or the gate dielectric 3471 may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode material 3470 such as, for example, tungsten or aluminum may be deposited. The gate oxides and gate metals may be different between the NMOS and PMOS V-groove devices, and may be accomplished with selective removal of one gate oxide/metal pair type and replacement with another gate oxide/metal pair type.

[0473] As illustrated in FIG. 34K, the gate electrode material 3470 and gate dielectric 3471 may be chemically mechanically polished with the polish stop in the polish stop layer regions 3422'. The gate electrode material regions 3470' and gate dielectric regions 3471' may thus be remaining in the intended V-groove. Remaining polish stop regions 3423 are shown.

[0474] As illustrated in FIG. 34L, a low temperature thick oxide 3478 may be deposited and NMOS source contact 3441, NMOS gate contact 3442, NMOS drain contact 3443, substrate P+ body tie contact 3444, PMOS source contact 3445, NMOS gate contact 3446, NMOS drain contact 3447, substrate N+ body tie contact 3448, and thru layer via 3460 openings may be masked and etched preparing the transistors to be connected via metallization. The thru layer via 3460 provides electrical connection among the donor wafer transistors and the acceptor metal connect strip 3480.

[0475] This flow enables the formation of planar V-groove NMOS and PMOS transistors constructed by layer transfer of wafer sized doped strips of mono-crystalline silicon and may be connected to an underlying multi-metal layer semiconductor device without exposing it to a high temperature (above approximately 400° C.) process step.

[0476] Persons of ordinary skill in the art will appreciate that while the transistors fabricated in FIGS. 34A through 34L are shown with their conductive channels oriented in a north-south direction and their gate electrodes oriented in an east-west direction for clarity in explaining the simultaneous

fabrication of P-channel and N-channel transistors, that other orientations and organizations may be possible. Such skilled persons will further appreciate that the transistors may be rotated 90° with their gate electrodes oriented in a north-south direction. For example, it will be evident to such skilled persons that transistors aligned with each other along an east-west strip or row can either be electrically isolated from each other with Low-Temperature gap fill Oxide 3454 or share source and drain regions and contacts as a matter of design choice. Such skilled persons will also realize that strips or rows of 'n' type transistors may contain multiple N-channel transistors aligned in a north-south direction and strips or rows of 'p' type transistors may contain multiple P-channel transistors aligned in a north-south direction, specifically to form back-to-back sub-rows of P-channel and N-channel transistors for efficient logic layouts in which adjacent sub-rows of the same type share power supply lines and connections. Such skilled persons will also realize that a variation of the p & n well strip donor wafer preprocessing above may be to also preprocess the well isolations with shallow trench etching, dielectric fill, and CMP prior to the layer transfer and that there may be many process flow arrangements and sequences to form the donor wafer stacked strips prior to the layer transfer to the acceptor wafer. Such skilled persons will also realize that a similar flow may be utilized to construct CMOS versions of other types of transistors, such as, for example, RCAT, S-RCAT, and junction-less. Many other design choices are possible within the scope of the invention and will suggest themselves to such skilled persons, thus the invention is to be limited only by the appended claims.

[0477] As illustrated in FIGS. 35A to 35M, an n-channel 4-sided gated junction-less transistor (JLT) may be constructed that may be suitable for 3D IC manufacturing. As illustrated in FIG. 35A, an N- substrate donor wafer 3500A may be processed to include a wafer sized layer of N+ doping 3504A. The N+ doped layer 3504A may be formed by ion implantation and thermal anneal. A screen oxide 3501A may be grown before the implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. The N+ doped layer 3504A may alternatively be formed by epitaxial growth of a doped silicon layer of N+ or may be a deposited layer of heavily N+ doped poly-crystalline silicon. The N+ doped layer 3504A may be formed by doping the N- substrate donor wafer 3500A by Plasma Assisted Doping (PLAD) techniques. These processes may be done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done.

[0478] As illustrated in FIG. 35B, the top surface of N- substrate donor wafer 3500A may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the N+ doped layer 3504A to form oxide layer 3502A, or a re-oxidation of implant screen oxide 3501A to form oxide layer 3502A. A layer transfer demarcation plane 3599 (shown as a dashed line) may be formed in N- substrate donor wafer 3500A or N+ doped layer 3504A (shown) by hydrogen implantation 3506 or other methods as previously described.

[0479] As illustrated in FIG. 35C, an acceptor wafer 3500 may be prepared in an identical manner as the N- substrate donor wafer 3500A as described related to FIG. 35A, thus forming N+ layer 3504 and oxide layer 3502. Both the N- substrate donor wafer 3500A (flipped upside down and on

'top') and acceptor wafer **3500** (bottom') may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) or high temperature bonded. Alternatively, N+ layer **3504** may be formed with conventional doped poly-crystalline silicon material that may be optically annealed to form large grains.

[0480] As illustrated in FIG. 35D, the portion of the N+ layer **3504A** and the N- substrate donor wafer **3500A** that may be above the layer transfer demarcation plane **3599** may be removed by cleaving and polishing, or other low or high temperature processes as previously described, such as, for example, ion-cut or other methods. The remaining N+ layer **3504A'** may have been layer transferred to acceptor wafer **3500**. The top surface of N+ layer **3504A'** may be chemically or mechanically polished and may be thinned to the desired thickness. The thin doped silicon N+ layer **3504A'** may be on the order of about 5 nm to about 40 nm thick and may eventually form the transistor channel that may be gated on four sides. The two 'half' gate oxides **3502** and **3502A** may now be atomically bonded together to form the gate oxide **3512**, which may eventually become the top gate oxide of the junction-less transistor. A high temperature anneal may be performed to remove any residual oxide or interface charges.

[0481] Now strips of transistor channels may be formed with processing temperatures higher than approximately 400° C. as necessary. As illustrated in FIG. 35E, a thin oxide may be grown or deposited, or formed by liquid oxidants such as, for example, 350° C. sulfuric peroxide to protect the thin transistor N+ layer **3504A'** top from contamination. Then parallel strips of repeated pitch (the repeat pitch distance may include space for future isolation and other device structures) of the thin N+ layer **3504A'** may be formed by conventional masking, etching, and then photoresist removal, thus creating eventual transistor channel strips **3514**. The thin masking oxide, if present, may then be striped in a dilute hydrofluoric acid (HF) solution.

[0482] As illustrated in FIG. 35F, a conventional thermal gate oxide **3516** may be grown and poly-crystalline or amorphous silicon **3518**, doped or undoped, may be deposited. Alternatively, a high-k metal gate (HKMG) process may be employed as previously described. The poly-crystalline silicon **3518** may be chemically mechanically polished (CMP'ed) flat and a thin oxide **3520** may be grown or deposited to prepare the acceptor wafer **3500** for low temperature oxide bonding.

[0483] As illustrated in FIG. 35G, a layer transfer demarcation plane **3599G** (shown as a dashed line) may be formed in now donor wafer **3500** or N+ layer **3504** (shown) by hydrogen implantation **3506** or other methods as previously described.

[0484] As illustrated in FIG. 35H, both the now donor wafer **3500** and acceptor wafer **3510** top layers and surfaces may be prepared for wafer bonding as previously described and then aligned to the acceptor wafer **3510** alignment marks (not shown) and low temperature (less than approximately 400° C.) bonded. The portion of the N+ layer **3504** and the now donor wafer **3500** that may be above the layer transfer demarcation plane **3599** may be removed by cleaving and polishing, or other low temperature processes as previously described, such as, for example, ion-cut or other methods. The acceptor wafer metal interconnect strip **3580** is illustrated.

[0485] FIG. 35I is a top view at the same step as FIG. 35H with cross-sectional views I and II. The N+ layer **3504** and the

top gate oxide **3512** form the gate of one side of the transistor channel strip **3514**, and the bottom and side gate oxide **3516** with poly-crystalline silicon bottom and side gates **3518** gate the other three sides of the transistor channel strip **3514**. The acceptor wafer **3510** may have a top oxide layer that may encase the acceptor metal interconnect strip **3580**.

[0486] As illustrated in FIG. 35J, a polish stop layer **3526** of a material such as, for example, oxide and silicon nitride may be deposited on the top surface of the wafer. Isolation openings **3528** may be masked and then etched to the depth of the acceptor wafer **3510** top oxide layer **3524**. The isolation openings **3528** may be filled with a low temperature gap fill oxide, and chemically and mechanically polished (CMP'ed) flat. This may fully isolate the transistors from each other.

[0487] As illustrated in FIG. 35K, the top gate **3530** may be masked and then etched. The etched openings may then be filled with a low temperature gap fill oxide **3529** by deposition, and chemically and mechanically (CMP'ed) polished flat. Then an additional oxide layer, shown merged with and labeled as **3529**, may be deposited to enable interconnect metal isolation. As illustrated in FIG. 35L the contacts may be masked and etched. The gate contact **3532** may be masked and etched, so that the contact etches through the top gate **3530**, and during the metal opening mask and etch processes the gate oxide **3512** may be etched and the top gate **3530** and bottom and side gates **3518** may be connected together. The contacts **3534** to the two terminals of the transistor channel strip **3514** may be masked and etched. Then the thru layer vias **3560** (TLV **3536** in some views) to acceptor wafer **3510** metal interconnect strip **3580** may be masked and etched.

[0488] As illustrated in FIG. 35M, metal lines **3540** may be mask defined and etched, filled with barrier metals and copper interconnect, and CMP'ed in a typical metal interconnect scheme. This may substantially complete the contact via **3532** simultaneous coupling to the top gate **3530** and bottom and side gates **3518** for the 4-sided gate connection. The two transistor channel terminal contacts (source and drain) **3534** independently connect to the transistor channel strip **3514** on each side of the top gate **3530**. The thru via **3560** electrically couples the transistor layer metallization to the acceptor wafer **3510** at acceptor wafer metal connect strip **3580**.

[0489] This flow enables the formation of a mono-crystalline silicon channel 4-sided gated junction-less transistor that may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

[0490] A p channel 4-sided gated JLT may be constructed as above with the N+ layer **3504A** formed as P+ doped, and the gate metals of bottom and side gates **3518** and top gates **3530** may be of appropriate work function to shutoff the p channel at a gate voltage of zero, such as, for example, heavily doped N+ silicon.

[0491] The following sections discuss some embodiments of the invention wherein wafer or die-sized sized pre-formed repeating device structures may be transferred and then may be processed to create 3D ICs.

[0492] An embodiment of the invention is to pre-process a donor wafer by forming wafer-sized or die-sized layers of pre-formed repeating device structures without a process temperature restriction, then layer transferring the pre-processed donor wafer to the acceptor wafer, and processing with either low temperature (below approximately 400° C.) or high temperature (greater than approximately 400° C.) after the layer transfer to form device structures, such as, for

example, transistors, on or in the donor wafer that may be physically aligned and may be electrically coupled to the acceptor wafer. Methods are described to build both 'n' type and 'p' type transistors on the same layer by partially processing the first phase of transistor formation on the donor wafer with typical CMOS processing including a 'dummy gate', a process known as 'gate-last'. The 'gate last' process flow may be referred to as a gate replacement process or a replacement gate process. In various embodiments of the invention, a layer transfer of the mono-crystalline silicon may be performed after the dummy gate is formed and before the formation of a replacement gate. The dummy gate and the replacement gate may include various materials such as, for example, silicon and silicon dioxide, or metal and low k materials such as, for example, TiAlN and HfO<sub>2</sub>. An example may be the high-k metal gate (HKMG) CMOS transistors that have been developed for the 45 nm, 32 nm, 22 nm, and future CMOS generations. Intel and TSMC have shown the utility of a 'gate-last' approach to construct high performance HKMG CMOS transistors (C. Auth et al., VLSI 2008, pp 128-129 and C. H. Jan et al, 2009 IEDM p. 647). The donor wafer and acceptor wafer in these discussions may include the compositions, such as metal layers and TLVs, referred to for donor wafers and acceptor wafers in the FIGS. 1, 2 and 3 layer transfer discussions.

[0493] FIGS. 36A to 36H describe an overall process flow wherein CMOS transistors may be partially processed on a donor wafer, temporarily transferred to a carrier or holder substrate or wafer and thinned, layer transferred to an acceptor substrate, and then the transistor and interconnections may be substantially completed in low temperature (below approximately 400° C.).

[0494] As illustrated in FIG. 36A, a donor wafer 3600 may be processed in the typical state of the art HKMG gate-last manner up to the step prior to where CMP exposure of the poly-crystalline silicon dummy gates takes place. The donor wafer 3600 may be a bulk mono-crystalline silicon wafer (shown), or a Silicon On Insulator (SOI) wafer, or a Germanium on Insulator (GeOI) wafer. Donor wafer 3600, the shallow trench isolation (STI) 3602 among transistors, the poly-crystalline silicon 3604 and gate oxide 3605 of both n-type and p-type CMOS dummy gates, their associated source and drains 3606 for NMOS and 3607 for PMOS, and the inter-layer dielectric (ILD) 3608 are shown in the cross section illustration. These structures of FIG. 36A illustrate substantial completion of the first phase of transistor formation.

[0495] As illustrated in FIG. 36B, a layer transfer demarcation plane (shown as dashed line) 3699 may be formed by hydrogen implantation 3609 or other methods as previously described.

[0496] As illustrated in FIG. 36C, donor wafer 3600 with the first phase of transistor formation substantially completed may be temporarily bonded to carrier or holder substrate 3614 at interface 3616 with a low temperature process that may facilitate a low temperature release. The carrier or holder substrate 3614 may be a glass substrate to enable state of the art optical alignment with the acceptor wafer. A temporary bond among the carrier or holder substrate 3614 and the donor wafer 3600 at interface 3616 may be made with a polymeric material, such as, for example, polyimide DuPont HD3007, which can be released at a later step by laser ablation, Ultra-Violet radiation exposure, or thermal decomposition. Alternatively, a temporary bond may be made with uni-polar or

bi-polar electrostatic technology such as, for example, the Apache tool from Beam Services Inc.

[0497] As illustrated in FIG. 36D, the portion of the donor wafer 3600 that may be below the layer transfer demarcation plane 3699 may be removed by cleaving or other processes as previously described, such as, for example, ion-cut or other methods. The remaining donor wafer regions 3601 and 3601' may be thinned by chemical mechanical polishing (CMP) so that the transistor STI 3602 may be exposed at the donor wafer surface 3618. Alternatively, the CMP could continue to the bottom of the junctions to eventually create fully depleted SOI transistors. The donor wafer 3600 may now also be processed and reused for more layer transfers.

[0498] As illustrated in FIG. 36E, oxide 3620 may be deposited on the remaining donor wafer 3601 surface 3618. Both the donor wafer surface 3618 and acceptor substrate 3610 may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) aligned and bonded at surface 3622. With reference to the FIG. 33D discussion, acceptor wafer metal connect strip 3624 is shown.

[0499] As illustrated in FIG. 36F, the carrier or holder substrate 3614 may then be released at interface 3616 using a low temperature process such as, for example, laser ablation. The bonded combination of acceptor substrate 3610 and first phase substantially completed HKMG CMOS transistor tier 3650 may now be ready for typical state of the art gate-last transistor formation completion.

[0500] As illustrated in FIG. 36G, the inter layer dielectric 3608 may be chemical mechanically polished to expose the top of the poly-crystalline silicon dummy gates and create interlayer dielectric regions 3608'. The dummy poly-crystalline silicon gates 3604 may then be removed by etching and the hi-k gate dielectric 3626 and the PMOS specific work function metal gate 3628 may be deposited. The PMOS work function metal gate may be removed from the NMOS transistors and the NMOS specific work function metal gate 3630 may be deposited. An aluminum fill may be performed on both NMOS and PMOS gates 3632 and the metal chemical mechanically polished. For illustration clarity, the oxide layers used to facilitate the wafer to wafer bond are not shown.

[0501] As illustrated in FIG. 36H, a low temperature dielectric layer 3633 may be deposited and the typical gate 3634 and source/drain 3636 contact formation and metallization may now be performed to connect to and among the PMOS & NMOS transistors. Thru layer via (TLV) 3640 may be lithographically defined, plasma/RIE etched, and metallization formed. TLV 3640 electrically couples the transistor layer metallization to the acceptor substrate 3610 at acceptor wafer metal connect strip 3624.

[0502] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 36A through 36H are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the top metal layer may be formed to act as the acceptor wafer landing strips for a repeat of the above process flow to stack another preprocessed thin mono-crystalline layer of two-phase formed transistors. Additionally, the above process flow may also be utilized to construct gates of other types, such as, for example, doped poly-crystalline silicon on thermal oxide, doped poly-crystalline silicon on oxynitride, or other metal gate configurations, as 'dummy gates,' perform a layer transfer of the thin mono-crystalline layer, replace the gate electrode and gate oxide, and then proceed with low



temperature interconnect processing. Moreover, other transistor types may be possible, such as, for example, RCAT and junction-less. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the scope of the invention is to be limited only by the appended claims.

[0503] With reference to the discussion of FIGS. 36A to 36H, FIGS. 37A to 37G describe a process flow wherein CMOS transistors may be partially processed on a donor wafer, which may be temporarily bonded and transferred to a carrier or holder wafer, after which it may be cleaved, thinned and planarized before being layer transferred to an acceptor substrate. After bonding to the acceptor substrate, the temporary carrier or holder wafer may be removed, the surface planarized, and then the transistor and interconnections may be substantially completed with low temperature (below approximately 400° C.) processes. State of the art CMOS transistors may be constructed with methods that may be suitable for 3D IC manufacturing.

[0504] As illustrated in FIG. 37A, a donor wafer 3706 may be processed in the typical state of the art HKMG gate-last manner up to the step prior to where CMP exposure of the poly-crystalline silicon dummy gates takes place. The donor wafer 3706 may be a bulk mono-crystalline silicon wafer (shown), or a Silicon On Insulator (SOI) wafer, or a Germanium on Insulator (GeOI) wafer. Donor wafer 3706 and CMOS dummy gates 3702 are shown in the cross section illustration. These structures of FIG. 37A illustrate substantial completion of the first phase of transistor formation.

[0505] As illustrated in FIG. 37B, a layer transfer demarcation plane (shown as dashed line) 3799 may be formed in donor wafer 3706 by hydrogen implantation 3716 or other methods as previously described. Both the donor wafer 3706 top surface and carrier or holder silicon wafer 3726 may be prepared for wafer bonding as previously described.

[0506] As illustrated in FIG. 37C, donor wafer 3706 with the first phase of transistor formation substantially completed may be permanently bonded to carrier or holder silicon wafer 3726 and may utilize oxide to oxide bonding.

[0507] As illustrated in FIG. 37D, the portion of the donor wafer 3706 that may be above the layer transfer demarcation plane 3799 may be removed by cleaving or other processes as previously described, such as, for example, ion-cut or other methods. The remaining donor wafer 3706' may be thinned by chemical mechanical polishing (CMP). Thus dummy gates 3702 and associated remaining donor wafer 3706' may be transferred and permanently bonded to carrier or holder silicon wafer 3726.

[0508] As illustrated in FIG. 37E, a thin layer of oxide 3732 may be deposited on the remaining donor wafer 3706' open surface. A layer transfer demarcation plane (shown as dashed line) 3798 may be formed in carrier or holder silicon wafer 3726 by hydrogen implantation 3746 or other methods as previously described.

[0509] As illustrated in FIG. 37F, carrier or holder silicon wafer 3726, with layer transfer demarcation plane (shown as dashed line) 3798, dummy gates 3702, oxide 3732, and remaining donor wafer 3706' may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) aligned and bonded to acceptor substrate 3710. Acceptor substrate 3710 may include pre-made circuitry as described previously, top oxide layer 3711, and acceptor wafer metal connect strip 3780.

[0510] As illustrated in FIG. 37G, the portion of the carrier or holder silicon wafer 3726 that may be above the layer transfer demarcation plane 3798 may be removed by cleaving or other processes as previously described, such as, for example, ion-cut or other methods. The remaining carrier or holder material may be removed by chemical mechanical polishing (CMP) or a wet etchant, such as, for example, Potassium Hydroxide (KOH). A second CMP may be performed to expose the top of the dummy gates 3702. The bonded combination of acceptor substrate 3710 and first phase substantially completed HKMG CMOS transistor tier including dummy gates 3702 and remaining donor wafer 3706' may now be ready for typical state of the art gate-last transistor formation completion as described previously with reference to FIGS. 36G and 36H.

[0511] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 37A through 37G are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the carrier or holder wafer may be composed of some other material than mono-crystalline silicon, or the top metal layer may be formed to act as the acceptor wafer landing strips for a repeat of the above process flow to stack another preprocessed thin mono-crystalline layer of two-phase formed transistors. Additionally, the above process flow may also be utilized to construct gates of other types, such as, for example, doped poly-crystalline silicon on thermal oxide, doped poly-crystalline silicon on oxynitride, or other metal gate configurations, as 'dummy gates,' perform a layer transfer of the thin mono-crystalline layer, replace the gate electrode and gate oxide, and then proceed with low temperature interconnect processing. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the scope of the invention is to be limited only by the appended claims.

[0512] FIGS. 38A to 38E illustrate an overall process flow similar to FIG. 36 wherein CMOS transistors may be partially processed on a donor wafer, temporarily transferred to a carrier or holder substrate and thinned, a double or back-gate may be processed, layer transferred to an acceptor substrate, and then the transistor and interconnections may be substantially completed in low temperature (below approximately 400° C.). This may provide a back-gated transistor (double gated) in a face-up process flow. State of the art CMOS transistors may be constructed with methods that may be suitable for 3D IC manufacturing.

[0513] As illustrated in FIG. 38A, planar CMOS dummy gate transistors may be processed as described in FIGS. 36A, 36B, 36C, and 36D. Carrier or holder substrate 3614, bonding interface 3616, inter layer dielectric (ILD) 3608, shallow trench isolation (STI) regions 3602 and remaining donor wafer regions 3601 and 3601' are shown. These structures illustrate substantial completion of the first phase of transistor formation. A second gate dielectric 3802 may be grown or deposited and second gate metal material 3804 may be deposited. The gate dielectric 3802 and second gate metal material 3804 may be formed with low temperature (approximately less than 400° C.) materials and processing, such as, for example, previously described TEL SPA gate oxide and amorphous silicon, ALD techniques, or hi-k metal gate stack (HKMG), or may be formed with a higher temperature gate oxide or oxynitride and doped poly-crystalline silicon if the carrier or holder substrate bond may be permanent and the

dopant movement or diffusion in the underlying transistors may be accounted or compensated for.

**[0514]** As illustrated in FIG. 38B, the gate stacks may be lithographically defined and plasma/RIE etched removing second gate metal material **3804** and gate dielectric **3802** leaving second transistor gates **3806** and associated gate dielectrics **3802'** remaining. Inter layer dielectric **3808** may be deposited and planarized, and then second gate contacts **3811** and partial thru layer via **3812** and associated metallization **3816** may be conventionally formed.

**[0515]** As illustrated in FIG. 38C, oxide layer **3820** may be deposited on the carrier or holder substrate with processed donor wafer surface for wafer bonding and electrical isolation of the metallization **3816** purposes. Both oxide layer **3820** surface and acceptor substrate **3810** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) aligned and bonded. Acceptor wafer metal connect strip **3880** is shown.

**[0516]** As illustrated in FIG. 38D, the carrier or holder substrate **3614** may then be released at interface **3616** using a low temperature process such as, for example, laser ablation. The bonded combination of acceptor substrate **3610** and first phase substantially completed HKMG CMOS transistors may now be ready for typical state of the art gate-last transistor formation completion. The inter layer dielectric **3608** may be chemical mechanically polished to expose the top of the poly-crystalline silicon dummy gates and create interlayer dielectric regions **3608'**.

**[0517]** As illustrated in FIG. 38E, the dummy poly-crystalline silicon gates may then be removed by etching and the hi-k gate dielectric **3826** and the PMOS specific work function metal gate **3828** may be deposited. The PMOS work function metal gate may be removed from the NMOS transistors and the NMOS specific work function metal gate **3830** may be deposited. An aluminum fill may be performed and the metal chemical mechanically polished to create NMOS gate **3852** and PMOS gate **3850**. A low temperature dielectric layer **3832** may be deposited and the typical gate contact **3834** and source/drain contact **3836** formation and associated metallization may now be performed to connect to and among the PMOS & NMOS transistors. Thru layer via (TLV) **3822** may be lithographically defined, plasma/RIE etched, and metallization formed to connect to partial thru layer via **3812**. TLV **3840** may be lithographically defined, plasma/RIE etched, and metallization formed to electrically couple the transistor layer metallization to the acceptor substrate **3810** via acceptor wafer metal connect strip **3880**. The PMOS transistor may be back-gated by connecting the PMOS gate **3850** to the bottom gate thru gate contact **3834** to metal line **3837** and to partial thru layer via **3812** and TLV **3822**. The NMOS transistor may be back biased by connecting metal line metallization **3816** to a back bias circuit that may be in the top transistor level or in the acceptor substrate **3810**.

**[0518]** Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 38A through 38E are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the above process flow may also be utilized to construct gates of other types, such as, for example, doped poly-crystalline silicon on thermal oxide, doped poly-crystalline silicon on oxynitride, or other metal gate configurations, as 'dummy gates,' perform a layer transfer of the thin mono-crystalline layer, replace the gate electrode and gate oxide, and then proceed with low temperature interconnect

processing. Such skilled persons will further appreciate that the above process flow may be utilized to create fully depleted SOI transistors, or junction-less, or RCATs. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the scope of the invention is to be limited only by the appended claims.

**[0519]** FIGS. 39A to 39D describe an overall process flow wherein CMOS transistors may be partially processed on a donor wafer, ion implanted for later cleaving, transistors and some interconnect substantially completed, then layer transferred to an acceptor substrate, donor cleaved and thinned, back-gate processing, and then interconnections may be substantially completed. This provides a back-gated transistor (double gated) in a transistor 'face-down' process flow. State of the art CMOS transistors may be constructed with methods that may be suitable for 3D IC manufacturing.

**[0520]** As illustrated in FIG. 39A, planar CMOS dummy gate transistors may be processed as described in FIGS. 36A and 36B. The dummy gate transistors may now be ready for typical state of the art gate-last transistor formation completion. The inter layer dielectric may be chemical mechanically polished to expose the top of the poly-crystalline silicon dummy gates and create interlayer dielectric regions **3608'**. The dummy gates may then be removed by etching and the hi-k gate dielectric **3626** and the PMOS specific work function metal gate **3628** may be deposited. The PMOS work function metal gate may be removed from the NMOS transistors and the NMOS specific work function metal gate **3630** may be deposited. An aluminum fill may be performed and the metal chemical mechanically polished to create NMOS and PMOS gates **3632**. Thus donor wafer **3600**, layer transfer demarcation plane (shown as dashed line) **3699**, shallow trench isolation (STI) regions **3602**, interlayer dielectric regions **3608'**, hi-k gate dielectric **3626**, PMOS specific work function metal gate **3628**, NMOS specific work function metal gate **3630**, and NMOS and PMOS gates **3632** are shown.

**[0521]** As illustrated in FIG. 39B, a low temperature dielectric layer **3932** may be deposited and the typical gate **3934** and source/drain **3936** contact formation and metallization may now be performed to connect to and among the PMOS & NMOS transistors. Partial top to bottom via **3940** may be lithographically defined, plasma/RIE etched into STI isolation region **3982**, and metallization formed.

**[0522]** As illustrated in FIG. 39C, oxide layer **3904** may be deposited on the processed donor wafer **3600** surface **3902** for wafer bonding and electrical isolation of the metallization purposes.

**[0523]** As illustrated in FIG. 39D, oxide layer **3904** surface **3906** and acceptor substrate **3910** may be prepared for wafer bonding as previously described and then donor wafer **3600** may be aligned to the acceptor substrate **3610** and they may be bonded at a low temperature (less than approximately 400° C.). Acceptor wafer metal connect strip **3980** and the STI isolation **3930** where the future thru layer via (TLV) may be formed is shown.

**[0524]** As illustrated in FIG. 39E, the portion of the donor wafer **3600** that may be above the layer transfer demarcation plane **3699** may be removed by cleaving or other processes as previously described, such as, for example, ion-cut or other methods. The remaining donor wafer regions **3601** and **3601'** may be thinned by chemical mechanical polishing (CMP) so that the transistor STI regions **3982** and **3930** may be exposed

at the donor wafer face **3919**. Alternatively, the CMP could continue to the bottom of the junctions to eventually create fully depleted SOI transistors as may be discussed later with reference to FIG. **39F-2**.

[**0525**] As illustrated in FIG. **39F**, a low-temperature oxide or low-k dielectric **3936** may be deposited and planarized. The thru layer via (TLV) **3928** may be lithographically defined and plasma/RIE etched. Contact **3941** may be lithographically defined and plasma/RIE etched to provide connection to partial top to bottom via **3940**. Metallization may be formed for interconnection purposes. Donor wafer to acceptor wafer electrical coupling may be provided by partial top to bottom via **3940** connecting to contact **3941** connecting to metal line **3950** connecting to thru layer via (TLV) **3928** connecting to acceptor metal strip **3980**.

[**0526**] The face down flow may have some potential advantages such as, for example, enabling double gate transistors, back biased transistors, 4 terminal transistors, or access to the floating body in memory applications.

[**0527**] As illustrated in FIG. **39E-1**, a back gate for a double gate transistor may be constructed. A second gate dielectric **3960** may be grown or deposited and second gate metal material **3962** may be deposited. The gate dielectric **3960** and second gate metal material **3962** may be formed with low temperature (approximately less than 400° C.) materials and processing, such as, for example, previously described TEL SPA gate oxide and amorphous silicon, ALD techniques, or hi-k metal gate stack (HKMG). The gate stacks may be lithographically defined and plasma/RIE etched.

[**0528**] As illustrated in FIG. **39F-1**, a low-temperature oxide or low-k dielectric **3936** may be deposited and planarized. The thru layer via (TLV) **3928** may be lithographically defined and plasma/RIE etched. Contacts **3941** and **3929** may be lithographically defined and plasma/RIE etched to provide connection to partial top to bottom via **3940** or to the second gate. Metallization may be formed for interconnection purposes. Donor wafer to acceptor wafer electrical connections may be provided by partial top to bottom via **3940** connecting to contact **3941** connecting to metal line **3950** connecting to thru layer via (TLV) **3928** connecting to acceptor metal strip **3980**. Back gate or double gate electrical coupling may be provided by PMOS gate **3632** connecting to gate contact **3933** connecting to metal line **3935** connecting to partial top to bottom via **3940** connecting to contact **3941** connecting to metal line **3951** connecting to contact **3929** connecting to back gate **3962**.

[**0529**] As illustrated in FIG. **39F-2**, fully depleted SOI transistors with P+ junctions **3970** and N+ junctions **3971** may be alternatively constructed in this flow. In the FIG. **39E** step description above, the CMP may be continued to the bottom of the junctions, thus creating fully depleted SOI transistors.

[**0530**] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **39A** through **39F-2** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the above process flow may also be utilized to construct gates of other types, such as, for example, doped poly-crystalline silicon on thermal oxide, doped poly-crystalline silicon on oxynitride, or other metal gate configurations, as 'dummy gates,' perform a layer transfer of the thin mono-crystalline layer, replace the gate electrode and gate oxide, and then proceed with low temperature interconnect processing. Such skilled persons will further appreciate that

the above process flow may be utilized to create junction-less transistors, or RCATs. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the scope of the invention is to be limited only by the appended claims.

[**0531**] FIGS. **40A** to **40J** describe an overall process flow utilizing a carrier wafer or a holder wafer wherein CMOS transistors may be processed on two sides of a donor wafer, NMOS on one side and PMOS on the other, and then the NMOS on top of PMOS donor wafer may be transferred to a target or acceptor substrate with pre-processed circuitry. State of the art CMOS transistors and compact 3D library cells may be constructed with methods that may be suitable for 3D IC manufacturing.

[**0532**] As illustrated in FIG. **40A**, a Silicon On Oxide (SOI) donor wafer substrate **4000** may be processed in the typical state of the art HKMG gate-last manner up to the step prior to where CMP exposure of the poly-crystalline silicon dummy gates takes place, but forming only NMOS transistors. SOI donor wafer substrate **4000**, the buried oxide (i.e., BOX) **4001**, the thin silicon layer **4002** of the SOI wafer, the shallow trench isolation (STI) **4003** among NMOS transistors, the poly-crystalline silicon **4004** and gate dielectric **4005** of the NMOS dummy gates, NMOS source and drains **4006**, the NMOS transistor channel **4007**, and the NMOS interlayer dielectric (ILD) **4008** are shown in the cross section illustration. These structures of FIG. **40A** illustrate the substantial completion of the first phase of NMOS transistor formation. The thermal cycles of the NMOS HKMG process may be adjusted to compensate for later thermal processing.

[**0533**] As illustrated in FIG. **40B**, a layer transfer demarcation plane (shown as dashed line) **4099** may be formed in SOI donor wafer substrate **4000** by hydrogen implantation **4010** or other methods as previously described.

[**0534**] As illustrated in FIG. **40C**, oxide **4016** may be deposited onto carrier or holder wafer **4020** and then both the SOI donor wafer substrate **4000** and carrier or holder wafer **4020** may be prepared for wafer bonding as previously described, and then may be permanently oxide to oxide bonded together at interface **4014**. Carrier or holder wafer **4020** may also be called a carrier or holder substrate, and may be composed of mono-crystalline silicon, or other materials.

[**0535**] As illustrated in FIG. **40D**, the portion of the SOI donor wafer substrate **4000** that may be below the layer transfer demarcation plane **4099** may be removed by cleaving or other processes as previously described, such as, for example, ion-cut or other methods. The remaining donor wafer layer **4000'** may be thinned by chemical mechanical polishing (CMP) and surface **4022** may be prepared for transistor formation.

[**0536**] As illustrated in FIG. **40E**, donor wafer layer **4000'** at surface **4022** may be processed in the typical state of the art HKMG gate last processing manner up to the step prior to where CMP exposure of the poly-crystalline silicon dummy gates takes place to form the PMOS transistors with dummy gates. The PMOS transistors may be precisely aligned at state of the art tolerances to the NMOS transistors as a result of the shared substrate possessing the same alignment marks. Carrier or holder wafer **4020**, oxide **4016**, BOX **4001**, the thin silicon layer **4002** of the SOI wafer, the shallow trench isolation (STI) **4003** among NMOS transistors, the poly-crystalline silicon **4004** and gate dielectric **4005** of the NMOS dummy gates, NMOS source and drains **4006**, the NMOS transistor channels **4007**, and the NMOS interlayer dielectric

(ILD) **4008**, donor wafer layer **4000'**, the shallow trench isolation (STI) **4033** among PMOS transistors, the poly-crystalline silicon **4034** and gate dielectric **4035** of the PMOS dummy gates, PMOS source and drains **4036**, the PMOS transistor channels **4037**, and the PMOS interlayer dielectric (ILD) **4038** are shown in the cross section illustration. A high temperature anneal may be performed to activate both the NMOS and the PMOS transistor dopants. These structures of FIG. **40E** illustrate substantial completion of the first phase of PMOS transistor formation.

[**0537**] As illustrated in FIG. **40F**, a layer transfer demarcation plane (shown as dashed line) **4098** may be formed in carrier or holder wafer **4020** by hydrogen implantation **4011** or other methods as previously described. The PMOS transistors may now be ready for typical state of the art gate-last transistor formation completion.

[**0538**] As illustrated in FIG. **40G**, the PMOS ILD **4038** may be chemical mechanically polished to expose the top of the PMOS poly-crystalline silicon dummy gates, composed of poly-crystalline silicon **4034** and gate dielectric **4035**, and the dummy gates may then be removed by etching. A hi-k gate dielectric **4040** and the PMOS specific work function metal gate **4041** may be deposited. An aluminum fill **4042** may be performed and the metal chemical mechanically polished. A low temperature dielectric layer **4039** may be deposited and the typical gate **4043** and source/drain **4044** contact formation and metallization may now be performed to connect to and among the PMOS transistors. Partially formed PMOS inter layer via (ILV) **4047** may be lithographically defined, plasma/RIE etched, and metallization formed. Oxide layer **4048** may be deposited to prepare for bonding.

[**0539**] As illustrated in FIG. **40H**, the donor wafer surface at oxide layer **4048** and top oxide surface of acceptor or target substrate **4088** with acceptor wafer metal connect strip **4050** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) aligned and oxide to oxide bonded at interface **4051**.

[**0540**] As illustrated in FIG. **40I**, the portion of the carrier or holder wafer **4020** that may be above the layer transfer demarcation plane **4098** may be removed by cleaving or other processes as previously described, such as, for example, ion-cut or other methods. The remaining layer of the carrier or holder wafer may be removed by chemical mechanical polishing (CMP) to or into oxide layer **4016**. The NMOS transistors may be now ready for typical state of the art gate-last transistor formation completion.

[**0541**] As illustrated in FIG. **40J**, oxide **4016** and the NMOS ILD **4008** may be chemical mechanically polished to expose the top of the NMOS dummy gates composed of poly-crystalline silicon **4004** and gate dielectric **4005**, and the dummy gates may then be removed by etching. A hi-k gate dielectric **4060** and an NMOS specific work function metal gate **4061** may be deposited. An aluminum fill **4062** may be performed and the metal chemical mechanically polished. A low temperature dielectric layer **4069** may be deposited and the typical gate **4063** and source/drain **4064** contact formation and metallization may now be performed to connect to and among the NMOS transistors. Partially formed NMOS inter layer via (ILV) **4067** may be lithographically defined, plasma/RIE etched, and metallization formed, thus electrically connecting NMOS ILV **4067** to PMOS ILV **4047**.

[**0542**] As illustrated in FIG. **40K**, oxide **4070** may be deposited and planarized. Thru layer via (TLV) **4072** may be lithographically defined, plasma/RIE etched, and metalliza-

tion formed. TLV **4072** electrically couples the NMOS transistor layer metallization to the acceptor or target substrate **4088** at acceptor wafer metal connect strip **4050**. A topmost metal layer, at or above oxide **4070**, of the layer stack illustrated may be formed to act as the acceptor wafer metal connect strips for a repeat of the above process flow to stack another preprocessed thin mono-crystalline silicon layer of NMOS on top of PMOS transistors.

[**0543**] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **40A** through **40K** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the transistor layers on each side of BOX **4001** may include full CMOS, or one side may be CMOS and the other n-type MOSFET transistors, or other combinations and types of semiconductor devices. Additionally, the above process flow may also be utilized to construct gates of other types, such as, for example, doped poly-crystalline silicon on thermal oxide, doped poly-crystalline silicon on oxynitride, or other metal gate configurations, as 'dummy gates,' perform a layer transfer of the thin mono-crystalline layer, replace the gate electrode and gate oxide, and then proceed with low temperature interconnect processing. Moreover, that other transistor types may be possible, such as, for example, RCAT and junction-less. Further, the donor wafer layer **4000'** in FIG. **40D** may be formed from a bulk mono-crystalline silicon wafer with CMP to the NMOS junctions and oxide deposition in place of the SOI wafer discussed. Additionally, the SOI donor wafer substrate **4000** may start as a bulk silicon wafer and utilize an oxygen implantation and thermal anneal to form a buried oxide layer, such as, for example, the SIMOX process (i.e., separation by implantation of oxygen), or SOI donor wafer substrate **4000** may be a Germanium on Insulator (GeOI) wafer. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the scope of the invention is to be limited only by the appended claims.

[**0544**] The challenge of aligning preformed or partially preformed planar transistors to the underlying layers and substrates may be overcome by the use of repeating structures on the donor wafer or substrate and the use of metal connect landing strips either on the acceptor wafer only or on both the donor and acceptor wafers. The metal connect landing strips may be formed with metals, such as, for example, copper or aluminum, and may include barrier metals, such as, for example, TiN or WCo. Repeating patterns in one direction, for example, North to South repeats of preformed structures may be accomplished with the alignment scheme and metal landing strips as described previously with reference to the FIG. **33**. The gate last HKMG process may be utilized to create a pre-processed donor wafer that builds not just one transistor type but both types by utilizing alternating parallel strips or rows that may be the die width plus maximum donor wafer to acceptor wafer misalignment in length.

[**0545**] As illustrated in FIG. **41** and with reference to FIG. **33**, the layout of the donor wafer formation into repeating strips and structures may be as follows. A four cardinal directions indicator **4140** may be used to assist the explanation. The width of the PMOS transistor strip width repeat  $W_p$  **4106** may be composed of two transistor isolations **4110** of width  $2F$  each, plus a PMOS transistor source **4112** of width  $2.5F$ , a PMOS gate **4113** of width  $F$ , and a PMOS transistor drain **4114** of width  $2.5F$ . The total  $W_p$  **4106** may be  $10F$ , where  $F$  may be 2 times lambda, the minimum design rule. The width

of the NMOS transistor strip width repeat  $W_n$  4104 may be composed of two transistor isolations 4110 of width  $2F$  each, plus a NMOS transistor source 4116 of width  $2.5F$ , a NMOS gate 4117 of width  $F$ , and a NMOS transistor drain 4118 of width  $2.5F$ . The total  $W_n$  4104 may be  $10F$  where  $F$  may be 2 times  $\lambda$ , the minimum design rule. The pattern repeat  $W$  4108, which may include one  $W_n$  4104 and one  $W_p$  4106, may be  $20F$  and may be oriented in the North to South direction for this example.

[0546] As illustrated in FIG. 42A, the top view of one pattern repeat  $W$  4108 layout (ref FIG. 41) and cross sectional view of acceptor wafer 4210 after layer transfer of the first phase of HKMG transistor formation, layer transfer & bonding of the thin mono-crystalline preprocessed donor layer to the acceptor wafer, and release of the bonded structure from the carrier or holder substrate, as previously described in FIGS. 36A to 36F, are shown. Interlayer dielectric (ILD) 4208, the NMOS poly-crystalline silicon 4204 and NMOS gate oxide 4205 of NMOS dummy gate (NMOS gate 4117 strip), the PMOS poly-crystalline silicon 4204' and PMOS gate oxide 4205' of PMOS dummy gate (PMOS gate 4113 strip), NMOS source 4206 (NMOS transistor source 4116 strip), NMOS drain 4206' (NMOS transistor drain 4118 strip), PMOS source 4207 (PMOS transistor source 4112 strip), PMOS drain 4207' (PMOS transistor drain 4114 strip), remaining donor wafer regions 4201 and 4201', the shallow trench isolation (STI) 4202 among transistors (transistor isolation 4110 strips), oxide 4220, and acceptor metal connect strip 4224 are shown in the cross sectional illustration.

[0547] As illustrated in FIG. 42B, the inter layer dielectric 4208 may be chemical mechanically polished to expose the top of the poly-crystalline silicon dummy gates and create interlayer dielectric regions 4208'. Partial thru layer via (TLV) 4240 may be lithographically defined, plasma/RIE etched, and metallization formed to couple with acceptor metal connect strip 4224.

[0548] As illustrated in FIG. 42C, the long strips or rows of pre-formed transistors may be lithographically defined and plasma/RIE etched into desired transistor lengths or segments by forming isolation regions 4252. A low temperature oxidation may be performed to repair damage to the transistor edge and regions and isolation regions 4252 may be filled with a low temperature gap fill dielectric and planarized with CMP.

[0549] As illustrated in FIG. 42D, the dummy poly-crystalline silicon gates 4204 may then be removed by etching and the hi-k gate dielectric 4226 and the PMOS specific work function metal gate 4228 may be deposited. The PMOS work function metal gate may be removed from the NMOS transistors and the NMOS specific work function metal gate 4230 may be deposited. An aluminum fill 4232 may be performed on both NMOS and PMOS gates and the metal chemical mechanically polished but not fully remove the aluminum fill 4232 and planarize the surface for the gate definition

[0550] As illustrated in FIG. 42E, the replacement gates 4255 may be lithographically defined and plasma/RIE etched and may provide a gate contact landing area 4258 on isolation region 4252.

[0551] As illustrated in FIG. 42F, a low temperature dielectric layer 4233 may be deposited and the typical gate 4257, source 4262, and drain 4264 contact formation and metallization may now be performed. Top partial TLV 4241 may be lithographically defined, plasma/RIE etched, and metallization formed to electrically couple with the previously formed

partial TLV 4240. Thus electrical connection from the donor wafer formed transistors to the acceptor wafer circuitry may be made.

[0552] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 42A through 42F are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the top metal layer may be formed to act as the acceptor wafer landing strips for a repeat of the above process flow to stack another preprocessed thin mono-crystalline layer of two-phase formed transistors. Or, the above process flow may also be utilized to construct gates of other types, such as, for example, doped poly-crystalline silicon on thermal oxide, doped poly-crystalline silicon on oxynitride, or other metal gate configurations, as 'dummy gates,' perform a layer transfer of the thin mono-crystalline layer, replace the gate electrode and gate oxide, and then proceed with low temperature interconnect processing. Or that other transistor types may be possible, such as, for example, RCAT and junction-less. Or that additional arrangement of transistor strips may be constructed on the donor wafer such as, for example, NMOS/NMOS/PMOS, or PMOS/PMOS/NMOS. Or that the direction of the transistor strips may be in a different than illustrated, such as, for example, East to West. Or that the partial TLV 4240 could be formed in various ways, such as, for example, before the CMP of dielectric 4208. Or, isolation regions 4252 may be selectively opened and filled with specific inter layer dielectrics for the PMOS and NMOS transistors separately so to provide specific compressive or tensile stress enhancement to the transistor channels for carrier mobility enhancement. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the scope of the invention is to be limited only by the appended claims.

[0553] An embodiment of the invention is to pre-process a donor wafer by forming repeating wafer-sized or die-sized strips of layers of various materials that repeat in two directions, such as, for example, orthogonal to each other, for example a North to South repeat combined with an East to West repeat. These repeats of preformed structures may be constructed without a process temperature restriction, then layer transferring the pre-processed donor wafer to the acceptor wafer, and processing with either low temperature (below approximately  $400^\circ\text{C}$ .) or high temperature (greater than approximately  $400^\circ\text{C}$ .) after the layer transfer to form device structures, such as, for example, transistors, on or in the donor wafer that may be physically aligned and may be electrically coupled to the acceptor wafer. Many of the process flows in this document may utilize pattern repeats in one or two directions, for example, FIG. 36.

[0554] Two alignment schemes for subsequent processing of structures on the bonded donor wafer are described. The landing strips or pads in the acceptor wafer could be made sufficiently larger than the repeating pattern on the donor wafer in both directions, as shown in FIG. 43E, such that the mask alignment can be moved in increments of the repeating pattern left or right (East or West) and up or down (North or South) until the thru layer connections may be on top of their corresponding landing strips or pads. Alternatively, a narrow landing strip or pad could extend sufficiently beyond the repeating pattern in one direction and a metallization strip or pad in the donor wafer could extend sufficiently beyond the repeating pattern in the other direction, as shown in FIG. 43D, that after shifting the masks in increments of the repeating

pattern in both directions to the right location the thru layer connection can be made at the intersection of the landing strip or pad in the acceptor wafer and the metallization strip or pad in the donor wafer.

[0555] As illustrated in FIG. 43A, a generalized process flow may begin with a donor wafer 4300 that may be preprocessed with repeating wafer-sized or die-sized strips of conducting, semi-conducting or insulating materials that may be formed by deposition, ion implantation and anneal, oxidation, epitaxial growth, combinations of above, or other semiconductor processing steps and methods. A four cardinal directions indicator 4340 may be used to assist the explanation. Width Wy strips or rows 4304 may be constructed on donor wafer 4300 and are drawn in illustration blow-up area 4302. The width Wy strips or rows 4304 may traverse from East to West and have repeats from North to South that may extend substantially all the way across the wafer or die from North to South. The donor wafer strips 4304 may extend in length from East to West by the acceptor die width plus the maximum donor wafer to acceptor wafer misalignment, or alternatively, may extend the entire length of a donor wafer from East to West. Width Wx strips or rows 4306 may be constructed on donor wafer 4300 and are drawn in illustration blow-up area 4302. The width Wx strips or rows 4306 may traverse from North to South and have repeats from East to West that may extend substantially all the way across the wafer or die from East to West. The donor wafer strips 4306 may extend in length from North to South by the acceptor die width plus the maximum donor wafer to acceptor wafer misalignment, or alternatively, may extend the entire length of a donor wafer from North to South. Donor wafer 4300 may have one or more donor alignment marks 4320. The donor wafer 4300 may be preprocessed with a layer transfer demarcation plane, such as, for example, a hydrogen implant cleave plane.

[0556] As illustrated in FIG. 43B, the donor wafer 4300 with a layer transfer demarcation plane may be flipped over, aligned, and bonded to the acceptor wafer 4310. Or carrier wafer or holder wafer layer transfer techniques as previously discussed may be utilized. Typically the donor wafer 4300 to acceptor wafer 4310 maximum misalignment at wafer to wafer placement and bonding may be approximately 1 micron. The acceptor wafer 4310 may be a preprocessed wafer that may have fully functional circuitry or may be a wafer with previously transferred layers, or may be a blank carrier or holder wafer, or other kinds of substrates and may also be called a target wafer. The acceptor wafer 4310 and the donor wafer 4300 may be a bulk mono-crystalline silicon wafer or a Silicon On Insulator (SOI) wafer or a Germanium on Insulator (GeOI) wafer. Both the donor wafer 4300 and the acceptor wafer 4310 bonding surfaces may be prepared for wafer bonding by oxide depositions, polishes, plasma, or wet chemistry treatments to facilitate successful wafer to wafer bonding. The donor wafer 4300 may be cleaved at or thinned to the layer transfer demarcation plane, leaving donor wafer portion 4300L and the pre-processed strips, rows, and layers such as Wy strips 4304 and Wx strips 4306.

[0557] As further illustrated in FIG. 43B, the remaining donor wafer portion 4300L may be further processed to create device structures and donor structure to acceptor structure connections that may be aligned to a combination of the acceptor wafer alignment marks 4321 and the donor wafer alignment marks 4320. A four cardinal directions indicator 4340 may be used to assist the explanation. The misalignment

in the East-West direction may be DX 4324 and the misalignment in the North-South direction may be DY 4322. For simplicity of the following explanations, the donor wafer alignment mark 4320 and acceptor wafer alignment mark 4321 may be assumed to be placed such that the donor wafer alignment mark 4320 may be always north and west of the acceptor wafer alignment mark 4321. The cases where donor wafer alignment mark 4320 may be either perfectly aligned with or aligned south or east of acceptor alignment mark 4321 may be handled in a similar manner. In addition, these alignment marks may be placed in only a few locations on each wafer, within each step field, within each die, within each repeating pattern W, or in other locations as a matter of design choice. If die-sized donor wafer strips are utilized, the repeating strips may overlap into the die scribeline the distance of the maximum donor wafer to acceptor wafer misalignment.

[0558] As illustrated in FIG. 43C, donor wafer alignment mark 4320 may land DY 4322 distance in the North-South direction away from acceptor alignment mark 4321. Wy strips 4304 are drawn in illustration blow-up area 4302. A four cardinal directions indicator 4340 may be used to assist the explanation. In this illustration, misalignment DY 4322 may include three repeat strip or row distances Wy 4304 and a residual Rdy 4325. In the generalized case, residual Rdy 4325 may be the remainder of DY 4322 modulo Wy 4304,  $0 \leq Rdy 4325 < Wy 4304$ . Proper alignment of images for further processing of donor wafer structures may be accomplished shifting Rdy 4325 from the acceptor wafer alignment mark 4321 in the North-South direction for the image's North-South alignment mark position. Similarly, donor wafer alignment mark 4320 may land DX 4324 distance in the East-West direction away from acceptor alignment mark 4321. Wx strips 4306 are drawn in illustration blow-up area 4302. In this illustration, misalignment DX 4324 includes two repeat strip or row distances Wx 4306 and a residual Rdx 4308. In the generalized case, residual Rdx 4308 may be the remainder of DX 4324 modulo Wx 4306,  $0 \leq Rdx 4308 < Wx 4306$ . Proper alignment of images for further processing of donor wafer structures may be accomplished shifting Rdx 4308 from the acceptor wafer alignment mark 4321 in the East-West direction for the image's East-West alignment mark position.

[0559] As illustrated in FIG. 43D acceptor metal connect strip 4338 may be designed with length Wy 4304 plus any extension for via design rules and angular misalignment within the die, and may be oriented length-wise in the North-South direction. A four cardinal directions indicator 4340 may be used to assist the explanation. The acceptor metal connect strip 4338 may be formed with metals, such as, for example, copper or aluminum, and may include barrier metals, such as, for example, TiN or WCo. The acceptor metal connect strip 4338 extension, in length or width, for via design rules may include compensation for angular misalignment as a result of wafer to wafer bonding that may not be compensated for by the stepper overlay algorithms, and may include uncompensated donor wafer bow and warp. The donor metal connect strip 4339 may be designed with length Wx 4306 plus any extension for via design rules and may be oriented length-wise in the East-West direction. The donor wafer metal connect strip 4339 may be formed with metals, such as, for example, copper or aluminum, and may include barrier metals, such as, for example, TiN or WCo. The donor wafer metal connect strip 4339 extension, in length or width, for via design rules may include compensation for angular misalignment during wafer to wafer bonding and may include

uncompensated donor wafer bow and warp. The acceptor metal connect strip **4338** may be aligned to the acceptor wafer alignment mark **4321**. Thru layer via (TLV) **4366** and donor wafer metal connect strip **4339** may be aligned as described above in a similar manner as other donor wafer structure definition images or masks. The TLV's **4366** and donor wafer metal connect strip's **4339** East-West alignment mark position may be Rdx **4308** from the acceptor wafer alignment mark **4321** in the East-West direction. The TLV's **4366** and donor wafer metal connect strip's **4339** North-South alignment mark position may be Rdy **4325** from the acceptor wafer alignment mark **4321** in the North-South direction. TLV **4366** may be drawn in the database (not shown) so that it may be positioned approximately at the center of donor wafer metal connect strip **4339** and acceptor metal connect strip **4338** landing strip, and, hence, may be away from the ends of donor wafer metal connect strip **4339** and acceptor metal connect strip **4338** at distances greater than approximately the nominal layer to layer misalignment margin.

[0560] As illustrated in FIG. 43E, a donor wafer to acceptor wafer metal connect scheme may be utilized when no donor wafer metal connect strip may be desirable. A four cardinal directions indicator **4340** may be used to assist the explanation. Acceptor metal connect rectangle **4338E** may be designed with North-South direction length of Wy **4304** plus any extension for via design rules and with East-West direction length of Wx **4306** plus any extension for via design rules. The acceptor metal connect rectangle **4338E** extensions, in length or width, for via design rules may include compensation for angular misalignment during wafer to wafer bonding and may include uncompensated donor wafer bow and warp. The acceptor metal connect rectangle **4338E** may be aligned to the acceptor wafer alignment mark **4321**. Thru layer via (TLV) **4366** may be aligned as described above in a similar manner as other donor wafer structure definition images or masks. The TLV's **4366** East-West alignment mark position may be Rdx **4308** from the acceptor wafer alignment mark **4321** in the East-West direction. The TLV's **4366** North-South alignment mark position may be Rdy **4325** from the acceptor wafer alignment mark **4321** in the North-South direction. TLV **4366** may be drawn in the database (not shown) so that it may be positioned approximately at the center of the acceptor metal connect rectangle **4338E**, and, hence, may be away from the edges of the acceptor metal connect rectangle **4338E** at distances greater than approximately the nominal layer to layer misalignment margin.

[0561] As illustrated in FIG. 43F, the length of donor wafer metal connect strip **4339F** may be designed less than East-West repeat length Wx **4306** to provide an increase in connection density of TLVs **4366**. This decrease in donor wafer metal connect strip **4339F** length may be compensated for by increasing the width of acceptor metal connect strip **4338F** by twice distance **4375** and shifting the East-West alignment towards the East after calculating and applying the usual Rdx **4308** offset to acceptor alignment mark **4321**. The North-South alignment may be done as previously described.

[0562] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 43A through 43F are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the North-South direction could become the East-West direction (and vice versa) by merely rotating the wafer 90° and that the Wy strips or rows **4304** could also run North-South as a matter of design choice with corresponding

adjustments to the rest of the fabrication process. Such skilled persons will further appreciate that the strips within Wx **4306** and Wy **4304** can have many different organizations as a matter of design choice. For example, the strips Wx **4306** and Wy **4304** can each include a single row of transistors in parallel, multiple rows of transistors in parallel, multiple groups of transistors of different dimensions and orientations and types (either individually or in groups), and different ratios of transistor sizes or numbers. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the scope of the invention is to be limited only by the appended claims.

[0563] As illustrated in FIG. 44A and with reference to FIGS. 41 and 43, the layout of the donor wafer formation into repeating strips and structures may be a repeating pattern in both the North-South and East-West directions. A four cardinal directions indicator **4440** may be used to assist the explanation. This repeating pattern may be a repeating pattern of transistors, of which each transistor may have gate **4422**, forming a band of transistors along the East-West axis. The repeating pattern in the North-South direction may include substantially parallel bands of transistors, of which each transistor may have PMOS active area **4412** or NMOS active area **4414**. The width of the PMOS transistor strip repeat Wp **4406** may be composed of transistor isolations **4410** of 3F and shared **4416** of 1F width, plus a PMOS transistor active area **4412** of width 2.5F. The width of the NMOS transistor strip repeat Wn **4404** may be composed of transistor isolations **4410** of 3F and shared **4416** of 1F width, plus an NMOS transistor active area **4414** of width 2.5F. The width Wv **4402** of the layer to layer via channel **4418**, composed of transistor isolation oxide, may be 5F. The total North-South repeat width Wy **4424** may be 18F, the addition of Wv **4402**+Wn **4404**+Wp **4406**, where F may be two times lambda, the minimum design rule. The gates **4422** may be of width F and spaced 4F apart from each other in the East-West direction. The East-West repeat width Wx **4426** may be 5F. This forms a repeating pattern of continuous diffusion sea of gates. Adjacent transistors in the East-West direction may be electrically isolated from each other by biasing the gate in-between to the appropriate off state; i.e., grounded gate for NMOS and Vdd gate for PMOS.

[0564] As illustrated in FIG. 44B and with reference to FIGS. 44A and 43, Wv **4432** may be enlarged for multiple rows (shown as two rows) of donor wafer metal connect strips **4439**. The width Wv **4432** of the layer to layer via channel **4418** may be 10F. Acceptor metal connect strip **4338** length may be Wy **4424** in length plus any extension indicated by design rules as described previously to provide connection to thru layer via (TLV) **4366**.

[0565] As illustrated in FIG. 44C and with reference to FIGS. 44B and 43, gates **4422C** may be repeated in the East to West direction as pairs with an additional repeat of transistor isolations **4410**. The East-West pattern repeat width Wx **4426** may be 14F. Donor wafer metal connect strip **4339** length may be Wx **4426** in length plus any extension indicated by design rules as described previously to provide connection to thru layer via (TLV) **4366**. This repeating pattern of transistors with gates **4422C** may form a band of transistors along the East-West axis.

[0566] The following sections discuss some embodiments of the invention wherein wafer or die-sized sized pre-formed

non-repeating device structures may be transferred and then may be processed to create 3D ICs.

[0567] An embodiment of the invention is to pre-process a donor wafer by forming a block or blocks of a non-repeating pattern device structures and layer transferred using the above described techniques such that the donor wafer structures may be electrically coupled to the acceptor wafer. This donor wafer of non-repeating pattern device structures may be a memory block of DRAM, or a block of Input-Output circuits, or any other block of non-repeating pattern circuitry or combination thereof. The donor wafer and acceptor wafer in these discussions may include the compositions, such as metal layers and TLVs, referred to for donor wafers and acceptor wafers in the FIGS. 1, 2 and 3 layer transfer discussions.

[0568] As illustrated in FIG. 45, an acceptor wafer die 4500 on an acceptor wafer may be aligned and bonded with a donor wafer which may have prefabricated non-repeating pattern device structures, such as, for example, block 4504. Acceptor alignment mark 4521 and donor wafer alignment mark 4520 may be located in the acceptor wafer die 4500 (as shown) or may be elsewhere on the bonded donor and acceptor wafer stack. A four cardinal directions indicator 4540 may be used to assist the explanation. A general connectivity structure 4502 may be drawn inside or outside of the donor wafer non-repeating pattern device structure block 4504 and a blowup of the general connectivity structure 4502 is shown. Maximum donor wafer to acceptor wafer misalignment in the East-West direction Mx 4506 and maximum donor wafer to acceptor wafer misalignment in the North-South direction My 4508 may include margin for incremental misalignment resulting from the angular misalignment during wafer to wafer bonding, and may include uncompensated donor wafer bow and warp. Acceptor wafer metal connect strips 4510, shown as oriented in the North-South direction, may have a length of at least My 4508 and may be aligned to the acceptor wafer alignment mark 4521. Donor wafer metal connect strips 4511, shown as oriented in the East-West direction, may have a length of at least Mx 4506 and may be aligned to the donor wafer alignment mark 4520. Acceptor wafer metal connect strips 4510 and donor wafer metal connect strips 4511 may be formed with metals, such as, for example, copper or aluminum, and may include barrier metals, such as, for example, TiN or WCo. The thru layer via (TLV) 4512 connecting donor wafer metal connect strip 4511 to acceptor wafer metal connect strips 4510 may be aligned to the acceptor wafer alignment mark 4521 in the East-West direction and to the donor wafer alignment mark 4520 in the North-South direction in such a manner that the TLV may typically be at the intersection of the correct two metal strips, which it may need to connect.

[0569] Alternatively, the donor wafer may include both repeating and non-repeating pattern device structures. The two elements, one repeating and the other non-repeating, may be patterned separately. The donor wafer non-repeating pattern device structures, such as, for example, block 4504, may be aligned to the donor wafer alignment mark 4520, and the repeating pattern device structures may be aligned to the acceptor wafer alignment mark 4521 with an offsets Rdx and Rdy as previously described with reference to FIG. 43. Donor wafer metal connect strips 4511, shown as oriented in the East-West direction, may be aligned to the donor wafer alignment mark 4520. Acceptor wafer metal connect strips 4510, shown as oriented in the North-South direction, may be aligned to the acceptor wafer alignment mark 4521 with the

offset Rdy. The thru layer via (TLV) 4512 connecting donor wafer metal connect strip 4511 to acceptor wafer metal connect strips 4510 may be aligned to the acceptor wafer alignment mark 4521 in the East-West direction with the offset Rdx and to the donor wafer alignment mark 4520 in the North-South direction

[0570] Persons of ordinary skill in the art will appreciate that the illustrations in FIG. 45 are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the North-South direction could become the East-West direction (and vice versa) by merely rotating the wafer 90° and that the donor wafer metal connect strips 4511 could also run North-South as a matter of design choice with corresponding adjustments to the rest of the fabrication process. Moreover, TLV 4512 may be drawn in the database (not shown) so that it may be positioned approximately at the center of donor wafer metal connect strip 4511 and acceptor wafer metal connect strip 4510, and, hence, may be away from the ends or edges of donor wafer metal connect strip 4511 and acceptor wafer metal connect strips 4510 at distances greater than approximately the nominal layer to layer misalignment margin. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the scope of the invention is to be limited only by the appended claims.

[0571] The following sections discuss some embodiments of the invention that enable various aspects of 3D IC formation.

[0572] It may be desirable to screen the sensitive gate dielectric and other gate structures from the layer transfer or ion-cut atomic species implantation previously described, such as, for example, Hydrogen and Helium implantation thru the gate structures and into the underlying silicon wafer or substrate.

[0573] As illustrated in FIG. 46, lithographic definition and etching of an atomically dense material 4650, for example about 5,000 angstroms of Tantalum, may be combined with a remaining after etch about 5,000 angstroms of photoresist 4652, to create implant stopping regions or shields on donor wafer 4600. Interlayer dielectric (ILD) 4608, gate metal 4604, gate dielectric 4605, transistor junctions 4606, shallow trench isolation (STI) 4602 are shown in the illustration. The screening of ion-cut implant 4609 may create segmented layer transfer demarcation planes 4699 (shown as dashed lines) in donor wafer 4600, or other layers in previously described processes, and may need additional post-cleave polishing, such as, for example, by chemical mechanical polishing (CMP), to provide a smooth bonding or device structure formation surface for 3D IC manufacturability. Alternatively, the ion-cut implant 4609 may be done in multiple steps with a sufficient tilt each to create an overlapping or continuous layer transfer demarcation plane 4699 below the protected regions.

[0574] When a high density of thru layer vias (TLVs) are made possible by the methods and techniques in this document, the conventional metallization layer scheme may be improved to utilize this interconnect dense 3D technology.

[0575] As illustrated in FIG. 47A, a conventional metallization layer scheme may be built on a conventional transistor silicon layer 4702. The conventional transistor silicon layer 4702 may be connected to the first metal layer 4710 thru the contact 4704. The dimensions of this interconnect pair of contact and metal lines (may be referred to as pitch, a line-



space pair) generally may be at the minimum line resolution of the lithography and etch capability for that technology process node, for example, in nanometers or tens of nanometers line-widths, spaces, and resultant pitches, and may have a few thousands of angstroms thickness of metal and insulator layers. Traditionally, this may be called a "1x" design rule metal layer. Typically, the next metal layer may be at the "1x" design rule, the metal layer 4712 and via below 4705 and via above 4706 that connects metal layer 4712 with metal layer 4710 or with metal layer 4714 where desired. The next few layers may be often constructed at twice the minimum lithographic and etch capability and may be called "2x" metal layers, and may have thicker metal than the 1x layers for higher current carrying capability. For example, a 1x metal layer or interconnect may be about 3000 angstroms thick, whereby a 2x metal layer or interconnect may have a thickness of about 6000 angstroms, and a 4x metal layer or interconnect may have a 12,000 angstrom thickness. These may be illustrated with metal layer 4714 paired with via 4707 and metal layer 4716 paired with via 4708 in FIG. 47. Accordingly, the metal via pairs of metal layer 4718 with via 4709, and metal layer 4720 with bond pad 4722, represent the "4x" metallization layers where the planar (line-space pairs or pitch) and thickness dimensions may be again larger and thicker than the 2x and 1x layers. The precise number of 1x or 2x or 4x metal and via layers may vary depending on interconnection needs and other requirements; however, the general flow may be that of increasingly larger metal line, metal to metal space, (and resultant pitch), and/or metal and insulator thicknesses and associated via dimensions as the metal layers may be farther from the silicon transistors in conventional transistor silicon layer 4702 and closer to the bond pads 4722.

[0576] As illustrated in FIG. 47B, an improved metallization layer scheme for 3D ICs may be built on the first mono-crystalline silicon device layer 4764. The first mono-crystalline silicon device layer 4764 may be illustrated as the NMOS silicon transistor layer from the previously described FIG. 20, but may be a conventional logic transistor silicon substrate or layer or other substrate as previously described for acceptor substrate or acceptor wafer. The "1x" metal layers metal layer 4750 and metal layer 4759 may be connected with contact 4740 to the silicon transistors and vias 4748 and 4749 to each other or metal layer 4758. The 2x layer pairs metal layer 4758 with via 4747 and metal layer 4757 with via 4746. The 4x metal layer 4756 may be paired with via 4745 and metal layer 4755, also at 4x. However, now via 4744 may be constructed in 2x design rules to enable metal layer 4754 to be at 2x design rules. Metal layer 4753 and via 4743 may be also at 2x design rules and thicknesses. Vias 4742 and 4741 may be paired with metal layers 4752 and 4751 at the 1x minimum design rule dimensions and thickness, thus utilizing the high density of TLVs 4760. The TLV 4760 of the illustrated PMOS layer transferred top transistor layer 4762, from the previously described FIG. 20, may then be constructed at the 1x minimum design rules and provide for maximum density of the top layer. The precise numbers of 1x or 2x or 4x layers may vary depending on circuit area and current carrying metallization requirements and tradeoffs. For example, for 1x, a 1x metal layer or interconnect may be about 3000 angstroms thick, the 1x metal linewidth may be less than about 100 nm, the 1x via diameter may be less than about 100 nm, the metal to metal space may be less than about 100 nm, the metal pitch may be less than about 200 nm, and/or the

layer to layer alignment may be less than about 40 nm, and in many cases less than about 10 nm or less than about 5 nm. The illustrated PMOS layer transferred top transistor layer 4762 may be composed of any of the low temperature devices or transferred layers illustrated in this document.

[0577] When a transferred layer may not be optically transparent to shorter wavelength light, and hence not able to detect alignment marks and images to a nanometer or tens of nanometer resolution, which may result from the transferred layer or its carrier or holder substrate's thickness, infra-red (IR) optics and imaging may be utilized for alignment purposes. However, the resolution and alignment capability may not be satisfactory. In an embodiment of the invention, alignment windows may be created that allow use of the shorter wavelength light for alignment purposes during process flows, procedures, and methodologies, such as, for example, layer transfer. The donor wafer and acceptor wafer in these discussions may include the compositions, such as metal layers and TLVs, referred to for donor wafers and acceptor wafers in the FIGS. 1, 2 and 3 layer transfer discussions.

[0578] As illustrated in FIG. 48A, a generalized process flow may begin with a donor wafer 4800 that may be preprocessed with layers 4802 of conducting, semi-conducting or insulating materials that may be formed by deposition, ion implantation and anneal, oxidation, epitaxial growth, combinations of above, or other semiconductor processing steps and methods. The donor wafer 4800 may be preprocessed with a layer transfer demarcation plane 4899, such as, for example, a hydrogen implant cleave plane, before or after layers 4802 may be formed, or may be thinned by other methods previously described. Alignment windows 4830 may be lithographically defined, plasma/RIE etched substantially through layers 4802, layer transfer demarcation plane 4899, and donor wafer 4800, and then filled with shorter wavelength transparent material, such as, for example, silicon dioxide, and planarized with chemical mechanical polishing (CMP). Donor wafer 4800 may be further thinned from the backside by CMP. The size and placement on donor wafer 4800 of the alignment windows 4830 may be determined based on the maximum misalignment tolerance of the alignment scheme used while bonding the donor wafer 4800 to the acceptor wafer 4810, and the placement locations of the acceptor wafer alignment marks 4890. Alignment windows 4830 may be processed before or after layers 4802 are formed. Acceptor wafer 4810 may be a preprocessed wafer that may have fully functional circuitry or may be a wafer with previously transferred layers, or may be a blank carrier or holder wafer, or other kinds of substrates and may be called a target wafer. The acceptor wafer 4810 and the donor wafer 4800 may be a bulk mono-crystalline silicon wafer or a Silicon On Insulator (SOI) wafer or a Germanium on Insulator (GeOI) wafer. Acceptor wafer 4810 metal connect pads or strips 4880 and acceptor wafer alignment marks 4890 are shown.

[0579] Both the donor wafer 4800 and the acceptor wafer 4810 bonding surfaces 4801 and 4811 may be prepared for wafer bonding by depositions, polishes, plasma, or wet chemistry treatments to facilitate successful wafer to wafer bonding.

[0580] As illustrated in FIG. 48B, the donor wafer 4800 with layers 4802, alignment windows 4830, and layer transfer demarcation plane 4899 may then be flipped over, high resolution aligned to acceptor wafer alignment marks 4890, and bonded to the acceptor wafer 4810.

[0581] As illustrated in FIG. 48C, the donor wafer 4800 may be cleaved at or thinned to the layer transfer demarcation plane, leaving a portion of the donor wafer 4800', alignment windows 4830' and the pre-processed layers 4802 aligned and bonded to the acceptor wafer 4810.

[0582] As illustrated in FIG. 48D, the remaining donor wafer portion 4800' may be removed by polishing or etching and the transferred layers 4802 may be further processed to create donor wafer device structures 4850 that may be precisely aligned to the acceptor wafer alignment marks 4890, and further process the alignment windows 4830' into alignment window regions 4831. These donor wafer device structures 4850 may utilize thru layer vias (TLVs) 4860 to electrically couple the donor wafer device structures 4850 to the acceptor wafer metal connect pads or strips 4880. As the transferred layers 4802 may be thin, on the order of about 200 nm or less in thickness, the TLVs may be easily manufactured as a typical metal to metal via, and said TLV may have state of the art diameters such as, for example, nanometers or tens to a few hundreds of nanometers, such as, for example about 150 nm or about 100 nm or about 50 nm. The thinner the transferred layers 4802, the smaller the thru layer via diameter obtainable, which may result from maintaining manufacturable via aspect ratios. Thus, the transferred layers 4802 (and hence, TLVs 4860) may be, for example, less than about 2 microns thick, less than about 1 micron thick, less than about 0.4 microns thick, less than about 200 nm thick, less than about 150 nm thick, or less than about 100 nm thick.

[0583] An additional use for the high density of TLVs 4860 in FIG. 48D, or any such TLVs in this document, may be to thermally conduct heat generated by the active circuitry from one layer to another connected by the TLVs, such as, for example, donor layers and device structures to acceptor wafer or substrate, and may be utilized to conduct heat to an on chip thermoelectric cooler, heat sink, or other heat removing device. A portion of TLVs on a 3D IC may be utilized primarily for electrical coupling, and a portion may be primarily utilized for thermal conduction. A portion of TLVs on a 3D IC may be utilized for thermal conduction to conduct heat, but do not provide electrical coupling or conduct electronic current. In many cases, the TLVs may provide utility for both electrical coupling and thermal conduction.

[0584] When multiple layers may be stacked in a 3D IC, the power density per unit area increases. The thermal conductivity of mono-crystalline silicon may be poor at approximately 150 W/m-K and silicon dioxide, the most common electrical insulator in modern silicon integrated circuits, may be a very poor about 1.4 W/m-K. If a heat sink is placed at the top of a 3D IC stack, then the bottom chip or layer (farthest from the heat sink) may have the poorest thermal conductivity to that heat sink, since the heat from that bottom layer must travel thru the silicon dioxide and silicon of the chip(s) or layer(s) above it.

[0585] As illustrated in FIG. 51, a heat spreader layer 5105 may be deposited on top of a thin silicon dioxide layer 5103 which may be deposited on the top surface of the interconnect metallization layers 5101 of substrate 5102. Heat spreader layer 5105 may include Plasma Enhanced Chemical Vapor Deposited Diamond Like Carbon (PECVD DLC), which may have a thermal conductivity of approximately 1000 W/m-K, or another thermally conductive material, such as, for example, Chemical Vapor Deposited (CVD) graphene (approximately 5000 W/m-K) or copper (approximately 400 W/m-K). Heat spreader layer 5105 may be of thickness

approximately 20 nm up to approximately 1 micron. A suitable thickness range may be approximately 50 nm to about 100 nm and a suitable electrical conductivity of the heat spreader layer 5105 may be an insulator to enable minimum design rule diameters of the future thru layer vias. If the heat spreader is electrically conducting, the TLV openings may need to be somewhat enlarged to allow for the deposition of a non-conducting coating layer on the TLV walls before the conducting core of the TLV may be deposited. Alternatively, if the heat spreader layer 5105 is electrically conducting, it may be masked and etched to provide the landing pads for the thru layer vias and a large grid around them for heat transfer, which could be used as the ground plane or as power and ground straps for the circuits above and below it. Oxide layer 5104 may be deposited (and may be planarized to fill any gaps in the heat transfer layer) to prepare for wafer to wafer oxide bonding. Acceptor wafer substrate 5114 may include substrate 5102, interconnect metallization layers 5101, thin silicon dioxide layer 5103, heat spreader layer 5105, and oxide layer 5104. The donor wafer substrate 5106 may be processed with wafer sized layers of doping as previously described, in preparation for forming transistors and circuitry after the layer transfer, such as, for example, junction-less, RCAT, V-groove, and bipolar. A screen oxide layer 5107 may be grown or deposited prior to the implant or implants to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. A layer transfer demarcation plane 5199 (shown as a dashed line) may be formed in donor wafer substrate 5106 by hydrogen implantation, 'ion-cut' method, or other methods as previously described. Donor wafer 5112 may include donor wafer substrate 5106, layer transfer demarcation plane 5199, screen oxide layer 5107, and any other layers (not shown) in preparation for forming transistors as discussed previously. Both the donor wafer 5112 and acceptor wafer substrate 5114 may be prepared for wafer bonding as previously described and then bonded at the surfaces of oxide layer 5104 and screen oxide layer 5107, at a low temperature (less than approximately 400° C.). The portion of donor wafer substrate 5106 that may be above the layer transfer demarcation plane 5199 may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining transferred layers 5106'. Alternatively, donor wafer 5112 may be constructed and then layer transferred, using methods described previously such as, for example, ion-cut with replacement gates (not shown), to the acceptor wafer substrate 5114. Now transistors or portions of transistors may be formed and aligned to the acceptor wafer alignment marks (not shown) and thru layer vias formed as previously described. Thus, a 3D IC with an integrated heat spreader may be constructed.

[0586] As illustrated in FIG. 52A, a set of power and ground grids, such as, for example, bottom transistor layer power and ground grid 5207 and top transistor layer power and ground grid 5206, may be connected by thru layer power and ground vias 5204 and thermally coupled to electrically non-conducting heat spreader layer 5205. If the heat spreader is an electrical conductor, than it could either be used as a ground plane, or a pattern should be created with power and ground strips in between the landing pads for the TLVs. The density of the power and ground grids and the thru layer vias to the power and ground grids may be designed to guarantee a certain overall thermal resistance for substantially all the circuits in the 3D IC stack. Bonding oxides 5210, printed

wiring board **5200**, package heat spreader **5225**, bottom transistor layer **5202**, top transistor layer **5212**, and heat sink **5230** are shown. Thus, a 3D IC with an integrated heat sink, heat spreaders, and thru layer vias to the power and ground grid is constructed.

[**0587**] As illustrated in FIG. **52B**, thermally conducting material, such as, for example, PECVD DLC, may be formed on the sidewalls of the 3D IC structure of FIG. **52A** to form sidewall thermal conductors **5260** for sideways heat removal. Bottom transistor layer power and ground grid **5207**, top transistor layer power and ground grid **5206**, thru layer power and ground vias **5204**, heat spreader layer **5205**, bonding oxides **5210**, printed wiring board **5200**, package heat spreader **5225**, bottom transistor layer **5202**, top transistor layer **5212**, and heat sink **5230** are shown.

[**0588**] FIG. **62** illustrates a procedure for a chip designer to ensure a good thermal profile for his or her design. After a first pass or a portion of the first pass of the desired chip layout process is complete, a thermal analysis may be conducted to determine temperature profiles for active or passive elements, such as gates, on the 3D chip. The thermal analysis may be started (**6200**). The temperature of any stacked gate, or region of gates, may be calculated and compared to a desired specification value (**6210**). If the gate, or region of gates, temperature is higher than the specification, which may, for example, be in the range of 65° C.-150° C., modifications **6220** may be made to the layout or design, such as, for example, power grids for stacked layers may be made denser or wider, additional contacts to the gate may be added, more through-silicon (TLV and/or TSV) connections may be made for connecting the power grid in stacked layers to the layer closest to the heat sink, or any other method to reduce stacked layer temperature that may be described herein or described in U.S. patent application Ser. Nos. 13/041,405 and 13/273,712 herein incorporated by reference, may be used alone or in combination. The output **6230** may give the designer the temperature of either the modified stacked gate ('Yes' tree), or region of gates, or an unmodified one ('No' tree), and may include the original un-modified gate temperature that was above the desired specification. The thermal analysis may end (**6240**) or may be iterated. Alternatively, the power grid may be designed (based on heat removal criteria) simultaneously with the logic gates and layout of the design, or for various regions of any layer of the 3D integrated circuit stack. The density of TLVs may be greater than 10<sup>4</sup> per cm<sup>2</sup>, and may be 10x, 100x, 1000x, denser than TSVs.

[**0589**] Thermal anneals to activate implants and set junctions in previously described methods and process flows may be performed with RTA (Rapid Thermal Anneal) or furnace thermal exposures. Alternatively, laser annealing may be utilized to activate implants and set the junctions. Optically absorptive and reflective layers as described previously in FIGS. **15G** and **15H** may be employed to anneal implants and activate junctions on many of the devices or structures discussed in this document.

[**0590**] The monolithic 3D integration concepts described in this patent application can lead to novel embodiments of poly-crystalline silicon based memory architectures. While the below concepts in FIGS. **49** and **50** are explained by using resistive memory architectures as an example, it will be clear to one skilled in the art that similar concepts can be applied to the NAND flash, charge trap, and DRAM memory architectures and process flows described previously in this patent application.

[**0591**] As illustrated in FIGS. **49A** to **49K**, a resistance-based 3D memory with zero additional masking steps per memory layer may be constructed with methods that may be suitable for 3D IC manufacturing. This 3D memory utilizes poly-crystalline silicon junction-less transistors that may have either a positive or a negative threshold voltage and may have a resistance-based memory element in series with a select or access transistor.

[**0592**] As illustrated in FIG. **49A**, a silicon substrate with peripheral circuitry **4902** may be constructed with high temperature (greater than approximately 400° C.) resistant wiring, such as, for example, Tungsten. The peripheral circuitry substrate **4902** may include memory control circuits as well as circuitry for other purposes and of various types, such as, for example, analog, digital, RF, or memory. The peripheral circuitry substrate **4902** may include peripheral circuits that can withstand an additional rapid-thermal-anneal (RTA) and still remain operational and retain good performance. For this purpose, the peripheral circuits may be formed such that they have not been subjected to a weak RTA or no RTA for activating dopants. Silicon oxide layer **4904** may be deposited on the top surface of the peripheral circuitry substrate.

[**0593**] As illustrated in FIG. **49B**, a layer of N+ doped poly-crystalline or amorphous silicon **4906** may be deposited. The amorphous silicon or poly-crystalline silicon layer **4906** may be deposited using a chemical vapor deposition process, such as, for example, LPCVD or PECVD, or other process methods, and may be deposited doped with N+ dopants, such as, for example, Arsenic or Phosphorous, or may be deposited un-doped and subsequently doped with, such as, for example, ion implantation or PLAD (PLasma Assisted Doping) techniques. Silicon Oxide **4920** may then be deposited or grown. This now forms the first Si/SiO<sub>2</sub> layer **4923** which includes N+ doped poly-crystalline or amorphous silicon layer **4906** and silicon oxide layer **4920**.

[**0594**] As illustrated in FIG. **49C**, additional Si/SiO<sub>2</sub> layers, such as, for example, second Si/SiO<sub>2</sub> layer **4925** and third Si/SiO<sub>2</sub> layer **4927**, may each be formed as described in FIG. **49B**. Oxide layer **4929** may be deposited to electrically isolate the top N+ doped poly-crystalline or amorphous silicon layer.

[**0595**] As illustrated in FIG. **49D**, a Rapid Thermal Anneal (RTA) may be conducted to crystallize the N+ doped poly-crystalline silicon or amorphous silicon layers **4906** of first Si/SiO<sub>2</sub> layer **4923**, second Si/SiO<sub>2</sub> layer **4925**, and third Si/SiO<sub>2</sub> layer **4927**, forming crystallized N+ silicon layers **4916**. Temperatures during this RTA may be as high as approximately 800° C. Alternatively, an optical anneal, such as, for example, a laser anneal, could be performed alone or in combination with the RTA or other annealing processes.

[**0596**] As illustrated in FIG. **49E**, oxide layer **4929**, third Si/SiO<sub>2</sub> layer **4927**, second Si/SiO<sub>2</sub> layer **4925** and first Si/SiO<sub>2</sub> layer **4923** may be lithographically defined and plasma/RIE etched to form a portion of the memory cell structure, which now includes multiple layers of regions of crystallized N+ silicon **4926** (previously crystallized N+ silicon layers **4916**) and oxide **4922**.

[**0597**] As illustrated in FIG. **49F**, a gate dielectric and gate electrode material may be deposited, planarized with a chemical mechanical polish (CMP), and then lithographically defined and plasma/RIE etched to form gate dielectric regions **4928** which may either be self-aligned to and substantially covered by gate electrodes **4930** (shown), or substantially cover the entire crystallized N+ silicon regions

**4926** and oxide regions **4922** multi-layer structure. The gate stack may include gate electrodes **4930** and gate dielectric regions **4928**, and may be formed with a gate dielectric, such as, for example, thermal oxide, and a gate electrode material, such as, for example, poly-crystalline silicon. Alternatively, the gate dielectric may be an atomic layer deposited (ALD) material that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Further, the gate dielectric may be formed with a rapid thermal oxidation (RTO), a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode such as, for example, tungsten or aluminum may be deposited.

**[0598]** As illustrated in FIG. **49G**, the entire structure may be substantially covered with a gap fill oxide **4932**, which may be planarized with chemical mechanical polishing. The oxide **4932** is shown transparently in the figure for clarity. Word-line regions (WL) **4950**, coupled with and composed of gate electrodes **4930**, and source-line regions (SL) **4952**, composed of crystallized N+ silicon regions **4926**, are shown.

**[0599]** As illustrated in FIG. **49H**, bit-line (BL) contacts **4934** may be lithographically defined, etched with plasma/RIE through oxide **4932**, the three crystallized N+ silicon regions **4926**, and associated oxide vertical isolation regions to connect substantially all memory layers vertically, and photoresist removed. Resistance change material **4938**, such as, for example, hafnium oxides or titanium oxides, may then be deposited, for example, with atomic layer deposition (ALD). The electrode for the resistance change memory element may then be deposited by ALD to form the electrode/BL contact **4934**. The excess deposited material may be polished to planarity at or below the top of oxide **4932**. Each BL contact **4934** with resistive change material **4938** may be shared among substantially all layers of memory, shown as three layers of memory in FIG. **49H**.

**[0600]** As illustrated in FIG. **49I**, BL metal lines **4936** may be formed and connect to the associated BL contacts **4934** with resistive change material **4938**. Contacts and associated metal interconnect lines (not shown) may be formed for the WL and SL at the memory array edges. Thru layer vias (not shown) may be formed to electrically couple the BL, SL, and WL metallization to the acceptor substrate peripheral circuitry via acceptor wafer metal connect pads (not shown).

**[0601]** As illustrated in FIGS. **49J**, **49J1** and **49J2**, cross section cut II of FIG. **49J** is shown in FIG. **49J1**, and cross section cut III of FIG. **49J** is shown in FIG. **49J2**. BL metal line **4936**, oxide **4932**, BL contact/electrode **4934**, resistive change material **4938**, WL regions **4950**, gate dielectric regions **4928**, crystallized N+ silicon regions **4926**, and peripheral circuitry substrate **4902** are shown in FIG. **49J1**. The BL contact/electrode **4934** couples to one side of the three levels of resistive change material **4938**. The other side of the resistive change material **4938** may be coupled to crystallized N+ regions **4926**. BL metal lines **4936**, oxide **4932**, gate electrode **4930**, gate dielectric regions **4928**, crystallized N+ silicon regions **4926**, interlayer oxide region ('ox'), and peripheral circuitry substrate **4902** are shown in FIG. **49J2**. The gate electrode **4930** may be common to substantially all six crystallized N+ silicon regions **4926** and forms six two-sided gated junction-less transistors as memory select transistors.

**[0602]** As illustrated in FIG. **49K**, a single exemplary two-sided gated junction-less transistor on the first Si/SiO<sub>2</sub> layer

**4923** may include crystallized N+ silicon region **4926** (functioning as the source, drain, and transistor channel), and two gate electrodes **4930** with associated gate dielectric regions **4928**. The transistor may be electrically isolated from beneath by oxide layer **4908**.

**[0603]** This flow enables the formation of a resistance-based multi-layer or 3D memory array with zero additional masking steps per memory layer, which utilizes poly-crystalline silicon junction-less transistors and may have a resistance-based memory element in series with a select transistor, and may be constructed by layer transfers of wafer sized doped poly-crystalline silicon layers, and this 3D memory array may be connected to an underlying multi-metal layer semiconductor device.

**[0604]** Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **49A** through **49K** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the RTAs and/or optical anneals of the N+ doped poly-crystalline or amorphous silicon layers **4906** as described for FIG. **49D** may be performed after each Si/SiO<sub>2</sub> layer is formed in FIG. **49C**. Additionally, N+ doped poly-crystalline or amorphous silicon layers **4906** may be doped P+, or with a combination of dopants and other polysilicon network modifiers to enhance the RTA or optical annealing and subsequent crystallization and lower the N+ silicon layer **4916** resistivity. Moreover, the doping of each crystallized N+ layer may be slightly different to compensate for interconnect resistances. Further, each gate of the double gated 3D resistance based memory may be independently controlled for increased control of the memory cell. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

**[0605]** As illustrated in FIGS. **50A** to **50J**, a resistance-based 3D memory with zero additional masking steps per memory layer may be constructed with methods that may be suitable for 3D IC manufacturing. This 3D memory utilizes poly-crystalline silicon junction-less transistors that may have either a positive or a negative threshold voltage, a resistance-based memory element in series with a select or access transistor, and may have the periphery circuitry layer formed or layer transferred on top of the 3D memory array.

**[0606]** As illustrated in FIG. **50A**, a silicon oxide layer **5004** may be deposited or grown on top of silicon substrate **5002**.

**[0607]** As illustrated in FIG. **50B**, a layer of N+ doped poly-crystalline or amorphous silicon **5006** may be deposited. The N+ doped poly-crystalline or amorphous silicon layer **5006** may be deposited using a chemical vapor deposition process, such as, for example, LPCVD or PECVD, or other process methods, and may be deposited doped with N+ dopants, such as, for example, Arsenic or Phosphorous, or may be deposited un-doped and subsequently doped with, such as, for example, ion implantation or PLAD (PLasma Assisted Doping) techniques. Silicon Oxide **5020** may then be deposited or grown. This now forms the first Si/SiO<sub>2</sub> layer **5023** which includes N+ doped poly-crystalline or amorphous silicon layer **5006** and silicon oxide layer **5020**.

**[0608]** As illustrated in FIG. **50C**, additional Si/SiO<sub>2</sub> layers, such as, for example, second Si/SiO<sub>2</sub> layer **5025** and third Si/SiO<sub>2</sub> layer **5027**, may each be formed as described in FIG.

**50B.** Oxide layer **5029** may be deposited to electrically isolate the top N+ doped poly-crystalline or amorphous silicon layer.

**[0609]** As illustrated in FIG. **50D**, a Rapid Thermal Anneal (RTA) may be conducted to crystallize the N+ doped poly-crystalline silicon or amorphous silicon layers **5006** of first Si/SiO<sub>2</sub> layer **5023**, second Si/SiO<sub>2</sub> layer **5025**, and third Si/SiO<sub>2</sub> layer **5027**, forming crystallized N+ silicon layers **5016**. Alternatively, an optical anneal, such as, for example, a laser anneal, could be performed alone or in combination with the RTA or other annealing processes. Temperatures during this step could be as high as approximately 700° C., and could even be as high as about 1400° C. Since there may be no circuits or metallization underlying these layers of crystallized N+ silicon, very high temperatures (such as about 1400° C.) can be used for the anneal process, leading to very good quality poly-crystalline silicon with few grain boundaries and very high carrier mobility approaching that of mono-crystalline silicon.

**[0610]** As illustrated in FIG. **50E**, oxide **5029**, third Si/SiO<sub>2</sub> layer **5027**, second Si/SiO<sub>2</sub> layer **5025** and first Si/SiO<sub>2</sub> layer **5023** may be lithographically defined and plasma/RIE etched to form a portion of the memory cell structure, which now includes multiple layers of regions of crystallized N+ silicon **5026** (previously crystallized N+ silicon layers **5016**) and oxide **5022**.

**[0611]** As illustrated in FIG. **50F**, a gate dielectric and gate electrode material may be deposited, planarized with a chemical mechanical polish (CMP), and then lithographically defined and plasma/RIE etched to form gate dielectric regions **5028** which may either be self-aligned to and substantially covered by gate electrodes **5030** (shown), or substantially cover the entire crystallized N+ silicon regions **5026** and oxide regions **5022** multi-layer structure. The gate stack may include gate electrode **5030** and gate dielectric region **5028**, and may be formed with a gate dielectric, such as, for example, thermal oxide, and a gate electrode material, such as, for example, poly-crystalline silicon. Alternatively, the gate dielectric may be an atomic layer deposited (ALD) material that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Further, the gate dielectric may be formed with a rapid thermal oxidation (RTO), a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate electrode such as, for example, tungsten or aluminum may be deposited.

**[0612]** As illustrated in FIG. **50G**, the entire structure may be substantially covered with a gap fill oxide **5032**, which may be planarized with chemical mechanical polishing. The oxide **5032** is shown transparently in the figure for clarity. Word-line regions (WL) **5050**, coupled with and composed of gate electrodes **5030**, and source-line regions (SL) **5052**, composed of crystallized N+ silicon regions **5026**, are shown.

**[0613]** As illustrated in FIG. **50H**, bit-line (BL) contacts **5034** may be lithographically defined, etched with plasma/RIE through oxide **5032**, the three crystallized N+ silicon regions **5026**, and associated oxide vertical isolation regions to connect substantially all memory layers vertically, and photoresist removed. Resistance change material **5038**, such as, for example, hafnium oxides or titanium oxides, may then be deposited, for example, with atomic layer deposition (ALD). The electrode for the resistance change memory element may then be deposited by ALD to form the electrode/BL

contact **5034**. The excess deposited material may be polished to planarity at or below the top of oxide **5032**. Each BL contact **5034** with resistive change material **5038** may be shared among substantially all layers of memory, shown as three layers of memory in FIG. **50H**.

**[0614]** As illustrated in FIG. **50I**, BL metal lines **5036** may be formed and connect to the associated BL contacts **5034** with resistive change material **5038**. Contacts and associated metal interconnect lines (not shown) may be formed for the WL and SL at the memory array edges.

**[0615]** As illustrated in FIG. **50J**, peripheral circuits **5078** may be constructed and then layer transferred, using methods described previously such as, for example, ion-cut with replacement gates, to the memory array, and then thru layer vias (not shown) may be formed to electrically couple the periphery circuitry to the memory array BL, WL, SL and other connections such as, for example, power and ground. Alternatively, the periphery circuitry may be formed and directly aligned to the memory array and silicon substrate **5002** utilizing the layer transfer of wafer sized doped layers and subsequent processing, for example, such as, for example, the junction-less, RCAT, V-groove, or bipolar transistor formation flows as previously described.

**[0616]** This flow enables the formation of a resistance-based multi-layer or 3D memory array with zero additional masking steps per memory layer, which utilizes poly-crystalline silicon junction-less transistors and may have a resistance-based memory element in series with a select transistor, and may be constructed by depositions of wafer sized doped poly-crystalline silicon and oxide layers, and this 3D memory array may be connected to an overlying multi-metal layer semiconductor device or periphery circuitry.

**[0617]** Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **50A** through **50J** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the RTAs and/or optical anneals of the N+ doped poly-crystalline or amorphous silicon layers **5006** as described for FIG. **50D** may be performed after each Si/SiO<sub>2</sub> layer is formed in FIG. **50C**. Additionally, N+ doped poly-crystalline or amorphous silicon layer **5006** may be doped P+, or with a combination of dopants and other polysilicon network modifiers to enhance the RTA or optical annealing crystallization and subsequent crystallization, and lower the N+ silicon layer **5016** resistivity. Moreover, the doping of each crystallized N+ layer may be slightly different to compensate for interconnect resistances. Further, each gate of the double gated 3D resistance based memory can be independently controlled for increased control of the memory cell. Additionally, by proper choice of materials for memory layer transistors and memory layer wires (e.g., by using tungsten and other materials that withstand high temperature processing for wiring), standard CMOS transistors may be processed at high temperatures (greater than about 700° C.) to form the periphery circuits **5078**. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

**[0618]** To improve the contact resistance of very small scaled contacts, the semiconductor industry employs various metal silicides, such as, for example, cobalt silicide, titanium silicide, tantalum silicide, and nickel silicide. The current advanced CMOS processes, such as, for example, 45 nm, 32 nm, and 22 nm employ nickel silicides to improve deep sub-

micron source and drain contact resistances. Background information on silicides utilized for contact resistance reduction can be found in “NiSi Salicide Technology for Scaled CMOS,” H. Iwai, et. al., *Microelectronic Engineering*, 60 (2002), pp 157-169; “Nickel vs. Cobalt Silicide integration for sub-50 nm CMOS”, B. Froment, et. al., *IMEC ESS Circuits*, 2003; and “65 and 45-nm Devices—an Overview”, D. James, *Semicon West*, July 2008, ctr\_024377. To achieve the lowest nickel silicide contact and source/drain resistances, the nickel on silicon must be heated to at least 450° C.

[0619] Thus it may be desirable to enable low resistances for process flows in this document where the post layer transfer temperature exposures must remain under approximately 400° C. as a result from metallization, such as, for example, copper and aluminum, and low-k dielectrics being present. The example process flow forms a Recessed Channel Array Transistor (RCAT), but this or similar flows may be applied to other process flows and devices, such as, for example, S-RCAT, JLT, V-groove, JFET, bipolar, and replacement gate flows.

[0620] A planar n-channel Recessed Channel Array Transistor (RCAT) with metal silicide source & drain contacts suitable for a 3D IC may be constructed. As illustrated in FIG. 53A, a P-substrate donor wafer 5302 may be processed to include wafer sized layers of N+ doping 5304, and P- doping 5301 across the wafer. The N+ doped layer 5304 may be formed by ion implantation and thermal anneal. In addition, P- doped layer 5301 may have additional ion implantation and anneal processing to provide a different dopant level than P- substrate donor wafer 5302. P- doped layer 5301 may have graded or various layers of P- doping to mitigate transistor performance issues, such as, for example, short channel effects, after the RCAT is formed. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers of P- doping 5301 and N+ doping 5304, or by a combination of epitaxy and implantation. Annealing of implants and doping may utilize optical annealing techniques or types of Rapid Thermal Anneal (RTA or spike). The N+ doped layer 5304 may have a doping concentration that may be more than 10× the doping concentration of P- doped layer 5301.

[0621] As illustrated in FIG. 53B, a silicon reactive metal, such as, for example, Nickel or Cobalt, may be deposited onto N+ doped layer 5304 and annealed, utilizing anneal techniques such as, for example, RTA, thermal, or optical, thus forming metal silicide layer 5306. The top surface of donor wafer 5302 may be prepared for oxide wafer bonding with a deposition of an oxide to form oxide layer 5308.

[0622] As illustrated in FIG. 53C, a layer transfer demarcation plane (shown as dashed line) 5399 may be formed by hydrogen implantation or other methods as previously described.

[0623] As illustrated in FIG. 53D donor wafer 5302 with layer transfer demarcation plane 5399, P- doped layer 5301, N+ doped layer 5304, metal silicide layer 5306, and oxide layer 5308 may be temporarily bonded to carrier or holder substrate 5312 with a low temperature process that may facilitate a low temperature release. The carrier or holder substrate 5312 may be a glass substrate to enable state of the art optical alignment with the acceptor wafer. A temporary bond between the carrier or holder substrate 5312 and the donor wafer 5302 may be made with a polymeric material, such as, for example, polyimide DuPont HD3007, which can be released at a later step by laser ablation, Ultra-Violet radiation

exposure, or thermal decomposition, shown as adhesive layer 5314. Alternatively, a temporary bond may be made with uni-polar or bi-polar electrostatic technology such as, for example, the Apache tool from Beam Services Inc.

[0624] As illustrated in FIG. 53E, the portion of the donor wafer 5302 that may be below the layer transfer demarcation plane 5399 may be removed by cleaving or other processes as previously described, such as, for example, ion-cut or other methods. The remaining donor wafer P- doped layer 5301 may be thinned by chemical mechanical polishing (CMP) so that the P-layer 5316 may be formed to the desired thickness. Oxide layer 5318 may be deposited on the exposed surface of P- layer 5316.

[0625] As illustrated in FIG. 53F, both the donor wafer 5302 and acceptor substrate or wafer 5310 may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) aligned and oxide to oxide bonded. Acceptor wafer 5310, as described previously, may include, for example, transistors, circuitry, metal, such as, for example, aluminum or copper, interconnect wiring, and thru layer via metal interconnect strips or pads. The carrier or holder substrate 5312 may then be released using a low temperature process such as, for example, laser ablation. Oxide layer 5318, P- layer 5316, N+ doped layer 5304, metal silicide layer 5306, and oxide layer 5308 have been layer transferred to acceptor wafer 5310. The top surface of oxide layer 5308 may be chemically or mechanically polished. Now RCAT transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer 5310 alignment marks (not shown).

[0626] As illustrated in FIG. 53G, the transistor isolation regions 5322 may be formed by mask defining and then plasma/RIE etching oxide layer 5308, metal silicide layer 5306, N+ doped layer 5304, and P- layer 5316 to the top of oxide layer 5318. Then a low-temperature gap fill oxide may be deposited and chemically mechanically polished, with the oxide remaining in isolation regions 5322. Then the recessed channel 5323 may be mask defined and etched. The recessed channel surfaces and edges may be smoothed by wet chemical or plasma/RIE etching techniques to mitigate high field effects. These process steps form oxide regions 5324, metal silicide source and drain regions 5326, N+ source and drain regions 5328 and P- channel region 5330, which may form the transistor body. The doping concentration of P- channel region 5330 may include gradients of concentration or layers of differing doping concentrations. The etch formation of recessed channel 5323 may define the transistor channel length.

[0627] As illustrated in FIG. 53H, a gate dielectric 5332 may be formed and a gate metal material may be deposited. The gate dielectric 5332 may be an atomic layer deposited (ALD) gate dielectric that may be paired with a work function specific gate metal in the industry standard high k metal gate process schemes described previously. Or the gate dielectric 5332 may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces and then a gate material such as, for example, tungsten or aluminum may be deposited. Then the gate material may be chemically mechanically polished, and the gate area defined by masking and etching, thus forming gate electrode 5334.

[0628] As illustrated in FIG. 53I, a low temperature thick oxide 5338 may be deposited and source, gate, and drain contacts, and thru layer via (not shown) openings may be

masked and etched preparing the transistors to be connected via metallization. Thus gate contact **5342** connects to gate electrode **5334**, and source & drain contacts **5336** connect to metal silicide source and drain regions **5326**.

[0629] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **53A** through **53I** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the temporary carrier substrate may be replaced by a carrier wafer and a permanently bonded carrier wafer flow such as, for example, as described in FIG. **40** may be employed. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0630] With the high density of layer to layer interconnection and the formation of memory devices & transistors that may be enabled by some embodiments in this document, novel FPGA (Field Programmable Gate Array) programming architectures and devices may be employed to create cost, area, and performance efficient 3D FPGAs. The pass transistor, or switch, and the memory device that controls the ON or OFF state of the pass transistor may reside in separate layers and may be connected by thru layer vias (TLVs) to each other and the routing network metal lines, or the pass transistor and memory devices may reside in the same layer and TLVs may be utilized to connect to the network metal lines.

[0631] As illustrated in FIG. **54A**, acceptor substrate **5400** may be processed to include logic circuits, analog circuits, and other devices, with metal interconnection and a metal configuration network to form the base FPGA. Acceptor substrate **5400** may include configuration elements such as, for example, switches, pass transistors, memory elements, programming transistors, and may contain a foundation layer or layers as described previously.

[0632] As illustrated in FIG. **54B**, donor wafer **5402** may be preprocessed with a layer or layers of pass transistors or switches or partially formed pass transistors or switches. The pass transistors may be constructed utilizing the partial transistor process flows described previously, such as, for example, RCAT or JLT or others, or may utilize the replacement gate techniques, such as, for example, CMOS or CMOS N over P or gate array, with or without a carrier wafer, as described previously. Donor wafer **5402** and acceptor substrate **5400** and associated surfaces may be prepared for wafer bonding as previously described.

[0633] As illustrated in FIG. **54C**, donor wafer **5402** and acceptor substrate **5400** may be bonded at a low temperature (less than approximately 400° C.) and a portion of donor wafer **5402** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining pass transistor layer **5402'**. Now transistors or portions of transistors may be formed or substantially completed and may be aligned to the acceptor substrate **5400** alignment marks (not shown) as described previously. Thru layer vias (TLVs) **5410** may be formed as described previously and as well as interconnect and dielectric layers. Thus acceptor substrate with pass transistors **5400A** may be formed, which may include acceptor substrate **5400**, pass transistor layer **5402'**, and TLVs **5410**.

[0634] As illustrated in FIG. **54D**, memory element donor wafer **5404** may be preprocessed with a layer or layers of memory elements or partially formed memory elements. The

memory elements may be constructed utilizing the partial memory process flows described previously, such as, for example, RCAT DRAM, JLT, or others, or may utilize the replacement gate techniques, such as, for example, CMOS gate array to form SRAM elements, with or without a carrier wafer, as described previously, or may be constructed with non-volatile memory, such as, for example, R-RAM or FG Flash as described previously. Memory element donor wafer **5404** and acceptor substrate with pass transistors **5400A** and associated surfaces may be prepared for wafer bonding as previously described.

[0635] As illustrated in FIG. **54E**, memory element donor wafer **5404** and acceptor substrate with pass transistors **5400A** may be bonded at a low temperature (less than approximately 400° C.) and a portion of memory element donor wafer **5404** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining memory element layer **5404'**. Now memory elements & transistors or portions of memory elements & transistors may be formed or substantially completed and may be aligned to the acceptor substrate with pass transistors **5400A** alignment marks (not shown) as described previously. Memory to switch thru layer vias **5420** and memory to acceptor thru layer vias **5430** as well as interconnect and dielectric layers may be formed as described previously. Thus acceptor substrate with pass transistors and memory elements **5400B** is formed, which may include acceptor substrate **5400**, pass transistor layer **5402'**, TLVs **5410**, memory to switch thru layer vias **5420**, memory to acceptor thru layer vias **5430**, and memory element layer **5404'**.

[0636] As illustrated in FIG. **54F**, a simple schematic of some elements of acceptor substrate with pass transistors and memory elements **5400B** is shown. An exemplary memory element **5440** residing in memory element layer **5404'** may be electrically coupled to exemplary pass transistor gate **5442**, residing in pass transistor layer **5402'**, with memory to switch thru layer vias **5420**. The pass transistor source **5444**, residing in pass transistor layer **5402'**, may be electrically coupled to FPGA configuration network metal line **5446**, residing in acceptor substrate **5400**, with TLV **5410A**. The pass transistor drain **5445**, residing in pass transistor layer **5402'**, may be electrically coupled to FPGA configuration network metal line **5447**, residing in acceptor substrate **5400**, with TLV **5410B**. The memory element **5440** may be programmed with signals from off chip, or above, within, or below the memory element layer **5404'**. The memory element **5440** may include an inverter configuration, wherein one memory cell, such as, for example, a FG Flash cell, may couple the gate of the pass transistor to power supply Vcc if turned on, and another FG Flash device may couple the gate of the pass transistor to ground if turned on. Thus, FPGA configuration network metal line **5446**, which may be carrying the output signal from a logic element in acceptor substrate **5400**, may be electrically coupled to FPGA configuration network metal line **5447**, which may route to the input of a logic element elsewhere in acceptor substrate **5400**.

[0637] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **54A** through **54F** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the memory element layer **5404'** may be constructed below pass transistor layer **5402'**. Additionally, the pass transistor layer **5402'** may include control and logic

circuitry in addition to the pass transistors or switches. Moreover, the memory element layer **5404'** may include control and logic circuitry in addition to the memory elements. Further, that the pass transistor element may instead be a transmission gate, or may be an active drive type switch. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

**[0638]** The pass transistor, or switch, and the memory device that controls the ON or OFF state of the pass transistor may reside in the same layer and TLVs may be utilized to connect to the network metal lines. As illustrated in FIG. **55A**, acceptor substrate **5500** may be processed to include logic circuits, analog circuits, and other devices, with metal interconnection and a metal configuration network to form the base FPGA. Acceptor substrate **5500** may include configuration elements such as, for example, switches, pass transistors, memory elements, programming transistors, and may contain a foundation layer or layers as described previously.

**[0639]** As illustrated in FIG. **55B**, donor wafer **5502** may be preprocessed with a layer or layers of pass transistors or switches or partially formed pass transistors or switches. The pass transistors may be constructed utilizing the partial transistor process flows described previously, such as, for example, RCAT or JLT or others, or may utilize the replacement gate techniques, such as, for example, CMOS or CMOS N over P or CMOS gate array, with or without a carrier wafer, as described previously. Donor wafer **5502** may be preprocessed with a layer or layers of memory elements or partially formed memory elements. The memory elements may be constructed utilizing the partial memory process flows described previously, such as, for example, RCAT DRAM or others, or may utilize the replacement gate techniques, such as, for example, CMOS gate array to form SRAM elements, with or without a carrier wafer, as described previously. The memory elements may be formed simultaneously with the pass transistor, for example, such as, for example, by utilizing a CMOS gate array replacement gate process where a CMOS pass transistor and an SRAM memory element, such as a 6-transistor memory cell, may be formed, or an RCAT pass transistor formed with an RCAT DRAM memory. Donor wafer **5502** and acceptor substrate **5500** and associated surfaces may be prepared for wafer bonding as previously described.

**[0640]** As illustrated in FIG. **55C**, donor wafer **5502** and acceptor substrate **5500** may be bonded at a low temperature (less than approximately 400° C.) and a portion of donor wafer **5502** may be removed by cleaving and polishing, or other processes as previously described, such as, for example, ion-cut or other methods, thus forming the remaining pass transistor & memory layer **5502'**. Now transistors or portions of transistors and memory elements may be formed or substantially completed and may be aligned to the acceptor substrate **5500** alignment marks (not shown) as described previously. Thru layer vias (TLVs) **5510** may be formed as described previously. Thus acceptor substrate with pass transistors & memory elements **5500A** is formed, which may include acceptor substrate **5500**, pass transistor & memory element layer **5502'**, and TLVs **5510**.

**[0641]** As illustrated in FIG. **55D**, a simple schematic of some elements of acceptor substrate with pass transistors & memory elements **5500A** is shown. An exemplary memory element **5540** residing in pass transistor & memory layer

**5502'** may be electrically coupled to exemplary pass transistor gate **5542**, also residing in pass transistor & memory layer **5502'**, with pass transistor & memory layer interconnect metallization **5525**. The pass transistor source **5544**, residing in pass transistor & memory layer **5502'**, may be electrically coupled to FPGA configuration network metal line **5546**, residing in acceptor substrate **5500**, with TLV **5510A**. The pass transistor drain **5545**, residing in pass transistor & memory layer **5502'**, may be electrically coupled to FPGA configuration network metal line **5547**, residing in acceptor substrate **5500**, with TLV **5510B**. The memory element **5540** may be programmed with signals from off chip, or above, within, or below the pass transistor & memory layer **5502'**. The memory element **5540** may include an inverter configuration, wherein one memory cell, such as, for example, a FG Flash cell, may couple the gate of the pass transistor to power supply Vcc if turned on, and another FG Flash device may couple the gate of the pass transistor to ground if turned on. Thus, FPGA configuration network metal line **5546**, which may be carrying the output signal from a logic element in acceptor substrate **5500**, may be electrically coupled to FPGA configuration network metal line **5547**, which may route to the input of a logic element elsewhere in acceptor substrate **5500**.

**[0642]** Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **55A** through **55D** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the pass transistor & memory layer **5502'** may include control and logic circuitry in addition to the pass transistors or switches and memory elements. Additionally, that the pass transistor element may instead be a transmission gate, or may be an active drive type switch. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

**[0643]** As illustrated in FIG. **56**, a non-volatile configuration switch with integrated floating gate (FG) Flash memory is shown. The control gate **5602** and floating gate **5604** may be common to both the sense transistor channel **5620** and the switch transistor channel **5610**. Switch transistor source **5612** and switch transistor drain **5614** may be coupled to the FPGA configuration network metal lines. The sense transistor source **5622** and the sense transistor drain **5624** may be coupled to the program, erase, and read circuits. This integrated NVM switch has been utilized by FPGA maker Actel Corporation and is manufactured in a high temperature (greater than approximately 400° C.) 2D embedded FG flash process technology.

**[0644]** As illustrated in FIG. **57A** to **57G**, a 1T NVM FPGA cell may be constructed with a single layer transfer of wafer sized doped layers and post layer transfer processing with a process flow that may be suitable for 3D IC manufacturing. This cell may be programmed with signals from off chip, or above, within, or below the cell layer.

**[0645]** As illustrated in FIG. **57A**, a P- substrate donor wafer **5700** may be processed to include two wafer sized layers of N+ doping **5704** and P- doping **5706**. The P- doped layer **5706** may have the same or a different dopant concentration than the P- substrate donor wafer **5700**. The doped layers may be formed by ion implantation and thermal anneal. The layer stack may alternatively be formed by successive epitaxially deposited doped silicon layers or by a combina-



tion of epitaxy and implantation and anneals. P- doped layer **5706** and N+ doped layer **5704** may have graded or various layers of doping to mitigate transistor performance issues, such as, for example, short channel effects, and enhance programming and erase efficiency. A screen oxide **5701** may be grown or deposited before an implant to protect the silicon from implant contamination and to provide an oxide surface for later wafer to wafer bonding. These processes may be done at temperatures above about 400° C. as the layer transfer to the processed substrate with metal interconnects has yet to be done. The N+ doped layer **5704** may have a doping concentration that may be more than 10× the doping concentration of P- doped layer **5704**.

[0646] As illustrated in FIG. **57B**, the top surface of P- substrate donor wafer **5700** may be prepared for oxide wafer bonding with a deposition of an oxide or by thermal oxidation of the P-doped layer **5706** to form oxide layer **5702**, or a re-oxidation of implant screen oxide **5701**. A layer transfer demarcation plane **5799** (shown as a dashed line) may be formed in P- substrate donor wafer **5700** (shown) or N+ doped layer **5704** by hydrogen implantation **5707**, or other methods as previously described. Both the P- substrate donor wafer **5700** and acceptor wafer **5710** may be prepared for wafer bonding as previously described and then low temperature (less than approximately 400° C.) bonded. The portion of the P- substrate donor wafer **5700** that may be above the layer transfer demarcation plane **5799** may be removed by cleaving and polishing, or other low temperature processes as previously described. This process of an ion implanted atomic species, such as, for example, Hydrogen, forming a layer transfer demarcation plane, and subsequent cleaving or thinning, may be called 'ion-cut'.

[0647] As illustrated in FIG. **57C**, the remaining N+ doped layer **5704'** and P- doped layer **5706**, and oxide layer **5702** have been layer transferred to acceptor wafer **5710**. The top surface of N+ doped layer **5704'** may be chemically or mechanically polished smooth and flat. Now FG and other transistors may be formed with low temperature (less than approximately 400° C.) processing and aligned to the acceptor wafer **5710** alignment marks (not shown). For illustration clarity, the oxide layers, such as, for example, oxide layer **5702**, used to facilitate the wafer to wafer bond are not shown in subsequent drawings.

[0648] As illustrated in FIG. **57D**, the transistor isolation regions may be lithographically defined and then formed by plasma/RIE etch removal of portions of N+ doped layer **5704'** and P- doped layer **5706** to at least the top oxide of acceptor substrate **5710**. Then a low-temperature gap fill oxide may be deposited and chemically mechanically polished, remaining in transistor isolation regions **5720** and SW-to-SE isolation region **5721**. "SW" in the FIG. **57** illustrations denotes that portion of the illustration where the switch transistor may be formed, and "SE" denotes that portion of the illustration where the sense transistor may be formed. Thus formed may be future SW transistor regions N+ doped **5714** and P- doped **5716**, and future SE transistor regions N+ doped **5715**, and P- doped **5717**.

[0649] As illustrated in FIG. **57E**, the SW recessed channel **5742** and SE recessed channel **5743** may be lithographically defined and etched, removing portions of future SW transistor regions N+ doped **5714** and P- doped **5716**, and future SE transistor regions N+ doped **5715**, and P-doped **5717**. The recessed channel surfaces and edges may be smoothed by wet chemical or plasma/RIE etching techniques to mitigate high

field effects. The SW recessed channel **5742** and SE recessed channel **5743** may be mask defined and etched separately or at the same step. The SW channel width may be larger than the SE channel width. These process steps form SW source and drain regions **5724**, SE source and drain regions **5725**, SW transistor channel region **5716** and SE transistor channel region **5717**, which may form the SE transistor body and SW transistor body. The doping concentration of the SW transistor channel region **5716** and SE transistor channel region **5717** may include gradients of concentration or layers of differing doping concentrations. The etch formation of SW recessed channel **5742** may define the SW transistor channel length. The etch formation of SE recessed channel **5743** may define the SE transistor channel length.

[0650] As illustrated in FIG. **57F**, a tunneling dielectric **5711** may be formed and a floating gate material may be deposited. The tunneling dielectric **5711** may be an atomic layer deposited (ALD) dielectric. Or the tunneling dielectric **5711** may be formed with a low temperature oxide deposition or low temperature microwave plasma oxidation of the silicon surfaces. Then a floating gate material, such as, for example, doped poly-crystalline or amorphous silicon, may be deposited. Then the floating gate material may be chemically mechanically polished, and the floating gate **5752** may be partially or fully formed by lithographic definition and plasma/RIE etching.

[0651] As illustrated in FIG. **57G**, an inter-poly dielectric **5741** may be formed by low temperature oxidation and depositions of a dielectric or layers of dielectrics, such as, for example, oxide-nitride-oxide (ONO) layers, and then a control gate material, such as, for example, doped poly-crystalline or amorphous silicon, may be deposited. The control gate material may be chemically mechanically polished, and the control gate **5754** may be formed by lithographic definition and plasma/RIE etching. The etching of control gate **5754** may include etching portions of the inter-poly dielectric and portions of the floating gate **5752** in a self-aligned stack etch process. Logic transistors for control functions may be formed (not shown) utilizing 3D IC compatible methods described in the document, such as, for example, RCAT, V-groove, and contacts, including thru layer vias, and interconnect metallization may be constructed. This flow enables the formation of a mono-crystalline silicon 1T NVM FPGA configuration cell constructed in a single layer transfer of prefabricated wafer sized doped layers, which may be formed and connected to the underlying multi-metal layer semiconductor device without exposing the underlying devices to a high temperature.

[0652] Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. **57A** through **57G** are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the floating gate may include nano-crystals of silicon or other materials. Additionally, a common well cell may be constructed by removing the SW-to-SE isolation region **5721**. Moreover, the slope of the recess of the channel transistor may be from zero to 180 degrees. Further, logic transistors and devices may be constructed by using the control gate as the device gate. Additionally, the logic device gate may be made separately from the control gate formation. Moreover, the 1T NVM FPGA configuration cell may be constructed with a charge trap technique NVM, a resistive memory technique, and may have a junction-less SW or SE transistor construction. Many other modifications within the

scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

**[0653]** The potential dicing streets, or scribe-lines, of 3D ICs may represent some loss of silicon area. The narrower the street the lower the loss is, and therefore, it may be potentially advantageous to use advanced dicing techniques that can create and work with narrow streets.

**[0654]** An advanced dicing technique may be the use of lasers for dicing the 3D IC wafers. Laser dicing techniques, including the use of water jets to cool the substrate and remove debris, may be employed to minimize damage to the 3D IC structures. Laser dicing techniques may be utilized to cut sensitive layers in the 3D IC, and then a conventional saw finish may be used.

**[0655]** Some embodiments of the invention may include alternative techniques to build IC (Integrated Circuit) devices including techniques and methods to construct 3D IC systems. Some embodiments of the invention may enable device solutions with far less power consumption than prior art. These device solutions could be very useful for the growing application of mobile electronic devices and mobile systems such as, for example, mobile phones, smart phone, and cameras, those mobile systems may also connect to the internet. For example, incorporating the 3D IC semiconductor devices according to some embodiments of the invention within these mobile electronic devices and mobile systems could provide superior mobile units that could operate much more efficiently and for a much longer time than with prior art technology.

**[0656]** Smart mobile systems may be greatly enhanced by complex electronics at a limited power budget. The 3D technology described in the multiple embodiments of the invention would allow the construction of low power high complexity mobile electronic systems. For example, it would be possible to integrate into a small form function a complex logic circuit with high density high speed memory utilizing some of the 3D DRAM embodiments of the invention and add some non-volatile 3D NAND charge trap or RRAM described in some embodiments of the invention.

**[0657]** In U.S. application Ser. No. 12/903,862, filed by some of the inventors and assigned to the same assignee, a 3D micro display and a 3D image sensor are presented. Integrating one or both of these with complex logic and or memory could be very effective for mobile system. Additionally, mobile systems could be customized to some specific market applications by integrating some embodiments of the invention.

**[0658]** Moreover, utilizing 3D programmable logic or 3D gate array as had been described in some embodiments of the invention could be very effective in forming flexible mobile systems.

**[0659]** The need to reduce power to allow effective use of limited battery energy and also the lightweight and small form factor derived by highly integrating functions with low waste of interconnect and substrate could be highly benefited by the redundancy and repair idea of the 3D monolithic technology as has been presented in embodiments of the invention. This unique technology could enable a mobile device that would be lower cost to produce or would require lower power to operate or would provide a lower size or lighter carry weight, and combinations of these 3D monolithic technology features may provide a competitive or desirable mobile system.

**[0660]** Another unique market that may be addressed by some of the embodiments of the invention could be a street corner camera with supporting electronics. The 3D image sensor described in the 12/903,862 application would be very effective for day/night and multi-spectrum surveillance applications. The 3D image sensor could be supported by integrated logic and memory such as, for example, a monolithic 3D IC with a combination of image processing and image compression logic and memory, both high speed memory such as 3D DRAM and high density non-volatile memory such as 3D NAND or RRAM or other memory, and other combinations. This street corner camera application would require low power, low cost, and low size or any combination of these features, and could be highly benefited from the 3D technologies described herein.

**[0661]** 3D ICs according to some embodiments of the invention could enable electronic and semiconductor devices with much a higher performance as a result from the shorter interconnect as well as semiconductor devices with far more complexity via multiple levels of logic and providing the ability to repair or use redundancy. The achievable complexity of the semiconductor devices according to some embodiments of the invention could far exceed what may be practical with the prior art technology. These potential advantages could lead to more powerful computer systems and improved systems that have embedded computers.

**[0662]** Some embodiments of the invention may enable the design of state of the art electronic systems at a greatly reduced non-recurring engineering (NRE) cost by the use of high density 3D FPGAs or various forms of 3D array based ICs with reduced custom masks as described herein. These systems could be deployed in many products and in many market segments. Reduction of the NRE may enable new product family or application development and deployment early in the product lifecycle by lowering the risk of upfront investment prior to a market being developed. The above potential advantages may also be provided by various mixes such as reduced NRE using generic masks for layers of logic and other generic masks for layers of memories and building a very complex system using the repair technology to overcome the inherent yield difficulties. Another form of mix could be building a 3D FPGA and add on it 3D layers of customizable logic and memory so the end system could have field programmable logic on top of the factory customized logic. There may be many ways to mix the many innovative elements to form 3D IC to support the needs of an end system, including using multiple devices wherein more than one device incorporates elements of embodiments of the invention. An end system could benefit from a memory devices utilizing the 3D memory of some embodiments of the invention together with high performance 3D FPGA of some of the embodiments of the invention together with high density 3D logic and so forth. Using devices that can use one or multiple elements according to some embodiments of the invention may allow for increased performance or lower power and other potential advantages resulting from the use of some embodiments of the inventions to provide the end system with a competitive edge. Such end system could be electronic based products or other types of systems that may include some level of embedded electronics, such as, for example, cars and remote controlled vehicles.

**[0663]** Commercial wireless mobile communications have been developed for almost thirty years, and play a special role in today's information and communication technology

Industries. The mobile wireless terminal device has become part of our life, as well as the Internet, and the mobile wireless terminal device may continue to have a more important role on a worldwide basis. Currently, mobile (wireless) phones are undergoing much development to provide advanced functionality. The mobile phone network is a network such as a GSM, GPRS, or WCDMA, 3G and 4G standards, and the network may allow mobile phones to communicate with each other. The base station may be for transmitting (and receiving) information to the mobile phone.

**[0664]** A typical mobile phone system may include, for example, a processor, a flash memory, a static random access memory, a display, a removable memory, a radio frequency (RF) receiver/transmitter, an analog base band (ABB), a digital base band (DBB), an image sensor, a high-speed bi-directional interface, a keypad, a microphone, and a speaker. A typical mobile phone system may include a multiplicity of an element, for example, two or more static random access memories, two or more displays, two or more RF receiver/transmitters, and so on.

**[0665]** Conventional radios used in wireless communications, such as radios used in conventional cellular telephones, typically may include several discrete RF circuit components. Some receiver architectures may employ superhetrodyne techniques. In a superhetrodyne architecture an incoming signal may be frequency translated from its radio frequency (RF) to a lower intermediate frequency (IF). The signal at IF may be subsequently translated to baseband where further digital signal processing or demodulation may take place. Receiver designs may have multiple IF stages. The reason for using such a frequency translation scheme is that circuit design at the lower IF frequency may be more manageable for signal processing. It is at these IF frequencies that the selectivity of the receiver may be implemented, automatic gain control (AGC) may be introduced, etc.

**[0666]** A mobile phone's need of a high-speed data communication capability in addition to a speech communication capability has increased in recent years. In GSM (Global System for Mobile communications), one of European Mobile Communications Standards, GPRS (General Packet Radio Service) has been developed for speeding up data communication by allowing a plurality of time slot transmissions for one time slot transmission in the GSM with the multiplexing TDMA (Time Division Multiple Access) architecture. EDGE (Enhanced Data for GSM Evolution) architecture provides faster communications over GPRS.

**[0667]** 4th Generation (4G) mobile systems aim to provide broadband wireless access with nominal data rates of 100 Mbit/s. 4G systems may be based on the 3GPP LTE (Long Term Evolution) cellular standard, WiMax or Flash-OFDM wireless metropolitan area network technologies. The radio interface in these systems may be based on all-IP packet switching, MIMO diversity, multi-carrier modulation schemes, Dynamic Channel Assignment (DCA) and channel-dependent scheduling.

**[0668]** Prior art such as U.S. application Ser. No. 12/871, 984 may provide a description of a mobile device and its block-diagram.

**[0669]** It is understood that the use of specific component, device and/or parameter names (such as those of the executing utility/logic described herein) are for example only and not meant to imply any limitations on the invention. The invention may thus be implemented with different nomenclature/terminology utilized to describe the components/de-

vices/parameters herein, without limitation. Each term utilized herein is to be given its broadest interpretation given the context in which that term is utilized. For example, as utilized herein, the following terms are generally defined:

**[0670]** (1) Mobile computing/communication device (MCD): is a device that may be a mobile communication device, such as a cell phone, or a mobile computer that performs wired and/or wireless communication via a connected wireless/wired network. In some embodiments, the MCD may include a combination of the functionality associated with both types of devices within a single standard device (e.g., a smart phones or personal digital assistant (PDA)) for use as both a communication device and a computing device.

**[0671]** A block diagram representation of an exemplary mobile computing device (MCD) is illustrated in FIG. 59, within which several of the features of the described embodiments may be implemented. MCD 5900 may be a desktop computer, a portable computing device, such as a laptop, personal digital assistant (PDA), a smart phone, and/or other types of electronic devices that may generally be considered processing devices. As illustrated, MCD 5900 may include at least one processor or central processing unit (CPU) 5902 which may be connected to system memory 5906 via system interconnect/bus 5904. CPU 5902 may include at least one digital signal processing unit (DSP). Also connected to system interconnect/bus 5904 may be input/output (I/O) controller 5915, which may provide connectivity and control for input devices, of which pointing device (or mouse) 5916 and keyboard 5917 are illustrated. I/O controller 5915 may also provide connectivity and control for output devices, of which display 5918 is illustrated. Additionally, a multimedia drive 5919 (e.g., compact disk read/write (CDRW) or digital video disk (DVD) drive) and USB (universal serial bus) port 5920 are illustrated, and may be coupled to I/O controller 5915. Multimedia drive 5919 and USB port 5920 may enable insertion of a removable storage device (e.g., optical disk or "thumb" drive) on which data/instructions/code may be stored and/or from which data/instructions/code may be retrieved. MCD 5900 may also include storage 5922, within/from which data/instructions/code may also be stored/retrieved. MCD 5900 may further include a global positioning system (GPS) or local position system (LPS) detection component 5924 by which MCD 5900 may be able to detect its current location (e.g., a geographical position) and movement of MCD 5900, in real time. MCD 5900 may include a network/communication interface 5925, by which MCD 5900 may connect to one or more second communication devices 5932 or to wireless service provider server 5937, or to a third party server 5938 via one or more access/external communication networks, of which a wireless Communication Network 5930 is provided as one example and the Internet 5936 is provided as a second example. It is appreciated that MCD 5900 may connect to third party server 5938 through an initial connection with Communication Network 5930, which in turn may connect to third party server 5938 via the Internet 5936.

**[0672]** In addition to the above described hardware components of MCD 5900, various features of the described embodiments may be completed/supported via software (or firmware) code or logic stored within system memory 5906 or other storage (e.g., storage 5922) and may be executed by CPU 5902. Thus, for example, illustrated within system memory 5906 are a number of software/firmware/logic components, including operating system (OS) 5908 (e.g.,

Microsoft Windows® or Windows Mobile®, trademarks of Microsoft Corp, or GNU®/Linux®, registered trademarks of the Free Software Foundation and The Linux Mark Institute, and AIX®, registered trademark of International Business Machines), and (word processing and/or other) application(s) **5909**. Also illustrated are a plurality (four illustrated) software implemented utilities, each providing different one of the various functions (or advanced features) described herein. Including within these various functional utilities are: Simultaneous Text Waiting (STW) utility **5911**, Dynamic Area Code Pre-pending (DACP) utility **5912**, Advanced Editing and Interfacing (AEI) utility **5912** and Safe Texting Device Usage (STDU) utility **5914**. In actual implementation and for simplicity in the following descriptions, each of these different functional utilities are assumed to be packaged together as sub-components of a general MCD utility **5910**, and the various utilities are interchangeably referred to as MCD utility **5910** when describing the utilities within the figures and claims. For simplicity, the following description will refer to a single utility, namely MCD utility **5910**. MCD utility **5910** may, in some embodiments, be combined with one or more other software modules, including for example, word processing application(s) **5909** and/or OS **5908** to provide a single executable component, which then may provide the collective functions of each individual software component when the corresponding combined code of the single executable component is executed by CPU **5902**. Each separate utility **111/112/113/114** is illustrated and described as a standalone or separate software/firmware component/module, which provides specific functions, as described below. As a standalone component/module, MCD utility **5910** may be acquired as an off-the-shelf or after-market or downloadable enhancement to existing program applications or device functions, such as voice call waiting functionality (not shown) and user interactive applications with editable content, such as, for example, an application within the Windows Mobile® suite of applications. In at least one implementation, MCD utility **5910** may be downloaded from a server or website of a wireless provider (e.g., wireless service provider server **5937**) or a third party server **5938**, and either installed on MCD **5900** or executed from the wireless service provider server **5937** or third party server **5913**.

**[0673]** CPU **5902** may execute MCD utility **5910** as well as OS **5908**, which, in one embodiment, may support the user interface features of MCD utility **5910**, such as generation of a graphical user interface (GUI), where required/supported within MCD utility code. In several of the described embodiments, MCD utility **5910** may generate/provide one or more GUIs to enable user interaction with, or manipulation of, functional features of MCD utility **5910** and/or of MCD **5900**. MCD utility **5910** may, in certain embodiments, enable certain hardware and firmware functions and may thus be generally referred to as MCD logic.

**[0674]** Some of the functions supported and/or provided by MCD utility **5910** may be enabled as processing code/instructions/logic executing on DSP/CPU **5902** and/or other device hardware, and the processor thus may complete the implementation of those function(s). Among, for example, the software code/instructions/logic provided by MCD utility **5910**, and which are specific to some of the described embodiments of the invention, may be code/logic for performing several (one or a plurality) of the following functions: (1) Simultaneous texting during ongoing voice communication providing a text waiting mode for both single number mobile com-

munication devices and multiple number mobile communication devices; (2) Dynamic area code determination and automatic back-filling of area codes when a requested/desired voice or text communication is initiated without the area code while the mobile communication device is outside of its home-base area code toll area; (3) Enhanced editing functionality for applications on mobile computing devices; (4) Automatic toggle from manual texting mode to voice-to-text based communication mode on detection of high velocity movement of the mobile communication device; and (5) Enhanced e-mail notification system providing advanced e-mail notification via (sender or recipient directed) texting to a mobile communication device.

**[0675]** Utilizing monolithic 3D IC technology described herein and in related application Ser. Nos. 12/903,862, 12/903,847, 12/904,103 and 13/041,405 significant power and cost could be saved. Most of the elements in MCD **5900** could be integrated in one 3D IC. Some of the MCD **5900** elements may be logic functions which could utilize monolithic 3D transistors such as, for example, RCAT or Gate-Last. Some of the MCD **5900** elements are storage devices and could be integrated on a 3D non-volatile memory device, such as, for example, 3D NAND or 3D RRAM, or volatile memory such as, for example, 3D DRAM or SRAM formed from RCAT or gate-last transistors, as been described herein. Storage **5922** elements formed in monolithic 3D could be integrated on top or under a logic layer to reduce power and space. Keyboard **5917** could be integrated as a touch screen or combination of image sensor and some light projection and could utilize structures described in some of the above mentioned related applications. The network/communication interface **5925** could utilize another layer of silicon optimized for RF and gigahertz speed analog circuits or even may be integrated on substrates, such as GaN, that may be a better fit for such circuits. As more and more transistors might be integrated to achieve a high complexity 3D IC system there might be a need to use some embodiments of the invention such as what were called repair and redundancy so to achieve good product yield.

**[0676]** Some of the system elements including non-mobile elements, such as the 3rd Party Server **5938**, might also make use of some embodiments of the 3D IC inventions including repair and redundancy to achieve good product yield for high complexity and large integration. Such large integration may reduce power and cost of the end product which is most attractive and most desired by the system end-use customers.

**[0677]** Some embodiments of the 3D IC invention could be used to integrate many of the MCD **5900** blocks or elements into one or a few devices. As various blocks get tightly integrated, much of the power required to transfer signals between these elements may be reduced and similarly costs associated with these connections may be saved. Form factor may be compacted as the space associated with the individual substrate and the associated connections may be reduced by use of some embodiments of the 3D IC invention. For mobile device these may be very important competitive advantages. Some of these blocks might be better processed in different process flow or wafer fab location. For example the DSP/CPU **5902** is a logic function that might use a logic process flow while the storage **5922** might better be done using a NAND Flash technology process flow or wafer fab. An important advantage of some of the embodiments of the monolithic 3D inventions may be to allow some of the layers in the 3D structure to be processed using a logic process flow while

another layer in the 3D structure might utilize a memory process flow, and then some other function the modems of the GPS or local position system (LPS) detection component 5924 might use a high speed analog process flow or wafer fab. As those diverse functions may be structured in one device onto many different layers, these diverse functions could be very effectively and densely vertically interconnected.

[0678] FIG. 60 illustrates an exemplary monolithic 3D integrated circuit. Two mono-crystalline silicon layers, 6004 and 6016 are shown. Mono-crystalline silicon layer 6016 could have a thickness in the range of approximately 2 nm to approximately 1  $\mu$ m. Mono-crystalline Silicon layer 6004, or silicon substrate, may include transistors which could have gate electrode region 6014, gate dielectric region 6012, and transistor junction regions 6010. Mono-crystalline silicon layer 6016 may include transistors which could have gate electrode region 6034, gate dielectric region 6032, and transistor junction regions 6030. A through-silicon connection 6018, or TLV (through-silicon via) could be present and may have a surrounding dielectric region 6020. Surrounding dielectric region 6020 may comprise a shallow trench isolation (STI) region, such as one of the many shallow trench isolation (STI) regions typically in a 3D integrated circuit stack (not shown). Mono-crystalline silicon layer 6004 may have wiring layers 6008 and wiring dielectric 6006. Mono-crystalline silicon layer 6016 may have wiring layers 6038 and wiring dielectric 6036. Wiring layer 6038 and wiring layer 6008 may be constructed of copper, aluminum or other materials with bulk resistivity lower than 2.8 uohm-cm. The choice of materials for through-silicon connection 6018 may be challenging. If copper is chosen as the material for through-silicon connection 6018, the co-efficient of thermal expansion (CTE) mismatch between copper and the surrounding mono-crystalline silicon layer 6016 may become an issue. Copper has a CTE of approximately 16.7 ppm/K while silicon has a CTE of approximately 3.2 ppm/K. This large CTE mismatch can cause reliability issues and large keep-out zones around the through-silicon connection 6018 whereby transistors cannot be placed. If transistors are placed within the keep-out zone of the through-silicon connections 6018, their current-voltage characteristics may be different from those placed in other areas of the chip. Similarly, if Aluminum (CTE=23 ppm/K) is used as the material for through-silicon connection 6018, its CTE mismatch with the surrounding mono-crystalline silicon layer 6016 could cause large keep-out zones and reliability issues.

[0679] An embodiment of the invention utilizes a material for the through-silicon connection 6018 that may have a CTE closer to silicon than, for example, copper or aluminum. The through-silicon connection 6018 may include materials such as, for example, tungsten (CTE approximately 4.5 ppm/K), highly doped polysilicon or amorphous silicon or single crystal silicon (CTE approximately 3 ppm/K), conductive carbon, or some other material with CTE less than 15 ppm/K. Wiring layers 6038 and wiring layers 6008 may have materials with CTE greater than 15 ppm/K, such as, for example, copper or aluminum.

[0680] According to an embodiment of this invention, the transistors in mono-crystalline silicon layer 6016 may be constructed using techniques similar to those described in U.S. patent application Ser. No. 13/273,712, incorporated herein by reference, as well as this document herein.

[0681] Persons of ordinary skill in the art will appreciate that the illustrations in FIG. 60 are exemplary only and are not

drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the through-silicon connection 6018 may include materials in addition to those (such as Tungsten, conductive carbon) described above, for example, liners and barrier metals such as TiN, TaN, and other materials known in the art for via, contact, and through silicon via formation. Moreover, the transistors in monocrystalline layer 6004 may be formed in a manner similar to mono-crystalline layer 6016. Furthermore, through-silicon connection 6018 may be physically and electrically connected (not shown) to wiring layers 6008 and 6038 by the same material as the wiring layers 6008/6038, or by the same materials as the through-silicon connection 6018 composition, or by other electrically and/or thermally conductive materials not found in either the wiring layers 6008/6038 or the through-silicon connection 6018. Many other modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0682] Ion-cut may require anneals to remove defects at temperatures higher than 400° C., so techniques to remove defects without the acceptor wafer seeing temperatures higher than 400° C. may be required. FIG. 61 illustrates an embodiment of this invention, wherein such a technique is described. As illustrated in FIG. 61, perforated carrier substrate 6100 may include perforations 6112, which may cover a portion of the entire surface of perforated carrier substrate 6100. The portion by area of perforations 6112 that may cover the entire surface of perforated carrier substrate 6100 may range from about 5% to about 60%, typically in the range of about 10-20%. The nominal diameter of perforations 6112 may range from about 1 micron to about 200 microns, typically in the range of about 5 microns to about 50 microns. Perforations 6112 may be formed by lithographic and etching methods or by using laser drilling. As illustrated in cross section I of FIG. 61, perforated carrier substrate 6100 may include perforations 6112 which may extend substantially through carrier substrate 6110 and carrier substrate bonding oxide 6108. Carrier substrate 6110 may include, for example, monocrystalline silicon wafers, high temperature glass wafers, germanium wafers, InP wafers, or high temperature polymer substrates. Perforated carrier substrate 6100 may be utilized as and called carrier wafer or carrier substrate or carrier herein this document. Desired layer transfer substrate 6104 may be prepared for layer transfer by ion implantation of an atomic species, such as Hydrogen, which may form layer transfer demarcation plane 6106, represented by a dashed line in the illustration. Layer transfer substrate bonding oxide 6102 may be deposited on top of desired layer transfer substrate 6104. Layer transfer substrate bonding oxide 6102 may be deposited at temperatures below about 250° C. to minimize out-diffusion of the hydrogen that may have formed the layer transfer demarcation plane 6106. Layer transfer substrate bonding oxide 6102 may be deposited prior to the ion implantation, or may utilize a preprocessed oxide that may be part of desired layer transfer substrate 6104, for example, the ILD of a gate-last partial transistor layer. Desired layer transfer substrate 6104 may include any layer transfer devices and/or layer or layers contained herein this document, for example, the gate-last partial transistor layers, DRAM Si/SiO<sub>2</sub> layers, sub-stack layers of circuitry, RCAT doped layers, or starting material doped monocrystalline silicon. Carrier substrate bonding oxide 6108 and layer transfer

substrate bonding oxide **6102** may be prepared for oxide to oxide bonding, for example, for low temperature (less than about 400° C.) or high temperature (greater than about 400° C.) oxide to oxide bonding, as has been described elsewhere herein.

[0683] As illustrated in FIG. 61, perforated carrier substrate **6100** may be oxide to oxide bonded to desired layer transfer substrate **6104** at carrier substrate bonding oxide **6108** and layer transfer substrate bonding oxide **6102**, thus forming cleaving structure **6190**. Cleaving structure **6190** may include layer transfer substrate bonding oxide **6102**, desired layer transfer substrate **6104**, layer transfer demarcation plane **6106**, carrier substrate bonding oxide **6108**, carrier substrate **6110**, and perforations **6112**.

[0684] As illustrated in FIG. 61, cleaving structure **6190** may be cleaved at layer transfer demarcation plane **6106**, removing a portion of desired layer transfer substrate **6104**, and leaving desired transfer layer **6114**, and may be defect annealed, thus forming defect annealed cleaved structure **6192**. Defect annealed cleaved structure **6192** may include layer transfer substrate bonding oxide **6102**, carrier substrate bonding oxide **6108**, carrier substrate **6110**, desired transfer layer **6114**, and perforations **6112**. The cleaving process may include thermal, mechanical, or other methods described elsewhere herein. Defect annealed cleaved structure **6192** may be annealed so to repair the defects in desired transfer layer **6114**. The defect anneal may include a thermal exposure to temperatures above about 400° C. (a high temperature thermal anneal), including, for example, 600° C., 800° C., 900° C., 1000° C., 1050° C., 1100° C. and/or 1120° C. The defect anneal may include an optical anneal, including, for example, laser anneals, Rapid Thermal Anneal (RTA), flash anneal, and/or dual-beam laser spike anneals. The defect anneal ambient may include, for example, vacuum, high pressure (greater than about 760 torr), oxidizing atmospheres (such as oxygen or partial pressure oxygen), and/or reducing atmospheres (such as nitrogen or argon). The defect anneal may include Ultrasound Treatments (UST). The defect anneal may include microwave treatments. The defect anneal may include other defect reduction methods described herein this document or in U.S. patent application Ser. No. 13/273,712 incorporated herein by reference. The defect anneal may repair defects, such as those caused by the ion-cut ion implantation, in transistor gate oxides or junctions and/or other devices such as capacitors which may be pre-formed and residing in desired transfer layer **6114** at the time of the ion-cut implant. The exposed (“bottom”) surface of desired transfer layer **6114** may be thermally oxidized and/or oxidized using radical oxidation to form defect annealed cleaved structure bonding oxide **6116**. These techniques may smoothen the surface and reduce the surface roughness after cleave.

[0685] As illustrated in FIG. 61, defect annealed cleaved structure **6192** may be oxide to oxide bonded to acceptor wafer or substrate **6120**, thus forming 3D stacked layers with carrier wafer structure **6194**. 3D stacked layers with carrier wafer structure **6194** may include acceptor wafer or substrate **6120**, acceptor bonding oxide **6118**, defect annealed cleaved structure bonding oxide **6116**, desired transfer layer **6114**, layer transfer substrate bonding oxide **6102**, carrier substrate bonding oxide **6108**, carrier substrate **6110**, and perforations **6112**. Acceptor bonding oxide **6118** may be deposited onto acceptor wafer or substrate **6120** and may be prepared for oxide to oxide bonding, for example, for low temperature

(less than about 400° C.) or high temperature (greater than about 400° C.) oxide to oxide bonding, as has been described elsewhere herein. Defect annealed cleaved structure bonding oxide **6116** may be prepared for oxide to oxide bonding, for example, for low temperature (less than about 400° C.) or high temperature (greater than about 400° C.) oxide to oxide bonding, as has been described elsewhere herein. Acceptor wafer or substrate **6120** may include layer or layers, or regions, of preprocessed circuitry, such as, for example, logic circuitry, microprocessors, MEMS, circuitry comprising transistors of various types, and other types of digital or analog circuitry including, but not limited to, the various embodiments described herein or in U.S. patent application Ser. No. 13/273,712 incorporated herein by reference, such as gate last transistor formation. Acceptor wafer or substrate **6120** may include preprocessed metal interconnects including copper, aluminum, and/or tungsten, but not limited to, the various embodiments described herein, such as, for example, peripheral circuitry substrates for 3D DRAM or metal strips/pads for 3D interconnection with TLVs or TSVs. Acceptor wafer or substrate **6120** may include layer or layers of monocrystalline silicon that may be doped or undoped, including, but not limited to, the various embodiments described herein, such as, for example, for 3D DRAM, 3D NAND, or 3D RRAM formation. Acceptor wafer or substrate **6120** may include relatively inexpensive glass substrates, upon which partially or fully processed solar cells formed in monocrystalline silicon may be bonded. Acceptor wafer or substrate **6120** may include alignment marks, which may be utilized to form transistors in layers in the 3D stack, for example, desired transfer layer **6114**, and the alignment marks may be used to form connections paths from transistors and transistor contacts within desired transfer layer **6114** to acceptor substrate circuitry or metal strips/pads within acceptor wafer or substrate **6120**, by forming, for example, TLVs or TSVs. Acceptor bonding oxide **6118** and defect annealed cleaved structure bonding oxide **6116** may form an isolation layer between desired transfer layer **6114** and acceptor wafer or substrate **6120**.

[0686] As illustrated in FIG. 61, carrier substrate **6110** with carrier substrate bonding oxide **6108** and perforations **6112**, may be released (lifted off) from the bond with acceptor wafer or substrate **6120**, acceptor bonding oxide **6118**, defect annealed cleaved structure bonding oxide **6116**, desired transfer layer **6114**, and layer transfer substrate bonding oxide **6102**, thus forming 3D stacked layers structure **6196**. 3D stacked layers structure **6196** may include acceptor wafer or substrate **6120**, acceptor bonding oxide **6118**, defect annealed cleaved structure bonding oxide **6116**, and desired transfer layer **6114**. The bond release, or debond, may utilize a wet chemical etch of the bonding oxides, such as layer transfer substrate bonding oxide **6102** and carrier substrate bonding oxide **6108**, which may include, for example, 20:1 buffered H<sub>2</sub>O:HF, or vapor HF, or other debond/release etchants that may selectively etch the bonding oxides over the desired transfer layer **6114** and acceptor wafer or substrate **6120** material (which may include monocrystalline silicon). The debond/release etchant may substantially access the bonding oxides, such as layer transfer substrate bonding oxide **6102** and carrier substrate bonding oxide **6108**, by travelling through perforations **6112**. The debond/release etchant may be heated above room temperature to increase etch rates. The wafer edge sidewalls of acceptor bonding oxide **6118**, defect annealed cleaved structure bonding oxide

**6116**, desired transfer layer **6114**, and acceptor wafer or substrate **6120** may be protected from the debond/release etchant by a sidewall resist coating or other materials which do not etch quickly upon exposure to the debond/release etchant, such as, for example, silicon nitride or organic polymers such as wax or photoresist. 3D stacked layers structure **6196** may continue 3D processing the defect annealed desired transfer layer **6114** and acceptor wafer or substrate **6120** including, but not limited to, the various embodiments described herein, or in U.S. patent application Ser. No. 13/273,712 incorporated herein by reference such as stacking Si/SiO<sub>2</sub> layers as in 3D DRAM, 3D NAND, or RRAM formation, RCAT formation, continuous array and FPGA structures, gate array, memory blocks, solar cell completion, or gate last transistor completion formation, and may include forming transistors, for example, CMOS p-type and n-type transistors. Continued 3D processing may include forming junction-less transistors, replacement gate transistors, thin-side-up transistors, double gate transistors, horizontally oriented transistors, finfet transistors, JLRCAT, DSS Schottky transistors, and/or trench MOSFET transistors as described by various embodiments herein. Continued 3D processing may include the custom function etching for a specific use as described, for example, in FIG. 183 and FIG. 84 of U.S. patent application Ser. No. 13/273,712 incorporated herein by reference, and may include etching to form scribelines or dice lines. Continued 3D processing may include etching to form memory blocks, for example, as described in FIGS. 195, 196, 205-210 of U.S. patent application Ser. No. 13/273,712 incorporated herein by reference. Continued 3D processing may include forming metal interconnects, such as, for example, aluminum or copper, within or on top of the defect annealed desired transfer layer **6114**, and may include forming connections paths from transistors and transistor contacts within desired transfer layer **6114** to acceptor substrate circuitry or metal strips/pads within acceptor wafer or substrate **6120**, by forming, for example, TLVs or TSVs. Thermal contacts which may conduct heat but not electricity may be formed and utilized as described in FIG. 162 through FIG. 166 of U.S. patent application Ser. No. 13/273,712 incorporated herein by reference. Carrier substrate **6110** with perforations **6112** may be used again ('reused' or 'recycled') for the defect anneal process flow.

[0687] Persons of ordinary skill in the art will appreciate that the illustrations in FIG. 61 are exemplary and are not drawn to scale. Such skilled persons will further appreciate that many variations may be possible such as, for example, perforations **6112** may evenly cover the entire surface of perforated carrier substrate **6100** with substantially equal distances between perforations **6112**, or may have unequal spacing and coverage, such as, less or more density of perforations **6112** near the wafer edge. Moreover, perforations **6112** may extend substantially through carrier substrate **6110** and not extend through carrier substrate bonding oxide **6108**. Further, perforations **6112** may be formed in perforated carrier substrate **6100** by methods, for example, such as laser drilling or ion etching, such as Reactive Ion Etching (RIE). Moreover, the cross sectional cut shape of perforations **6112** may be tapered, with the widest diameter of the perforation towards where the etchant may be supplied, which may be accomplished by, for example, inductively coupled plasma (ICP) etching or vertically controlled shaped laser drilling. Further, perforations **6112** may have top view shapes other than circles; they may be oblong, ovals, squares, or rectangles for

example, and may not be of uniform shape across the face of perforated carrier substrate **6100**. Furthermore, perforations **6112** may include a material coating, such as thermal oxide, to enhance wicking of the debond/release etchant, and may include micro-roughening of the perforation interiors, by methods such as plasma or wet silicon etchants or ion bombardment, to enhance wicking of the debond/release etchant. Moreover, the thickness of carrier substrate **6110**, such as, for example, the 750 micron nominal thickness of a 300 mm single crystal silicon wafer, may be adjusted to optimize the technical and operational trades of attributes such as, for example, debond etchant access and debond time, strength of carrier substrate **6110** to withstand thin film stresses, CMP shear forces, and the defect anneal thermal stresses, carrier substrate **6110** reuse/recycling lifetimes, and so on. Furthermore, preparation of desired layer transfer substrate **6104** for layer transfer may utilize flows and processes described herein this document. Moreover, bonding methods other than oxide to oxide, such as oxide to metal (Titanium/TiN) to oxide, or nitride to oxide, may be utilized. Further, acceptor wafer or substrate **6120** may include a wide variety of materials and constructions, for example, from undoped or doped single crystal silicon to 3D sub-stacks. Furthermore, the exposed ("bottom") surface of desired transfer layer **6114** may be smoothed with techniques such as gas cluster ion beams, or radical oxidations utilizing, for example, the TEL SPA tool. Further, the exposed ("bottom") surface of desired transfer layer **6114** may be smoothed with "epi smoothing" techniques, whereby, for example, high temperature (about 900-1250° C.) etching with hydrogen or HCL may be coupled with epitaxial deposition of silicon. Moreover, the bond release etchant may include plasma etchant chemistries that are selective etchants to oxide and not silicon, such as, for example, CHF<sub>3</sub> plasmas. Furthermore, a combination of etchant release and mechanical force may be employed to debond/release the carrier substrate **6110** from acceptor wafer or substrate **6120** and desired transfer layer **6114**. Moreover, carrier substrate **6110** may be thermally oxidized before and/or after deposition of carrier substrate bonding oxide **6108** and/or before and/or after perforations **6112** are formed. Further, the total oxide thickness of carrier substrate bonding oxide **6108** plus layer transfer substrate bonding oxide **6102** may be adjusted to make technical and operational trades between attributes, for example, such as debond time, carrier wafer perforation spacing, and thin film stress, and the total oxide thickness may be about 1 micron or about 2 micron or about 5 microns or less than 1 micron. Moreover, the composition of carrier substrate bonding oxide **6108** and layer transfer substrate bonding oxide **6102** may be varied to increase lateral etch time; for example, by changing the vertical and/or lateral oxide density and/or doping with dopants carbon, boron, phosphorous, or by deposition rate and techniques such as PECVD, SACVD, APCVD, SOG spin & cure, and so on. Furthermore, carrier substrate bonding oxide **6108** and layer transfer substrate bonding oxide **6102** may include multiple layers of oxide and types of oxides (for example 'low-k'), and may have other thin layers inserted, such as, for example, silicon nitride, to speed lateral etching in HF solutions, or Titanium to speed lateral etch rates in hydrogen peroxide solutions. Further, the wafer edge sidewalls of acceptor bonding oxide **6118** and defect annealed cleaved structure bonding oxide **6116** may not need debond/release etchant protection; depending on the design and placement of perforations **6112**, design/layout keep-out zones and edge

bead considerations, and the type of debond/release etchant, the wafer edge undercut may not be harmful. Moreover, a debond/release etchant resistant material, such as silicon nitride, may be deposited over substantially all or some of the exposed surfaces of acceptor wafer or substrate **6120** prior to deposition of acceptor bonding oxide **6118**. Further, desired layer transfer substrate **6104** may be an SOI or GeOI substrate base and, for example, an ion-cut process may be used to form layer transfer demarcation plane **6106** in the bulk substrate of the SOI wafer and cleaving proceeds as described in FIG. **61**, or after bonding with the carrier the SOI wafer may be sacrificially etched/CMP'd off with no ion-cut implant and the damage repair may not be needed (described elsewhere herein). Many other modifications within the scope of the illustrated embodiments of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

**[0688]** FIG. **63** illustrates an embodiment of the invention wherein sub-threshold circuits may be stacked above or below a logic chip layer. The 3DIC illustrated in FIG. **63** may include input/output interconnect **6308**, such as, for example, solder bumps and a packaging substrate **6302**, logic layer **6306**, and sub-threshold circuit layer **6304**. The 3DIC may place logic layer **6306** above sub-threshold circuit layer **6304** and they may be connected with through-layer vias (TLVs) as described elsewhere herein. Alternatively, the logic and sub-threshold layers may be swapped in position, for example, logic layer **6306** may be a sub-threshold circuit layer and sub-threshold circuit layer **6304** may be a logic layer. The sub-threshold circuit layer **6304** may include repeaters of a chip with level shifting of voltages done before and after each repeater stage or before and after some or all of the repeater stages in a certain path are traversed. Alternatively, the sub-threshold circuit layer may be used for SRAM. Alternatively, the sub-threshold circuit layer may be used for some part of the clock distribution, such as, for example, the last set of buffers driving latches in a clock distribution. Although the term sub-threshold is used for describing elements in FIG. **63**, it will be obvious to one skilled in the art that similar approaches may be used when the supply voltage for the stacked layers is slightly above the threshold voltage values and may be utilized to increase voltage toward the end of a clock cycle for a better latch. In addition, the sub-threshold circuit layer stacked above or below the logic layer may include optimized transistors that may have lower capacitance, for example, if it is used for clock distribution purposes.

**[0689]** As illustrated in FIG. **64A-D**, a description of a prior art shallow trench isolation (STI) process is shown. The process flow for forming the integrated circuit or structure may include the following steps that occur in sequence from Step (A) to Step (D). When the same reference numbers are used in different drawing figures (among FIG. **64A-D**), they may indicate analogous, similar or identical structures to enhance the understanding of the embodiments of the invention being discussed by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

**[0690]** As illustrated in FIG. **64A** (Step A), a silicon wafer **6402** suitable for integrated circuit or structure formation may be constructed.

**[0691]** As illustrated in FIG. **64B** (Step B), a silicon nitride layer may be formed on top of silicon wafer **6402** using a process such as chemical vapor deposition (CVD) and may then be lithographically patterned. Following this, an etch process removing the regions of silicon nitride and the silicon wafer **6402** may be conducted to form trench **6410** and silicon nitride regions **6406**. The silicon region **6408** may remain after these process steps. A silicon oxide (not shown) may be utilized as a stress relief layer between the silicon nitride regions **6406** and silicon wafer **6402**. Etch resistant materials, such as, for example, amorphous carbon, may be utilized in place of or in addition to the silicon nitride layer and subsequently formed silicon nitride regions **6406**.

**[0692]** As illustrated using FIG. **64C** (Step C), a thermal oxidation process at greater than about 700° C. may be conducted to form oxide region **6412**. The silicon nitride regions **6406** may prevent the silicon nitride covered surfaces of silicon region **6408** from becoming oxidized during this process. This high temperature oxidation may repair some or all of the damages from the etch process of FIG. **64B**.

**[0693]** As illustrated in FIG. **64D** (Step D), an oxide fill material, such as, for example, PECVD silicon oxide, may be deposited, following which an anneal may be done to densify the deposited oxide. The anneal is generally performed at temperatures above 400° C. A chemical mechanical polish (CMP) may be conducted to planarize the surface. Silicon nitride regions **6406** may be removed either with a CMP process or with a selective etch, such as hot phosphoric acid. The oxide fill layer after the CMP process is indicated as STI oxide fill **6414**.

**[0694]** The prior art process described in FIG. **64A-D** may be prone to the drawback of high temperature (>400° C.) processing which may be not suitable for some embodiments of the invention herein that involve 3D stacking of components such as, for example, junction-less transistors (JLT) and recessed channel array transistors (RCAT). Processing and steps that involve temperatures greater than about 400° C. may include the thermal oxidation conducted to form oxide region **6412** and the densification anneal conducted in FIG. **64D** above.

**[0695]** FIG. **65A-D** describes an embodiment of the invention, wherein sub-400° C. process steps may be utilized to form the shallow trench isolation (STI) regions that enable high quality oxide isolation between transistors and circuit elements. A high quality isolation, typically formed with oxide, between active transistor junctions may have a leakage current of less than 1 picoamp per micron at Vcc and 25° C., Vcc being the nominal power supply voltage. The process flow for the integrated circuit or structure may include the following steps that may occur in sequence from Step (A) to Step (D). When the same reference numbers are used in different drawing figures (among FIG. **65A-D**), they are used to indicate analogous, similar or identical structures to enhance the understanding of the present invention by clarifying the relationships between the structures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures.

**[0696]** As illustrated in FIG. **65A** (Step A), a silicon wafer **6502** suitable for integrated circuit or structure formation may be constructed.

**[0697]** As illustrated in FIG. **65B** (Step B), a silicon nitride layer may be formed on top of silicon wafer **6502** using a process such as chemical vapor deposition (CVD) and may



then be lithographically patterned. Following this, an etch process removing the regions of silicon nitride and the silicon wafer **6502** may be conducted to form trench **6510** and silicon nitride regions **6506**. The silicon region **6508** may remain after these process steps. A silicon oxide (not shown) may be utilized as a stress relief layer between the silicon nitride regions **6506** and silicon wafer **6502**. Etch resistant materials, such as, for example, amorphous carbon, may be utilized in place of or in addition to the silicon nitride layer and subsequently formed silicon nitride regions **6506**.

**[0698]** As illustrated using FIG. **65C** (Step C), a plasma-assisted radical thermal oxidation process, which has a process temperature typically less than about 400° C., may be conducted to form the oxide region **6512**. The silicon nitride regions **6506** may prevent the silicon nitride covered surfaces of silicon region **6508** from becoming oxidized during this process. This high electron density plasma-assisted radical thermal oxidation process may repair some or all of the damages from the etch process of FIG. **65B**.

**[0699]** As illustrated in FIG. **65D** (Step D), an oxide fill material, such as, for example, a high-density plasma (HDP) process that produces dense oxide layers at low temperatures, less than about 400° C. Depositing a dense oxide avoids the requirement for a densification anneal that would need to be conducted at a temperature greater than about 400° C. A chemical mechanical polish (CMP) may be conducted to planarize the surface. Silicon nitride regions **6506** may be removed either with a CMP process or with a selective etch, such as hot phosphoric acid. The oxide fill layer after the CMP process is indicated as STI oxide fill **6514**.

**[0700]** The process described using FIG. **65A-D** can be conducted at less than 400° C., and this is advantageous for many 3D stacked architectures.

**[0701]** An additional embodiment of the invention is to utilize the underlying interconnection layer or layers to provide connections and connection paths for the overlying transistors. While the common practice in the IC industry is that interconnection layers are overlaying the transistors that they connect, the 3D IC technology may include the possibility of constructing connections underneath (below) the transistors as well. For example, some of the connections to, from, and in-between transistors in a layer of transistors may be provided by the interconnection layer or layers above the transistor layer; and some of the connections to, from, and in-between the transistors may be provided by the interconnection layer or layers below the transistor layer or layers. In general there is an advantage to have the interconnect closer to the transistors that they are connecting and using both sides of the transistors—both above and below—provides enhanced “closeness” to the transistors. In addition, there may be less interconnect routing congestion that would impede the efficient or possible connection of a transistor to transistors in other layers and to other transistors in the same layer.

**[0702]** The connection layers may, for example, include power delivery, heat removal, macro-cell connectivity, and routing between macro-cells. As illustrated in FIG. **66A-D**, an exemplary illustration and description of connections below a layer of transistors and macro-cell formation and connection is shown. When the same reference numbers are used in different drawing figures (among FIGS. **66A-D**), they may indicate analogous, similar or identical structures to enhance the understanding of the embodiments of the invention being discussed by clarifying the relationships between the struc-

tures and embodiments presented in the various diagrams—particularly in relating analogous, similar or identical functionality to different physical structures. The term macro-cell may include one or more logic cells.

**[0703]** As illustrated in FIG. **66A**, a repeating device or circuit structure, such as, for example, a gate-array like transistor structure, may be constructed in a layer, such as for example, monocrystalline silicon, as described elsewhere herein and in U.S. Patent Application Publication No. 20110121366, whose contents are incorporated by reference. FIG. **66A** is an exemplary illustration of the top view of three of the repeating elements of the structure layer. The exemplary repeating elements of the structure may include a first element **6618**, a second element **6620**, and a third element **6622**, and each element may include two transistor pairs, for example, N transistor pair **6612** and P transistor pair **6614**. N transistor pair **6612** may include common diffusion **6692** and a portion of common gate **6616** and second common gate **6617**. P transistor pair **6614** may include common diffusion **6694** and a portion of common gate **6616** and second common gate **6617**. The structure of FIG. **66A** can represent a small section of a gate-array in which the structure keeps repeating.

**[0704]** As illustrated in FIG. **66B**, the interconnection layers underneath (below) the transistors of FIG. **66A** may be constructed to provide connections (along with the vias of FIG. **66C**) between the transistors of FIG. **66A**. Underneath (below) the transistors may be defined as being in the direction of the TLVs (thru Layer Vias) or TSVs (Thru Silicon Vias) that are going through the layer of transistor structures and transistors referred to in the FIG. **66A** discussion. The view of exemplary illustration FIG. **66B** is from below the interconnection layers which are below the repeating device or circuit structure; however, the orientation of the repeating device or circuit structure is kept the same as FIG. **66A** for clarity. The interconnection layers underneath may include a ground-‘Vss’ power grid **6624** and a power-‘Vdd’ power grid **6626**. The interconnection layers underneath may include macro-cell construction connections such as NOR gate macro-cell connection **6628** for a NOR gate cell formation formed by the four transistors of first element **6618**, NAND gate macro-cell connection **6630** for a NAND gate cell formation formed by the four transistors of second element **6620**, and Inverter macro-gate cell connection **6632** for an Inverter gate cell formation formed by two of the four transistors of third element **6622**. The interconnection layers may include routing connection **6640** which connects the output of the NOR gate of first element **6618** to the input of the NAND gate of second element **6620**, and additional routing connection **6642** which connects the output of the NAND gate of second element **6620** to the input of the inverter gate of third element **6622**. These macro-cells and the routing connections (or routing structures) are part of the logic cell and logic circuit construction. The connection material may include for example, copper, aluminum, and/or conductive carbon.

**[0705]** As illustrated in FIG. **66C**, generic connections **6650** may be formed to electrically connect the transistors of FIG. **66A** to the underlying connection layer or layers presented in FIG. **66B**. Generic connections **6650** may also be called contacts as they represent the contact made between the interconnection layers and the transistors themselves, and may also be called TLVs (Thru Layer Vias), as described elsewhere herein. The diameter of the connections, such as, for example, generic connections **6650**, may be less than 1  $\mu\text{m}$  and/or less than 100 nm, and the alignment of the connections

to the underlying interconnection layer or layers or to the transistors may be less than 40 nm or even less than 10 nm using conventional industry lithography tools.

**[0706]** The process flow may involve first processing the connection layers such as presented in FIG. 66B and then overlying these connection layers by a transistor layer such as presented in FIG. 66A. These monolithic 3D transistors in the transistor layer could be made by any of the techniques presented herein or other techniques. After that the connections between the transistors and the underlying connection layers may be processed. For example, as illustrated in FIG. 66C generic connections 6650 may be specifically employed as power grid connections, such as Vss connection 6652 and second Vss connection 6651, and Vdd connection 6653. Further, generic connections 6650 may be specifically employed as macro-cell connections, such as macro-cell connection 6654 and second macro-cell connection 6655. Moreover, generic connections 6650 may be specifically employed as connections to routing, such as, for example, routing connection 6660 and second routing connection 6662. FIG. 66C also includes an illustration of the logic schematic 6670 represented by the physical illustrations of FIG. 66A, FIG. 66B and FIG. 66C.

**[0707]** As illustrated in FIG. 66D, and with reference to the discussion of FIGS. 47A and 47B herein, thru silicon connection 6689, which may be the generic connections 6650 previously discussed, may provide connection from the transistor layer 6684 to the underlying interconnection layer 6682. Underlying interconnection layer 6682 may include one or more layers of '1x' thickness metals, isolations and spacing as described with respect to FIGS. 47A&B. Alternatively, thru silicon connection 6688, which may be the generic connections 6650 previously discussed, may provide connection from the transistor layer 6684 to the underlying interconnection layer 6682 by connecting to the above interconnection layer 6686 which connects to the transistor layer 6684. Further connection to the substrate transistor layer 6672 may utilize making a connection from underlying interconnection layer 6682 to 2x interconnection layer 6680, which may be connected to 4x interconnection layer 6678, which may be connected to substrate 2x interconnection layer 6676, which may be connected to substrate 1x interconnection layer 6674, which may connect to substrate transistor layer 6672. Underlying interconnection layer 6682, above interconnection layer 6686, 2x interconnection layer 6680, 4x interconnection layer 6678, substrate 2x interconnection layer 6676, and substrate 1x interconnection layer 6674 may include one or more interconnect layers, each of which may include metal interconnect lines, vias, and isolation materials. As described in detail in the FIGS. 47A&B discussion, 1x layers may be thinner than 2x layers, and 2x layers may be thinner than 4x layers.

**[0708]** The design flow of a 3D IC that incorporates the "below-transistor" connections, such as are described for example, with respect to FIGS. 66A-D, would need to be modified accordingly. The chip power grid may need to be designed to include the below-transistors grid and connection of this grid to the overall chip power grid structure. The macro-cell library may need to be designed to include below-transistor connections. The Place and Route tool may need to be modified to make use of the below-transistor routing resources. These might include the power grid aspect, the macro-cell aspect, the allocation of routing resources underneath (below), and the number of layers underneath that are

allocated for the routing task. Typically, at least two interconnection layers underneath may be allocated.

**[0709]** For the case of connecting below-transistor routing layers to the conventional above-transistor routing layers, each connection may pass through a generic connections 6650 to cross the transistor-forming layers. Such contacts may already exist for many nets that directly connect to transistor sources, drains, and gates; and hence, such nets can be relatively freely routed using both below- and above-transistors interconnection routing layers. Other nets that may not normally include generic connections 6650 in their structure may be routed on either side of the transistor layer but not both, as crossing the transistor layer will incur creating additional generic connections 6650; and hence, potentially congest the transistor layer.

**[0710]** Consequently, a good approach for routing in such a situation may be to use the below-transistor layers for short-distance wiring and for wiring library macros that tend to be short-distance by their nature. Macro outputs, on the other hand, frequently need to connect also to remote locations and hence should be available at contacts, such as generic connections 6650, to be used on both sides of the transistor layer. When routing, nets that are targeted for both below and above the transistor layer and that do not include contacts such as generic connections 6650 may need special prioritized handling that will split them into two or more parts and insert additional contact[s] in the transistor layer before proceeding to route the design. An additional advantage of the availability and use of an increased number of routing layers on both sides of the transistor layer is the router's greater ability to use relaxed routing rules while not increasing routing congestion. For example, relaxing routing rules such as wider traces, wherein 1.5x or more the width of those traces used for the same layer in one sided routing for the same process node could be utilized in the two sided routing (above and below transistor layer), any may result in reduced resistance; and larger metal spacing, wherein 1.5x or more the space of those spaces used for the same layer in one sided routing for the same process node, could be utilized in the two sided routing (above and below transistor layer), and may result in decreased crosstalk and capacitance.

**[0711]** Persons of ordinary skill in the art will appreciate that the illustrations in FIGS. 66A through 66C are exemplary only and are not drawn to scale. Such skilled persons will further appreciate that many variations are possible such as, for example, the interconnection layer or layer below or above the transistor layer may also be utilized for connection to other strata and transistor layers, not just the transistor layer that is between the above and below interconnection layer or layers. Furthermore, connections made directly underneath and to common diffusions, such as common diffusion 6692 and second common diffusion 6694 (and described, for example, in relation to FIG. 20P herein), may be problematic in some process flows and TLVs through the adjacent STI (shallow trench isolation) area with routing thru the first layer of interconnect above the transistor layer to the TLV may instead be utilized. Moreover, silicon connection 6689 may be more than just a diffusion connection such as Vss connection 6652, second Vss connection 6651, and Vdd connection 6653, such as, for example, macro-cell connection 6654, second macro-cell connection 6655, routing connection 6660, or second routing connection 6662. Furthermore, substrate transistor layer 6672 may also be a transistor layer above a lower transistor layer in a 3DIC stack. Many other

modifications within the scope of the invention will suggest themselves to such skilled persons after reading this specification. Thus the invention is to be limited only by the appended claims.

[0712] It will also be appreciated by persons of ordinary skill in the art that the invention is not limited to what has been particularly shown and described hereinabove. For example, drawings or illustrations may not show n or p wells for clarity in illustration. Further, combinations and sub-combinations of the various features described hereinabove may be utilized to form a 3D IC based system. Rather, the scope of the invention includes both combinations and sub-combinations of the various features described hereinabove as well as modifications and variations which would occur to such skilled persons upon reading the foregoing description. Thus the invention is to be limited only by the appended claims.

1. A method to process an Integrated Circuit device comprising:

processing a first layer of first transistors, then  
 processing a first metal layer overlaying said first transistors and providing at least one connection to said first transistors, then  
 processing a second metal layer overlaying said first metal layer, then  
 processing a second layer of second transistors overlaying said second metal layer, wherein  
 said second metal layer is connected to provide power to at least one of said second transistors.

2. A method according to claim 1, comprising said second transistors forming logic cells, wherein  
 at least one of said logic cells comprises a connection made by said second metal layer.

3. A method according to claim 1, wherein  
 said second metal layer comprises a plurality of routing structures connecting between a plurality of said second transistors.

4. A method according to claim 1, comprising forming a connection path between said second transistors and said second metal layer, wherein

said connection path comprises at least one through-layer via, and wherein said through-layer via comprises material whose co-efficient of thermal expansion is within 50 percent of a coefficient of thermal expansion of said second layer.

5. A method according to claim 1, comprising a process forming high quality oxide isolation between said second transistors using radical oxidation or a high density plasma deposition.

6. A method according to claim 1, wherein said first layer comprises a first alignment mark, and comprises forming at least one via through said second layer, wherein said forming at least one via comprises alignment at least partially to said first alignment mark.

7. A method according to claim 1, comprises forming at least one via through said second layer, wherein said at least one via is adapted to conduct heat.

8. A method to process an Integrated Circuit device comprising:

processing a first layer of first transistors, then  
 processing a first metal layer overlaying said first transistors and providing at least one connection to said first transistors, then  
 processing a second metal layer overlaying said first metal layer, then

processing a second layer of second transistors overlaying said second metal layer, then processing a third metal layer overlying said second transistors, wherein at least one of said second transistors is provided with a back-bias.

9. A method according to claim 8, wherein  
 said second metal layer is connected to provide power to at least one of said second transistors.

10-11. (canceled)

12. A method according to claim 8, comprising forming a connection path between said second transistors and said second metal layer, wherein

said connection path comprises at least one through-layer via, and wherein said through-layer via comprises material whose co-efficient of thermal expansion is within 50 percent of a coefficient of thermal expansion of said second layer.

13. A method according to claim 8, comprising a process forming high quality oxide isolation between said second transistors using radical oxidation or a high density plasma deposition.

14. A method according to claim 8, wherein said first layer comprises a first alignment mark, and comprises forming at least one via through said second layer, wherein said forming at least one via comprises alignment at least partially to said first alignment mark.

15-22. (canceled)

23. A method to process an Integrated Circuit device comprising:

processing a first layer of first transistors, then  
 processing a first metal layer overlaying said first transistors and providing at least one connection to said first transistors, then

processing a second metal layer overlaying said first metal layer, then

processing a second layer of second transistors overlaying said second metal layer, comprising

forming at least one connection path between said second transistors and said second metal layer, wherein

said connection path comprises at least one through-layer via, and wherein said through-layer via comprises material whose co-efficient of thermal expansion is within 50 percent of a coefficient of thermal expansion of said second layer.

24. A method according to claim 23, wherein  
 said second metal layer comprises a power grid to provide power to at least one of said second transistors.

25-26. (canceled)

27. A method according to claim 23, comprising a process forming high quality oxide isolation between said second transistors using radical oxidation or a high density plasma deposition.

28. A method according to claim 23, wherein said first layer comprises a first alignment mark, and comprises forming at least one via through said second layer, wherein said forming at least one via comprises alignment at least partially to said first alignment mark.

29. A method according to claim 23, comprises forming at least one via through said second layer, wherein said at least one via comprises tungsten.

30. A method according to claim 23 wherein said second metal layer comprises mostly copper or aluminum.

**31.** A method according to claim **8**, comprising forming at least one via through said second layer, wherein said at least one via is adapted to conduct heat.

**32.** A method according to claim **8**, comprising forming at least one via through said second layer, wherein said at least one via is forming a direct contact with at least one of said second transistors.

**33.** A method according to claim **8**, wherein at least one of said second transistors is one of:

- (i) a replacement-gate transistor;
- (ii) a Finfet transistor; or
- (iii) a double gate horizontally oriented transistor.

**34.** A method to process an Integrated Circuit device comprising:

processing a first layer of first transistors, then  
processing a first metal layer overlaying said first transistors and providing at least one connection to said first transistors, then

processing a second metal layer overlaying said first metal layer, then processing a second layer of second transistors overlaying said second metal layer, then

processing a third metal layer overlying said second transistors,

wherein at least one of said second transistors is one of:

- (i) a replacement-gate transistor;
- (ii) a Finfet transistor; or
- (iii) a double gate horizontally oriented transistor.

**35.** A method according to claim **34**, comprising; back-bias for at least one of said second transistors.

**36.** A method according to claim **34**, wherein said second metal layer is connected to provide power to at least one of said second transistors.

**37.** A method according to claim **34**, comprising forming a connection path between said second transistors and said first transistors, wherein

said connection path comprises at least one through-layer via, and wherein said through-layer via comprises material whose co-efficient of thermal expansion is within 50 percent of a coefficient of thermal expansion of said second layer.

**38.** A method according to claim **34**, comprising a process forming high quality oxide isolation between said second transistors using radical oxidation or a high density plasma deposition.

**39.** A method according to claim **34**, wherein said first single crystal layer comprises a first alignment mark, and comprises forming at least one via through said second layer, wherein said forming at least one via comprises alignment at least partially to said first alignment mark.

**40.** A method according to claim **34**, comprising vias through said second layer wherein said vias are adapted to conduct heat.

**41.** A method according to claim **23**, wherein at least one of said second transistors is one of:

- (i) a replacement-gate transistor;
- (ii) a Finfet transistor; or
- (iii) a double gate horizontally oriented transistor.

**42.** A method according to claim **23**, comprising; back-bias for at least one of said second transistors.

\* \* \* \* \*