United States Patent

Horgan et al.

[15]   **3,657,706**

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[54]   **KEYBOARD DIGITAL DATA ENTRY SYSTEM**

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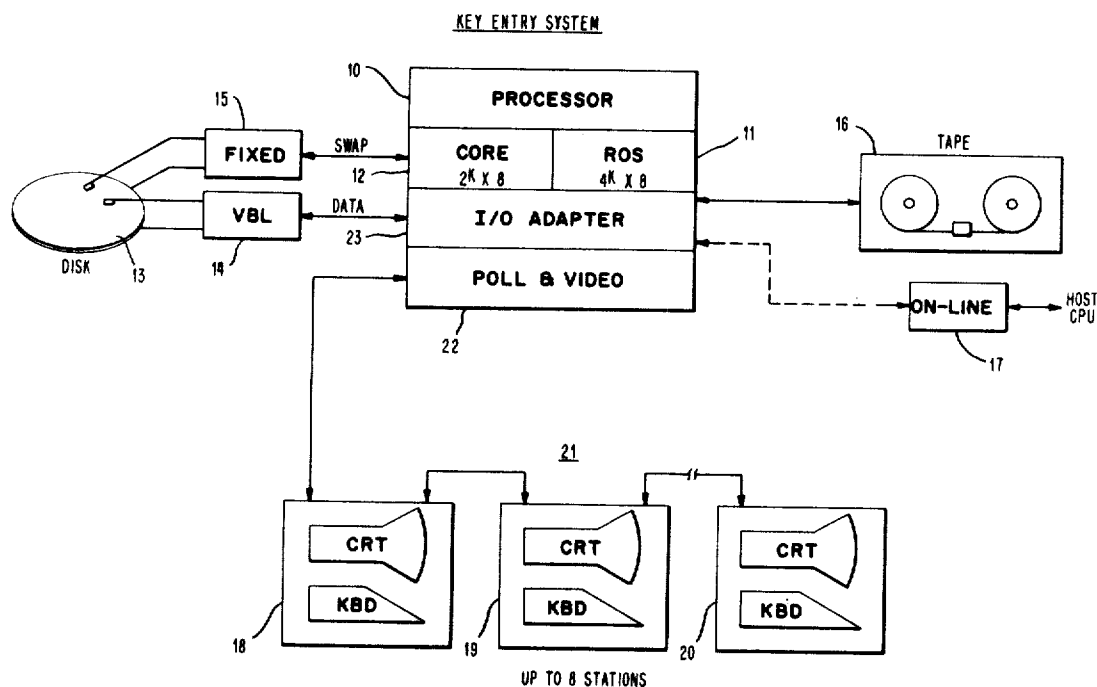
Primary Examiner—Gareth D. Shaw
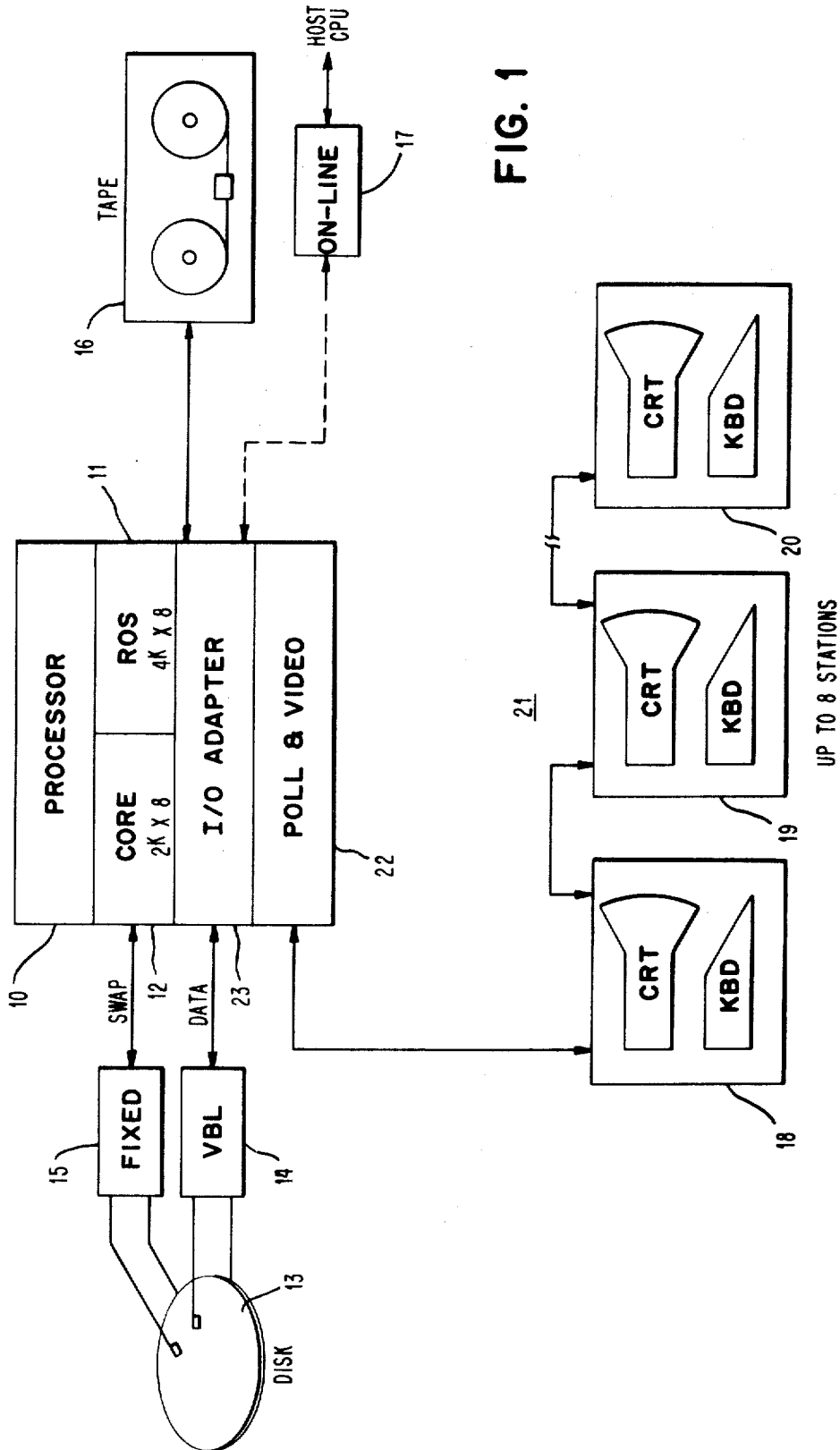*Attorney*—Woodcock, Washburn, Kurtz & Mackiewicz

[57]   **ABSTRACT**

In an input system for a digital computer, format control data is periodically swapped between the magnetic disc unit and memory so that all of the keystations are effectively provided with independent format control data while sharing keystroke processing routines. Each of the keystations is periodically polled to transfer keystroke data into the memory while display devices at each keystation are enable in synchronism with the keystroke polling so that data for each keystation can be transmitted over a single data transmission channel connecting the memory to all of the data display devices. A single-bit latch controls whether the next installation to be executed is fetched from a fixed memory or from a read-write memory.
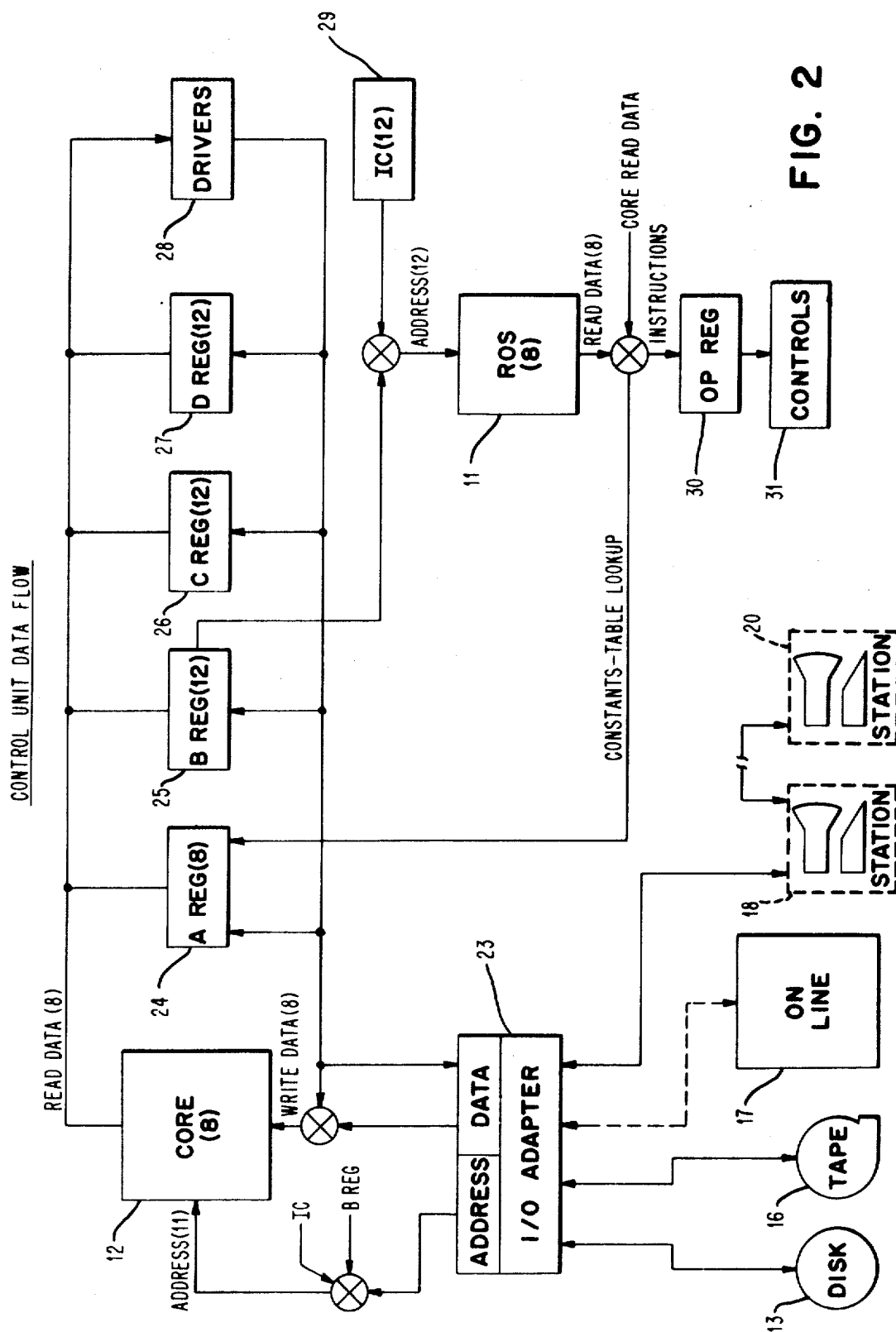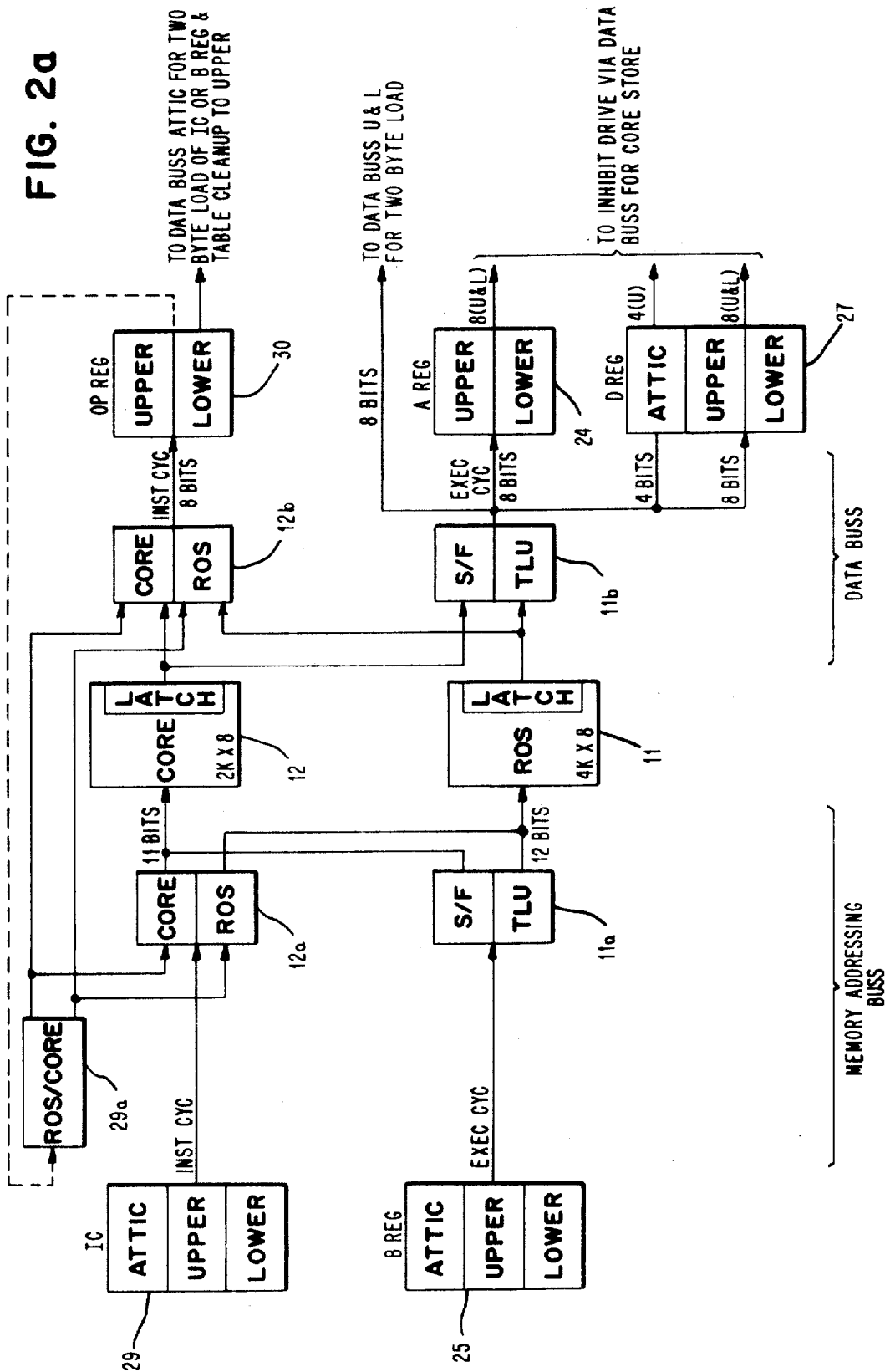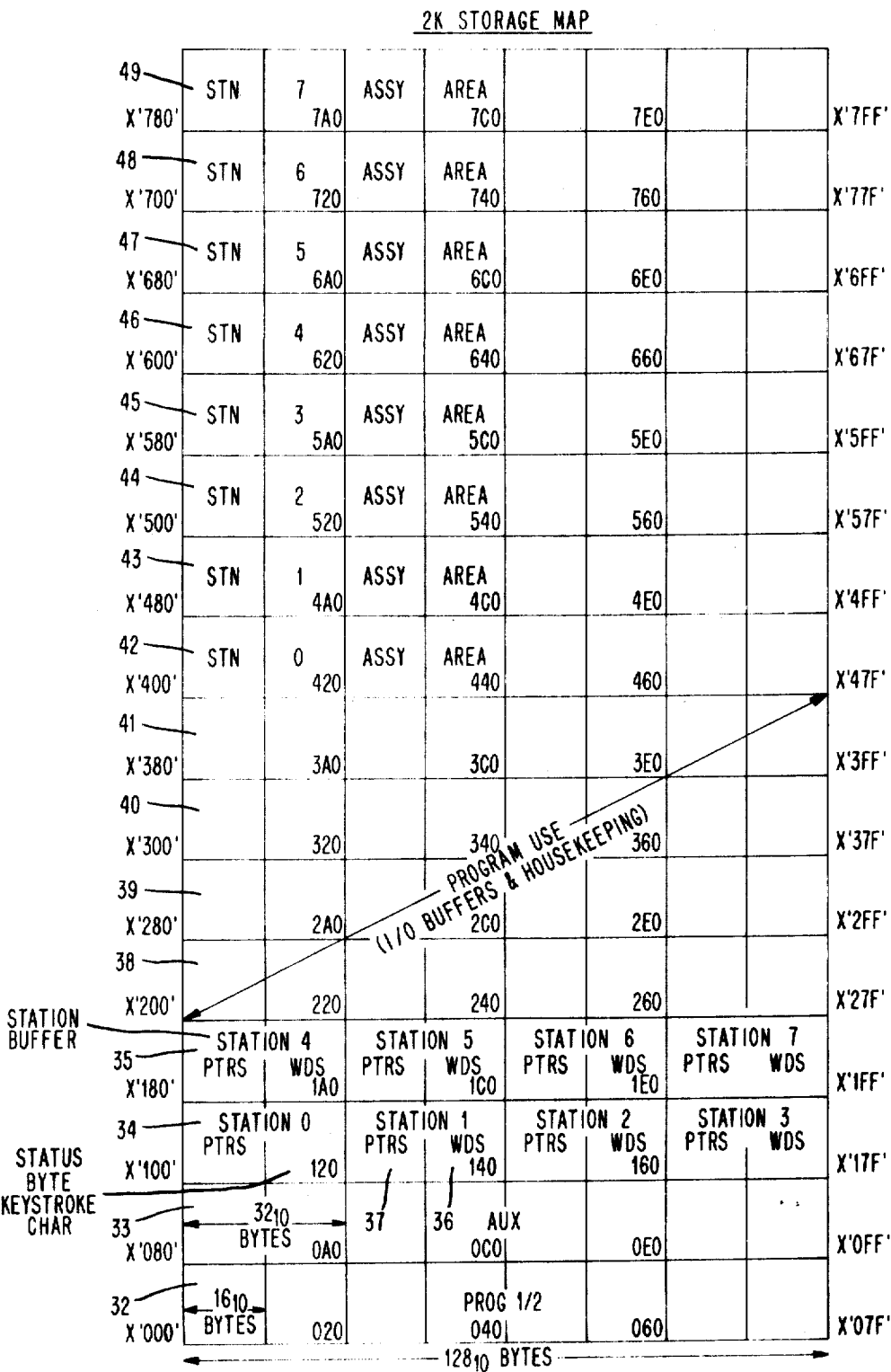
8 Claims, 6 Drawing Figures
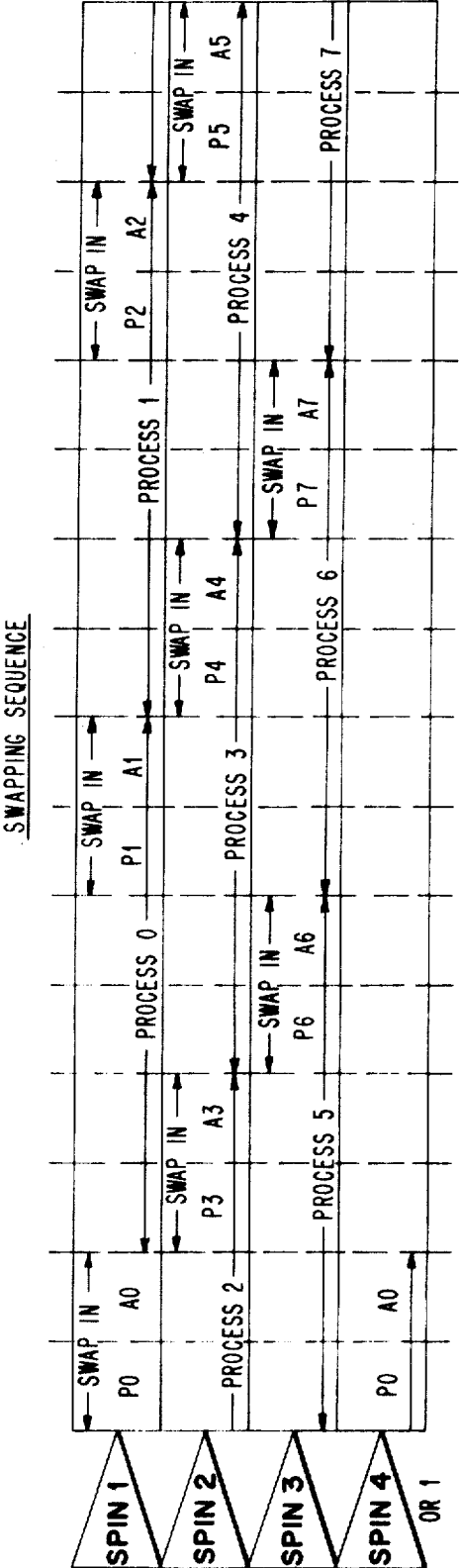
KEY ENTRY SYSTEM

UP TO 8 STATIONS

FIG. 1

CONTROL UNIT DATA FLOW

FIG. 2

FIG. 2a

FIG. 3

2K STORAGE MAP

49 — X'780'	STN	7 7A0	ASSY	AREA 7C0	7E0	X'7FF'
48 — X'700'	STN	6 720	ASSY	AREA 740	760	X'77F'
47 — X'680'	STN	5 6A0	ASSY	AREA 6C0	6E0	X'6FF'
46 — X'600'	STN	4 620	ASSY	AREA 640	660	X'67F'
45 — X'580'	STN	3 5A0	ASSY	AREA 5C0	5E0	X'5FF'
44 — X'500'	STN	2 520	ASSY	AREA 540	560	X'57F'
43 — X'480'	STN	1 4A0	ASSY	AREA 4C0	4E0	X'4FF'
42 — X'400'	STN	0 420	ASSY	AREA 440	460	X'47F'
41 — X'380'		3A0		3C0	3E0	X'3FF'
40 — X'300'		320		340	360	X'37F'
39 — X'280'		2A0		2C0	2E0	X'2FF'
38 — X'200'		220		240	260	X'27F'

PROGRAM USE
(I/O BUFFERS & HOUSEKEEPING)

STATION BUFFER

35 — X'180'	STATION 4 PTRS WDS 1A0	STATION 5 PTRS WDS 1C0	STATION 6 PTRS WDS 1E0	STATION 7 PTRS WDS	X'1FF'
34 — X'100'	STATION 0 PTRS 120	STATION 1 PTRS WDS 140	STATION 2 PTRS WDS 160	STATION 3 PTRS WDS	X'17F'

STATUS BYTE
KEYSTROKE CHAR

33 — X'080'	32₁₀ BYTES 0A0	37 36 AUX 0C0	0E0	X'0FF'
32 — X'000'	16₁₀ BYTES 020	PROG 1/2 040	060	X'07F'

←———————— 128₁₀ BYTES ————————→

FIG. 4

FIXED HEAD MAP

SECTOR	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
UPPER	PROG 0	AUX 0	PROG 3	AUX 3	PROG 6	AUX 6	PROG 1	AUX 1	PROG 4	AUX 4	PROG 7	AUX 7	PROG 2	AUX 2	PROG 5	AUX 5
LOWER	TEMP 2		TEMP 5		TEMP 0		TEMP 3		TEMP 6		TEMP 1		TEMP 4		TEMP 7	

FIG. 5

SWAPPING SEQUENCE

SPIN 1	SWAP IN P0 A0			SWAP IN P3 A3			SWAP IN P1 A1			SWAP IN P4 A4			SWAP IN P2 A2			SWAP IN P5 A5
SPIN 2	PROCESS 2			PROCESS 5			PROCESS 3			PROCESS 6			PROCESS 4			PROCESS 7
SPIN 3	PROCESS 0			SWAP IN P6 A6			PROCESS 1			SWAP IN P7 A7						
SPIN 4 OR 1	P0 A0															

KEYBOARD DIGITAL DATA ENTRY SYSTEM

BACKGROUND OF THE INVENTION

This invention relates to keyboard data input systems for digital computers and more particularly to an input system in which a central processor unit is shared by a number of keystations.

Originally, data input to a digital computer was performed on a keypunch. An operator at a keyboard is assisted by mechanical entry functions for duplicating and skipping. The operator produces a punched card which then must be inserted into a card reader for input to a computer. These machines operate independently of each other, each with its own data entry function capability. Keypunches are relatively slow and noisy. Extensive equipment is needed to read the cards, pool the data and transfer it to the computer in usable form.

Key-to-tape systems are an improvement over the keypunch in many applications. They are faster and quieter because of extensive use of electronic rather than mechanical components. Some key-to-tape systems have a memory and a control unit which provide data entry functions, such as skipping and automatic balancing. However, these systems are similar to keypunches in that each unit has its own independent source of data entry functions. Additional peripheral equipment is often required to pool data into a form usable by the computer.

Recently developed key-disc data entry systems have been assembled from available hardware. Software or programs have been written to utilize features of the hardware. Systems of this type are available from the Computer Machinery Corporation, Haddonfield, New Jersey, and from the Logic Corporation, Los Angeles, California. Because of the high cost of purchased hardware components and subsystems, presently available key-disc systems are competitive in cost with key-to-tape terminals only in installations requiring a large number of keystations, for example, 32 or more. When a large number of keystations are tied into one control unit in this manner, maintenance problems with the control unit results in downtime for many keystations.

The system of the present invention is an alternative to those systems described above.

SUMMARY OF THE INVENTION

In accordance with an important aspect of this invention, significant cost and performance advantages are achieved in an input system including a plurality of keystations which share a control unit having a fixed memory containing resident keystroke processing routines and a read-write memory for keystroke assembly and format control. Format control data is swapped between a magnetic disc unit and the read-write memory so that all of the keystations are effectively provided with independent format control data while sharing the keystroke processing routines.

In accordance with another important aspect of the present invention, the read-write memory has a station buffer and an assembly area for each keystation. Each of the keystations is periodically polled to transfer the keystroke data into the associated station buffer. The keystroke data is periodically transferred from the station buffer to the assembly area under control of the format control data currently in the read-write memory.

In accordance with another important aspect of the present invention, each of the keystations has a data display device. A single data transmission channel connects the read-write memory to all of the data display devices. The keystroke data in each of the assembly areas is sequentially and periodically read onto the data channel in synchronism with keystroke polling, but the keystroke data is displayed only on the proper display device because these display devices are enabled in synchronism with the keystroke polling.

In accordance with another important aspect of the present invention, non-resident keystroke processing routines are

stored in a portion of the disc unit and are selectively read into the read-write memory. The instruction counter has an associated latch which controls whether the next instruction to be executed is fetched from the fixed memory or the read-write memory.

In accordance with another important aspect of the present invention, the words stored in the fixed and read-write memories are only eight bits long, which is all that is required for handling eight-bit magnetic tape. However, the instruction counter and certain registers have a capacity for 12-bit words in order to address all storage locations in the memory. In order to accommodate 12-bit words in the fixed memory, a two-byte word assembly technique is used.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the system;

FIG. 2 shows a more detailed block diagram;

Fig. 2a shows the data flow between the registers;

Fig. 3 is a storage map of the read-write memory;

Fig. 4 is a map of the storage on the disc; and

Fig. 5 is a timing diagram showing the swapping sequence.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 1, the control unit includes a processor 10 having a read only, or fixed, memory 11 and a read-write magnetic core memory 12. In the particular example being described, the fixed memory 11 has 4,096 eight-bit storage locations and the read-write memory 12 has 2,048 eight bit storage locations. The fixed memory 11 contains fixed, or resident, subroutines such as left zero, check digit, and so on. Read-write memory 12 is used for keystroke assembly, job control format programs and programming scratch pad. It will be appreciated that the use of the read only, fixed, memory 11 represents a significant reduction in cost. By way of example, the fixed memory 11 having 4,096 storage locations is approximately the same cost as the read-write memory 12 having 2,048 storage locations.

A magnetic disc unit 13 provides storage for record pooling and for non-resident, i.e., less frequently used, routines. These are accessed by the movable heads 14.

The disc also has two tracks which are accessed by the fixed head 15. As will be more fully explained subsequently, these tracks contain the format control data which is swapped back and forth between the disc unit and the read-write memory 12. By continuously swapping this format control data, each of the keystations is effectively provided with its own independent format control data while sharing the keystroke processing routines stored in the fixed memory 11.

The control unit also includes a magnetic tape drive unit 16 which is the output medium for any job ready for input to the digital computer.

In certain situations, it will be desirable to operate the input system of this invention on-line with the computer. This can be done with a system of this type because the output of the system is pooled, verified data which can be operated upon on-line by the digital computer. This on-line operating capability has been indicated at 17.

In the particular embodiment of the invention being described, up to eight keystations may be provided, the keystations 18, 19 and 20 being shown. Each keystation includes a keyboard and a visual display device, in this case a cathode ray tube. A single data transmission channel 21 connects the processor to all of the keystations. That is, the stations are down-line dropped, or "daisy chained" along the cable length. This is contrasted, for example, to a star connection wherein a separate cable connects the processor to each of the keystations. The cathode ray tube at each unit displays text organized 32 characters per line in four lines, a total of 128 characters. A moving cursor on the CRT indicates the operating position on the displayed text to the operator.

The central processor 10 includes the section 22 for periodically polling each of the keystations to store keystrokes.

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Input-output adapter 23 decodes the address portion of each word and transmits the data portion of each word to the correct address.

Each keystation is poled 60 times a second and the keystrokes are transferred to an associated station buffer of the read-write memory 12. At the same time that a keystation is poled for keystrokes, the brightness control on the CRT is turned-up, that is, the visual display unit is enabled. Since the display unit is enabled in synchronism with the polling rate, it will display only that data present on the cable 21 during the time period that the keystation is being poled. The data being worked on by a particular keystation, and stored in an assembly area in the read-write memory 12, is sequentially read onto the data channel 21 in synchronism with the keystroke polling. Therefore, only the data being inputted at a particular keystation will be displayed on the CRT of that keystation.

CONTROL UNIT DATA FLOW

The data flow in the control unit is shown in simplified form in FIG. 2.

The control unit further includes the A, B, C and D registers 24 – 27 which are in communication with each other as well as with the fixed memory 11 and the read-write memory 12. Each register has a primary function which is summarized below:

A Reg. 24 - eight bits, serves as data buffer for read-write memory 12. It is also the data buffer for constants fetched from fixed memory 11. The programmer can test and set individual bits of this register.

5 B Reg. 25 - 12 bits, serves as address buffer for read-write memory 12, as well as fetch address for fixed memory 11. The programmer can increment this register (1-up), or load it with a fixed word.

C Reg. 26 - 12 bits, general purpose.

10 D Reg. 27 - 12 bits, serves as address LINK REGISTER ON BRANCH INSTRUCTION. During execution of a branch, the old Instruction Counter (IC) address is automatically entered here.

Drivers 28 are provided for these registers as is the usual practice. The control unit also includes the usual instruction counter 29, operations register 30 and controls 31. The read-write memory 12 may be addressed by the B Reg. 25, the instruction counter 29, or the input-output adapter 23. The fixed memory 11 may be addressed by the B Reg. 25 or the instruction counter 29. These operations are summarized as follows:

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Since eight-bit instructions are used, there are 2^8, or 256, possible instructions. It is necessary to use two of these instructions to set the latch but there are still 254 instructions remaining to operate the system. This very minor disadvantage is more than compensated for by the significant savings in instruction storage space. In the absence of the latch 29a, a nine-bit word would be required to provide the capability for fetching instructions from either the fixed memory 11 or the read-write memory 12. These nine-bit words require a significant increase in the amount of storage space over that required by the eight-bit words used in the present system.

During the execute cycle, the gates 11a and 11b control whether a store or fetch operation is performed in the read-write memory 12 or, alternatively, a table look-up operation is performed in the fixed memory 11. The condition of the gates 11a and 11b is controlled by the last bit in the OP register 30. In a store or fetch operation, the B register 25 addresses the read-write memory 12 via the gate 11a. The fetched data from the read-write memory 12 is applied via the gate 11b to the A register 24. In a table look-up operation, the B register addresses the fixed memory 11 via the gate 11a. The result of the table look-up is applied via the gate 11b to the A register. Simple arithmetic operations are performed in these table look-up operations. For example, instead of actually adding two numbers, the sum of the two numbers is stored in the table and is addressed by the two addends.

Another important capability of the system of the present invention is the provision for the use of two-byte instructions. Note that the words in the fixed memory 11 are only eight bits. This is all that is required for handling eight-bit tape. However, instruction counter 29, B register 25, C register 26, and D register 27 must all be supplied with 12-bit words. These 12-bit words are required to address all of the storage locations in the fixed memory 11 and the read-write memory 12. (Actually, the fixed memory 11 is addressed with a 12-bit word and the read-write memory 12 is addressed with an 11-bit word.)

The first four bits of certain instructions identify them as being part of a two-byte word. For example, when the word 1101 XXXX is in the OP register 30, the first four bits 1101 are decoded as identifying a two-byte word for the instruction counter. The last four bits of this word and the eight bits of the word at the next addressed storage location are combined and the 12 bits are supplied to the instruction counter. A different combination of the first four bits may identify a two-byte word

	Normal		Alternate	Alternate
Read-write memory 12	General Storage	Non-resident Program Execute	I/O Cycle Steal.	
	Addressed by B	Addressed by IC	Addressed by I/O.	
	Data to/from A	Data to Op Reg	Data to/from I/O.	
Fixed memory 11	Fixed Program Execute	Table Lookup		
	Addressed by IC	Addressed by B		
	Data to Op Reg	Data to A		

The foregoing may be better understood with reference to FIG. 2a showing the gates 12a and 12b which control whether the instruction to be executed is fetched from the read-write memory 12, or from the fixed memory 11. The latch 29a controls the gates 12a and 12b. When the latch 29a is set to the normal condition, the contents of the instruction counter address the fixed memory 11 is transferred via the gate 12a. The addressed instruction in the fixed memory 11 is transferred via the gate 12b to the operations register (OP register) 30. When the latch 29a is set to the alternate condition, the contents of the instruction counter address the read-write memory 12 via gate 12a. The addressed instruction in the read-write memory 12 is transferred, via gate 12b to the OP REGISTER 30.

The condition of the latch 29a is set by an instruction as indicated by the dashed line from the OP register 30 to the latch 29a. That is, there is a separate instruction to switch the condition of the latch from the normal to the alternate mode, and another instruction to switch the latch from the alternate to the normal mode. A string of instructions will be executed with the latch 29a in the normal mode, followed by an instruction which switches the latch to the alternate mode. Then, a string of instructions are executed with the latch in the alternate mode.

for the B register, and other combinations of the first four bits identify two-byte words for the C and D registers.

ALLOCATION OF READ-WRITE MEMORY STORAGE LOCATIONS, FIG. 3

The allocations of the storage locations in the read-write memory 12 are shown in the storage map of Fig. 3. The map is 128 bytes wide (standard record length) and is 16 records high. The first two lines 32 and 33 contain the format control information for the job in process. There is a continuous swapping of format control data between the fixed head tracks of the magnetic disc 13 and the storage locations 32 and 33 in the read-write memory 12. This format control data is swapped between the fixed head of disc 13 and lines 32 and 33 every 15 milliseconds. The line 32 contains the program control records designated PROG1 and PROG2. The line 33 contains the auxiliary duplication and forms records which are designated AUX.

The lines 34 and 35 of the read-write memory 12 contain the station buffers for keystroke data from each keystation. They also contain a pointers section for each keystation.

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Specifically, keystroke data from keystation one is assembled in the station buffer 36. For each station, there is also assigned an area of storage used as a pointer. For example, for station one, the area of storage 36 is switched from bit position to bit position to indicate the location of the last keystroke in a record. Each keystation is similarly assigned 16 bytes for programming pointers and 16 bytes for a keystroke station buffer. The keystroke buffer stations are continuously entered by the input-output polling sequence. That is, words representing the coordinate of a keystroke are picked up by the polling sequence and entered into the associated station buffer.

Lines 38 – 41 are used for programming scratchpad. These lines are also used as temporary storage for non-resident programs which may be transferred from the disc into the read-write memory as required.

Lines 42 – 49 are assembly areas for the keystations. Keystroke coordinate data from station buffer 36 is transferred to assembly area 43 under control of the format control data in lines 32 and 33. Note that the data in the station buffer 36 represents only which key has been stroked. This is converted to a word representing alphabetic or numeric information, for example, by the format control data in lines 32 and 33.

Then, the format control data for use by keystation two is swapped into lines 32 and 33. Keystroke coordinate data from the station buffer for keystation two is transferred to assembly area 44 under control of that format data. There is a continuous swapping of format control data between the disc 13 and lines 32 and 33 of the read-write memory. During the time that the format control data for a particular station is present in lines 32 and 33, keystroke coordinate data from the station buffer is transferred to the assembly area for that keystation.

DISC 13, FIXED HEAD MAP FIG. 4 AND SWAPPING SEQUENCE FIG. 5

The disc 13 is a single fixed platter rotating at 1,500 rpm and is accessible over 200 cylinders by a pair of moving heads. In addition, a single extra cylinder is accessed by a pair of fixed heads. The disc is sectored into sixteen 128 byte records per track. The 200 random access cylinders are assigned as follows:

Job data (pooled records)	128 cylinders = 128×2×16 = 4,096 records or 524,288 bytes
Job control library	16 cylinders = 128 job formats (PROG,AUX)
Non-resident programs	56 cylinders

The fixed head tracks contain the format control data currently in use. As shown in FIG. 4, sector zero contains a program for station zero, sector 1 contains the auxiliary data for station zero, sector 2 contains the program for station 3, sector 3 contains the auxiliary data for station 3 and so on. Each station has an independent selection of format control data. As will be subsequently described, format control data may be called to the fixed head swapping tracks by name from the job control library or they may be entered from the keyboard.

The other, lower, track associated with the fixed heads is used for temporary storage when an error occurs. When an entry error has been indicated, the assembly area in the read-write memory is unloaded and a special error message to be displayed to the keystation operator is substituted. However, the information previously in the assembly area is retained by temporarily storing it in one of the areas indicated on the lower track associated with the fixed heads.

The swapping and processing sequence is shown in FIG. 5. During the first revolution of the disc, the program and auxiliary data for keystation zero are transferred to lines 32 and 33 of the read-write memory as the zero and 1 sector of the drum pass under the fixed head. As sectors 2 – 5 pass under the fixed head, keystroke data in the station buffer is transferred to the assembly area for keystation zero. That is, the keystroke data for keystation zero is processed.

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As the sectors 6 and 7 pass under the fixed head, program and AUX data for keystation one is swapped to the read-write memory. As the sectors 8 – 11 pass under the fixed head, the keystroke data for keystation one is processed. As sectors 12 and 13 pass under the fixed head, the format control data for keystation two is swapped to the read-write memory. The keystroke data for keystation two is processed as sectors 14 and 15 pass under the fixed head. This processing continues during the initial portion of the second revolution of the disc. The swapping and processing sequence continues as shown in Fig. 5 so that the keystroke data for all of the stations is processed during three complete revolutions of the disc.

KEYSTATION POOLING AND DISPLAY REFRESH

Referring back to Fig. 1, the eight keystations are each polled 60 times per second. The duration of the polling is $1/480^{th}$ of a second during which time any keystroke from the keystation is stored in lines 34 and 35 (Fig. 3) of the read-write memory 12. During this time, the cathode ray tube associated with that station is unblanked to display the video dot stream appearing on the cable 21.

While a particular embodiment of the invention has been shown and described, it will be understood that various modifications may be made without departing from the true spirit and scope of the invention. The appended claims are, therefore, intended to cover any such modifications.

What is claimed is:

1. In an input system for a digital computer, comprising:
a plurality of independent keystations each having a data entry keyboard,
a data transmission channel connecting said keystations to a central processor which includes:
a control unit having:
a fixed memory containing resident keystroke processing routines,
a read-write memory having a section for keystroke assembly and a section for format control, each of said keystations being connected to apply keystroke data to said section for keystroke assembly of said read-write memory, and
a magnetic disc unit, at least a portion of said disc unit being used for storing format control data, the improvement comprising:
an adapter connected between said magnetic disc unit and said read-write memory, said adapter being controlled to periodically swap said format control data between said portion of said magnetic disc unit and said section for format control of said read-write memory so that all of said keystations are effectively provided with independent format control while sharing the keystroke processing routines.

2. The system recited in claim 1 wherein said read-write memory has a station buffer for each keystation and an assembly area for each keystation,
means for periodically polling each of said keystations to transfer said keystroke data into the associated station buffer, and
means for periodically transferring said keystroke data from said station buffer to the assembly area under control of the format control data currently in said read-write memory.

3. The system recited in claim 2 wherein each of said keystations has a visual display device, and wherein said data transmission channel is a single channel connecting said read-write memory to all said data display devices,
means for sequentially and periodically reading the keystroke data in each of said assembly areas onto said data channel in synchronism with keystroke polling, and
means for enabling each of said display devices in synchronism with said keystroke polling.

4. The system recited in claim 1 wherein non-resident keystroke processing routines are stored in a portion of said disc

unit, said non-resident keystroke processing routines being selectively read into said read-write memory, and

an instruction counter connected to address said read-write memory and said fixed memory, and

a single-bit latch controlling whether the next instruction to be executed is fetched from said fixed memory or from said read-write memory.

5. In an input system for a digital computer, comprising:

a plurality of independent keystations each having a data entry keyboard,

a control unit at a central location,

a read-write memory in said control unit, said read-write memory having a plurality of keystroke data assembly areas,

a visual display device at each of said keystations,

a single data transmission channel connecting said read-write memory to all said data display devices, the improvement comprising:

means for sequentially and periodically reading the keystroke data in each of said assembly areas onto said data channel in synchronism with keystroke polling, and

means for enabling each of said display devices in synchronism with said keystroke polling.

6. In an input system for a digital computer, comprising:

a plurality of independent keystations each having a data entry keyboard,

a control unit at a central location having:

a fixed memory containing resident keystroke processing routines,

a read-write memory having a section for keystroke assembly and a section for format control, each of said keystations being connected to apply keystroke data to said section for keystroke assembly of said read-write memory, and

a magnetic disc unit, at least a portion of said disc unit being used for storing format control data, non-resident keystroke processing routines being stored in a portion of said disc unit, said non-resident keystroke processing routines being selectively read into said read-write memory, and

a data transmission channel connecting said keystations to said control unit, the improvement comprising:

an instruction counter in said control unit, said instruction counter being connected to address said read-write memory and said fixed memory,

a single-bit latch means controlling whether the next instruction to be executed is in said fixed memory or in said read-write memory, and gating means connected to the outputs of said fixed memory and said read-write memory, said gating means being controlled by said single-bit latch means.

7. The input system recited in claim 6 and an operations register connected to receive instructions from said gating means, said operations register being connected to control the execution of said instruction, said single-bit latch being set to a normal condition by one instruction in the operations register and being set to an alternate condition by another instruction in said operations register.

8. The system recited in claim 1 wherein said memories each include a plurality of storage locations each having n bit positions, where n is the number of bits in the data words in the output to said digital computer, the storage locations in said memories being addressable by words which are k bits in length, where k is greater than n, and

at least one register having k bit positions, said register being loaded with words from two storage locations to form a two-byte instruction.

* * * * *

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,657,706 ·   Dated April 18, 1972

Inventor(s) Thomas B. Horgan et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 3, line 29, delete "5" before "Reg.";
"   line 34, delete "10" before "Reg.";
"   line 47, underscore "General Storage", Non-resident
                   Program Execute", and"I/O Cycle Steal";
"   line 50, underscore "Fixed Program Execute","Table
                   Lookup";
"   line 59, omit "is transferred";
"   line 59, change"gage" to --gate--;

Column 7, line 2, delete "and";
"   line 35, delete "and";

        Signed and sealed this 22nd day of August 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.   ROBERT GOTTSCHALK
Attesting Officer   Commissioner of Patents