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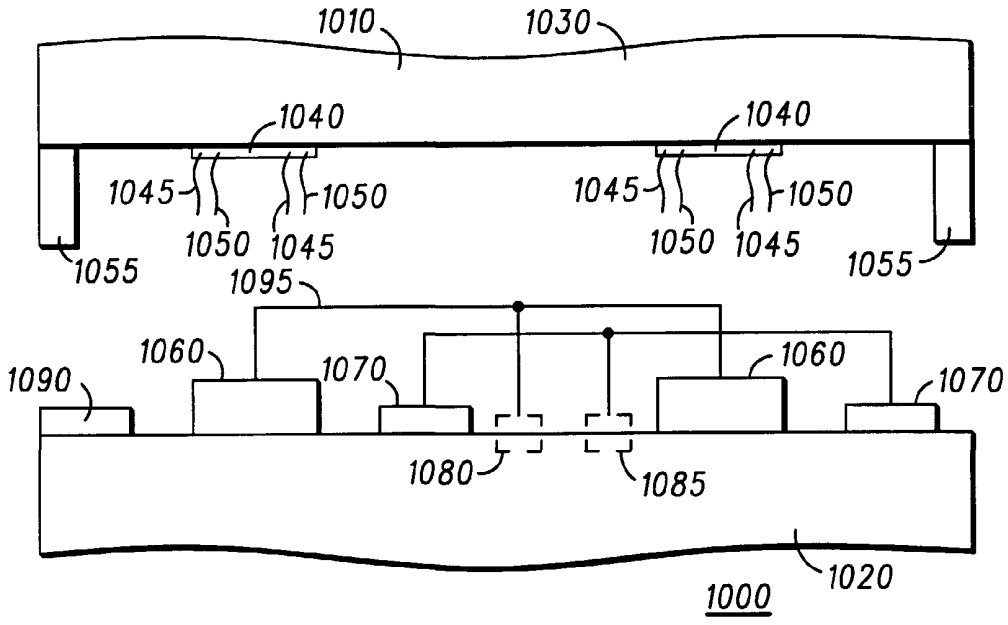

(57) Abstract: A biological material analysis system (1000) suitable for analyzing material (1045) on a biochip (1010) is disclosed. The system includes light emitting (1060) and detecting devices (1070) formed using high quality epitaxial layers of compound semiconductor materials (1112) overlying an accommodating buffer layer (1160) on a silicon wafer (1150). The accommodating buffer layer is a layer of monocrystalline material spaced apart from the silicon wafer by an amorphous interface layer. The amorphous interface layer dissipates strain and permits the growth of a high quality monocrystalline accommodating buffer layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous interface layer.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

BIOCHIP EXCITATION AND ANALYSIS STRUCTURE

Field of the Invention

This invention relates generally to semiconductor structures and devices and to a method for their fabrication, and more specifically to semiconductor structures for light emitting and light detecting applications that are suitable for facilitating analysis of materials on a biochip.

Background of the Invention

Biochips have recently been developed in an effort to expedite biological testing and reduce the cost of such testing. The term "biochip" generally refers to a substrate or chip that includes materials that facilitate compositional analysis of biological material. For example, a biochip may include a substrate formed of glass, plastic, or silicon with "pads" of material designed to attach to or react with biological material to be analyzed. The pads may be designed to attach to or react with particular DNA sequences, chemical agents, proteins, or the like. For example, the pads may include DNA oligonucleotide ("oiligo") material configured to react with a complimentary oligo, which may be present in the sample.

A compositional analysis of a biological sample may be obtained using a biochip by passing a sample of the biological material (which may have been "prepared" by, for example, exposing the sample to reagents and/or heat to form oligos) over the pads and analyzing the biochip to determine whether any of the sample attached to or reacted with the material on the pads: if materials reacted or attached to portions of the biochip (e.g., oligos present on one or more pads), the sample includes material know to react with the material on the pads.

To facilitate determination of whether the sample reacted with or attached to a particular pad, the sample is often "marked" with a fluorescent tag that is configured to react with and bond to particular chemical composition, such that a sample portions that attach to a pad are marked with the florescent material. In this case, the biochip can be

analyzed by determining which pads include fluorescent material. Often, a determination of whether biological material has attached to a pad is made by exposing the biochip to a light source and manually determining which pads contain fluorescent material. Alternatively, large scale scopes may be used to determine which pads on a biochip include material from the sample.

Now-known methods for analyzing material on a biochip are problematic in several regards. For example, manual methods are generally time consuming and expensive. Further, methods requiring large scale lab equipment are undesirable because the equipment used to analyze the sample is typically not portable and thus the biochip cannot generally be analyzed in remote locations. Accordingly, improved methods and apparatus for analyzing material on a biochip are desired.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGS. 1 – 3 and 12 - 13 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer;

FIG. 5 illustrates a high resolution Transmission Electron Micrograph of a structure including a monocrystalline accommodating buffer layer;

FIG. 6 illustrates an x-ray diffraction spectrum of a structure including a monocrystalline accommodating buffer layer;

FIG. 7 illustrates a high resolution Transmission Electron Micrograph of a structure including an amorphous oxide layer;

FIG. 8 illustrates an x-ray diffraction spectrum of a structure including an amorphous oxide layer;

FIG. 9 illustrate schematically, in cross section, a structure including devices formed within a compound semiconductor layer and a Group IV semiconductor layer in accordance with the present invention;

FIG. 10 illustrates schematically, in cross section, a biological material analysis system in accordance with the present invention;

FIGS. 11, 14, and 15 illustrate schematically, in cross section, structures for facilitating analysis of biological material in accordance with the present invention;

FIGS. 16 – 17 illustrate schematically, in cross section, detectors in accordance with various embodiments of the present invention; and

FIG. 18 illustrates schematically, in cross section, an emitter in accordance with the present invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

The present invention provides improved apparatus and methods for analyzing material on a biochip. In particular, the invention provides an apparatus for analyzing the material using microelectronic light emitting and light detecting devices formed on a substrate, wherein at least one of the devices is formed using compound semiconductor material. Using microelectronic devices to emit and detect light to analyze biochip material facilitates automatic, portable analysis of the material.

In accordance with preferred embodiments of the invention, a light detecting and/or a light emitting device is formed on or within a compound semiconductor layer formed over a Group IV semiconductor substrate such as a silicon wafer. Forming a light emitting and/or a light detecting device using compound semiconductor material over Group IV material provides a relatively inexpensive substrate to form the devices and allows for integration of the light emitting and/or detecting devices formed within

the compound semiconductor material with other devices that are formed within the Group IV substrate.

FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 which may be used to form light emitting and light detecting devices suitable for analyzing material on a biochip. Semiconductor structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of a monocrystalline compound semiconductor material. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

In accordance with one embodiment of the invention, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and compound semiconductor layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the compound semiconductor layer on the accommodating buffer layer. The amorphous intermediate layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table, and preferably a material from Group IVA. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used

in the semiconductor industry. Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer by the oxidation of substrate 22 during the growth of layer 24. The amorphous intermediate layer serves to relieve strain that might otherwise occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in monocrystalline compound semiconductor layer 26.

Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. For example, the material could be an oxide or nitride having a lattice structure substantially matched to the substrate and to the subsequently applied semiconductor material. Materials that are suitable for the accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for the accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxides or nitrides typically include at least two different metallic elements and have a

perovskite structure. In some specific applications, the metal oxides or nitrides may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

The compound semiconductor material of layer 26 can be selected, as needed for a particular semiconductor structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II(A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs), gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur selenide (ZnSSe), and the like. Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of the subsequent compound semiconductor layer 26. Appropriate materials for template 30 are discussed below.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the previously described semiconductor structure 20, except that an additional buffer layer 32 is positioned between accommodating buffer layer 24 and layer of monocrystalline compound semiconductor material 26. Specifically, the additional buffer layer is positioned between template layer 30 and the overlying layer of compound semiconductor material. The additional buffer layer, formed of a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of the accommodating buffer layer cannot be adequately matched to the overlying monocrystalline compound semiconductor material layer.

FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 20, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional semiconductor layer 38.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. Monocrystalline semiconductor layer 38 is then formed (by epitaxial growth) overlying the monocrystalline accommodating buffer layer. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between substrate 22 and semiconductor layer 38 (subsequent to layer 38 formation) relieves stresses between layers 22 and 38 and provides a true compliant substrate for subsequent processing--*e.g.*, compound semiconductor layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline compound semiconductor layers over a monocrystalline substrate. However, the process described in connection with FIG. 3, which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline compound semiconductor layers because it allows any strain in layer 26 to relax.

Semiconductor layer 38 may include any of the materials described throughout this application in connection with either of compound semiconductor material layer 26 or additional buffer layer 32. For example, layer 38 may include monocrystalline Group IV or monocrystalline compound semiconductor materials.

In accordance with one embodiment of the present invention, semiconductor layer 38 serves as an anneal cap during layer 36 formation and as a template for

subsequent semiconductor layer 26 formation. Accordingly, layer 38 is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 38 to form as a substantially defect free monocrystalline semiconductor compound.

In accordance with another embodiment of the invention, semiconductor layer 38 comprises compound semiconductor material (*e.g.*, a material discussed above in connection with compound semiconductor layer 26) that is thick enough to form devices (*e.g.*, light emitting and/or light detection devices) within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include compound semiconductor layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one compound semiconductor layer disposed above amorphous oxide layer 36.

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40, and 34 in accordance with various alternative embodiments of the invention. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1 and the amorphous intermediate layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. The accommodating buffer layer can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the compound semiconductor layer from the substrate to obtain the desired electrical and optical properties. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

In accordance with this embodiment of the invention, compound semiconductor material layer 26 is a layer of gallium arsenide (GaAs) or aluminum gallium arsenide (AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm. The thickness generally depends on the application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer is formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O. By way of a preferred example, 1-2 monolayers of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers.

Example 2

In accordance with a further embodiment of the invention, monocrystalline substrate 22 is a silicon substrate as described above. The accommodating buffer layer is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or orthorhombic phase with an amorphous intermediate layer of silicon oxide formed at the interface between the silicon substrate and the accommodating buffer layer. The accommodating buffer layer can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline $SrZrO_3$, $BaZrO_3$, $SrHfO_3$, $BaSnO_3$ or $BaHfO_3$. For example, a monocrystalline oxide layer of $BaZrO_3$ can grow at a temperature of about 700 degrees C. The lattice structure of the resulting crystalline oxide exhibits a 45 degree rotation with respect to the substrate silicon lattice structure.

An accommodating buffer layer formed of these zirconate or hafnate materials is suitable for the growth of compound semiconductor materials in the indium phosphide (InP) system. The compound semiconductor material can be, for example, indium phosphide (InP), indium gallium arsenide (InGaAs), aluminum indium arsenide, (AlInAs), or aluminum gallium indium arsenic phosphide (AlGaInAsP), having a thickness of about 1.0 nm to 10 μm. A suitable template for this structure is 1-10 monolayers of zirconium-arsenic (Zr-As), zirconium-phosphorus (Zr-P), hafnium-arsenic (Hf-As), hafnium-phosphorus (Hf-P), strontium-oxygen-arsenic (Sr-O-As), strontium-oxygen-phosphorus (Sr-O-P), barium-oxygen-arsenic (Ba-O-As), indium-strontium-oxygen (In-Sr-O), or barium-oxygen-phosphorus (Ba-O-P), and preferably 1-2 monolayers of one of these materials. By way of an example, for a barium zirconate accommodating buffer layer, the surface is terminated with 1-2 monolayers of zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template. A monocrystalline layer of the compound semiconductor material from the indium phosphide system is then grown on the template layer. The resulting lattice

structure of the compound semiconductor material exhibits a 45 degree rotation with respect to the accommodating buffer layer lattice structure and a lattice mismatch to (100) InP of less than 2.5%, and preferably less than about 1.0%.

Example 3

In accordance with a further embodiment of the invention, a structure is provided that is suitable for the growth of an epitaxial film of a II-VI material overlying a silicon substrate. The substrate is preferably a silicon wafer as described above. A suitable accommodating buffer layer material is $Sr_xBa_{1-x}TiO_3$, where x ranges from 0 to 1, having a thickness of about 2-100 nm and preferably a thickness of about 5-15 nm. The II-VI compound semiconductor material can be, for example, zinc selenide (ZnSe) or zinc sulfur selenide (ZnSSe). A suitable template for this material system includes 1-10 monolayers of zinc-oxygen (Zn-O) followed by 1-2 monolayers of an excess of zinc followed by the selenidation of zinc on the surface. Alternatively, a template can be, for example, 1-10 monolayers of strontium-sulfur (Sr-S) followed by the ZnSeS.

Example 4

This embodiment of the invention is an example of structure 40 illustrated in FIG. 2. Substrate 22, monocrystalline oxide layer 24, and monocrystalline compound semiconductor material layer 26 can be similar to those described in example 1. In addition, an additional buffer layer 32 serves to alleviate any strains that might result from a mismatch of the crystal lattice of the accommodating buffer layer and the lattice of the monocrystalline semiconductor material. Buffer layer 32 can be a layer of germanium or a GaAs, an aluminum gallium arsenide (AlGaAs), an indium gallium phosphide (InGaP), an aluminum gallium phosphide (AlGaP), an indium gallium arsenide (InGaAs), an aluminum indium phosphide (AlInP), a gallium arsenide phosphide (GaAsP), or an indium gallium phosphide (InGaP) strain compensated

superlattice. In accordance with one aspect of this embodiment, buffer layer 32 includes a $GaAs_xP_{1-x}$ superlattice, wherein the value of x ranges from 0 to 1. In accordance with another aspect, buffer layer 32 includes an $In_yGa_{1-y}P$ superlattice, wherein the value of y ranges from 0 to 1. By varying the value of x or y, as the case may be, the lattice constant is varied from bottom to top across the superlattice to create a match between lattice constants of the underlying oxide and the overlying compound semiconductor material. The compositions of other materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. The superlattice can have a thickness of about 50-500 nm and preferably has a thickness of about 100-200 nm. The template for this structure can be the same of that described in example 1. Alternatively, buffer layer 32 can be a layer of monocrystalline germanium having a thickness of 1-50 nm and preferably having a thickness of about 2-20 nm. In using a germanium buffer layer, a template layer of either germanium-strontium (Ge-Sr) or germanium-titanium (Ge-Ti) having a thickness of about one monolayer can be used as a nucleating site for the subsequent growth of the monocrystalline compound semiconductor material layer. The formation of the oxide layer is capped with either a monolayer of strontium or a monolayer of titanium to act as a nucleating site for the subsequent deposition of the monocrystalline germanium. The monolayer of strontium or titanium provides a nucleating site to which the first monolayer of germanium can bond.

Example 5

This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline compound semiconductor material layer 26 and template layer 30 can be the same as those described above in example 2. In addition, a buffer layer 32 is inserted between the accommodating buffer layer and the overlying monocrystalline compound semiconductor material layer. The buffer layer, a further monocrystalline semiconductor material, can be, for example, a graded layer of indium gallium arsenide (InGaAs) or indium aluminum arsenide (InAlAs). In accordance with one aspect of this embodiment, buffer layer 32 includes InGaAs, in which the indium composition varies from 0 to about 47%. The buffer layer preferably has a thickness of about 10-30 nm. Varying the composition of the buffer layer from GaAs to InGaAs serves to provide a lattice match between the underlying monocrystalline oxide material and the overlying layer of monocrystalline compound semiconductor material. Such a buffer layer is especially advantageous if there is a lattice mismatch between accommodating buffer layer 24 and monocrystalline compound semiconductor material layer 26.

Example 6

This example provides exemplary materials useful in structure 34, as illustrated in FIG. 3. Substrate material 22, template layer 30, and monocrystalline compound semiconductor material layer 26 may be the same as those described above in connection with example 1.

Amorphous layer 36 is an amorphous oxide layer which is suitably formed of a combination of amorphous intermediate layer materials (*e.g.*, layer 28 materials as described above) and accommodating buffer layer materials (*e.g.*, layer 24 materials as described above). For example, amorphous layer 36 may include a combination of SiO_x

and $Sr_zBa_{1-z}TiO_3$ (where z ranges from 0 to 1),which combine or mix, at least partially, during an anneal process to form amorphous oxide layer 36.

The thickness of amorphous layer 36 may vary from application to application and may depend on such factors as desired insulating properties of layer 36, type of semiconductor material comprising layer 26, and the like. In accordance with one exemplary aspect of the present embodiment, layer 36 thickness is about 2 nm to about 100 nm, preferably about 2-10 nm, and more preferably about 5-6 nm.

Layer 38 comprises a monocrystalline compound semiconductor material that can be grown epitaxially over a monocrystalline oxide material such as material used to form accommodating buffer layer 24. In accordance with one embodiment of the invention, layer 38 includes the same materials as those comprising layer 26. For example, if layer 26 includes GaAs, layer 38 also includes GaAs. However, in accordance with other embodiments of the present invention, layer 38 may include materials different from those used to form layer 26. In accordance with one exemplary embodiment of the invention, layer 38 is about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1 - 3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In a similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of a grown crystal layer of high crystalline quality as a function of the mismatch between the

lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that have a large number of defects. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of the invention, a high quality, thick, monocrystalline titanate layer is achievable.

Still referring to FIGS. 1 - 3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected

materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. If the grown crystal is gallium arsenide, aluminum gallium arsenide, zinc selenide, or zinc sulfur selenide and the accommodating buffer layer is monocrystalline $Sr_xBa_{1-x}TiO_3$, substantial matching of crystal lattice constants of the two materials is achieved, wherein the crystal orientation of the grown layer is rotated by 45° with respect to the orientation of the host monocrystalline oxide. Similarly, if the host material is a strontium or barium zirconate or a strontium or barium hafnate or barium tin oxide and the compound semiconductor layer is indium phosphide or gallium indium arsenide or aluminum indium arsenide, substantial matching of crystal lattice constants can be achieved by rotating the orientation of the grown crystal layer by 45° with respect to the host oxide crystal. In some instances, a crystalline semiconductor buffer layer between the host oxide and the grown compound semiconductor layer can be used to reduce strain in the grown monocrystalline compound semiconductor layer that might result from small differences in lattice constants. Better crystalline quality in the grown monocrystalline compound semiconductor layer can thereby be achieved.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a semiconductor structure such as the structures depicted in FIGS. 1 - 3. The process starts by providing a monocrystalline semiconductor substrate comprising silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 0.5° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a

grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other alkali earth metals or combinations of alkali earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a temperature of about 750° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of a monocrystalline oxide layer by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown

on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stochiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer that is conducive to the subsequent growth of an epitaxial layer of a desired compound semiconductor material. For the subsequent growth of a layer of gallium arsenide, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an appropriate template for deposition and formation of a gallium arsenide monocrystalline layer. Following the formation of the template, gallium is subsequently introduced to the reaction with the arsenic and gallium arsenide forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the present invention. Single crystal $SrTiO_3$ accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth process, amorphous interfacial layer 28 is formed which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

FIG. 6 illustrates an x-ray diffraction spectrum taken on structure including GaAs compound semiconductor layer 26 grown on silicon substrate 22 using accommodating buffer layer 24. The peaks in the spectrum indicate that both the accommodating buffer layer 24 and GaAs compound semiconductor layer 26 are single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer deposition step. The buffer layer is formed overlying the template layer before the deposition of the monocrystalline compound semiconductor layer. If the buffer layer is a compound semiconductor superlattice, such a superlattice can be deposited, by MBE for example, on the template described above. If instead the buffer layer is a layer of germanium, the process above is modified to cap the strontium titanate monocrystalline layer with a final layer of either strontium or titanium and then by depositing germanium to react with the strontium or titanium. The germanium buffer layer can then be deposited directly on this template.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22, and growing semiconductor layer 38 over the accommodating buffer layer, as described above. The accommodating buffer layer and the amorphous oxide layer are then exposed to an anneal process sufficient to change the crystalline structure of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer and the now amorphous accommodating buffer layer form a single amorphous oxide layer 36. Layer

26 is then subsequently grown over layer 38. Alternatively, the anneal process may be carried out subsequent to growth of layer 26.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the accommodating buffer layer, the amorphous oxide layer, and semiconductor layer 38 to a rapid thermal anneal process with a peak temperature of about 700°C to about 1000°C and a process time of about 10 seconds to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing or "conventional" thermal annealing processes (in the proper environment) may be used to form layer 36. When conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 may be required to prevent degradation of layer 38 during the anneal process. For example, when layer 38 includes GaAs, the anneal environment preferably includes an overpressure of arsenic to mitigate degradation of layer 38.

As noted above, layer 38 of structure 34 may include any materials suitable for either of layers 32 or 26. Accordingly, any deposition or growth methods described in connection with either layer 32 or 26 may be employed to deposit layer 38.

FIG. 7 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the embodiment of the invention illustrated in FIG. 3. In Accordance with this embodiment, a single crystal $SrTiO_3$ accommodating buffer layer was grown epitaxially on silicon substrate 22. During this growth process, an amorphous interfacial layer forms as described above. Next, GaAs layer 38 is formed above the accommodating buffer layer and the accommodating buffer layer is exposed to an anneal process to form amorphous oxide layer 36.

FIG. 8 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor layer 38 and amorphous oxide layer 36 formed on silicon substrate 22. The peaks in the spectrum indicate that GaAs compound

semiconductor layer 38 is single crystal and (100) orientated and the lack of peaks around 40 to 50 degrees indicates that layer 36 is amorphous.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a monocrystalline gallium arsenide compound semiconductor layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, peroskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other III-V and II-VI monocrystalline compound semiconductor layers can be deposited overlying the monocrystalline oxide accommodating buffer layer.

Each of the variations of compound semiconductor materials and monocrystalline oxide accommodating buffer layer uses an appropriate template for initiating the growth of the compound semiconductor layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of arsenic or phosphorus to react with the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if the monocrystalline oxide accommodating buffer layer is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of arsenic or phosphorous to react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum arsenide, or indium phosphide layer, respectively. In a similar manner, strontium titanate can be capped with a layer of strontium or strontium and

oxygen and barium titanate can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of arsenic or phosphorus to react with the capping material to form a template for the deposition of a compound semiconductor material layer comprising indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

FIG. 9 illustrates schematically, in cross section, a device structure 50 in accordance with a further embodiment of the invention. Device structure 50 includes a monocrystalline semiconductor substrate 52, preferably a monocrystalline silicon wafer. Monocrystalline semiconductor substrate 52 includes two regions, 53 and 54. An electrical semiconductor component generally indicated by the dashed line 56 is formed, at least partially, in region 53. Electrical component 56 can be a resistor, a capacitor, an active semiconductor component such as a diode or a transistor or an integrated circuit such as a CMOS integrated circuit. For example, electrical semiconductor component 56 can be a CMOS integrated circuit configured to perform digital signal processing or another function for which silicon integrated circuits are well suited. The electrical semiconductor component in region 53 can be formed by conventional semiconductor processing as well known and widely practiced in the semiconductor industry. A layer of insulating material 58 such as a layer of silicon dioxide or the like may overlie electrical semiconductor component 56.

Insulating material 58 and any other layers that may have been formed or deposited during the processing of semiconductor component 56 in region 53 are removed from the surface of region 54 to provide a bare silicon surface in that region. As is well known, bare silicon surfaces are highly reactive and a native silicon oxide layer can quickly form on the bare surface. A layer of barium or barium and oxygen is deposited onto the native oxide layer on the surface of region 54 and is reacted with the oxidized surface to form a first template layer (not shown). In accordance with one embodiment of the invention a monocrystalline oxide layer is formed overlying the template layer by a process of molecular beam epitaxy. Reactants including barium, titanium and oxygen are deposited onto the template layer to form the monocrystalline

oxide layer. Initially during the deposition the partial pressure of oxygen is kept near the minimum necessary to fully react with the barium and titanium to form the monocrystalline barium titanate layer. The partial pressure of oxygen is then increased to provide an overpressure of oxygen and to allow oxygen to diffuse through the growing monocrystalline oxide layer. The oxygen diffusing through the barium titanate reacts with silicon at the surface of region 54 to form an amorphous layer of silicon oxide on the second region and at the interface between the silicon substrate and the monocrystalline oxide.

In accordance with an embodiment of the invention, the step of depositing the monocrystalline oxide layer is terminated by depositing a second template layer 60, which can be 1-10 monolayers of titanium, barium, strontium, barium and oxygen, titanium and oxygen, or strontium and oxygen. A layer 64 of a monocrystalline semiconductor material is then deposited overlying the second template layer by a process of molecular beam epitaxy. The deposition of layer 64 may be initiated by depositing a layer of arsenic onto the template. This initial step is followed by depositing gallium and arsenic to form monocrystalline gallium arsenide.

In accordance with one aspect of the present embodiment, after semiconductor layer 60 formation, the monocrystalline titanate layer and the silicon oxide layer, which is interposed between substrate 52 and the titanate layer, are exposed to an anneal process such that the titanate and oxide layers form an amorphous oxide layer 62. An additional compound semiconductor layer 66 is then epitaxially grown over layer 64, using the techniques described above in connection with layer 64, to form compound semiconductor layer 67. Alternatively, the above described anneal process can be performed after formation of additional compound semiconductor layer 66.

In accordance with a further embodiment of the invention, a semiconductor component, generally indicated by a dashed line 68 is formed, at least partially, in compound semiconductor layer 66. Semiconductor component 68 can be formed by processing steps conventionally used in the fabrication of gallium arsenide or other III-V compound semiconductor material devices. Semiconductor component 68 can be

any active or passive component, and preferably is a semiconductor laser, an electromagnetic radiation (*e.g.*, light--infra red to ultra violet radiation) emitting device, an electromagnetic radiation detector such as a photodetector, a heterojunction bipolar transistor (HBT), a high frequency MESFET, or another component that utilizes and takes advantage of the physical properties of compound semiconductor materials. A metallic conductor schematically indicated by the line 70 can be formed to electrically couple device 68 and device 56, thus implementing an integrated device that includes at least one component formed in the silicon substrate and one device formed in the monocrystalline compound semiconductor material layer. Although illustrative structure 50 has been described as a structure formed on a silicon substrate 52 and having a barium (or strontium) titanate layer and a gallium arsenide layer 66, similar devices can be fabricated using other monocrystalline substrates, oxide layers and other monocrystalline compound semiconductor layers as described elsewhere in this disclosure.

FIG. 10 illustrates a biological material analysis system 1000 in accordance with the present invention. System 1000 includes a biochip 1010 and an analysis chip or structure 1020. The combination of biochip 1010 and structure 1020 facilitates analysis of biomaterial (present on the biochip), and allows the analysis to be performed in remote locations at relatively low cost.

Biochip 1010 includes a substrate 1030, pads 1040, biological material or probe 1045 and sample material or target 1050. Substrate 1030 may be formed of any suitable material. For example, substrate 1030 may be formed of glass, plastic, or semiconductor material such as silicon that is suitably modified to be compatible with biological material. Pads 1040 generally include material 1045 that reacts with or bonds to sample material 1050. For example, when used to analyze DNA material, material 1045 suitably includes DNA oligos designed to attract particular DNA oligos of sample material 1050.

Pads or probe sites 1040 may be formed in a variety of ways. For example, when biochip 1010 is used to perform DNA analysis, sites 1040 may be formed by (1)

photolithographically patterning porous gel such as agarose or polyacrylamide and spotting properly conjugated reagents and DNA probes onto the gel using, for example, ink jet technology; or (2) selectively chemically activating areas to attach DNA material (*e.g.*, material 1045).

As described in more detail below, sample biological material 1050 (*e.g.*, target oligos), which bonds to the complimentary probe 1045, includes fluorescent tags or markers to facilitate detection of particular oligos in the sample. The fluorescent tags may be excited at a particular wavelength, and once the fluorescent material is excited, the material emits light of a wavelength that is longer than the wavelength of the incident light. Exemplary fluorescent tag materials include: Cyanine 5 (excitation 8 = 630 nm, emission 8 = 650 nm), Cyanine 3 (excitation 8 = 530 nm, emission 8 = 550 nm), Texan Red 5 (excitation 8 = 530 nm, emission 8 = 550 nm), and Tamra 5 (excitation 8 = 530 nm, emission 8 = 550 nm), all available from Molecular Probes.

Biochip 1010 may also include spacers 1055 configured to maintain a separation between biochip 1010 and structure 1020. Spacers 1055 may be formed of any suitable material such as plastic or the like. In accordance with alternate aspects of the invention, spacers 1055 may be formed on substrate 1020, or a combination of substrate 1020 and biochip 1010. In accordance with yet another aspect of this embodiment, spacers 1055 may be interposed between biochip 1010 and structure 1020 and held in place by, for example, pressure applied to biochip 1010, structure 1020, or both.

Structure 1020 includes a light emitting device 1060, a light detecting device 1070 and circuits 1080 and 1085 configured to drive devices 1060 and 1070, respectively . Structure 1020 may also include additional circuits and/or devices such as an RF transmission device 1090.

In general, structure 1020 is configured to facilitate analysis of material 1050 by emitting light toward material 1050 using emitter 1060 and analyzing light reflected from material 1050 using detector 1070. In particular, when biological material 1050 includes fluorescent material, material present on a pad 1040 can be detected by emitting light of a first wavelength toward material 1050 and detecting light of a second

wavelength emitted from the sample. Light of the second wavelength is emitted from the sample if the sample includes a fluorescent marker and an excitation event occurs; light of the second wavelength is not emitted if biological material, having a fluorescent marker attached thereto, is absent from the pad.

Structure 1020 may be further configured to transmit information obtained from detector 1070 to a remote location using RF device 1090. For example, information obtained from detectors 1070 may be analyzed using one or more circuits 1080, and the results from the analysis may be transmitted to a remote site using device 1090.

As discussed in greater detail below, emitting device 1060 is formed using one or more compound semiconductor material layers such as layer 66 described above in connection with FIG. 9. In accordance with exemplary embodiments of the invention, device 1060 includes a laser, such as an edge emitting laser or a vertical cavity surface emitting laser (VCSEL), or a light emitting diode formed using one or more compound semiconductor layers. Structure 1020 may include various numbers of emitters 1060 for each biochip pad 1040 to be analyzed. For example, structure 1020 may include one emitter 1060 for each pad 1040, or one emitter may be configured to emit light toward and excite fluorescent material on multiple pads 1040.

Detector 1070 may include any suitable photodetector such as a photodiode, and may be formed either using compound semiconductor material or a Group IV semiconductor material or materials. In accordance with exemplary embodiments of the invention, structure 1020 includes at least one detector 1070 for each pad 1040 to be analyzed.

Circuit 1080 may include any suitable circuit for driving and/or controlling emitting device 1060 and/or detector 1070. For example, circuit 1080 may include a metal-oxide-semiconductor (MOS) circuit formed within either a Group IV material or materials or a compound semiconductor material layer. Circuit 1080 or additional circuits (not illustrated) formed within structure 1020 may further include programmed logic to facilitate diagnosis or analysis of biological material. As illustrated, circuit

1080 is suitably coupled to emitters 1060 and detectors 1070 using conductive material schematically illustrated as line 1095.

FIG. 11 illustrates a structure 1100 suitable for facilitating analysis of biological material in accordance with a further embodiment of the invention. Structure 1100 includes a VCSEL light emitting source 1110, a photodetector 1120, a circuit 1130 to drive VCSEL 1110 and photodetector 1120, and an RF transmitting device 1140.

VCSEL 1110 includes bottom mirror layers 1112, a laser cavity region 1114, an upper mirror region 1116, and a ring-shaped contact 1118. In accordance with one embodiment of the invention, VCSEL 1110 is formed by epitaxially growing lower mirror region 1112 layers, laser cavity region 1114 layers, and upper mirror 1116 layers over a Group IV substrate 1150 (which may include various devices such as CMOS circuits and driver circuit 1130 formed therein) and an amorphous oxide layer 1160, as discussed above in connection with FIGS. 3 and 7. Alternatively, mirror regions 1112, 1116 and active region 1114 layers may be formed over a monocrystalline oxide layer as discussed above in connection with FIGS. 1 - 2.

Lower mirror region 1112 layers include alternating layers of compound semiconductor materials. For example, the first, third, and fifth layers of the lower region may include a material such as gallium arsenide, and the second, fourth, and sixth layers within the mirror region 1112 may include aluminum gallium arsenide or vice versa.

Upper mirror region 1116 layers are formed in a similar manner to the lower mirror region 1112 layers and include alternating films of compound semiconductor materials. In one particular embodiment, upper mirror 1116 layers may be p-type doped compound semiconductor materials, and lower mirror 1140 layers may be n-type doped compound semiconductor materials, and each layer within mirror regions 1112 and 1116 have a thickness of about 8/4, where 8 is the wavelength of light emitted from the laser source.

Detector 1120 is generally configured to convert light emitted from fluorescent markers or tags on a biological sample into an electrical signal. Accordingly, detector

1120 is typically configured to produce electrical signals in response to particular light wavelengths that are emitted by the fluorescent material.

In accordance with an exemplary embodiment of the invention, detector 1120 includes an active region 1122 and contacts 1126 and 1128. Active region 1122 may be formed of a variety of crystalline, polycrystalline, or amorphous materials such as silicon, GaAs, and InGaAs; however, in accordance with one embodiment of the present invention, region 1122 is formed of the same material used to form region 1114 of emitter 1110, such as monocrystalline GaAs, and a lower portion of detector 1124 is formed of material layers used to form lower mirror region 1112 of emitter 1110.

An exemplary method of forming monolithically integrated emitters and photodetectors over a group IV substrate is discussed below in connection with FIGS. 12 - 14. Initially, a structure 1200 is formed by forming a monocrystalline oxide layer over a Group IV substrate 1210, forming an amorphous oxide layer between the growing crystalline oxide and substrate 1220, capping the oxide with a cap layer 1230, and exposing the crystalline oxide and amorphous oxide layers to an anneal process to cause the monocrystalline oxide material to form amorphous oxide layer 1220. Next, lower mirror region layers 1240, active region layer 1250, and upper mirror region layers are epitaxially grown over cap layer 1230 using methods described above in connection with FIGS. 1-3.

A structure 1300, illustrated in FIG. 13, is then formed by photolithographically patterning structure 1200 and removing portions of structure 1220 to form VCSEL 1310 and photo diode 1320.

An integrated circuit may be formed using substrate 1210 either before or after emitter 1310 and detector 1320 are formed. For example, in accordance with one embodiment of the invention, after emitter 1310 and detector 1320 are formed, structure 1300 is patterned and etched to remove a portion of layer 1220, as illustrated in FIG. 14. A circuit 1410 such as a bipolar or MOS circuit may then be formed using semiconductor substrate 1210, and circuit 1410 may be electrically coupled to emitter 1310 and detector 1320 using interconnects illustrated as lines 1420 – 1450.

Alternatively, circuit 1410 may be formed prior to growing layers 1220- 1260, illustrated in FIG. 12.

FIG. 15 illustrates a structure 1500 in accordance with another exemplary embodiment of the invention. Structure 1500 is similar to structure 1100, except structure 1500 includes an edge emitting laser 1510 rather than a VCSEL, and a detector 1520 is formed using a Group IV substrate, rather than using a compound semiconductor layer to form the detector. Similar to structure 1100, structure 1500 suitably includes an RF transmission device 1530 and circuits 1540 and 1545 to drive emitter 1510 and detector 1520, respectively. Circuit 1540 is coupled to emitter 1510 and detector 1520 using interconnects represented as lines 1550 and 1560.

Various components of structures 1100 and 1500 may be interchanged in accordance with various embodiments of the invention. For example, a structure in accordance with the present invention may include a VCSEL and a detector formed within a Group IV substrate. Similarly a structure in accordance with another embodiment may include an edge emitting laser and a detector formed using compound semiconductor material layers.

In accordance with the illustrated embodiment, emitter 1510 is formed over a Group IV substrate 1570 and an amorphous oxide layer 1580 formed thereon, wherein amorphous oxide layer 1580 is formed according to the method described above, for example, in connection with layer 36. In accordance with an alternate embodiment of the invention, emitter 1510 may be formed over a monocrystalline oxide layer such as layer 24 discussed above in connection with FIGS. 1,2, and 5.

In accordance with one aspect of the embodiment illustrated in FIG. 15, emitter 1510 includes a first cladding layer 1512, an active region 1514, and a second cladding layer 1516. Layers 1512-1516 may be formed of any suitable semiconductor material such as compound semiconductor materials discussed above in connection with layer 26. For example, first cladding layer 1512 may include n-type doped AlGaAs, active layer 1514 may include GaAs, and second cladding layer 1516 may include p-doped AlGaAs, where each of layer 1512-1516 is epitaxially formed over substrate 1570.

Although not illustrated, structure 1500 may also include insulating layers to facilitate electrical isolation of emitter 1510 or components thereof and/or conducting layers to facilitate coupling of emitter 1510 to other devices or components.

Detector 1520 includes diode structures formed using substrate 1570 material. In accordance with various embodiments of the invention, detector 1520 may include p-n junction diodes, p-i-n diodes, or metal-semiconductor diodes.

RF device 1530 and circuit 1540 may include the same devices discussed above in connection with RF device 1140 and circuit 1130. Accordingly, further discussion of these components is omitted from the description of structure 1500.

To facilitate light emission in a direction perpendicular to a surface of substrate 1570, structure 1500 may be formed within a trench 1590 formed in a Group IV substrate 1570. Trench 1590 may be formed using any suitable etch techniques and is preferably formed using an anisotropic etch, such that side walls 1595 of the trench are angled (e.g., at above 57.4 degrees from a plane perpendicular to a plane intersecting a top surface of substrate 1570) as illustrated in FIG. 15. Substrate 1570 may include various devices such as CMOS circuits formed therein.

Emitter 1510 may then be formed by depositing first cladding, active region, and second cladding layers, patterning the layers, and etching the layers to form emitter 1510.

In accordance with various embodiments of the present invention, detectors may include lenses to focus light. For example, FIG. 16 illustrates a structure 1600 that includes a detector 1610, which may include a photodiode formed using either a compound semiconductor material or a Group IV semiconductor material or materials as described above in connection with detectors 1120 and 1520, and a microlens 1620 formed above detector 1610.

Microlens 1620 is generally configured to focus light received from fluorescent material on a nearby biochip pad onto a portion of detector 1610. In accordance with one embodiment of the invention, microlens 1620 is formed by molding material such as plastic or epoxy over a portion of detector 1610. Alternatively, diffractive optical

elements or holograms may be used to focus and/or direct light on or toward a desired location.

Various structures in accordance with the present invention may also include light filters to facilitate detection of fluorescent markers present on a biochip. FIG. 17 illustrates a structure 1700 that includes a detector 1710, which may include any device suitable for detector 1610. A filter 1720, configured to transmit light within a certain range of wavelengths, is placed between detector 1710 and a light source. Filter 1720 may include any suitable filter such as a narrow band pass filter that transmits light of a wavelength at or near the wavelength of light resulting from excitation of the fluorescent tag material and reflects light having a wavelength of light emitted from lasers or other light sources.

Filter 1720 may be formed in a variety of ways and in a variety of configurations. For example, filter 1720 may include films deposited on a top surface of detector 1710 to form, for example, an interference filter. Alternatively, filter 1710 may include a thin film of material such as plastic interposed between detector 1710 and a biochip, wherein the plastic material is cut, drilled, etched, or otherwise removed from areas between an emitter and the biochip. This configuration allows unfiltered light to pass from the emitter to the biological material sample, and only allows filtered light to pass from the biological sample to detector 1710.

Emitters, in accordance with the present invention, may also include lenses to focus light. FIG. 18 illustrate a structures 1800, including an emitter 1810 and a microlens 1820. Emitter 1810 may be an edge emitting laser, a VCSEL, or a light emitting diode as discussed above in connection with FIGS. 11- 15.

Microlens 1820 is configured to direct and focus light emitted from emitter 1810 toward a specific pad on a biochip. Structure 1800 may be used, for example, when an analysis system in accordance with the present invention is configured to activate a subset of emitters at one time. Microlens 1820 may be formed according to the method and using the materials described above in connection with microlens 1620. In accordance with alternate embodiments of the invention, diffractive optical elements

or holograms may be used to focus and/or direct light of a desired wavelength onto or toward the desired pad.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

What is claimed:

1. A structure suitable for facilitating analysis of biological material comprising:

a Group IV substrate;

a compound semiconductor material epitaxially formed over said substrate;

a light emitting device formed using said compound semiconductor material; and

a light detecting device proximate said light emitting device.

2. The structure of claim 1, further comprising a monocrystaline buffer layer interposed between said substrate and said compound semiconductor material.

3. The structure of claim 2, wherein said buffer layer comprises a monocrystaline oxide material.

4. The structure of claim 3, wherein said monocrystaline oxide material is selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

5. The structure of claim 2, wherein said buffer material includes $Sr_zBa_{1-z}TiO_3$.

6. The structure of claim 2, further comprising an amorphous layer interposed between said substrate and said buffer layer.

7. The structure of claim 1, further comprising an amorphous intermediate layer interposed between said substrate and said compound semiconductor material.

8. The structure of claim 7, wherein said amorphous intermediate layer includes an amorphous oxide material.

9. The structure of claim 1, further comprising a template layer interposed between said substrate and said compound semiconductor material.

10. The structure of claim 9, wherein said template layer is configured to facilitate monocrystaline growth of said compound semiconductor material.

11. The structure of claim 9, wherein said template layer is configured to facilitate monocrystaline growth of said buffer layer.

12. The structure of claim 1, wherein said compound semiconductor material includes GaAs.

13. The structure of claim 1, wherein said substrate comprises silicon.

14. The structure of claim 1, further comprising a second layer of compound semiconductor material.

15. The structure of claim 1, wherein said detector includes a photo diode.

16. The structure of claim 1, wherein said detector is formed using a portion of said substrate.

17. The structure of claim 14, wherein said photodetector is formed using a portion of said compound semiconductor material.

18. The structure of claim 1, further comprising an RF device formed using said compound semiconductor material.

19. The structure of claim 1, further comprising a circuit formed within said substrate, said circuit coupled to said light emitting device.

20. The structure of claim 1, further comprising a microlens formed over a portion of said light emitting device.

21. The structure of claim 1, further comprising a microlens formed over a portion of said detector.

22. The structure of claim 1, further comprising a filter formed over a portion of said detector.

23. The structure of claim 1, wherein said light emitting device includes a vertical cavity surface emitting laser.

24. The structure of claim 1, wherein said light emitting device includes an edge emitting laser.

25. The structure of claim 1, wherein said light emitting device includes a light emitting diode.

26. A method of forming a structure suitable for analyzing biologic material, said method comprising the steps of:

providing a Group IV substrate;

forming a buffer layer on said substrate;

epitaxially growing a compound semiconductor over said buffer layer; and

forming a light emitting device using at least a portion of said compound semiconductor material.

27. The method of claim 26, further comprising the step of forming an amorphous interface layer.

28. The method of claim 26, further comprising the step of exposing the buffer layer to an anneal process to cause the buffer layer to become amorphous.

29. The method of claim 28, wherein said step of exposing the buffer layer to an anneal process includes exposing the buffer layer to a rapid thermal anneal process at a temperature of about 700 – 1000 °C.

30. The method of claim 26, further comprising the step of removing a native oxide from a surface of said substrate.

31. The method of claim 26, further comprising the step of forming an anneal cap over the buffer layer.

32. The method of claim 26, wherein the step of forming a buffer layer includes depositing buffer layer material using a process selected from the group consisting of molecular beam epitaxy, chemical vapor deposition, metal organic

chemical vapor deposition, migration enhanced epitaxy, atomic layer epitaxy, physical vapor deposition, chemical solution deposition, or pulsed laser deposition.

33. The method of claim 26, wherein the step of epitaxially growing a compound semiconductor material includes depositing the material using a process selected from a from a group consisting of molecular beam epitaxy, chemical vapor deposition, metal organic chemical vapor deposition, migration enhanced epitaxy, atomic layer epitaxy, physical vapor deposition, chemical solution deposition, or pulsed laser deposition.

34. A biological material analysis system comprising:

a biochip; and

a structure for analyzing material on said biochip comprising a light emitting device having epitaxially layers of compound semiconductor material formed over a Group IV substrate, said structure placed proximate said biochip.

35. The biological material analysis system of claim 34, wherein said structure further comprises of photodetector.

36. The biological material analysis system of claim 35, further comprising a microlens coupled to a portion of said photodetector.

37. The biological material analysis system of claim 35, further comprising a filter coupled to a portion of said photodetector.

38. The biological material analysis system of claim 34, further comprising an RF device.

39. The biological material analysis system of claim 34, further comprising a microelectronic circuit coupled to said light emitting device.

40. The biological material analysis system of claim 34, further comprising a spacer interposed between said biochip and said structure.

41. The biological material analysis system of claim 34, further comprising a microlens formed over a portion of said light emitting device.

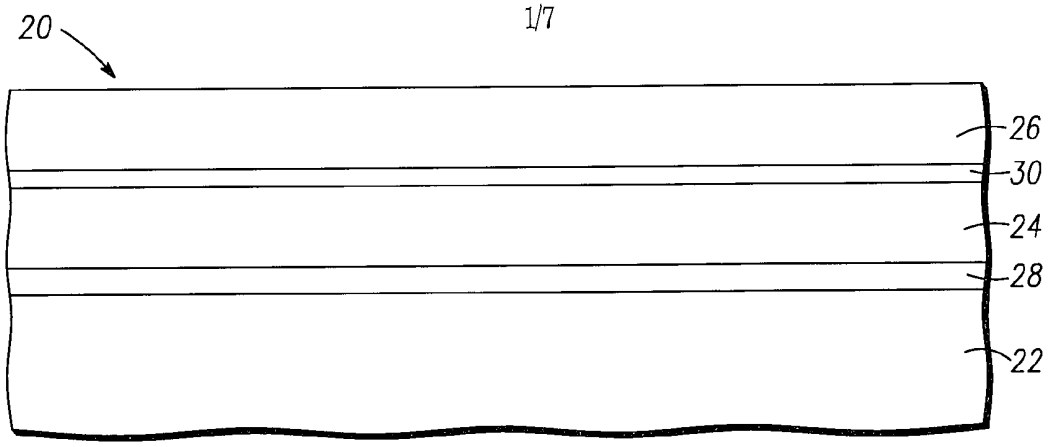


FIG. 1

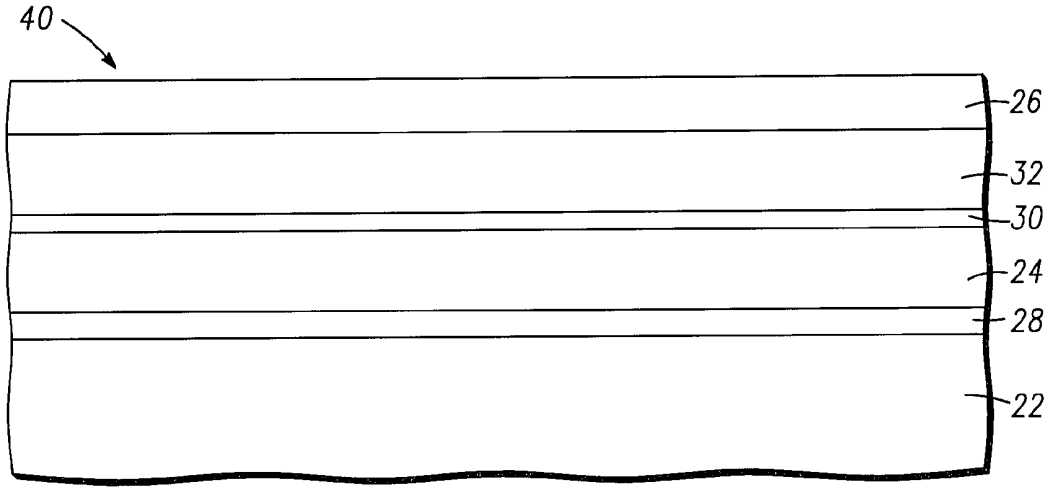


FIG. 2

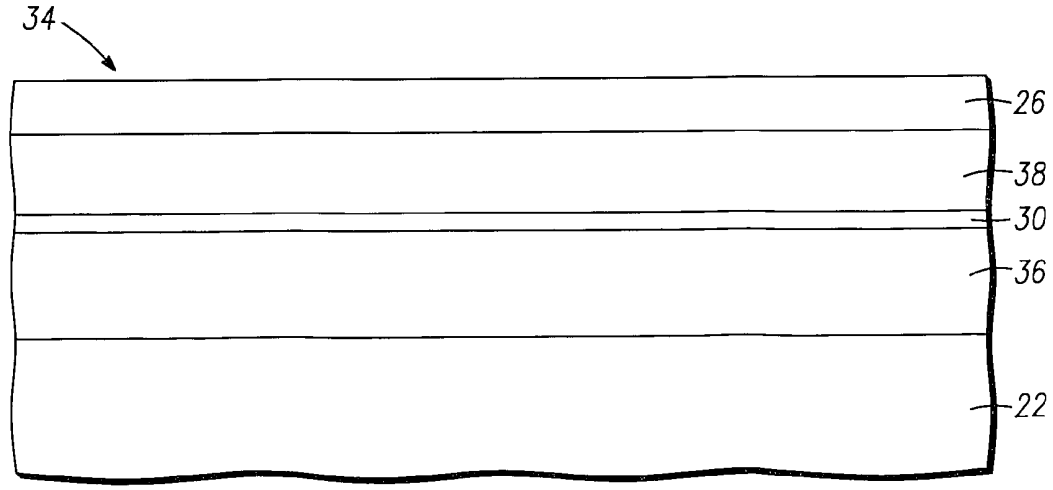


FIG. 3

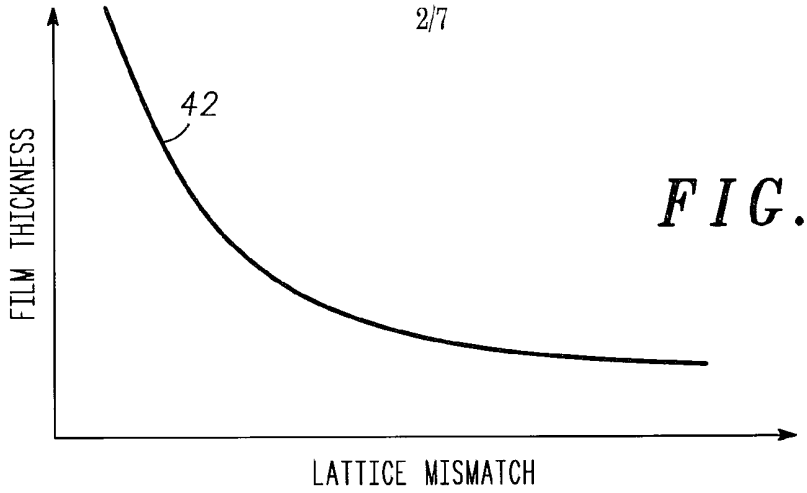


FIG. 4

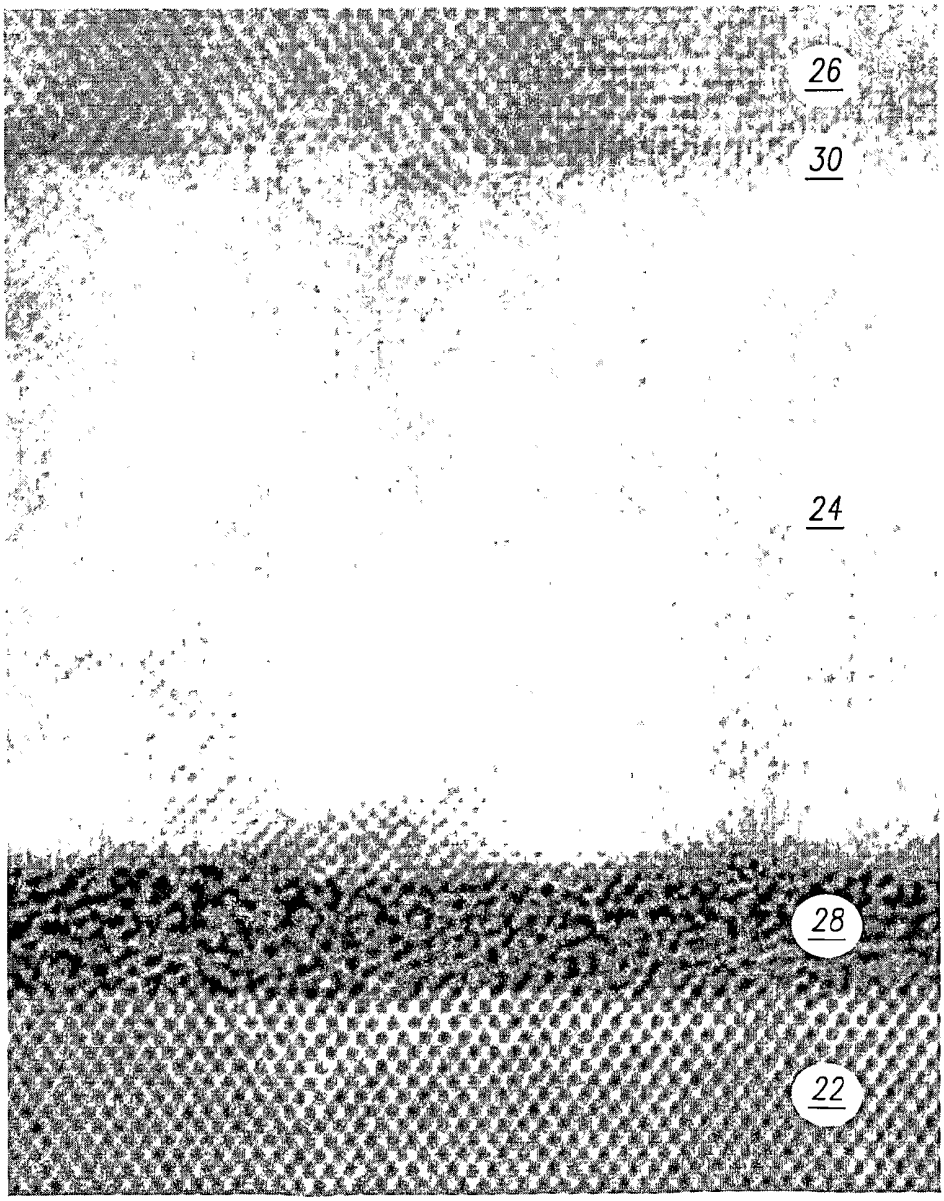
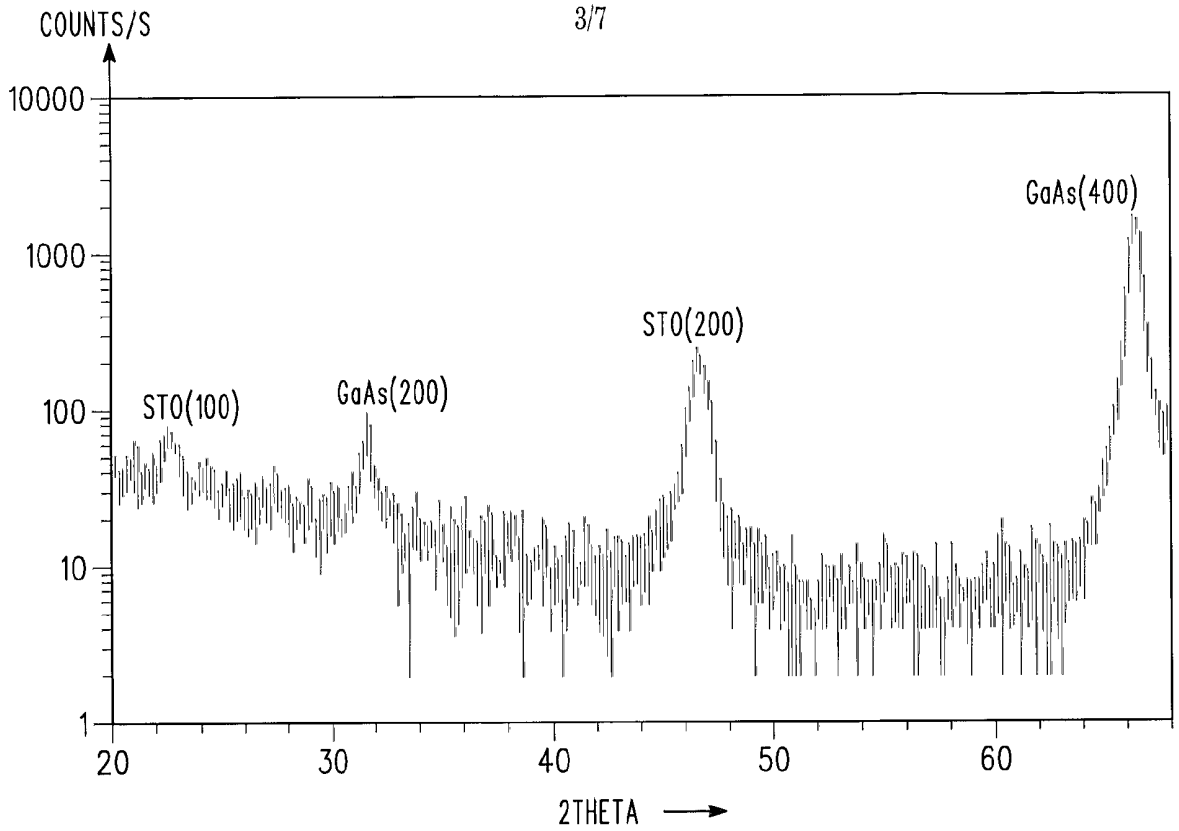


FIG. 5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60
2THETA
STO(100)
GaAs(200)
STO(200)
GaAs(400)

FIG. 6

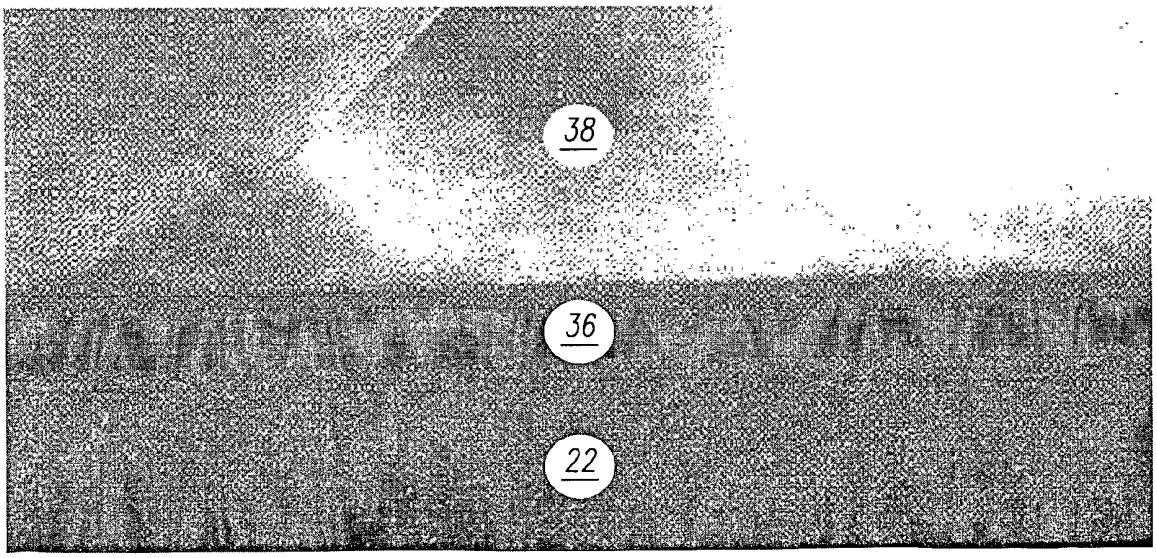
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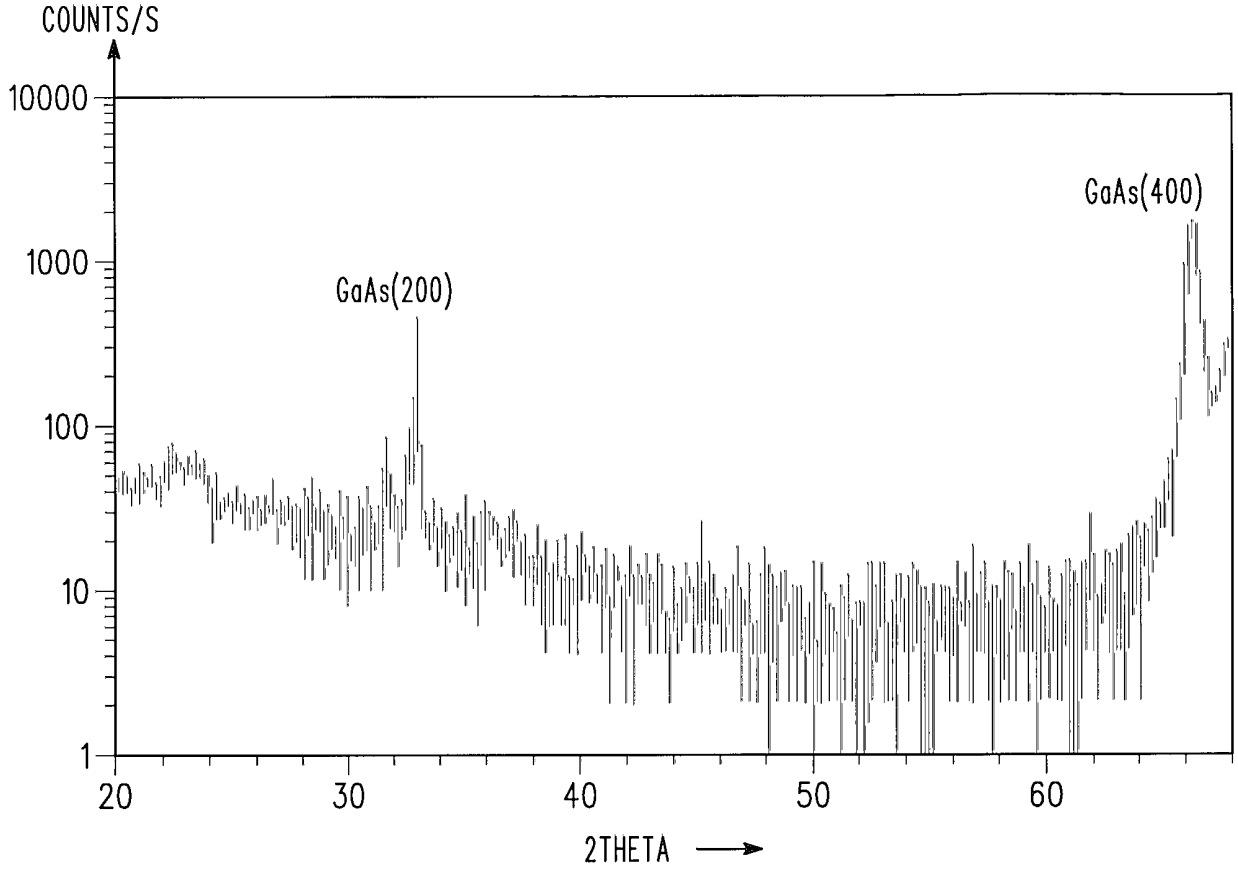
FIG. 7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2THETA
GaAs(200)
GaAs(400)

FIG. 8

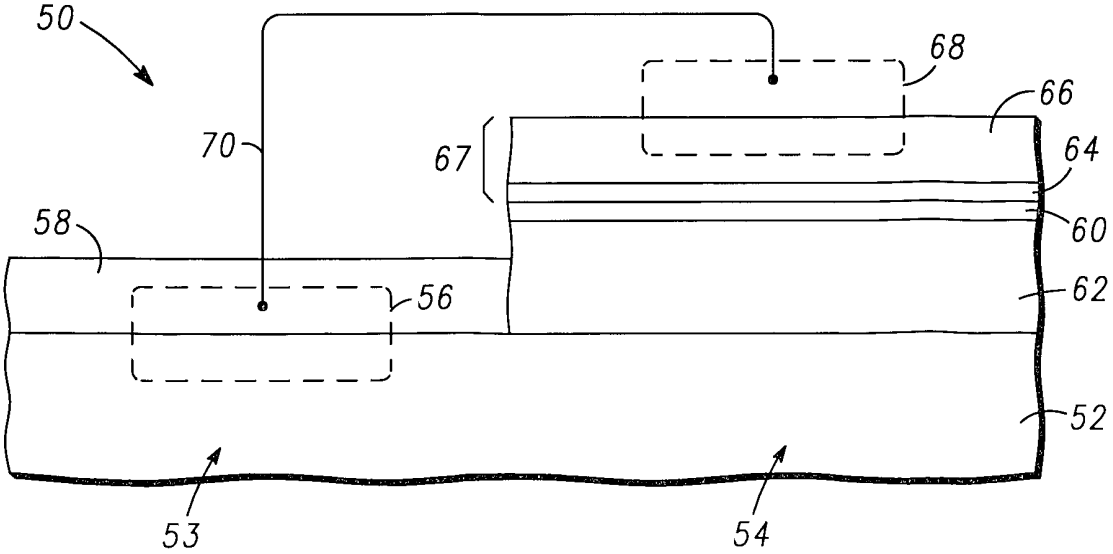
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FIG. 9

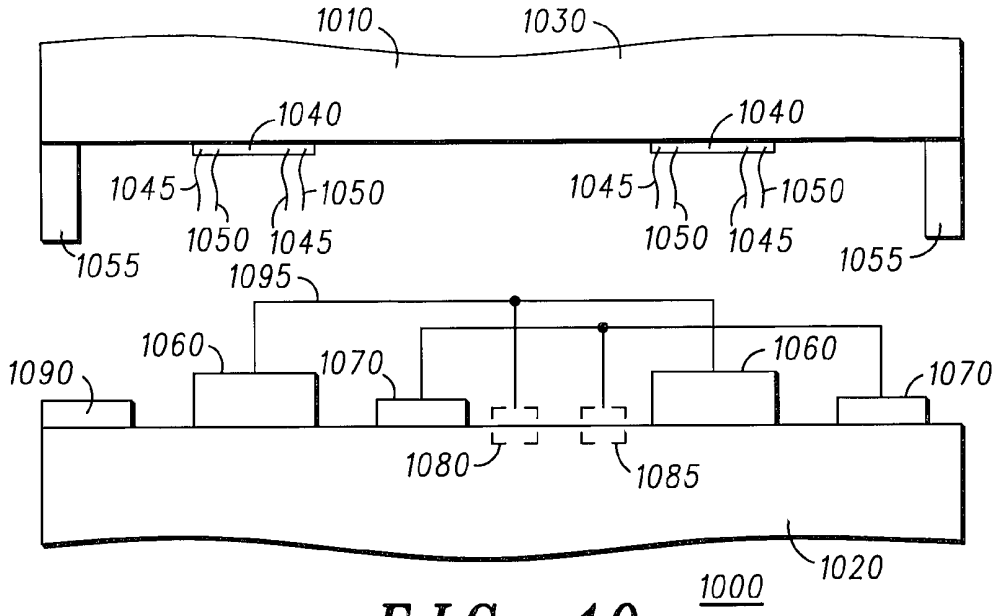

FIG. 10

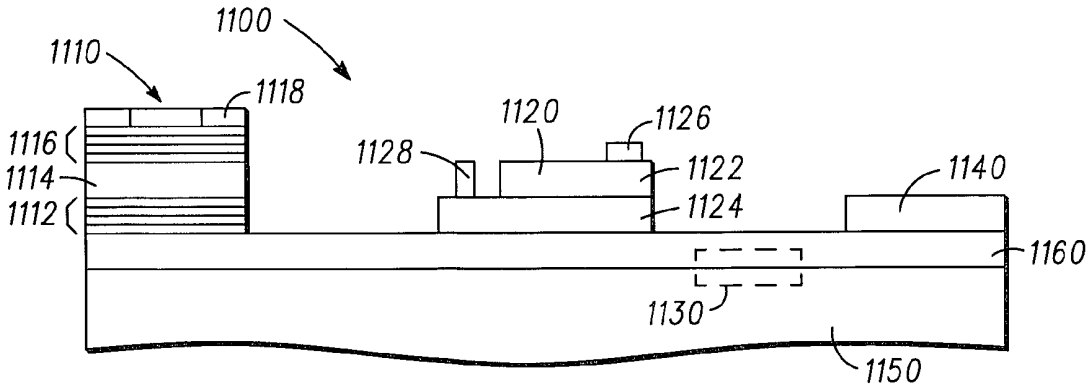

FIG. 11

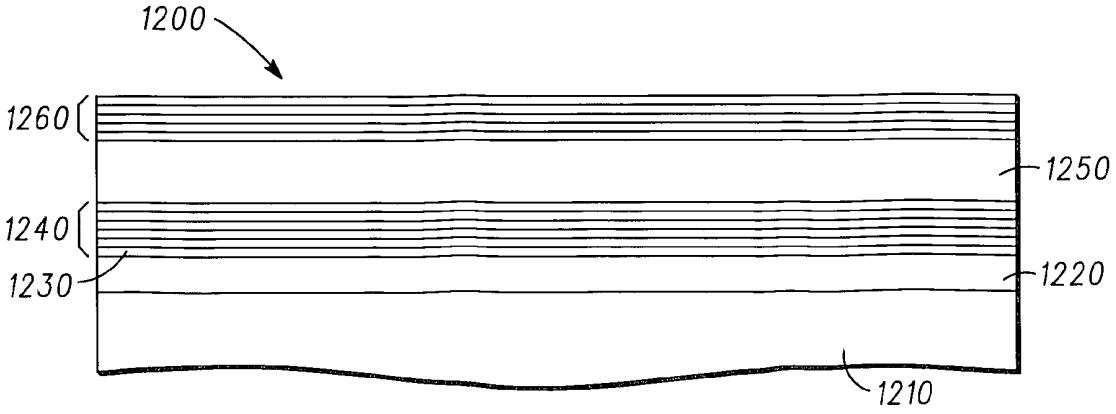

FIG. 12

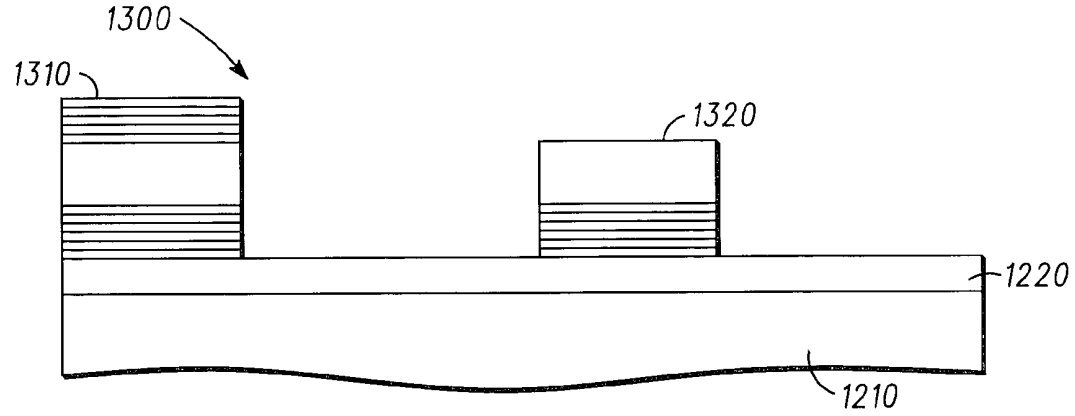

FIG. 13

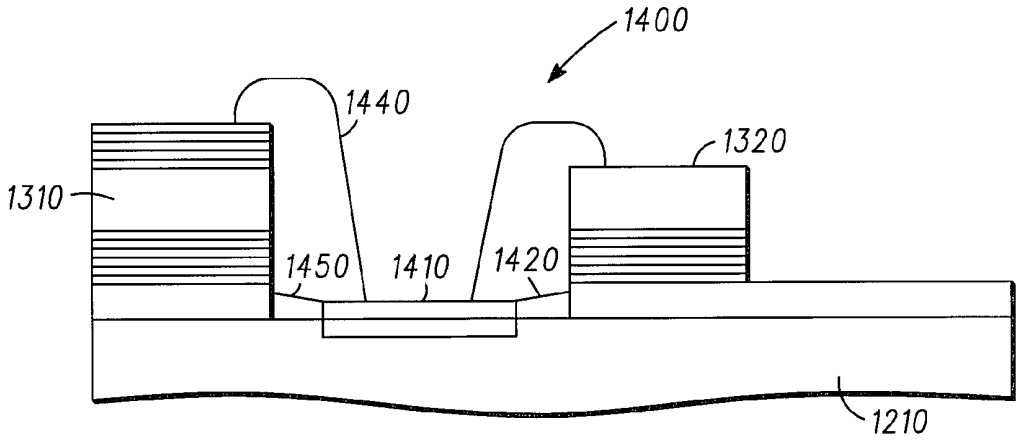

FIG. 14

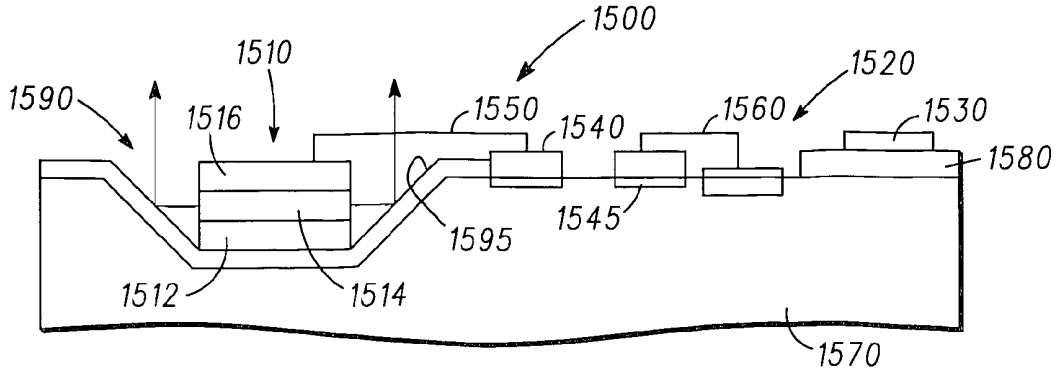

FIG. 15

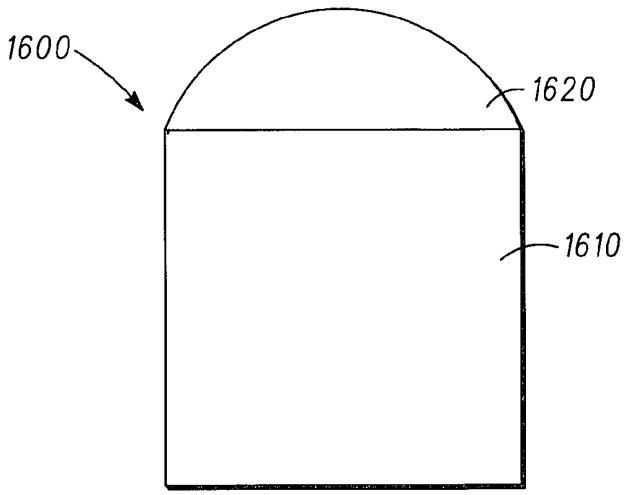

FIG. 16

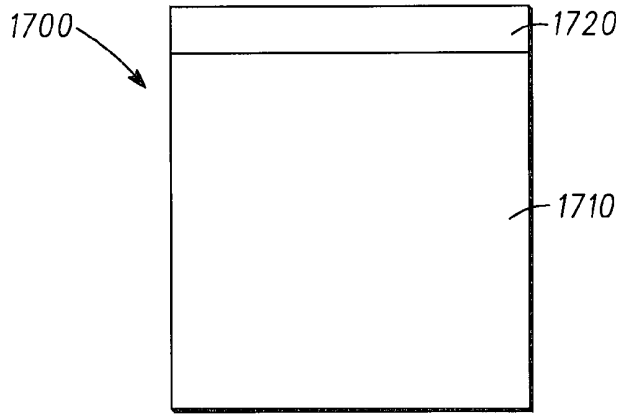

FIG. 17

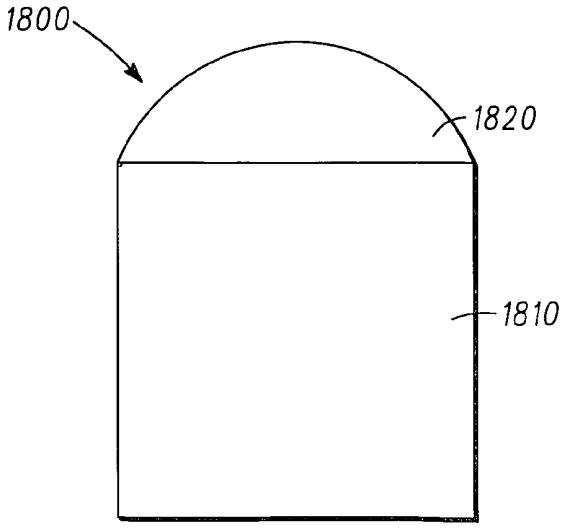

FIG. 18