(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 December 2016 (29.12.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/209861 A1

(51) International Patent Classification:
G06F 13/42 (2006.01)

(21) International Application Number:
PCT/US2016/038614

(22) International Filing Date:
22 June 2016 (22.06.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/183,272 23 June 2015 (23.06.2015) US
15/188,464 21 June 2016 (21.06.2016) US

(71) Applicant: **MICROCHIP TECHNOLOGY INCORPORATED** [US/US]; 2355 West Chandler Blvd., Chandler, Arizona 85224-6199 (US).

(72) Inventor: **SAMUEL, Roshan**; 5065 S. Mingus Pl., Chandler, Arizona 85249 (US).

(74) Agent: **SLAYDEN, Bruce W., II**; Slayden Grubert Beard PLLC, 401 Congress Ave., Suite 1900, Austin, Texas 78701 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: UART WITH LINE ACTIVITY DETECTOR

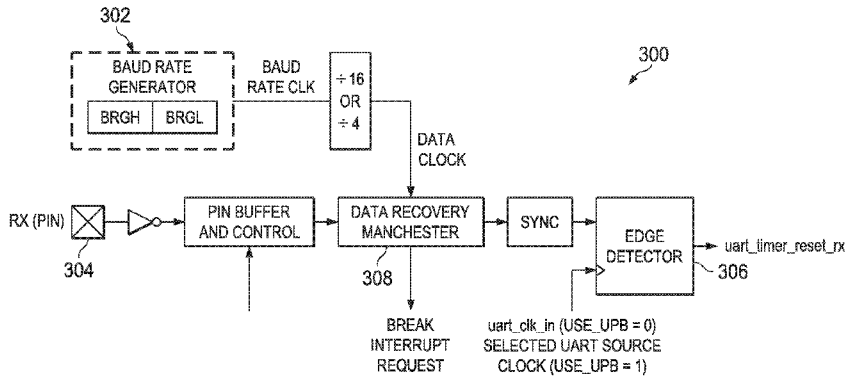

FIG. 3

(57) Abstract: A universal asynchronous receiver/transmitter (UART) module is disclosed. The UART module may include an edge detector coupled with a data line of the UART module, wherein the edge detector resets a counter on a rising and a falling edge.

WO 2016/209861 A1

UART With Line Activity Detector

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to United States Provisional Patent Application No. 62/183,272, filed June 23, 2015, which is hereby incorporated by reference herein for all purposes.

TECHNICAL FIELD

The present disclosure relates to serial interfaces, in particular to a universal asynchronous receiver/transmitter (UART) interface with line activity detector.

BACKGROUND

UARTs are well known and commonly used in microcontrollers to provide a communication channel. A UART interface translates parallel data into a serial transmission form. Various types of protocols exists and are used in UART communication as defined by various communication standards such as EIA, RS-232, RS-422 or RS-485. Other protocols, such as the DMX protocol use the same interface configuration as a RS-232 interface.

SUMMARY

There exists a need to provide a UART that allows for a timeout period in accordance with certain protocols in a simplified manner that does not rely on a dedicated timer or software.

According to various embodiments, a universal asynchronous receiver/transmitter (UART) module is disclosed. The UART module may include an edge detector coupled with a data line of the UART module, wherein the edge detector resets a counter on a rising and a falling edge.

In some embodiments, the edge detector may include a first edge detector circuit coupled with a receiving line. In such embodiments, an external receiving line is coupled with a buffer and a data recovery unit and wherein the first edge detector is coupled with an output of the data recovery unit. In other such embodiments, the module may further include a first counter which is reset on each rising and falling edge.

In some embodiments, the edge detector may include a second edge detector circuit coupled with a transmitting line. In such embodiments, the module may also include a transmit register coupled with a buffer which is coupled with an external pin and a second edge detector. In other such embodiments, the module may include a second counter which is reset on each rising and falling edge on the transmitting line.

According to various embodiments, a microcontroller is disclosed. The microcontroller may include a universal asynchronous receiver/transmitter (UART) module comprising an edge detector coupled with a data line of the UART module, wherein the edge detector resets a counter on a rising and a falling edge, wherein the microcontroller does not include a dedicated timer for timing a timeout period associated with a communication protocol.

In some embodiments, the edge detector may include a first edge detector circuit coupled with a receiving line. In such embodiments, an external receiving line is coupled with a buffer and a data recovery unit and wherein the first edge detector is coupled with an output of the data recovery unit. In other such embodiments, the module may further include a first counter which is reset on each rising and falling edge.

In some embodiments, the edge detector may include a second edge detector circuit coupled with a transmitting line. In such embodiments, the module may also include a transmit register coupled with a buffer which is coupled with an external pin and a second edge detector. In other such embodiments, the module may include a second counter which is reset on each rising and falling edge on the transmitting line.

According to various embodiments, a universal asynchronous receiver/transmitter (UART) module is disclosed. The module may include a first edge detector circuit coupled with a receiving line, wherein the first edge detector resets a first counter on a rising and a falling edge of the receiving line, and a second edge detector circuit coupled with a transmitting line, wherein the second edge detector resets a second counter on a rising and a falling edge of the transmitting line.

In some embodiments, the receiving line may be coupled with a buffer and a data recovery unit and wherein the first edge detector is coupled with an output of the data recovery unit. In alternative embodiments, a transmit register may be coupled with a buffer which is coupled with an external pin and the second edge detector.

In some embodiments, the first and second timers may be operable to time a timeout period associated with a communication protocol. In such embodiments, the communication protocol may include a digital multiplex protocol. In other such embodiments, the timeout period may be one second.

BRIEF DESCRIPTION OF THE DRAWINGS

DETAILED DESCRIPTION

Figure 1 illustrates an example known transmitter module of a known universal asynchronous receiver transmitter as implemented in known microcontrollers;

Figure 2 illustrates an example known receiver module of a known universal asynchronous receiver transmitter as implemented in known microcontrollers

Figure 3 illustrates an example receiving UART module for monitoring line transitions, in accordance with certain embodiments of the present disclosure; and

Figure 4 illustrates an example transmission UART module for monitoring line transitions, in accordance with certain embodiments of the present disclosure.

DETAILED DESCRIPTION

Certain known UARTs used by many microcontrollers may be implemented to handle various communication protocols that use a "timeout" period. For example, the digital multiplex ("DMX") protocol implements a timeout period that may be as long as one second. In some embodiments, in an effort to reduce software overhead involved in implementing the timeout period, an activity detector monitors transmissions on a data line to set or reset an onboard timer rather than implementing a software routine.

Figures 1 and 2 show a typical conventional universal asynchronous receiver/transmitter as implemented in many microcontrollers. Figure 1 shows a transmitter module and Figure 2 an associated receiver module. The UART module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The UART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers.

In some embodiments, the UART module may include the following additional features that may be useful in, for example, Local Interconnect Network (LIN) bus systems: Automatic detection and calibration of the baud rate; Wake-up on Break reception; 13-bit Break character transmit. During Sleep mode, all clocks to the UART may be suspended. Because of this, the Baud Rate Generator may be inactive and a proper character reception cannot be performed. The Auto-Wake-up feature may allow a coupled microcontroller to wake-up due to activity on a receive/data transmission line. This feature may be available only in Asynchronous mode. An Auto-Wake-up feature may enabled by setting a certain memory portion of UART. For example, the Auto-Wake-up feature may be enabled by setting the wake-up enable ("WUE") bit of a BAUDCON register. Once set, the normal receive sequence on RX/DT line may be disabled, and an Enhanced Universal Synchronous Asynchronous Receiver Transmitter ("EUSART") may remain in an idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event may consist of, for example, a high-to-low transition on RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.) The EUSART module may generate a receive interrupt flag (e.g., an RCIF interrupt) coincident with the wake-up event. The interrupt may be generated synchronously to the Q clocks in normal CPU operating modes, and asynchronously if the device is in Sleep mode. The interrupt condition may be cleared by reading another memory portion of the UART (e.g., the RCREG register). The WUE bit may be automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module may be in Idle mode waiting to receive the next character.

The UART may transmit and receive data using a standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a high-voltage output ("VOH") mark state which represents a '1' data bit, and a low-voltage output ("VOL") space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of one/(Baud Rate). An on-chip dedicated eight-bit/sixteen-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. The UART may transmit and receive the least

significant bit first. The UART's transmitter and receiver are functionally independent, but may share the same data format and baud rate. Parity may not be supported according to some embodiments, but may be implemented in software and stored as the ninth data bit. The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the UART receiver. The FIFO and RSR registers are not directly accessible by software according to some embodiments. Access to the received data may be given via the RCREG register.

Figures 3 and 4 illustrates example UART modules 300, 400, in accordance with certain embodiments of the present disclosure. In some embodiments, UART module 300, 400 may include amongst others the following additional modes of operation: Full-duplex asynchronous transmit and receive; Two-character input buffer; One-character output buffer; Programmable 8-bit or 9-bit character length; Address detection in 9-bit mode; Input buffer overrun error detection; Received character framing error detection; Sleep operation.

Many communication protocols such as the DMX protocol have timeout requirements. However the timeouts may be as long as one second. According to various embodiments, to reduce the number of counter bits, an activity detector monitors transitions on the line to set or reset an on board timer instead of a dedicated timer.

Figure 3 illustrates an example receiving UART module 300 for monitoring line transitions, in accordance with certain embodiments of the present disclosure. In some embodiments, UART 300 may include edge detector 306 coupled to baud rate generator 302 and receive line 304. Edge detector 306 may be operable to detect an edge of a data line of UART module 300. For example, as illustrated in Figure 3, edge detector 306 may be operable to detect an edge on RX line 304. An output of edge detector 306 may be coupled to an on-chip timer that may be reset every time activity on the data line (e.g., RX line 304) occurs. In some embodiments, edge detector 306 may also be coupled to an output of a data recovery unit 308. Data recovery unity 308 may be operable to receive an incoming data stream from RX

line 304. In such embodiments, UART 300 may also include a counter that is reset every time a falling or rising edge is present in the sampled data stream.

Figure 4 illustrates an example transmission UART module 400 for monitoring line transitions, in accordance with certain embodiments of the present disclosure. In some embodiments, UART module 400 may include edge detector 408 coupled to baud rate generator 402 and transmit line 404. Edge detector 408 may be operable to detect an edge on TX line 404. In some embodiments, UART module 400 may also include transmit register 406 coupled to a buffer that is coupled with an external pin and edge detector 408. In such embodiments, UART module 400 may include a second counter that reset on each rising and falling edge on the transmitting line.

There exists a need to provide a UART that allows for a timeout period in accordance with certain protocols in a simplified manner that does not rely on a dedicated timer or software.

CLAIMS

WHAT IS CLAIMED IS:

1. A universal asynchronous receiver/transmitter (UART) module comprising an edge detector coupled with a data line of the UART module, wherein the edge detector resets a counter on a rising and a falling edge.

2. The UART according to claim 1, wherein the edge detector comprises a first edge detector circuit coupled with a receiving line.

3. The UART according to claim 2, wherein an external receiving line is coupled with a buffer and a data recovery unit and wherein the first edge detector is coupled with an output of the data recovery unit.

4. The UART according to claim 2 or 3, further comprising a first counter which is reset on each rising and falling edge.

5. The UART according to one of the preceding claims, wherein the edge detector comprises a second edge detector circuit coupled with a transmitting line.

6. The UART according to claim 5, wherein a transmit register is coupled with a buffer which is coupled with an external pin and a second edge detector.

7. The UART according to claim 5 or 6, further comprising a second counter which is reset on each rising and falling edge on the transmitting line.

8. A microcontroller comprising:

a universal asynchronous receiver/transmitter (UART) module comprising an edge detector coupled with a data line of the UART module, wherein the edge detector resets a counter on a rising and a falling edge; wherein

the microcontroller does not include a dedicated timer for timing a timeout period associated with a communication protocol.

9. The microcontroller according to claim 8, wherein the edge detector comprises a first edge detector circuit coupled with a receiving line.

10. The microcontroller according to claim 9, wherein an external receiving line is coupled with a buffer and a data recovery unit and wherein the first edge detector is coupled with an output of the data recovery unit.

11. The microcontroller according to claim 9 or 10, further comprising a first counter which is reset on each rising and falling edge.

12. The microcontroller according to one of the preceding claims 8-11, wherein the edge detector comprises a second edge detector circuit coupled with a transmitting line.

13. The microcontroller according to claim 12, wherein a transmit register is coupled with a buffer which is coupled with an external pin and a second edge detector.

14. The microcontroller according to claim 12 or 13, further comprising a second counter which is reset on each rising and falling edge on the transmitting line.

15. A universal asynchronous receiver/transmitter (UART) module comprising:

a first edge detector circuit coupled with a receiving line, wherein the first edge detector resets a first counter on a rising and a falling edge of the receiving line; and

a second edge detector circuit coupled with a transmitting line, wherein the second edge detector resets a second counter on a rising and a falling edge of the transmitting line.

16. The UART according to claim 15, wherein the receiving line is coupled with a buffer and a data recovery unit and wherein the first edge detector is coupled with an output of the data recovery unit.

17. The UART according to claim 15 or 16, wherein a transmit register is coupled with a buffer which is coupled with an external pin and the second edge detector.

18. The UART according to one of the preceding claims 15-17, wherein the first and second timers are operable to time a timeout period associated with a communication protocol.

19. The UART according to claim 18, wherein the communication protocol comprises a digital multiplex protocol.

20. The UART according to claim 18 or 19, wherein the timeout period is one second.

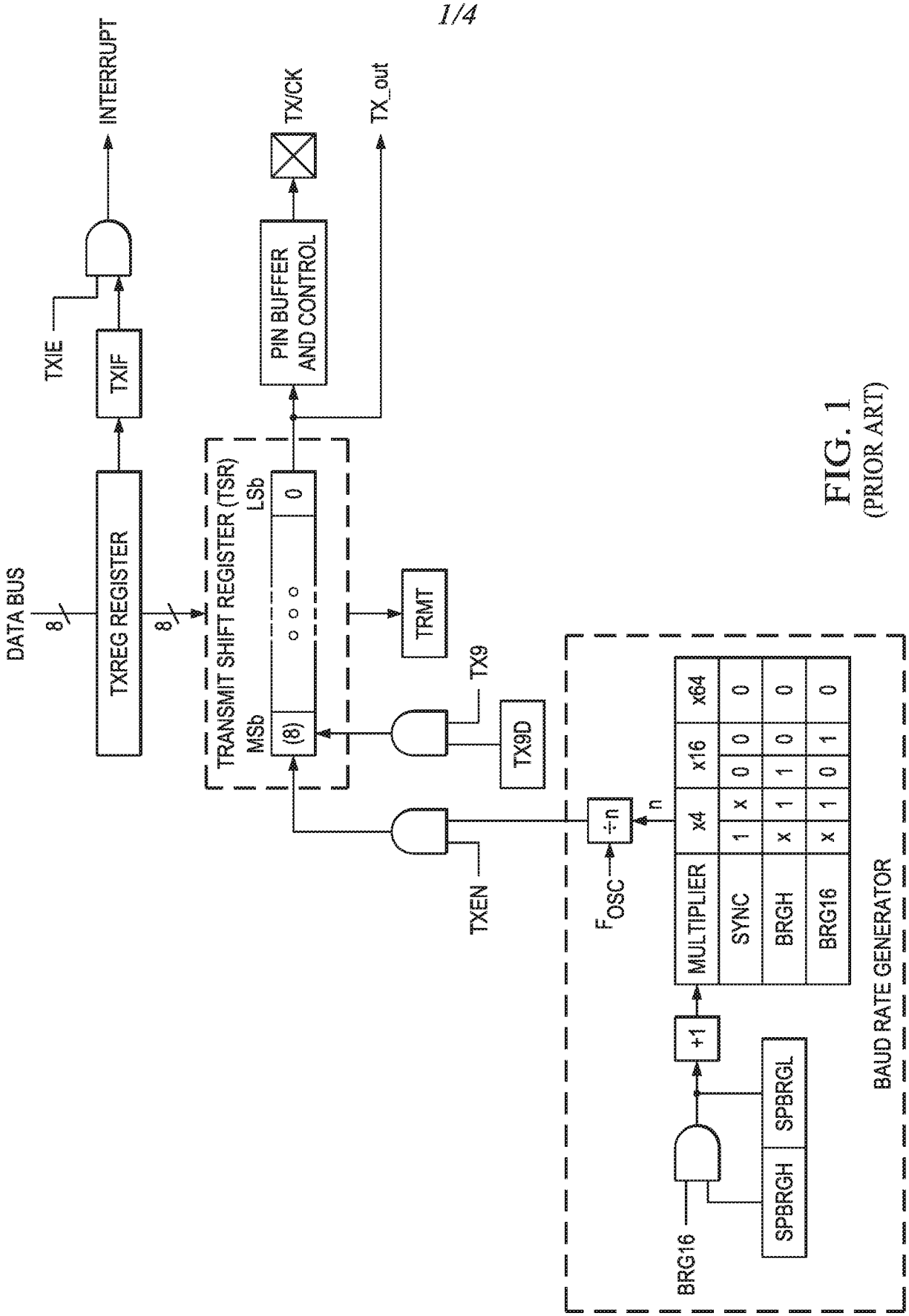

FIG. 1
(PRIOR ART)

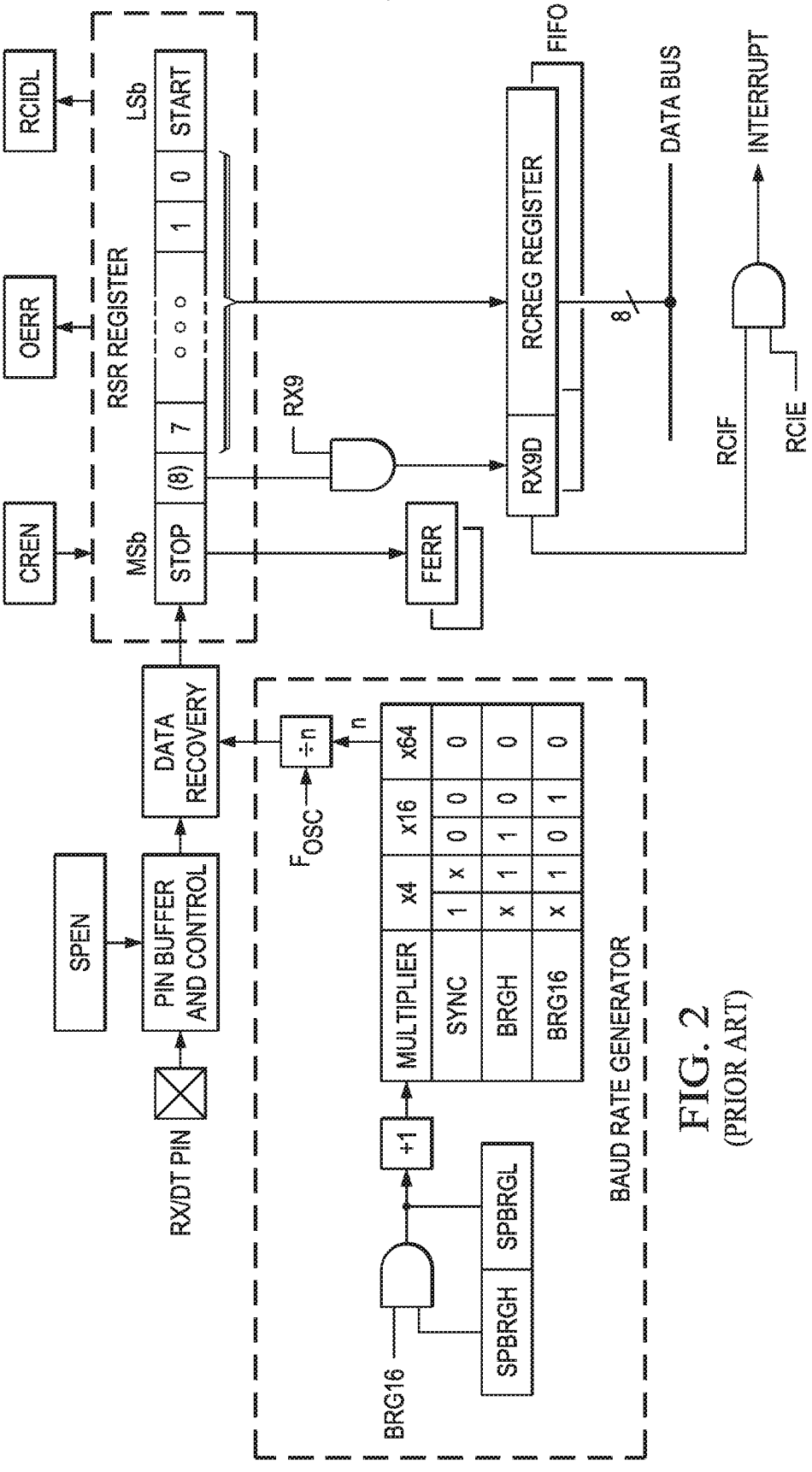

FIG. 2
(PRIOR ART)

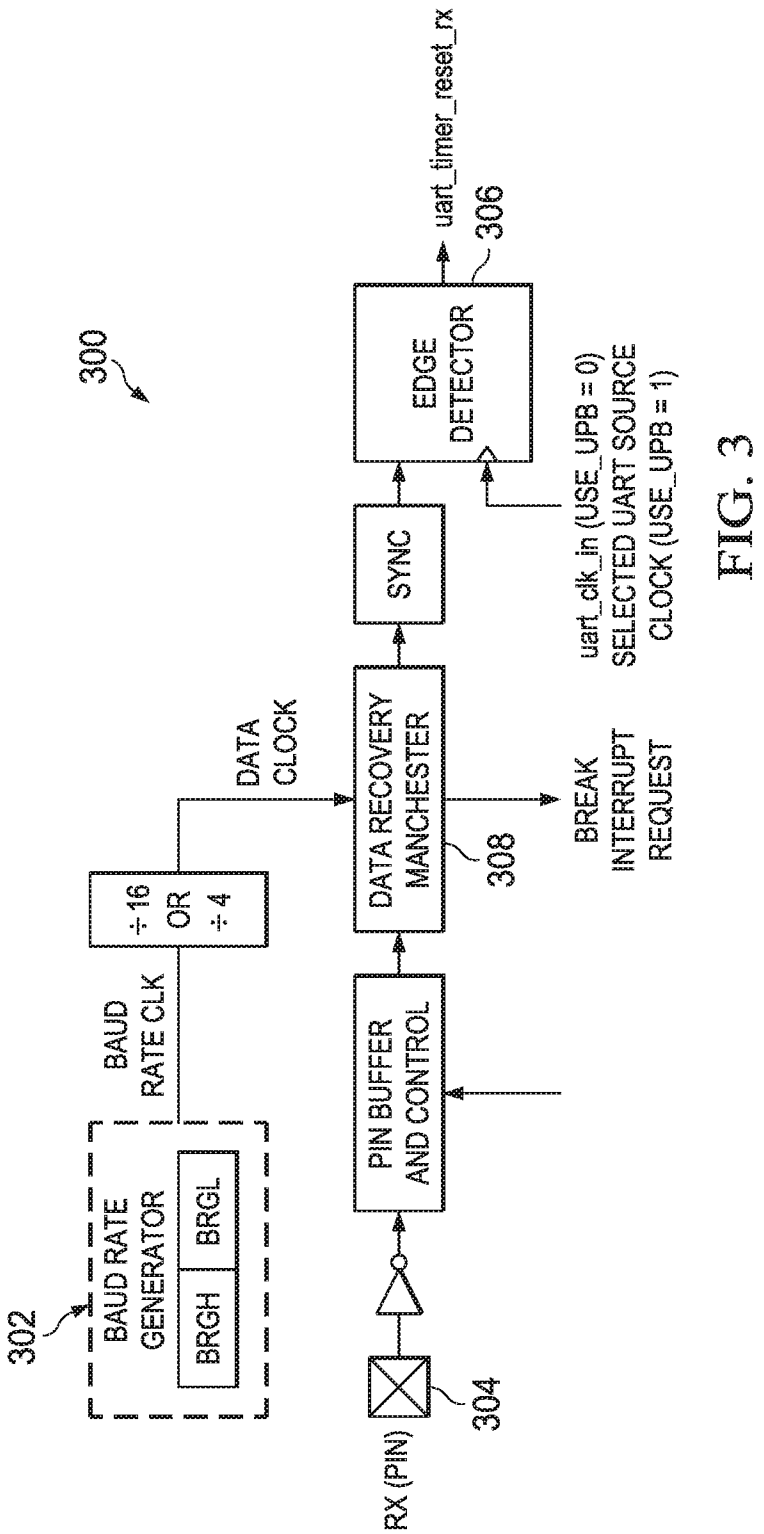
300
302
BAUD RATE GENERATOR
BRGH
BRGL
BAUD RATE CLK
÷16 OR ÷4
DATA CLOCK
RX (PIN)
304
PIN BUFFER AND CONTROL
DATA RECOVERY MANCHESTER
308
BREAK INTERRUPT REQUEST
SYNC
EDGE DETECTOR
306
uart_timer_reset_rx
uart_clk_in (USE_UPB = 0)
SELECTED UART SOURCE CLOCK (USE_UPB = 1)

FIG. 3

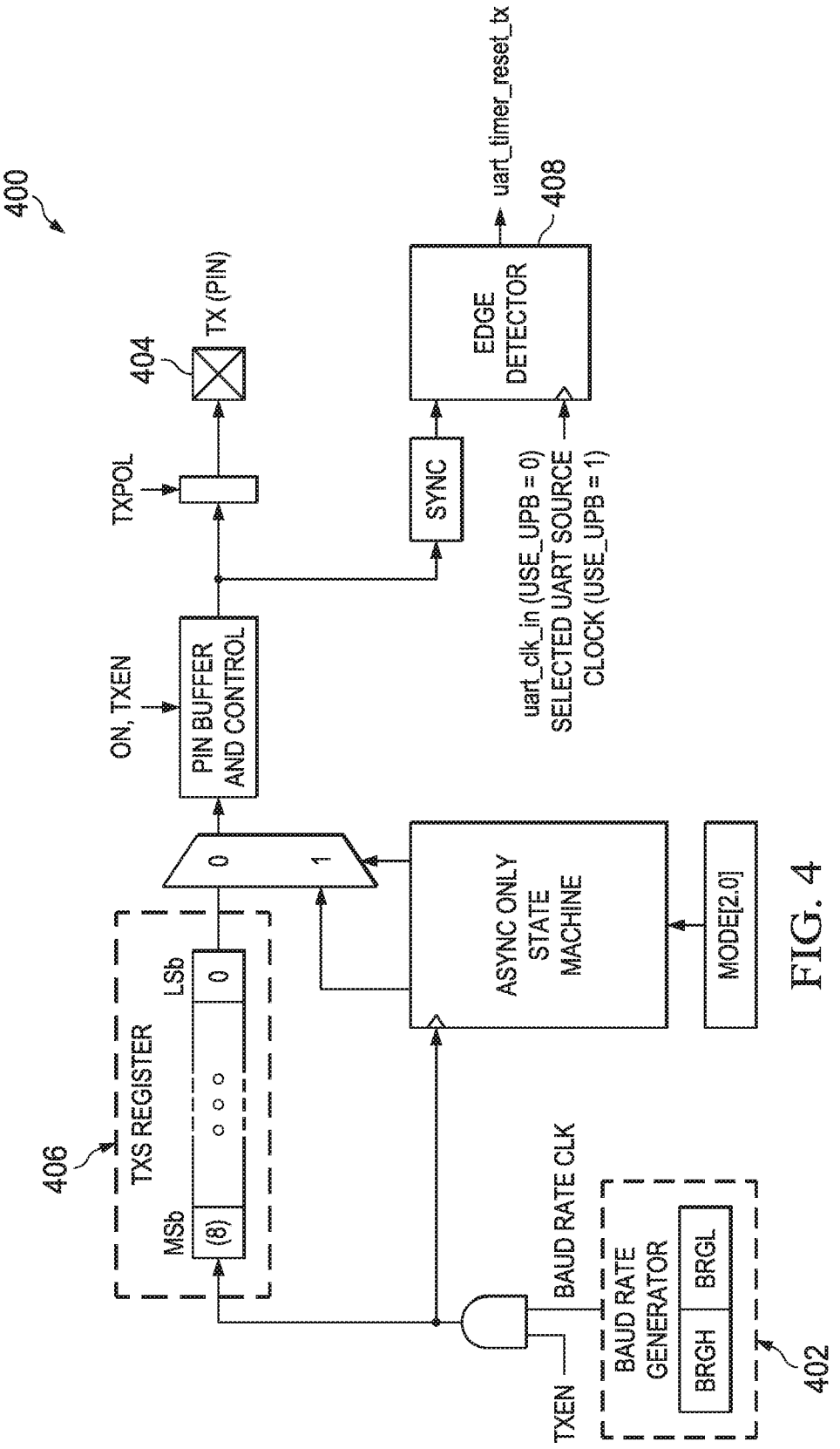
400
uart_timer_reset_tx
408
EDGE DETECTOR
404
TX (PIN)
TXPOL
SYNC
ON, TXEN
PIN BUFFER AND CONTROL
uart_clk_in (USE_UPB = 0)
SELECTED UART SOURCE CLOCK (USE_UPB = 1)
0
1
ASYNC ONLY STATE MACHINE
MODE[2.0]
406
TXS REGISTER
LSb
MSb
(8)
0
BAUD RATE CLK
TXEN
BAUD RATE GENERATOR
BRGH
BRGL
402

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/038614

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/42
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 97/31663 A1 (MINNESOTA MINING & MFG [US]) 4 September 1997 (1997-09-04) page 10, line 25 - line 32 page 15, line 27 - page 16, line 5	1-20
X	US 2004/233937 A1 (RUAT LUDOVIC [FR] ET AL) 25 November 2004 (2004-11-25) paragraph [0044] - paragraph [0051] paragraph [0074] - paragraph [0079]	1-20
X	US 2012/314738 A1 (KASHIMA HIDEKI [JP] ET AL) 13 December 2012 (2012-12-13) paragraph [0173] - paragraph [0178]	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 August 2016	01/09/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Rudolph, Stefan

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2016/038614

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9731663 A1	04-09-1997	DE 69616830 D1	13-12-2001
		DE 69616830 T2	20-06-2002
		EP 0883411 A1	16-12-1998
		JP 2000506750 A	06-06-2000
		US 5728154 A	17-03-1998
		US 6106551 A	22-08-2000
		WO 9731663 A1	04-09-1997
US 2004233937 A1	25-11-2004	DE 60202697 D1	24-02-2005
		DE 60202697 T2	06-04-2006
		EP 1436713 A2	14-07-2004
		FR 2830954 A1	18-04-2003
		US 2004233937 A1	25-11-2004
		WO 03034246 A2	24-04-2003
US 2012314738 A1	13-12-2012	CN 102820900 A	12-12-2012
		DE 102012209636 A1	13-12-2012
		JP 5541234 B2	09-07-2014
		JP 2012257035 A	27-12-2012
		KR 20120136308 A	18-12-2012
		US 2012314738 A1	13-12-2012