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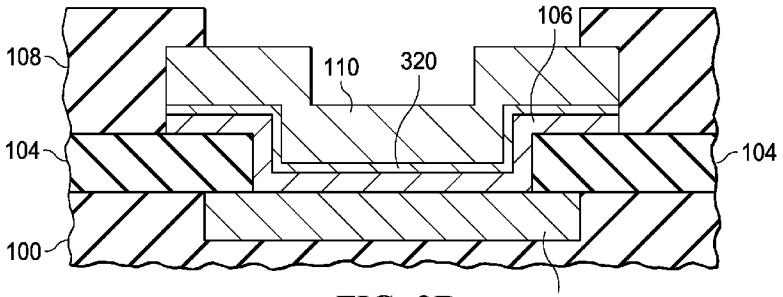


FIG. 3B

(57) Abstract: In described examples, an integrated circuit includes an underlying metal geometry (102), a dielectric layer (104) on the underlying metal geometry (102), a contact opening through the dielectric layer (104), an overlying metal geometry (110) wherein a portion of the overlying metal geometry (110) fills a portion of the contact opening, and an oxidation resistant barrier layer (320) disposed between the underlying metal geometry (102) and overlying metal geometry (110). The oxidation resistant barrier layer (320) is formed of TaN or TiN with a nitrogen content of at least 20 atomic % and a thickness of at least 5 nm.

WO 2017/106828 A1

OXIDATION RESISTANT BARRIER METAL PROCESS FOR SEMICONDUCTOR DEVICES

[0001] This relates generally to integrated circuits, and more particularly to formation of contacts with stable resistance in integrated circuits.

BACKGROUND

[0002] During processing of an integrated circuit, openings typically referred to as contacts or vias are made through dielectric overlying metal interconnect leads to form electrical contact to the leads. The metal interconnect that is exposed in the these contact or via openings may form a layer of metal oxide on the surface that increases the electrical contact resistance and also may cause significant variation in the electrical contact resistance in these openings across an integrated circuit chip or wafer.

[0003] A typical example of forming an aluminum bond pad 110 on a top layer of copper interconnect 102 is illustrated in FIG. 1B. The underlying copper interconnect layer 102 is formed in a dielectric layer 100 using either a single or a dual damascene process. An opening is formed in dielectric layer 104 overlying the copper interconnect layer to form electrical connection to an overlying aluminum bondpad 110. An interdiffusion barrier layer 106 of a material such as Ta or TaN is disposed between the underlying copper interconnect and the overlying aluminum bondpad 110 to prevent interdiffusion of copper and aluminum.

[0004] A typical example of forming an upper level of aluminum interconnect 210 on a lower layer of copper interconnect 202 is illustrated in FIG. 2B. The underlying copper interconnect layer 202 is formed in a dielectric layer 200 using either a single or a dual damascene process. Contact or via openings are formed in dielectric layer 204 overlying the copper interconnect layer 202 to form electrical connection between the interconnect layers 202 and 210. An interdiffusion barrier layer 206 of a material such as Ta or TaN is disposed between the underlying copper interconnect 202 and the overlying aluminum interconnect 210 to prevent interdiffusion of copper and aluminum.

[0005] As illustrated in TABLE 1, the TaxOy (or TaxNyOz) layer that forms on the TaN interdiffusion barrier layer 106 (FIG. 1A) and layer 206 (FIG. 2A) causes the contact resistance to increase by 6x after 12 hours of exposure to air and by 10x after 24 hours of exposure to air. Also, the increase in electrical contact resistance caused by the TaxOy layer typically varies

significantly from contact to contact. The magnitude of the increase in electrical resistance depends on both the test structure and measurement technique used. TABLE 1 was generated from 4-point probe measurements to maximize sensitivity to interface resistance and is intended solely to provide a baseline reference for quantifying the improvement afforded by an example embodiment.

TABLE 1

TaN in via exposure to air	Resistance Increase
12 hours	6x
24 hours	10x

[0006] The metal oxide layer may be removed by various means such as sputter etching before deposition of the aluminum bondpad metal 110 or the upper aluminum interconnect metal 210, but this often causes other problems. For example if an argon sputter etch is used to remove the TaxOy layer that forms on the TaN barrier layer 106 and 206 before AlCu 110 and 210 deposition, the sputter etch process introduces particles which reduces yield. Also, the presputter etch alters the morphology of the deposited AlCu, 110 or 210, resulting in a decrease in electromigration resistance.

SUMMARY

[0007] In described examples, an integrated circuit includes an underlying metal geometry, a dielectric layer on the underlying metal geometry, a contact opening through the dielectric layer, an overlying metal geometry wherein a portion of the overlying metal geometry fills a portion of the contact opening, and an oxidation resistant barrier layer disposed between the underlying metal geometry and overlying metal geometry. The oxidation resistant barrier layer is formed of TaN or TiN with a nitrogen content of at least 20 atomic % and a thickness of at least 5 nm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIGS. 1A and 1B (prior art) are cross-sections of a lower copper interconnect to upper aluminum bondpad metal contact with an interdiffusion barrier in the bottom of the contact.

[0009] FIGS. 2A and 2B (prior art) are cross-sections of a lower copper interconnect to upper aluminum interconnect metal contact with an interdiffusion barrier in the bottom of the contact.

[0010] FIGS. 3A and 3B are cross-sections of a lower copper interconnect to upper aluminum

bondpad contact with an interdiffusion barrier plus an oxidation resistant barrier layer formed according to embodiments.

[0011] FIGS. 4A and 4B are cross-sections of a lower copper interconnect to upper aluminum interconnect contact with an interdiffusion barrier plus an oxidation resistant barrier layer formed according to embodiments.

[0012] FIGS. 5A and 5B are cross-sections of a lower metal to upper metal contact with an oxidation resistant barrier layer formed according to embodiments wherein the oxidation resistant barrier layer covers the sidewalls and the bottom of the contact.

[0013] FIGS. 6A and 6B are cross-sections of a lower metal to upper metal contact with an oxidation resistant barrier layer formed according to principles of example embodiments, wherein the oxidation resistant barrier layer covers the lower metal geometry.

[0014] FIG. 7 is a flow diagram describing the primary manufacturing steps to form the contact structures depicted in FIGS. 2A, 2B, 3A, 3B, 4A, 4B, 5A and 5B.

[0015] FIG. 8 is a flow diagram describing the primary manufacturing steps to form the contact structures depicted in FIGS. 6A and 6B.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0016] The figures are not necessarily drawn to scale. Some illustrated ordering of acts or events may occur in different orders and/or concurrently with other acts or events. Furthermore, not all illustrated acts or events are required to implement a methodology in accordance with example embodiments.

[0017] An aluminum copper (AlCu) bondpad 110 to underlying copper interconnect 102 structure with an interdiffusion barrier layer 106 and with an embodiment oxidation resistant barrier layer 320 is illustrated in FIG. 3B. A copper interconnect geometry 102 is formed in a dielectric layer 100 using a damascene process. A dielectric layer 104 with a contact opening to the copper interconnect geometry 102 overlies dielectric layer 100 and copper interconnect geometry 102. A bondpad stack including an interdiffusion barrier layer 106, an embodiment oxidation resistant barrier surface (ORBS) layer 320 and aluminum or aluminum copper alloy 110 overlies the dielectric layer 104 and contacts the underlying copper interconnect geometry 102 through the contact opening in dielectric layer 104. The interdiffusion barrier layer 106 may be a material such as TaN or TiN with a thickness between about 60 nm and 90 nm, and a nitrogen content between about 0 and 12 atomic percent. The ORBS layer 320 may be nitrogen

rich tantalum nitride with nitrogen content in the range of about 20 to 35 atomic percent and a thickness in the range of about 5 nm to 15 nm. The ORBS layer 320 may also be a nitrogen rich titanium nitride with a thickness slightly higher than the nitrogen rich tantalum nitride oxidation resistant layer.

[0018] An aluminum copper (AlCu) interconnect 210 to underlying copper interconnect 202 structure with an interdiffusion barrier layer 206 and with an embodiment oxidation resistant barrier layer 420 is illustrated in FIG. 4B. A copper interconnect geometry 202 is formed in a dielectric layer 200 using a damascene process. A dielectric layer 204 with contact or via openings to the copper interconnect geometries 202 overlies dielectric layer 200 and copper interconnect geometries 202. A upper aluminum interconnect stack including an interdiffusion barrier layer 206, an embodiment oxidation resistant barrier surface (ORBS) layer 420 and aluminum or aluminum copper alloy 210 overlies the dielectric layer 204 and contacts the underlying copper interconnect geometries 202 through the contact or via openings in dielectric layer 204. The interdiffusion barrier layer 206 may be a material such as TaN or TiN with a thickness between about 60 nm and 90 nm, and a nitrogen content between about 0 and 12 atomic percent. The ORBS layer 420 may be nitrogen rich tantalum nitride with nitrogen content in the range of about 20 to 35 atomic percent and a thickness in the range of about 5 nm to 15 nm. The ORBS layer 420 may also be a nitrogen rich titanium nitride with a thickness slightly higher than the nitrogen rich tantalum nitride oxidation resistant layer.

[0019] The ORBS layers 320 and 420 enable the IC to be exposed to air for 24 hours or longer before deposition of the bondpad metal 110 or the upper aluminum interconnect metal 210 with an increase in contact resistance of less than 2x. Also, with the ORBS layers 320 and 420, the resistance of many contacts or vias across the integrated circuit (IC) chip and across the IC wafer remains tightly distributed.

[0020] A copper interconnect interdiffusion barrier layer with an embodiment oxidation resistant barrier layer structure is used for illustration. In this structure, an interdiffusion barrier layer 106 or 206 is required to prevent interdiffusion of copper and aluminum. If the underlying interconnect layer is another material such as TiW or W which does not interdiffuse with AlCu, the barrier layer 106 or 206 may be omitted and the ORBS layer 320 or 420 may be deposited directly on the underlying interconnect.

[0021] Overlying aluminum or aluminum copper is used in FIGS. 3 and 4 for illustration.

Other overlying metals such as nickel palladium alloy may be used for the overlying bondpad 110 or overlying interconnect 210 material instead of aluminum or aluminum copper.

[0022] When the underlying metal layer is formed by deposition, pattern, and etch instead of by a damascene process, two options for the embodiment ORBS layer are available. As with an underlying metal geometry formed using a damascene process, a contact opening may be formed in a dielectric layer that overlies the underlying metal layer and the ORBS layer may be deposited on the dielectric layer and into the contact opening as described above. Alternatively, for metal geometries formed by deposition, pattern, and etch the ORBS layer may be deposited on the underlying metal layer (or on a barrier layer on the underlying metal layer) before patterning and etching to form the underlying metal layer geometry. In this alternative structure a contact opening is etched through an overlying dielectric layer stopping on the ORBS layer. This contact opening with the ORBS layer in the bottom may be exposed to air for an extended time (up to 24 hours) with little (less than 2x) increase in contact resistance.

[0023] A structure in which the underlying metal layer 510 is deposited, patterned and etched and the embodiment oxidation resistant barrier layer 520 is deposited into a contact opening in a dielectric 104 overlying the underlying metal layer 510 is illustrated in FIG. 5B. The underlying metal layer 510 to which contact is made may be a metal resistor or an electrical fuse (efuse) or a top plate of a metal-to-metal capacitor for example.

[0024] The oxidation resistant barrier layer 520 is deposited into openings in the dielectric 104 overlying the metal layer 510 to form electrical contact to underlying metal layer 510, as shown in FIG. 5A. Top metal 110 which overlies the oxidation resistant barrier 520 may be used to form a bondpad or may be used as an upper layer of interconnect. In this example, a metal which does not require an interdiffusion barrier layer is used for illustration so the oxidation resistant barrier 520 may be deposited directly onto the underlying metal layer 510.

[0025] The ORBS layer (which may be nitrogen rich TaN as described hereinabove) provides low and consistent contact resistance across a wafer and also increases the span of time (process window) that the wafer may be exposed to air between oxidation resistant barrier layer 520 deposition and top metal 110 deposition thus improving manufacturability.

[0026] Another structure in which an embodiment oxidation resistant barrier layer 620 is deposited on the underlying metal layer 610 before patterning and etching to form the underlying metal layer 610 geometry is shown in FIG. 6B. For example, the lower metal layer 610 may be a

top capacitor plate or a metal resistor. An optional interdiffusion barrier layer may be deposited on the underlying metal layer 610 before deposition of the ORBS layer 620 if needed.

[0027] In this structure, contact or via openings are etched through an overlying dielectric layer 104 and stop on the ORBS layer 620 which is on top of the underlying metal layer 610, as shown in FIG. 6A. The top metal 110 is deposited directly onto the ORBS layer 620 that is exposed in the bottom of the contact or via openings. The ORBS layer 620 may be exposed to air for up to 24 hours with less than a 2x increase in resistance. Also, the distribution of contact or via resistance across contacts across an IC chip or across an IC wafer remains tightly distributed.

[0028] FIG. 7 is a process flow diagram for a method for forming contacts using an embodiment ORBS layer such as those shown in FIGS. 3A, 3B, 4A, 4B, and 5A and 5B.

[0029] In step 700, a contact pattern is formed on a dielectric layer 104 overlying the underlying metal 102 (FIG. 3A) or 202 (FIG. 4A) or 510 (FIG. 5A) and openings are etched through the dielectric layer 104 (FIGS. 3A, 5A) or 204 (FIG. 4A) stopping on the underlying metal layer 102/202/510.

[0030] In step 702, an optional interdiffusion barrier layer 106 (FIG. 3A) or 206 (FIG. 4B) may be deposited over the dielectric layer 104 or 204 and into the contact opening. A degas step (such as a bake at a temperature in the range of 250°C to 400 °C under reduced pressure) and/or a presputter clean step (such as an argon presputter clean) or a reactive preclean (such as a high bias preclean with hydrogen plus argon or hydrogen plus helium) may be performed before the interdiffusion barrier layer 106 (FIG. 3A) or 206 (FIG. 4A) deposition. FIGS. 3A and 4A illustrate a process flow that incorporates the optional interdiffusion barrier layer 106 or 206. FIG. 5A illustrates a process flow that does not incorporate an interdiffusion barrier layer. The interdiffusion barrier layer may be TaN or TiN with a thickness between about 60 nm and 90 nm and a nitrogen content between about 0 atomic % and 12 atomic %.

[0031] In step 704, the embodiment oxidation resistance barrier surface (ORBS) layer, 320 (FIG. 3A) or 420 (FIG. 4A) is deposited. The ORBS layer, 320 (FIG. 3A) or 420 (FIG. 4A), may be a high nitrogen content TaN layer with a thickness between about 5 nm and 15 nm and a nitrogen content of about 20 atomic % to 35 atomic %. One tool that the ORBS film may be deposited in is an EnCoRe1 chamber on the Applied Endura platform. In this tool, the ORBS layer may be deposited at room temperature with a pressure between about 2.5 and 5 torr, a

power in the range of 15 to 30 KW, a bias in the range of 250 W to 500 W and a flow rate of nitrogen in the range of about 115 to 125 sccm. The deposition time may vary depending upon the deposition conditions. A time sufficient to deposit a TaN film with a thickness in the range of 5 nm to 15 nm is used.

[0032] Other deposition tools with different deposition conditions may be used to produce an equivalent ORBS TaN film with a thickness in the range of 5 nm to 15 nm and a nitrogen content in the range of 20 atomic % to 35 atomic %.

[0033] In step 706, the ORBS film may be exposed to air for an extended length of time if desired. At least a short exposure to air may be desirable. The air exposure may affect the grain structure and electromigration resistance of subsequently deposited interconnect or bondpad metal. The ORBS film enables the IC wafer to be exposed to air for an extended period of time (24 hours) with less than a 2x increase in resistance. Also, the distribution of resistance of all the contacts across an IC chip and across an IC wafer remains tightly distributed.

[0034] In step 708, an upper metal used for either interconnect or bondpad formation is deposited on the oxidation resistant barrier surface (ORBS) layer.

[0035] In step 710, the upper metal used for either interconnect or bondpad formation is patterned.

[0036] In step 712, the upper metal used for either interconnect or bondpad formation is etched and the ORBS material is etched.

[0037] In step 714, the interdiffusion barrier layer is etched if it exists.

[0038] FIG. 8 is a process flow diagram for a method for forming contacts using an ORBS layer 620 (FIG. 6A) that is deposited on an underlying metal layer 610 before patterning and etching to form the underlying metal geometry 610 is shown in FIGS. 6A and 6B.

[0039] In step 800, the underlying metal layer 610 is deposited.

[0040] In step 802, an optional interdiffusion barrier layer is deposited to prevent interdiffusion of the underlying metal layer 610 with the overlying metal layer 110 if it is needed. If it is not needed, the embodiment ORBS layer 620 may be deposited directly on the underlying metal layer 610. If the underlying metal layer has been exposed to air, a degas step may be used. The degas step (such as a bake at 250 C to 400 C under reduced pressure) and/or a presputter clean step (such as an argon presputter clean) or a reactive preclean (such as a high bias preclean with hydrogen plus argon or hydrogen plus helium) may be performed before the ORBS layer 620

deposition.

[0041] In step 804, the ORBS layer 620 is deposited on the underlying metal layer 610. The ORBS layer 620 may be a high nitrogen content TaN layer with a thickness between about 5 nm and 15 nm and a nitrogen content of about 20 atomic % to 35 atomic %. One tool that the ORBS film may be deposited in is an EnCoRe1 chamber on the Applied Endura platform. In this tool The ORBS layer may be deposited at room temperature with a pressure between about 2.5 to 5 torr, a power in the range of 15 to 30 KW, a bias in the range of 250 W to 500 W and a flow rate of nitrogen in the range of about 115 to 125 sccm. The deposition time may vary depending upon the deposition conditions. A time sufficient to deposit a TaN film with a thickness in the range of 5 nm to 15 nm is used.

[0042] Other deposition tools with different deposition conditions may be used to produce an equivalent ORBS TaN film with a thickness in the range of 5 nm to 15 nm and a nitrogen content in the range of 20 atomic % to 35 atomic %.

[0043] In step 806, the underlying metal is patterned and etched to form the underlying interconnect geometry 610. The ORBS layer 620 is etched first. The optional interdiffusion barrier layer is etched next if it exists. The underlying metal 610 is then etched.

[0044] In step 808, a dielectric layer 104 such as silicon dioxide or polyimide is deposited over the underlying dielectric 100 and metal layer 610.

[0045] In step 810, a pattern is formed on the dielectric layer 104 with openings over the underlying metal geometry 610. The dielectric material is etched out of the openings stopping on the ORBS layer 620. The ORBS layer 620 enables the IC wafers to be exposed to air for an extended period of time (24 hours) with little (less than 2x) increase in resistance. Also, the ORBS layer 620 provides for a tight distribution of contact resistance across the IC chip and across the IC wafer.

[0046] In step 812, an upper metal used for either interconnect or bondpad formation is deposited on the dielectric layer 104 and on the oxidation resistant (ORBS) barrier layer in the bottom of the contact openings.

[0047] In step 814, the upper metal used for either interconnect or bondpad formation is patterned and etched to form the upper interconnect metal geometries 110.

[0048] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

an underlying metal geometry;

a dielectric layer on the underlying metal geometry;

a contact opening through the dielectric layer wherein the contact opening stops on the underlying metal geometry;

an overlying metal geometry wherein a portion of the overlying metal geometry fills a portion of the contact opening; and

an oxidation resistant barrier layer wherein the oxidation resistant barrier layer is disposed between the underlying metal geometry and overlying metal geometry and wherein the oxidation resistant barrier layer is formed of TaN or TiN with a nitrogen content of at least 20 atomic % and a thickness of at least 5 nm.

2. The integrated circuit of claim 1, wherein the oxidation resistant barrier layer extends under the contact opening.

3. The integrated circuit of claim 1, wherein the oxidation resistant barrier layer extends along the sides and bottom of the contact opening.

4. The integrated circuit of claim 1 further comprising an interdiffusion barrier layer disposed between the underlying metal geometry and the oxidation resistant barrier layer.

5. The integrated circuit of claim 4 wherein the interdiffusion barrier layer is TaN or TiN with a thickness between 60 nm and 90 nm and a nitrogen content between 0 and 12 atomic percent.

6. The integrated circuit of claim 1 wherein the oxidation resistant barrier layer is formed of TaN with a thickness between 5 and 15 nm and with a nitrogen content between 20 and 35 atomic percent.

7. The integrated circuit of claim 1 wherein the oxidation resistant barrier layer is formed of TaN with a thickness of about 10 nm and a nitrogen content of about 28 atomic percent.

8. A process of forming an integrated circuit, the process comprising:

forming an underlying metal geometry on a first dielectric;

depositing a second dielectric layer over the underlying metal geometry and over the first dielectric;

forming a contact photo resist pattern on the second dielectric layer with a contact opening over the underlying metal geometry;

etching a contact opening through the second dielectric layer and stopping on the underlying metal geometry;

depositing an overlying metal layer in the contact opening;

forming an oxidation resistant barrier layer between the underlying metal geometry and the overlying metal layer wherein the oxidation resistant barrier layer is TaN or TiN with a nitrogen content of at least 20 atomic percent and a thickness of at least 5 nm;

forming a photo resist pattern on the overlying metal layer with an overlying metal geometry covering the contact opening; and

etching the overlying metal layer to form the overlying metal geometry.

9. The process of claim 8, wherein forming the oxidation resistant barrier layer comprises depositing an oxidation resistant barrier layer on the second dielectric layer and on the sides and bottom of the contact opening.

10. The process of claim 9, wherein the oxidation resistant barrier layer is deposited on the underlying metal geometry before depositing the second dielectric layer.

11. The process of claim 8, further comprising: exposing the oxidation resistant barrier layer to air for a period of time up to 24 hours before the step of depositing the overlying metal layer.

12. The process of claim 8, further comprising: depositing a interdiffusion barrier layer before the step of depositing the oxidation resistant barrier layer.

13. The process of claim 12, wherein the interdiffusion barrier layer is a TaN or TiN layer with a thickness between 60 nm and 90 nm and a nitrogen content in the range of 0 to 12 atomic percent.

14. The process of claim 8, wherein the oxidation resistance barrier layer is a TaN layer with a thickness in the range of 5 nm to 15 nm and a nitrogen content in the range of 20 to 35 atomic percent.

15. The process of claim 8, wherein the oxidation resistant barrier layer is TaN with a thickness in the range of 5 nm to 15 nm deposited at room temperature with a pressure between about 2.5 to 5 torr, a power in the range of 15 to 30 KW, a bias in the range of 250 W to 500 W, and a flow rate of nitrogen in the range of about 115 to 125 sccm.

16. A process of forming an integrated circuit, the process comprising:

depositing an underlying metal layer on a first dielectric layer;

depositing an oxidation resistant barrier layer on the underlying metal layer wherein the oxidation resistant barrier layer is TaN or TiN with a nitrogen content of at least 20 atomic percent and a thickness of at least 5 nm.

forming a photo resist pattern on the oxidation resistant barrier layer;

etching the oxidation resistant barrier layer and etching the underlying metal to form an underlying metal geometry;

depositing a second dielectric layer over the underlying metal geometry and over the first dielectric layer;

forming a contact photo resist pattern on the second dielectric layer with a contact opening over the underlying metal geometry;

etching a contact opening through the second dielectric layer and stopping on the oxidation resistant barrier layer on the underlying metal geometry;

depositing an overlying metal layer wherein the overlying metal layer fills the contact opening;

forming a photo resist pattern on the overlying metal layer; and

etching the overlying metal layer to form an overlying metal geometry which covers the contact opening.

17. The process of claim 16, wherein the oxidation resistant barrier layer is TaN with a thickness in the range of 5 nm to 15 nm deposited at room temperature with a pressure between about 2.5 to 5 torr, a power in the range of 15 to 30 KW, a bias in the range of 250 W to 500 W, and a flow rate of nitrogen in the range of about 115 to 125 sccm.

18. The process of claim 16, further comprising: depositing a interdiffusion barrier layer before the step of depositing the oxidation resistant barrier layer.

19. The process of claim 18, wherein the interdiffusion barrier layer is a TaN or TiN layer with a thickness between 60 nm and 90 nm and a nitrogen content in the range of 0 to 12 atomic percent.

20. The process of claim 16, wherein the oxidation resistance barrier layer is a TaN layer with a thickness in the range of 5 nm to 15 nm and a nitrogen content in the range of 20 to 35 atomic percent.

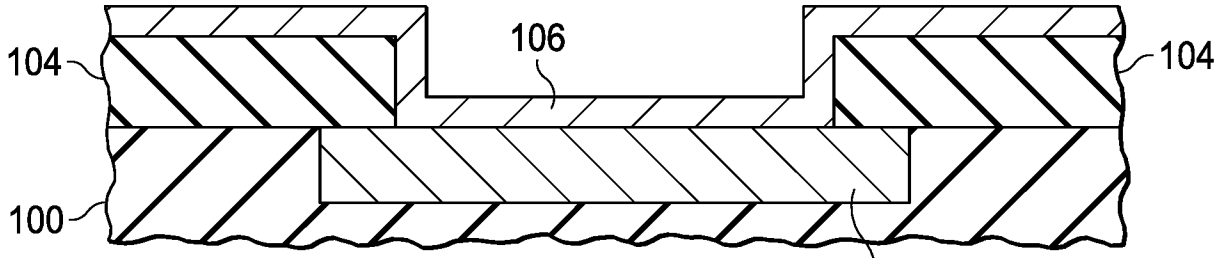


FIG. 1A
(PRIOR ART)

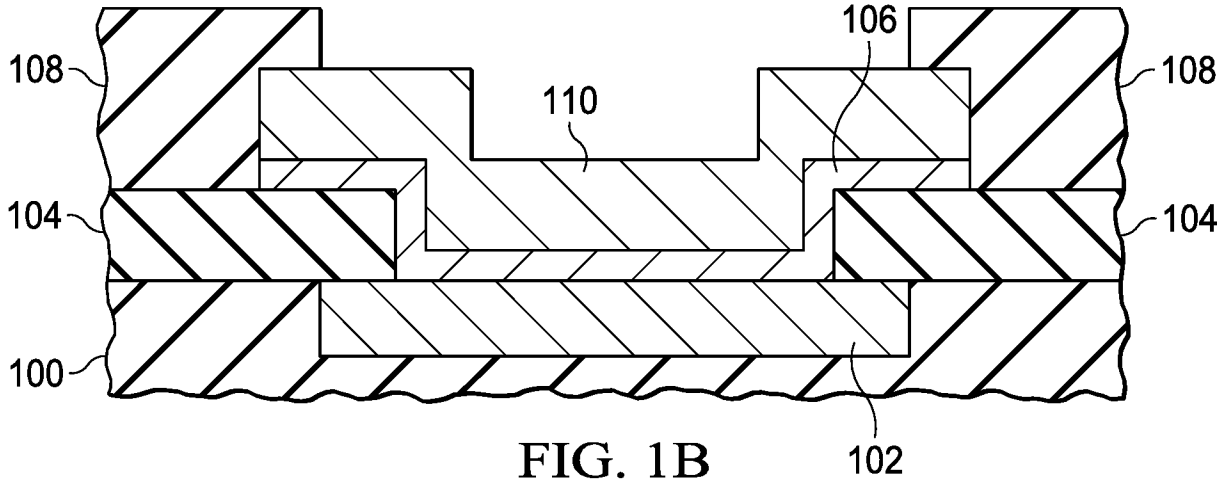


FIG. 1B
(PRIOR ART)

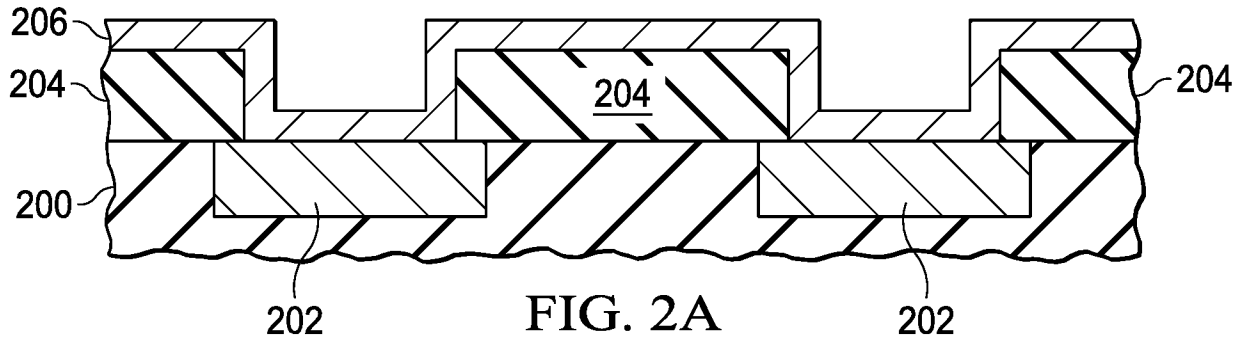


FIG. 2A
(PRIOR ART)

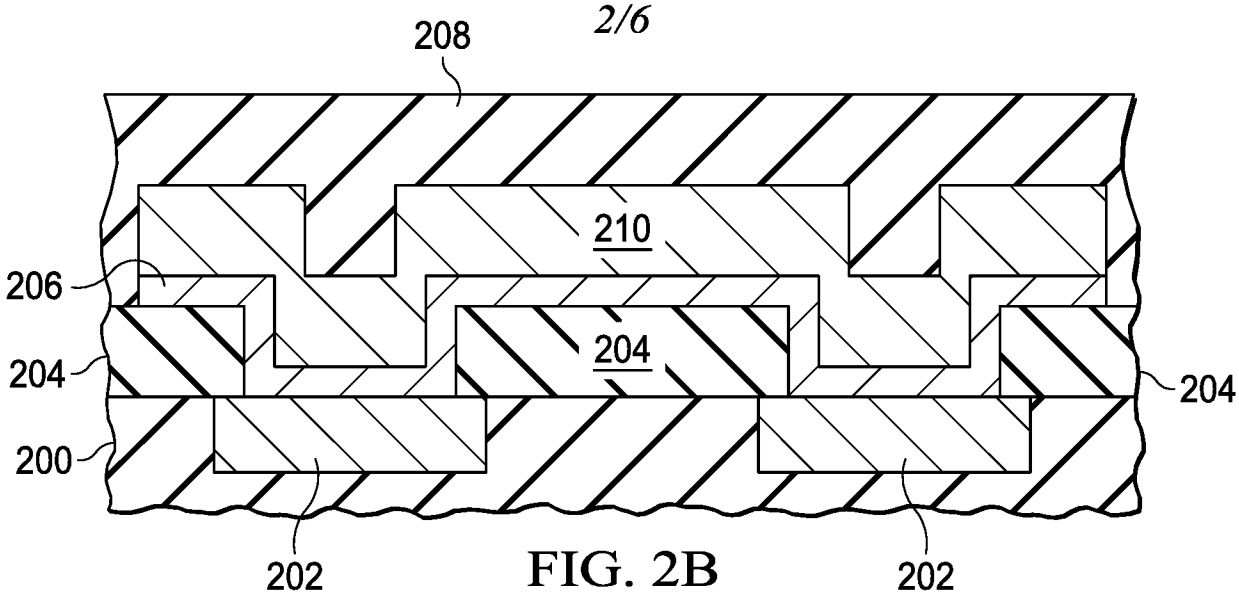


FIG. 2B
(PRIOR ART)

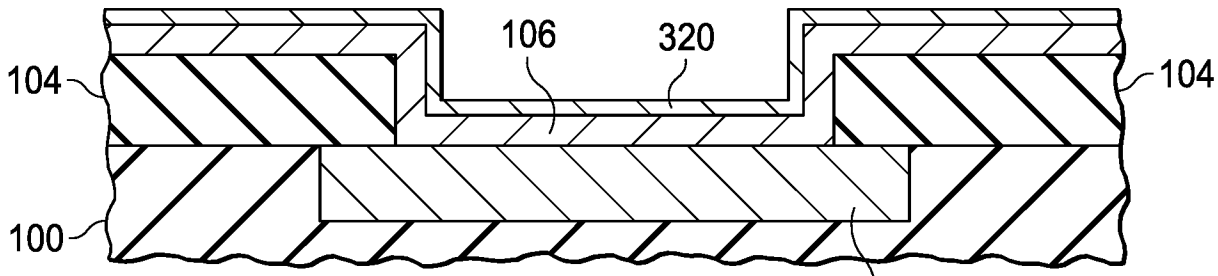


FIG. 3A

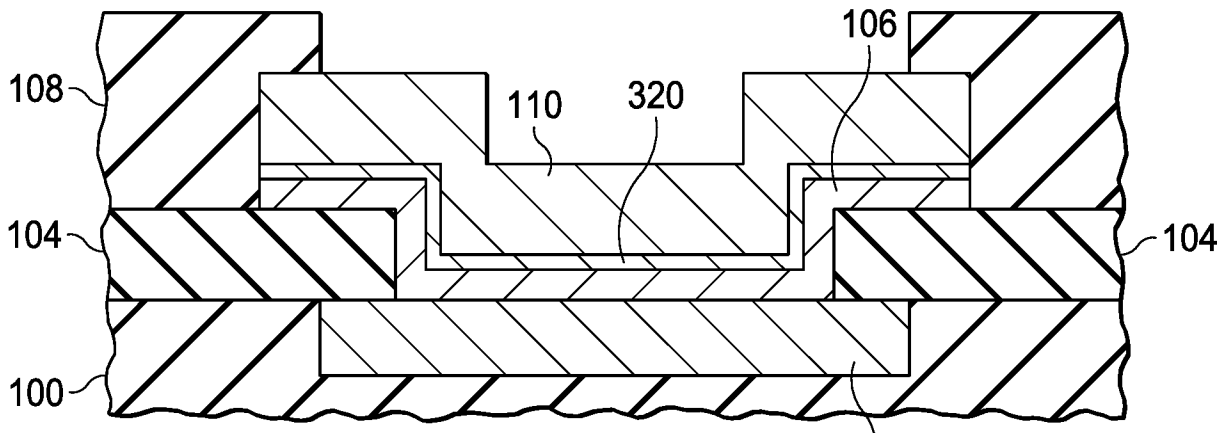


FIG. 3B

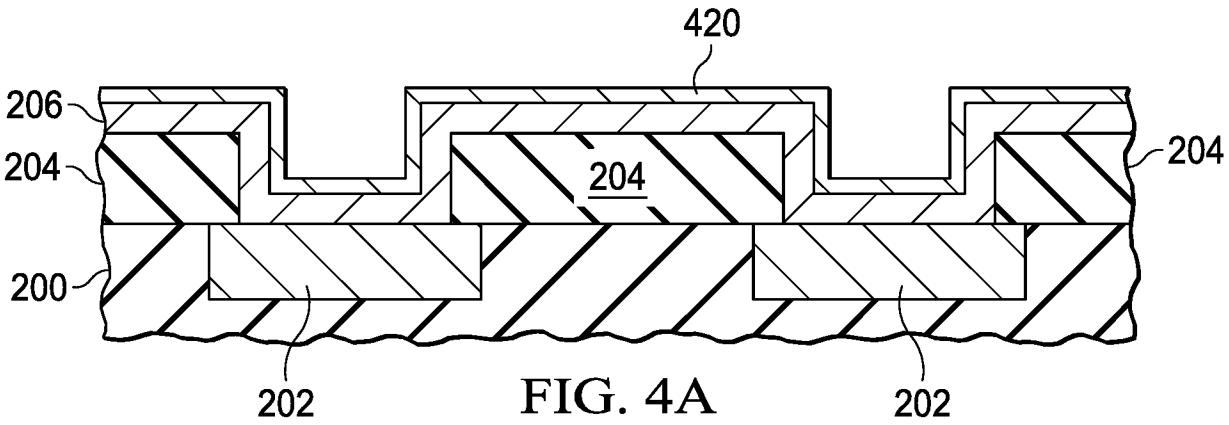
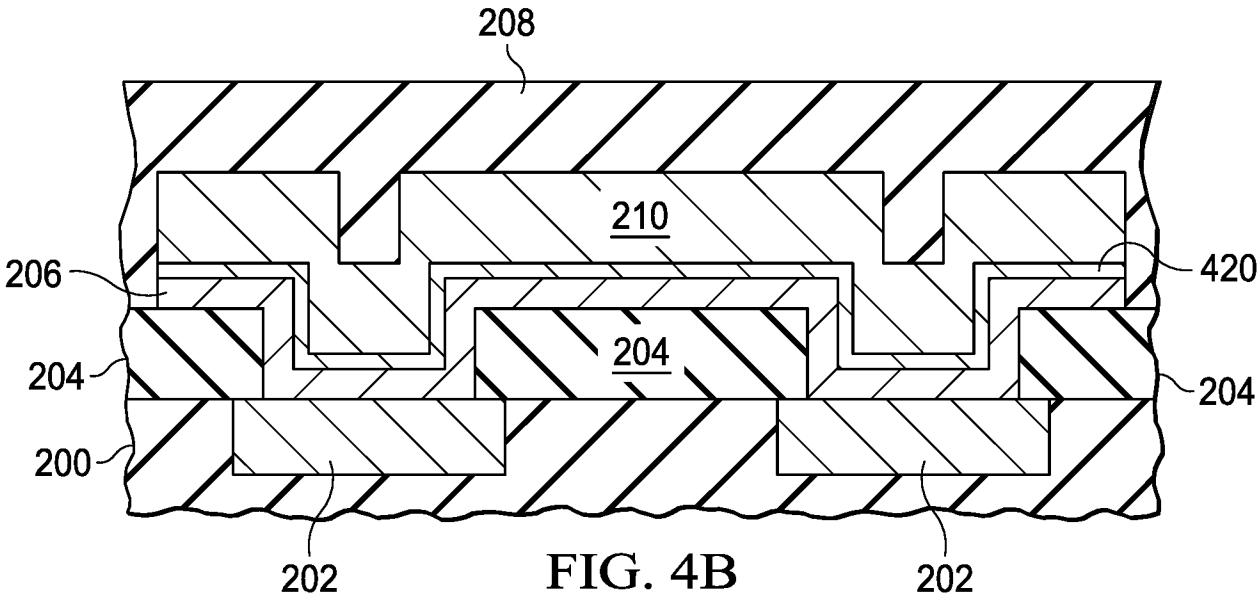

420
206
204
204
204
200
202
202

FIG. 4A


208
210
206
420
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200
202
202

FIG. 4B

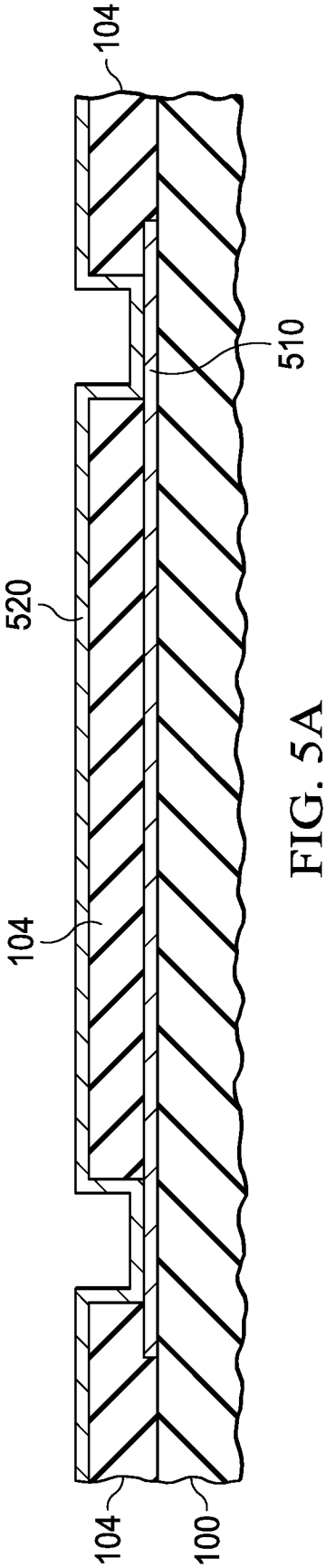

FIG. 5A

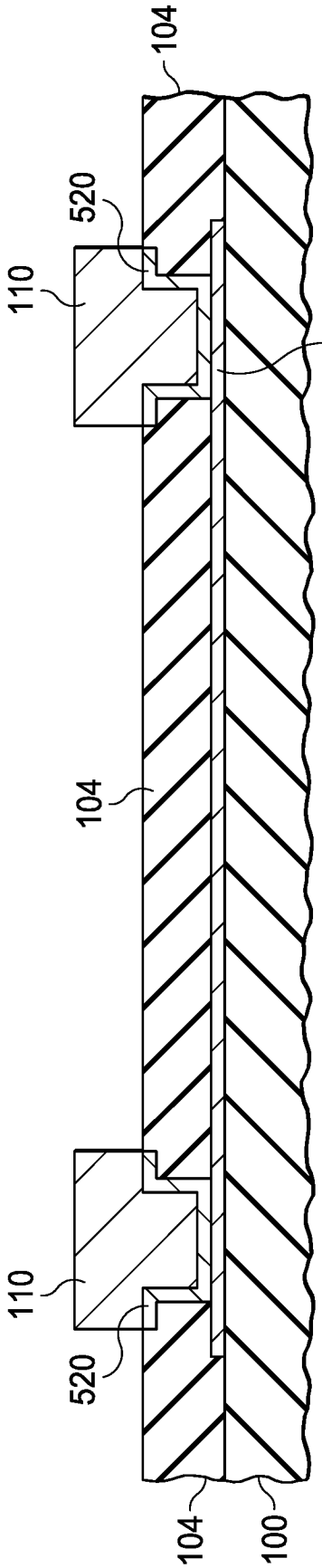

FIG. 5B

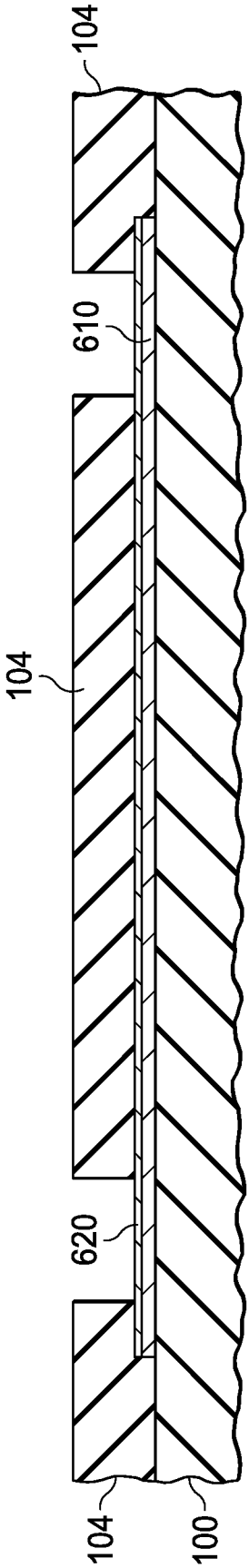

FIG. 6A

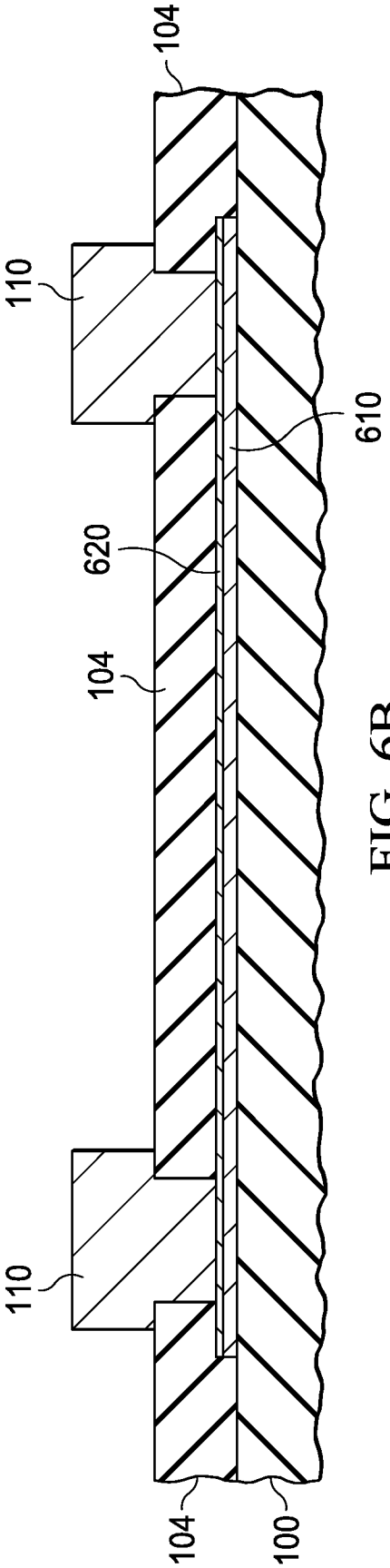

FIG. 6B

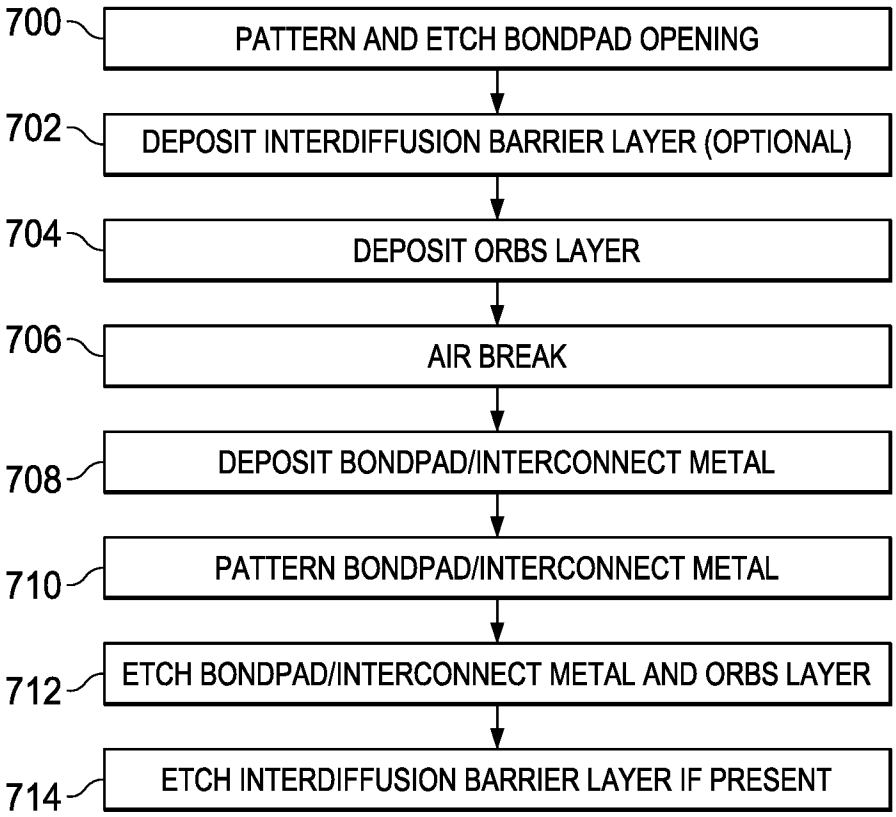
700
PATTERN AND ETCH BONDPAD OPENING
702
DEPOSIT INTERDIFFUSION BARRIER LAYER (OPTIONAL)
704
DEPOSIT ORBS LAYER
706
AIR BREAK
708
DEPOSIT BONDPAD/INTERCONNECT METAL
710
PATTERN BONDPAD/INTERCONNECT METAL
712
ETCH BONDPAD/INTERCONNECT METAL AND ORBS LAYER
714
ETCH INTERDIFFUSION BARRIER LAYER IF PRESENT

FIG. 7

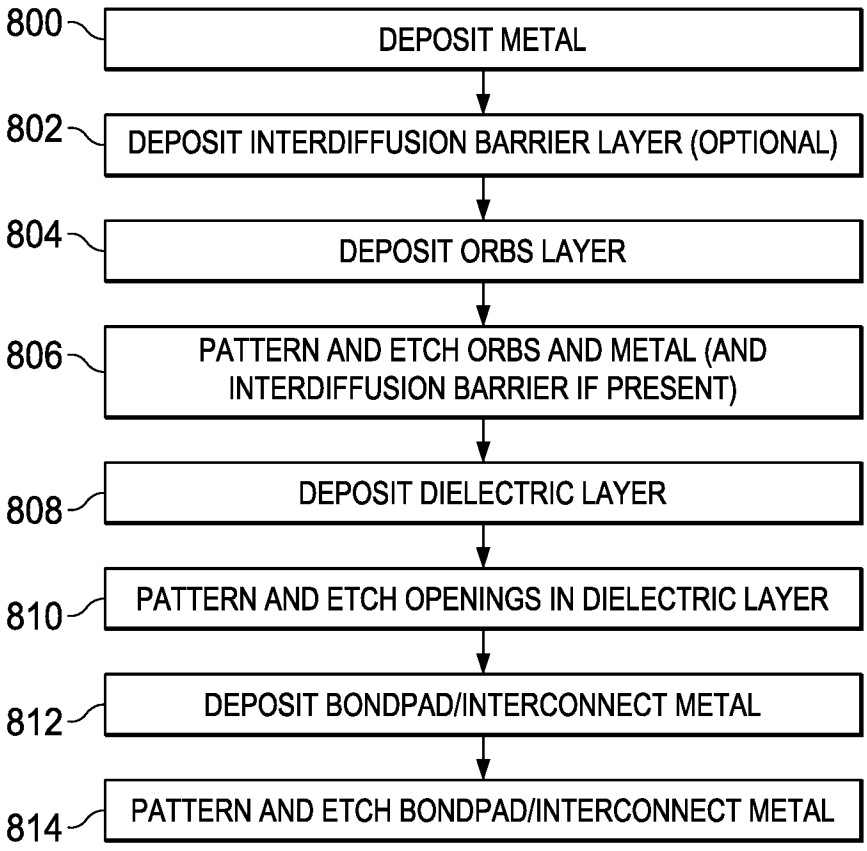
800
DEPOSIT METAL
802
DEPOSIT INTERDIFFUSION BARRIER LAYER (OPTIONAL)
804
DEPOSIT ORBS LAYER
806
PATTERN AND ETCH ORBS AND METAL (AND INTERDIFFUSION BARRIER IF PRESENT)
808
DEPOSIT DIELECTRIC LAYER
810
PATTERN AND ETCH OPENINGS IN DIELECTRIC LAYER
812
DEPOSIT BONDPAD/INTERCONNECT METAL
814
PATTERN AND ETCH BONDPAD/INTERCONNECT METAL

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/067495

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/4763 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00, 21/02, 21/04, 21/18, 21/30, 21/302, 21/34, 21/46, 21/461, 21/4763

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6339029 B1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY) 15.01.2002	1-20
A	US 6953742 B2 (APPLIED MATERIALS, INC.) 11.10.2005	1-20
A	US 7585765 B2 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 08.09.2009	1-20
A	US 2002/0192940 A1 (SHYH-DAR LEE et al.) 19.12.2002	1-20
A	US 7265038 B2 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY) 04.09.2007	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 March 2017 (31.03.2017)	13 April 2017 (13.04.2017)

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