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Barrigher et al.

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[54] **VARIABLE RATE LOAD SETBACK CIRCUIT**

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[52] **U.S. Cl.**.................. **307/149**, 60/105, 290/40 C, 415/15

[51] **Int. Cl.**.. **F01d 17/08**

[58] **Field of Search**........................ 60/105, 108, 73; 415/15; 307/149, 150; 290/52, 40 R, 40 A, 40 C, 40 D; 317/5

[56] **References Cited**

UNITED STATES PATENTS

3,340,883	9/1967	Petenel	415/15
3,561,216	2/1971	Moore	60/105 X
3,643,437	2/1972	Birnbaum et al.	60/105 X

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Assistant Examiner—William J. Smith
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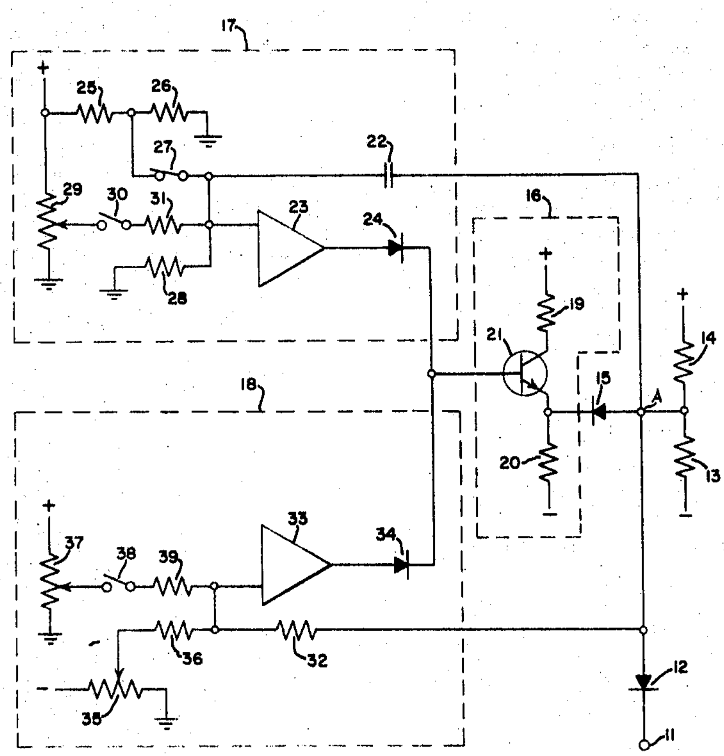
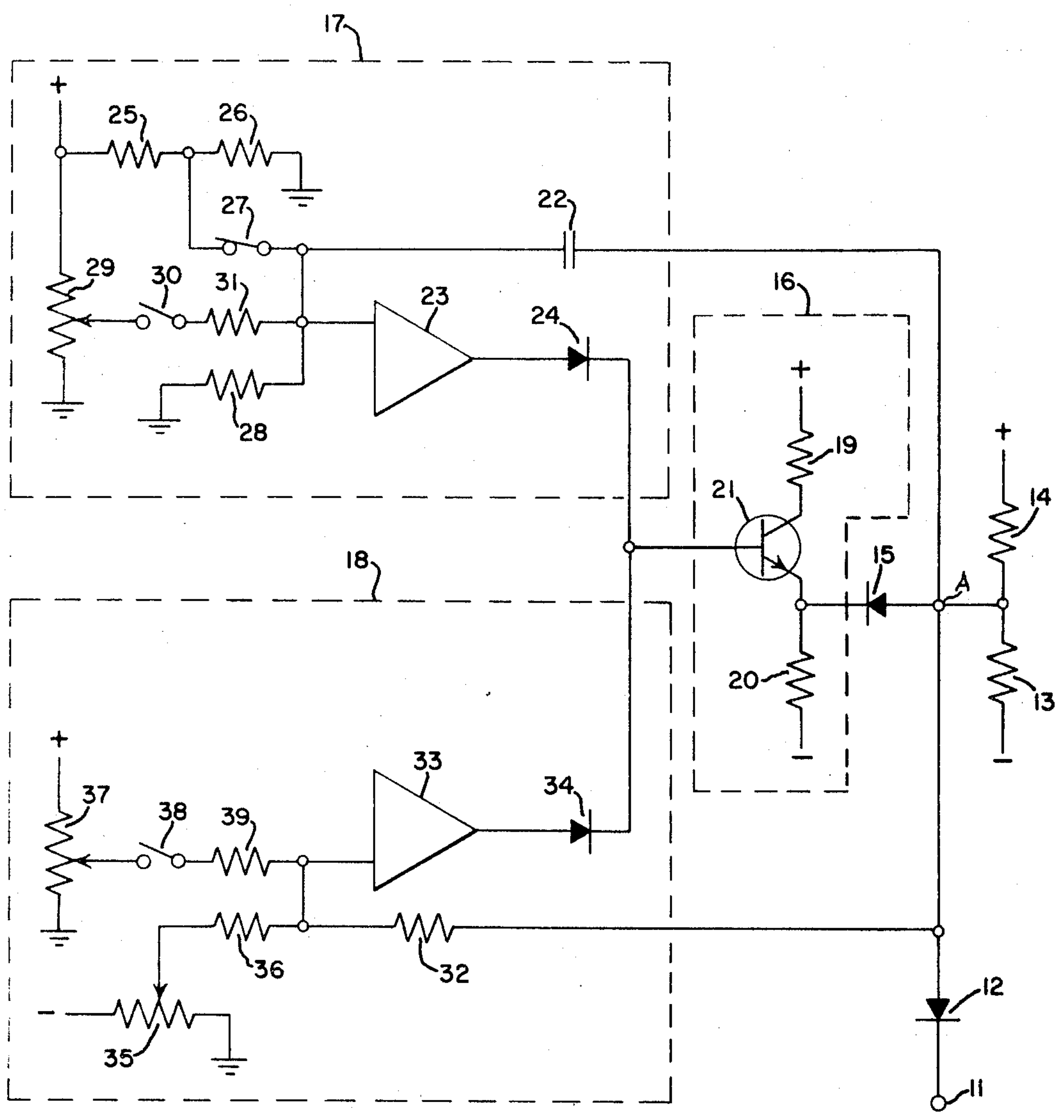
[57] **ABSTRACT**

A turbine control circuit which adjust the rate of power reduction by adjusting a load reference signal to control a steam control valve to compensate for the rate of loss of steam for the continued operation of a turbine with a failed component in the steam generating loop.

12 Claims, 1 Drawing Figure

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VARIABLE RATE LOAD SETBACK CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to control circuitry for a turbine system and is especially applicable to control of steam turbine systems.

In operating steam turbine systems, it is important to reduce the mechanical power output of the turbine gradually rather than an abruptly during a failure of some critical components in the power plant, such as forced draft fans, coal crushers, boiler feed-water pumps or the like. When such a failure occurs, it is mandatory to reduce the steam flow and, consequently, the mechanical power output of the turbine. The rate of reduction of steam flow to the turbine should bear some relationship to the criticality of the failed component, the amount of load reduction necessary for continued operation without the failed component, and whether or not several components failed simultaneously or consecutively.

Present load setback circuits, as evidenced by U.S. Pat. No. 3,561,216, issued upon an application by J. H. Moore, Jr., and U.S. Pat. No. 3,340,883, issued upon an application by J. R. Peternel, both of which patents are assigned to the present assignee, accomplish the task of producing a load reference signal to control the steam control valve to reduce the steam flow in proportion to the criticality of the failed component and number of failures. However, present setback circuits lack means of adjusting the steam control valve to compensate for the rate of the loss of steam.

This problem has been substantially eliminated by providing in a preferred embodiment of my invention a novel variable rate load setback circuit which has the ability to reduce the steam flow to any desired level, as determined by a plant operator. When compensation for the rate of the loss of steam is desired, a switch will be activated which will set a preselected bias to an input of a first operational amplifier in an integrator circuit to decrease the selected load reference signal at a predetermined rate to form a load setback reference signal which will control the steam control valve. Simultaneously, a preset bias to an input of a second operational amplifier in a limiter is applied and this action clamps the load setback reference signal at the preset level.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a new and improved variable rate load setback circuit which will automatically adjust the rate of power reduction to compensate for the rate of loss of steam in a turbine system by controlling the steam control valve with a load setback reference signal.

It is another object of this invention to provide a new load setback circuit in which a plant operator can alter at will, the flow rate of steam.

It is a further object of this invention to provide a new and improved variable load setback circuit for a steam turbine which responds at the fastest desired rate and to the lowest desired level automatically.

Briefly stated and according to one aspect of the invention, the foregoing objects are achieved by producing a new and improved variable rate load setback circuit comprising an integrator and a limiter. When an amplifier in the integrator and an amplifier in the limiter are individually biased at a value determined by the

operator, the load reference signal will be decreased from its operating value at a predetermined rate and clamped at a predetermined level to form a load setback reference signal. The load setback reference signal provides a means for the adjustment of the rate of power reduction by controlling the steam control valve and thus compensate for the rate of loss of steam in a turbine system with a failed component in the steam generating loop.

BRIEF DESCRIPTION OF THE DRAWING

The invention, both as to its organization and principle of operation together with further objects and advantages thereof may better be understood by reference to the following detailed description of an embodiment of the invention when taken in conjunction with the accompanying drawing in which the sole FIGURE is a circuit diagram illustrating the basic components of a variable rate load setback circuit in accordance with this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to the drawing, input terminal **11** provides a connection to receive a load reference signal or voltage from an amplifier which in the prior art is used to control a steam control valve. The load on the turbine is proportional to this load reference signal. The input terminal **11** is connected through diode **12** to a point A. The voltage at point A is held at a value corresponding to the load reference signal. Point A with respect to ground is also the output of the variable rate load setback circuit and this output ultimately controls a steam control valve (not shown). Resistors **13** and **14** are impressed with a voltage to provide a positive biasing voltage to diode **12.**

Diode **15,** which also receives a positive bias through resistors **13** and **14,** is shown connected in a first feedback loop of integrator **17** and in a second feedback loop of limiter **18.** A current amplifier **16** comprises resistors **19** and **20,** which produce voltage drops to allow a transistor **21** to perform its normal current amplification function, and are connected to the collecter and emitter respectively of transistor **21.** The emitter of transistor **21** is also connected to point A through diode **15.** Note that diode **15** forms an overall low value gate between the integrator **17,** limiter **18,** and the load reference signal applied at input terminal **11.**

Integrator **17,** which will provide a linearly decreasing voltage (from the load reference signal) at point A, is determined by an operator mandated setting of a control. Integrator **17** is connected in a feedback loop from the output of an operational amplifier **23** through a diode **24** to the base of transistor **21** in current amplifier **16** and serially through the emitter of transistor **21** and diode **15** to the input of integrator **17** through capacitor **22.** Input resistors **25** and **26** form a voltage divider and along with normally closed relay contact **27** apply a fixed positive bias to operational amplifier **23** to keep operational amplifier **23** in negative saturation. Also connected at an input to operational amplifier **23** is resistor **28,** the other end of which resistor is connected to ground. Resistor **28** is utilized to reduce the input impedance of operational amplifier **23** to overcome the extremely high impedance of amplifier **23** which would cause capacitor **22** to slowly continue charging and thus produce large steps whenever the integrator 17 was operating. Resistor 29 is utilized to control the amount of input voltage, as a preset bias, to be applied to an input of operational amplifier 23 through an input resistor 31 when normally open contact 30 is closed.

Limiter 18, which clamps the load reference setback signal at a preset value controlled by the operator, is connected to point A in a second feedback loop through resistor 32 to an input of operational amplifier 33. The output of operational amplifier 33 is applied to the base of transistor 21 in current amplifier 16 through a high value gate or diode 34 and from the emitter of transistor 21 through diode 15 to point A. Resistor 35 applies a negative voltage through input resistor 36 to an input of operational amplifier 33 to maintain operational amplifier 33 in positive saturation. Resistor 37 controls the voltage or preset bias applied to an input of operational amplifier 33 through closure of contact 38, which is normally open, and serially connected input resistor 39.

When it is desired to activate the variable rate load setback circuit, normally closed contact 27 is opened and normally open contact 30 in integrator 17 and contact 38 in limiter 18 are set, or closed. This is done in a manner well known in the art, such as energizing a coil of a relay which in turn closes contacts 30 and 38 and opens contact 27.

This drawing, for the sake of simplicity, shows only one input terminal 11 from the turbine system and only one variable rate load setback input. However, several of these inputs in practice are connected in parallel in a manner well known in the art, and the smallest signal present from any output ultimately controls the load signal.

In operation, the voltage at point A is initially held at whatever value corresponds with the load reference signal applied to input terminal 11.

Before the operator activates the setback circuit, the operational amplifier 23 in integrator 17 has a positive bias applied to its input to keep amplifier 23 saturated negatively, and the capacitor 22 charges to the voltage value at point A. The positive bias applied to amplifier 23 allows for a very fast integration rate. Therefore, the capacitor can rapidly follow changes in the voltage at point A.

In limiter 18, the negative bias applied through resistors 35 and 36 to operational amplifier 33 keeps amplifier 33 in positive saturation because of the low value gate diode 15 blocking feedback voltage in the second feedback loop of limiter 18. The voltage value of the negative bias applied to operational amplifier 33 is kept at a small increment above the largest positive voltage at point A, ever to be encountered in order to prevent diode 15 from conducting. The conduction of diode 15 is prevented due to the polarity reversal of operational amplifier 33 inherent in such an amplifier.

When automatically operated relay contacts 30 and 38 close and contact 27 opens, the load setback is initiated. The opening of contact 27 removes the fast integration rate from integrator 17 and, in closing, contact 30 applies a positive preset rate voltage to operational amplifier 33. Simultaneously, the closing of contact 38 applies a preset positive voltage to limiter 18. This new preset voltage in limiter 18 is positive but smaller in absolute value than the normal negative bias voltage of amplifier 33 and thus produces a net voltage subtraction at the input of operational amplifier 23 and thus a reduced positive voltage at the anode of diode 34.

The reduction of the anode voltage of diode 34 to a smaller positive value than present at point A biases diode 15 on, and causes the voltage at point A to begin to fall. This voltage drop is felt by capacitor 22 in integrator 17, and capacitor 22 begins to discharge into the input of operational amplifier 23. This discharge changes the input to operational amplifier 23 in a negative direction, driving amplifier 23 towards positive saturation. Amplifier 23 does not reach positive saturation in that, when the anode of diode 24 reaches the value of voltage slightly above that of its cathode, diode 24 conducts limiting the rise to the voltage value existing at point A. Integrator 17 takes control of the circuit operation and forces the output voltage at point A to decrease at the setback rate determined by the ohmic value of resistor 31, the preset value of voltage at resistor 29, and the capacitive value of capacitor 22.

When the voltage at the anode of diode 34 in limiter 18 falls due to the closing of contact 38, the reduction of voltage, as pointed out previously is initiated in that the limiter 18 is low value gated with respect to point A by diode 15. It is also high value gated with respect to amplifier 23 by diode 24. When diode 24 conducts as described above, operational amplifier 33 is forced into negative saturation due to the positive feedback voltage at the input of amplifier 33 through resistor 32. This voltage reduces as the voltage at point A reduces.

When the voltage output of operational amplifier 23 has been reduced at the preset rate to a smaller positive value than the difference between the bias at resistor 35 and at resistor 37, the limiter 18 due to its being high value gated with operational amplifier 23, and since the voltage at the input of operational amplifier 23 has already reached effective zero, will come out of negative saturation and take control. The voltage at point A will stabilize at the preset limit while oeprational amplifier 23 will be forced back into negative saturation from loss of feedback through diode 15 and the reversion of the effective voltage at the input of operational amplifier 23 to a positive value.

To remove the effect of the variable rate load setback circuit, normally open contacts 30 and 38 are reopened, and normally closed contact 27 is reclosed. The negative bias on operational amplifier 33, now free of the positive preset voltage from resistor 37, forces the anode of diode 34 to increase in a positive polarity direction. The effect of positive voltage placed at the input of operational amplifier 23 by the closure of contact 27 plus the increase in voltage at point A rapidly charges the capacitor 22 and forces operational amplifier 23 in integrator 17 into negative saturation. As soon as operational amplifier 33 loses control to the load reference signal, the loss of feedback forces it into positive saturation and the circuit is again ready for the next demand for a load setback.

It has been shown that, by providing an integrator which will produce a linearly decreasing voltage from a load reference signal and a limiter which will clamp the load reference signal at a preset value, a normal load reference signal can be compensated for the rate of the loss of steam to ultimately adjust the rate of power reduction by controlling a steam control valve.

While an embodiment and application of this invention has been shown and described, it will be apparent to those skilled in the art that many more modifications are possible without departing from the inventive concepts herein described. The invention, therefore, is not to be restricted except as is necessary by the prior art and by the spirit of the appended claims.

What is claimed as new and desired to be secured by Letters Patent of the United States is:

1. A turbine control circuit comprising:
means for receiving a load reference signal proportional to a desired load on a turbine;
means for linearly decreasing the load reference signal at a predetermined rate to form a load setback reference signal; and
means for clamping the load setback reference signal at a preset level.

2. A turbine control circuit as in claim 1 wherein said means for linearly decreasing the load reference signal is an integrator.

3. A turbine control circuit as in claim 2 wherein said integrator further comprises a first operational amplifier having a first feedback loop, a capacitor in series in said first feedback loop, and means for connecting a first preset bias to an input of said first operational amplifier.

4. A turbine control circuit as in claim 3 wherein said first preset bias is variable.

5. A turbine control circuit as in claim 1 wherein said means for clamping the load setback reference signal is a limiter.

6. A turbine control circuit as in claim 5 wherein said limiter further comprises a second operational amplifier having a second feedback loop, a resistor in series in said second feedback loop, and means for connecting a second preset bias to an input of said second operational amplifier.

7. A turbine control circuit as in claim 6 wherein said second preset bias is variable.

8. A turbine control circuit as in claim 3 wherein said means for connecting the first preset bias is remotely controlled.

9. A turbine control circuit as in claim 6 wherein said means for connecting the second preset bias is remotely controlled.

10. A turbine control circuit comprising:
means for receiving a load reference signal proportional to a desired load on the turbine;
an integrator circuit for linearly decreasing the load reference signal at a predetermined rate to form a load setback reference signal, said integrator circuit further comprising a first operational amplifier having a first feedback loop, a capacitor in series in said first feedback loop, and means for connecting a first preset bias to an input of said first operational amplifier; and
a limiter circuit for clamping said load setback reference signal at a preset level comprising a second operational amplifier having a second feedback loop and means for connecting a second preset bias to an input of said second operational amplifier.

11. A turbine control circuit as in claim 10 wherein said first and second preset biases are variable.

12. A turbine control circuit as in claim 10 wherein said means for connecting the first preset bias and said means for connecting the second preset bias are simultaneously remotely controlled.

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