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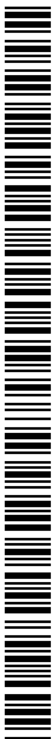

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(54) Title: INTEGRATED ELECTRONIC DEVICE WITH FLEXIBLE AND STRETCHABLE SUBSTRATE

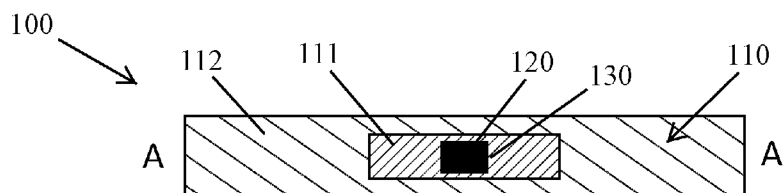

FIG. 1C

(57) Abstract: Disclosed herein is a flexible and stretchable integrated electronic device comprising a substrate having at least a first portion and a second portion, wherein a rigid electronic device is embedded within the substrate. The stiffness of the first portion and the second portion differ, creating a stiffness gradient within the substrate to prevent delamination at the interface between the substrate and the embedded device.

TITLE

Integrated Electronic Device with Flexible and Stretchable Substrate

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit under 35 U.S.C. § 119 of Provisional Application Serial No. 62/389,853, filed March 10, 2016, which is incorporated herein by reference.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

[0002] This invention was made with Government support under 1547810-CBET and 1100430-CMMI awarded by the National Science Foundation. The Government has certain rights in this invention.

BACKGROUND OF THE INVENTION

[0003] The invention relates generally to flexible and stretchable electronics. More specifically, the invention relates to an integrated device comprising a substrate with an embedded rigid electronic device, where the substrate has a stiffness gradient around the embedded device to allow flexible and stretchable movement of the integrated device.

[0004] Flexible and stretchable electronics have emerged as a new technology for realizing smart sensors and actuators for applications ranging from medicine to personal electronic devices. Such systems have been evolving at a rapid rate with the promise of integration into areas such as the human body. However, integrating rigid electronics with a flexible substrate (i.e. the human body) poses problems resulting from the mismatch in compliance between the two materials.

[0005] Stretchable electronics have been pursued through a wide variety of techniques including organic electronic materials such as conductive polymers, nanowires, microfluidic circuits, and thin inorganic materials patterned on soft polymers. An elusive goal of these approaches is to simultaneously achieve the performance and reliability of established foundry electronic devices in a stretchable platform. However, the goal is

unmet as these designs suffer from relatively poor transistor density and performance in addition to uncertain reliability.

[0006] Inorganic materials such as silicon processors have been used in electronic devices for decades and embedding these materials in stretchable and flexible structures would provide integrated functionality and reliability. However, delamination of the rigid processor from the soft substrate has inhibited the impact of this approach. To overcome this problem, one method attempts to use sub-micron layers of inorganic materials within an electronic device, which allows the stiff materials to have a higher degree of flexibility. However, thinning the devices causes significant challenges for integrating silicon-based electronics as the interconnect stack for complementary metal-oxide semiconductors (CMOS), for example, is well over 1 μm in thickness and is over 10 μm thick for state-of-the-art CMOS available from foundries. These devices cannot be easily thinned.

[0007] Along with the challenges in the lack of flexibility of these silicon-based electronics is the mechanical response associated with embedding them into flexible materials. For example, there is a significant mismatch in mechanical properties of silicon-based electronics (Young's modulus, $E \approx 170$ GPa) and soft materials mimicking those of the human body (Young's modulus, $E \approx 100$ kPa). This mismatch causes difficulties in the attachment, stretching, and functionality for wearable biomedical instruments. Silicon-based electronics that are rigid and planar have a fracture strain less than 2%, while flexible and stretchable electronics can be bent, stretched, and twisted with typical failure strain greater than 10%.

[0008] As another approach to overcome the mismatch problem, thin polymer films that are relatively stiff compared with stretchable materials are embedded into stretchable substrates in order to suppress the onset of interconnect and device breakage. In one example of this approach, patches of polyethylene terephthalate are embedded within a softer polymer to help suppress strain local to the device substrate and increase the shear area, demonstrating operation up to 100% uniaxial stretching and 300% localized

internal strain. However, the general intent of locally suppressing strain works when the electronic devices are on the surface of the substrate since no interface exists for normal stress to cause delamination in this configuration.

[0009] It would therefore be advantageous to develop a flexible and stretchable substrate incorporating traditional electronic devices that prevents delamination between the materials.

BRIEF SUMMARY

[0010] According to embodiments of the present invention is an integrated electronic device comprising a rigid electronic device embedded within a substrate having variable stiffness. More specifically, the substrate demonstrates a stiffness gradient with the greatest stiffness adjacent to the rigid electronic device. By creating a gradient, the incidence of delamination of the substrate from the embedded device is decreased when the integrated device is stretched or flexed.

[0011] The integrated device allows the use of “thick” silicon chips (e.g., thickness greater than 10 μm) mimicking CMOS electronic chips for wearable system applications such as biomedical health monitors that interface with the skin where large deformation can occur. Further, in this configuration the peak strain experienced in the device is moved away from the rigid/elastomeric interface. Eliminating the delamination effects between the soft and rigid material is required for design of stretchable systems that will embed standard microfabricated electronics (i.e., CMOS), especially in wearable applications.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0012] Figs. 1A-1C show the integrated device, according to one embodiment.

[0013] Fig. 2 is an image showing delamination at the interface of the rigid device and the substrate.

[0014] Fig. 3 is a graph depicting the stiffness of various components of the integrated device.

[0015] Figs. 4-5 are graphs showing the energy release rate for integrated devices with varying parameters.

[0016] Figs. 6A-6B show the strain in the device as a function of the distance from a center.

[0017] Figs. 7A-7B are graphs depicting energy release rates.

[0018] Fig. 8 shows the failure strain at various interfaces.

[0019] Figs. 9-11 are graphs depicting energy release rates.

[0020] Figs. 12A-12C depict a fabrication method of the integrated device according to one embodiment.

[0021] Figs. 13A-13C depict an alternative fabrication method.

[0022] Figs. 14A-14C show another fabrication method.

[0023] Figs. 15A-15D depict a fabrication method with the inclusion of passive electronic devices.

DETAILED DESCRIPTION

[0024] According to one embodiment of the present invention is an integrated electronic device 100 comprising a flexible and stretchable substrate 110 and a rigid electronic device 120. As shown in the embodiment depicted in Fig. 1A, the substrate 110 comprises a plurality sections. More specifically, the substrate 110 of the embodiment shown in Fig. 1A comprises a first section 111 and a second section 112, where the first section 111 has a greater stiffness than the second section 112. As further shown in Figs. 1A-1B, the rigid electronic device 120 is embedded within the first section 111 of the substrate 110. By providing a gradient in the stiffness of the substrate 110, delamination at the interface 130 between the rigid electronic device 120 and the substrate 110 can be reduced. That is, the presence of the intermediate soft material (first section 111) with a Young’s modulus between that of the primary soft material (second section 112) and the embedded device 120 decreases the risk of delamination.

[0025] While example embodiments will be discussed in terms of a first section 111 and a section 112, the substrate 110 may comprise additional sections to further smooth the stiffness gradient. In alternative embodiments, a continuous stiffness gradient is employed on the substrate 110 without distinct sections. The presence of distinct sections or a continuous gradient in the substrate depends, in part, on the particular fabrication method employed.

[0026] As stated, the stiffness gradient aims to prevent delamination at the interface 130 of the embedded device 120 and the flexible substrate 110. To quantify the delamination characteristic of the interface 130, the ‘energy release rate’, G in units of J/m^2, is used to guide the fabrication of the integrated flexible electronic device 100. In testing, the energy introduced to a pre-formed crack, which causes it to increase in size, must be balanced by the amount of energy lost due to the formation of new surfaces and other dissipative processes, such as plasticity. The crack size increases when the energy release rate equals a critical value, the fracture energy denoted as Γ.

[0027] The risk of delamination at the interface 130 between a soft material and rigid material is significant and this risk increases when the system is stretched and thus subjected to mechanical strain. Therefore, if the structure has sufficiently high stress at the interface 130 between the two materials, delamination occurs (see Fig. 2). To address this challenge, the amount of strain and strain energy in the soft material (i.e. substrate 110) at the interface 130 should be minimized to prevent delamination. This minimization is accomplished using the intermediate material gradient such that the mechanical stiffness properties between the soft and rigid materials are changed gradually (see Fig. 3). Adding a single intermediate material in the first section 111 of the substrate 110, where the first section 111 has a stiffness value between the soft second section 112 and the rigid embedded device 120, has a significant effect in reducing delamination and allows for the integration of rigid devices 120, such as CMOS chips.

[0028] In one embodiment, the substrate 110 that surrounds the silicon-based electronic device 120 is made of two soft polymers with

different Young's modulus, E_1 and E_2 ($E_2 > E_1$). The stiffer intermediate polymer (Young's Modulus E_2) is in contact with the silicon-based device 120 while the softer material (Young's Modulus E_1) occupies the outer domain. When the composite substrate 110 is strained, the outer, second portion 112 has a higher strain when compared to the intermediate inner first portion 111. The value of Young's modulus (E_2) of the intermediate material has an effect in minimizing the delamination in the flexible integrated device 100.

[0029] For example, the effect of the ratio, E_2/E_1, can be determined by calculating the energy release rates using techniques such as a two-dimensional finite element analysis (FEA). The two conditions $E_2/E_1 = 10$ and $E_2/E_1 = 100$ shown in Fig. 4 indicate the significance of the Young's modulus ratio on delamination of layers. The energy release rate values for additional ratios are shown in Fig. 5. As shown in Fig. 4, the system having the higher Young's modulus ratio has the lowest energy release rate for all values of L_2, which corresponds to the length or radius of the first section 111. As the energy release rate rises with external applied strain, the system with the higher Young's modulus ratio results in a larger safe region where delamination does not occur. Of note, for any case where a first portion 111 and second portion 112 are used, the energy release rate is lower when compared to just a single soft material having either Young's modulus E_1 or E_2.

[0030] Results from an example finite-element analysis are shown in Figs. 6A-6B. Maximum principal elastic strain for two structures without (Fig. 2A) and with (Fig. 2B) the engineered two-part substrate 110, indicate the amount of strain in the cut-plane coinciding with the top surface of silicon device 120. The strain at the interface 130 between the silicon electronic device 120 and the intermediate first portion 111 in the engineered substrate 110 is approximately six times smaller than in the example substrate 110 having only a single material. This lower strain region at the chip interface 130 to the engineered substrate 110 reduces the onset of delamination from the embedded electronic device 120.

[0031] In the example shown in Fig. 6B, the highest strain occurs at the interface between the first portion 111 and the second portion 112. Accordingly, this region is the most susceptible to delamination. However, by selecting two materials with strong bonding capability, the substrate 110 can be designed to withstand higher strains before delamination. In one embodiment, the substrate comprises polydimethylsiloxane (PDMS) with a differing amount of elastomer base-to-curing agent mixing ratio. PDMS with different base-to-curing agent mixing ratios exhibit strong bonding. In addition, the bonding between the two sections 111, 112 can be enhanced by selecting materials with high surface adhesion. Also, in general, an enhanced roughness at the border between the two has a positive effect on bonding between the two soft materials. In alternative embodiments, other soft polymers are used in the substrate 110.

[0032] In order to compare variations in the two-section substrate 110, three example embodiments (listed in Table 1) are analyzed. In these examples, the rigid electronic device 120 is a 1 mm × 1 mm × 50 μm silicon chip. For the compliant substrate 110, two mixtures of PDMS with a base-to-curing ratios of 5:1 and 20:1 are used. Using PDMS with different ratios of base and curing agent for the materials of the first section 111 and second section 112 allows the Young's modulus values to be modified between regions while still achieving strong bonding at their interface. The substrate 110 in examples #1 and #2 are made completely of a single type of PDMS, while the substrate 110 in example #3 implements the composite structure with a first section 111 and a second section 112 of PDMS each having different stiffness.

[0033] Table 1

Sample	1st Sec. Material	2nd Sec. Material	Energy Release
#1	PDMS (5:1), L = 3 mm	none	10.99 J/m^2
#2	PDMS (20:1), L = 3 mm	none	1.493 J/m^2
#3	PDMS (20:1),	PDMS (5:1),	0.689 J/m^2

	L = 2 mm	L = 1 mm	

[0034] The energy release rate, which indicates the likelihood of delamination, was determined for a given interface using a FEA with a symmetric quarter model of the entire substrate. A fine mesh was placed on an initial 10 μm-wide separation (i.e., a crack initiator) located at the interface 130 between the sidewall of the rigid device 120 and the surrounding PDMS substrate 110. The crack with the highest degree of stress was located at the corner of the device 120. The energy release rate was determined by subtracting the strain energy before and after crack growth, while dividing by the area of the crack. Mesh refinements were used to verify numerical convergence.

[0035] Table 1 indicates that the energy release rate in the stiffest substrate (PDMS (5:1)) used in sample #1 is over 7 times higher than the energy release rate in the intermediate stiffness substrate 110 (PDMS (20:1)) used in sample #2. The energy release rate for sample #3 was found to be approximately two times lower than the next best case of sample #2. When the energy release rate exceeded a critical value, as determined empirically, the crack propagated and the substrate 110 delaminated from the embedded rigid device 120. As a result of the lowest energy release rate occurring for sample #3, the risk of delamination at the interface was low and the interface remained intact.

[0036] To compare FEA predictions shown in Table 1 and to quantify the onset of strain failure, tensile tests were performed for all three sample types. In many applications, the rigid device 120 will often be no greater than 1 mm in size and sparsely embedded within the substrate 110, while the radius of bending curvature of the soft substrate 110 is expected to be much greater than 1 mm. Tensile strain loading at each end of the substrate was applied as a series of small incremental step functions. The system was elongated at a low strain rate (0.001 s^{-1}) to achieve a pseudo steady-state and the strain failure was examined through optical microscopy imaging. Delamination for sample #1 occurred at 20% strain, as indicated

by a crack initiation and subsequent growth. The strain for delamination for sample # 2 was higher, occurring at 30% strain at the interface 130 and in line with the finite-element predictions (see Table 1). The silicon-PDMS (5:1) interface 130 in sample #3 did not delaminate. Instead, crack growth occurred at the interface of the PDMS (5:1) and PDMS (20:1) materials between the first section 111 and second section 112, rather than at the interface 130 with the embedded device 120, and initiated at 100% strain. This strain failure threshold was six times larger than that of sample #1 (with the silicon-PDMS (5:1) interface). Further, the strain cycling performance of sample #3 up to 100 cycles under maximum 50% strain was studied and delamination was not detected at either interface.

[0037] While the foregoing analyzes the effect of material stiffness on the risk of delamination, the relative length of each section 111, 112 of the substrate 110 also have an effect. To minimize the delamination risk, the substrate 110 can be analyzed based on the ratio of the length of first section, L_2, to the total substrate length, $L = L_1 + L_2$. The energy release rates for different values of the L_2/L ratio at the interface 130 of silicon-PDMS (5:1) and at the interface 130 of PDMS (5:1)-PDMS (20:1) were calculated.

[0038] At these interfaces, material properties and geometric design parameters affect the energy release rate function:

$$G = f(a, E_1, E_2, \varepsilon, L_1, L_2, h_1, h_2, h_3) \quad (1)$$

where a is crack length, ε is the applied strain, h_1 is the thickness of the material in the second section 112 of substrate 110 on top of the embedded device 120, h_2 is the thickness of the material in the first section 111 on top of the embedded device 120, and h_3 is the thickness of the embedded device 120.

[0039] For this comparison, all parameters except L_2 are fixed. The energy release rate increases with increasing applied strain with approximately quadratic dependence. This nonlinear dependence of G on strain arises in Fig. 7A, which also illustrates a nonlinear dependence on L_2. A comparison in Fig. 7B of energy release rates at 20% strain for the

interface 130 (top line) and for the first section 111 / second section 112 (PDMS (5:1) / PDMS (20:1)) interface (bottom line) indicates that *G* for the silicon-PDMS interface 130 is roughly two times higher than for the PDMS-PDMS interface. In Fig. 7B, $L_2/L = 0$ represents the sample #1 case and $L_2/L = 1$ represents the sample #2 case, with these endpoint values corresponding to those in Table 1. For intermediate values of L_2/L, the energy release rate at the silicon-PDMS interface 130 decreases significantly.

[0040] Fig. 8 shows the tensile responses of integrated devices 100 with different L_2/L (0.05, 0.15, 0.25, 0.35, 0.45) and a fixed L = 10 mm. The graph of Fig. 8 shows the quantified the strain level at the onset of delamination and indicates in all cases that the interface between the first section 111 and second section 112 failed first. The failure strain values for the example without an intermediate stiffness first section 111 ($L_2/L = 0$ and $L_2/L = 1$) were relatively small. The highest failure strain of 140% occurred with the geometric condition of $L_2/L = 0.05$ (see Fig. 8). The effects on *G* of h_3/h_2, h_1/h_2, and E_2/E_1 are shown in Figs. 9, 10, and 11, respectively. Delamination typically happens at corners, edges and regions of the device/substrate interface 130 where there is high strain. Having rounded corners or circular chips can reduce the energy release rate.

[0041] It is estimated that the adhesion energy of Si–PDMS interfaces is about 0.05–0.4 J/m^2. The work of adhesion for a PDMS-PDMS interface is in the range of about 250−300 J/m^2. Therefore, the PDMS-PDMS bonding is stronger than Si-PDMS bonding by four orders of magnitude. While the Si-PDMS adhesion could possibly be enhanced through a geometric interlock design or through use of adhesion promoters, the substrate 110 of the present invention moves the critical interface to the interface of the first section 111 and the second section 112, enabling exploitation of the natural adhesion between similar polymers.

[0042] To create a substrate 110 having a gradient, PDMS with mixing ratios of base to curing agent of (5:1) and (20:1) were used in the example embodiment described above. However, in alternative embodiments, other mixing ratios, additional materials, or distinct materials can be used to

create the gradient. In the example embodiment, the Young's modulus values are E_2 = 1.98 MPa for PDMS (5:1) and E_1 = 0.26 MPa for PDMS (20:1).

[0043] One fabrication method comprises embedding a 1 mm × 1 mm × 50 µm silicon chip (E = 170 GPa) as the rigid device 120 into a 90 µm-thick PDMS sheet as the substrate 110. To make the two-material substrate, a handle wafer as a base 141 is spin coated with 10 µm-thick PDMS (5:1), which will become part of the first portion 111 of the substrate 110. Next, the silicon chip (i.e. device 120) is then transferred to this first layer, and a second 60 µm-thick PDMS (5:1) layer is spin coated and then cured at 80°C for 4 hrs., thereby embedding the rigid device 120 in the first portion 111 of the substrate 110. This composite structure is then etched into a 1 mm diameter circle and released from the base 141 and subsequently transferred to a second base 141 having an initial 10 µm-thick spin-coat PDMS (20:1) layer, which will be part of the second portion 112. The composite structure is then embedded into PDMS (20:1) by spin coating an additional 80 µm-thick PDMS (20:1) layer followed by 4 hrs. curing at 80°C. The soft PDMS (20:1) material of the second portion 112 covers the first portion 111 by approximately 10 µm on its top and bottom surfaces. Thus, in this embodiment of the method of fabrication, there are two general stages: first, embedding the rigid device 120 into the first portion 111 of the substrate 110; and, second, embedding the combined structure into the second portion 112 of the substrate 110.

[0044] In an alternative embodiment, the base 141 is coated with a submicron layer of gelatin (1%). Gelatin is used as a sacrificial layer 143 (see Fig. 1B) since it is soluble in water and it aids in release of the device 100. For example, the device 100 can be released in hot water (70°C) since gelatin is highly soluble at this temperature level. In yet another embodiment, the combined embedded device 120 / first portion 111 composite structure is patterned into a circular shape using a hard mask through reactive-ion etching using SF_6/O_2 plasma for 3 hrs.

[0045] In an alternative fabrication method, as shown in Figs. 12A-12C, the embedded device 120 is placed on a cured layer of the second

portion 112 of the substrate 110. Next, as shown in Fig. 12A, drops of the material for the first portion 111 are deposited around the device 120. The material can be added manually, or with the aid of equipment such as an inkjet or 3D printer. Fig. 12B shows the material of the second portion 112 of the substrate 110 added. The released integrated device 100 is shown in Fig. 12C.

[0046] Figs. 13A-13C depict another alternative embodiment of the fabrication method. First, the rigid electronic device 120 and the first portion 111 of the substrate 110 are fabricated, as described above, and place on a cured layer of the second portion 112. The composite structure is then surrounded with uncured polymer, as shown in Fig. 13B. Drops of material are then deposited at the interface between the first portion 111 and the second portion 112, creating a gradient at the interface of the two portions 111, 112.

[0047] Figs. 14A-14C show embodiment of the fabrication method with a continuous gradient without a distinct first section 111 and second section 112. In this method, the gradient in stiffness in the substrate 110 is created by diffusing a curing agent into the substrate 110. For example, as shown in Fig. 14A, the device 120 is embedded within the substrate 110, which can be cured or semi-cured. If semi-cured, the substrate 110 may have some portion of the curing agent pre-mixed into the material. Once the device 120 is embedded in the substrate 110, drops of the curing agent are deposited onto the substrate 110, which will then diffuse into the material. As previously stated, the drops can be added manually or by using an inkjet or 3D printer, where it can diffuse into the substrate 110. If using a printer, the pattern of drops can be programmed digitally to provide any gradient pattern. For example, the printer can make a first pass of depositing a curing agent at the interface 130. A second pass can cover the same area, but also extend beyond the area of the first pass. Subsequent passes can enlarge the area covered by the curing agent. In this manner, the first area will be covered by the most passes and, thus, will have the highest

concentration of curing agent, leading to a higher stiffness in the substrate 110.

[0048] When using an inkjet printer, addition steps may be performed to aid the process. For example, in one alternative embodiment the curing agent is combined with a solvent, such as xylene or trichlorobenze, to reduce the viscosity of the curing agent. Alternatively, the curing agent could be heated to reduce the viscosity. However, if the curing agent becomes too hot, cross-linking of the polymer is possible, which would affect the stiffness. As such, the substrate 110 can be heated while cooling the curing agent in the printing equipment. Other variations of this technique can be employed to develop an appropriate viscosity and surface tension to allow printing and diffusion of the curing agent into the substrate 110.

[0049] Figs. 15A-15D show an alternative fabrication embodiment where antennas, coils, and other passive devices 150 are embedded in the substrate 110. As a person having skill in the art will appreciate, several fabrication methods to create a gradient in the substrate 110 can be employed.

[0050] While the disclosure has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modification can be made therein without departing from the spirit and scope of the embodiments. Thus, it is intended that the present disclosure cover the modifications and variations of this disclosure provided they come within the scope of the appended claims and their equivalents.

CLAIMS

What is claimed is:

1. A method of making an integrated electronic device having a stiffness gradient, the method comprising:

embedding a rigid electronic device in a substrate,

applying a curing agent to a first area of the substrate adjacent to the rigid electronic device; and

applying the curing agent to a second area of the substrate,

wherein the curing agent creates a portion of the substrate adjacent the embedded electronic device with a modulus in between a modulus of a portion of the substrate not adjacent to the embedded electronic device and the modulus of the rigid electronic device.

2. The method of claim 1, wherein the curing agent is applied using an inkjet device.

3. The method of claim 2, further comprising:

thinning the curing agent using a solvent.

4. The method of claim 3, wherein the solvent is selected from the group consisting of xylene and trichlorobenzene.

5. The method of claim 1:

wherein the curing agent is applied to the first section at a ratio of base-to-curing agent of 5:1; and

wherein the curing agent is applied to the second section at a ratio of base-to-curing agent of 20:1.

6. An integrated electronic device comprising:
   a substrate having a stiffness gradient,
      wherein the substrate has a stiffness gradient with a maximum stiffness adjacent a rigid electronic device,
      wherein the rigid electronic device is embedded in the substrate.

7. The integrated electronic device of claim 6, further comprising:

8. The integrated electronic device of claim 6, wherein the substrate comprises PDMS.

9. The integrated electronic device of claim 6, wherein the substrate comprises:
   a first section adjacent the rigid electronic device,
      wherein the second section has a second Young's modulus;
   a second section adjacent the first section,
      wherein the second section has a second Young's modulus,
      wherein the second Young's modulus is less than the first Young's modulus.

10. The integrated electronic device of claim 6, further comprising:
   a passive electronic device embedded in the substrate and connected to the rigid electronic device.

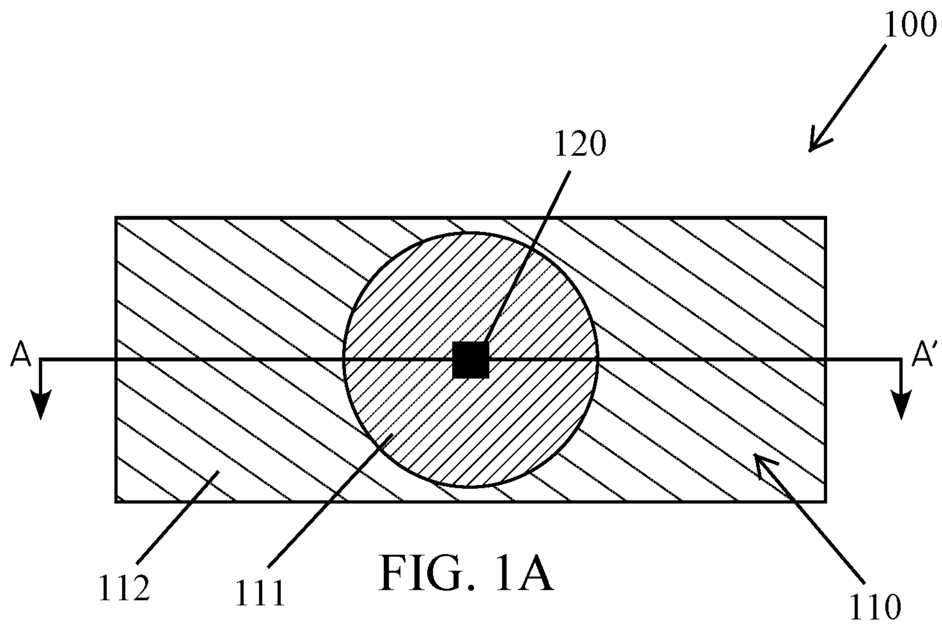

FIG. 1A

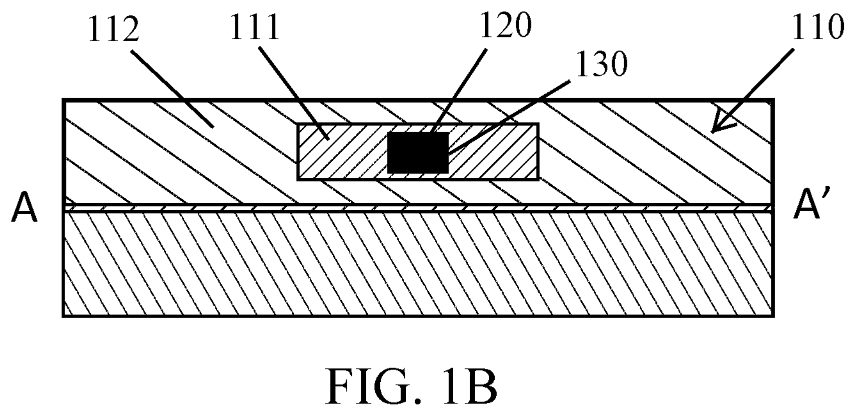

FIG. 1B

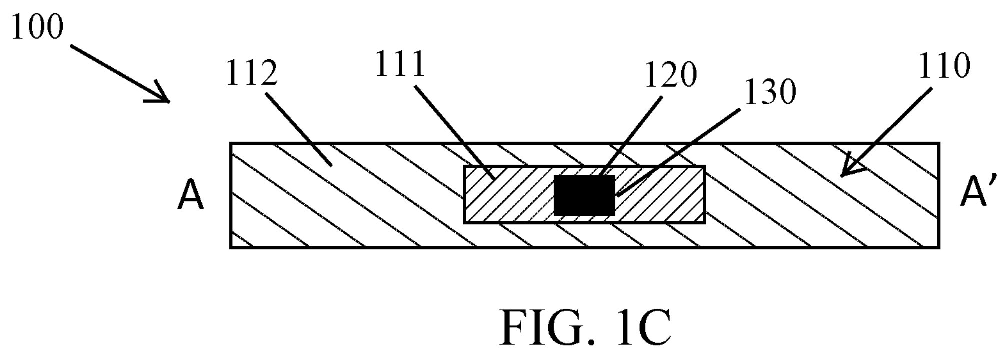

FIG. 1C

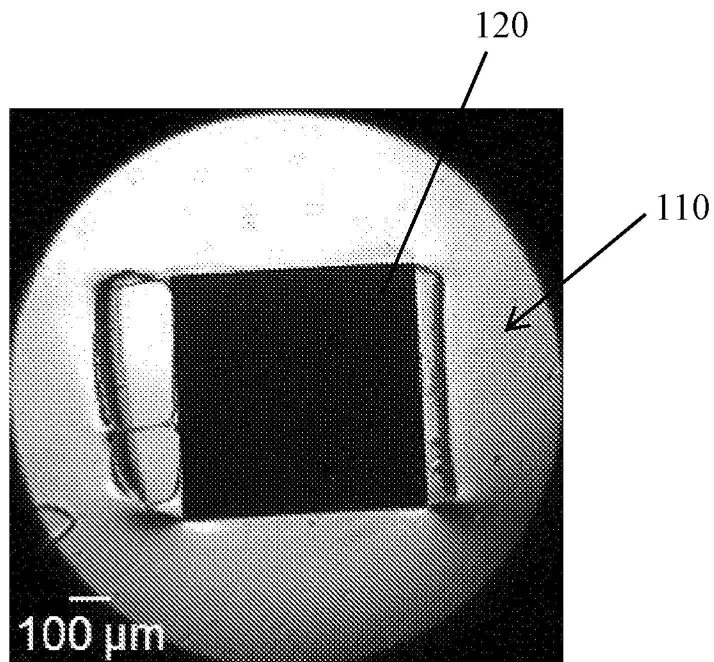

FIG. 2

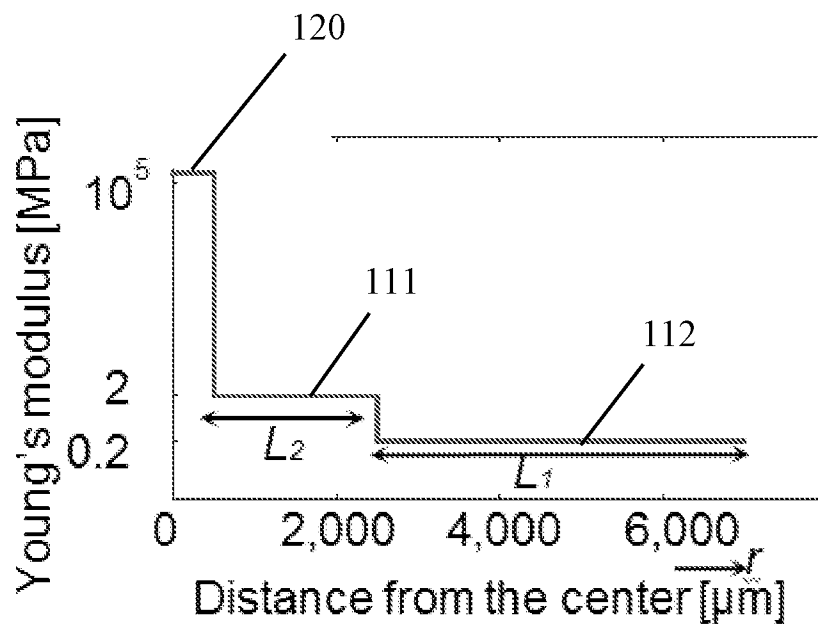

FIG. 3

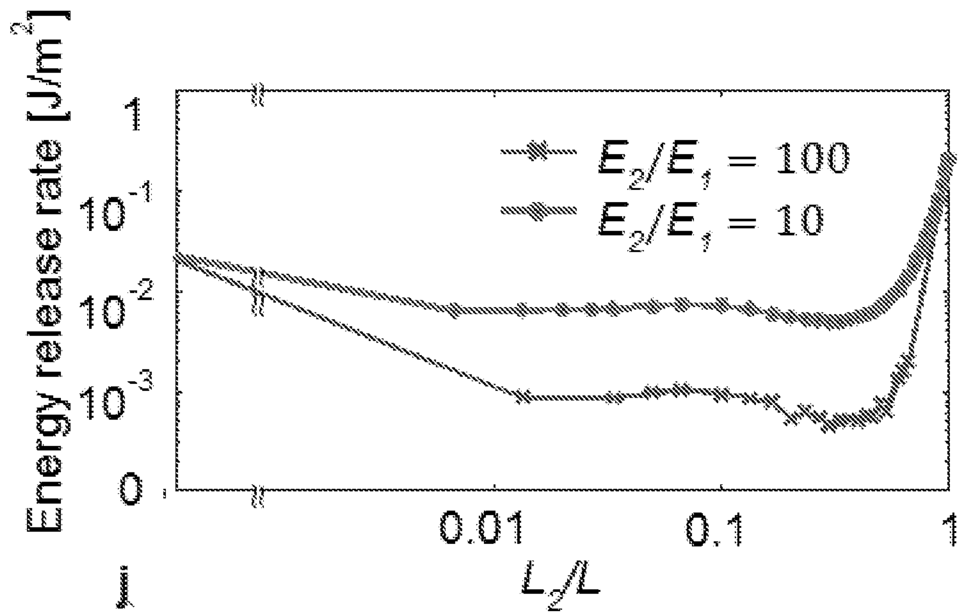

FIG. 4

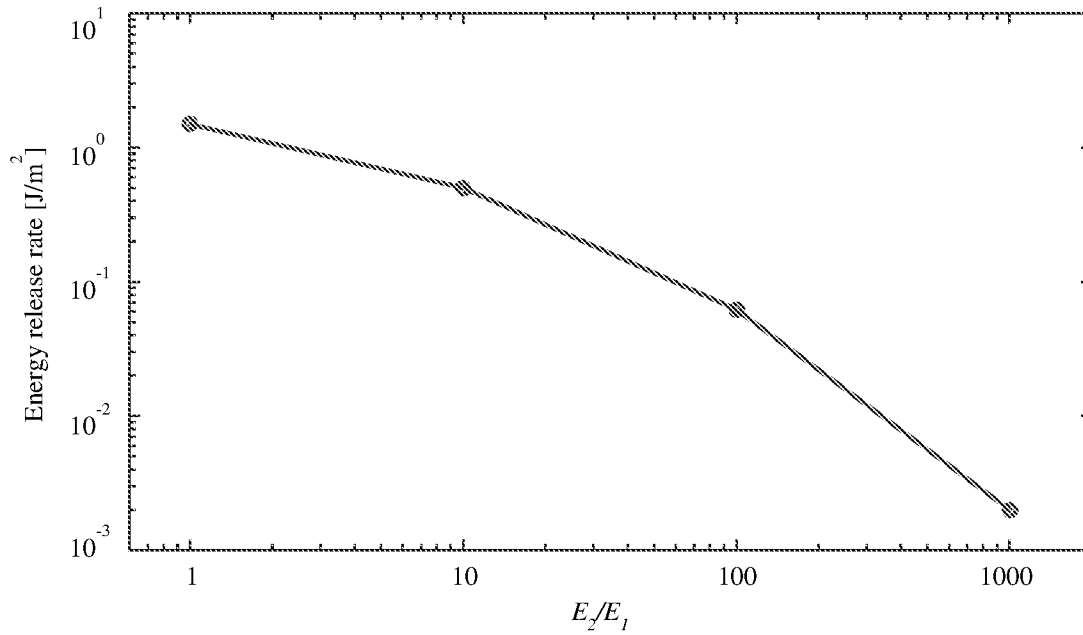

FIG. 5

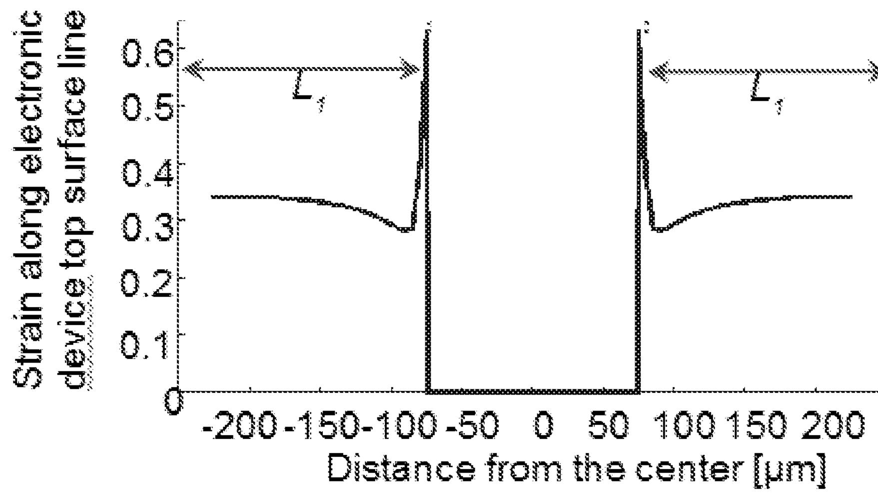

FIG. 6A

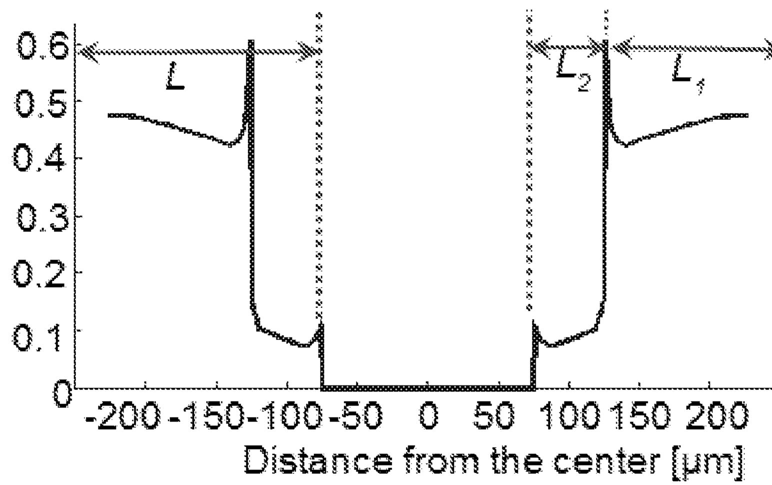

FIG. 6B

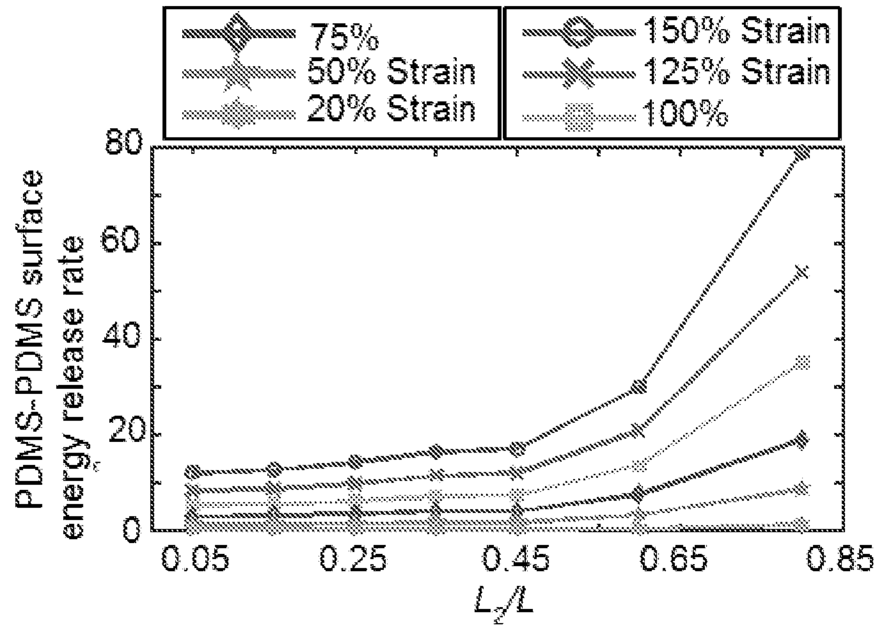

FIG. 7A

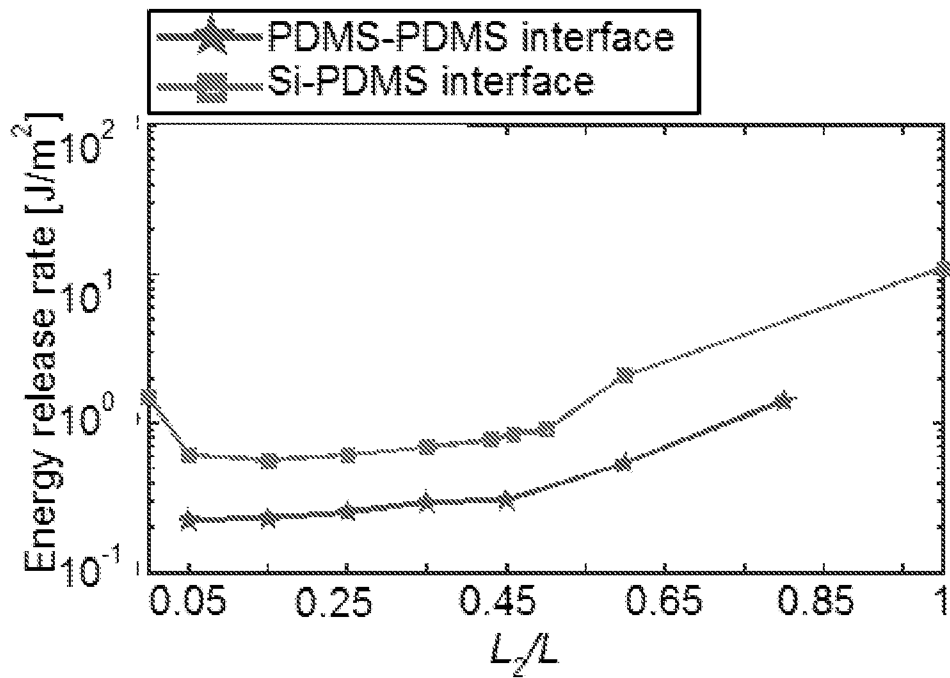

FIG. 7B

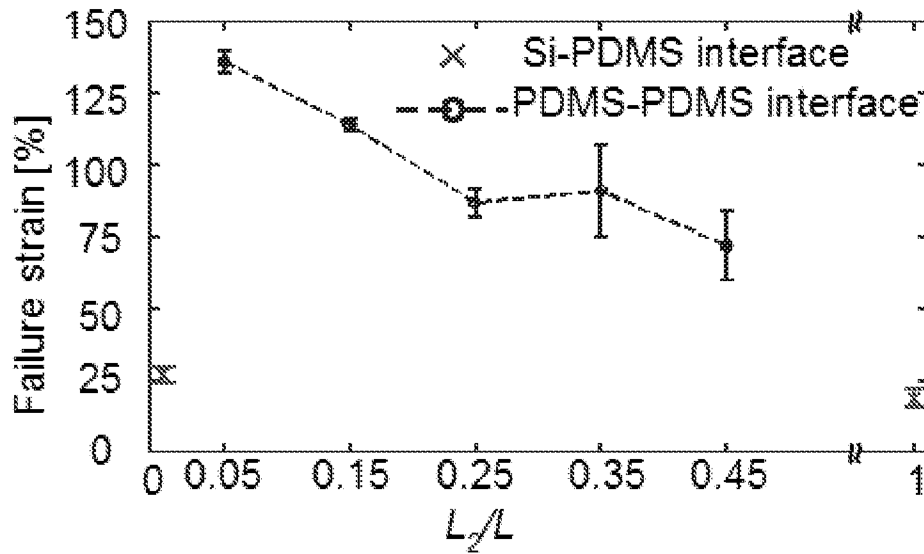

FIG. 8

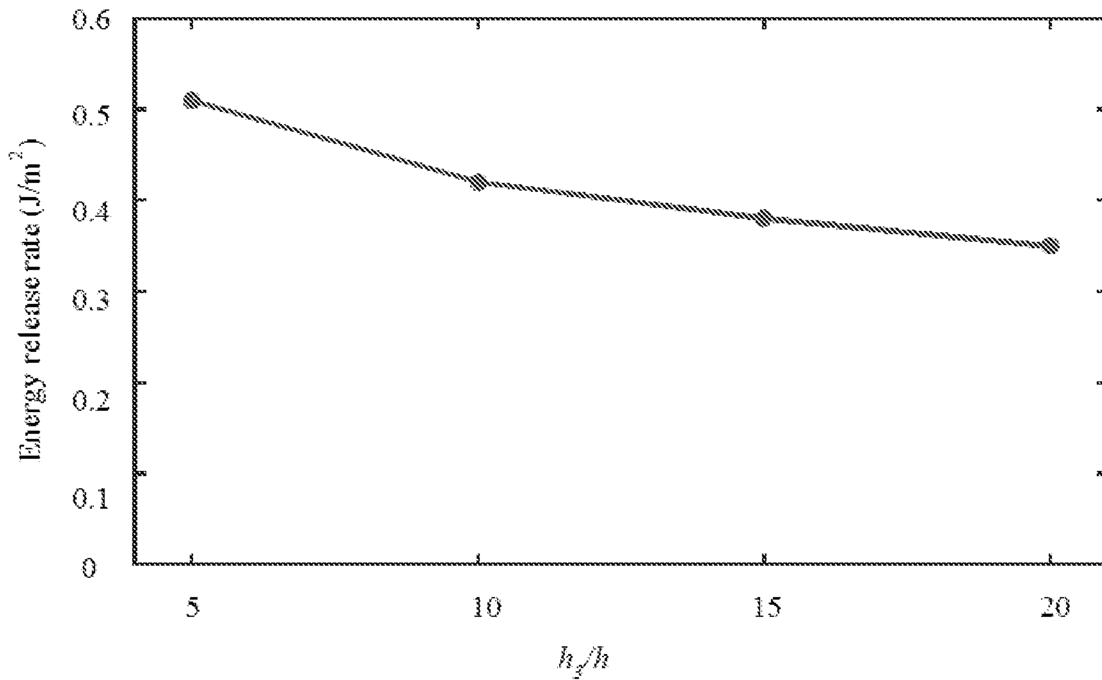

FIG. 9

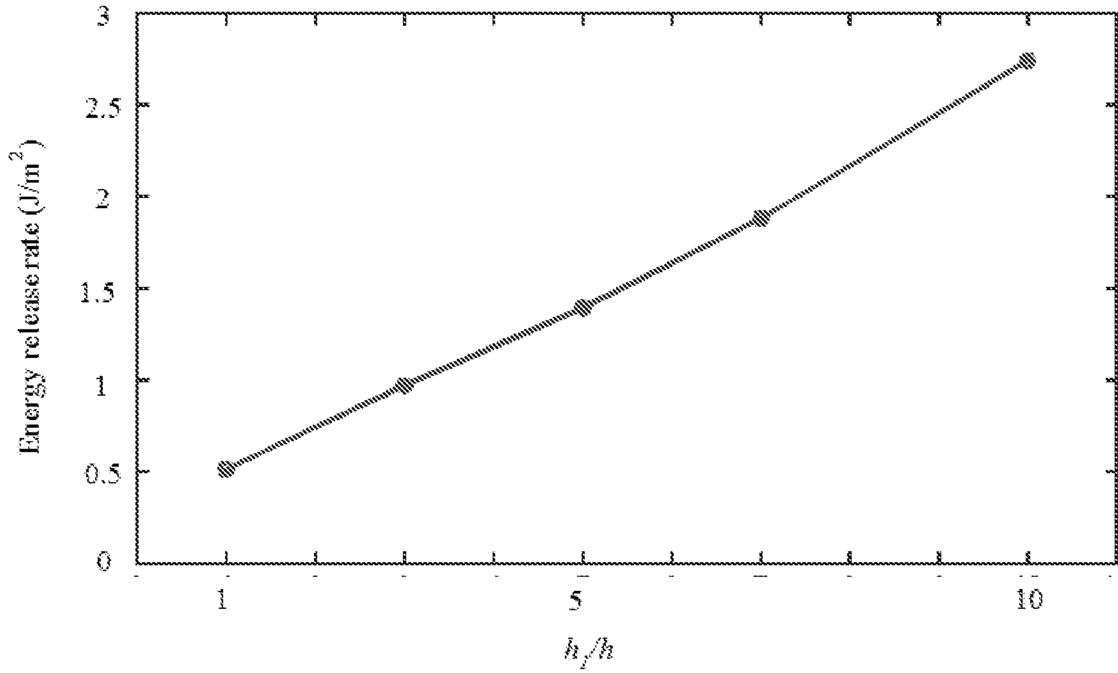

FIG. 10

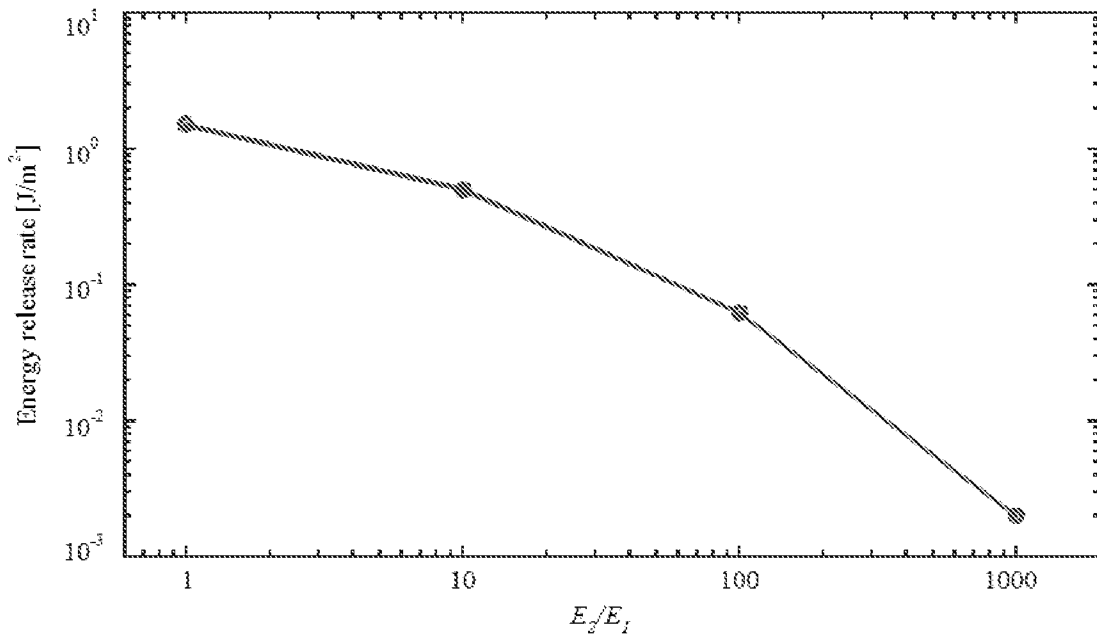

FIG. 11

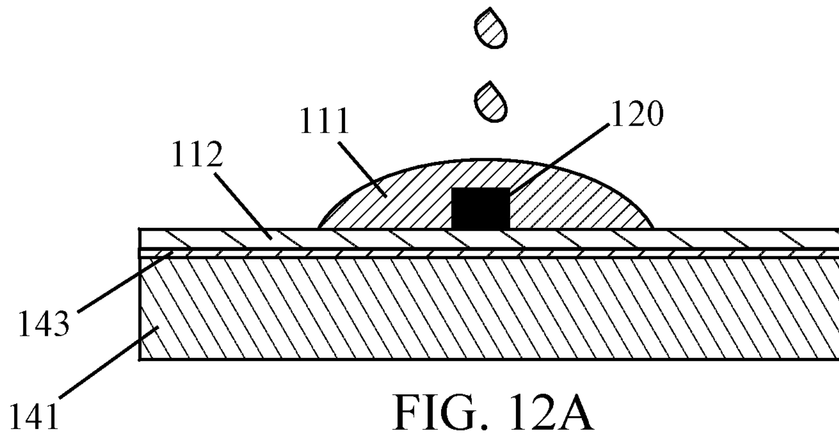

FIG. 12A

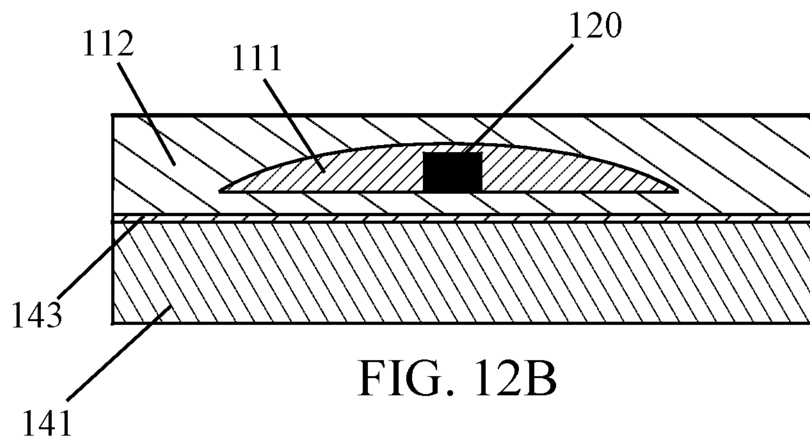

FIG. 12B

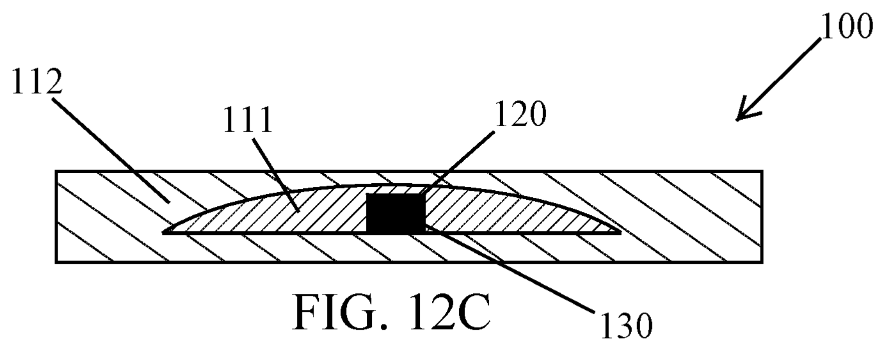

FIG. 12C

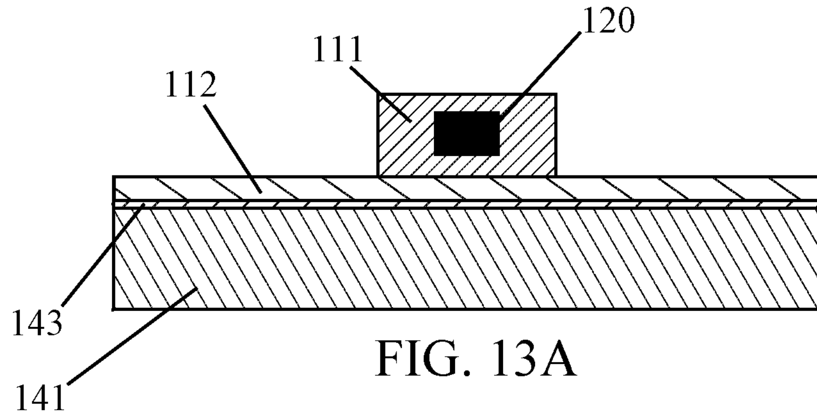

FIG. 13A

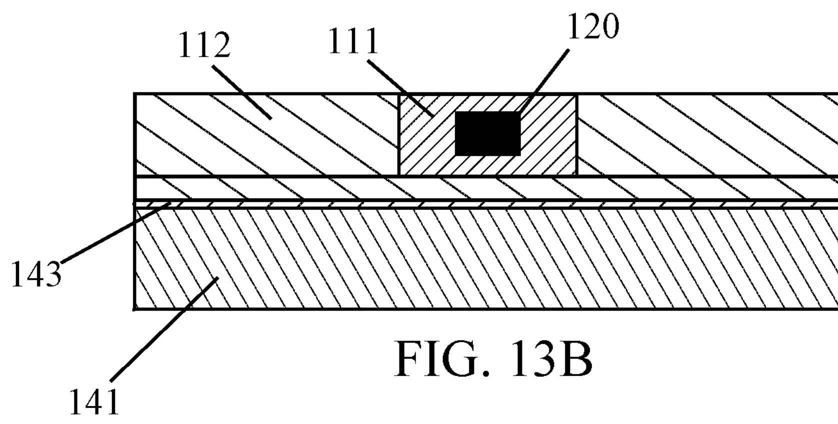

FIG. 13B

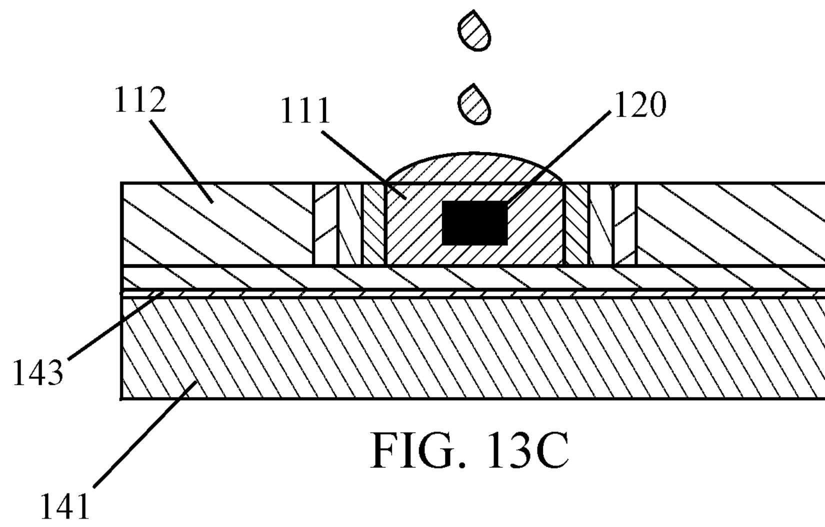

FIG. 13C

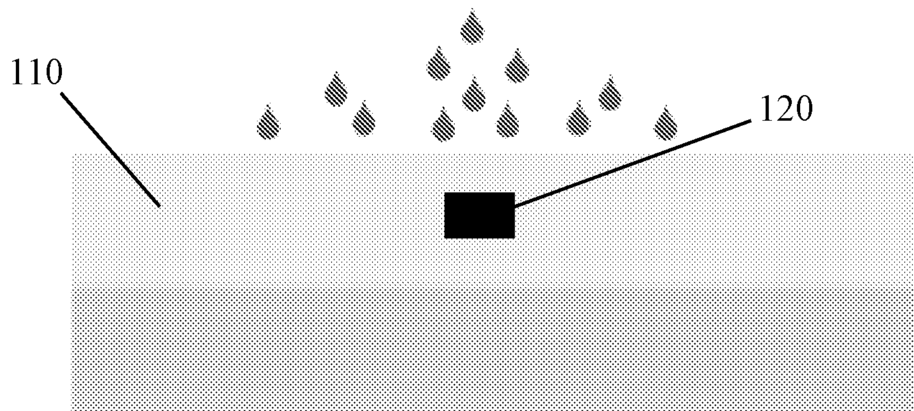

FIG. 14A

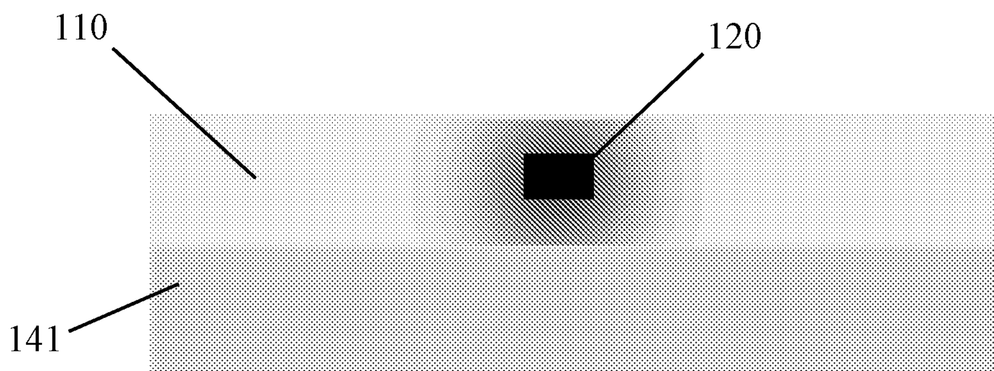

FIG. 14B

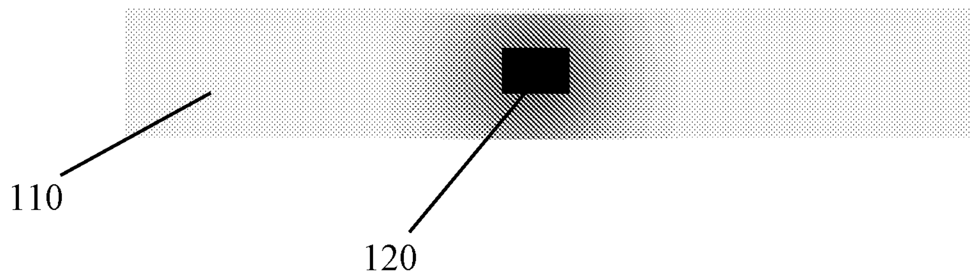

FIG. 14C

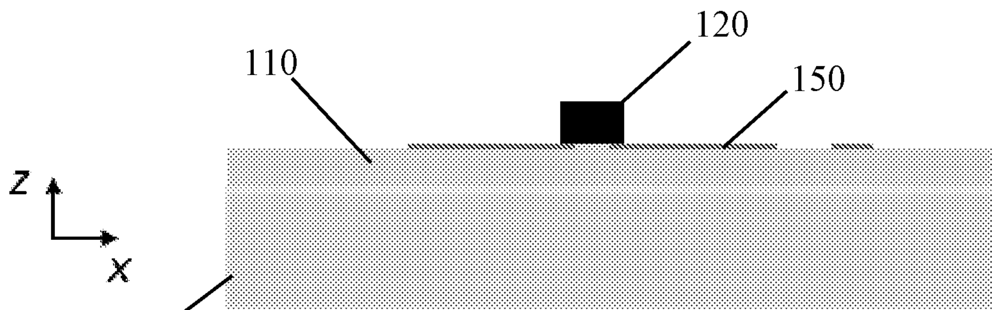

FIG. 15A

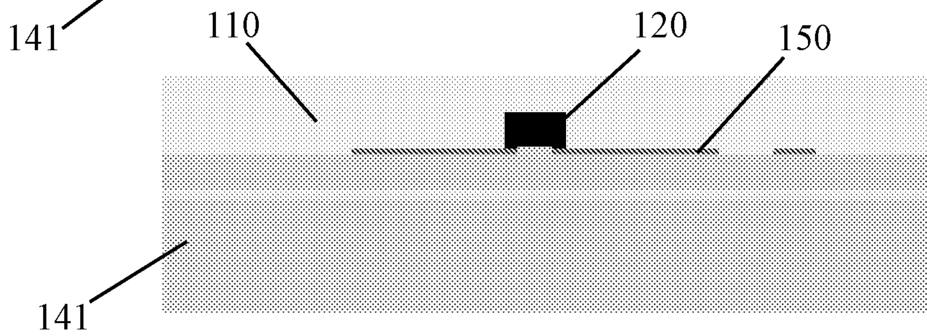

FIG. 15B

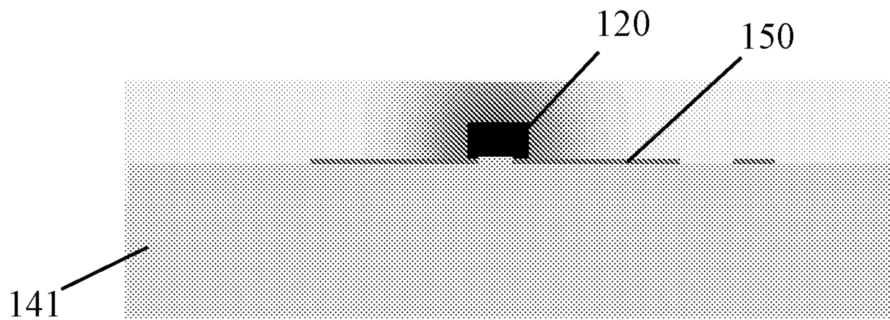

FIG. 15C

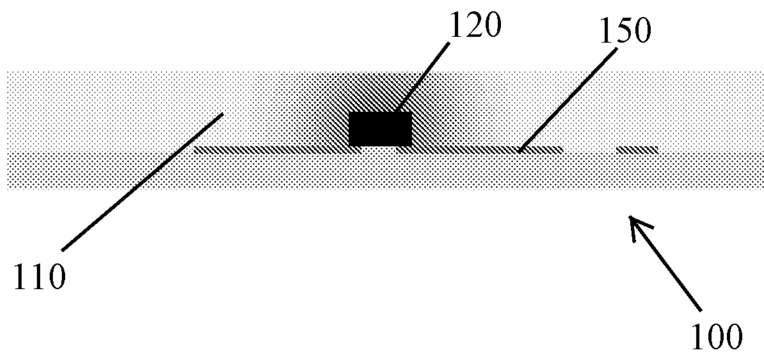

FIG. 15D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US17/21974

A. CLASSIFICATION OF SUBJECT MATTER
IPC - A41D 1/00; A61B 5/00, 5/0402; B29C 33/40; H01L 23/28, 21/56; H05K 1/02 (2017.01)
CPC - A41D 1/005, 1/002, 13/1281, 13/1236; A61B 5/6801, 5/0408, 5/0082, 5/0245, 5/02444; B29C 33/405; H01L 21/02518, 21/02521, 24/01, 23/4985, 23/3192, 27/1292, 23/5387; H05K 1/189, 1/0277, 1/0283

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015/0001462 A1 (THE BOARD OF TRUSTEES OF THE UNIVERSITY OF ILLINOIS) January 1, 2015; paragraphs [0081], [0095], [0104], [0107], [0121], [0123]	1-5
A	US 2014/0240932 A1 (MC10, INC.) August 28, 2014; figure 2a; paragraphs [0060], [0061] & [0067]	1-5
A	US 2016/0045162 A1 (MC10, INC.) February 18, 2016; paragraphs [0094], [0114]-[0115], [0154] & [0222]	1-5
A	US 2014/0110859 A1 (MC10, INC.) April 24, 2014; figures 3A & 3B; paragraphs [0098], [0127]-[0132]	1-5
A	US 2015/0099976 A1 (MC10, INC.) April 9, 2015; paragraph [0077], [0092], [0110]	1-5
E, X	US 2017/0181275 A1 (INTEL CORPORATION) June 22, 2017; paragraph [0087]-[0093]; claim 1	1-5
A	US 2010/0083489 A1 (ELDRIDGE, B et al.) April 8, 2010; entire document	1-5

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 June 2017 (28.06.2017)	19 JUL 2017

Name and mailing address of the ISA/	Authorized officer
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US17/21974

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See attached sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-5

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

-***-Continued from Box III: Observations where unity of invention is lacking-***-

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-5 appear to be directed towards applying a curing agent to a first area of a substrate.
Group II: Claims 6-10 appear to be directed towards a stiffness gradient.

The inventions listed as Groups I & II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features.

The special technical features of Group I are at least applying a curing agent to a first area of the substrate adjacent to the rigid electronic device; and applying the curing agent to a second area of the substrate, wherein the curing agent creates a portion of the substrate adjacent the embedded electronic device with a modulus in between a modulus of a portion of the substrate not adjacent to the embedded electronic device and the modulus of the rigid electronic device, which are not present in Group II.

The special technical features of Group II are wherein the substrate has a stiffness gradient with a maximum stiffness adjacent a rigid electronic device, which are not present in Group I.

The common technical features of Groups I and II are an integrated electronic device comprising: a substrate having a stiffness gradient, wherein the rigid electronic device is embedded in the substrate.

US 2010/0083489 A1 to Eldridge, B et al. (ELDRIDGE) discloses an integrated electronic device comprising: a substrate having a stiffness gradient, wherein a rigid electronic device is embedded in the substrate (a uniform electronic device having a column with a stiffness gradient, the column is between two rigid substrates; figure 2A, paragraph [0088]).

Since the common technical features are previously disclosed by ELDRIDGE, they are not special and Groups I and II lack unity.