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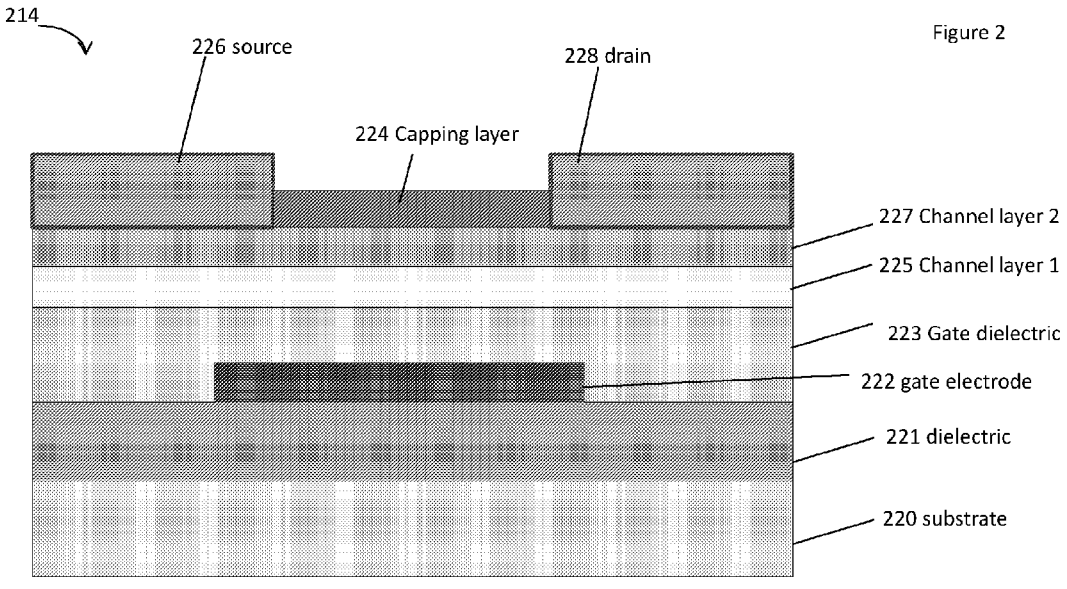

Figure 2

(57) Abstract: Embodiments herein describe techniques for a semiconductor device including a TFT having high mobility, while keeping the leakage low. Embodiments may include a gate electrode above a substrate, a first channel layer including a first material above the gate electrode, and a second channel layer including a second material above the first channel layer, wherein the first material may have a higher mobility than the second material, and the second material may have a lower leakage than the first material. Embodiments may further include a source electrode and a drain electrode above the second channel layer. Other embodiments may be described and/or claimed.

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THIN FILM TRANSISTORS WITH MULTIPLE CHANNEL LAYERS

Field

Embodiments of the present disclosure generally relate to the field of integrated circuits, and more particularly, to transistors.

Background

A memory device, e.g., a dynamic random access memory (DRAM) array, may include a plurality of memory cells, where a memory cell may include a selector, e.g., a transistor, to control the access to a storage cell. When a silicon transistor is used as a selector, the silicon transistor may be very leaky, which may bring adverse impact to the performance of the storage cell. For example, when the storage cell is a capacitor, a relatively large capacitor may be used to store enough charge for the storage cell due to the leakage of the transistor as a selector, which may take up a significant substrate area. Sometimes, a large capacitor may be implemented by creating a deep trench in a silicon substrate, making the process non-CMOS compatible.

A thin-film transistor (TFT) is a kind of field-effect transistor including a channel layer, a gate electrode, and source and drain electrodes, over a supporting but non-conducting substrate. A TFT differs from a conventional transistor, where a channel of the conventional transistor is typically within a substrate, such as a silicon substrate. TFTs have emerged as an attractive option to fuel Moore's law by integrating TFTs vertically in the back-end, while leaving the silicon substrate areas for high-speed transistors. A TFT may be used as a selector for a memory cell in a memory device. However, a TFT may often have low mobility. When a TFT is used as a selector for a memory cell, high mobility may be desired for the TFT. On the other hand, a high mobility TFT may have higher leakage. Hence, it is often difficult to have a TFT that has high mobility and low leakage at the same time.

Brief Description of the Drawings

Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

Figure 1 schematically illustrates a memory array with multiple memory cells wherein a thin-film transistor (TFT) may be a selector of a memory cell, in accordance with various embodiments.

Figure 2 schematically illustrates a diagram of a TFT having multiple channel layers including a high mobility layer and a low leakage layer, in accordance with some embodiments.

Figure 3 schematically illustrates a diagram of another TFT having multiple channel layers including a high mobility layer and a low leakage layer, in accordance with some embodiments.

Figure 4 schematically illustrates a diagram of a memory cell including a TFT coupled to a storage cell, wherein the TFT has multiple channel layers including a high mobility layer and a low leakage layer, in accordance with some embodiments.

Figure 5 illustrates a process for forming a TFT having multiple channel layers including a high mobility layer and a low leakage layer, in accordance with some embodiments.

Figure 6 schematically illustrates an interposer implementing one or more embodiments of the disclosure, in accordance with some embodiments.

Figure 7 schematically illustrates a computing device built in accordance with an embodiment of the disclosure, in accordance with some embodiments.

Figure 8 schematically illustrates a diagram of a TFT having multiple channel layers including a high mobility layer and a low leakage layer formed in back-end-of-line (BEOL) on a substrate, in accordance with some embodiments.

Detailed Description

A memory cell in a memory device, e.g., a memory array, may include a selector, e.g., a transistor, to control the access to a storage cell. In embodiments, the storage cell may be a capacitor to store charge, resulting in a 1T1C (one transistor, one capacitor) architecture for the memory cell, or a resistive random access memory (RRAM) storage cell, resulting in a 1T1R (one transistor, one resistive cell) architecture for the memory cell. A thin-film transistor (TFT) may be used as a selector of a memory cell. Typically, a TFT may have low leakage or high mobility, but not both. A TFT with low mobility may be useful for low power applications, e.g., displays. However, when used as a selector for a memory cell, it is desirable for a TFT to have high mobility, while keeping the leakage low.

Embodiments herein may present techniques to form a TFT having multiple channel layers including a high mobility layer and a low leakage layer, so that the TFT may have high mobility while keeping the leakage low. Embodiments herein may present

TFTs having multiple channel layers including a high mobility layer and a low leakage layer. As a result, the TFTs may be used as selectors for memory cells with improved performance. For example, a TFT presented herein may improve gate length scaling without increasing off current for the TFT. Other advantages for the TFT presented herein may include: low off current and high drive current which may be useful for memory devices, tuning and controlling of work function and threshold voltage of the TFT based on different channel layers, doping-friendly layers either exposed or buried as a buffer layer, and formation of backside surface charge to mitigate short channel effects.

Embodiments herein may present a semiconductor device, which may include a gate electrode above a substrate. Multiple channel layers may be above the gate electrode. For example, the semiconductor device may include a first channel layer including a first material above the gate electrode and a second channel layer including a second material above the first channel layer. In embodiments, the first material may be a high mobility material and the second material may be a low leakage material. For example, the first material may have higher mobility than the second material, and the second material may have lower leakage than the first material. The semiconductor device may further include a source electrode and a drain electrode above the second channel layer. In embodiments, the semiconductor device may have high mobility, while keeping the leakage low.

Embodiments herein may present a computing device, which may include a circuit board, and a memory device coupled to the circuit board and including a memory array. In more detail, the memory array may include a plurality of memory cells, wherein a memory cell of the plurality of memory cells may include a transistor and a storage cell. In embodiments, the transistor may include a gate electrode coupled to a word line of the memory array. Furthermore, the transistor may include a first channel layer including a first material above the gate electrode, and a second channel layer including a second material above the first channel layer. In embodiments, the first material may be a high mobility material and the second material may be a low leakage material. For example, the first material may have higher mobility than the second material, and the second material may have lower leakage than the first material. The transistor may further include a source electrode above the second channel layer and coupled to a source line of the memory array, and a drain electrode above the second channel layer and coupled to a first electrode of the storage cell. In addition, the storage cell may further include a second electrode coupled to a bit line of the memory array.

In embodiments, a method for forming a semiconductor device may include: forming a gate electrode above a substrate, and forming a gate dielectric layer conformally covering the gate electrode and the substrate. The method may further include: forming a first channel layer including a first material above the gate dielectric layer, and forming a second channel layer including a second material above the first channel layer. In embodiments, the first material may be a high mobility material and the second material may be a low leakage material. For example, the first material may have higher mobility than the second material, and the second material may have lower leakage than the first material. Furthermore, the method may include forming a source electrode and a drain electrode above the second channel layer. In embodiments, the semiconductor device formed by the method may have high mobility, while keeping the leakage low.

In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure. However, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation.

For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

The terms "over," "under," "between," "above," and "on" as used herein may refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers.

Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening features.

The description may use the phrases "in an embodiment," or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous.

The term "coupled with," along with its derivatives, may be used herein. "Coupled" may mean one or more of the following. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or more elements indirectly contact each other, but yet still cooperate or interact with each other, and may mean that one or more other elements are coupled or connected between the elements that are said to be coupled with each other. The term "directly coupled" may mean that two or more elements are in direct contact.

In various embodiments, the phrase "a first feature formed, deposited, or otherwise disposed on a second feature" may mean that the first feature is formed, deposited, or disposed over the second feature, and at least a part of the first feature may be in direct contact (e.g., direct physical and/or electrical contact) or indirect contact (e.g., having one or more other features between the first feature and the second feature) with at least a part of the second feature.

Where the disclosure recites "a" or "a first" element or the equivalent thereof, such disclosure includes one or more such elements, neither requiring nor excluding two or more such elements. Further, ordinal indicators (e.g., first, second, or third) for identified elements are used to distinguish between the elements, and do not indicate or imply a required or limited number of such elements, nor do they indicate a particular position or order of such elements unless otherwise specifically stated.

As used herein, the term "circuitry" may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group), and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable hardware components that provide the described functionality. As used herein, "computer-implemented method" may refer to any method executed by one or more

processors, a computer system having one or more processors, a mobile device such as a smartphone (which may include one or more processors), a tablet, a laptop computer, a set-top box, a gaming console, and so forth.

Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the disclosure may also be carried out using nonplanar transistors.

Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some

embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type work function metal or N-type work function metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a work function that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a work function that is between about 3.9 eV and about 4.2 eV.

In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming

sidewall spacers are well known in the art and generally include deposition and etching process operations. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

Figure 1 schematically illustrates a memory array 100 with multiple memory cells (e.g., a memory cell 102, a memory cell 104, a memory cell 106, and a memory cell 108), wherein a TFT, e.g., a TFT 114, may be a selector of a memory cell, e.g., the memory cell 102, in accordance with various embodiments.

In embodiments, the multiple memory cells may be arranged in a number of rows

and columns coupled by bit lines, e.g., bit line B1 and bit line B2, word lines, e.g., word line W1 and word line W2, and source lines, e.g., source line S1 and source line S2. The memory cell 102 may be coupled in series with the other memory cells of the same row, and may be coupled in parallel with the memory cells of the other rows. The memory array 100 may include any suitable number of one or more memory cells. Although the memory array 100 is shown in Figure 1 with two rows that each includes two memory cells coupled in series, other embodiments may include other numbers of rows and/or numbers of memory cells within a row. In some embodiments, the number of rows may be different from the number of columns in a memory array. Each row of the memory array may have a same number of memory cells. Additionally, or alternatively, different rows may have different numbers of memory cells.

In some embodiments, multiple memory cells, such as the memory cell 102, the memory cell 104, the memory cell 106, and the memory cell 108, may have a similar configuration, such as the 1T1C configuration. For example, the memory cell 102 may include the TFT 114 coupled to a storage cell 112 that may be a capacitor. A memory cell with the 1T1C configuration, e.g., the memory cell 102, may be controlled through multiple electrical connections to read from the memory cells, write to the memory cells, and/or perform other memory operations. In some other embodiments, the storage cell 112 may be another type of storage device, e.g., a RRAM cell, resulting in the 1T1R architecture for the memory cell 102.

In embodiments, when the storage cell 112 is a capacitor, the storage cell 112 may be switchable between charged or discharged states upon application of an electric current or voltage. The charged or discharged states of the storage cell 112 may be taken to represent the two values of a bit, conventionally called 0 and 1. The storage cell 112 may be individually controllable by the TFT 114 as a selector to switch between the charged or discharged states.

In embodiments, when the storage cell 112 is a RRAM cell, the storage cell 112 may be switchable between two or more resistance values upon application of an electric current or voltage. For example, the storage cell 112 may have a first resistance value to store a logic 0, and may have a second resistance value to store a logic 1. In embodiments, the resistance difference between the two resistance values may be one or more orders of magnitude.

The TFT 114 may be a selector for the memory cell 102. A word line W1 of the memory array 100 may be coupled to a gate electrode 111 of the TFT 114. When the

word line W1 is active, the TFT 114 may select the storage cell 112. A source line S1 of the memory array 100 may be coupled to an electrode 101 of the storage cell 112, while another electrode 107 of the storage cell 112 may be shared with the TFT 114. In addition, a bit line B1 of the memory array 100 may be coupled to another electrode, e.g., an electrode 109 of the TFT 114. The shared electrode 107 may be a source electrode or a drain electrode of the TFT 114, while the electrode 109 may be a drain electrode or a source electrode of the TFT 114. A drain electrode and a source electrode may be used interchangeably herein. Additionally, a source line and a bit line may be used interchangeably herein.

In various embodiments, the memory cells and the transistors, e.g., the memory cell 102 and the TFT 114, included in the memory array 100 may be formed in back-end-of-line (BEOL). For example, the TFT 114 may be illustrated as a TFT 814 shown in Figure 8 at the BEOL. Accordingly, the memory array 100 may be formed in higher metal layers, e.g., metal layer 3 and/or metal layer 4, of the integrated circuit above the active substrate region, and may not occupy the active substrate area that is occupied by conventional transistors or memory devices.

Figure 2 schematically illustrates a diagram of a TFT, e.g., a TFT 214, having multiple channel layers including a high mobility layer, e.g., a first channel layer 225, and a low leakage layer, e.g., a second channel layer 227, in accordance with some embodiments. The TFT 214 may be an example of the TFT 114 in Figure 1. The structure of the TFT 214 may be for illustration purpose only and is not limiting. The TFT 214 may have other configurations including more or fewer layers than are shown in Figure 2.

In embodiments, the TFT 214 may include a substrate 220, a dielectric layer 221 above the substrate 220, a gate electrode 222 above the dielectric layer 221, a gate dielectric layer 223 conformally covering the gate electrode 222 and the substrate 220, the first channel layer 225 above the gate dielectric layer 223, and the second channel layer 227 above the first channel layer 225. In addition, the TFT 214 may include a source electrode 226, a drain electrode 228, and a capping layer 224 above the second channel layer 227, where the drain electrode 228 may be separated from the source electrode 226 by the capping layer 224. In embodiments, there may be other layers, e.g., a top dielectric layer above the source electrode 226, the drain electrode 228, and the capping layer 224, not shown.

In embodiments, the substrate 220 may be a glass substrate, such as soda lime

glass or borosilicate glass, a metal substrate, a plastic substrate, or another suitable substrate. Other inter-metal dielectric layer may be formed on the substrate. The substrate 220 may include an inter-metal dielectric layer, or other devices, not shown for clarity.

In embodiments, the dielectric layer 221, or the capping layer 224, may include a silicon oxide (SiO) film, a silicon nitride (SiN) film, O_3-tetraethylorthosilicate (TEOS), O_3-hexamethyldisiloxane (HMDS), plasma-TEOS oxide layer, or other suitable materials. There may be other dielectric layer for the TFT 214. For example, there may be another dielectric layer above the gate dielectric layer 223, not shown.

In embodiments, the gate electrode 222 may be formed as a single layer or a stacked layer using one or more conductive films including a conductive material. For example, the gate electrode 222 may include gold (Au), platinum (Pt), ruthenium (Ru), iridium (Ir), titanium (Ti), aluminum (Al), copper (Cu), tantalum (Ta), tungsten (W), tantalum nitride (TaN), titanium nitride (TiN), iridium-tantalum alloy (Ir-Ta), indium-tin oxide (ITO), the like, and/or a combination thereof.

In embodiments, the gate dielectric layer 223 may include silicon and oxygen; silicon and nitrogen; yttrium and oxygen; silicon, oxygen, and nitrogen; aluminum and oxygen; hafnium and oxygen; tantalum and oxygen; or titanium and oxygen. For example, the gate dielectric layer 223 may include silicon oxide (SiO_2), silicon nitride (SiN_x), yttrium oxide (Y_2O_3), silicon oxynitride (SiO_xN_y), aluminum oxide (Al_2O_3), hafnium(IV) oxide (HfO_2), tantalum oxide (Ta_2O_5), titanium dioxide (TiO_2), or other dielectric materials.

In embodiments, the first channel layer 225 may include a high mobility (μ) material. A mobility of a material may be a proportionality constant that relates the drift velocity to the electric field strength in a semiconductor. A mobility of a material may gauge how easily current carriers (i.e. electrons, holes) may move through a piece of material. In embodiments, the first channel layer 225 may include a material having a high mobility, e.g., a mobility in a range of about 12cm^2/VS to about 132 cm^2/VS, such as, 25 cm^2/VS. For example, the first channel layer 225 may include indium doped zinc Oxide (IZO), zinc tin oxide (ZTO), amorphous silicon (a-Si), amorphous germanium (a-Ge), low-temperature polycrystalline silicon (LTPS), transition metal dichalcogenide (TMD), yttrium-doped zinc oxide (YZO), or zinc oxide (ZnO), or other similar high mobility materials. In embodiments, the first channel layer 225 may have a thickness in a range of about 0.5 nanometers (nm) to about 20 nm.

In embodiments, the second channel layer 227 may include a low leakage material. For a transistor, a leakage current may refer to a small amount of current that flows (or "leaks") through the transistor when it is "turned off." In an ideal transistor, the leakage current would be zero, but in practice, leakage current may have a finite value larger than zero. In embodiments, the TFT 214 having the second channel layer 227 with a low leakage material may have a low leakage current, e.g., in a range of about 10^{-4} amp to about 10^{-12} amp. For example, the second channel layer 227 may include indium, gallium, zinc, and oxide; molybdenum and sulfur; a group-VI transition metal dichalcogenide, or other low leakage materials. In more detail, the second channel layer 227 may include indium gallium zinc oxide (IGZO), molybdenum disulfide (MoS_2), or tungsten diselenide (WSe_2). The second channel layer 227 may have a thickness in a range of about 0.5 nm to about 20 nm.

In embodiments, the first channel layer 225 may include a material with a higher mobility than a material included in the second channel layer 227. On the other hand, the second channel layer 227 may include a material with a lower leakage than a material included in the first channel layer 225. The TFT 214 including both the first channel layer 225 and the second channel layer 227 may have high mobility, while keeping the leakage low.

In embodiments, the source electrode 226 and the drain electrode 228 may include one or more conductive films including a conductive material. For example, the source electrode 226 and the drain electrode 228 may include Ti, molybdenum (Mo), Au, Pt, Al, nickel (Ni), Cu, chromium (Cr), Ru, iridium (Ir), Ta, W, an alloy of Ti, Mo, Au, Pt, Al, Ni, Cu, Cr, Ru, Ir, Ta, W, or another conductive material.

Figure 3 schematically illustrates a diagram of another TFT, e.g., a TFT 314, having multiple channel layers including a high mobility layer e.g., a first channel layer 325, and a low leakage layer, e.g., a second channel layer 327, in accordance with some embodiments. The TFT 314 may be an example of the TFT 114 in Figure 1. Various layers in the TFT 314 may be similar to corresponding layers in the TFT 214 in Figure 2. The structure of the TFT 314 may be for illustration purpose only and is not limiting.

In embodiments, the TFT 314 may include a substrate 320, a dielectric layer 321 above the substrate 320, a gate electrode 322 above the dielectric layer 321, a gate dielectric layer 323 conformally covering the gate electrode 322 and the substrate 320, the first channel layer 325 above the gate dielectric layer 323, and the second channel layer 327 above the first channel layer 325. In addition, the TFT 314 may include a buffer layer

329 between the first channel layer 325 and the second channel layer 327. Furthermore, a source electrode 326, a drain electrode 328, and a capping layer 324 may be above the second channel layer 327, where the drain electrode 328 may be separated from the source electrode 326 by the capping layer 324. In embodiments, there may be other layers, e.g., a top dielectric layer above the source electrode 326, the drain electrode 328, and the capping layer 324, not shown.

In embodiments, the first channel layer 325 may include a high mobility (μ) material, similar to the first channel layer 225 in Figure 2, while the second channel layer 327 may include a low leakage material, similar to the second channel layer 227 in Figure 2. In embodiments, the first channel layer 325 may include a material with a higher mobility than a material included in the second channel layer 327. On the other hand, the second channel layer 327 may include a material with a lower leakage than a material included in the first channel layer 325. The TFT 314 including both the first channel layer 325 and the second channel layer 327 may have high mobility, while keeping the leakage low.

The buffer layer 329 may be between the first channel layer 325 and the second channel layer 327, providing lattice matching between the high mobility material for the first channel layer 325 and the low leakage material for the second channel layer 327. For example, the buffer layer 329 may include indium doped zinc and oxygen. The buffer layer 329 may have a thickness in a range of about 0.5 nm to about 20 nm.

Figure 4 schematically illustrates a diagram of a memory cell, e.g., a memory cell 402, including a TFT, e.g., a TFT 414, coupled to a storage cell, e.g., a storage cell 412, wherein the TFT has multiple channel layers including a high mobility layer and a low leakage layer, in accordance with some embodiments. The memory cell 402 may be an example of the memory cell 102 in Figure 1, while the TFT 414 may be an example of the TFT 114 in Figure 1. Various layers in the TFT 414 may be similar to corresponding layers in the TFT 214 in Figure 2. The structure of the TFT 414 and the memory cell 402 may be for illustration purpose only and is not limiting.

In embodiments, the TFT 414 may include a substrate 420, a dielectric layer 421 above the substrate 420, a gate electrode 422 above the dielectric layer 421, a gate dielectric layer 423 conformally covering the gate electrode 422 and the substrate 420, a first channel layer 425 above the gate dielectric layer 423, and a second channel layer 427 above the first channel layer 425. In embodiments, the first channel layer 425 may include a high mobility (μ) material, similar to the first channel layer 225 in Figure 2,

while the second channel layer 427 may include a low leakage material, similar to the second channel layer 227 in Figure 2. In embodiments, the first channel layer 425 may include a material with a higher mobility than a material included in the second channel layer 427. On the other hand, the second channel layer 427 may include a material with a lower leakage than a material included in the first channel layer 425. The TFT 414 including both the first channel layer 425 and the second channel layer 427 may have high mobility, while keeping the leakage low.

In addition, the TFT 414 may include a source electrode 426, a drain electrode 428, and a capping layer 424 above the second channel layer 427, where the drain electrode 428 may be separated from the source electrode 426 by the capping layer 424. In embodiments, there may be other layers, e.g., a top dielectric layer above the source electrode 426, the drain electrode 428, and the capping layer 424, not shown. Furthermore, the TFT 414 may further include a buffer layer, similar to the buffer layer 329 as shown in Figure 3.

In embodiments, the storage cell 412 may include a first electrode 431, a second electrode 435, and a resistive switching material layer 433 between the first electrode 431 and the second electrode 435. The first electrode 431 may be coupled to the drain electrode 428 of the TFT 414, while the second electrode 435 may be coupled to a bit line of a memory array, not shown. In addition, the source electrode 426 of the TFT 414 may be coupled to a source line of the memory array, and the gate electrode 422 may be coupled to a word line of the memory array.

In embodiments, the first electrode 431 and/or the second electrode 435 may include Au, Pt, Ru, Ir, Ti, Al, Cu, Ta, W, or an alloy such as Ir-Ta, ITO, TaN, TiN, TiAlN, TiW, Hf, or other conductive material. The thickness of the first electrode 431 and/or the second electrode 435 may be between a range about 100-500 nm.

In embodiments, the resistive switching material layer 433 may include hafnium and oxygen; tantalum and oxygen; hafnium, tantalum and oxygen; tellurium; germanium; silicon; or chalcogenide. For example, the resistive switching material layer 433 may include HfOx, TaOx, HfTaOx, Te, Ge, Si, chalcogenide, a transition metal oxide, or a transition metal chalcogenide. Additionally or alternatively, in some embodiments, the resistive switching material layer 433 may include one or more oxide of W, Ta, Ti, Ni, Co, Hf, Ru, Zr, Zn, Fe, Sn, Al, Cu, Ag, Mo, Cr. In some embodiments, silicon may be included in the resistive switching material layer 433 to form a composite material. The

thickness of the resistive switching material layer 433 may be between a range of about 20 nm to about 100 nm.

In embodiments, the material in the resistive switching material layer 433 may be formed in an initial state with a first resistance value, e.g., a relatively low-resistance state such as 10^5 ohms. When a first voltage, e.g., a set operating voltage, such as 3 V, is applied to the storage cell 412, the resistive switching material layer 433 may switch to a stable second resistance value, e.g., a high-resistance state, such as 10^7 ohms, which is maintained even after the voltage is removed. This resistance switching may be reversible such that subsequent application of an appropriate current or a second voltage can serve to return the resistive material layer 433 to a stable first resistance value which is maintained even after the voltage or current is removed. In some embodiments, the first resistance value may be a high-resistance value rather than a low-resistance value.

Figure 5 illustrates a process 500 for forming a TFT having multiple channel layers including a high mobility layer and a low leakage layer, in accordance with some embodiments. In embodiments, the process 500 may be applied to form the TFT 114 in Figure 1, the TFT 214 in Figure 2, the TFT 314 in Figure 3, or the TFT 414 in Figure 4.

At block 501, the process 500 may include forming a gate electrode above a substrate. For example, the process 500 may include forming the gate electrode 222 above the substrate 220 as shown in Figure 2.

At block 503, the process 500 may include forming a gate dielectric layer conformally covering the gate electrode and the substrate. For example, the process 500 may include forming the gate dielectric layer 223 conformally covering the gate electrode 222 and the substrate 220, as shown in Figure 2. In embodiments, the gate dielectric layer, e.g., the gate dielectric layer 223, may include silicon and oxygen, silicon and nitrogen, yttrium and oxygen, silicon, oxygen, and nitrogen, aluminum and oxygen, hafnium and oxygen, tantalum and oxygen, or titanium and oxygen.

At block 505, the process 500 may include forming a first channel layer including a first material above the gate dielectric layer. For example, the process 500 may include forming the first channel layer 225 above the gate dielectric layer 223, as shown in Figure 2. In embodiments, the first channel layer 225 may include a high mobility material, such as indium doped zinc Oxide (IZO), zinc tin oxide (ZTO), amorphous silicon (a-Si), amorphous germanium (a-Ge), low-temperature polycrystalline silicon (LTPS), transition metal dichalcogenide (TMD), yttrium-doped zinc oxide (YZO), or zinc oxide (ZnO).

At block 507, the process 500 may include forming a second channel layer

including a second material above the first channel layer. For example, the process 500 may include forming the second channel layer 227 above the first channel layer 225, as shown in Figure 2. In embodiments, the second channel layer formed at the block 507 may include a low leakage material, such as indium, gallium, zinc, and oxide; molybdenum and sulfur; a group-VI transition metal dichalcogenide, or other low leakage materials. As a result, the TFT with the low leakage material may have a low leakage current, e.g., in a range of about 10^{-4} amp to about 10^{-12} amp. Furthermore, the first channel layer formed at the block 505 may include a material with a higher mobility than a material included in the second channel layer formed at the block 507. On the other hand, the second channel layer formed at the block 507 may include a material with a lower leakage than a material included in the first channel layer formed at the block 505. The TFT including both the first channel layer formed at the block 505 and the second channel layer formed at the block 507 may have high mobility, while keeping the leakage low.

At block 509, the process 500 may include forming a source electrode and a drain electrode above the second channel layer. For example, the process 500 may include forming the source electrode 226 and the drain electrode 228 above the second channel layer 227. The source electrode 226 or the drain electrode 228 may include Au, Pt, Ru, Ir, Ti, Al, Cu, Ta, W, Ir-Ta, or ITO.

In addition, the process 500 may include additional operations. For example, the process 500 may include forming a buffer layer between the first channel layer and the second channel layer, e.g., the buffer layer 329 shown in Figure 3. Furthermore, the process 500 may include forming a capping layer between the source electrode and the drain electrode and above the second channel layer.

Figure 6 illustrates an interposer 600 that includes one or more embodiments of the disclosure. The interposer 600 is an intervening substrate used to bridge a first substrate 602 to a second substrate 604. The first substrate 602 may be, for instance, a substrate support for a TFT, e.g., the TFT 114 shown in Figure 1, the TFT 214 shown in Figure 2, the TFT 314 shown in Figure 3, or the TFT 414 shown in Figure 4. The second substrate 604 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. For example, the second substrate 604 may be a memory module including the memory array 100 as shown in Figure 1. Generally, the purpose of an interposer 600 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 600 may couple an integrated circuit die

to a ball grid array (BGA) 606 that can subsequently be coupled to the second substrate 604. In some embodiments, the first and second substrates 602/604 are attached to opposing sides of the interposer 600. In other embodiments, the first and second substrates 602/604 are attached to the same side of the interposer 600. And in further embodiments, three or more substrates are interconnected by way of the interposer 600.

The interposer 600 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 608 and vias 610, including but not limited to through-silicon vias (TSVs) 612. The interposer 600 may further include embedded devices 614, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 600.

In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer 600.

Figure 7 illustrates a computing device 700 in accordance with one embodiment of the disclosure. The computing device 700 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die, such as a SoC used for mobile devices. The components in the computing device 700 include, but are not limited to, an integrated circuit die 702 and at least one communications logic unit 708. In some implementations the communications logic unit 708 is fabricated within the integrated circuit die 702 while in other implementations the communications logic unit 708 is fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 702. The integrated circuit die 702 may include a processor 704 as well as on-die memory 706, often used as cache memory, which can be provided by technologies such as embedded DRAM (eDRAM), or SRAM. For example, the on-die memory 706 may include the TFT 114 shown in Figure

1, the TFT 214 shown in Figure 2, the TFT 314 shown in Figure 3, the TFT 414 shown in Figure 4, or a TFT formed according to the process 500 shown in Figure 5.

In embodiments, the computing device 700 may include a display or a touchscreen display 724, and a touchscreen display controller 726. A display or the touchscreen display 724 may include a FPD, an AMOLED display, a TFT LCD, a micro light-emitting diode (μLED) display, or others. For example, the touchscreen display 724 may include the TFT 114 shown in Figure 1, the TFT 214 shown in Figure 2, the TFT 314 shown in Figure 3, the TFT 414 shown in Figure 4, or a TFT formed according to the process 500 shown in Figure 5.

Computing device 700 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within a SoC die. These other components include, but are not limited to, volatile memory 710 (e.g., dynamic random access memory (DRAM), non-volatile memory 712 (e.g., ROM or flash memory), a graphics processing unit 714 (GPU), a digital signal processor (DSP) 716, a crypto processor 742 (e.g., a specialized processor that executes cryptographic algorithms within hardware), a chipset 720, at least one antenna 722 (in some implementations two or more antenna may be used), a battery 730 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 728, a compass, a motion coprocessor or sensors 732 (that may include an accelerometer, a gyroscope, and a compass), a microphone (not shown), a speaker 734, a camera 736, user input devices 738 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 740 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). The computing device 700 may incorporate further transmission, telecommunication, or radio functionality not already described herein. In some implementations, the computing device 700 includes a radio that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space. In further implementations, the computing device 700 includes a transmitter and a receiver (or a transceiver) that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space.

The communications logic unit 708 enables wireless communications for the transfer of data to and from the computing device 700. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the

associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 708 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Infrared (IR), Near Field Communication (NFC), Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 700 may include a plurality of communications logic units 708. For instance, a first communications logic unit 708 may be dedicated to shorter range wireless communications such as Wi-Fi, NFC, and Bluetooth and a second communications logic unit 708 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 704 of the computing device 700 includes one or more devices, such as transistors. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The communications logic unit 708 may also include one or more devices, such as transistors.

In further embodiments, another component housed within the computing device 700 may contain one or more devices, such as DRAM, that are formed in accordance with implementations of the current disclosure, e.g., the memory array 100 shown in Figure 1, the TFT 114 shown in Figure 1, the TFT 214 shown in Figure 2, the TFT 314 shown in Figure 3, the TFT 414 shown in Figure 4, or a TFT formed according to the process 500 shown in Figure 5.

In various embodiments, the computing device 700 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a dumbphone, a tablet, a tablet/laptop hybrid, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 700 may be any other electronic device that processes data.

Figure 8 schematically illustrates a diagram of the TFT 814 having multiple channel layers including a high mobility layer and a low leakage layer formed in BEOL on a substrate 820, in accordance with some embodiments. The TFT 814 may be an example of the TFT 114 in Figure 1, an example of the TFT 214 in Figure 2, or an

example of the TFT 314 in Figure 3. Various layers in the TFT 814 may be similar to corresponding layers in the TFT 214 in Figure 2, or the TFT 314 in Figure 3. The structure of the TFT 814 may be for illustration purpose only and is not limiting.

In embodiments, the TFT 814 may be formed on the substrate 820, and may include a dielectric layer 821 above the substrate 820, a gate electrode 822 above the dielectric layer 821, a gate dielectric layer 823 conformally covering the gate electrode 822 and the substrate 820, a first channel layer 825 above the gate dielectric layer 823, and a second channel layer 827 above the first channel layer 825. In embodiments, the first channel layer 825 may be similar to the first channel layer 225 shown in Figure 2, and may include a high mobility (μ) material, while the second channel layer 827 may be similar to the first channel layer 227 shown in Figure 2, and may include a low leakage material. In addition, the TFT 814 may include a buffer layer, not shown, between the first channel layer 825 and the second channel layer 827. Furthermore, a source electrode 826, a drain electrode 828, and a capping layer 824 may be above the second channel layer 827, where the drain electrode 828 may be separated from the source electrode 826 by the capping layer 824. In embodiments, there may be other layers, e.g., a top dielectric layer above the source electrode 826, the drain electrode 828, and the capping layer 824, not shown.

In embodiments, the TFT 814 may be formed at the BEOL 840. In addition to the TFT 814, the BEOL 840 may further include a dielectric layer 810, where one or more vias, e.g., a via 818, may be connected to one or more interconnect, e.g., an interconnect 816, and an interconnect 812 within the dielectric layer 810. In embodiments, the interconnect 816 and the interconnect 812 may be of different metal layers at the BEOL 840. The dielectric layer 810 is shown for example only. Although not shown by Figure 8, in various embodiments there may be multiple dielectric layers included in the BEOL 840.

In embodiments, the BEOL 840 may be formed on the front-end-of-line (FEOL) 830. The FEOL 830 may include the substrate 820. In addition, the FEOL 830 may include other devices, e.g., a transistor 834. In embodiments, the transistor 834 may be a FEOL transistor, including a source 811, a drain 813, and a gate 815, with a channel 817 between the source 811 and the drain 813 under the gate 815. Furthermore, the transistor 834 may be coupled to interconnects, e.g., the interconnect 812, through a via 819.

The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the

disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

Some non-limiting Examples are provided below.

Example 1 may include a thin film transistor (TFT), comprising: a gate electrode above a substrate; a first channel layer including a first material above the gate electrode; a second channel layer including a second material above the first channel layer, wherein the first material has a higher mobility than the second material, and the second material has a lower leakage than the first material; a source electrode above the second channel layer; and a drain electrode above the second channel layer.

Example 2 may include the TFT of example 1 and/or some other examples herein, wherein the first material includes indium doped zinc Oxide (IZO), zinc tin oxide (ZTO), amorphous silicon (a-Si), amorphous germanium (a-Ge), low-temperature polycrystalline silicon (LTPS), transition metal dichalcogenide (TMD), yttrium-doped zinc oxide (YZO), or zinc oxide (ZnO).

Example 3 may include the TFT of example 1 and/or some other examples herein, wherein the first channel layer has a thickness in a range of 0.5 nanometers (nm) – 20 nm, and the second channel layer has a thickness in a range of 0.5 nm – 20 nm.

Example 4 may include the TFT of example 1 and/or some other examples herein, wherein the second material includes indium, gallium, zinc, and oxide; molybdenum and sulfur; or a group-VI transition metal dichalcogenide.

Example 5 may include the TFT of example 1 and/or some other examples herein, further comprising a buffer layer between the first channel layer and the second channel layer.

Example 6 may include the TFT of example 5 and/or some other examples herein, wherein the buffer layer includes indium doped zinc and oxygen.

Example 7 may include the TFT of any one of examples 1-6 and/or some other examples herein, further comprising: a gate dielectric layer above the gate electrode and below the first channel layer, wherein the gate dielectric layer includes silicon and oxygen; silicon and nitrogen; yttrium and oxygen; silicon, oxygen, and nitrogen; aluminum and oxygen; hafnium and oxygen; tantalum and oxygen; or titanium and oxygen.

Example 8 may include the TFT of any one of examples 1-6 and/or some other examples herein, wherein the TFT is above an interconnect that is above the substrate.

Example 9 may include the TFT of any one of examples 1-6 and/or some other examples herein, further comprising: a capping layer between the source electrode and the drain electrode and above the second channel layer.

Example 10 may include a method for forming a thin film transistor (TFT), the method comprising: forming a gate electrode above a substrate; forming a gate dielectric layer conformally covering the gate electrode and the substrate; forming a first channel layer including a first material above the gate dielectric layer; forming a second channel layer including a second material above the first channel layer, wherein the first material has a higher mobility than the second material, and the second material has a lower leakage than the first material; and forming a source electrode and a drain electrode above the second channel layer.

Example 11 may include the method of example 10 and/or some other examples herein, wherein the first material includes indium doped zinc Oxide (IZO), zinc tin oxide (ZTO), amorphous silicon (a-Si), amorphous germanium (a-Ge), low-temperature polycrystalline silicon (LTPS), transition metal dichalcogenide (TMD), yttrium-doped zinc oxide (YZO), or zinc oxide (ZnO).

Example 12 may include the method of example 10 and/or some other examples herein, wherein the first channel layer has a thickness in a range of 0.5 nanometers (nm) – 20 nm, and the second channel layer has a thickness in a range of 0.5 nm – 20 nm.

Example 13 may include the method of example 10 and/or some other examples herein, wherein the second material includes indium, gallium, zinc, and oxide; molybdenum and sulfur; or a group-VI transition metal dichalcogenide.

Example 14 may include the method of example 10 and/or some other examples herein, further comprising: forming a buffer layer between the first channel layer and the second channel layer.

Example 15 may include the method of example 14 and/or some other examples herein, wherein the buffer layer includes indium doped zinc and oxygen.

Example 16 may include the method of any one of examples 10-15 and/or some other examples herein, further comprising: forming a capping layer between the source electrode and the drain electrode and above the second channel layer.

Example 17 may include the method of any one of examples 10-15 and/or some other examples herein, wherein wherein the source electrode or the drain electrode

includes gold (Au), platinum (Pt), ruthenium (Ru), iridium (Ir), titanium (Ti), aluminum (Al), copper (Cu), tantalum (Ta), tungsten (W), iridium-tantalum alloy (Ir-Ta), or indium-tin oxide (ITO).

Example 18 may include a computing device, comprising: a circuit board; and a memory device coupled to the circuit board and including a memory array, wherein the memory array includes a plurality of memory cells, a memory cell of the plurality of memory cells includes a transistor and a storage cell, and wherein the transistor includes: a gate electrode coupled to a word line of the memory array; a first channel layer including a first material above the gate electrode; a second channel layer including a second material above the first channel layer, wherein the first material has a higher mobility than the second material, and the second material has a lower leakage than the first material; a source electrode above the second channel layer and coupled to a source line of the memory array; and a drain electrode above the second channel layer and coupled to a first electrode of the storage cell; and the storage cell further includes a second electrode coupled to a bit line of the memory array.

Example 19 may include the computing device of example 18 and/or some other examples herein, wherein the storage cell further includes a resistive switching material layer between the first electrode and the second electrode.

Example 20 may include the computing device of example 19 and/or some other examples herein, wherein the resistive switching material layer includes hafnium and oxygen; tantalum and oxygen; hafnium, tantalum and oxygen; tellurium; germanium; silicon; or chalcogenide.

Example 21 may include the computing device of any one of examples 18-20 and/or some other examples herein, wherein the first material includes indium doped zinc Oxide (IZO), zinc tin oxide (ZTO), amorphous silicon (a-Si), amorphous germanium (a-Ge), low-temperature polycrystalline silicon (LTPS), transition metal dichalcogenide (TMD), yttrium-doped zinc oxide (YZO), or zinc oxide (ZnO).

Example 22 may include the computing device of any one of examples 18-20 and/or some other examples herein, wherein the transistor is above an interconnect that is above a substrate.

Example 23 may include the computing device of any one of examples 18-20 and/or some other examples herein, wherein the second material includes indium, gallium, zinc, and oxide; molybdenum and sulfur; or a group-VI transition metal dichalcogenide.

Example 24 may include the computing device of any one of examples 18-20 and/or some other examples herein, wherein the transistor further includes a buffer layer between the first channel layer and the second channel layer.

Example 25 may include the computing device of any one of examples 18-20 and/or some other examples herein, wherein the computing device is a wearable device or a mobile computing device, the wearable device or the mobile computing device including one or more of an antenna, a touchscreen controller, a display, a battery, a processor, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, a Geiger counter, an accelerometer, a gyroscope, a speaker, or a camera coupled with the memory device.

Various embodiments may include any suitable combination of the above-described embodiments including alternative (or) embodiments of embodiments that are described in conjunctive form (and) above (e.g., the "and" may be "and/or"). Furthermore, some embodiments may include one or more articles of manufacture (e.g., non-transitory computer-readable media) having instructions, stored thereon, that when executed result in actions of any of the above-described embodiments. Moreover, some embodiments may include apparatuses or systems having any suitable means for carrying out the various operations of the above-described embodiments.

The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the embodiments of the present disclosure to the precise forms disclosed. While specific implementations and examples are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the present disclosure, as those skilled in the relevant art will recognize.

These modifications may be made to embodiments of the present disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit various embodiments of the present disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims

What is claimed is:

1. A thin film transistor (TFT), comprising:

a gate electrode above a substrate;

a first channel layer including a first material above the gate electrode;

a second channel layer including a second material above the first channel layer, wherein the first material has a higher mobility than the second material, and the second material has a lower leakage than the first material;

a source electrode above the second channel layer; and

a drain electrode above the second channel layer.

2. The TFT of claim 1, wherein the first material includes indium doped zinc Oxide (IZO), zinc tin oxide (ZTO), amorphous silicon (a-Si), amorphous germanium (a-Ge), low-temperature polycrystalline silicon (LTPS), transition metal dichalcogenide (TMD), yttrium-doped zinc oxide (YZO), or zinc oxide (ZnO).

3. The TFT of claim 1, wherein the first channel layer has a thickness in a range of 0.5 nanometers (nm) – 20 nm, and the second channel layer has a thickness in a range of 0.5 nm – 20 nm.

4. The TFT of claim 1, wherein the second material includes indium, gallium, zinc, and oxide; molybdenum and sulfur; or a group-VI transition metal dichalcogenide.

5. The TFT of claim 1, further comprising a buffer layer between the first channel layer and the second channel layer.

6. The TFT of claim 5, wherein the buffer layer includes indium doped zinc and oxygen.

7. The TFT of any one of claims 1-6, further comprising:

a gate dielectric layer above the gate electrode and below the first channel layer, wherein the gate dielectric layer includes silicon and oxygen; silicon and nitrogen; yttrium and oxygen; silicon, oxygen, and nitrogen; aluminum and oxygen; hafnium and oxygen; tantalum and oxygen; or titanium and oxygen.

8. The TFT of any one of claims 1-6, wherein the TFT is above an interconnect, and the interconnect is above the substrate.

9. The TFT of any one of claims 1-6, further comprising:

a capping layer between the source electrode and the drain electrode and above the second channel layer.

10. A method for forming a thin film transistor (TFT), the method comprising:

forming a gate electrode above a substrate;

forming a gate dielectric layer conformally covering the gate electrode and the substrate;

forming a first channel layer including a first material above the gate dielectric layer;

forming a second channel layer including a second material above the first channel layer, wherein the first material has a higher mobility than the second material, and the second material has a lower leakage than the first material; and

forming a source electrode and a drain electrode above the second channel layer.

11. The method of claim 10, wherein the first material includes indium doped zinc Oxide (IZO), zinc tin oxide (ZTO), amorphous silicon (a-Si), amorphous germanium (a-Ge), low-temperature polycrystalline silicon (LTPS), transition metal dichalcogenide (TMD), yttrium-doped zinc oxide (YZO), or zinc oxide (ZnO).

12. The method of claim 10, wherein the first channel layer has a thickness in a range of 0.5 nanometers (nm) – 20 nm, and the second channel layer has a thickness in a range of 0.5 nm – 20 nm.

13. The method of claim 10, wherein the second material includes indium, gallium, zinc, and oxide; molybdenum and sulfur; or a group-VI transition metal dichalcogenide.

14. The method of claim 10, further comprising:

forming a buffer layer between the first channel layer and the second channel layer.

15. The method of claim 14, wherein the buffer layer includes indium doped zinc and oxygen.

16. The method of any one of claims 10-15, further comprising:

forming a capping layer between the source electrode and the drain electrode and above the second channel layer.

17. The method of any one of claims 10-15, wherein the source electrode or the drain electrode includes gold (Au), platinum (Pt), ruthenium (Ru), iridium (Ir), titanium (Ti), aluminum (Al), copper (Cu), tantalum (Ta), tungsten (W), iridium-tantalum alloy (Ir-Ta), or indium-tin oxide (ITO).

18. A computing device, comprising:

a circuit board; and

a memory device coupled to the circuit board and including a memory array, wherein the memory array includes a plurality of memory cells, a memory cell of the plurality of memory cells includes a transistor and a storage cell, and wherein the transistor includes:

a gate electrode coupled to a word line of the memory array;

a first channel layer including a first material above the gate electrode;

a second channel layer including a second material above the first channel layer, wherein the first material has a higher mobility than the second material, and the second material has a lower leakage than the first material;

a source electrode above the second channel layer and coupled to a source line of the memory array; and

a drain electrode above the second channel layer and coupled to a first electrode of the storage cell; and

the storage cell further includes a second electrode coupled to a bit line of the memory array.

19. The computing device of claim 18, wherein the storage cell further includes a resistive switching material layer between the first electrode and the second electrode.

20. The computing device of claim 19, wherein the resistive switching material layer includes hafnium and oxygen; tantalum and oxygen; hafnium, tantalum and oxygen; tellurium; germanium; silicon; or chalcogenide.

21. The computing device of any one of claims 18-20, wherein the first material includes indium doped zinc Oxide (IZO), zinc tin oxide (ZTO), amorphous silicon (a-Si), amorphous germanium (a-Ge), low-temperature polycrystalline silicon (LTPS), transition metal dichalcogenide (TMD), yttrium-doped zinc oxide (YZO), or zinc oxide (ZnO).

22. The computing device of any one of claims 18-20, wherein the transistor is above an interconnect, and the interconnect is above a substrate.

23. The computing device of any one of claims 18-20, wherein the second material includes indium, gallium, zinc, and oxide; molybdenum and sulfur; or a group-VI transition metal dichalcogenide.

24. The computing device of any one of claims 18-20, wherein the transistor further includes a buffer layer between the first channel layer and the second channel layer.

25. The computing device of any one of claims 18-20, wherein the computing device is a wearable device or a mobile computing device, the wearable device or the mobile computing device including one or more of an antenna, a touchscreen controller, a display, a battery, a processor, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, a Geiger counter, an accelerometer, a gyroscope, a speaker, or a camera coupled with the memory device.

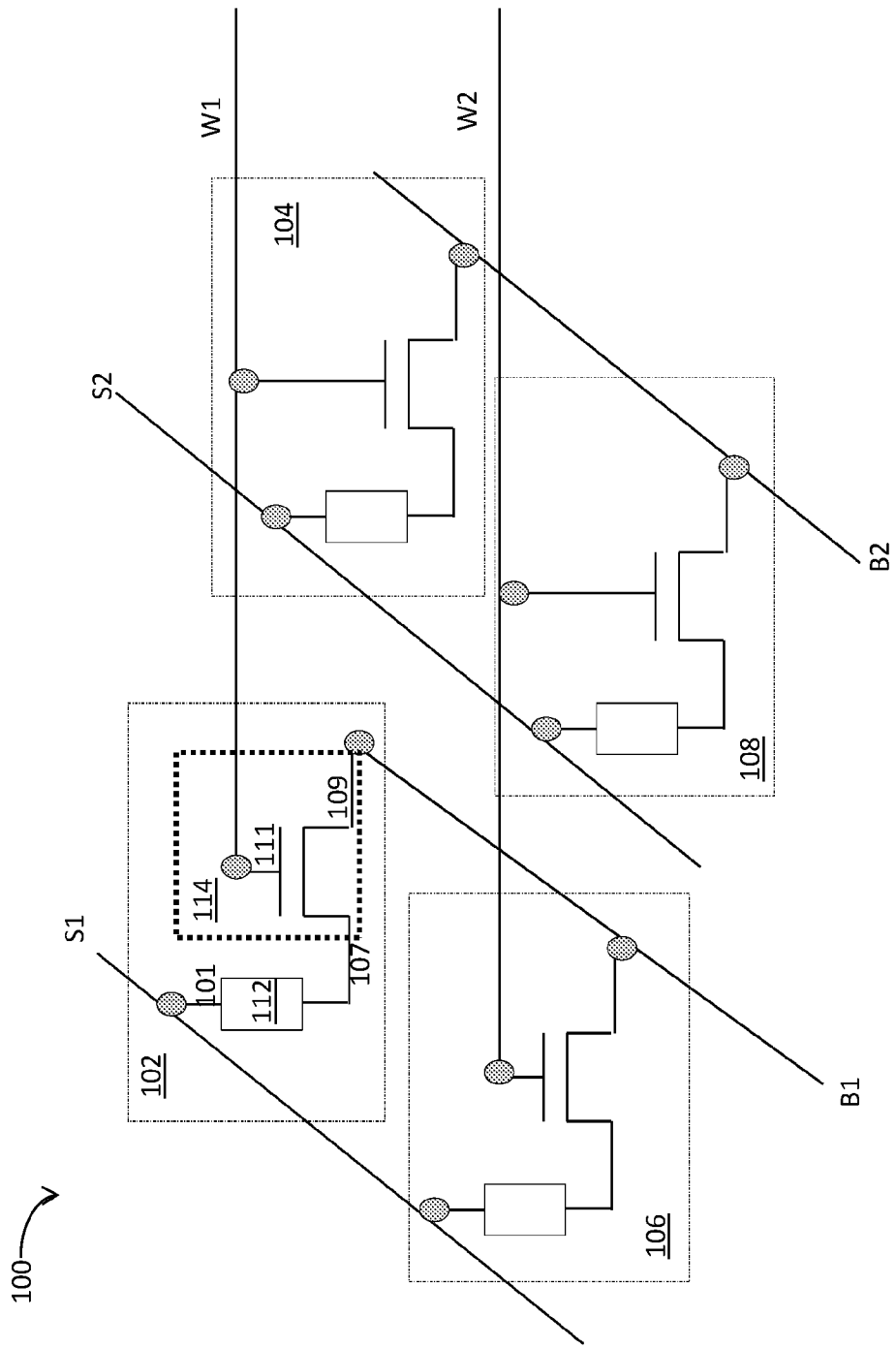

Figure 1

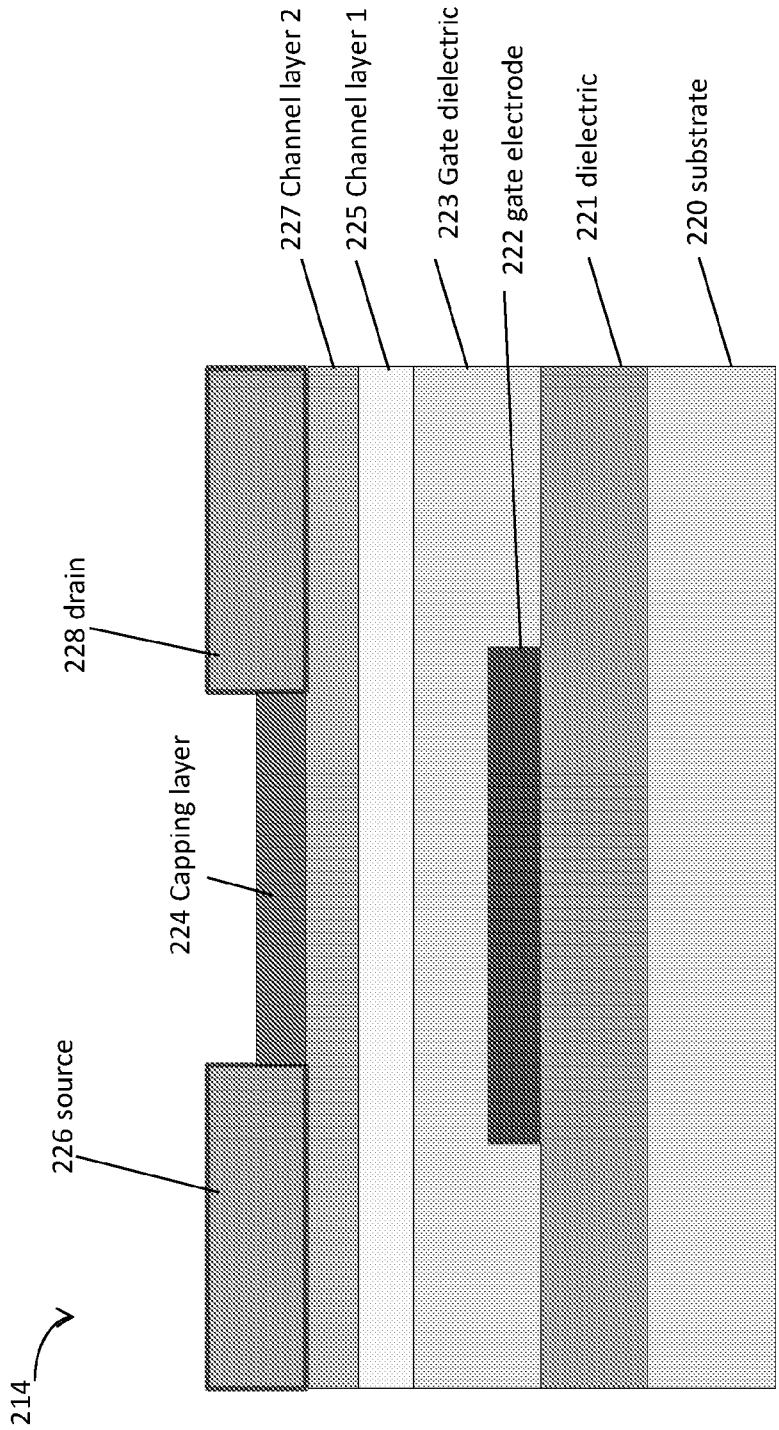
227 Channel layer 2
225 Channel layer 1
223 Gate dielectric
222 gate electrode
221 dielectric
220 substrate
228 drain
224 Capping layer
226 source
214

Figure 2

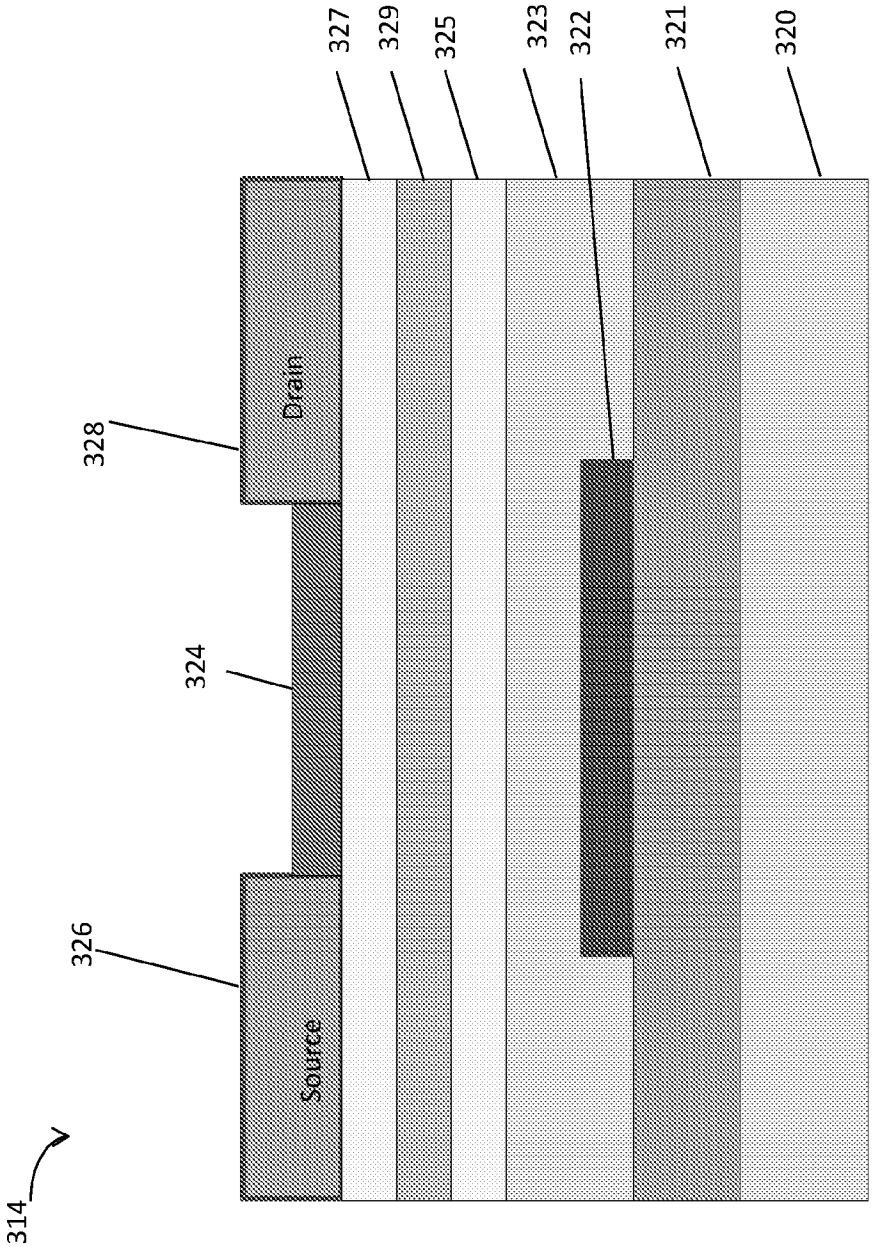

Figure 3

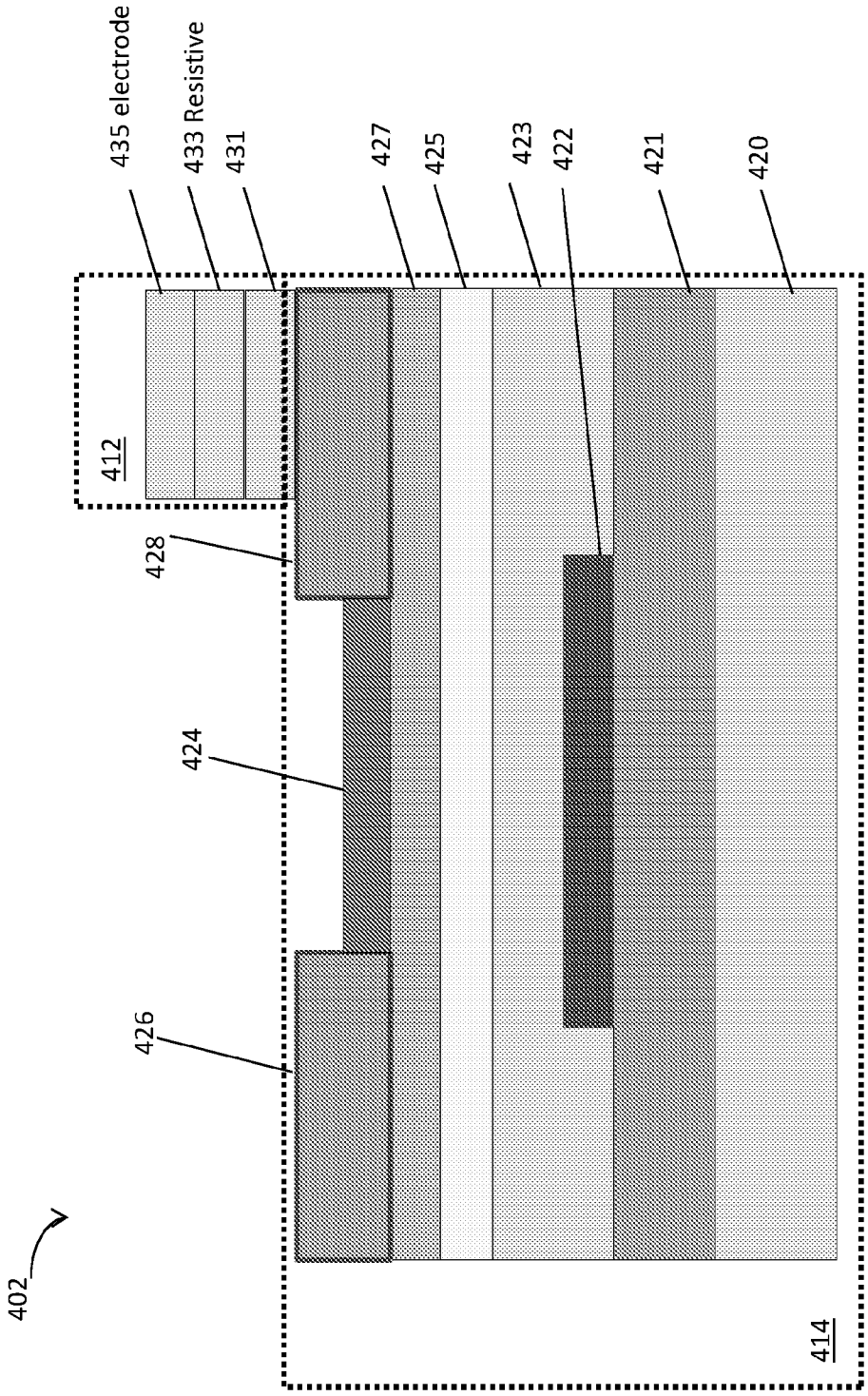
435 electrode
433 Resistive
431
427
425
423
422
421
420
412
428
424
426
402
414

Figure 4

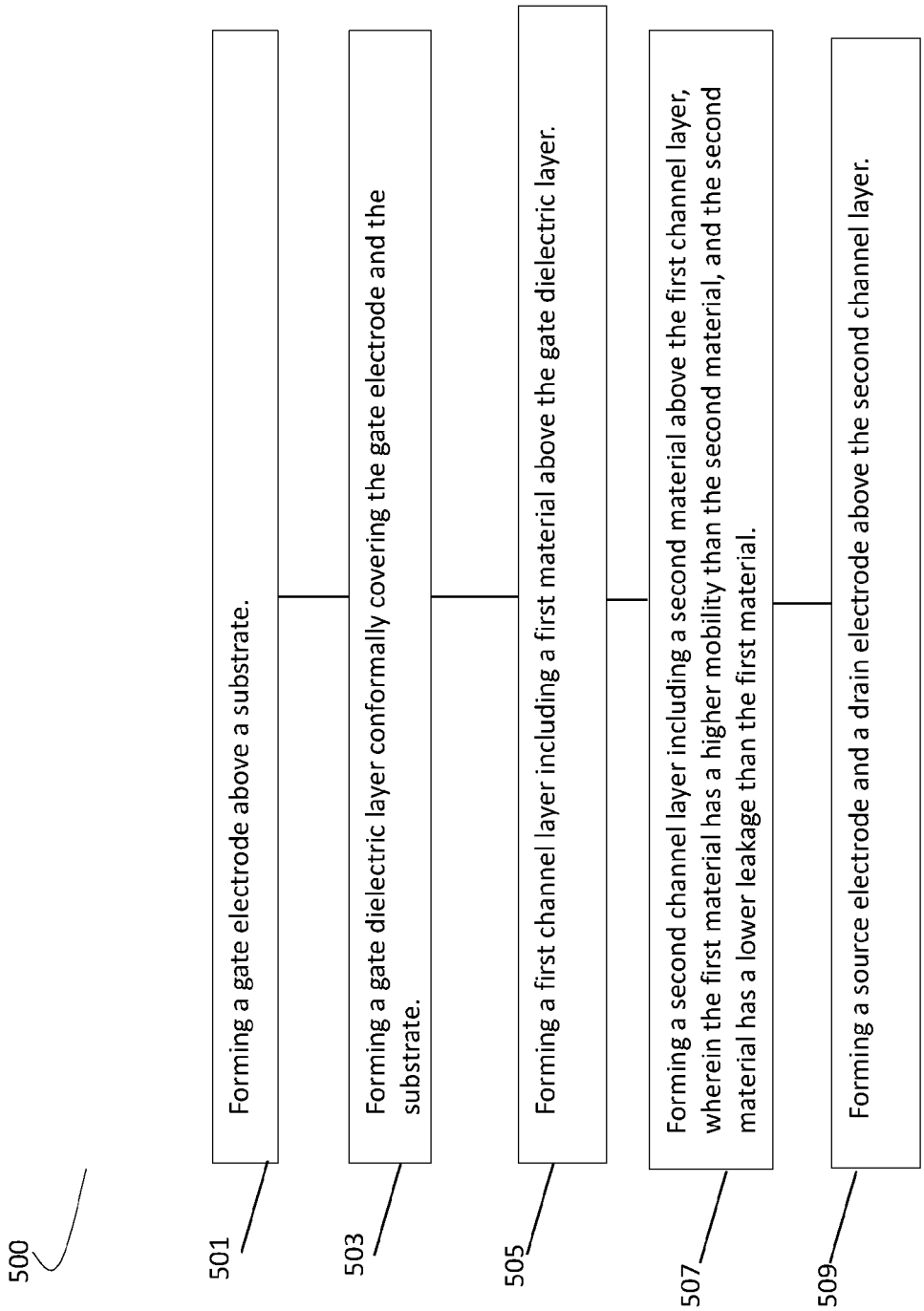
500
501
Forming a gate electrode above a substrate.
503
Forming a gate dielectric layer conformally covering the gate electrode and the substrate.
505
Forming a first channel layer including a first material above the gate dielectric layer.
507
Forming a second channel layer including a second material above the first channel layer, wherein the first material has a higher mobility than the second material, and the second material has a lower leakage than the first material.
509
Forming a source electrode and a drain electrode above the second channel layer.

Figure 5

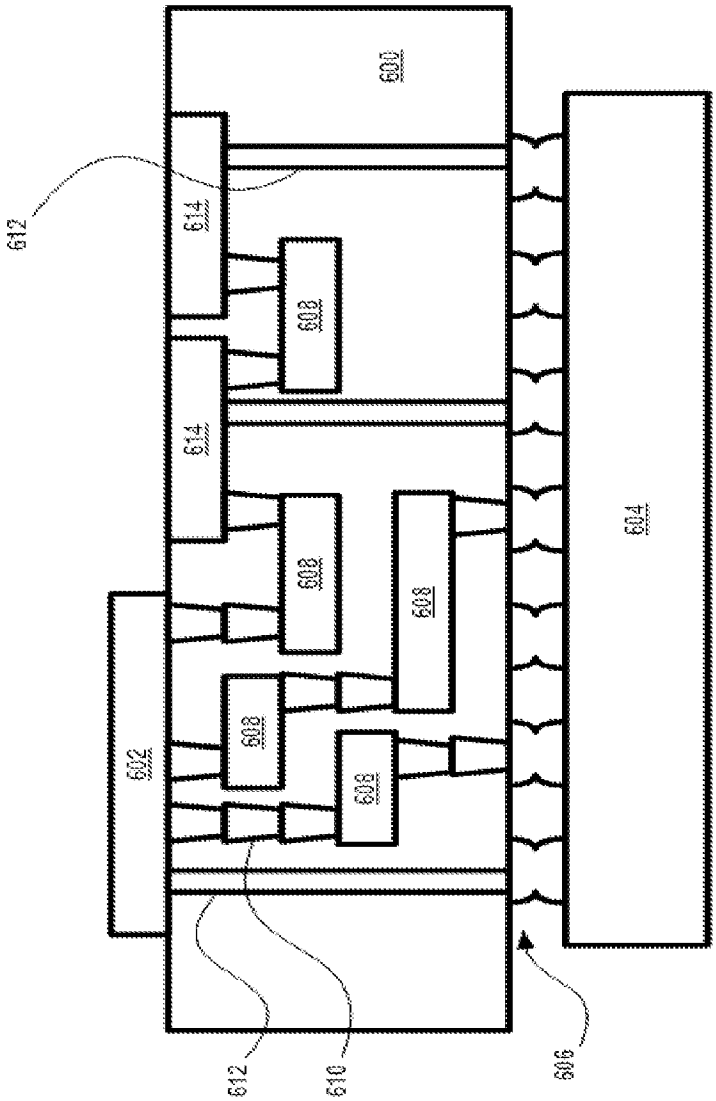

Figure 6

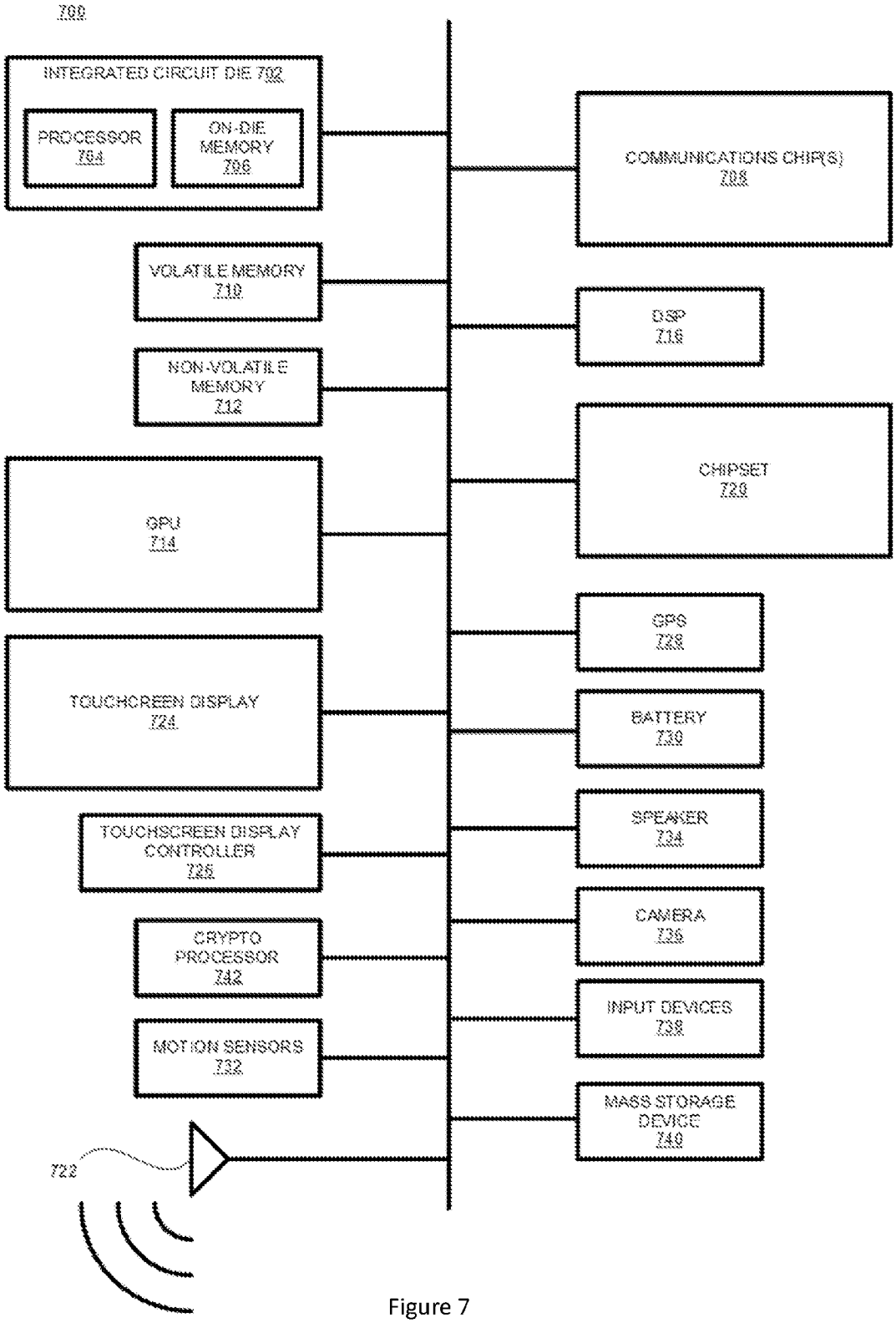
700
INTEGRATED CIRCUIT DIE 702
PROCESSOR 704
ON-DIE MEMORY 706
VOLATILE MEMORY 710
NON-VOLATILE MEMORY 712
GPU 714
TOUCHSCREEN DISPLAY 724
TOUCHSCREEN DISPLAY CONTROLLER 726
CRYPTO PROCESSOR 742
MOTION SENSORS 732
722
COMMUNICATIONS CHIP(S) 708
DSP 716
CHIPSET 720
GPS 728
BATTERY 730
SPEAKER 734
CAMERA 736
INPUT DEVICES 738
MASS STORAGE DEVICE 740

Figure 7

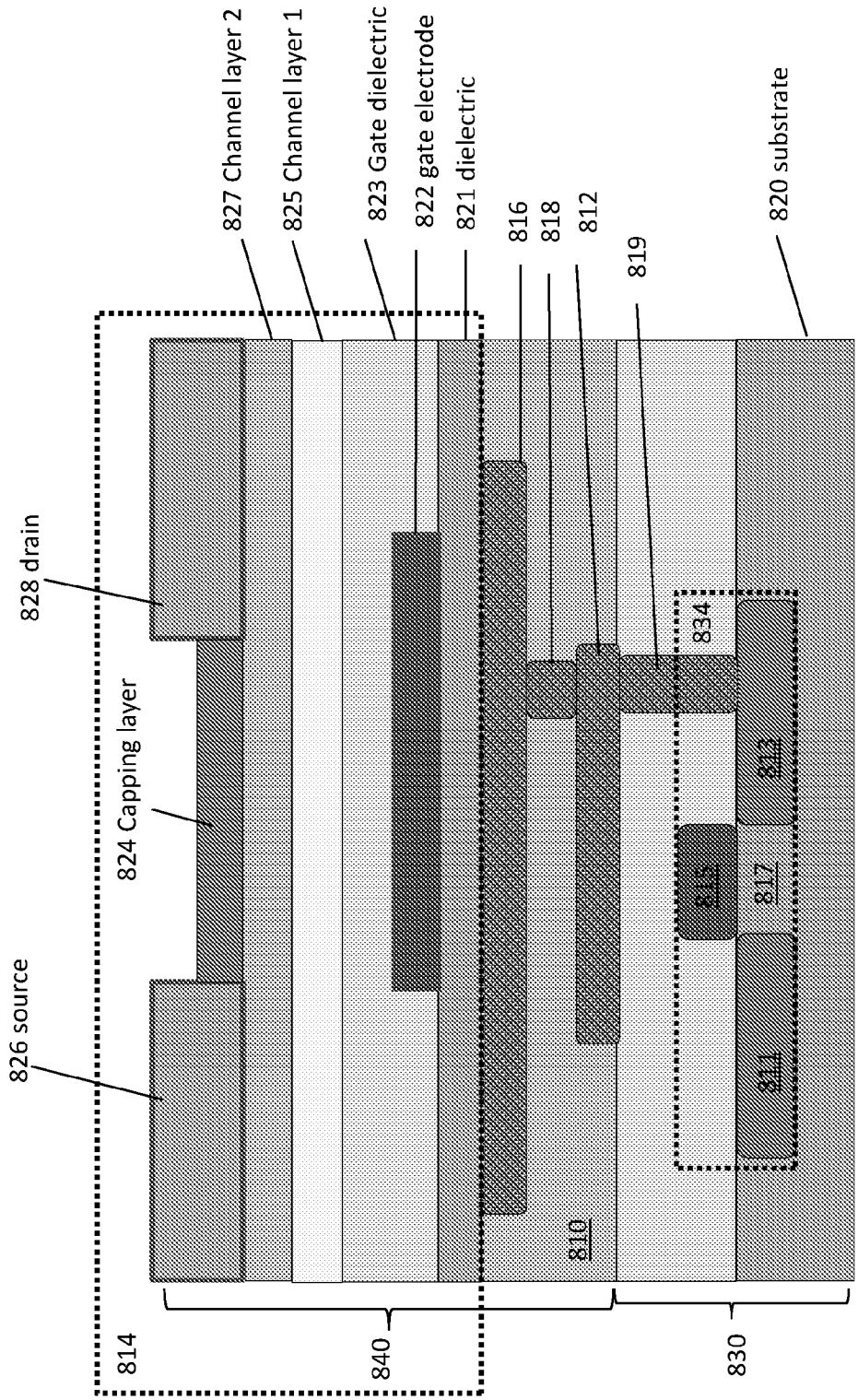
827 Channel layer 2
825 Channel layer 1
823 Gate dielectric
822 gate electrode
821 dielectric
816
818
812
819
820 substrate
828 drain
824 Capping layer
826 source
834
813
815
817
811
810
814
840
830

Figure 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/025490

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/786(2006.01)i, H01L 27/108(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/786; H01L 21/84; H01L 21/336; H01L 29/12; H01L 29/24; H01L 21/00; H01L 21/44; H01L 27/108

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: thin film transistor, TFT, channel, leakage, mobility, gate, source, drain, bottom

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0032784 A1 (GHOLAMREZA CHAJI et al.) 07 February 2013 See paragraphs 21-38, claims 1-16 and figures 1-6.	1,3-4,8,10,12-13
Y		2,5-7,9,11,14-25
Y	US 2014-0131698 A1 (SAMSUNG ELECTRONICS CO., LTD.) 15 May 2014 See paragraphs 29-48, claims 1-20 and figures 1-5.	2,5-7,9,11,14-17 ,21,24
Y	US 2003-0045037 A1 (PING MEI et al.) 06 March 2003 See paragraph 2, claims 1-25 and figures 1-8.	18-25
A	US 2012-0012840 A1 (VINCENT KORTHUIS et al.) 19 January 2012 See paragraphs 13-35 and figures 1A-4.	1-25
A	US 2008-0191204 A1 (SUN-IL KIM et al.) 14 August 2008 See paragraphs 50-57 and figures 1-2.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 December 2017 (27.12.2017)	**27 December 2017 (27.12.2017)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/025490

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