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(30) JP-P-2000-00297443 2000 09 28 (JP)

(73) 가 가
1 1 1

(72) 가 가 가
1가 가

가 가 가
1가 가

(74)

:

(54)

1, 2	.	1
,	.	,
2		2
	1	

1

, , , , ,

1
2
3a, 3b

1

(1) (2)

4		NAND						
5	2							
6a,	6b,	6c,	6d				I/O	
7a,	7b	1			RD			
8a,	8b,	8c	1	CG			, 8d	8c
9a	1					9b		
10	1			RD				
11	1							
12								
13	12							
14								
15a	1			(15a)			, 15b	(15b)
16	4							
17a							, 17b,	17c
18								
19								
20								
21	1							
22	1							
23	1							
24	1							
25								
26a,	26b,	26c	2					
27								
28	2	1						
29								
30								
31								
32	2							
33a,	33b	1						
34	2							
35	1							
36								
37								
38								
39								
40								
41	1							
42		2						
43	1	,	2					
44	1	,	2					
45a,	45b,	45c,	45d	1	,	2		
46	1	,	2					
47	1	,	2					

< >

1 :

2 :

3 :

4 :

5 : I/O

6 :

7 :

8 : ECC

9 : CG

10 : RD

	(16)	(7)	(13)	(14) 가	(13)	(1)
3)	(14) ,			,	,	.
	(10)	(17)	RD	(7)	RD()	
,	(3)	.	.	RD	(10)	
(9)	CG)	(9)	(18)	(7)	CG()	(14)
ROM	(6)	(20) 가	(12) 가	(6)		(11)
.	(1)	(19)	.	RD	(12)	(19) 가
M ROM	(6)	(19),	(19),	RD	(12)	(1)
.	(1)	, CG	(9)	(6)	,	
	(20)		ROM	ROM	가	,
M			.	, ROM	.	, ROM
2 1	(31 ₀ , 31 ₁ 31 _{n/2})	(1)		(2)	.	(2)
(4),	(7)	CSL0, CSL1	CSLn/2	(31 ₀ , 31 ₁ 31 _{n/2})	(31 ₀ , 31 ₁ 31 _{n/2})	(3)
BL0, BL1	.	.	.	BL2, BL3	.	(31 ₀)
.	(31 _{n/2})
PROM	(1)	NAND	M0 M15	.	NAND	16 EE
S2	2 CELSRC	S2	1	1	M15 S1	M0
SGD2	.	.	1	S1	1 BLO	,
1)	,	.	.	.	2	2
,	2	1	, 4	1	,	1
NAND	2	.	.	2	,	
.	
(BLi)	1	.	.	2	(BLi, BLi+1)	1
3a, 3b	.	.	,	(BLi+1)	.	.
41)	.	.	n	3a	(41)	(43)
3b	.	(44) 가	.	(42)	.	.
(41)	.	.	.	(44)	.	.
4	.	(48)	.	(41)	.	.
M0 M15 가	.	NAND	.	(45)	.	.
S2 3b	1	S1	2	n	(46) 가	.
5	2	.	.	.	(47)	.
BLTR	N	(310)	.	.	NAND	16
(61c)	NAND	NAND
.	S1	2
(62a)	.	(61a)
VBLA 가	.	(61a)
.
(61b)	(61b)	(62a)
.	PREA 가

A17	A26	ARD가	1	가	AROWA	AROW
E가 ROM	(109)	, ROM	, ROM	CMD_ROMBA가 가	,	가
,	, ROM	, (109)가 15a 1 (15)	12 ROM	(15a)	, 15b ROM	(108) (2)
0)	(15b)	(15a) P MOS (151e, 151f, 151h), NOR VDD가 (151g)	(151a, 151b), N MOS (151g)	(151a)	(151c), (151a, 151b)	(151)
d),	(151g)	(151c) LOWVDDn	(151d)가 NOR NOR (151g) PROENABL	(151a) (151e) (151f)	(151h)	NOR (152)
1c)	CMD_ROMBA가 (151h)	(15b) VDD가 (152c)	(152d)가 NOR NOR (152g) ERAENABL	(152a) (152e) (152f)	(152h)	(152c) NOR (152)
15b	LOWVDDn	PROENABL, (151d, 152d)	ERAENABL ROM	CMD_ROMBA가 , ROM	,	,
g)	CMD_ROMBA가 (152h)	PROENABL, ERAENABL (151d, 152d)	,	,	,	,
가	LOWVDDn	PROENABL, (151d, 152d)	ERAENABL ROM	CMD_ROMBA가 , ROM	,	,
(4 (值))	4					
16, 17a	'0' '3' '0'	, 가				
16	, , 2	가 '1'	가	, , 1	1	가
'0'	, , , 2	가 '0'	가	, , 1	1	2
, , , , 1	'0'	가 '1'	가	1	'O'	가
, , , , , 2	가 '0'	1	'1'	'2'	, , 1	가 '1'
, , , , , , 1	가 '1'	, , 1	'0'	'0'	, , , 1	'3'
, , , , , , , 1	1	1	1	1	1	1
16, 17a	가 '0', '0'	, , 1	1	1	1	1
2	가 '2', '3'	가 '1'	1	1	2	2
, , , 1	1	1	1	1	1	1
, , , , 1	1	1	1	1	1	1
, , , , , 1	1	1	1	1	1	1

	가	1	LAT(A)	가	,	OK
(41	1	(14))
14)	s	Vpgm	,	Vpgm,	Vera	Vpas
	,	,	,	가		,
41	가	,	,	Vpgm,	Vpass	
,	(161)	Vpgm,	Vpass	(161),	(162)	Vera
era	(162)	CT1, CT2	가	(162)	(162)	Vpgm,
)	CT1	,	1	,	(162)	Vpass
,	CT2	,	1	,	NG	V
,	가	,	,	(163)	1	(162)
,	CT2	,	가	,	,	(161)
,	CT2	,	가	,	가	,
,	Vpass, Vpgm	가	(162)	(161)	,	,
9	1	,	bkl0 bkl23	(1)	bkl0 bkl23,	bIkRD0 bIkRD
D9	(6a)	(109)	ROM	(109)	bIkRD0 bIkRD9	(6a)가
	가,	(15)	ROM	(15a),	(15b)	(151c, 152c)
,	,	, ROM	,	,	,	,
,	,	((6a)	(109)	()
,	ECC	,	ECC	21	(15)	,
,	,	NG	,	,	가	,
,	,	,	,	,	,	,
,	(162)	CT2	가	CT2	(161)	,
,	가	,	가	,	가	,
(2)	2	2	1	1	1
1	1	2	1	1	2	2
1	2	1	2	1	1	2

, '12h' , BUSY . . . 1 LAT(A) 2 LA
T(B) . , '80h', (. . .), , '11h'
BUSY . . . (A15, A16) 4 . ,
'11h' . . . '10h'
2 , 1, 2 . ,
. , , ,
, 1, 2 (6a) (109) , (15a) (15b)
(151c, 152c) 가 . . . EEPROM
가 . , . . .
가
가
,

(57)

1.

1, 2 , , 1 (blk) ;
2 (blkRD) , , 2

2.

1 1 , , 3

3.

2 , , 3 2

4.

3 , , 2

5.

1 , , 2 (20) ,

2

6.

1, 2 , , 1 ;
1, 2 , , 2 (6, 6a) - ; (109)
1 2 (108) , , , 가 , , 가

7.

6 , , 1 3

8.

7 , , 3 2

; (163);
(161);

, (162)

, 1 (CT2) ↳

21.

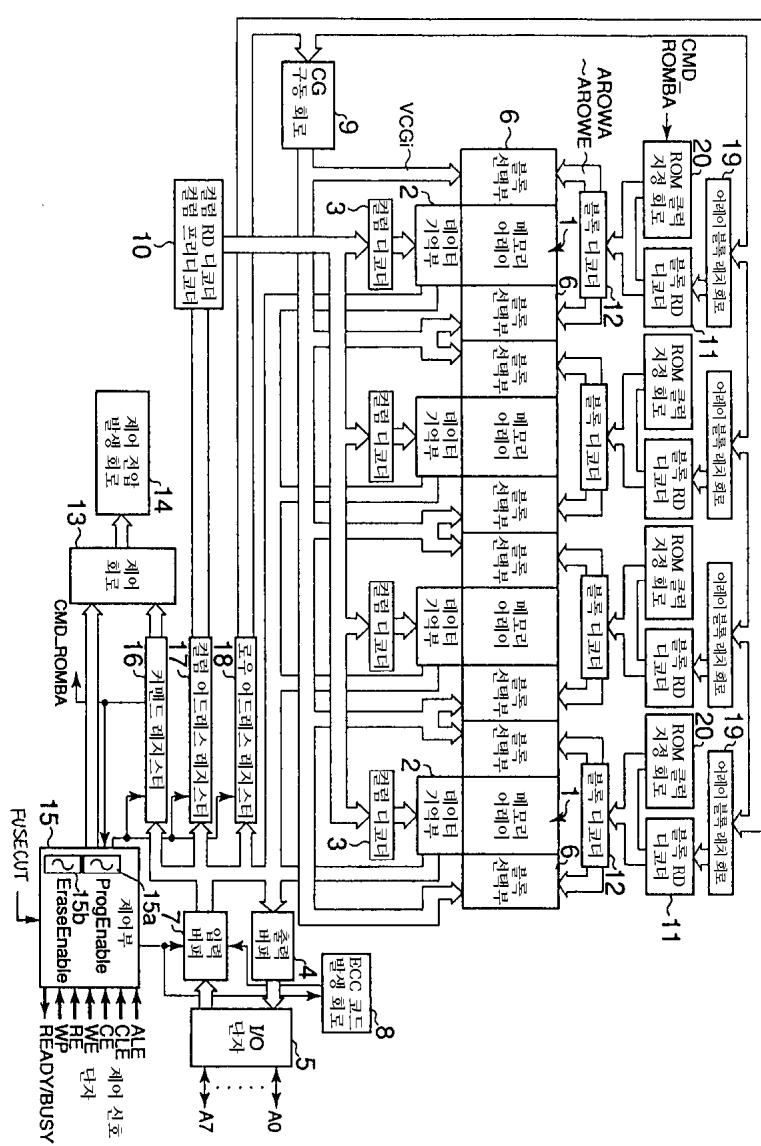
20 ,
21 (161)

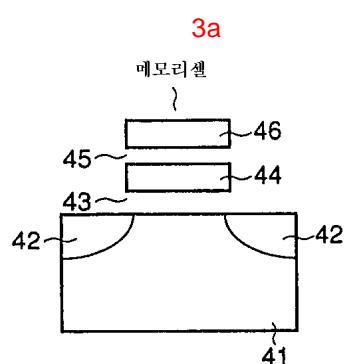
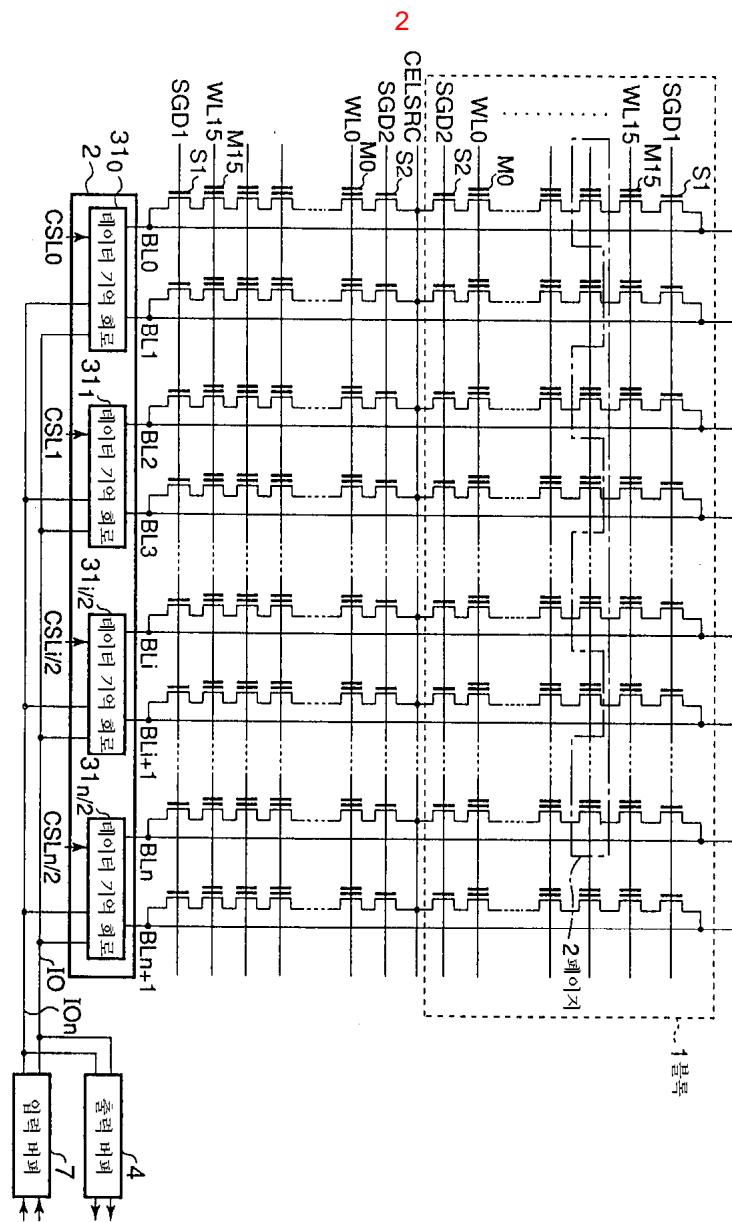
22.

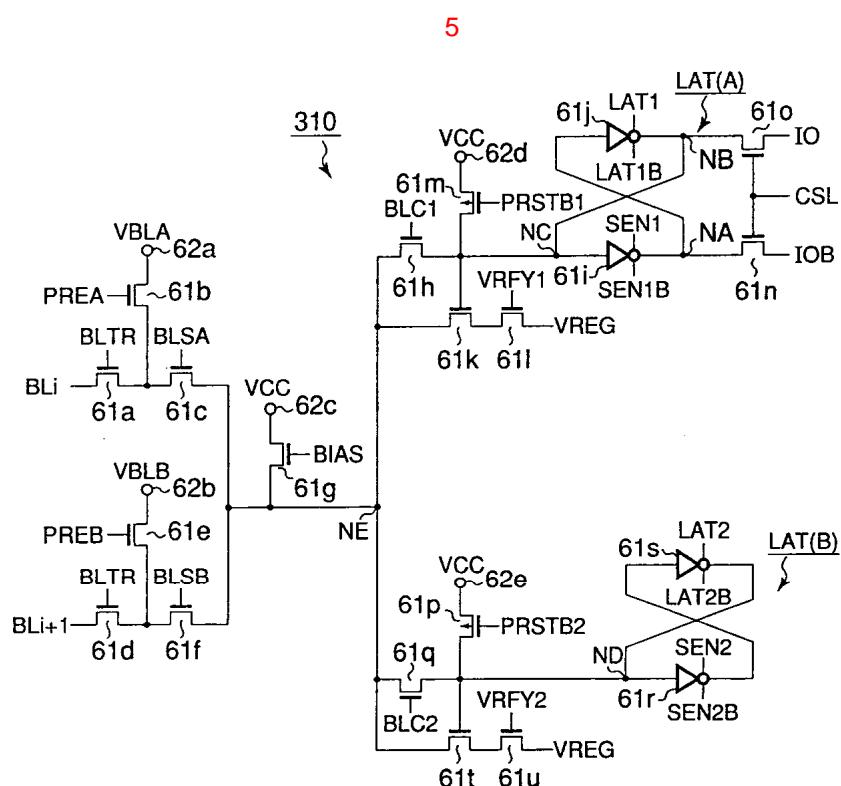
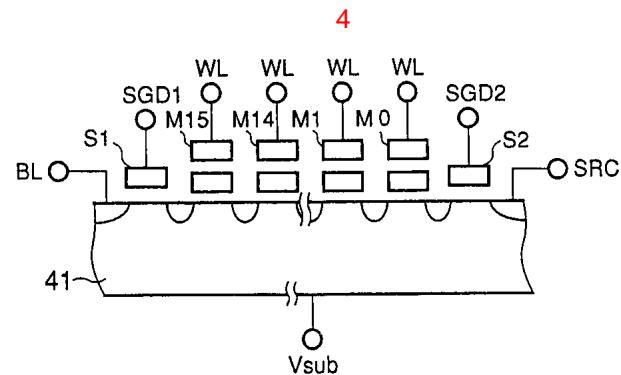
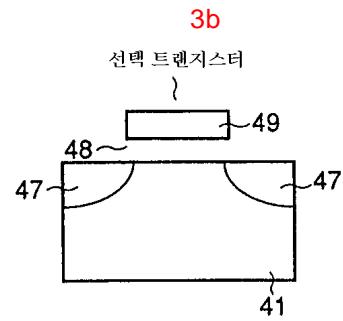
21 ,
22 1

23.

20 ,
21 1 , NG



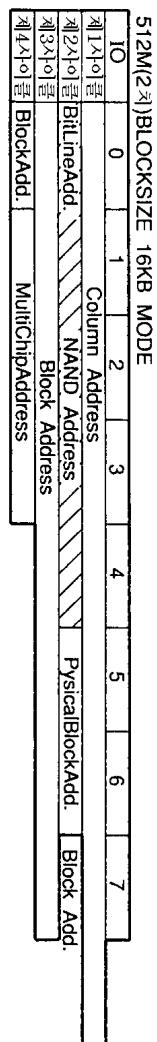




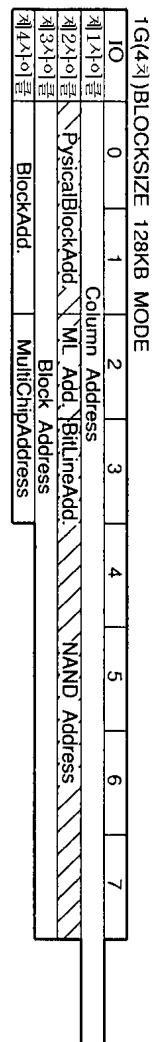
6a

1G(4 치)BLOCKSIZE 32KB MODE							
IO	0	1	2	3	4	5	6
제1사이클	A0	A1	A2	A3	A4	A5	A6
Column Address							A8E
제2사이클	A9	A10	A11	A12	A13	A14	A15
제3사이클	ML Add.	BLtineAdd.		NAND Address			PhysicalBlockAd.
제4사이클	A17	A18	A19	A20	A21	A22	A23
			Block Address				A24
	A25	A26	A27	A28	A29		
	BlockAdd.		MultiChipAddress				

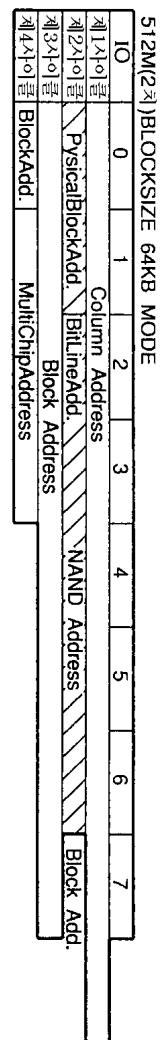
6b



6c



6d



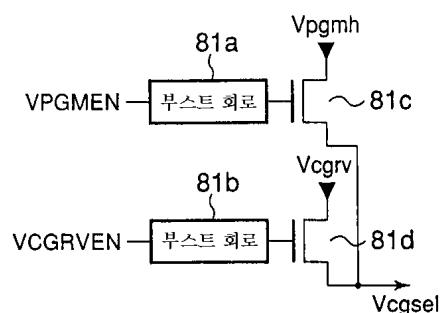
7a

A0	L	H	L	~	H	H
A1	L	L	H	~	H	H
A2	L	L	L	~	H	H
CA	0	1	2	~	7	
A3	L	H	L	~	H	
A4	L	L	H	~	H	
A5	L	L	L	~	H	
CB	0	1	2	~	7	
A6	L	H	L	~	H	—
A7	L	L	H	~	H	—
A8	L	L	L	~	H	—
A8E	L	L	L	~	H	H
CC	0	1	2	~	7	8

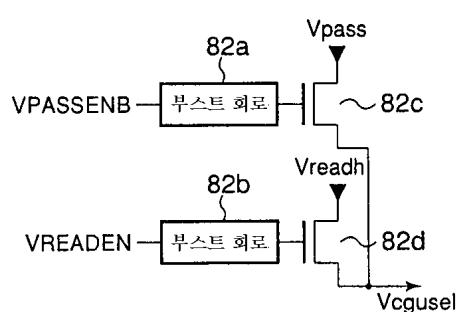
7b

	분체 영역	ECC 코드 영역	ECC 코드 또는 R/D	R/D 영역
	528컬럼	17컬럼	4컬럼	4컬럼
CA	0 1 6 7	0 1 7 0		
CB	0 0 ~ 1 1	2 2 ~ 3 4		
CC	0 0 8 8	8 8 8 8		
CSS			4 5 6 7	0 1 2 3
CSL	0 1 ~ 525 527	528 529 ~ 543 544		
A0	L H L H	L H H L	H L H L	
A1	L L H H	L L H L	L H H L	
A2	L L H H	L L H L	L L L H	
A3	L L H H	L L H L	L L L L	
A4	L L ~ L L	H H ~ H L	L L L L	
A5	L L L L	L L L H	H H H H	
A6	L L L L	L L L L	L L L L	
A7	L L L L	L L L L	L L L L	
A8	L L L L	L L L L	L L L L	
A8E	L L H H	H H H H	H H H H	

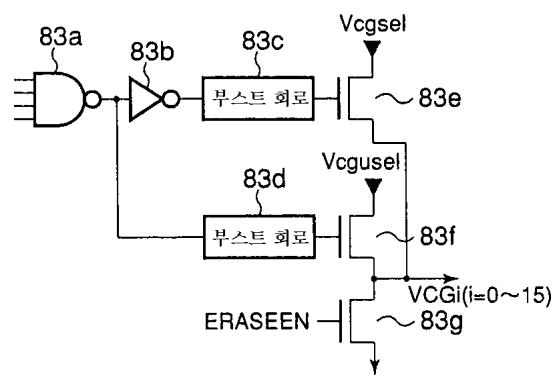
8a



8b



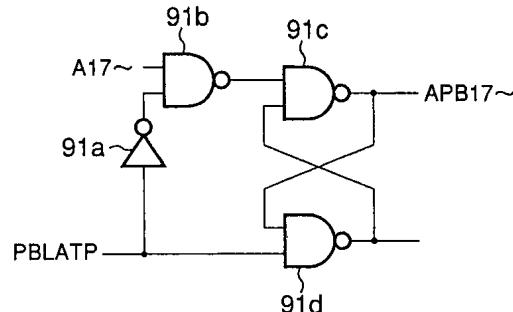
8c



9a

어레이	0	1	2	3
A15	L	H	L	H
A16	L	L	H	H
PBLATPB	0	1	2	3

9b



10

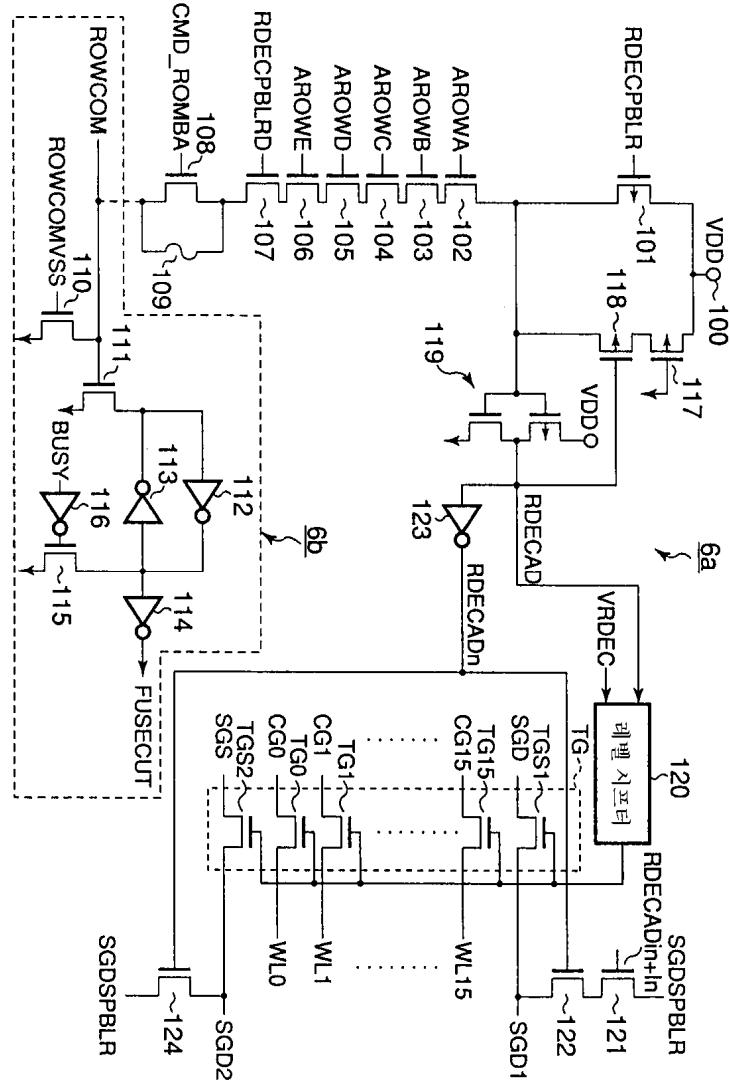
APB17	L	H	H		ATPB17	L
	H				ATPB18	H
APB26	H	L				L
					ATPB26	L
					ATPBRD	H

일치 →

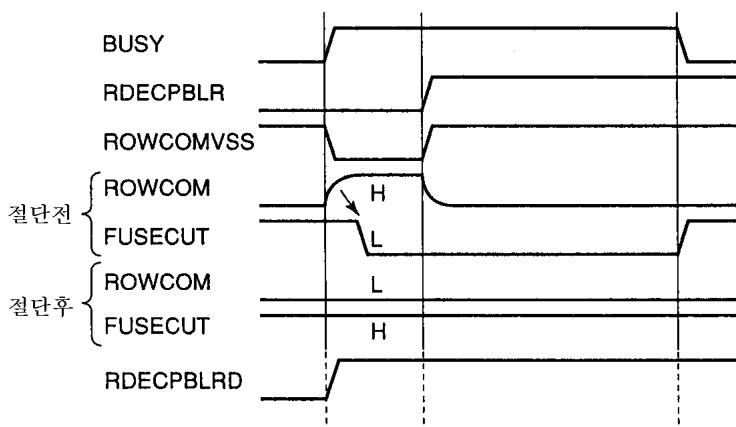
11

ATPB17	L	H	L	H
ATPB19	L	L	H	H
AROWA	0	1	2	3
ATPB18	L	H		
RDECPB	L	R		
ATPB20	L	H	L	H
ATPB21	L	L	H	H
AROWB	0	1	2	3
ATPB22	L	H	L	H
ATPB23	L	L	H	H
AROWC	0	1	2	3
ATPB24	L	H	L	H
ATPB25	L	L	H	H
AROWD	0	1	2	3
ATPB26	L	H	L	
ATPBRD	L	L	H	
AROWE	0	1	2	

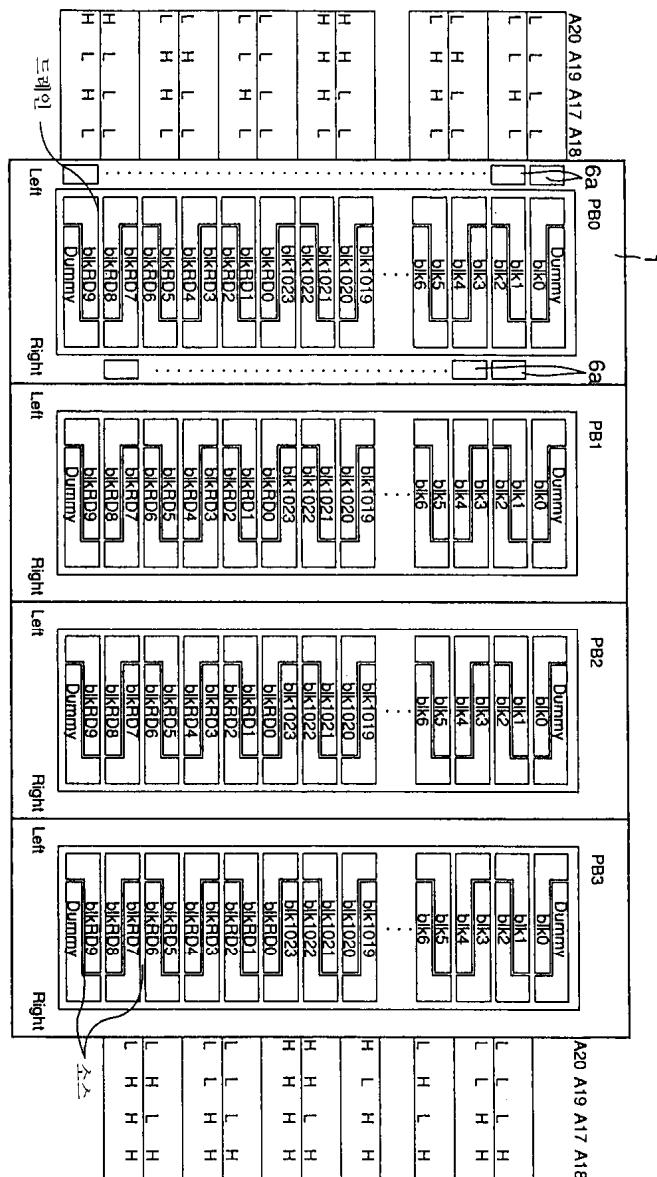
12



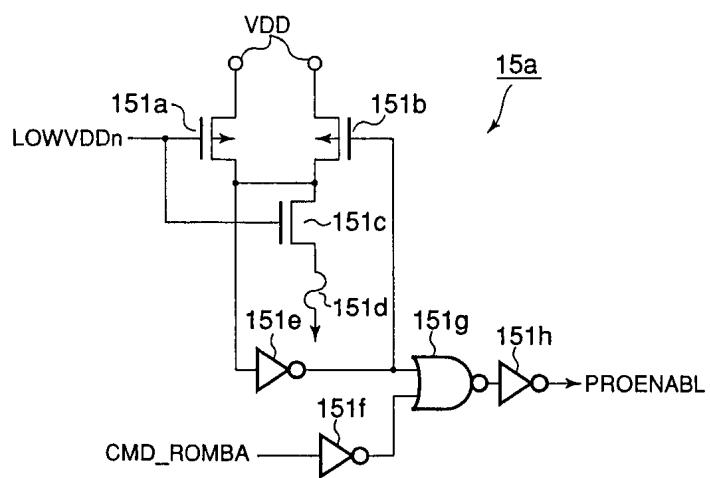
13

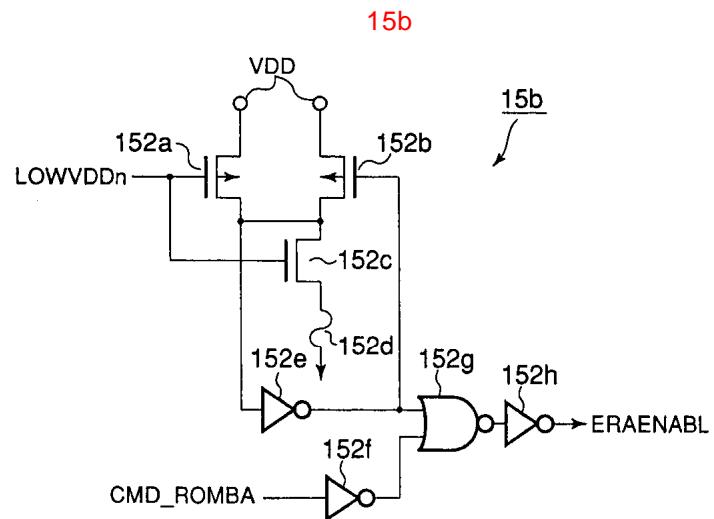


14

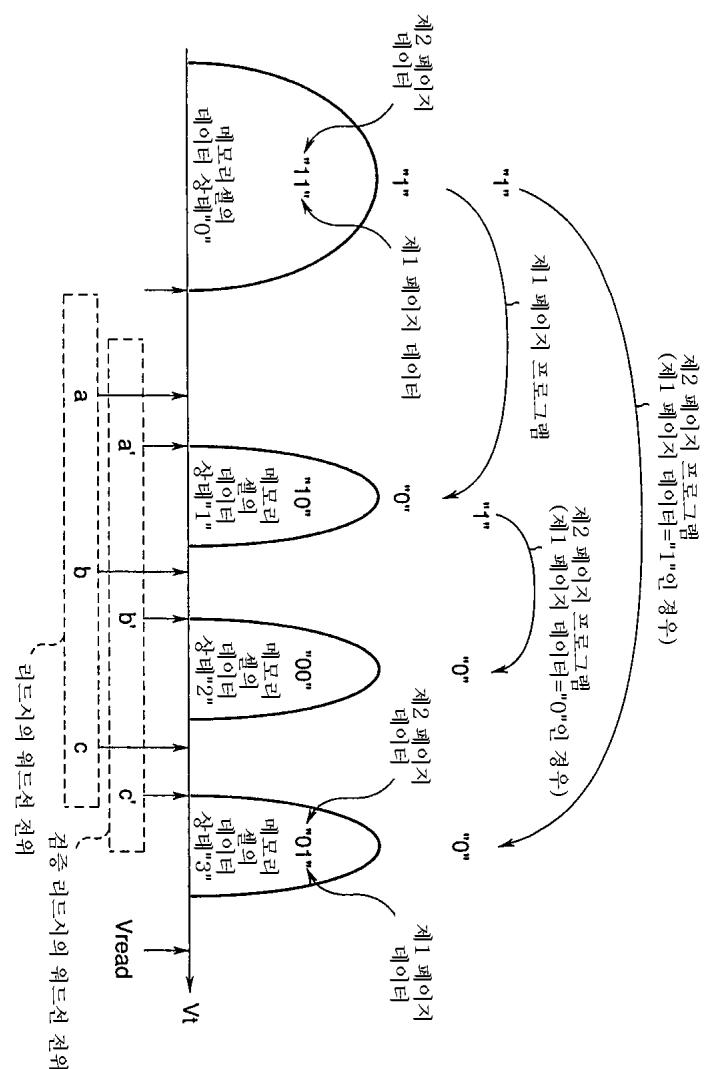


15a





16



17a

메모리셀의 데이터	메모리셀의 임계치	기입 및 판독되는 데이터	
		제1 페이지	제2 페이지
0	0V 이하	1	1
1	0.3V~0.5V	0	1
2	0.8V~1.0V	0	0
3	1.3V~1.5V	1	0

메모리셀의 데이터와 메모리셀의 임계치

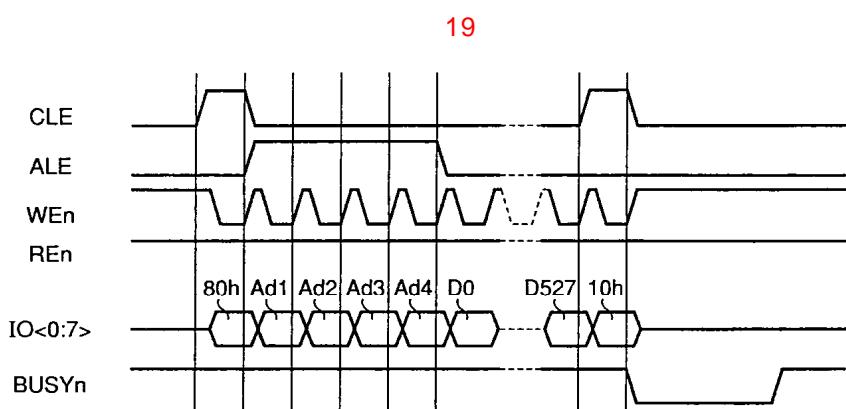
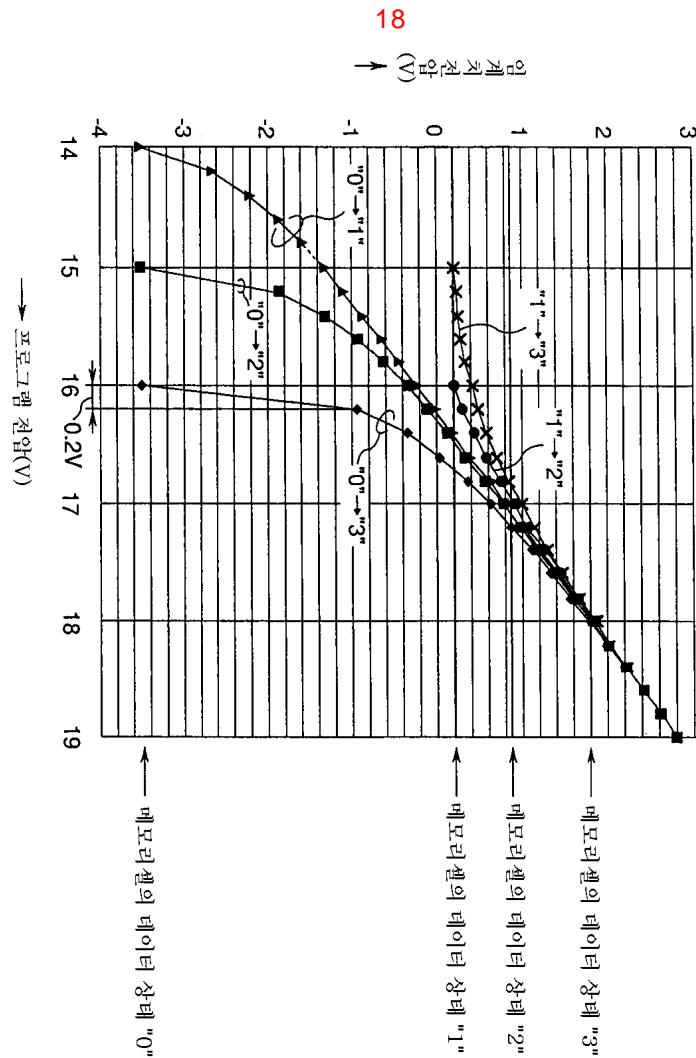
17b

	필요 스텝 업 횟수	
제1 페이지 기입	13회	(0→1)13회
제2 페이지 기입	11회	(0→3)11회 (1→2)6회
합계	24회	

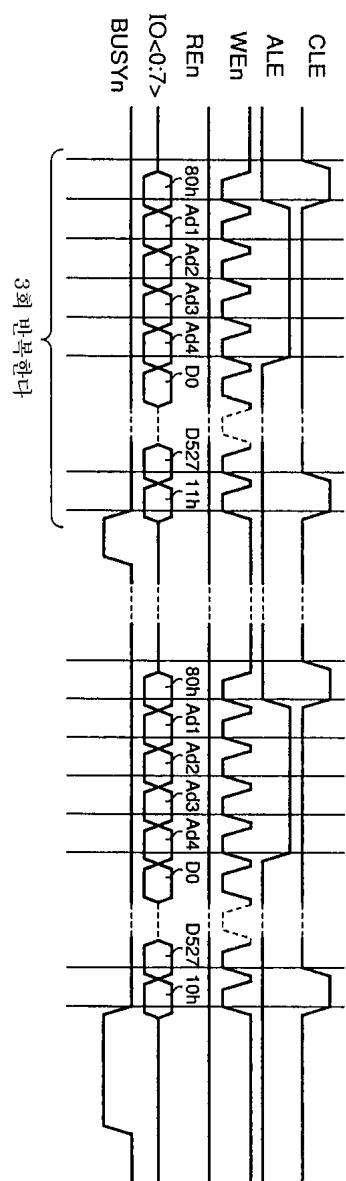
17c

	필요 스텝 업 횟수	
제1,2 페이지 동시 기입	20회	(0→1)13회 (0→2)17회 (0→3)20회
합계	20회	

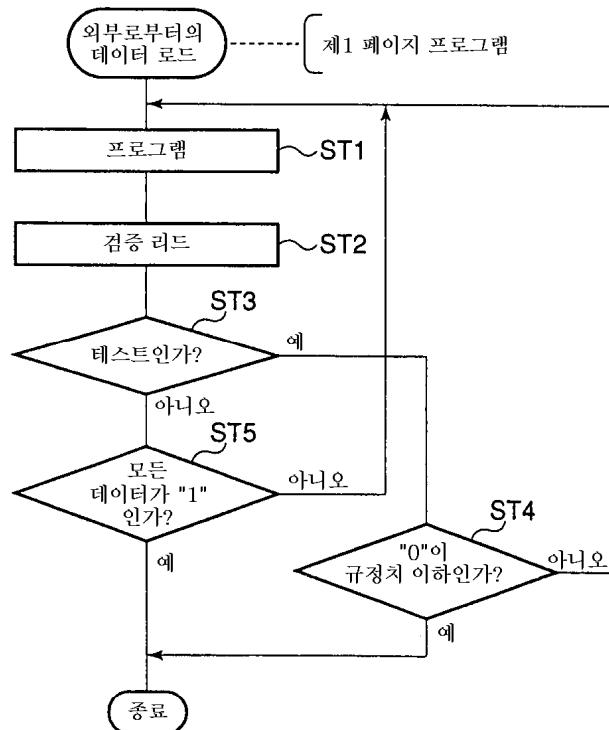
기입 횟수



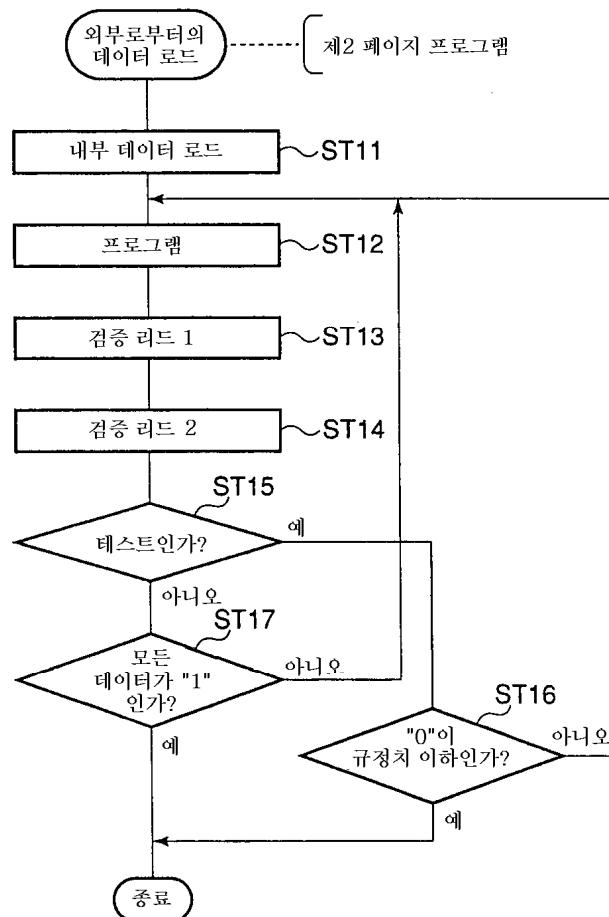
20



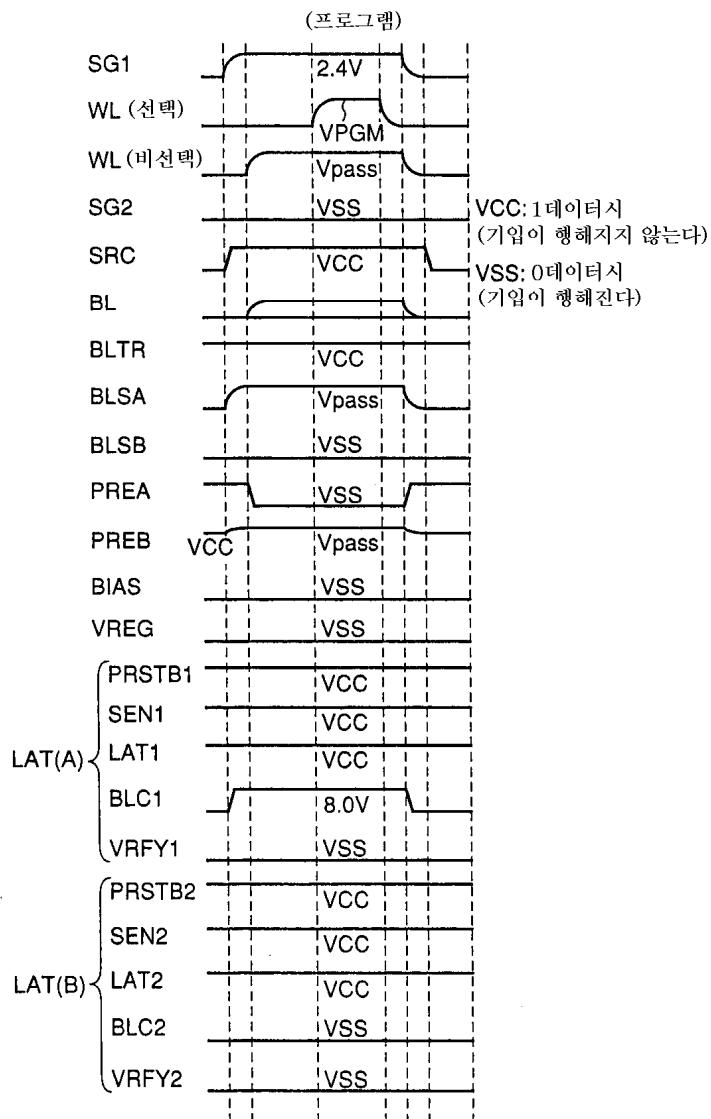
21



22



23



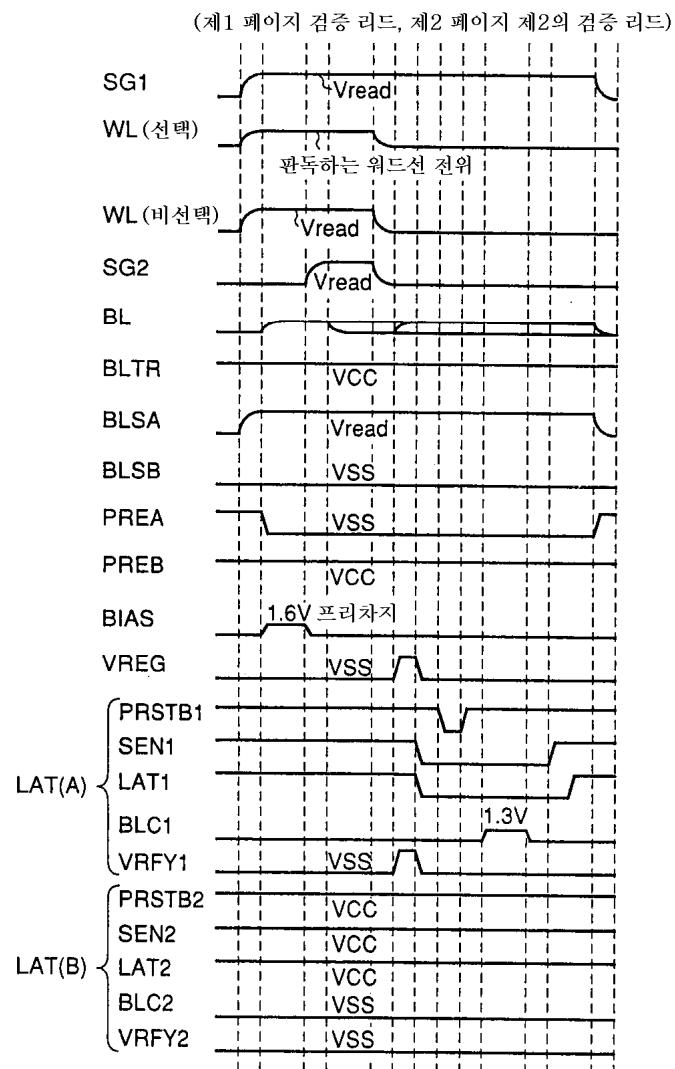
24

프로그램 검증 (제1 페이지)

상태 0	상태 0→1		메모리셀의 데이터	
	A B bit	A B bit		
inhibit	Write(OK)	Write(NG)		
A B bit	A B bit	A B bit		
H	L	L	데이터 로드 (A와 write→L, inhibit→H)	
H L	L H	L L	b'로 리드	0→1
H H	L H	L L	A가 H일 때 비트선 H(VRFY1)	검증
H H	H H	L L	비트선의 전위를 A로 래치	

(inhibit=비기입, A=LAT(A), B=LAT(B))

25



26a

26b

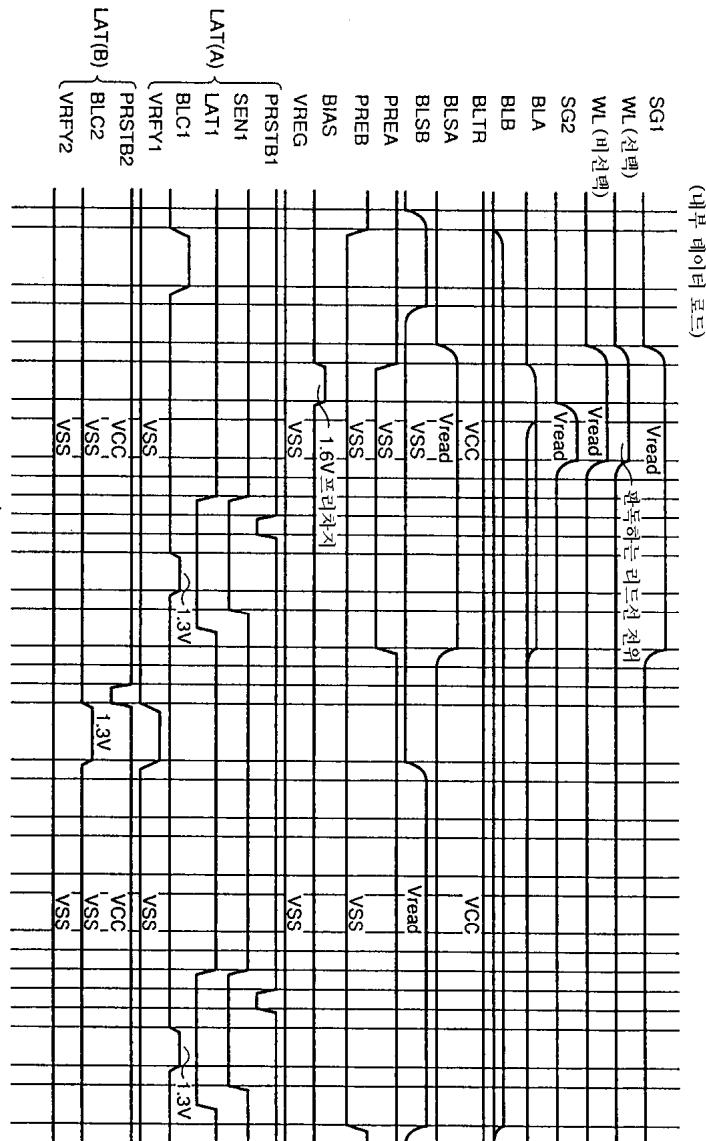
HH	LH	HL	LL	LL	b'로 카드 B가 H일 때 비트선 L(VRFY2) A가 H일 때 비트선 H(VRFY1) 비트선의 천위를 A에 입력한다	1→2 접종
HHL	LHSH	HLL	LLH	LLL		
HHL	LHL	HLH	LLH	LLL		
HHH	LHL	HLH	LLH	LLL		
HH	LHL	HLH	LLH	LLL		

26c

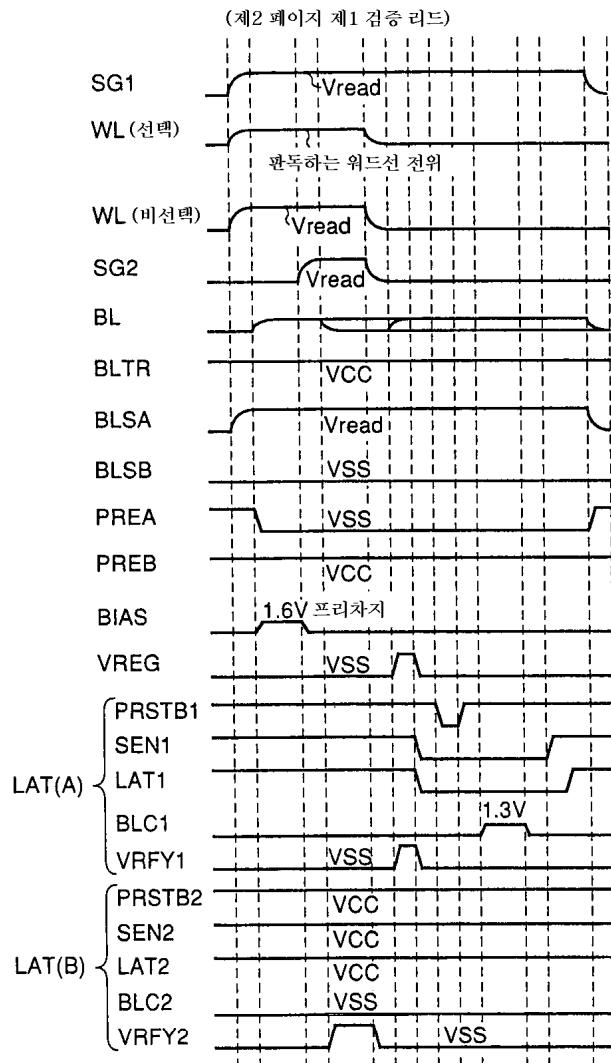
HH	LH	LH	HL	LL		
HL	LHH	LHL	HLL	LLL	c'로 리드	0~3
HH	LHH	LHL	HLL	LLL	A가 H일 때 비트선 HV(RFY1)	검증
HH	LHL	HLH	HLH	LLL	비트선의 전위를 A에 입력한다	
				LLL		

(inhibit=비)일, NSbit=비|선택 비트, A=LAT(A), B=LAT(B))

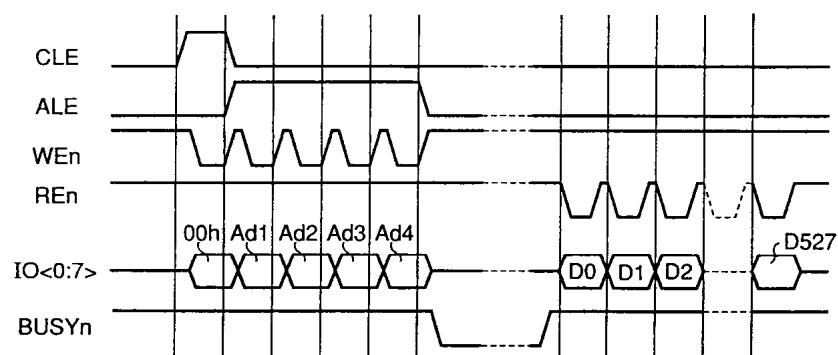
27



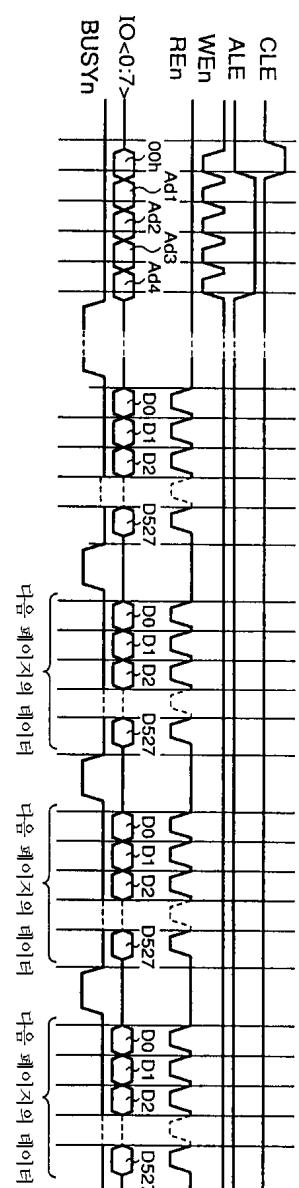
28



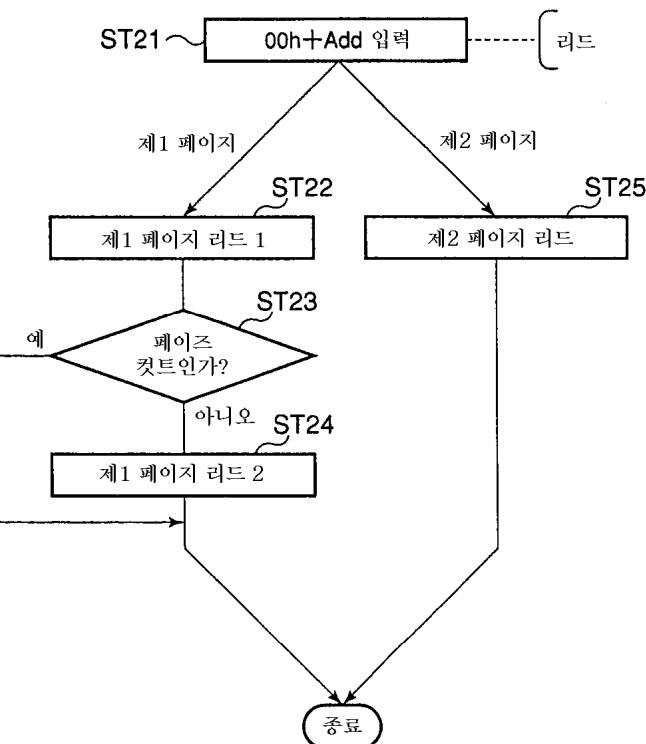
29



30



31



32

리드(제2 페이지)

상태 0,1	상태 2,3			
A B bit	A B bit			
L	H	b로 리드		제2 페이지 리드
L L	H H	비트선의 전위를 A로 래치		

(A=LAT(A)、B=LAT(B))

33a

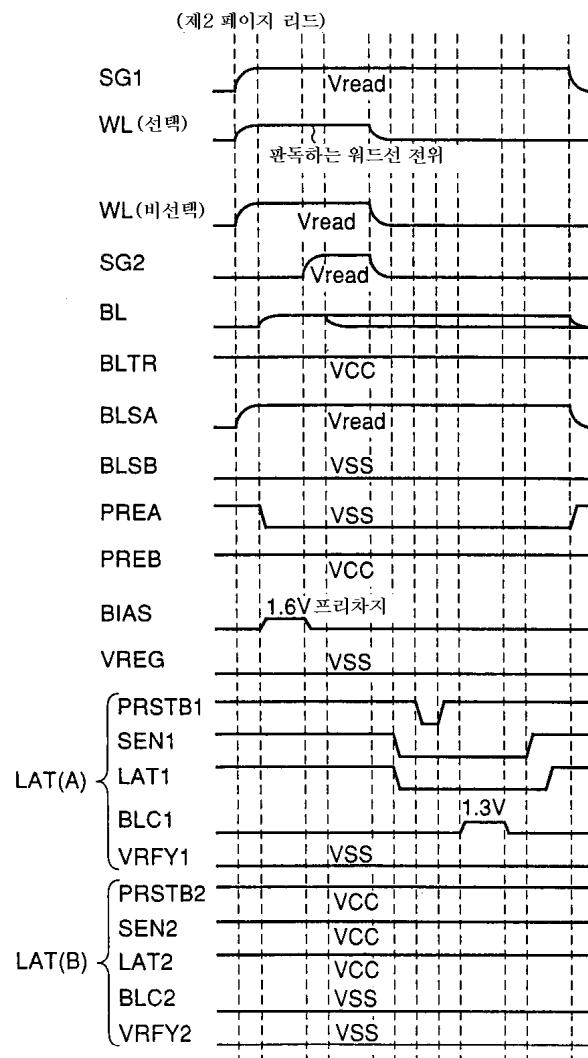
리드(제1 페이지)

상태 0	상태 1,2	상태 3			
A B bit	A B bit	A B bit			
L	L	H	c로 리드		
L L	L L	H H	비트선의 전위를 LAT(A)로 래치	제1의 리드	

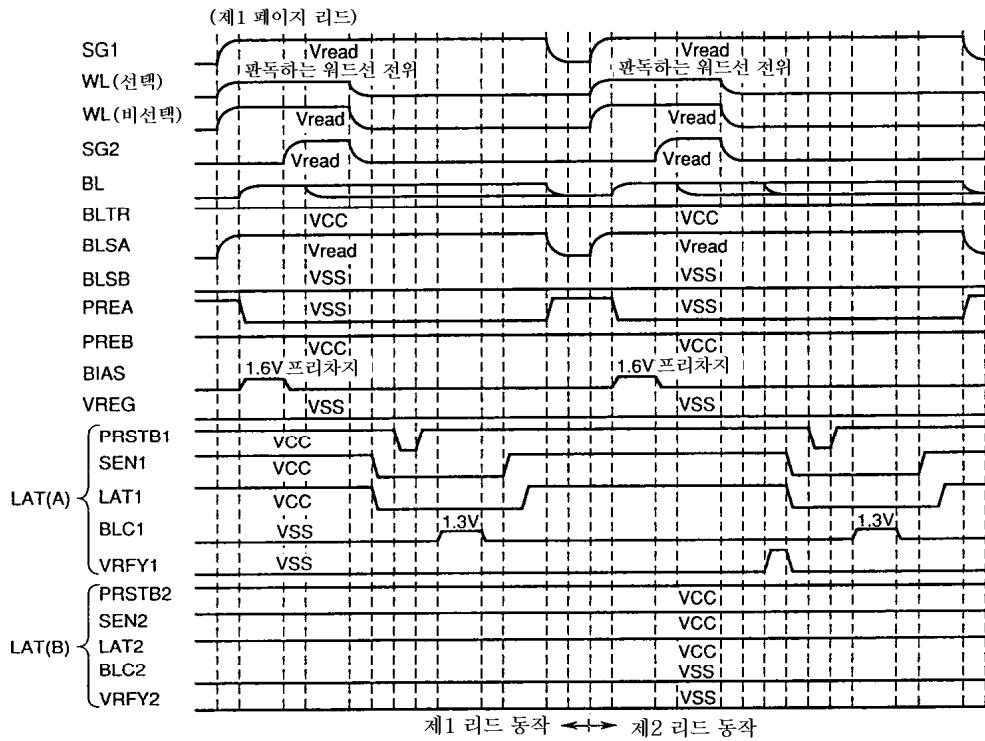
33b

L L	L H	H	a로 리드	
L L	L H	H L	LAT(A)가 H라면 비트선 L (VRFY1)	제2의 리드
L L	H H	L L	비트선의 전위를 A로 래치	

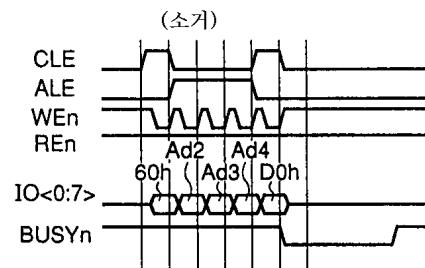
(A=LAT(A)、B=LAT(B))



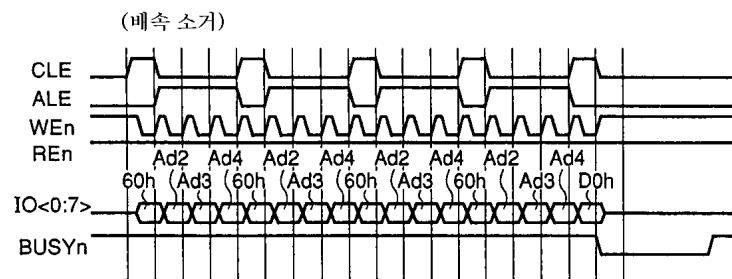
35



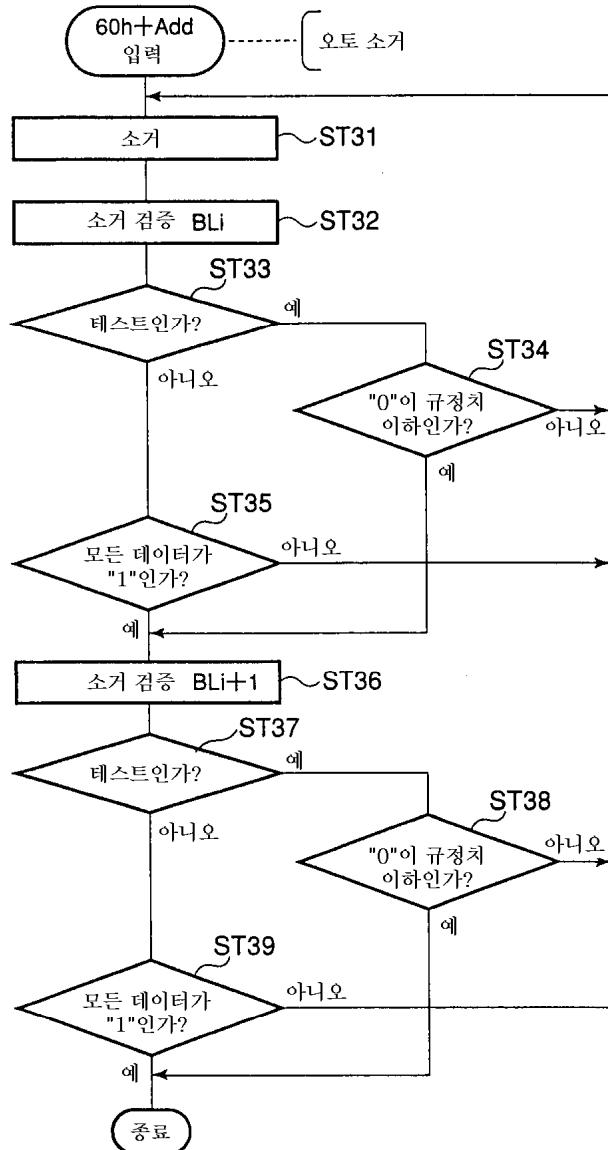
36

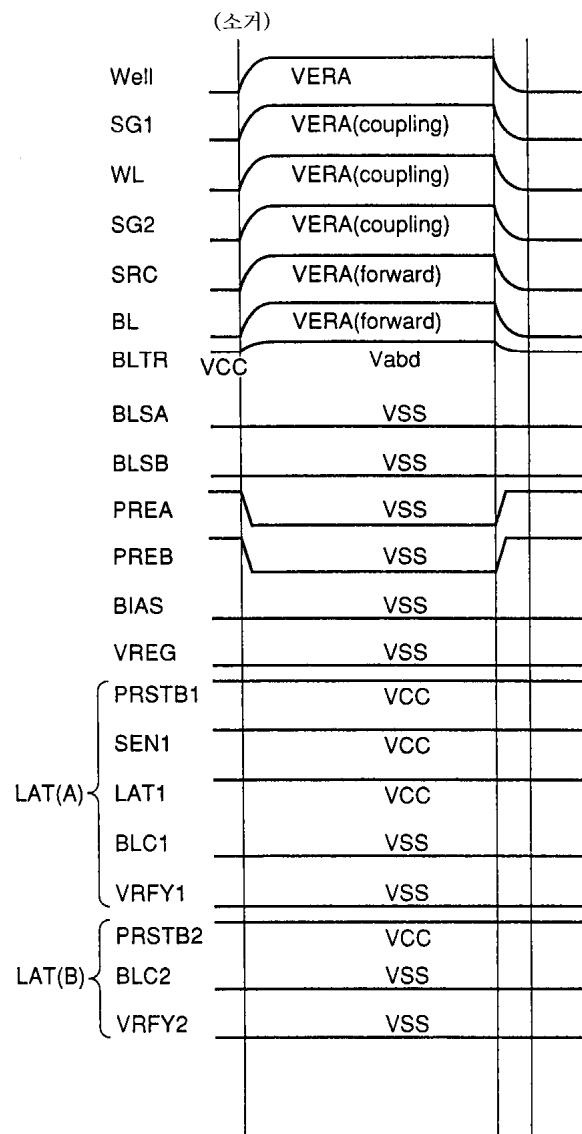


37

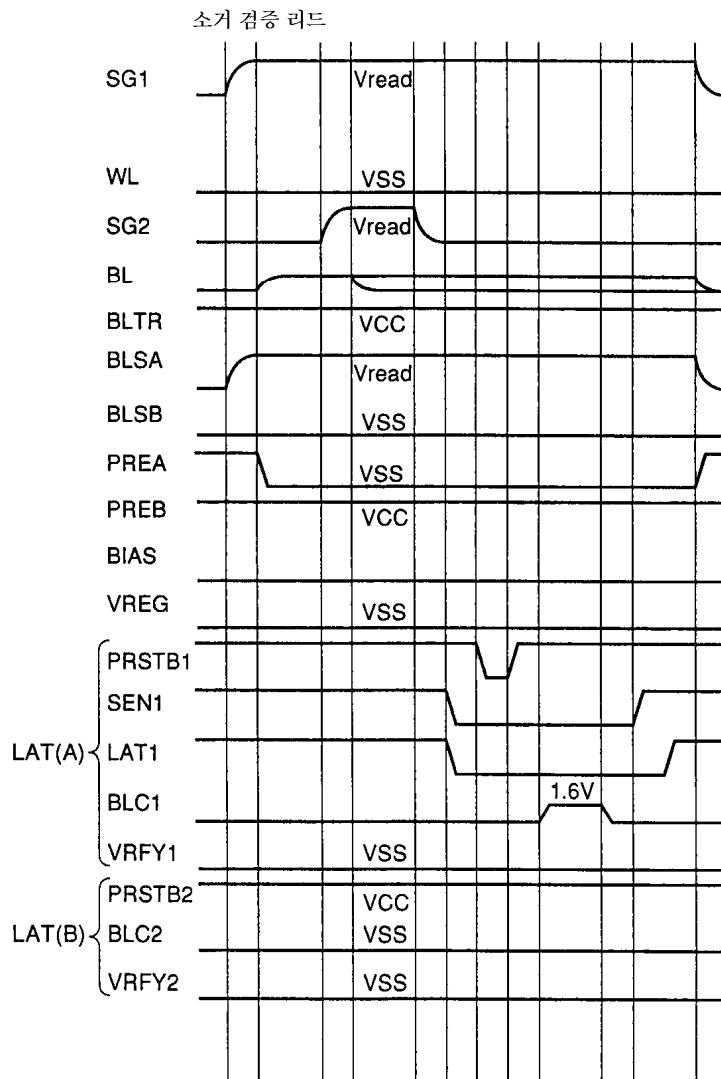


38

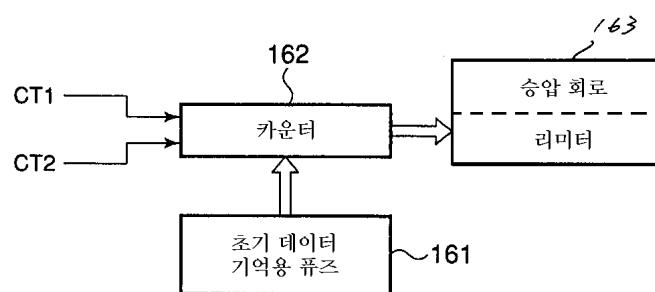


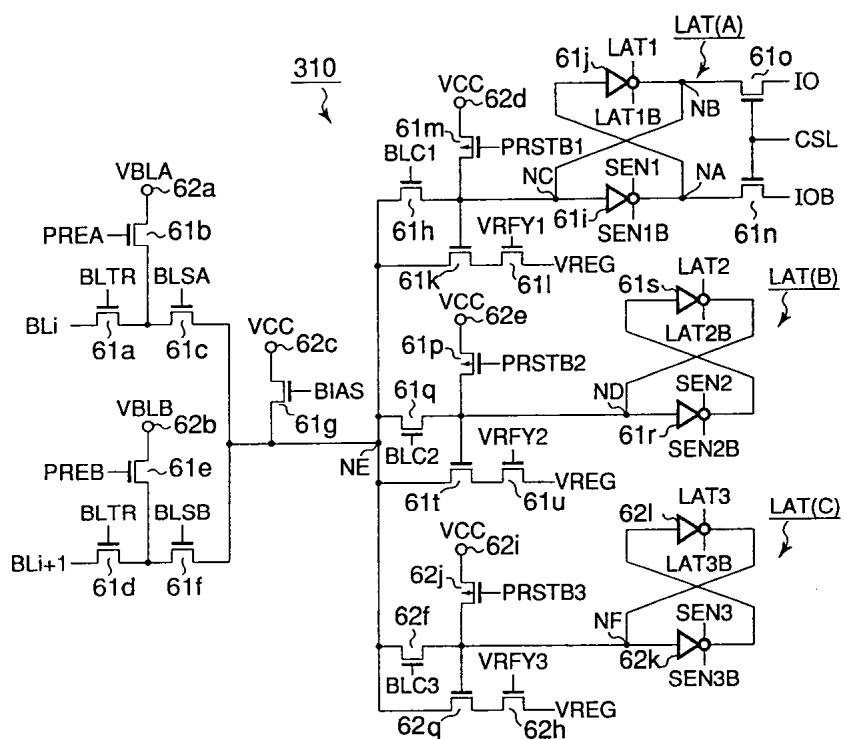


40

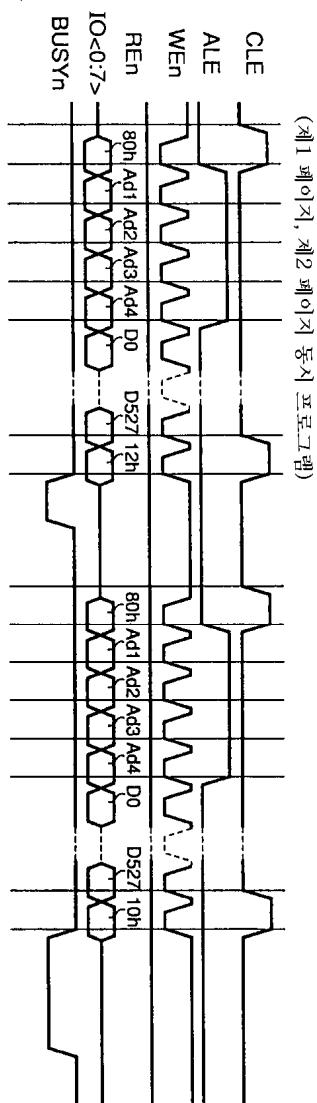


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프로그램 검증(제1, 제2 페이지 풋지)							
상태 0	상태 0→1	상태 0→2	상태 0→3	메모리 셸의 데이터			
Inhibit	Write(OK)	Write(NG)	Write(OK)	Write(OK)	Write(NG)		
A B C bit NS bit	A B C bit NS bit	A B C bit NS bit	A B C bit NS bit	A B C bit NS bit	A B C bit NS bit		
H	L	L	H	비밀 풋지(A에 write→L, inhibit→H) B를 H로 카운트 A가 H일 때 B를 H→L			
HH	L H	L H	HH				
HL	L H	L H	HL				

(inhibit= H) 가 유효, NSbit= 비 선택 비트, A=LAT(A), B=LAT(B), C=LAT(C))

45a

프로그램 검증(제1, 제2 페이지 동시에)											
상태0	상태0→1		상태0→2		상태0→3		메모리셀의 데이터				
inhibit ABC bit NS bit	Write(OK) ABC bit NS bit	Write(NG) ABC bit NS bit	Write(OK) ABC bit NS bit	Write(NG) ABC bit NS bit	Write(OK) ABC bit NS bit	Write(NG) ABC bit NS bit	Write(OK) ABC bit NS bit	Write(NG) ABC bit NS bit	Write(OK) ABC bit NS bit	Write(NG) ABC bit NS bit	
HL	HH	LH	LL	데이터 로드(A에 write→inhibit→H)							
HL	HH	LH	LL	C를 H로 리셋							
HL	HH	LH	LL	A가 H일 때 C를 H→L							
HL	HH	LH	LL	B가 H일 때 선택 비트선 H							
HL	HH	LH	LL	B가 H일 때 선택 비트선 L							
HL	HH	LH	LL	선택 비트를 A에 꾸acle한다							
HL	HH	LH	LL	B를 H로 리셋							
HL	HH	LH	LL	A가 H일 때 B를 H→L							
HL	HH	LH	LL	비선택 비트를 A에 꾸acle한다							

45b

HL LL LH LLH LHL LHH	UL LL LH LLH LHL LHH	LH HL HH HL HL HH	a.로 리드 C가 H일 때 비트선 L (VRRYZ) A가 H일 때 비트선 M (VRRYI) 비트선의 전위를 A에 담백한다	0→1 검증
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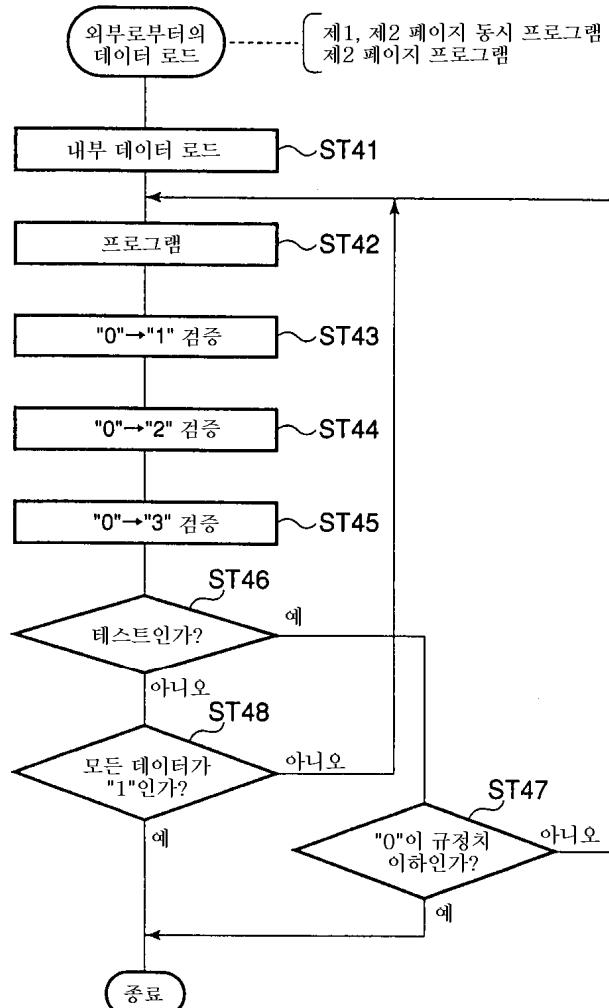
45c

HL	LL	UL	LH	b;로 리드
HL	LL	UL	LH	B가 H에 비트선 LV(RFV2)
HL	LL	UL	LH	A가 H에 비트선 HV(RFV1)
HL	LL	UL	LH	비트선의 전류를 A에 입력한다
HL	LL	UL	LH	

45d

HLLL	LLLL	LLHL	LHHH	LHHL	c로 뒤드 A가 H일때 비트선 HVVRFYI 비트선의 전위를 A에 입력한다	D-3 8
HLLH	LLLL	LLHL	LHHH	LHHL		
HLLH	LLLL	LLHL	LHHH	LHHL		

(inhibit=비기압, NSbit=비선택 비트, A=LAT(A), B=LAT(B), C=LAT(C))



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