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(54) COMPOUND SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

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(21) Appl. No.: **09/880,867**

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Related U.S. Application Data

(62) Division of application No. 09/330,085, filed on Jun. 11, 1999, now Pat. No. 6,274,893.

(30) **Foreign Application Priority Data**

Jul. 31, 1998 (JP) 10-217833
Jun. 15, 1998 (JP) 10-166734

Publication Classification

(51) **Int. Cl.**[7] **H01L 31/112**
(52) **U.S. Cl.** **257/192**; 257/280

(57) **ABSTRACT**

The impurity concentration contained in a layer on an electron supply layer of a high electron mobility field effect transistor is set in the range of 1×10^{16} to 1×10^{17} atoms/cm^3, or the bandgap of a Schottky layer is set wider than that of the electron supply layer. Otherwise, in the steps of manufacturing the high electron mobility field effect transistor, after a silicon nitride film has been formed on a GaAs buried layer in which a second recess is formed and in a region on the inside of a first recess formed in a GaAs contact layer, the GaAs buried layer is still heated.

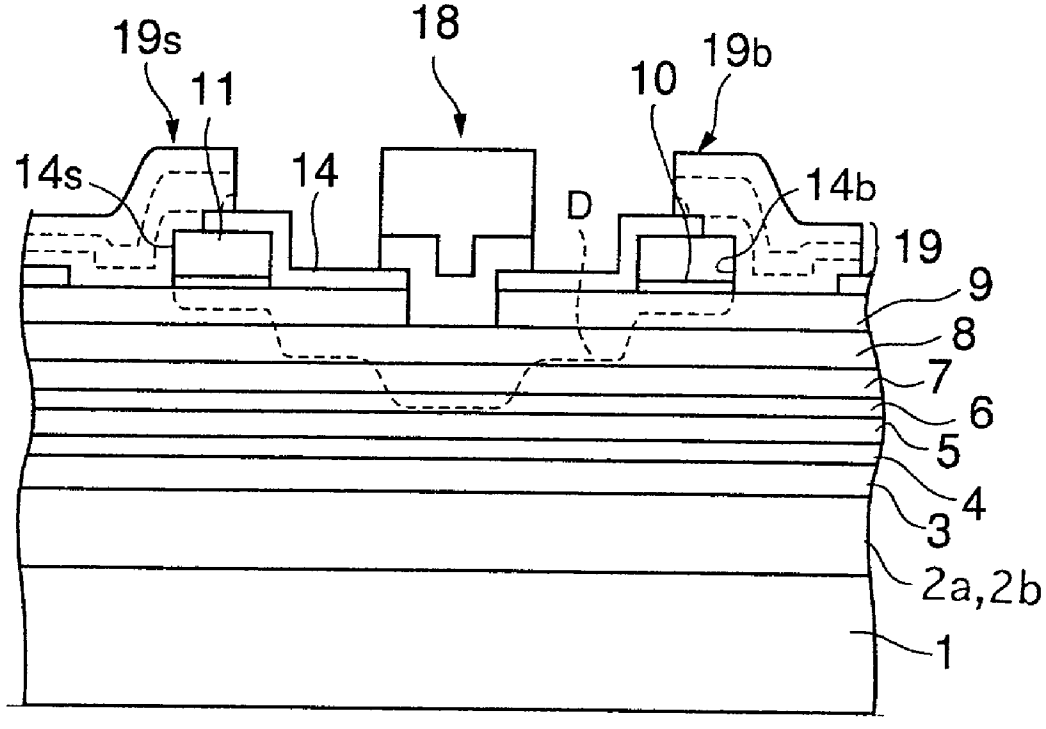


FIG. 1 (Prior Art)

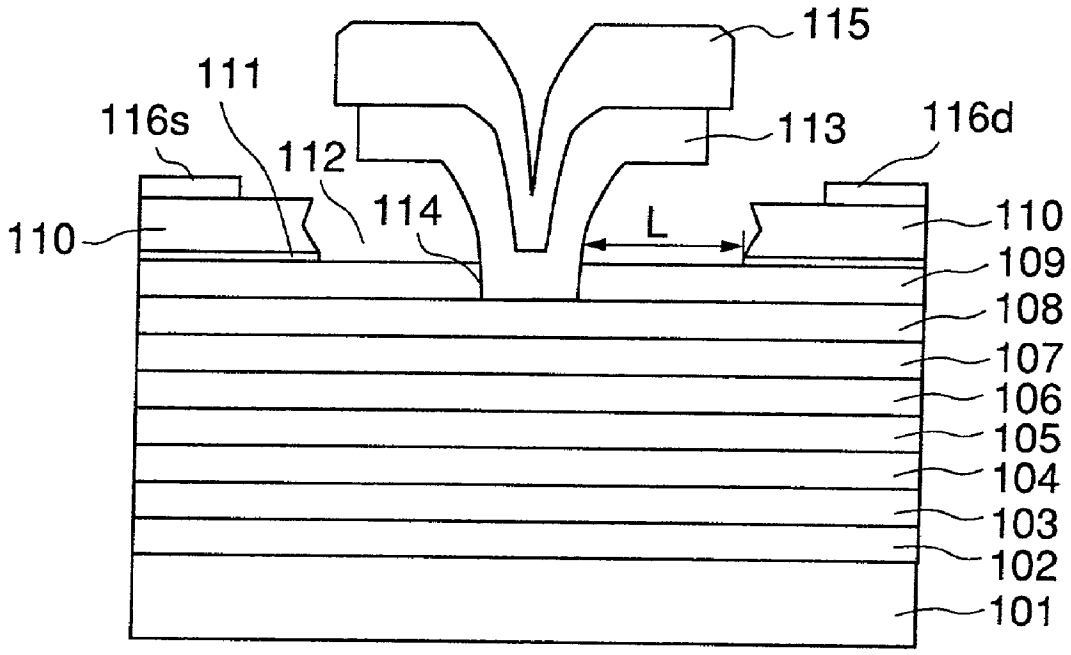


FIG. 2A

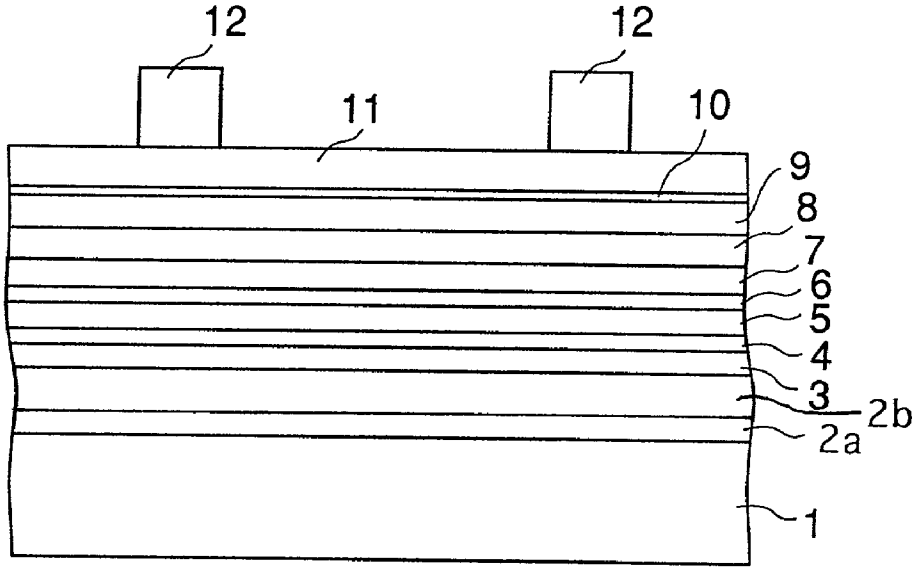


FIG. 2B

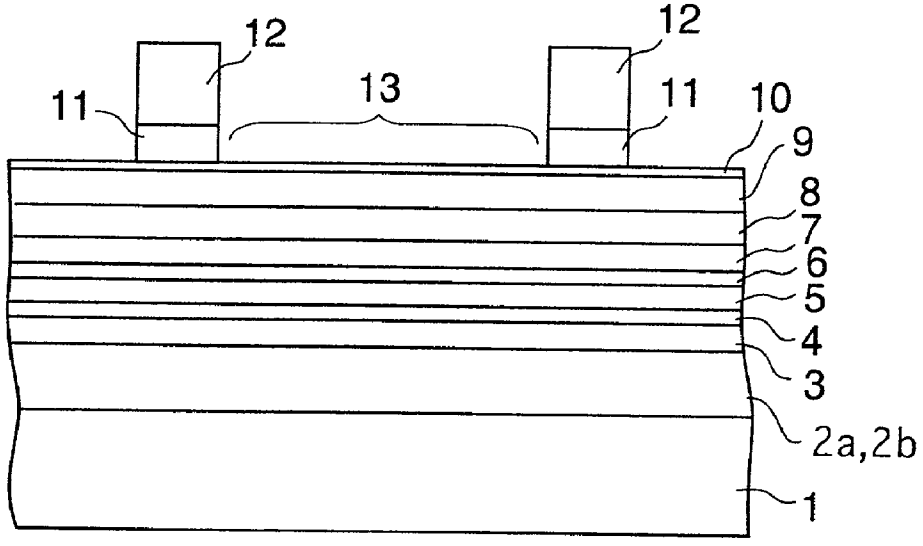


FIG. 2C

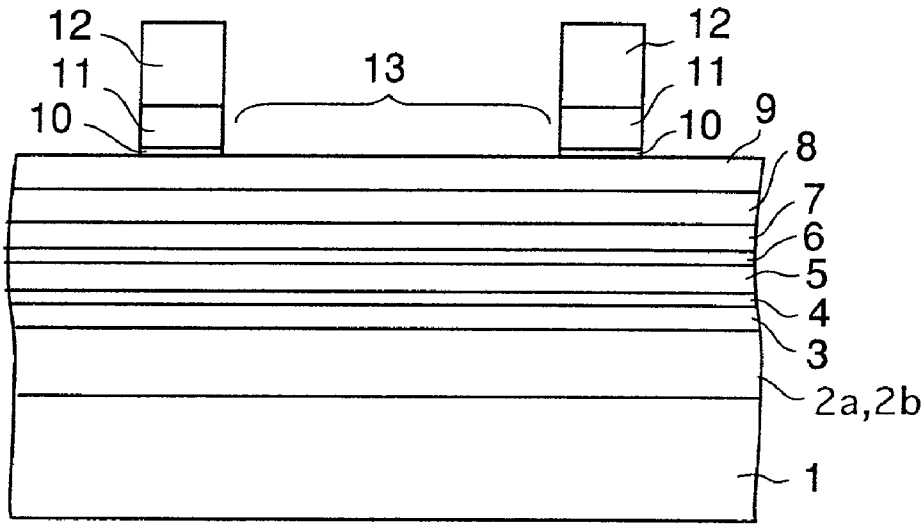


FIG. 2D

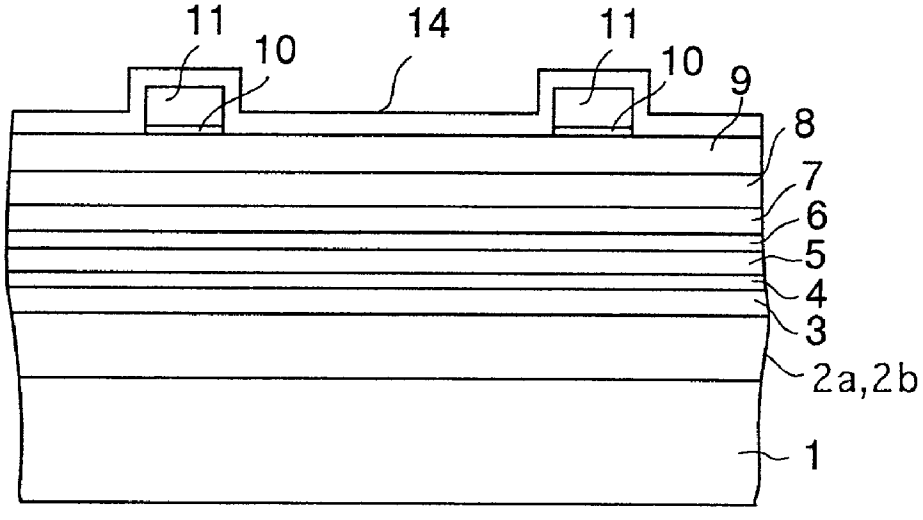
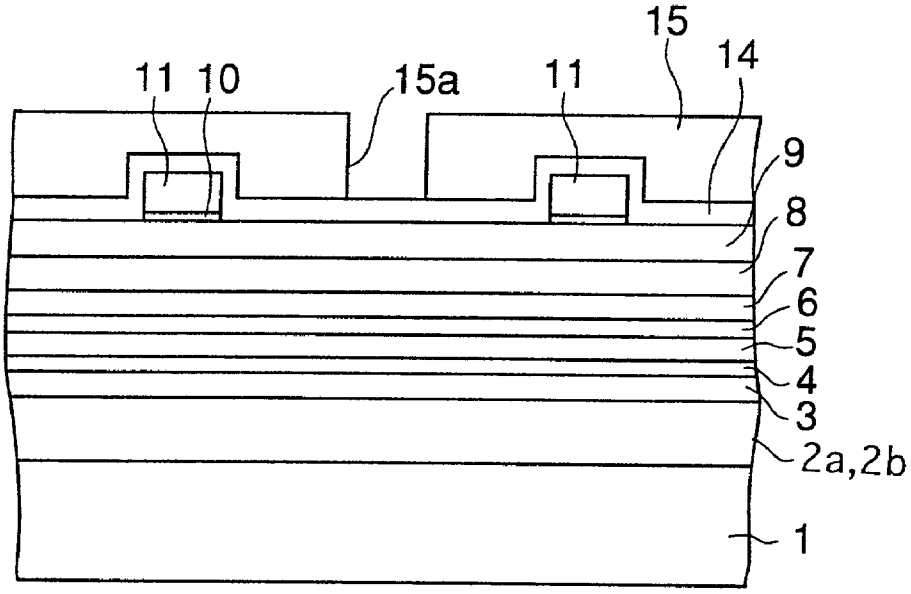


FIG. 2E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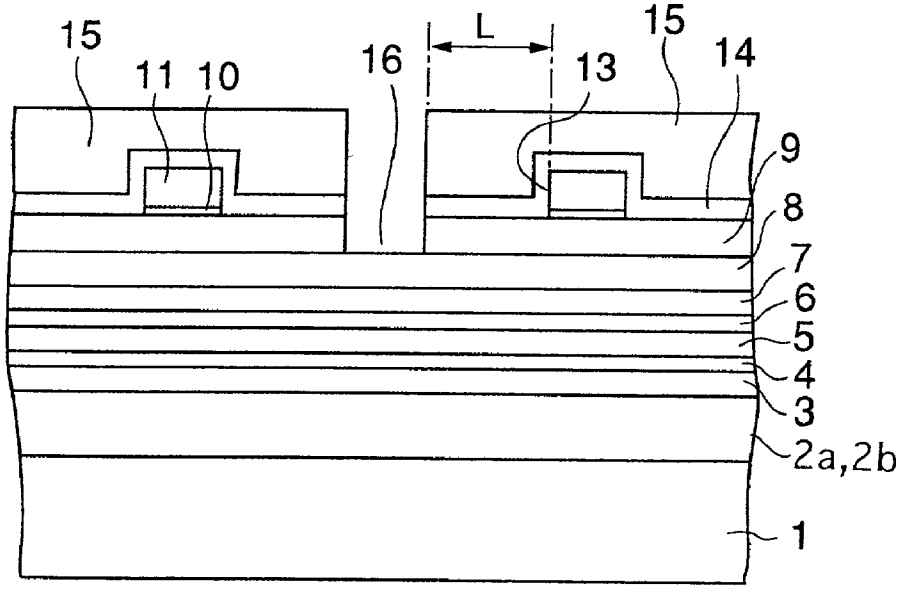
14
11 10
15a
11
9
8
7
6
5
4
3
2a,2b
1

FIG. 2F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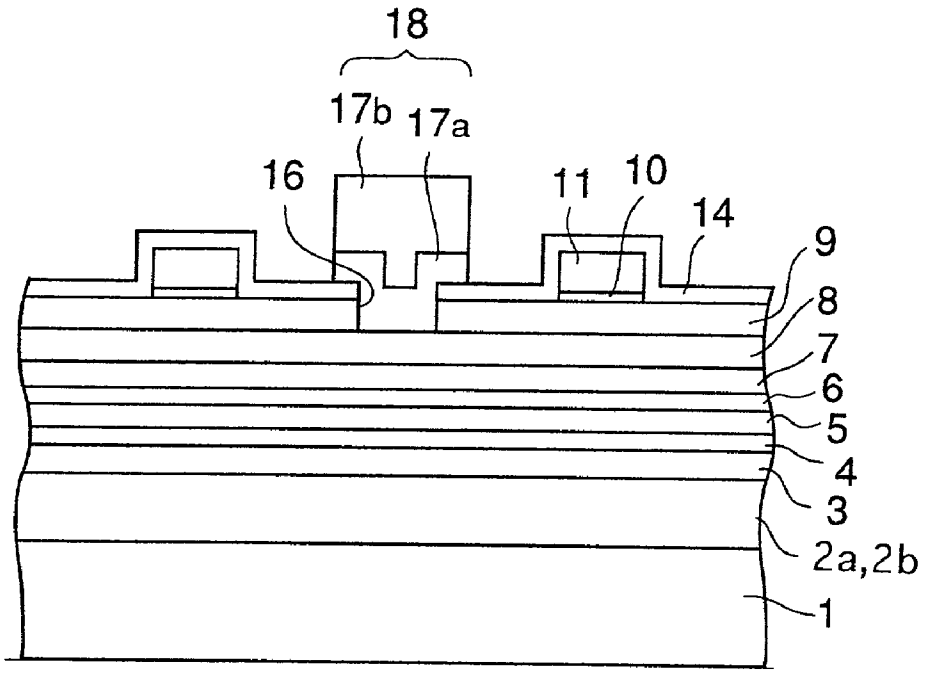
L
15
16
13
14
11 10
9
8
7
6
5
4
3
2a,2b
1

FIG. 2G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17b
17a
16
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14
9
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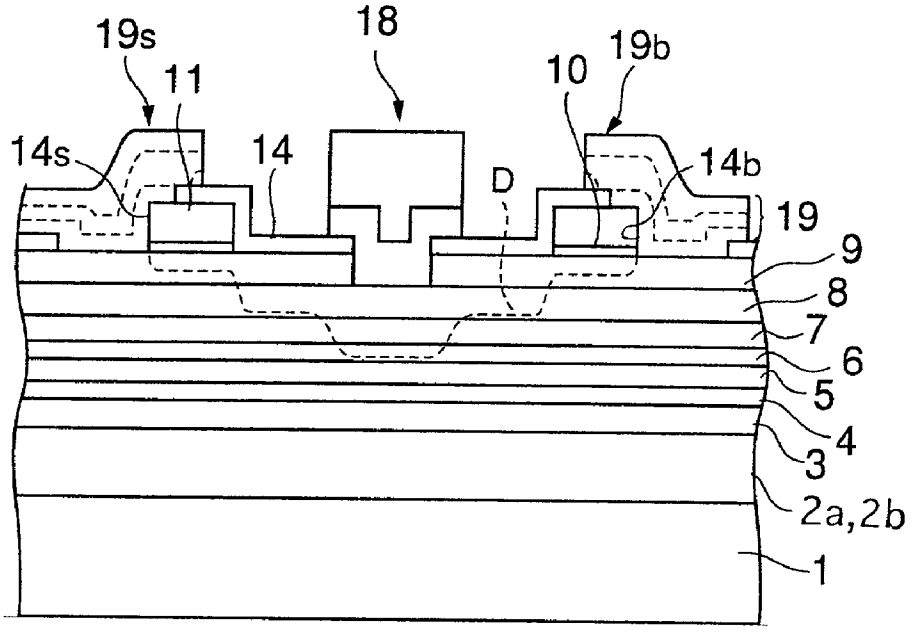
7
6
5
4
3
2a,2b
1

FIG. 2H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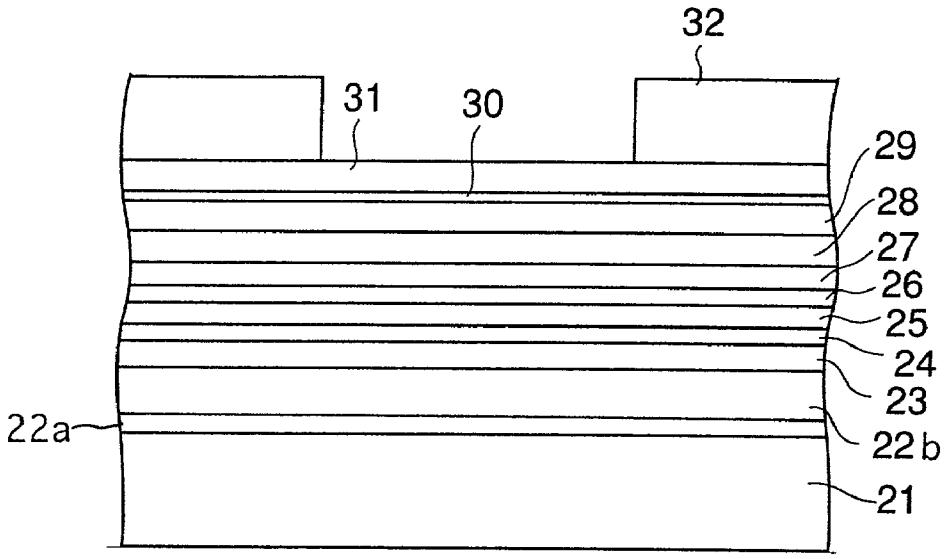
11
18
10
19b
14s
14
D
14b
19
9
8
7
6
5
4
3
2a,2b
1

FIG. 3A


32
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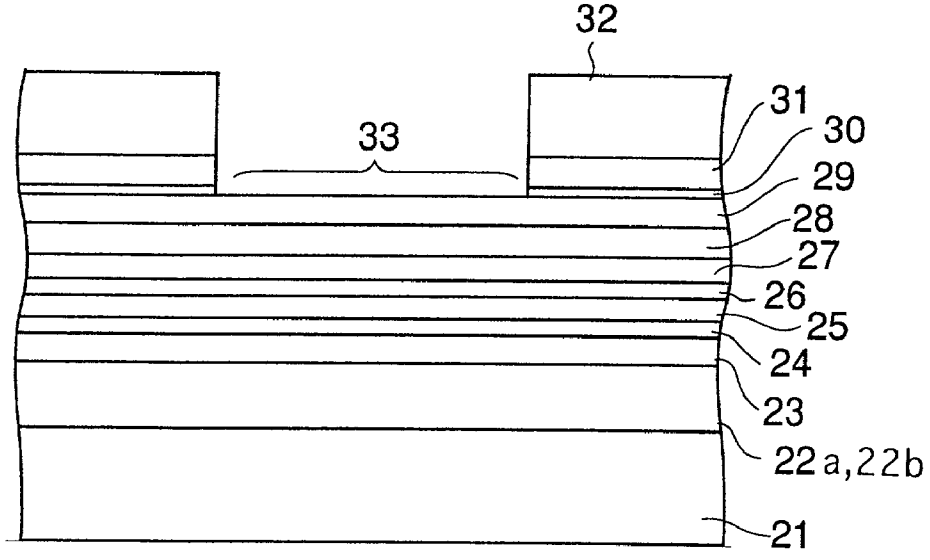
28
27
26
25
24
23
22a
22b
21

FIG. 3B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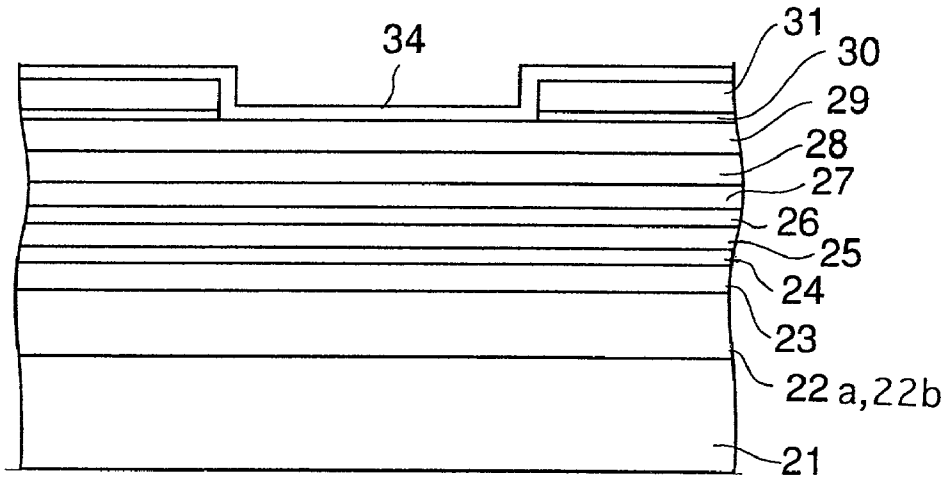
29
28
27
26
25
24
23
22a,22b
21

FIG. 3C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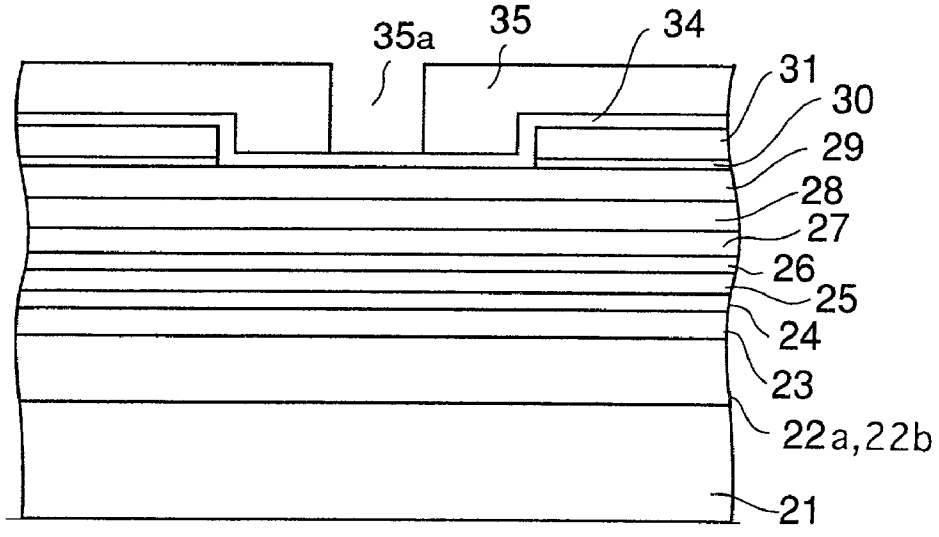
28
27
26
25
24
23
22a,22b
21

FIG. 3D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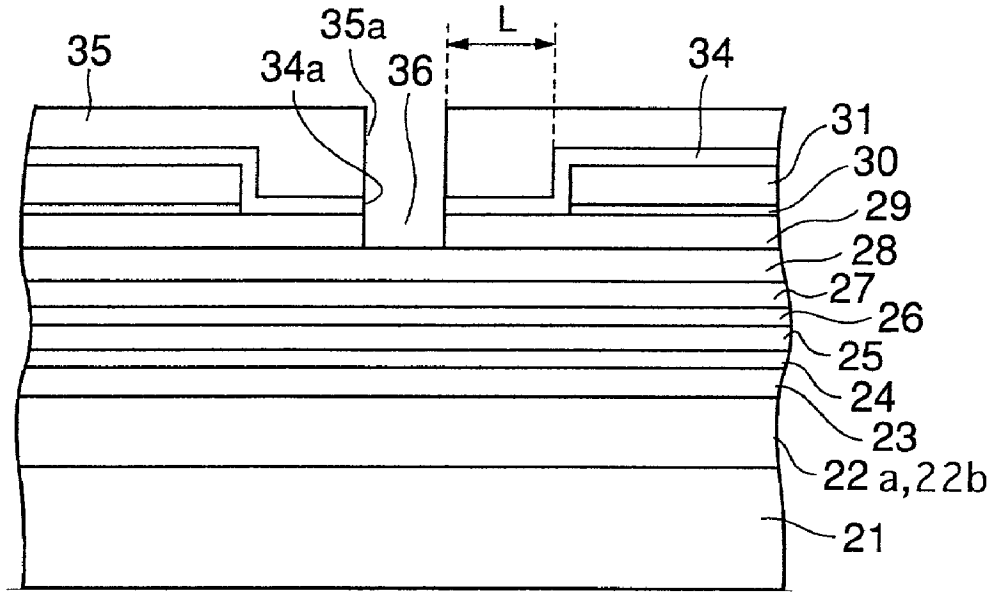
31
30
29
28
27
26
25
24
23
22a,22b
21

FIG. 3E


35
35a
34a
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26
25
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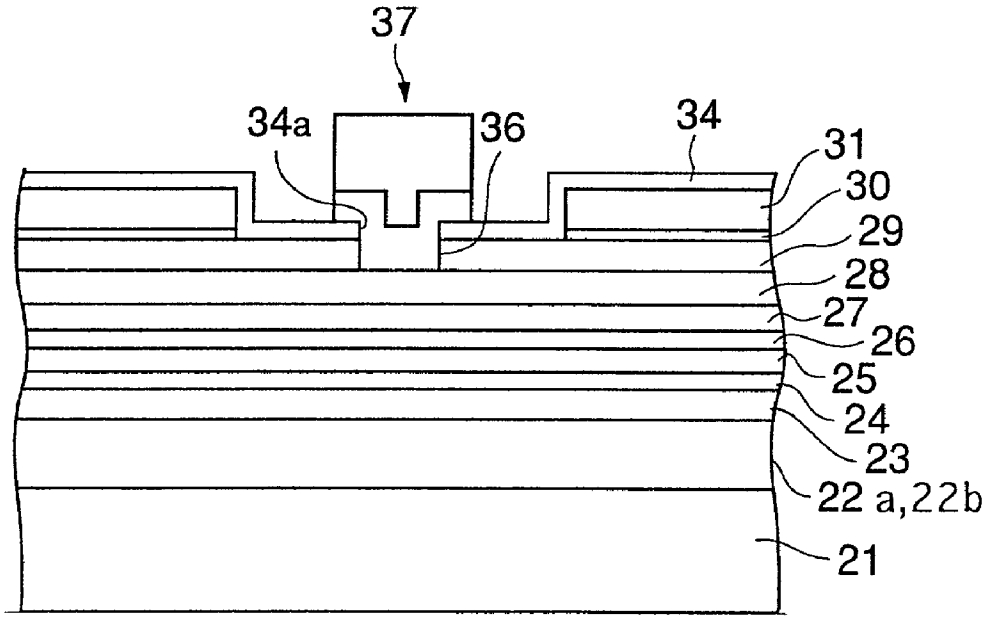
23
22 a,22b
21

FIG. 3F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27
26
25
24
23
22 a,22b
21

FIG. 3G

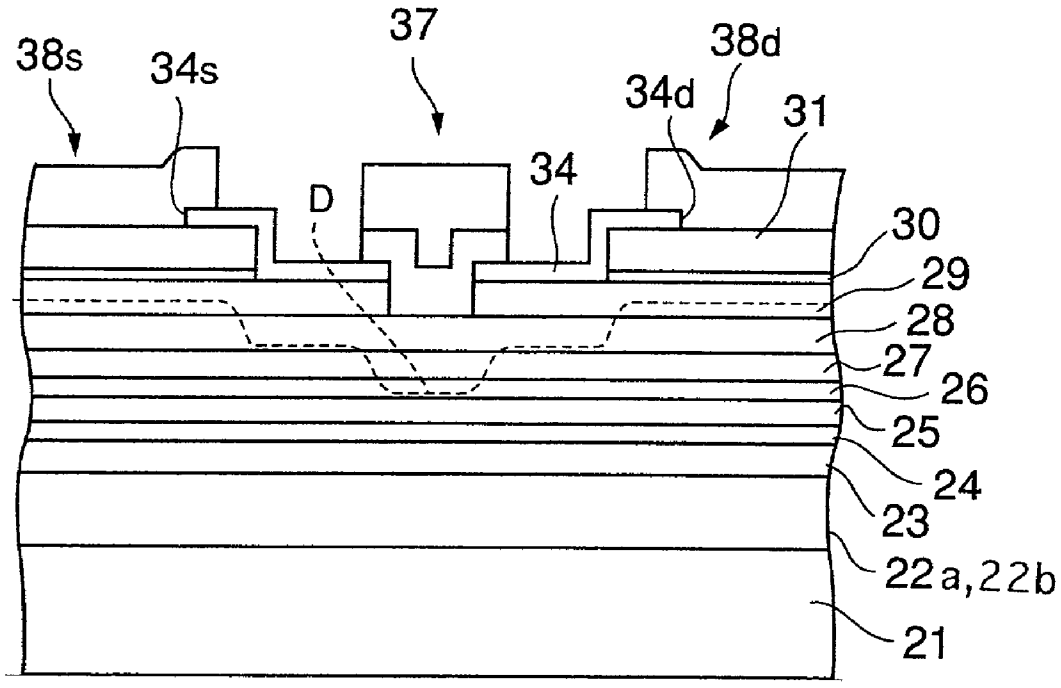


FIG. 4

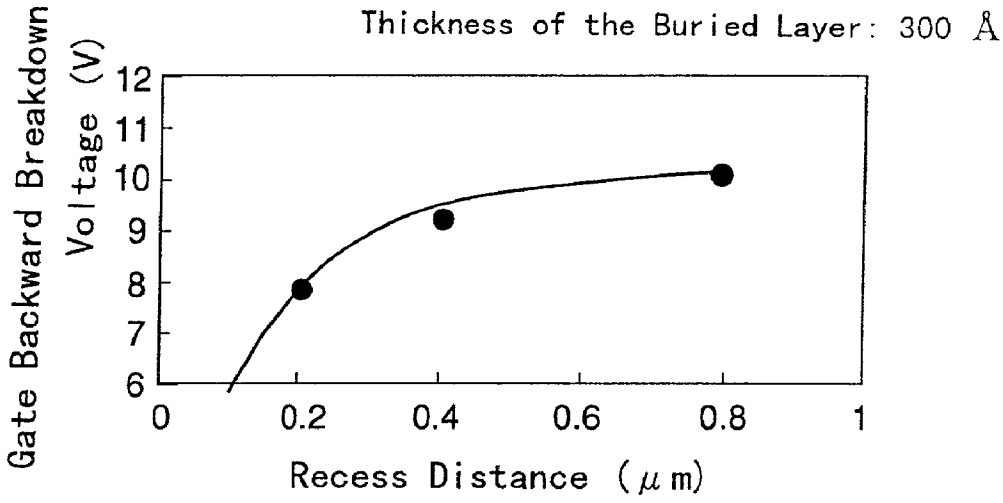

Thickness of the Buried Layer: 300 Å
Gate Backward Breakdown Voltage (V)
12
11
10
9
8
7
6
0
0.2
0.4
0.6
0.8
1
Recess Distance (μm)

FIG. 5

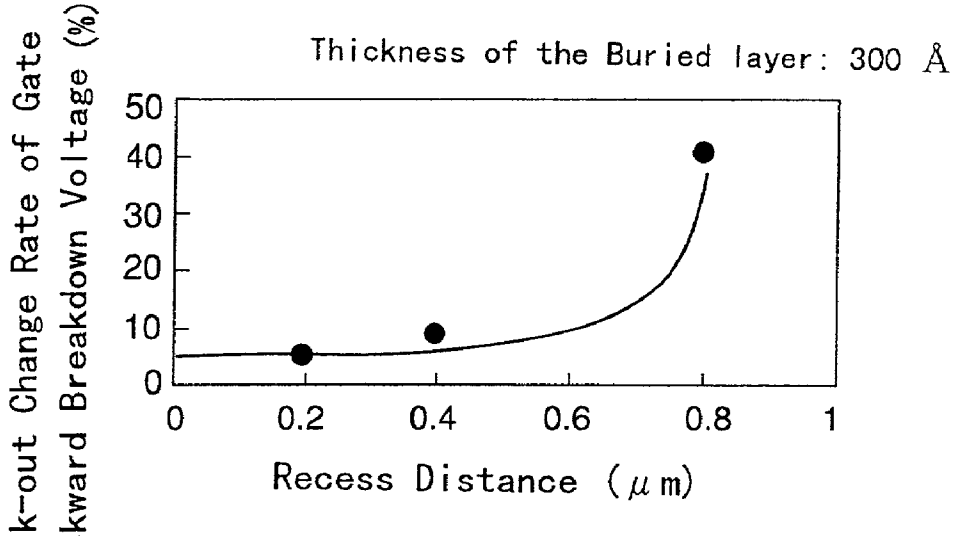

Thickness of the Buried layer: 300 Å
Walk-out Change Rate of Gate Backward Breakdown Voltage (%)
50
40
30
20
10
0
0
0.2
0.4
0.6
0.8
1
Recess Distance (μm)

FIG. 6

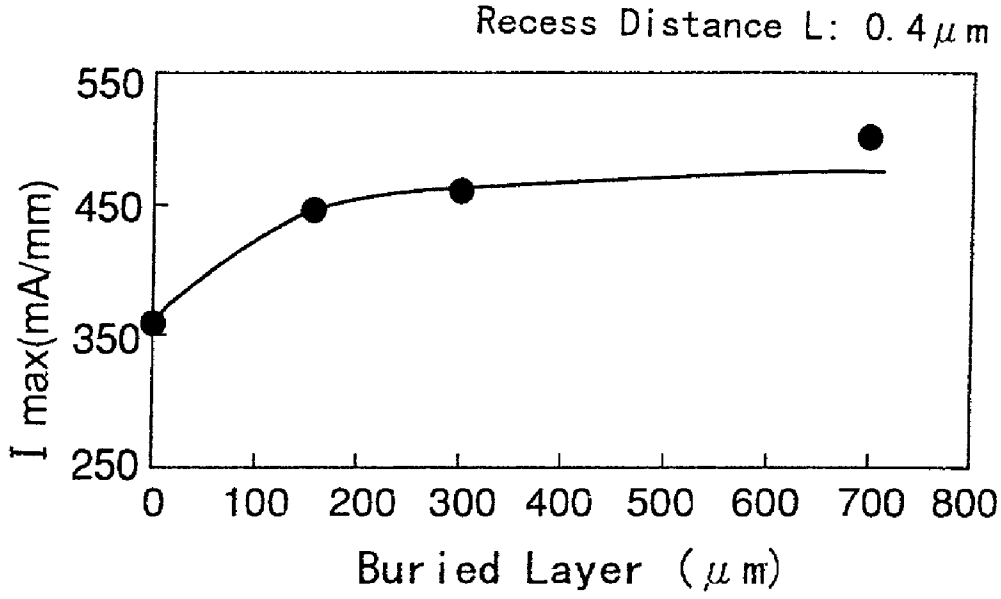

Recess Distance L: 0.4μm
I max(mA/mm)
550
450
350
250
0
100
200
300
400
500
600
700
800
Buried Layer (μm)

FIG. 7

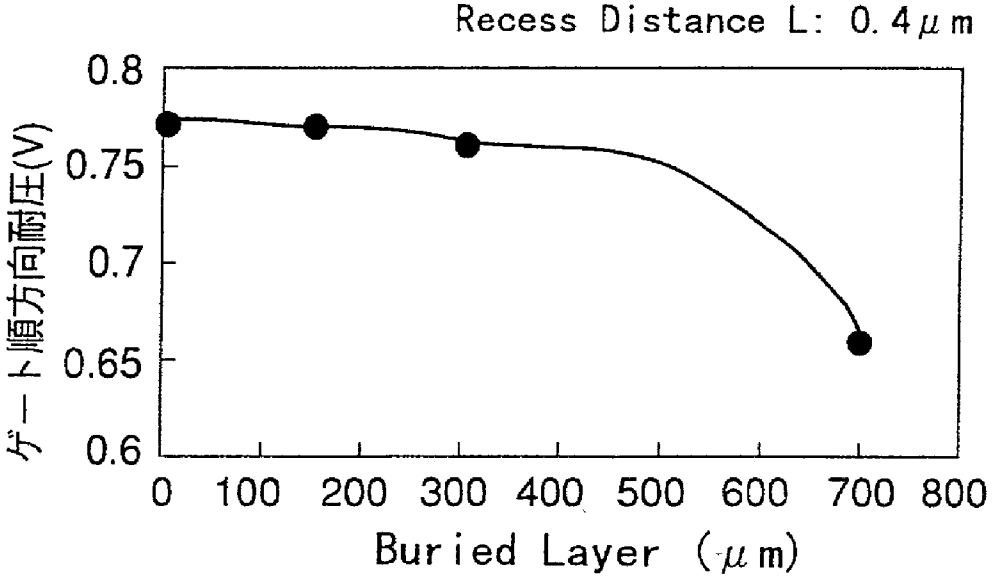

Recess Distance L: 0.4μm
ゲート順方向耐圧(V)
0.8
0.75
0.7
0.65
0.6
0
100
200
300
400
500
600
700
800
Buried Layer (μm)

FIG. 8

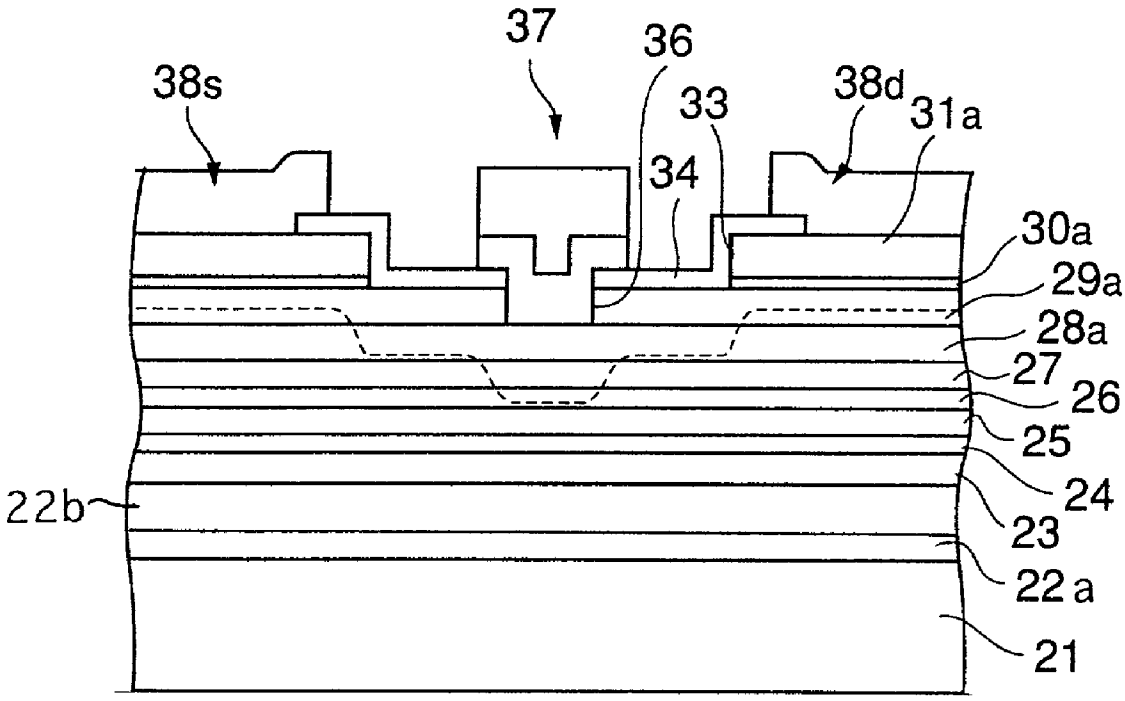


FIG. 9

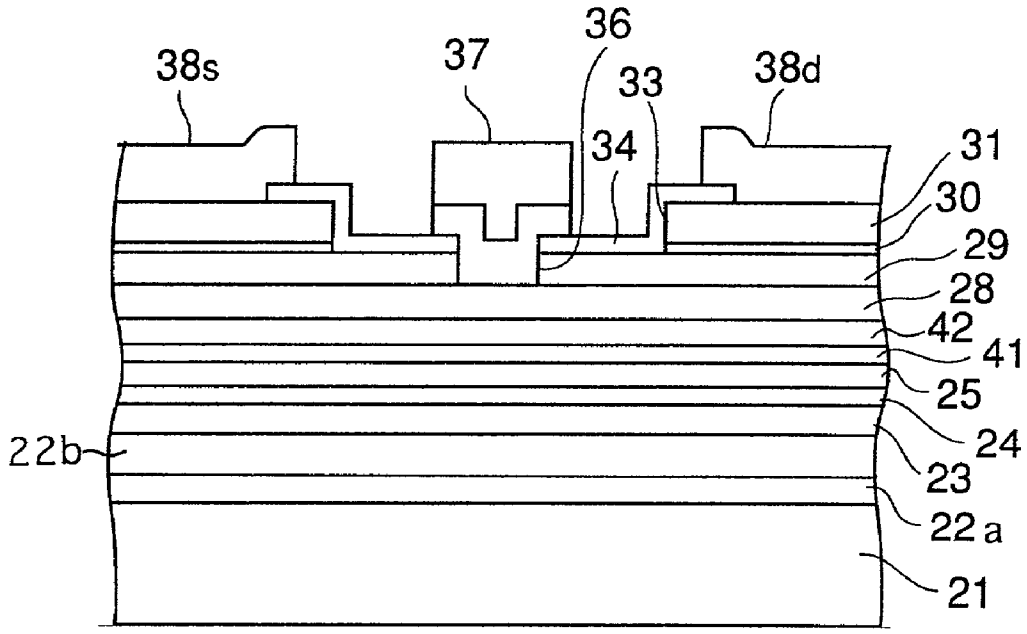


FIG. 10

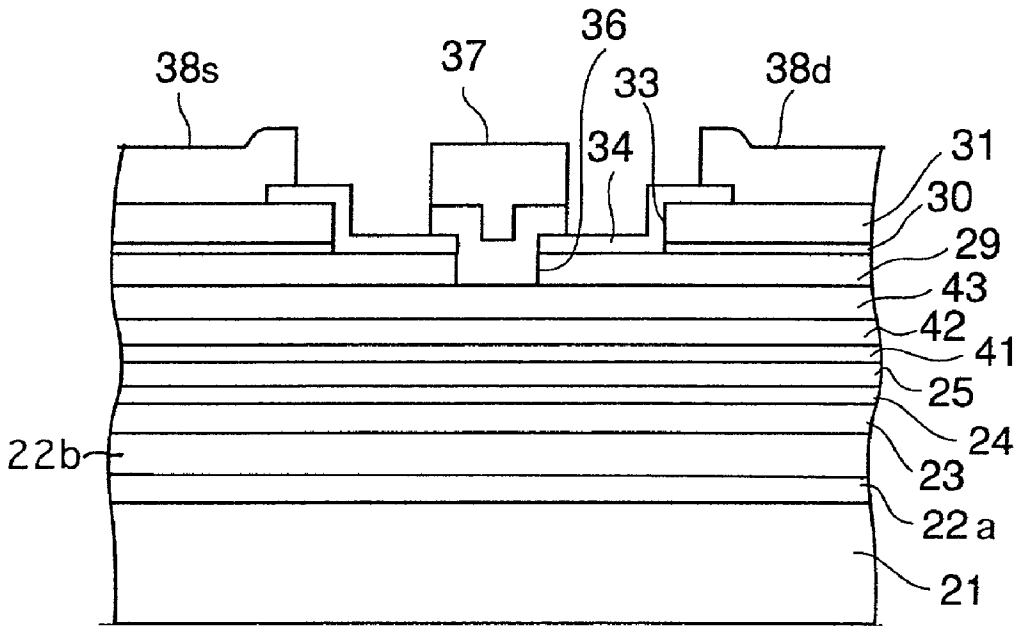


FIG. 11

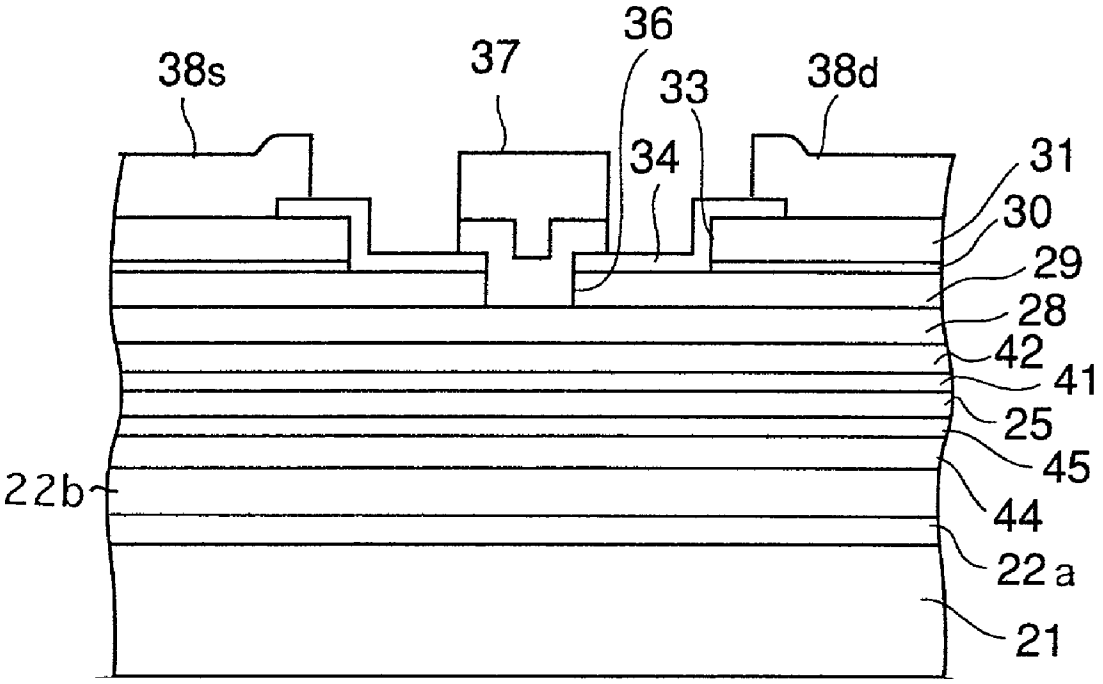


FIG. 12

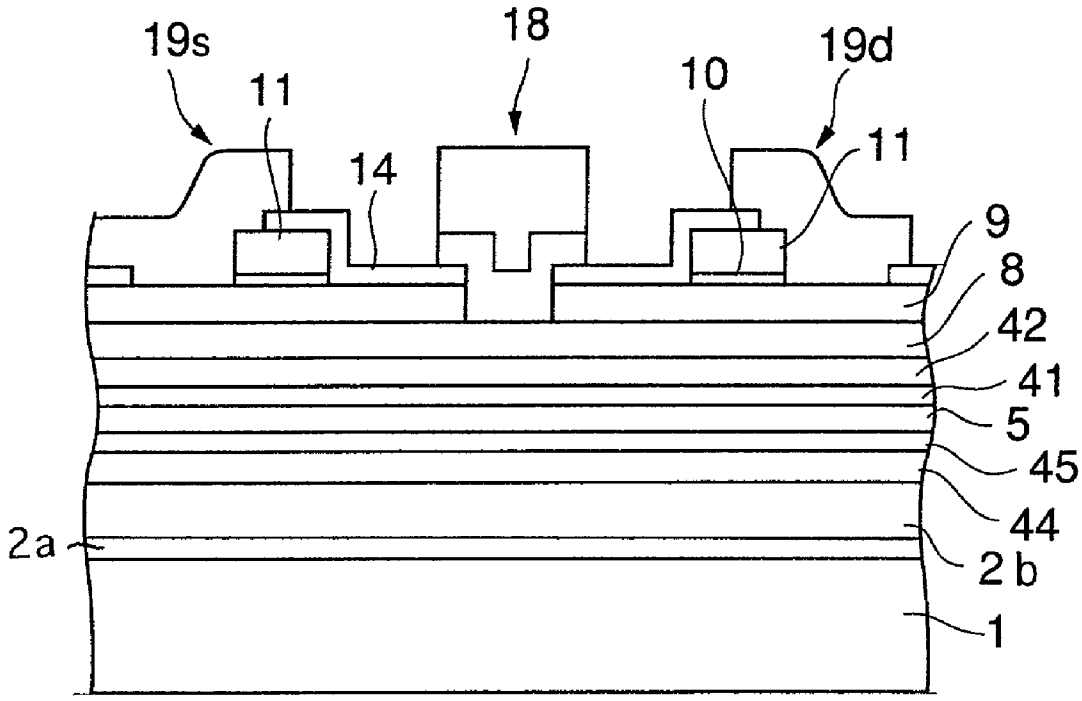


FIG. 13

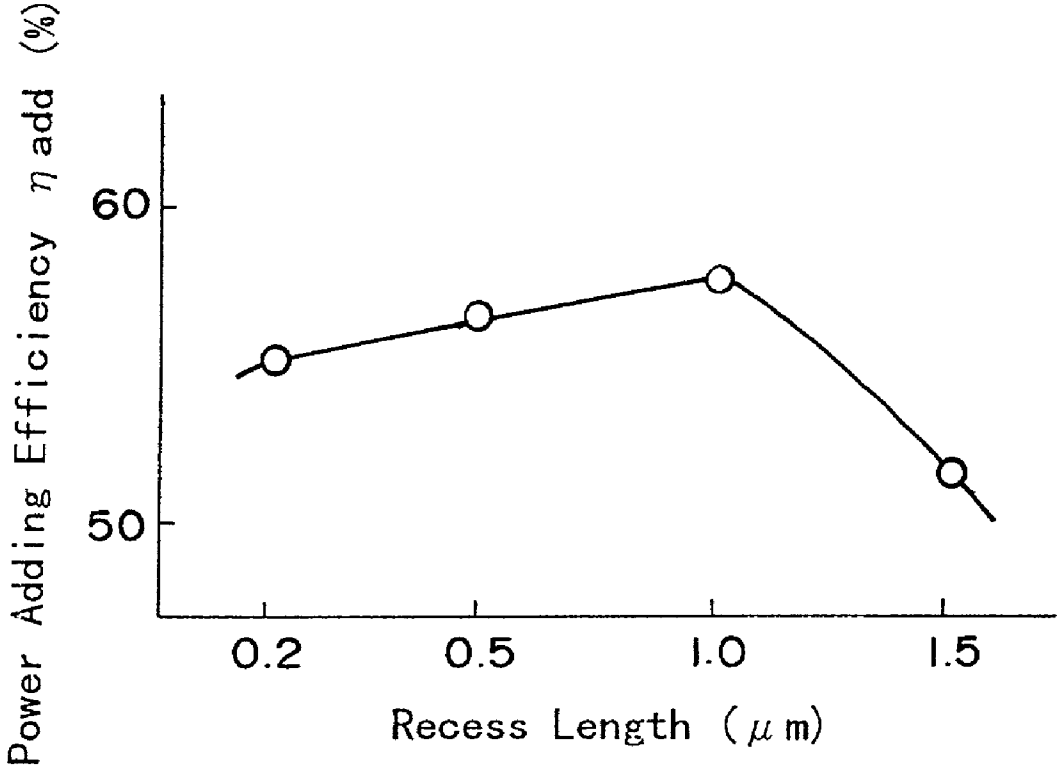

Power Adding Efficiency η add (%)
60
50
0.2
0.5
1.0
1.5
Recess Length (μm)

FIG. 14A

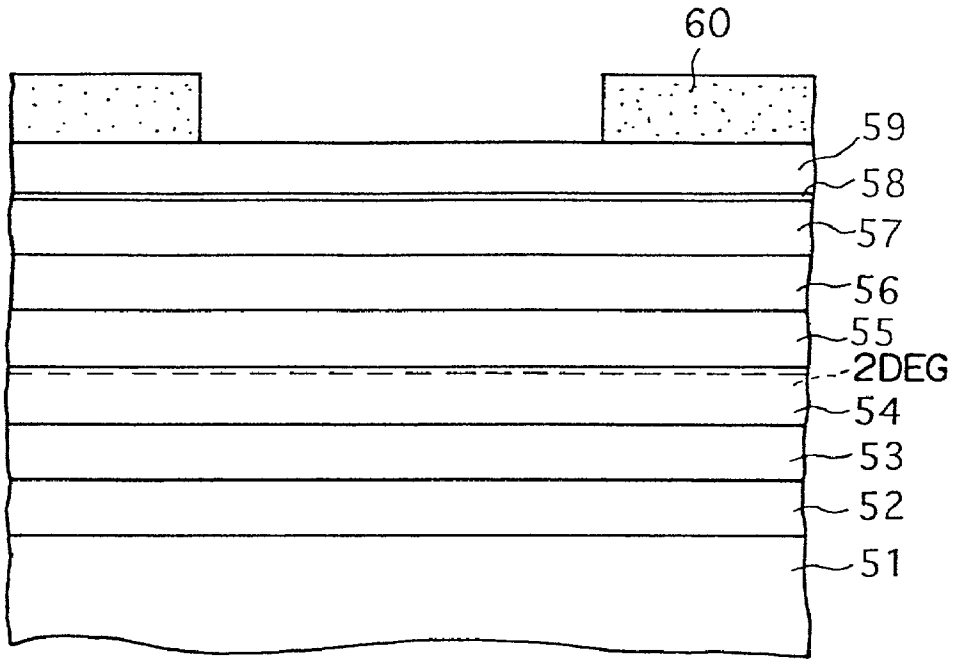


FIG. 14B

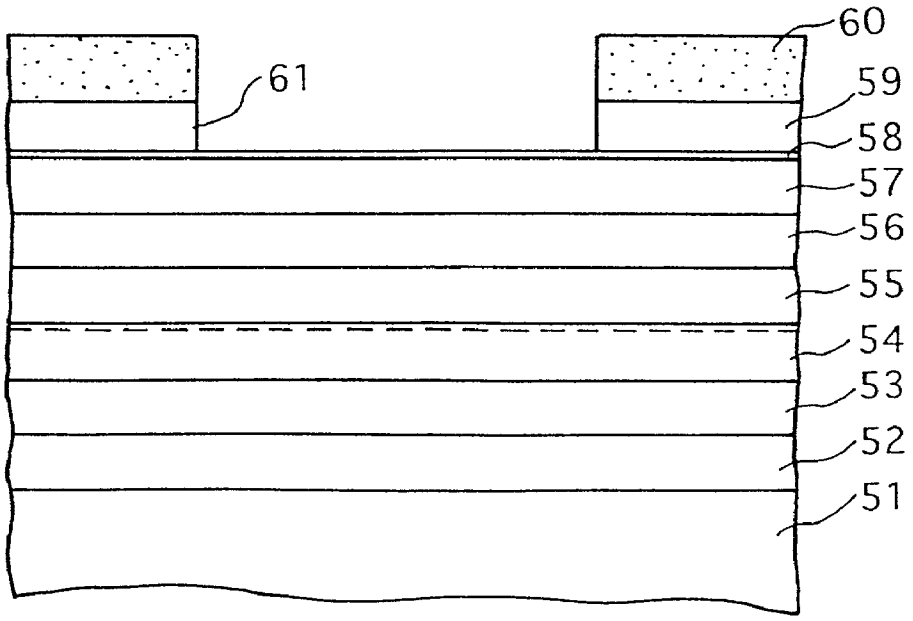


FIG. 14C

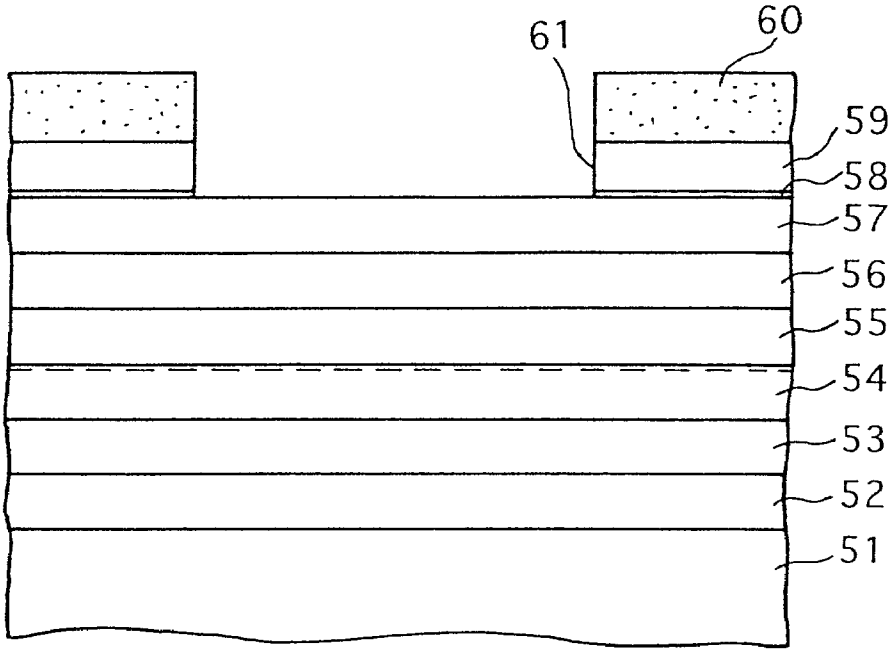


FIG. 14D

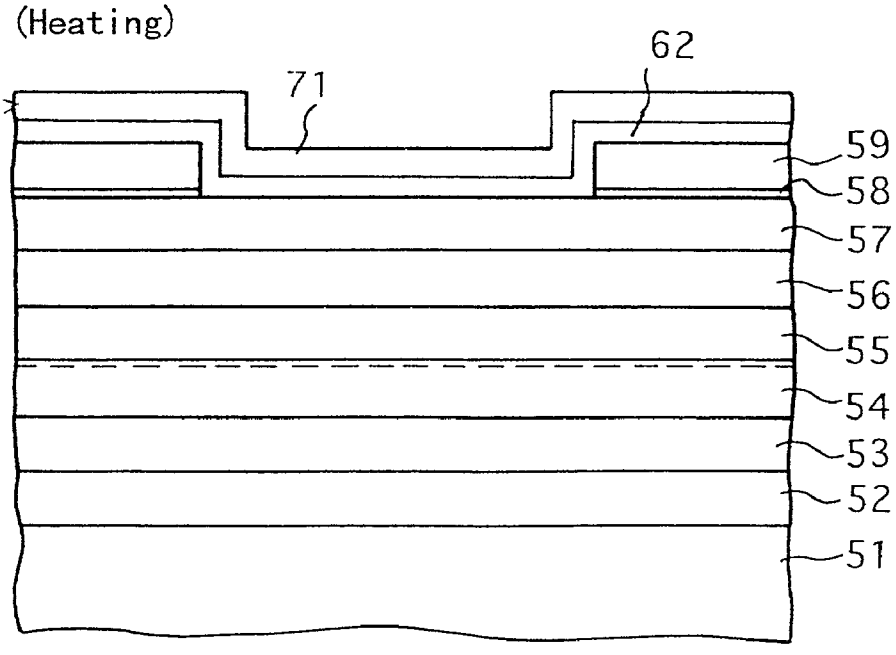


FIG. 14E

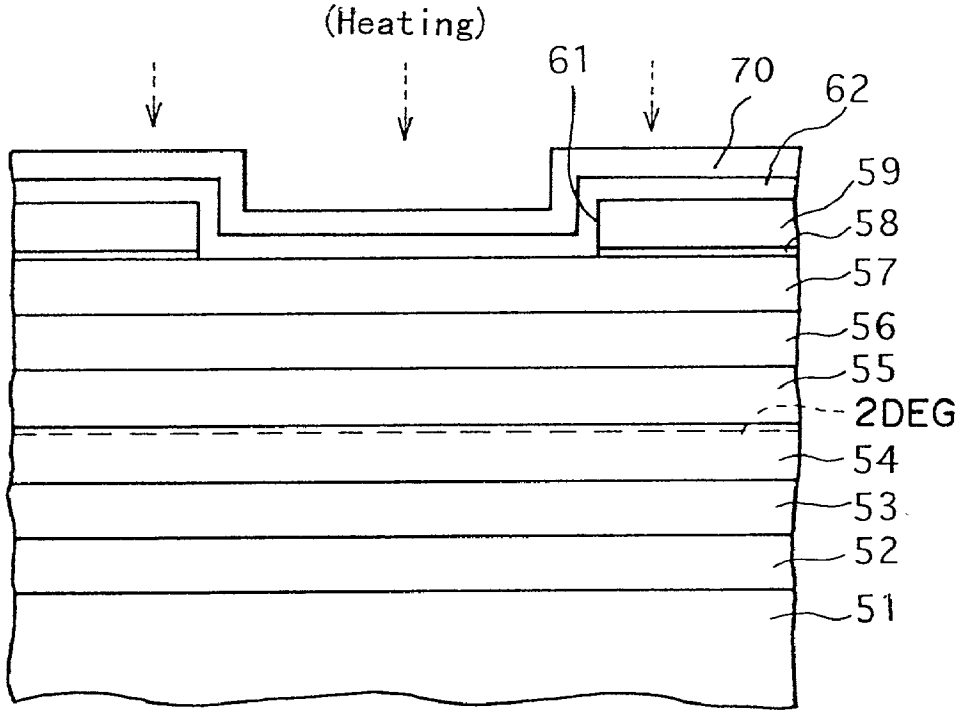


FIG. 14F

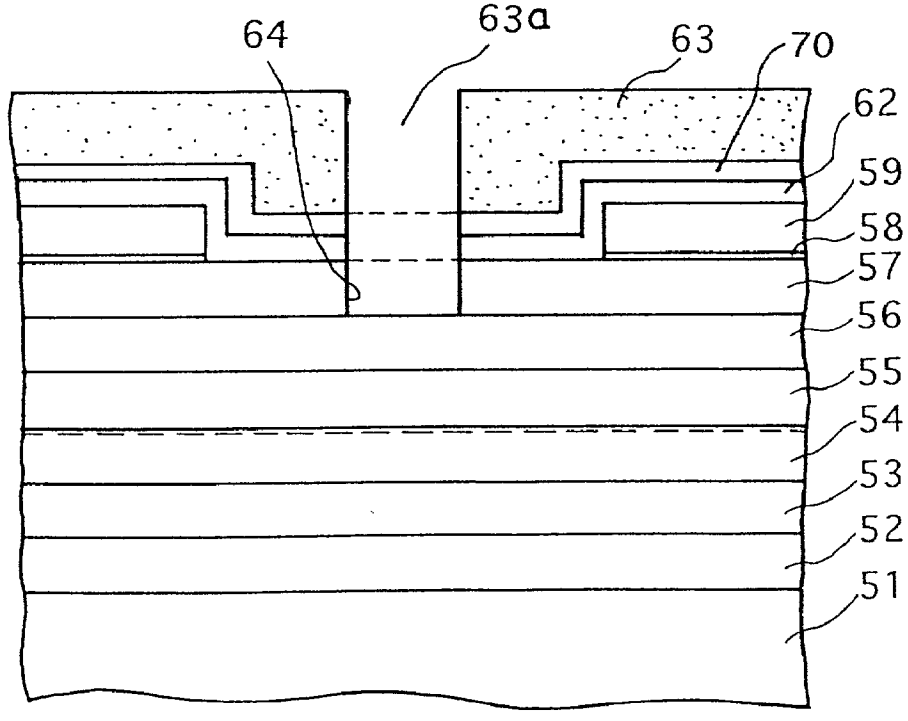


FIG. 14G

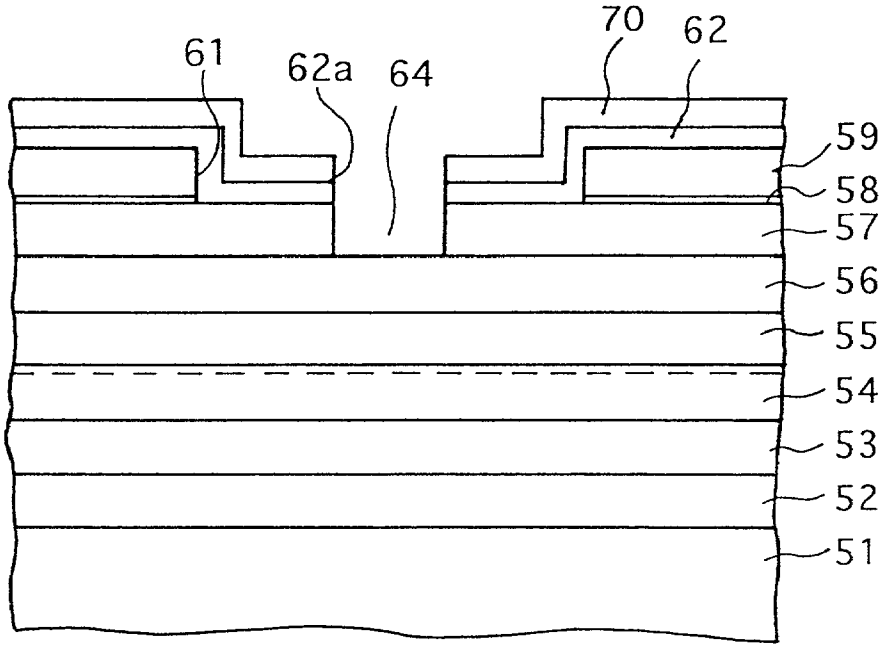


FIG. 14H

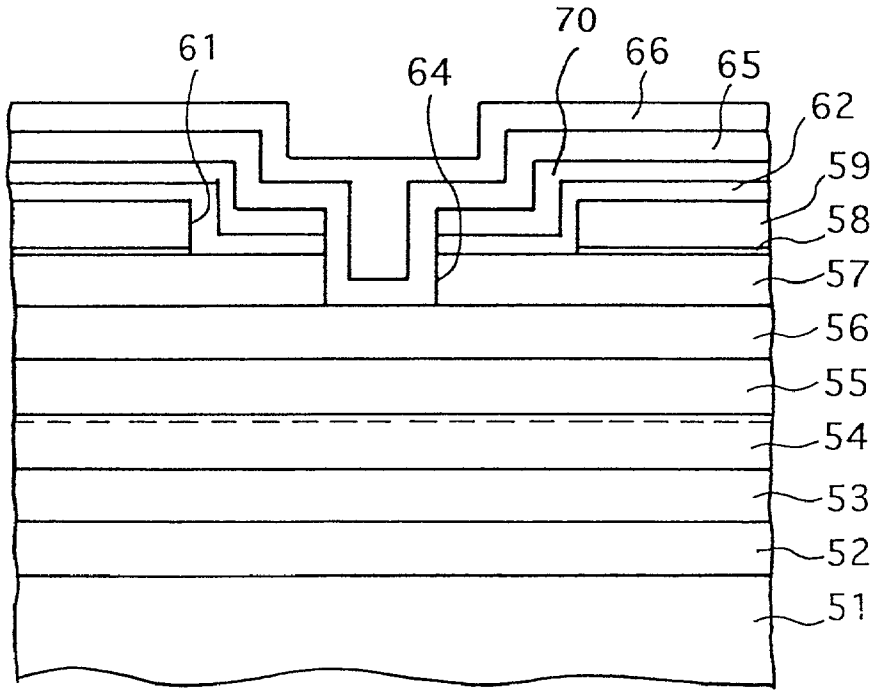


FIG. 14I

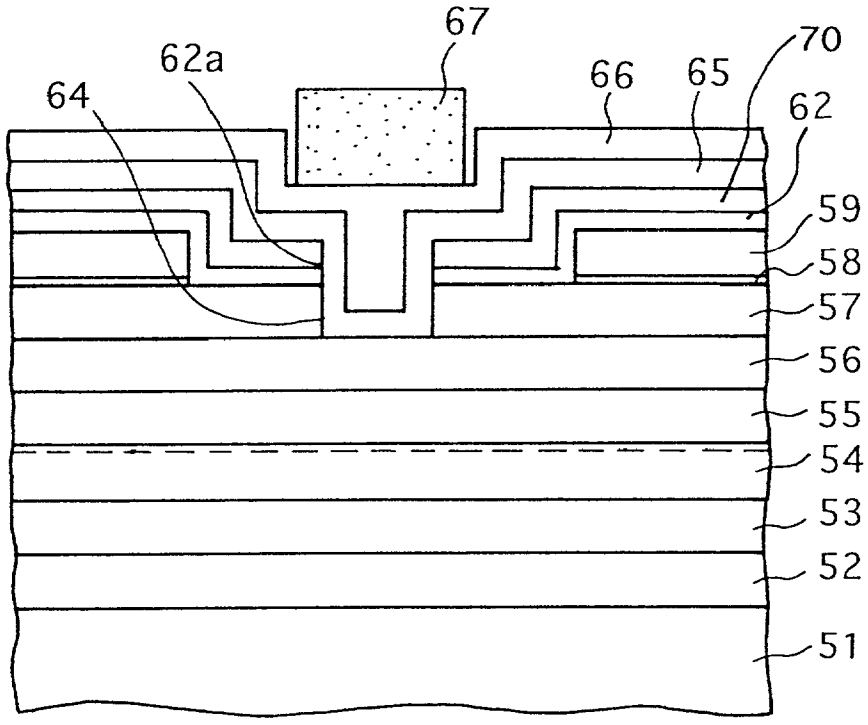


FIG. 14J

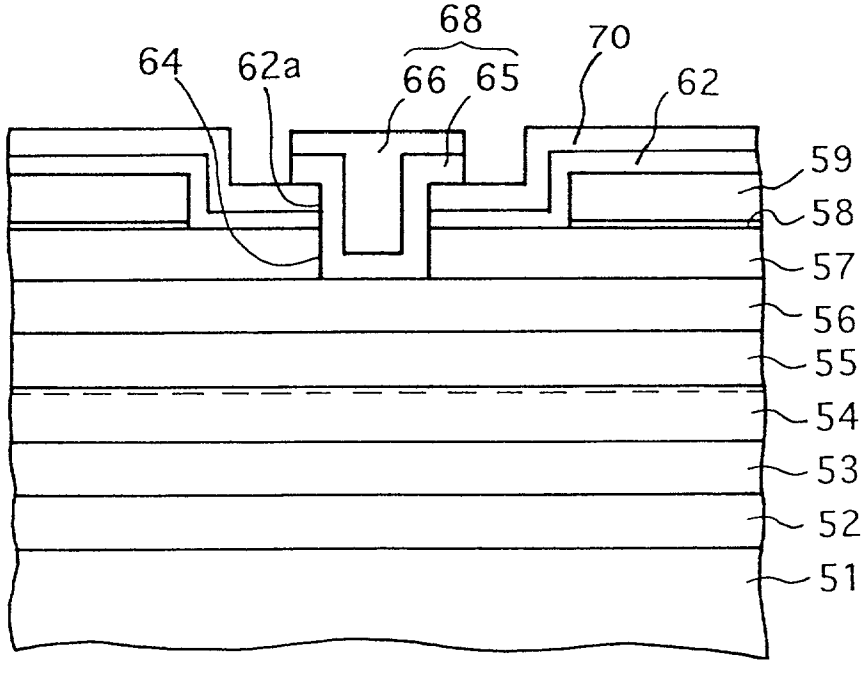


FIG. 14K

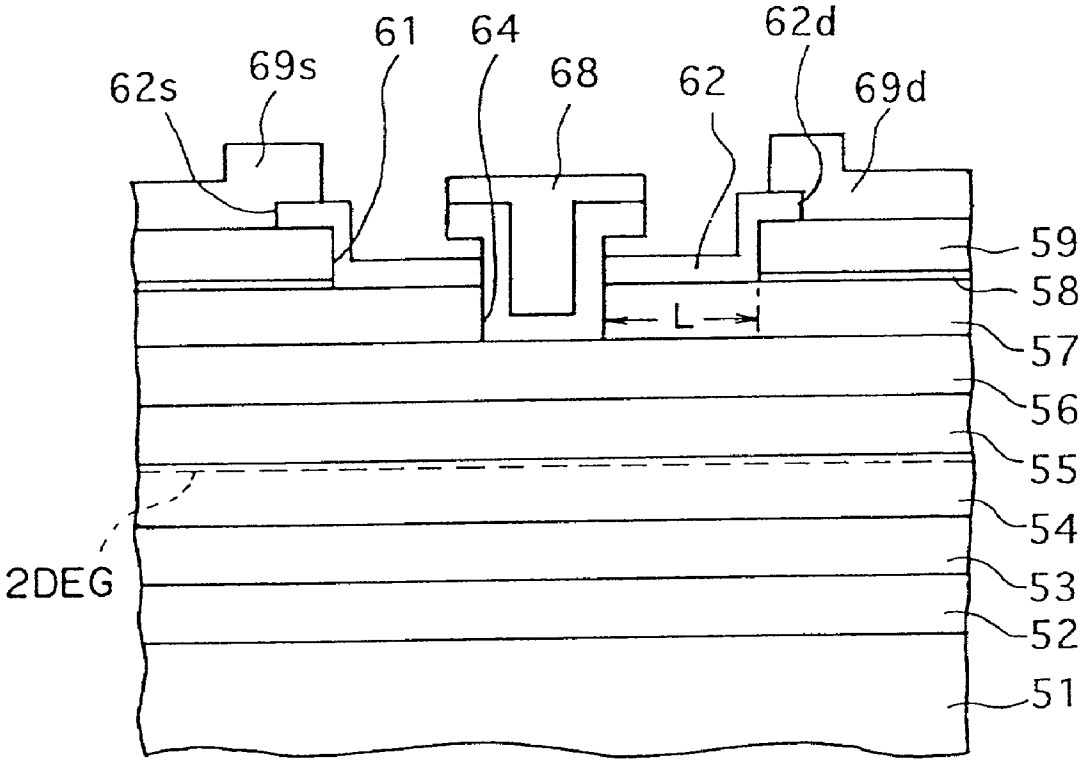


FIG. 15

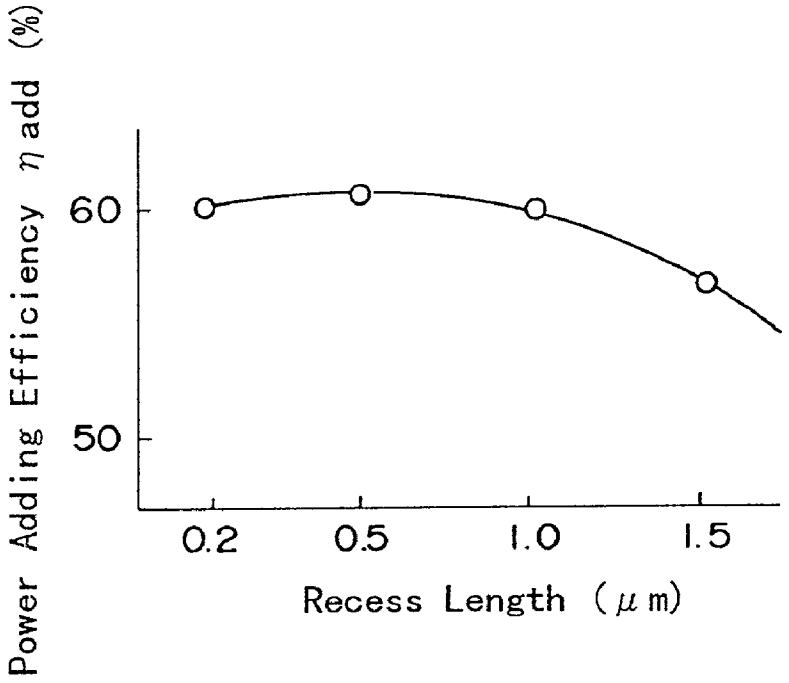

Power Adding Efficiency ηadd (%)
60
50
0.2
0.5
1.0
1.5
Recess Length (μm)

FIG. 16

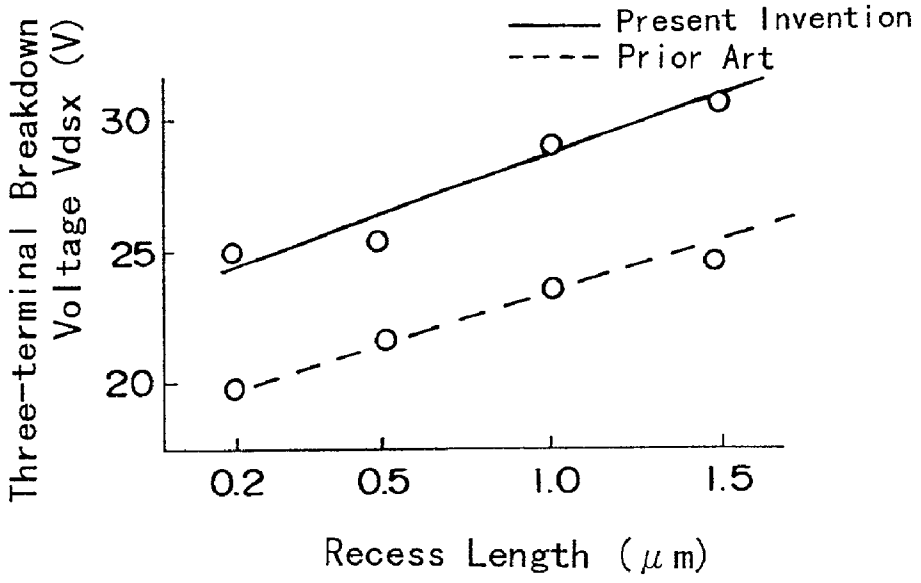

Present Invention
Prior Art
Three-terminal Breakdown Voltage Vdsx (V)
30
25
20
0.2
0.5
1.0
1.5
Recess Length (μm)

FIG. 17A

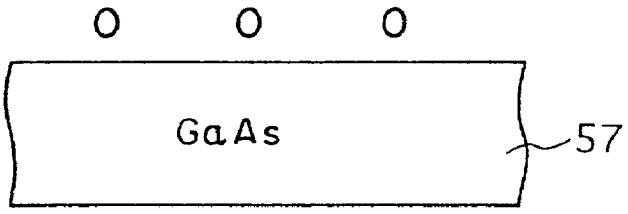


FIG. 17B

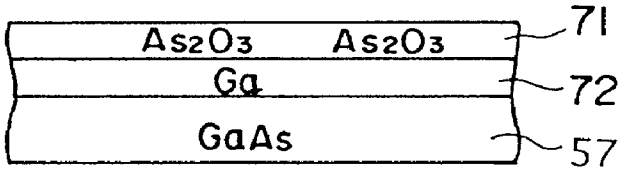


FIG. 17C

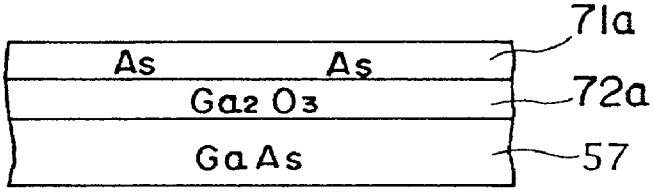


FIG. 17D

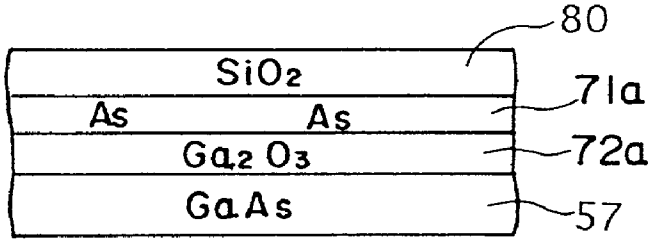


FIG. 17E

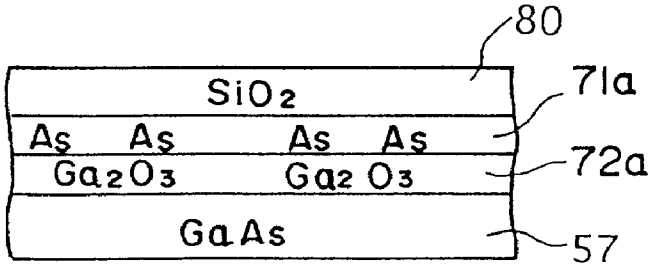


FIG. 18A

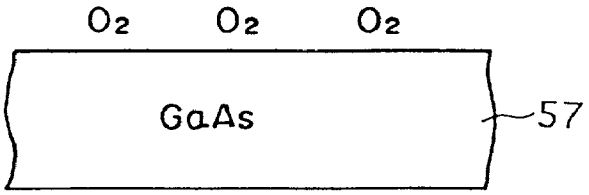


FIG. 18B

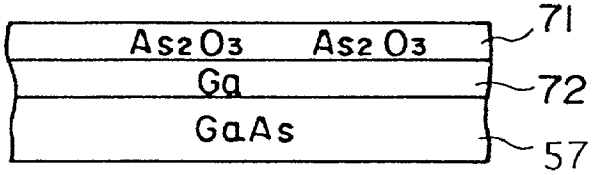


FIG. 18C

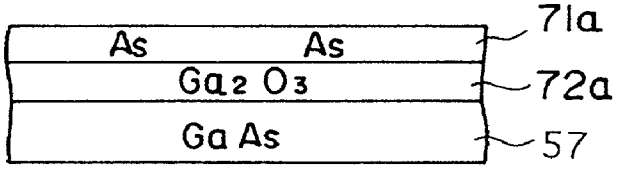


FIG. 18D

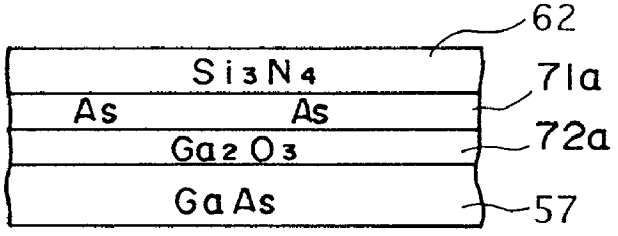


FIG. 18E

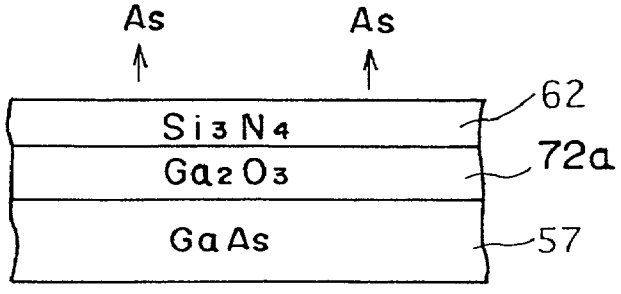


FIG. 19

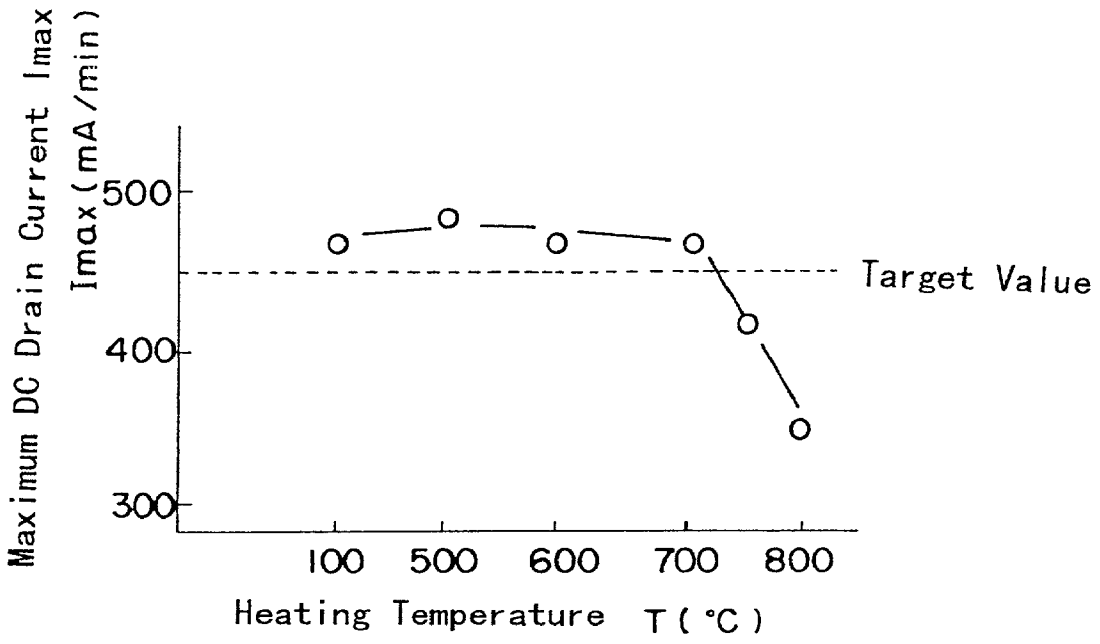

Maximum DC Drain Current Imax
Imax(mA/min)
500
400
300
Target Value
100
500
600
700
800
Heating Temperature T(°C)

FIG. 20

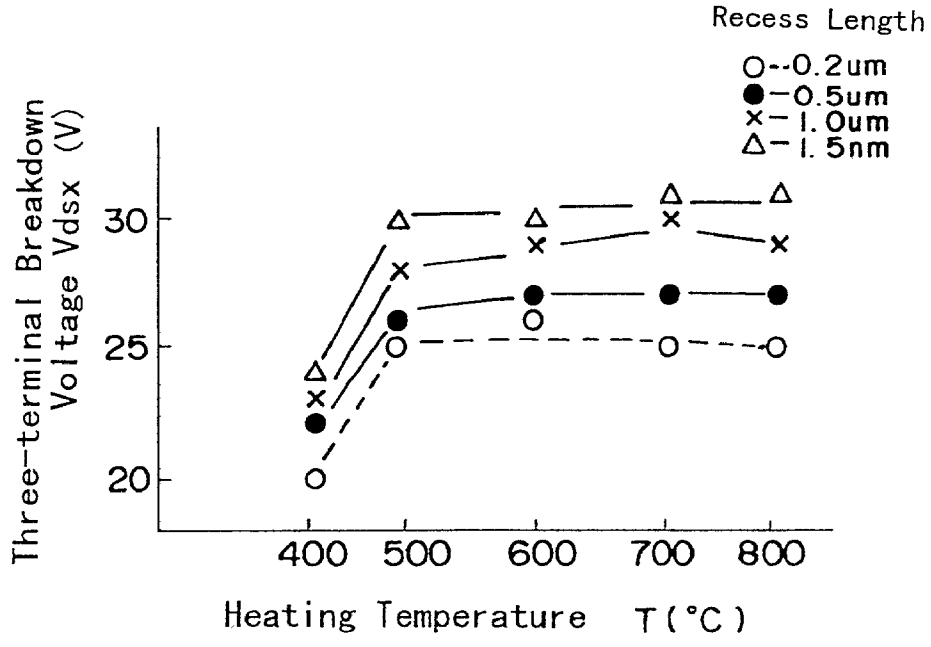

Recess Length
O--0.2um
●—0.5um
×—1.0um
△—1.5nm
Three-terminal Breakdown Voltage Vdsx (V)
30
25
20
400
500
600
700
800
Heating Temperature T(°C)

FIG. 21

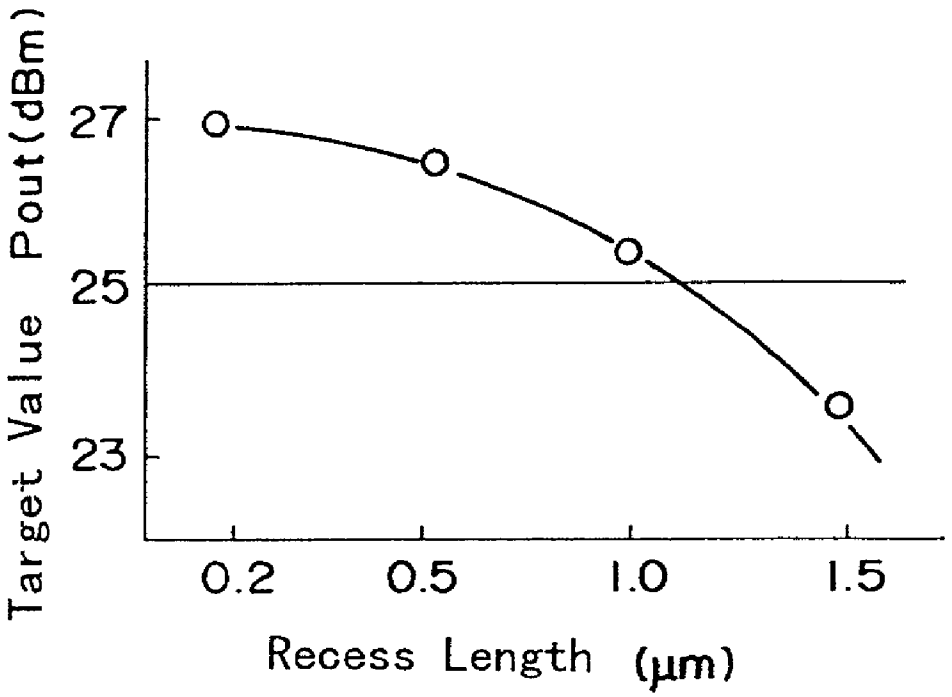
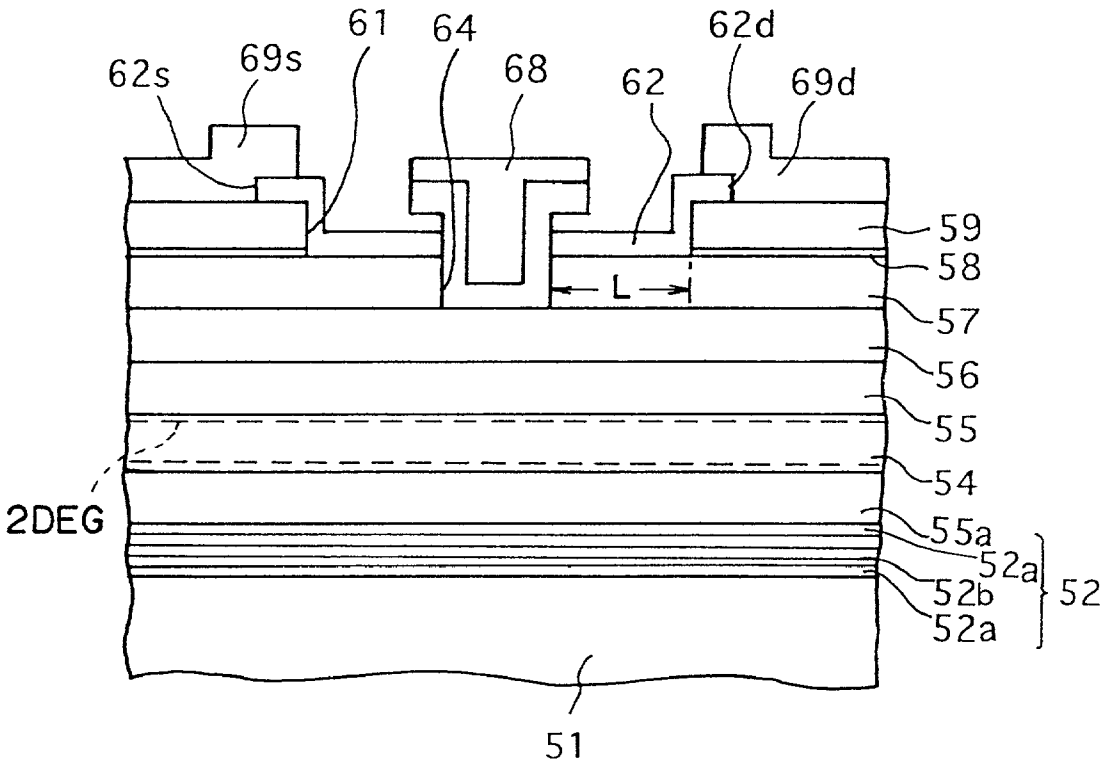


FIG. 22


61
64
62d
62s
69s
68
62
69d
59
58
L
57
56
55
54
2DEG
55a
52a
52b
52a
52
51

COMPOUND SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a compound semiconductor device and a method of manufacturing the same and, more particularly, a compound semiconductor device having a Schottky gate such as a high electron mobility transistor, a metal semiconductor field effect transistor, etc. and a method of manufacturing the same.

[0003] 2. Description of the Prior Art

[0004] As a compound semiconductor device having a Schottky gate, there have been known a high electron mobility transistor (HEMT), a metal semiconductor field effect transistor (MESFET), and the like.

[0005] In such compound semiconductor device, reduction in an influence of surface state upon a surface depletion layer and control of a threshold voltage of a transistor have been achieved by providing a recessed structure in a compound semiconductor layer which is located in a gate electrode connection portion and its peripheral area.

[0006] The field effect transistor employing the recessed structure has been set forth in, e.g., ① IEEE MTT-S Digest (1997) pp1187-1190, ② IEEE MTT-S Digest (1998) pp439-442, ③ Patent Application Publication (KOKAI) Hei 5-129341, ④ Patent Application Publication (KOKAI) Hei 5-251471, ⑤ Patent Application Publication (KOKAI) Hei 9-8283, and the like.

[0007] For example, the HEMT set forth in the reference ① has a structure shown in **FIG. 1**.

[0008] In **FIG. 1**, an undoped AlGaAs buffer layer **102**, an n^+-AlGaAs first electron supply layer **103**, an undoped AlGaAs first spacer layer **104**, an undoped InGaAs channel layer **105**, an undoped AlGaAs second spacer layer **106**, an n^+-AlGaAs second electron supply layer **107**, an undoped AlGaAs Schottky layer **108**, an n^--GaAs intermediate layer (buried layer) **109**, and an n^+-GaAs cap layer **110** are formed in sequence on a semi-insulating GaAs substrate **101**. An AlGaAs layer **111** is formed between the n^+-GaAs cap layer **110** and the n^--GaAs intermediate layer **109**.

[0009] A first recess **112** is formed in the cap layer **110** to expose the intermediate layer **109** in the periphery of a gate region. In addition, a second recess **114** is formed in the intermediate layer **109** to bury a lower portion of a gate electrode **113** made of tungsten silicide (WSi). The first recess **112** and the second recess **114** are formed to adjust a depth of a surface depletion layer.

[0010] A gold (Au) layer **115** is connected to the gate electrode **113** to reduce its resistance value.

[0011] The cap layer **110** is separated into a source side and a drain side on both sides of the gate electrode **113** by the first recess **112**. A source electrode **116***s* and a drain electrode **116***d*, both being ohmic-connected to the cap layer **110**, are formed on the cap layer **110** which has remained on the source side and the drain side respectively. In this case, a distance L from an edge of the first recess **112** to an edge of the second recess **114** between the drain electrode **116***d* and the gate electrode **113** is referred to as a recess length hereinafter.

[0012] In such HEMT, carriers supplied from the drain electrode **116***d* come up to the channel layer **105** via the cap layer **110**, . . . , the second spacer layer **106**, etc. Then, the carriers travels in the channel layer **105** from the lower side of the drain electrode **116***d* to the lower side of source electrode **116***s* by the electric field. Then, the carriers come up to the source electrode **116***s* via the second spacer layer **106**, . . . , the cap layer **110**. Travel of the carriers in the channel layer **105** can be controlled by a depletion layer which spreads out from the gate electrode **113** when the voltage is applied.

[0013] By the way, in the HEMT having the above structure, a sufficient gate breakdown voltage has not been able to be achieved since, if the backward vias voltage is applied to the gate electrode **113**, a phenomenon that a leakage current is increased gradually with the lapse of application time, i.e., a walk-out phenomenon, is caused.

[0014] Moreover, control of the gate forward vias has not been able to be sufficiently performed.

[0015] Besides, the fact that, if the recess length is less than 1 μm, a high power adding efficiency cannot be maintained has been confirmed according to the experiment done by the inventors of the present invention.

SUMMARY OF THE INVENTION

[0016] It is an object of the present invention to provide a compound semiconductor device which is capable of improving a breakdown voltage while suppressing generation of a walk-out phenomenon and also maintaining a high power adding efficiency even if a recess length in a region between a gate electrode and a cap layer is set to 1 μm or less, and a method of manufacturing the same.

[0017] (1) The above problems can be overcome by providing a compound semiconductor device which comprises a channel layer formed on a compound semiconductor substrate, and formed of material which has a first donor concentration and a first bandgap; a carrier supply layer formed on the channel layer, and formed of material which has a second donor concentration being higher than the first donor concentration and a second bandgap being wider than the first bandgap; a first compound semiconductor layer formed on the carrier supply layer, and containing donors in at least one of a lower layer portion and an upper layer portion within a range of impurity concentration of 1×10^{16} to 1×10^{17} atoms/cm^3; a gate electrode connected to the first compound semiconductor layer; a cap layer formed on the first compound semiconductor layer in a source region and a drain region which are formed on both sides of the gate electrode, and formed of material which has a third donor concentration being higher than the first donor concentration and a third bandgap being narrower than the second bandgap; a source electrode at least a part of which is formed on the cap layer in the source region; and a drain electrode at least a part of which is formed on the cap layer in the drain region.

[0018] According to the compound semiconductor device of the present invention, the first compound semiconductor

layer whose donor concentration is set to 1×10^{16} atoms/cm^3 to 1×10^{17} atoms/cm^3 is provided between the cap layer and the carrier supply layer.

[0019] According to the donor of such concentration, the holes being separated in the channel layer can be prevented from reaching the surface of the first compound semiconductor layer, whereby contraction of the surface depletion layer can be suppressed and thus generation of the walk-out phenomenon can be prevented.

[0020] In this case, since the donor concentration is set to less than 1×10^{17} atoms/cm^3, the situation that the gate breakdown voltage is easily reduced because of high concentration of donor in the first compound semiconductor layer cannot be brought about.

[0021] (2) The above problems can be overcome by providing a compound semiconductor device which comprises a channel layer formed on a compound semiconductor substrate, and formed of material which has a first donor concentration and a first bandgap; a carrier supply layer formed on the channel layer, and formed of material which has a second donor concentration being higher than the first donor concentration and a second bandgap being wider than the first bandgap; a Schottky layer formed on the carrier supply layer, and formed of material which has a third bandgap being wider than the second bandgap; a gate electrode connected to the Schottky layer; a buried layer having a recess in which a part of the gate electrode is buried; a cap layer formed on the Schottky layer in a source region and a drain region which are formed on both sides of the gate electrode, and formed of material which has a third donor concentration being higher than the first donor concentration and a fourth bandgap being narrower than the second bandgap; a source electrode at least a part of which is formed on the cap layer in the source region; and a drain electrode at least a part of which is formed on the cap layer in the drain region.

[0022] According to the compound semiconductor device of the present invention, the bandgap of the Schottky layer formed on the carrier supply layer is set higher than that of the carrier supply layer.

[0023] Therefore, the energy barrier between the gate electrode and the Schottky layer can be enhanced to thus improve the gate breakdown voltage.

[0024] However, if the bandgap of the Schottky layer is enhanced, the ohmic resistance of the source/drain regions is increased. Therefore, while suppressing a total film thickness from the Schottky layer to the cap layer, metal constituting the source/drain electrodes and the semiconductor layers therebelow are alloyed by heating, so that such alloy layer can be easily made to reach the electron supply layer. As a result, the ohmic resistance value can be reduced. However, when such film thickness is adjusted, it is not preferable that the thickness is made too thin to such extent that the surface depletion layer comes up to the carrier supply layer since supply of the carrier to two dimensional carrier gas area is decreased.

[0025] (3) The above problems can be overcome by providing a method of manufacturing a compound semiconductor device which comprises the steps of forming a channel layer on a semiconductor substrate; forming a carrier supply layer, which supplies carriers to the channel layer, on the channel layer; forming a Schottky semiconductor layer, which has a gate connection region, on the carrier supply layer; forming a gallium-arsenic buried layer on the Schottky semiconductor layer; forming a gallium-arsenic cap layer on the gallium-arsenic buried layer; forming a first recess in a region containing a gate region by etching a part of the gallium-arsenic cap layer; forming a silicon nitride film in the first recess and on the gallium-arsenic buried layer; heating the gallium-arsenic buried layer which is covered with the silicon nitride film; forming an opening portion by selectively etching the silicon nitride film on the gate connection region; forming a second recess by etching the gallium-arsenic buried layer via the opening portion; forming a gate electrode on the gate connection region of the Schottky semiconductor layer via the second recess; forming a source opening portion and a drain opening portion in the gallium-arsenic cap layer on both sides of the first recess by patterning the silicon nitride film; and forming a source electrode in the gallium-arsenic cap layer via the source opening portion and forming a drain electrode in the gallium-arsenic cap layer via the drain opening portion.

[0026] Also, the above problems can be overcome by providing a compound semiconductor device which comprises a channel layer formed on a semiconductor substrate; a carrier supply layer formed on the channel layer; a Schottky semiconductor layer formed on the carrier supply layer and having a gate connection region; a gallium-arsenic buried layer formed on the Schottky semiconductor layer; a gallium-arsenic cap layer formed on the gallium-arsenic buried layer; a first recess formed in the gallium-arsenic cap layer to expose a part of the gallium-arsenic buried layer, and having a width which is wider than the gate connection region; a second recess formed in the gallium-arsenic buried layer to expose the gate connection region of the Schottky semiconductor layer; a silicon nitride film provided in the first recess to extend from an end surface of the second recess onto the gallium-arsenic buried layer and the gallium-arsenic cap layer; a gate electrode connected to the Schottky semiconductor layer in the second recess; and a source electrode and a drain electrode formed on the gallium-arsenic cap layer respectively.

[0027] Next, an operation of the present invention will be explained.

[0028] According to the invention, the GaAs buried layer is heated after the silicon nitride film has been formed on the GaAs buried layer, in which the second recess is formed, in the region located on the inside of the first recess formed in the cap layer. Therefore, even if the gallium oxide layer and the arsenic layer are generated because the surface of the GaAs buried layer is oxidized, such arsenic layer can be discharged into the outside through the silicon nitride film by heating.

[0029] The leakage current is made easily flow since conductivity of the arsenic layer is high, so that the three-terminal breakdown voltage (Vdsx) is caused to reduce. Since the arsenic layer disappears substantially by heating, the three-terminal breakdown voltage (Vdsx) between the drain electrode, the gate electrode, and the source electrode can be increased. The power adding efficiency can also be improved since the three-terminal breakdown voltage (Vdsx) can be increased.

[0030] As a result, it has been evident experimentally that, if the interval between the first recess and the second recess is set to less than 1 μm, reduction in the power adding efficiency can be prevented.

[0031] It is preferable that the heating temperature is set in the range of 500 to 700° C.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] **FIG. 1** is a sectional view showing an example of a compound semiconductor device in the prior art;

[0033] **FIGS. 2A** to **2**H are sectional views showing steps of manufacturing a HEMT according to a first embodiment of the present invention;

[0034] **FIGS. 3A** to **3**G are sectional views showing steps of manufacturing a HEMT according to a second embodiment of the present invention;

[0035] **FIG. 4** is a view showing a relationship between a recess distance L and a gate backward breakdown voltage in the HEMT according to the second embodiment of the present invention;

[0036] **FIG. 5** is a view showing a relationship between the recess distance L and a walk-out change rate of the gate backward breakdown voltage in the HEMT according to the second embodiment of the present invention;

[0037] **FIG. 6** is a view showing a relationship between a film thickness of a buried layer and a maximum channel current in the HEMT according to the second embodiment of the present invention;

[0038] **FIG. 7** is a view showing a relationship between the film thickness of the buried layer and a gate forward breakdown voltage in the HEMT according to the second embodiment of the present invention;

[0039] **FIG. 8** is a sectional view showing a configuration of a HEMT according to a third embodiment of the present invention;

[0040] **FIG. 9** is a sectional view showing a configuration of a HEMT according to a fourth embodiment of the present invention;

[0041] **FIG. 10** is a sectional view showing a configuration of a HEMT according to a fifth embodiment of the present invention;

[0042] **FIG. 11** is a sectional view showing a configuration of a HEMT according to a sixth embodiment of the present invention;

[0043] **FIG. 12** is a sectional view showing a configuration of a HEMT according to a seventh embodiment of the present invention;

[0044] **FIG. 13** is a characteristic view showing a relationship between a recess length and a power adding efficiency of the compound semiconductor device in the prior art;

[0045] **FIGS. 14A** to **14**K are sectional views showing steps of manufacturing a HEMT according to an eighth embodiment of the present invention;

[0046] **FIG. 15** is a characteristic view showing a relationship between a recess length and a power adding efficiency in the HEMT according to the eighth embodiment of the present invention;

[0047] **FIG. 16** is a characteristic view showing a relationship between the recess length and a three-terminal breakdown voltage in the HEMT according to the eighth embodiment of the present invention and a relationship between the recess length and the three-terminal breakdown voltage in the HEMT in the prior art;

[0048] **FIGS. 17A** to **17**E are sectional views showing change in a GaAs layer employed in steps of manufacturing the HEMT in the prior art;

[0049] **FIGS. 18A** to **18**E are sectional views showing change in a GaAs layer employed in steps of manufacturing the HEMT according to the eighth embodiment of the present invention;

[0050] **FIG. 19** is a characteristic view showing a relationship between a heating temperature and a maximum DC drain current after a GaAs buried layer has been covered with a silicon nitride film, in steps of manufacturing the HEMT according to the eighth embodiment of the present invention;

[0051] **FIG. 20** is a characteristic view showing a relationship between a heating temperature and a three-terminal breakdown voltage of the GaAs buried layer which has been covered with the silicon nitride film, in steps of manufacturing the HEMT according to the eighth embodiment of the present invention;

[0052] **FIG. 21** is a characteristic view showing a relationship between a recess length and an output of the HEMT according to the eighth embodiment of the present invention; and

[0053] **FIG. 22** is a sectional view showing another configuration of the HEMT according to the eighth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0054] Embodiments of the present invention will be explained in detail with reference to the accompanying drawings hereinafter.

First Embodiment

[0055] **FIGS. 2A** to **2**H are sectional views showing steps of manufacturing a HEMT according to a first embodiment of the present invention.

[0056] First of all, as shown in **FIG. 2**A, formation of a plurality of compound semiconductor layers, which constitute the HEMT, on a semi-insulating gallium-arsenic (GaAs) substrate **1** will be explained hereinbelow.

[0057] In **FIG. 2A, a** first buffer layer **2***a* made of undoped GaAs, a second buffer layer **2***b* made of undoped aluminum-gallium-arsenic (AlGaAs), a first electron supply layer **3** made of n^+-AlGaAs, a first spacer layer **4** made of undoped AlGaAs, a channel layer (channel layer) **5** made of undoped indium-gallium-arsenic (InGaAs), a second spacer layer **6** made of undoped AlGaAs, a second electron supply layer (carrier supply layer) **7** made of n^+-AlGaAs, a Schottky

layer **8** made of undoped AlGaAs, an n^--GaAs buried layer **9**, an n^+-AlGaAs etching stopper layer **10**, and an n^+-GaAs cap layer **11** are formed in sequence on a GaAs substrate **1**.

[**0058**] As the growth method for the compound semiconductor layers **2** to **11**, there are the MOVPE method, the MBE method, and the like. The above term "undoped" does not mean that the impurity is not contained in the semiconductor layer at all, but means that the impurity is not doped in growing the semiconductor layer. These semiconductor layers are formed under the conditions that they can substantially satisfy the lattice matching for respective underlying layers. In this case, it is preferable that a composition ratio of aluminum (Al) in group III elements which are contained in AlGaAs constituting the Schottky layer **8** should be set to more than 0.4 (e.g., 0.5). Thus, the Schottky layer **8** is composed of $Al_xGa_{1-x}As$ (x>0.4). Similarly, it is preferable that a composition ratio of aluminum (Al) in the group III elements which are contained in AlGaAs constituting the etching stopper layer **10** should be set to more than 0.1 (e.g., 0.25). Thus, the etching stopper layer **10** is composed of $Al_yGa_{1-y}As$ (y>0.4).

[**0059**] In addition, a composition ratio of aluminum (Al) in the group III elements which are contained in AlGaAs constituting the first electron supply layer **3**, the first spacer layer **4**, the second spacer layer **6**, and the second electron supply layer **7** is set to 0.1 to 0.3 (e.g., 0.25). Also, a composition ratio of indium (In) in the group III elements which are contained in InGaAs constituting the channel layer **5** is set to 0.1 to 0.3 (e.g., 0.25).

[**0060**] An energy bandgap in AlGaAs becomes wider as the composition ratio of aluminum is increased. According to the larger energy bandgap, the AlGaAs layers are aligned in order of the Schottky layer **8**, the etching stopper layer **10**, and other AlGaAs layers (the first electron supply layer **3**, the first spacer layer **4**, the second spacer layer **6**, and the second electron supply layer **7**).

[**0061**] Next, examples of the film thickness range of the compound semiconductor layers will be explained hereinbelow.

[**0062**] A thickness of the GaAs first buffer layer **2***a* is about 150 nm, a thickness of the AlGaAs second buffer layer **2***b* is about 500 nm, a thickness of the AlGaAs first electron supply layer **3** is 3 to 15 nm (e.g., 7 nm), a thickness of the AlGaAs first spacer layer **4** is less than 5 nm (e.g., 2 nm), a thickness of the InGaAs channel layer **5** is 10 to 25 nm (e.g., 14 nm), a thickness of the AlGaAs second spacer layer **6** is less than 5 nm (e.g., 2 nm), a thickness of the AlGaAs second electron supply layer **7** is 10 to 30 nm (e.g., 20 nm), a thickness of the AlGaAs Schottky layer **8** is 1 to 30 nm (e.g., 20 nm), a thickness of the GaAs buried layer **9** is 10 to 70 nm (e.g., 30 nm), a thickness of the AlGaAs etching stopper layer **10** is 1 to 10 nm (e.g., 3 nm), and a thickness of the GaAs cap layer **11** is more than 50 nm (e.g., 80 nm).

[**0063**] As for the impurity concentration of the impurity doped layers, the silicon concentration of the AlGaAs first electron supply layer **3** is 1×10^{18} to 3×10^{18} atoms/cm^3 (e.g., 2×10^{18} atoms/cm^3), the silicon concentration of the AlGas second electron supply layer **7** is 1×10^{18} to 3×10^{18} atoms/cm^3 (e.g., 2×10^{18} atoms/cm^3), the silicon concentration of the GaAs buried layer **9** is less than 5×10^{17} atoms/cm^3 (e.g., 5×10^{16} atoms/cm^3), the silicon concentration of the AlGaAs etching stopper layer **10** is more than 0 (e.g., 2×10^{18} atoms/cm^3), and the silicon concentration of the GaAs cap layer **11** is more than 1×10^{18} atoms/cm^3 (e.g., 3×10^{18} atoms/cm^3). Although the Schottky layer **8** is formed of undoped layer in the above, the silicon may be contained in the Schottky layer **8** at the concentration of less than 5×10^{17} atoms/cm^3 by the impurity doping from overlying and underlying layers during the impurity diffusion or the film growth. For example, the silicon may be employed as the impurity.

[**0064**] After the growth of the above semiconductor layers has been completed, first resist **12** is coated on the cap layer **11** and then the first resist **12** is left like an island in regions, which define the gate region and the source/drain regions, by exposing and developing the first resist **12**.

[**0065**] The GaAs cap layer **11** is then etched by using the first resist **12** as a mask to be left like the island, as shown in **FIG. 2B**.

[**0066**] In this case, the GaAs cap layer **11** is etched by the plasma etching method using silicon tetrachloride ($SiCl_4$) and sulfur hexafluoride (SF_6) as the reaction gas. Since an etching rate of the AlGaAs etching stopper layer **10** becomes slow quickly if the etching is continued under such conditions, it is possible to make it easy to control stop of the etching of the GaAs cap layer **11**.

[**0067**] A first recess **13** is formed in the source/drain regions on the inside of the GaAs cap layer **11** by the etching. Concave regions are then ensured on the outside of the GaAs cap layer **11** to form the source/drain regions.

[**0068**] As shown in **FIG. 2**C, the AlGaAs etching stopper layer **10** exposed from the first recess **13** is then removed by using ammonia, nitric acid, or hydrogen fluoride, for example, while using the first resist **12** as a mask.

[**0069**] The first resist **12** is then removed and, as shown in **FIG. 2**D, an insulating film **14** made of silicon oxide (SiO_2), silicon nitride (Si_3N_4), silicon oxide nitride (SiON), or the like is formed by the CVD method to cover the GaAs buried layer **9** and the cap layer **11**. Such formation of the insulating film **14** will be explained in detail in the eighth embodiment of the present invention.

[**0070**] Second resist is then coated on the insulating film **14** and, as shown in **FIG. 2E, a** window **15***a* is then formed by exposing and developing the second resist.

[**0071**] An opening portion **14***a* is then formed in the gate region by patterning the insulating film **14** exposed from the window **15***a* by virtue of the photolithography method. The GaAs buried layer **9** exposed from the opening portion **14***a* is then etched, whereby a second recess **16** is formed in the GaAs buried layer **9**, as shown in **FIG. 2F**. This etching in forming the second recess **16** is effected by the plasma etching method using a mixed gas of $SiCl_4$ and SF_6.

[**0072**] A distance L between an inner edge portion of the first recess **13** and an outer edge portion of the second recess **16** is a recess length.

[**0073**] As shown in **FIG. 2G, a** tungsten silicide (WSi) layer **17***a* and a gold (Au) layer **17***b* are then formed on the insulating film **14** and in the second recess **14** by sputtering to have a thickness of 150 nm and 500 nm respectively.

[0074] The Au layer **17***b* and the WSi layer **17***a* are then left in the first recess **16** and its peripheral area by patterning them. Thus, as shown in **FIG. 2G, a** T-shaped gate electrode **18** is formed of the Au layer **17***b* and the WSi layer **17***a*. A Schottky barrier exists on the boundary between the gate electrode **18** and the Schottky layer **8**.

[0075] The insulating film **14** is then patterned by the photolithography technique using the resist, and thus source/drain openings **14***s*, **14***d* are formed on the outside of two island-like cap layers **11**. A triple-layered metal layer **19** made of gold-germanium (AuGe)/nickel (Ni)/gold (Au) is then formed by evaporation.

[0076] The triple-layered metal layer **19** is then patterned by the lift-off method and thus left on the buried layer **9** on the outside of two island-like cap layers **11**. As a result, two triple-layered metal layers **19** which are formed on the outside of two island-like cap layers **11** can be employed as a drain electrode **19***d* and a source electrode **19***s*.

[0077] After this, the lowermost layer made of AuGe is diffused up to the second electron supply layer **7** by heating the triple-layered metal layers **19** at the temperature of 400 to 450° C.

[0078] With the above, a basic structure of the HEMT is completed.

[0079] In the above HEMT, since the composition ratio of aluminum in AlGaAs constituting the Schottky layer **8** is set to 0.4, the bandgap is increased in itself. Therefore, the Schottky barrier against the gate electrode **18** becomes higher than the device shown in **FIG. 1** in the prior art. As a result, a gate breakdown voltage is enhanced by 0.1 to 0.2 V to thereby suppress generation of a walk-out phenomenon.

[0080] If the bandgap of the Schottky layer **8** is increased, ohmic contact resistance between the source electrode **19***s*, the drain electrode **19***d* being formed thereon and the Schottky layer **8** becomes higher, and in turn an ON resistance of the transistor is increased to thus cause deterioration of the characteristic.

[0081] However, in the first embodiment, a distance (depth) from the source electrode **19***s*, the drain electrode **19***d* to an upper surface of the second electron supply layer **7** is made small by removing the cap layer **11** and the etching stopper layer **10**, so that the constituent metal (AuGe) of the source electrode **19***s*, the drain electrode **19***d* can be thermal-diffused easily into the second electron supply layer **7**. Therefore, the ohmic resistance is reduced and thus the ON resistance is also decreased.

[0082] It has been found that, when a relationship between the distance from the source electrode **19***s*, the drain electrode **19***d* to an upper surface of the second electron supply layer **7** and the ohmic resistance is examined, it is significant for reduction in the ohmic resistance and in turn reduction in the ON resistance to set a resultant thickness from an upper surface of the electron supply layer to the source/drain electrodes to less than 100 nm. For instance, the ON resistance has been less than 1 Ωmm when the thickness is 55 nm, nevertheless the ON-resistance has been 2 to 8 Ωmm when the thickness is 140 nm.

[0083] In the first embodiment, with regard to the above respects, a thickness T from the upper surface of the second electron supply layer **7** to the upper surface of the buried layer **9** is set to about 100 nm at its maximum.

[0084] There is the limit in thinning the thickness. More particularly, the thickness must be set such that a surface depletion layer, which extends from the buried layer **9** downward, does not reach the second electron supply layer **7** in the neighborhood of the gate electrode **18**. If the surface depletion layer reaches the second electron supply layer **7**, the 2-DEG (two-dimensional electron gas) concentration of the channel layer **5** is reduced to cause deterioration of the transistor parameters. It is preferable that, with regard to this respect, a lower limit of the thickness T from the upper surface of the second electron supply layer **7** to the upper surface of the buried layer **9** should be set to 15 nm in the first embodiment.

[0085] A reference D in **FIG. 2H** denotes an example of the distribution of the surface depletion layer and the depletion layer generated by the gate.

[0086] In the above explanation, the source/drain electrodes are connected to the buried layer. In contrast, the distance between the source/drain electrodes and the channel layer may be shortened by etching the layers located below the buried layer within the region of the second spacer layer.

Second Embodiment

[0087] **FIGS. 3A** to **3**G are sectional views showing steps of manufacturing a HEMT according to a second embodiment of the present invention.

[0088] First, as shown in **FIG. 3A**, formation of a plurality of compound semiconductor layers constituting the HEMT on the semi-insulating gallium-arsenic (GaAs) substrate **1** will be explained hereinbelow.

[0089] In **FIG. 3A, a** first buffer layer **22***a* made of undoped GaAs, a second buffer layer **22***b* made of undoped AlGaAs, a first electron supply layer **23** made of n^+AlGaAs, a first spacer layer **24** made of undoped AlGaAs, a channel layer **25** made of undoped indium-gallium-arsenic (InGaAs), a second spacer layer **26** made of undoped AlGaAs, a second electron supply layer (carrier supply layer) **27** made of n^+-AlGaAs, a Schottky layer **28** made of undoped n^--AlGaAs, a buried layer **29** made of n^-GaAs, an etching stopper layer **30** made of n^+-AlGaAs, and a cap layer **31** made of n^+-GaAs are grown in sequence on a GaAs substrate **21**.

[0090] These layers are grown by the MOVPE method, the MBE method, and the like. In this case, it is preferable that a composition ratio of aluminum (Al) in group III elements which are contained in AlGaAs constituting the Schottky layer **28** should be set to 0.1 to 0.3 (e.g., 0.25). Thus, the Schottky layer **28** is composed of $Al_xGa_{1-x}As$ (0.1>x>0.3). Similarly, it is preferable that a composition ratio of aluminum (Al) in the group III elements which are contained in the etching stopper layer **30** should be selected within the same range as the Schottky layer **28**.

[0091] In addition, a composition ratio of aluminum (Al) in the group III elements which are contained in AlGaAs constituting the first electron supply layer **23**, the first spacer layer **24**, the second spacer layer **26**, and the second electron supply layer **27** is set to 0.1 to 0.3 (e.g., 0.25). Also, a composition ratio of indium (In) in the group III elements

which are contained in InGaAs constituting the channel layer **5** is set to 0.1 to 0.3 (e.g., 0.25).

[**0092**] Next, preferable ranges of the film thickness of the compound semiconductor layers will be explained hereinbelow.

[**0093**] Thicknesses of the GaAs first buffer layer **22***a* to the AlGaAs second electron supply layer **27** are set to be equal to those of the GaAs first buffer layer **2***a* to the AlGaAs second electron supply layer **7**, which have the same functions as those of the above layers, in the first embodiment respectively. A thickness of the AlGaAs Schottky layer **28** is 5 to 30 nm (e.g., 20 nm), a thickness of the GaAs buried layer **29** is 15 to 50 nm (e.g., 30 nm), a thickness of the AlGaAs etching stopper layer **30** is 1 to 10 nm (e.g., 3 nm), and a thickness of the GaAs cap layer **31** is 30 to 150 nm (e.g., 80 nm).

[**0094**] As with the impurity concentration of the impurity doped layers, the silicon concentration of the AlGaAs first electron supply layer **23** to the AlGaAs second electron supply layer **27** are set identically to that of the AlGaAs first electron supply layer **3** to the AlGaAs second electron supply layer **7** in the first embodiment respectively. Also, the silicon concentration of the Schottky layer **28** is 1×10^{18} to 3×10^{18} atoms/cm^3 (e.g., 5×10^{18} atoms/cm^3), and the silicon concentration of the GaAs buried layer **29** is 1×10^{16} to 10×10^{16} atoms/cm^3 (e.g., 5×10^{16} atoms/cm^3). Also, the silicon concentration of the AlGaAs etching stopper layer **30** and the GaAs cap layer **31** is set to be equal to that in the first embodiment.

[**0095**] After the growth of the above semiconductor layers has been completed, resist **32** is coated on the cap layer **31**. Then, the resist **32** is patterned by exposing and developing the resist **32** to have a shape covering the source/drain regions.

[**0096**] The GaAs cap layer **31** is then etched by using the resist **32** as a mask to form a first recess **33**, as shown in **FIG. 3B**.

[**0097**] In this etching step, if the GaAs cap layer **31** is etched by the plasma etching method using the mixed gas of $SiCl_4$ and SF_6 as the reaction gas, an etching rate becomes slow rapidly at a point of time when the AlGaAs etching stopper layer **30** formed beneath the GaAs cap layer **31** is exposed. Thus, stop of the etching of the GaAs cap layer **31** can be easily controlled.

[**0098**] While using the resist **32** as a mask, the AlGaAs etching stopper layer **30** exposed from the first recess **33** is removed by using ammonia, nitric acid, or hydrogen fluoride, for example.

[**0099**] The resist **32** is then removed and, as shown in **FIG. 3**C, an insulating film **34** is grown on an exposed surface of the GaAs cap layer **31** and an exposed surface of the AlGaAs etching stopper layer **30** by the plasma CVD method.

[**0100**] Another resist **35** is then coated on the insulating film **34** and then, as shown in **FIG. 3D, a** window **35***a* is formed in the gate region by exposing and developing the another resist **35**. Then, an opening portion **34***a* is formed by etching the insulating film **34** being exposed from the window **35***a* by virtue of the reactive ion etching.

[**0101**] As shown in **FIG. 3**E, the GaAs buried layer **29** is etched via the opening portion **34***a* under the same conditions as the first recess **33**, whereby a second recess **36** is formed in the GaAs buried layer **29**.

[**0102**] The resist **35** is then removed.

[**0103**] As shown in **FIG. 3F, a** metal film is formed in the opening portion **34***a* of the insulating film **34** and the second recess **36** by sputtering. The metal film is formed to have a double-layered structure in which a tungsten silicide (WSi) layer and a gold (Au) layer **17***b* formed to have a thickness of 150 nm and 500 nm respectively.

[**0104**] Further, as shown in **FIG. 8B, a** T-sectional shaped gate electrode **37** which is connected to the Schottky layer **28** by virtue of the Schottky contact via the opening portion **34***a* and the second recess **36** is formed by patterning the metal layer by means of the photolithography. A length of the gate electrode **37** along the direction from the source region to the drain region, i.e., a gate length, is set to less than 0.6 μm.

[**0105**] The insulating film **34** is then patterned by the photolithography technique using the resist (not shown), and thus two opening portions **34***s*, **34***d* are formed on the GaAs cap layer **31** on both sides of the gate electrode **18**. A multi-layered conductive layer is then formed by growing three layers of gold-germanium (AuGe)/nickel (Ni)/gold (Au) in sequence by evaporation.

[**0106**] The multi-layered conductive layer is then patterned by the lift-off method. Thus, the multi-layered conductive layer being left in two opening portions **34***s*, **34***d* is employed as a drain electrode **38***d* and a source electrode **38***s*, as shown in **FIG. 3G**.

[**0107**] Thereby, a basic structure of the HEMT can be completed.

[**0108**] In the above HEMT, because the impurity concentration of the Schottky layer **28** and the buried layer **29** is set to more than 1×10^{16} atoms/cm^3, generation of the walk-out phenomenon can be suppressed. The reason why the walk-out phenomenon can be suppressed may be supposed as follows.

[**0109**] For the walk-out phenomenon, such a model has been proposed that holes are released from the bonded elements because electrons collide with the bonded elements in the channel layer **25** and then the surface depletion layer is reduced because the holes are trapped (caught) by the surface state. For example, such model is set forth in IEEE, Transaction on Electronic Device, Vol. 45., No. 1, 1998, p. 18.

[**0110**] Therefore, in the second embodiment, the Schottky layer **28** and the buried layer **29** can act as the barrier against the holes by enhancing the impurity concentration of the Schottky layer **28** and the buried layer **29**, so that they can prevent the holes which are separated from the channel layer **25** from reaching the surface depletion layer of the buried layer **29**. If the holes are trapped by the surface state, an amount of trapped holes is very small and thus a degree of reduction in the surface depletion layer can be made small rather than the HEMT structure in the prior art shown in **FIG. 1**.

[**0111**] The surface depletion layer whose reduction can be prevented in this manner can prevent the travel of the

carriers supplied from the drain electrode **38***d* toward the gate electrode **18**. Therefore, the walk-out phenomenon can be suppressed and also reduction in the gate breakdown voltage can be prevented.

[**0112**] On the contrary, if the impurity concentration of the Schottky layer **28** and the buried layer **29** is more than 1×10^{17} atoms/cm^3, the resistance values of these layers are reduced. As a result, the electrons are ready to transmit through the Schottky layer **28** and the buried layer **29**, and thus the gate breakdown voltage can be reduced. Accordingly, it is preferable that the impurity concentration is reduced smaller than 1×10^{17} atoms/cm^3.

[**0113**] If the recess distance L is reduced smaller than 0.15 μm, the number of electrons which can travel from the drain electrode **38***d* to the gate electrode **37** is increased to thus reduce the gate breakdown voltage. In contrast, if the recess distance L becomes longer than 0.6 μm, a surface area of the recess acting as the cause of the walk-out phenomenon is increased and therefore the holes are ready to be trapped by the surface state.

[**0114**] A relationship between the recess distance L and a gate backward breakdown voltage in the HEMT according to the second embodiment is shown in **FIG. 4**. A relationship between the recess distance L and a walk-out change rate of the gate backward breakdown voltage in the HEMT according to the second embodiment is shown in **FIG. 5**.

[**0115**] Therefore, it is preferable that the recess distance L should be set in the range of 0.15 to 0.6 μm.

[**0116**] In addition, based on the examination conducted by the inventors of the present invention, it has become evident that, if a thickness of the buried layer **29** is set thinner than 15 nm, the surface depletion layer reaches the second electron supply layer **27** to thus reduce the maximum value Ifmax of the channel current whereas, if the thickness of the buried layer **29** is set thicker than 50 nm, a contact area to the gate electrode **18** is increased to thus reduce the gate forward breakdown voltage.

[**0117**] A relationship between a film thickness of the buried layer **29** and the maximum channel current Ifmax in the HEMT according to the second embodiment is shown in **FIG. 6**. A relationship between the film thickness of the buried layer **29** and a gate forward breakdown voltage in the HEMT according to the second embodiment is shown in **FIG. 7**.

[**0118**] Accordingly, it is preferable that the thickness of the buried layer should be set thicker than 15 nm but thinner than 50 nm.

Third Embodiment

[**0119**] A third embodiment of the present invention has a structure in which the composition and the impurity concentration of the Schottky layer and respective layers formed on the Schottky layer in the HEMT shown in the second embodiment are changed.

[**0120**] **FIG. 8** is a sectional view showing a configuration of a HEMT according to the third embodiment of the present invention. In **FIG. 8**, the same references as those in **FIG. 3G** refer to the same elements in **FIG. 3G**.

[**0121**] In **FIG. 8**, the first buffer layer **22***a* made of undoped GaAs, the second buffer layer **22***b* made of undoped AlGaAs, the first electron supply layer **23** made of n^+-AlGaAs, the first spacer layer **24** made of undoped AlGaAs, the channel layer **25** made of undoped indium-gallium-arsenic (InGaAs), the second spacer layer **26** made of undoped AlGaAs, the second electron supply layer (carrier supply layer) **27** made of n^+-AlGaAs, a Schottky layer **28***a* made of undoped AlGaAs, an n^--GaAs buried layer **29***a*, an n^+-AlGaAs etching stopper layer **30***a*, and an n^+-GaAs cap layer **31***a* are grown in sequence on the GaAs substrate **21**.

[**0122**] These layers are grown by the MOVPE method, the MBE method, and the like.

[**0123**] In this case, it is preferable that a composition ratio of aluminum (Al) in group III elements which are contained in AlGaAs constituting the Schottky layer **28***a* should be set to more than 0.4 (e.g., 0.5). Thus, the Schottky layer **28***a* is composed of $Al_xGa_{1-x}As$ (x>0.4). Similarly, it is preferable that a composition ratio of aluminum (Al) in the group III elements which are contained in the etching stopper layer **30***a* should be set to more than 0.1 (e.g., 0.25). Thus, the etching stopper layer **30***a* is composed of $Al_yGa_{1-y}As$ (y>0.1). Other layers made of AlGaAs are set to the same composition ratio of aluminum in the second embodiment.

[**0124**] Accordingly, the bandgap of AlGaAs constituting the Schottky layer **28***a* becomes wider than that of AlGaAs constituting other layers.

[**0125**] Next, preferable ranges of the film thickness of the compound semiconductor layers will be explained hereinbelow.

[**0126**] Thicknesses of the GaAs first buffer layer **22***a* to the AlGaAs second electron supply layer **27** are set to be equal to those in the second embodiment respectively. A thickness of the AlGaAs Schottky layer **28***a* is 5 to 30 nm (e.g., 20 nm), a thickness of the GaAs buried layer **29***a* is 10 to 70 nm (e.g., 30 nm), a thickness of the AlGaAs etching stopper layer **30***a* is 1 to 10 nm (e.g., 3 nm), and a thickness of the GaAs cap layer **31***a* is less than 50 nm (e.g., 20 nm).

[**0127**] Concerning the impurity concentration of the silicon doped layers, the silicon concentration of the GaAs first buffer layer **22***a* to the AlGaAs second electron supply layer **27** are set identically to that in the second embodiment respectively. Although the Schottky layer **28***a* is formed of the undoped layer, the impurity may be contained at the impurity concentration of less than 5×10^{17} atoms/cm^3. In addition, the silicon concentration of the GaAs buried layer **29***a* is set to less than 5×10^{17} atoms/cm^3 (e.g., 5×10^{16} atoms/cm^3). Also, the silicon concentration of the AlGaAs etching stopper layer **30***a* and the GaAs cap layer **31***a* is set to be equal to that in the second embodiment.

[**0128**] After this, according to the steps explained in the second embodiment, a first recess **33** is formed, then the buried layer **29***a* is covered with an insulating film **34**, then a second recess **36** is formed, then a gate electrode **37** is formed, and then a source electrode **38***s* and a drain electrode **38***d* are formed.

[**0129**] Then, a lowermost layer of AuGe of the triple-layered AuGe/Ni/Au structure constituting the source electrode **38***s* and the drain electrode **38***d* is heated at the temperature of 400 to 450° C. so as to reach the second electron supply layer **27**.

[0130] According to such HEMT, since the composition ratio of Al in AlGaAs constituting the Schottky layer **28***a* is set higher than that in the device in the prior art, the bandgap of the Schottky layer **28***a* is increased, so that the Schottky barrier between the gate electrode **37** and the Schottky layer **28***a* can be increased higher than that of the device in the prior art. In the case of enhancement operation of the device, the gate forward operational voltage can be improved by 0.1 to 0.2 V.

[0131] However, as described in the first embodiment, if the bandgap of the Schottky layer **28***a* is increased, the ohmic resistance of the source electrode **38***s* and the drain electrode **38***d* is increased to thus increase the ON resistance.

[0132] In order to overcome such problem, it is effective to diffuse the lowermost layer of AuGe of the triple-layered metal layer constituting the source electrode **38***s* and the drain electrode **38***d* by heating until it can reach the electron supply layer.

[0133] In this case, it is preferable that a distance from lower surfaces of the source electrode **38***s* and the drain electrode **38***d* to an upper surface of the second electron supply layer **27** is set to less than 100 nm. In the third embodiment, the distance is set to 75 nm.

[0134] The distance must be held to such extent that the surface depletion layer caused by the buried layer **26** in the first recess **33** does not reach the second electron supply layer **27**. This is because, if the surface depletion layer reaches the second electron supply layer **27**, the 2-DEG concentration of the channel layer **25** is reduced so that the transistor parameters are degraded.

Fourth Embodiment

[0135] In the above first to third embodiments, the first electron supply layer **25**, the second electron supply layer **27**, the first spacer layer **24**, the second spacer layer **26**, and the Schottky layer **28** are formed of AlGaAs respectively.

[0136] However, as shown in **FIG. 9**, if a second spacer layer **41** and a second electron supply layer **42** are formed of InGaP, it is ready to increase the impurity concentration. Accordingly, under the condition that an amount of electron supplied from the second electron supply layer **42** to the channel layer **25** is fixed constant, if InGaP is employed, it is possible to reduce thicknesses of the second spacer layer **41** and the second electron supply layer **42** up to ½ to ⅓ rather than the case where AlGaAs is employed. As a result, transconductance (gm) can be enhanced if the second spacer layer **41** and the second electron supply layer **42** are formed of InGaP.

[0137] In this case, in **FIG. 9**, configurations of the HEMT according to the fourth embodiment other than the second spacer layer **41** and the second electron supply layer **42** is identical to those of the second embodiment. In **FIG. 9**, the same references as those in **FIG. 3G** denote the same elements.

[0138] In **FIG. 9**, the first buffer layer **22***a* made of undoped GaAs, the second buffer layer **22***b* made of undoped AlGaAs, a first electron supply layer **23** made of n^+-AlGaAs, the first spacer layer **24** made of undoped AlGaAs, the channel layer (channel layer) **25** made of undoped indium-gallium-arsenic (InGaAs), a second spacer layer **41** made of undoped InGaP, a second electron supply layer (carrier supply layer) **42** made of n^+-InGaP, the Schottky layer **28** made of n^--AlGaAs, the buried layer **29** made of n^--GaAs, the etching stopper layer **30** made of n^+-AlGaAs, and the cap layer **31** made of n^+-GaAs are formed in sequence on the GaAs substrate **21**.

[0139] A composition ratio of indium (In) in group III elements which are contained in InGaP constituting the second spacer layer **41** and the second electron supply layer **42** is set to 0.48. A thickness of the second spacer layer **41** is set to less than 5 nm (e.g., 2 nm), and a thickness of the second electron supply layer **42** is set to 5 to 20 nm (e.g., 8 nm). In addition, the silicon impurity concentration of the second electron supply layer **42** is set in the range of 1×10^{18} to 3×10^{18} atoms/cm^3 (e.g., 2×10^{18} atoms/cm^3).

[0140] Other configurations of the HEMT are similar to those of the second embodiment.

Fifth Embodiment

[0141] In the above fourth embodiment, only the second spacer layer **41** and the second electron supply layer **42** are formed of InGaP. But, as shown in **FIG. 10, a** Schottky layer **43** may also be formed of InGaP.

[0142] In **FIG. 10**, the same references as those in **FIG. 9** refer to the same elements.

[0143] As shown in **FIG. 10**, if the Schottky layer **43** is formed of InGaP, the gate breakdown voltage can be enhanced rather than the case where the Schottky layer **43** is formed of AlGaAs.

[0144] A configuration of a HEMT according to a fifth embodiment shown in **FIG. 10** is similar to that of the fourth embodiment except for the Schottky layer **43**.

[0145] A composition ratio of indium (In) in group III elements which are contained in InGaP constituting the Schottky layer **43** is set to 0.48. In addition, the impurity concentration contained in InGaP is set in the range of 1×10^{18} to 3×10^{18} atoms/cm^3 (e.g., 2×10^{18} atoms/cm^3). A thickness of the Schottky layer **43** is set to 5 to 30 nm (e.g., 20 nm).

[0146] Other configurations of the HEMT are similar to those of the fourth embodiment.

Sixth Embodiment

[0147] In the above fourth embodiment, only the second spacer layer **41** and the second electron supply layer **42** are formed of InGaP.

[0148] However, as shown in **FIG. 11, a** first electron supply layer **44** and a first spacer layer **45** may also be formed of InGaP respectively. If such material is selected, thicknesses of the first electron supply layer **44** and the first spacer layer **45** can be thinned and the transconductance (gm) can be enhanced rather than the fourth embodiment. However, it is preferable that, if easiness of epitaxial growth is taken into account, material shown in the fourth embodiment should be selected as constituent material of the first electron supply layer and the first spacer layer.

[0149] A layer configuration of a HEMT according to a sixth embodiment shown in **FIG. 11** is similar to that of the fourth embodiment other than the first electron supply layer

44 and the first spacer layer **45**. The impurity concentration, composition, and film thickness of the first electron supply layer **44** and the first spacer layer **45**, which have different composition from that in the fourth embodiment, are given as follows.

[**0150**] A composition ratio of indium (In) in group III elements which are contained in InGaP constituting the first spacer layer **44** is set to 0.48. A thickness of the first spacer layer **44** is set to more than 0 nm but less than 5 nm (e.g., 2 nm).

[**0151**] A composition ratio of indium (In) in group III elements which are contained in InGaP constituting the first electron supply layer **45** is set to 0.48. In addition, the impurity concentration contained in InGaP is set in the range of 1×10^{18} to 3×10^{18} atoms/cm^3 (e.g., 2×10^{18} atoms/cm^3). A thickness of the first electron supply layer **45** is set to 1 to 10 nm (e.g., 4 nm).

[**0152**] Other configurations of the HEMT are similar to those of the fourth embodiment.

Seventh Embodiment

[**0153**] **FIG. 12** is a sectional view showing a configuration of a HEMT according to a seventh embodiment of the present invention. In **FIG. 12**, the same references as those in **FIG. 2A** denotes the same elements.

[**0154**] The HEMT of the seventh embodiment has a configuration in which material of the first electron supply layer, the first spacer layer, the second spacer layer, and the second electron supply layer of the HEMT in the first embodiment is changed into InGaP.

[**0155**] In **FIG. 12**, the first buffer layer **2***a* made of undoped GaAs, the second buffer layer **2***b* made of undoped AlGaAs, a first electron supply layer **44** made of n^+-InGaP, a first spacer layer **45** made of undoped InGaAs, the channel layer **5** made of undoped InGaAs, a second spacer layer **41** made of undoped InGaP, a second electron supply layer **42** made of n^+-InGaP, the Schottky layer **8** made of undoped AlGaAs, the buried layer **9** made of n^--GaAs, the etching stopper layer **10** made of n^+AlGaAs, and the cap layer **11** made of n^+-GaAs are formed in order on the GaAs substrate **1**.

[**0156**] In this case, material, impurity concentration, and film thickness of the first electron supply layer **44**, the first spacer layer **45**, the second spacer layer **41**, and the second electron supply layer **42** are selected similarly to those in the sixth embodiment. Material, impurity concentration, and film thickness of remaining layers are set to those in the first embodiment.

[**0157**] Layer configurations from the Schottky layer **8** to the cap layer **11** are same as those of the first embodiment. Since the Schottky layer **8** has the wider bandgap, the gate breakdown voltage can be made higher to thus reduce the ON-resistance rather than the HEMT shown in the sixth embodiment.

[**0158**] In the fourth to seventh embodiments, the electron supply layers, the spacer layers, etc. are formed of InGaP. In this case, AlInGaP or AlInAs may be employed in place of InGaP.

[**0159**] In the first to seventh embodiments, the first buffer layer is composed of a GaAs single layer. But, the present invention is not limited to this. For example, as shown in **FIG. 22, a** multi-layered structure in which an undoped GaAS layer and an undoped AlGaAs layer are stacked alternatively may be employed, as described later. In the above HEMT, the electron supply layer is formed on and under the electron traveling layer, but the first electron traveling layer and the first spacer layer may be omitted.

Eighth Embodiment

[**0160**] In an eighth embodiment, an insulating film for covering the GaAs buried layer of the HEMT will be explained hereinbelow.

[**0161**] In the recent HEMT, it is essential to shorten a gate length to operate the HEMT at the high frequency.

[**0162**] For example, according to the examination conducted by the inventors of the present invention, it has been confirmed that, if the gate length is set to less than 0.5 μm in the HEMT shown in **FIG. 1, a** characteristic shown in **FIG. 13** can be derived when a relationship between a recess length and a power adding efficiency is examined. In this case, the recess length L indicates a length L from an edge of the first recess **110** between the drain electrode **116***d* and the gate electrode **115** to an edge of the second recess **114** in **FIG. 1**.

[**0163**] According to **FIG. 13**, in the compound semiconductor device in which the recess length L is set to more than 1 μm, the power adding efficiency (η add) tends to decrease smaller as the recess length L becomes longer and longer. On the contrary, in the range where the recess length L is smaller than 1 μm, the power adding efficiency (η add) also tends to decrease smaller as the recess length L becomes shorter and shorter. In other words, in the HEMT in the prior art, the power adding efficiency (η add) is maximized in the structure in which the recess length L is set to 1 μm.

[**0164**] In principle, it can be understood theoretically that, since the distance between the drain electrode **116***d* and the gate electrode **115** become longer according to increase in the recess length L, the ON-resistance is increased and thus the power adding efficiency (η add) is decreased.

[**0165**] However, since the power adding efficiency (η add) cannot be kept high by merely reducing the ON-resistance in the situation that the recess length L is less than 1 μm, any treatment is needed.

[**0166**] Therefore, in following embodiment, the HEMT which enables the transistor, in which the recess length spread over ranges from the gate electrode to the cap layer is less than 1 μm, to keep the high power adding efficiency (η add) will be explained hereinbelow.

[**0167**] **FIGS. 14A** to **14**K are sectional views showing steps of manufacturing a HEMT according to an eighth embodiment of the present invention.

[**0168**] To begin with, as shown in **FIG. 14A, a** plurality of compound semiconductor layers constituting the HEMT are formed on a semi-insulating gallium-arsenic (GaAs) substrate **51**.

[**0169**] In **FIG. 14A, a** first buffer layer **52** made of undoped gallium-arsenic (GaAs), a second buffer layer **53** made of undoped aluminum-gallium-arsenic (AlGaAs), an electron travel layer (channel layer) **54** made of undoped

indium-gallium-arsenic (InGaAs), an electron supply layer (carrier supply layer) **55** made of n^+-AlGaAs, a Schottky layer **56** made of n-AlGaAs, an n-GaAs buried layer **57**, an n^+-AlGaAs etching stopper layer **58**, and an n^+-GaAs cap layer **59** are formed in sequence on a GaAs substrate **51**. As the growth method for these layers, there are the MOVPE method, the MBE method, etc. In **FIG. 14A,** 2-DEG denotes a two-dimensional electron gas.

[**0170**] Thicknesses of these layers are not limited particularly. By way of example, a thickness of the GaAs first buffer layer **52** is 150 nm, a thickness of the AlGaAs second buffer layer **53** is 500 nm, a thickness of the InGaAs electron travel layer **54** is 14 nm, a thickness of the AlGaAs electron supply layer **55** is 20 nm, a thickness of the AlGaAs Schottky layer **56** is 20 nm, a thickness of the GaAs buried layer **57** is 30 nm, a thickness of the AlGaAs etching stopper layer **58** is 5 nm, and a thickness of the GaAs cap layer **59** is 80 nm.

[**0171**] As for the impurity concentration of the impurity doped layers, for example, the silicon concentration of the AlGaAs electron supply layer **55** is more than 1×10^{18} atoms/cm^3, the silicon concentration of the AlGaAs Schottky layer **56** is about 4×10^{16} atoms/cm^3, the silicon concentration of the GaAs buried layer **57** is about 4×10^{16} atoms/cm^3, the silicon concentration of the AlGaAs etching stopper layer **58** is more than 2×10^{18} atoms/cm^3, and the silicon concentration of the GaAs cap layer **59** is more than 3×10^{18} atoms/cm^3. The GaAs buried layer **57** may be formed of the undoped layer.

[**0172**] After the formation of the above semiconductor layers has been finished, first resist **60** is coated on the cap layer **59** and then the first resist **60** is patterned by exposing and developing the first resist **60** so as to cover the source/drain regions.

[**0173**] The GaAs cap layer **59** is then etched by using the first resist **60** as a mask to thus form a first recess **61**, as shown in **FIG. 14B**.

[**0174**] The GaAs cap layer **59** is etched by the plasma etching method using a chlorine gas or a chlorine compound gas. Since an etching rate becomes slow quickly at a point of time when the AlGaAs etching stopper layer **58** formed below the GaAs cap layer **59** is exposed, stop of the etching of the GaAs cap layer **59** can be easily controlled. The first recess **61** is formed in the GaAs cap layer **59** by this etching.

[**0175**] As shown in **FIG. 14**C, while using the first resist **60** as a mask, the AlGaAs etching stopper layer **58** being exposed from the first recess **61** is then removed by using ammonia, nitric acid, or hydrogen fluoride, for example.

[**0176**] The first resist **60** is then removed and, as shown in **FIG. 14D, a** silicon nitride film **62** is grown on exposed surfaces of the GaAs cap layer **59** and the AlGaAs etching stopper layer **58** by the plasma CVD method to have a thickness of 30 nm to 100 nm. For example, growth conditions of the silicon nitride film **62** are that a mixed gas of silane (SiH_4) and nitrogen (N_2) is employed as a growth gas, a growth temperature is set to 250° C. to 350° C., preferably 300° C., a pressure in the growth atmosphere is set to 0.5 to 2.0 Torr, preferably about 1 Torr, a power density is set to 0.05 to 0.11 W/cm^2, and a growth rate is set to 5 to 15 nm/min.

[**0177**] After the silicon nitride film **62** has been formed, the silicon nitride film **62** and underlying compound semiconductor layers **2** to **9** are heated at the temperature of 500° C. to 700° C., as shown in **FIG. 14E**.

[**0178**] A silicon oxide film (SiO_2) **70** of 250 nm to 300 nm thickness is grown on the silicon nitride film **62** by the CVD method.

[**0179**] Second resist **63** is then coated on the silicon oxide film **70** and, as shown in **FIG. 14F, a** window **63***a* is then formed in the gate region by exposing and developing the second resist **63**. An opening portion **62***a* is then formed by etching the silicon oxide film **70** and the silicon nitride film **62** being exposed from the window **63***a* by virtue of the reactive ion etching. There is SF_6 as an etching gas employed in etching the silicon oxide film **70** and the silicon nitride film **62**, for example.

[**0180**] Like the formation of the first recess **61**, the GaAs buried layer **57** is etched via the opening portion **62***a* by the plasma etching method using the chlorine gas or the chlorine compound gas, whereby a second recess **64** is formed in the GaAs buried layer **57**.

[**0181**] As shown in **FIG. 14**G, the second resist **63** is removed.

[**0182**] As shown in **FIG. 14H, a** tungsten silicide (WSi) layer **65** and a gold (Au) layer **66** are then formed on the silicon nitride film **62** and in the opening portion **62***a* and the second recess **64** by sputtering to have a thickness of 150 nm and 500 nm respectively.

[**0183**] Third resist **67** is then coated on the Au layer **66** and then, as shown in **FIG. 14I, a** pattern for covering the gate region is formed by exposing and developing the third resist **67**.

[**0184**] While using the third resist **67** as a mask, the Au layer **66** and the WSi layer **65** are patterned by the photolithography to be left in the first recess **64** and its peripheral area.

[**0185**] Thus, as shown in **FIG. 14J, a** T-sectional shaped gate electrode **68**, which is Schottky-contacted to the AlGaAs Schottky layer **56** via the opening portion **62***a* and the second recess **64**, is formed of the Au layer **66** and the WSi layer **65**. A length of the gate electrode **68** between the source region and the drain region, i.e., the gate length, is set to less than 0.5 μm.

[**0186**] The silicon nitride film **62** and the silicon oxide film **70** are then patterned by the photolithography technique using the resist (not shown), so that two opening portions **62***s*,**62***d* are formed on the GaAs cap layer **59** on both sides of the gate electrode **68**. A multi-layered conductive film is formed by growing gold-germanium (AuGe)/nickel (Ni)/gold (Au) in sequence by virtue of evaporation.

[**0187**] The multi-layered conductive film is then patterned by the lift-off method. Thus, as shown in **FIG. 14**K, the multi-layered conductive film which are left in two opening portions **62***s*, **62***d* can be employed as a drain electrode **69***d* and a source electrode **69***s*.

[**0188**] After this, only the silicon oxide film **70** is removed by hydrogen fluoride. At this time, since the etching rate of the silicon nitride film **62** formed under the silicon oxide film **70** by the hydrogen fluoride is small 1/10 or less the silicon oxide, removal of the silicon nitride film **62** can be prevented.

[0189] In the HEMT or MESFET which is operated at a low frequency, there are the cases where the silicon oxide film **70** is not removed.

[0190] Accordingly, a basic structure of the HEMT is completed.

[0191] In the above steps of manufacturing the HEMT, the GaAs buried layer **57** is heated at the temperature of 500 to 700° C. after the silicon nitride film **62** has been formed. In this case, it has been found that, as shown in **FIG. 15**, the power adding efficiency is not lowered in the HEMT which is subjected to such heating even if the recess length L is reduced to less than 1.0 μm and that the power adding efficiency can be improved rather than the case where the recess length L is more than 1.0 μm.

[0192] In order to study the cause, for the HEMT which is heated at the temperature of 500 to 700° C. after the silicon nitride film **62** has been formed on the GaAs buried layer **57**, a relationship between the recess length L and a three-terminal breakdown voltage Vdsx in the HEMT has been examined. In addition, a relationship between the recess length L and the three-terminal breakdown voltage Vdsx in the HEMT without the silicon nitride film in the prior art has been examined.

[0193] Such relationships are shown in **FIG. 16**. It has been found that the three-terminal breakdown voltage Vdsx of the eighth embodiment of the present invention is higher than that of the prior art.

[0194] Accordingly, it has been found that heating of the HEMT at the temperature of 500 to 700° C. after the GaAs buried layer **57** has been covered with the silicon nitride film **62** can make the three-terminal breakdown voltage Vdsx higher, and as a result make the three-terminal breakdown voltage Vdsx higher.

[0195] The reason for enhancing the three-terminal breakdown voltage Vdsx in the eighth embodiment of the present invention in this manner will be supposed as follows.

[0196] First, in the prior art, when, as shown in **FIG. 17A, a** surface of the GaAs buried layer **57** is exposed to the oxygen containing atmosphere, GaAs reacts with oxygen (O) to then grow an As_2O_3 layer **71**, as shown in **FIG. 17B**. In this case, since As constituting the As_2O_3 layer **71** is supplied from the GaAs buried layer **57** formed below the As_2O_3 layer **71**, a gallium (Ga) layer **72** appears beneath the As_2O_3 layer **71**.

[0197] In addition, since the oxygen can bond more easily with the gallium than the arsenic, the oxygen in the As_2O_3 layer **71** is bonded with the gallium (Ga). Thus, as shown in **FIG. 17**C, the Ga layer **72** is changed into a Ga_2O_3 layer **72***a* and also the As_2O_3 layer **71** is changed into an As layer **71***a*.

[0198] Because the As layer **71***a* has higher conductivity than the GaAs buried layer **57**, the carriers are ready to shift via the As layer **71***a* to thereby make the three-terminal breakdown voltage (Vdsx) lower.

[0199] As shown in **FIG. 17**D, if the As layer **71***a* is covered with an oxygen containing film **80** such as SiO_2, the oxygen in the oxygen containing film **80** diffuses downward to then increase an amount of the As layer **71***a* and the Ga_2O_3 layer **72***a*. Thus, the three-terminal breakdown voltage (Vdsx) is decreased further more.

[0200] On the contrary, as shown in **FIGS. 18A** to **18**C, in the eighth embodiment of the present invention, the As layer **71***a* and the Ga_2O_3 layer **72***a* appear on the surface of the GaAs buried layer **57** because of the reaction with the oxygen in the oxygen containing atmosphere. The processes are similar to **FIGS. 17A** to **17**C until now.

[0201] As shown in **FIG. 18D, a** resultant structure is heated at the temperature of 500 to 700° C. after the As layer **71***a* has been covered with the silicon nitride (Si_3N_4) film **62**. Thus, as shown in **FIG. 18**E, As in the As layer **71***a* volatilizes to the outside through the silicon nitride film **62**. As a result, merely the Ga_2O_3 layer **72***a* of high resistance exists substantially between the GaAs buried layer **57** and the silicon nitride film **62**.

[0202] Therefore, since the As layer **71***a* produced on the GaAs buried layer **57** disappears, it is difficult for the carriers to shift through the overlying layer of the GaAs buried layer **57**, so that the three-terminal breakdown voltage (Vdsx) is increased.

[0203] In this manner, it has been found that, after the GaAs buried layer **57** has been covered with the silicon nitride film **62**, heating of the GaAs buried layer **57** at the temperature of 500 to 700° C. is important to improve the power adding efficiency.

[0204] By the way, the reason why the temperature at which the GaAs buried layer **57** is heated after the silicon nitride film **62** has been formed is set in the range of 500 to 700° C. can be given based on following experimental results.

[0205] First of all, a result shown in **FIG. 19** has been derived when a relationship between a heating temperature T and a drain current Imax is examined if a DC voltage is applied to the gate electrode **68** of the HEMT shown in **FIG. 14K**. In other words, the drain current Imax is reduced if the heating temperature T is set higher than 700° C., and the drain current Imax becomes lower than the target drain current value of 450 mA/mm at the temperature slightly higher than 700° C. The reason why the drain current is reduced lower as the heating temperature is increased higher than 700° C. is that the carriers are difficult to shift because semiconductor crystal in the 2-REG region of the electron travel layer is destroyed.

[0206] When a relationship between the heating temperature T and the three-terminal breakdown voltage (Vdsx) of the GaAs buried layer is examined, as shown in **FIG. 20**, the three-terminal breakdown voltage (Vdsx) is lowered regardless of the recess length if the heating temperature T is reduced than 500° C. This is due to the phenomenon shown in **FIGS. 18D and 18E**, i.e., the fact that the As layer **71***a* between the GaAs buried layer **57** and the silicon nitride film **62** hardly disappears and thus the leakage current is increased at the time when the high voltage is applied between the source and the drain, to thereby reduce the three-terminal breakdown voltage (Vdsx).

[0207] Next, under the conditions that the gate width is 600 μm and the frequency of the gate applied signal is 20 GHz, when a relationship between the recess length and a saturation output power (Pout) of the HEMT according to the eighth embodiment of the present invention is examined, the output becomes higher than the target value 25 dBm in the range where the recess length is shorter than 1.0 μm, as

shown in **FIG. 21**. As a result, in the HEMT according to the eighth embodiment of the present invention, the power adding efficiency can be increased.

[**0208**] In the eighth embodiment of the present invention, the first buffer layer is formed of the GaAs single layer, but it is not limited to such single layer. For example, as shown in **FIG. 22, a** multi-layered structure in which the undoped GaAs layer **52***a* and the undoped AlGaAs layer **52***b* are stacked alternatively may be employed. Also, the electron supply layer **55** is formed only on the electron travel layer **54** in the above HEMT, but the second electron supply layer **55***a* is formed below the electron travel layer **54**, as illustrated in **FIG. 22**.

[**0209**] As described above, according to the present invention, the first compound semiconductor layer whose donor concentration is set to 1×10^{16} atoms/cm^3 to 1×10^{17} atoms/cm^3 is provided between the cap layer and the carrier supply layer. Therefore, according to the donor of such concentration, the holes being separated in the channel layer can be prevented from reaching the surface of the first compound semiconductor layer, whereby contraction of the surface depletion layer can be suppressed and thus generation of the walk-out phenomenon can be prevented.

[**0210**] In this case, since the donor concentration is set to less than 1×10^{17} atoms/cm^3, the situation that the gate breakdown voltage is easily reduced because of high concentration of donor in the first compound semiconductor layer cannot be brought about.

[**0211**] According to another invention, since the bandgap of the Schottky layer formed on the carrier supply layer is set higher than that of the carrier supply layer, the energy barrier between the gate electrode and the Schottky layer can be enhanced to thus improve the gate breakdown voltage.

[**0212**] According to still another invention, the GaAs buried layer is heated after the silicon nitride film has been formed on the GaAs buried layer, in which the second recess is formed, in the region located on the inside of the first recess formed in the cap layer. Thus, even if the gallium oxide layer and the arsenic layer are generated because the surface of the GaAs buried layer is oxidized, such arsenic layer can be discharged into the outside through the silicon nitride film by heating, so that the three-terminal breakdown voltage (Vdsx) can be increased. The power adding efficiency can also be improved since the three-terminal breakdown voltage (Vdsx) can be increased.

[**0213**] As a result, if the interval between the first recess and the second recess is set to less than 1 μm, reduction in the power adding efficiency can be prevented.

What is claimed is:

1. A compound semiconductor device comprising:

a channel layer formed on a compound semiconductor substrate, and formed of material which has a first donor concentration and a first bandgap;

a carrier supply layer formed on the channel layer, and formed of material which has a second donor concentration being higher than the first donor concentration and a second bandgap being wider than the first bandgap;

a first compound semiconductor layer formed on the carrier supply layer, and containing donors in at least one of a lower layer portion and an upper layer portion within a range of impurity concentration of 1×10^{16} to 1×10^{17} atoms/cm^3;

a gate electrode connected to the first compound semiconductor layer;

a cap layer formed on the first compound semiconductor layer in a source region and a drain region which are formed on both sides of the gate electrode, and formed of material which has a third donor concentration being higher than the first donor concentration and a third bandgap being narrower than the second bandgap;

a source electrode at least a part of which is formed on the cap layer in the source region; and

a drain electrode at least a part of which is formed on the cap layer in the drain region.

2. A compound semiconductor device according to claim 1, wherein the lower layer portion of the first compound semiconductor layer is a Schottky layer which is connected to the gate electrode via Schottky junction, and the upper layer portion of the first compound semiconductor layer is a buried layer to cover the Schottky layer.

3. A compound semiconductor device according to claim 2, wherein a thickness of the buried layer is set to 15 to 50 nm.

4. A compound semiconductor device according to claim 1, further comprising a second carrier supply layer formed below the channel layer.

5. A compound semiconductor device according to claim 2, wherein the cap layer and the buried layer are formed of GaAs, the carrier supply layer and the Schottky layer are formed of AlGaAs, and the channel layer is formed of InGaAs.

6. A compound semiconductor device according to claim 2, wherein the carrier supply layer and the Schottky layer are formed of InGaP.

7. A compound semiconductor device comprising:

a channel layer formed on a compound semiconductor substrate, and formed of material which has a first donor concentration and a first bandgap;

a carrier supply layer formed on the channel layer, and formed of material which has a second donor concentration being higher than the first donor concentration and a second bandgap being wider than the first bandgap;

a Schottky layer formed on the carrier supply layer, and formed of material which has a third bandgap being wider than the second bandgap;

a gate electrode connected to the Schottky layer;

a buried layer having a recess in which a part of the gate electrode is buried;

a cap layer formed on the Schottky layer in a source region and a drain region which are formed on both sides of the gate electrode, and formed of material which has a third donor concentration being higher than the first donor concentration and a fourth bandgap being narrower than the second bandgap;

a source electrode at least a part of which is formed on the cap layer in the source region; and

a drain electrode at least a part of which is formed on the cap layer in the drain region.

8. A compound semiconductor device according to claim 7, wherein the source electrode and the drain electrode are formed to contact to a layer which is located lower than the cap layer and located higher than the carrier supply layer.

9. A compound semiconductor device according to claim 7, wherein the channel layer and the carrier supply layer are formed of AlxGa1-xAs whose composition ratio x of aluminum is less than 0.3, and the Schottky layer is formed of AlyGa1-yAs whose composition ratio y of aluminum is more than 0.3.

10. A compound semiconductor device according to claim 7, wherein a total film thickness from the Schottky layer to the cap layer is less than 100 nm.

11. A compound semiconductor device according to claim 4, further comprising a second carrier supply layer formed below the channel layer.

12. A compound semiconductor device according to claim 4, wherein the cap layer and the buried layer are formed of GaAs, the carrier supply layer and the Schottky layer are formed of AlGaAs, and the channel layer is formed of InGaAs.

13. A compound semiconductor device according to claim 10, wherein the carrier supply layer is formed of InGaP, and the Schottky layer and the second carrier supply layer are formed of AlGaAs.

14. A compound semiconductor device according to claim 7, wherein the carrier supply layer and the Schottky layer are formed of InGaP.

15. A method of manufacturing a compound semiconductor device comprising the steps of:

forming a channel layer on a semiconductor substrate;

forming a carrier supply layer, which supplies carriers to the channel layer, on the channel layer;

forming a first gallium-arsenic layer on the carrier supply layer;

forming a silicon nitride film on the first gallium-arsenic layer;

heating the first gallium-arsenic layer which is covered with the silicon nitride film;

forming an opening portion by selectively etching the silicon nitride film on a gate region;

forming a first recess by etching the gallium-arsenic layer via the opening portion;

forming a gate electrode on the gate region of the carrier supply layer via the first recess;

forming a source opening portion and a drain opening portion in the first gallium-arsenic layer on both sides of the first recess by patterning the silicon nitride film; and

forming a source electrode on or above the first gallium-arsenic layer via the source opening portion and forming a drain electrode on or above the first gallium-arsenic layer via the drain opening portion.

16. A method of manufacturing a compound semiconductor device according to claim 15, further comprising the step of:

forming a Schottky semiconductor layer between the carrier supply layer and the first gallium-arsenic layer on the first gallium-arsenic layer; and

forming a second recess, which is wider than the first recess, by etching the second gallium-arsenic layer in the gate region and an environment of the same.

17. A method of manufacturing a compound semiconductor device according to claim 16, further comprising the step of:

forming an aluminum-gallium-arsenic etching stopper layer between the first gallium-arsenic layer and the second gallium-arsenic layer; and

wherein etching of the second gallium-arsenic layer in forming the second recess is stopped at a point of time when the aluminum-gallium-arsenic etching stopper layer is exposed, and the aluminum-gallium-arsenic etching stopper layer which appears from the second recess is removed after the second recess has been formed.

18. A method of manufacturing a compound semiconductor device according to claim 15, wherein a temperature employed to heat the first gallium-arsenic layer is set in a range of 500 to 700° C.

19. A compound semiconductor device comprising:

a channel layer formed on a semiconductor substrate;

a carrier supply layer formed on the channel layer;

a Schottky semiconductor layer formed on the carrier supply layer and having a gate connection region;

a gallium-arsenic buried layer formed on the Schottky semiconductor layer;

a gallium-arsenic cap layer formed on the gallium-arsenic buried layer;

a first recess formed in the gallium-arsenic cap layer to expose a part of the gallium-arsenic buried layer, and having a width which is wider than the gate connection region;

a second recess formed in the gallium-arsenic buried layer to expose the gate connection region of the Schottky semiconductor layer;

a silicon nitride film provided in the first recess to extend from an end surface of the second recess onto the gallium-arsenic buried layer and the gallium-arsenic cap layer;

a gate electrode connected to the Schottky semiconductor layer in the second recess; and

a source electrode and a drain electrode formed on the gallium-arsenic cap layer respectively.

20. A compound semiconductor device according to claim 19, wherein an interval between the first recess and the second recess is smaller than 1 μm.

21. A compound semiconductor device according to claim 19, wherein a length of the gate electrode along a direction from the source electrode to the drain electrode is shorter than 0.5 μm.

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