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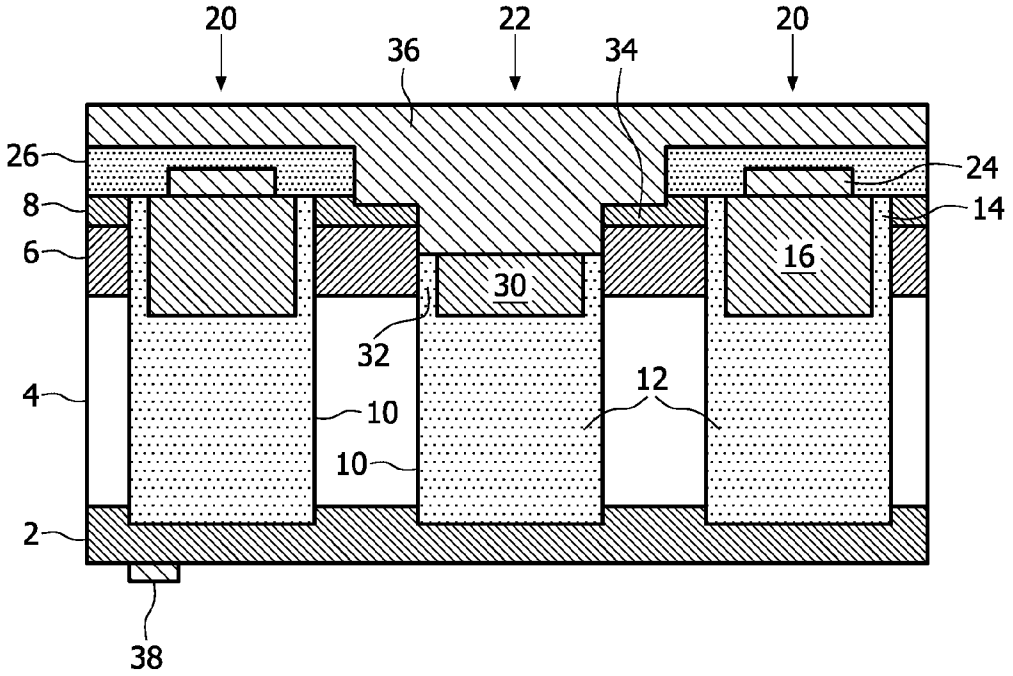
(54) Title: TRENCH FIELD EFFECT TRANSISTORS



(57) Abstract: Trench field effect transistors (trench FETs) include alternating gate trenches (20) and source trenches (22). The gate trenches (20) include insulated gates (16). The source trenches (22) include a source connected conductive layer (30) and insulated sidewalls (32). A source electrode (36) extends into the top of the source trenches (22) to contact the source connected conductive layer (30) as well as the source electrode (8) and body (6), the latter being contacted at the side of the source trenches (22). The field effect transistors can deliver a useful combination of switching speed, specific on-resistance and breakdown voltage.

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DESCRIPTION

TRENCH FIELD EFFECT TRANSISTORS

The invention relates to Trench gated Field Effect Transistors (Trench FETs) and to methods of making them.

Trench FETs have a number of applications, including in particular the use as so-called control or sync FETs for switching power applications.

An approach to trench FETs according to related art is shown in Figure 1. A substrate is heavily doped n+ to provide a highly doped drain region 2, and a low doped drain region 4 doped n-type is provided on top. A p-type body region 6 is provided on the drain region, and a n+ doped source region 8 is provided on top of the body region.

Insulated trenches 10 define mesas 18 between the trenches. The trenches 10 are each filled with a plug 12 at the base of the trench and a gate 16 above the plug. The gate 16 is insulated from the body region 6 with gate insulator 14 on the sidewalls of the trenches.

The n+ doped source region 8 is provided adjacent to the trenches. However, in order that a source electrode can also connect to the body 6, the source region 8 is not provided in the centre of the mesas to allow the body region 6 to be exposed there for connection to the source electrode.

In operation, voltage applied to the gate creates a channel adjacent to the trench through the body region.

A useful figure of merit for Trench FETs is the specific on-resistance, R_{dson}, i.e. the resistance of the transistor per unit area in the on-state. It is desirable to reduce this value. To reduce the specific on-resistance in such structures it is usual to use thin trench widths to achieve a short cell pitch, for example 1 μm, to increase the number of channels per unit width and hence to decrease the resistance in the on state. Even shorter cell pitches are possible, for example using deep ultra-violet processing techniques.

However, a problem of using this approach is that it provides an undesirable rise in the gate resistance. Long lengths of very narrow gate require a number of connections using additional gate bus bars to avoid the gate resistance being too high.

A further problem is that the narrow pitches give rise to higher capacitances, for example the gate-source capacitance and gate-drain capacitance. These result in higher switching and gate driver losses.

A still further problem is that the connection to both source 8 and body 6 is very difficult when the mesa width is narrow.

Low-voltage trench MOSFETs are commonly used, for example in voltage regulator modules (VRMs) in power supplies for electronic equipment such as personal computers. Commonly, a pair of MOSFETs are used, known as a control FET and a sync FET. The ideal characteristics of these FETs differ slightly. For the sync FET the power loss in the conducting state should be as low as possible. Since this power loss is proportional to the specific on-resistance, this resistance should be as low as possible. For the control FET on the other hand the switching loss should be minimised. This switching loss is proportional to the gate-drain charge per unit area, the gate-drain charge density.

A figure of merit (FOM) has been defined as the multiple of the specific on-resistance and the gate-drain charge density to provide a measure of how suitable a transistor is for use in VRMs. The smaller the FOM the better.

A known approach to achieving an improved transistor is described in US 5,637,898 (Baliga). The gate in the trench may have a stepped gate structure so that the gate is closer to the base region than the drift region, with a thicker insulating layer between the gate and most of the drift region than the thin gate insulating layer between the gate and the base region. However, this by no means eliminates all disadvantages and there remains a need for an improved trench-gated FET design.

According to the invention, there is provided a semiconductor device according to claim 1.

By adopting a structure where each gate trench is surrounded by trenches connected to the source regions, the source connected trenches may be used to assist in the depletion of the mesas in the off state and so support a significant gate voltage in the off state with a significant doping in the drain region in the mesas thereby ensuring a lower resistance in the on-state by the so-called reduced surface field (RESURF) effect.

The source connected stripe lowers the gate source and gate drain capacitances simply by increasing the effective gate pitch compared with a structure in which each trench includes a gate.

A particular benefit is that the source electrode can connect to both the source and body at the source trench therefore avoiding the need for small source electrodes to be patterned on the first major surface. This enables the trenches to be closer together than is possible in the related art.

It might be thought that the best devices would have the maximum possible density of trenches, and hence channels. However, in embodiments of the invention the increased width of the trench compared with the mesas allows an improved figure of merit.

Embodiments of the invention will now be described, purely by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a trench FET according to related art;

Figure 2 shows a section through a trench FET according to a first embodiment of the invention;

Figure 3 shows a section through a trench FET according to a second embodiment of the invention;

Figure 4 shows a top view of a trench FET according to a third embodiment of the invention;

Figures 5 and 6 show results on simulations of the device of Figure 1;

Figures 7 and 8 show results on simulations of the device of Figure 2; and

Figures 9 and 10 show results on simulations of the device of Figure 3;

Figure 11 shows a top view of a trench FET according to a fourth embodiment of the invention; and

Figure 12 shows a side view of a trench FET according to a preferred implementation of the fourth embodiment.

The drawings are schematic and not to scale. Like components are given the same reference numerals in different figures.

Referring to Figure 2, a silicon substrate is heavily doped n+ to provide a highly doped drain region 2, and a low doped drain region 4 doped n-type is provided on top. The low doped drain region may also be referred to as a drift region, and as the name suggests has a lower doping than the highly doped drain region 2. The doping in the low doped drain region is such that the region can be depleted with the transistor off to support a voltage across it. The drain region 2,4 is made up of the highly doped and low doped regions together. A p-type body region 6 is provided on the drain region, and a n+ doped source region 8 is provided on top of the body region.

Insulated trenches 10 are provided, defining mesas 18 between the insulated trenches 10. The mesas are made up of the top of the highly doped drain region 2, the low doped drain region 4, the body region 6 and the source region 8.

The insulated trenches are filled with a plug 12 at the base of the trench. Unlike the related art of Figure 1, Figure 2 shows trenches alternating between a gate trench 20 and a source trench 22. In the embodiment, the plug is of silicon dioxide, though alternatives may be used.

The gate trenches 20 include a gate 16 of doped polysilicon above the plug 12, the gate being insulated with gate insulator 14 on the sidewalls of the trenches from the body region 6. The gate extends to a depth just below the interface between the body region 6 and the low doped drain region 4, so that the gate is adjacent to the full thickness of the body region. Any suitable gate insulator material may be used, for example silicon dioxide, silicon nitride, or multiple layers of these materials.

A gate electrode 24 of aluminium extends along the length of the gate trenches, the gate electrode being in contact with the gate 16 along the length of the gate 16. An insulating layer 26 covers the gate electrode 24.

The source trenches 22 also include the plug 12, and above that a conductive trench source region 30, which like the gate 16 is insulated from the adjacent mesa, in this case by source insulating layer 32 on the sidewalls of the trenches. The bottom of the trench source region 30 is just below the interface between the body region 6 and the low doped drain region 4. The top of the trench source region 30 is level with the top of the source insulating layer 32, but below the level of the junction between the source 8 and body 6 in the mesa 18. In the embodiment, the trench source region is of polysilicon.

A via hole 34 is provided in insulating layer 26 in communication with the top of source trench 22. The via hole 34 is slightly wider than the source trench 22, and extends just into the top of the source layer 8.

A source electrode 36 of aluminium fills the top of the source trench 22 above the top of the trench source region 30 and insulating layer 32. It is in contact with both the body region 6 and the source region 8 in the adjoining mesas 18. The contact of the source electrode 36 with the source region 8 is both on the side of the source region and the top of the source region 8 by virtue of the greater width of the via hole 34 than the source trench 22. This ensures a good contact to the source.

A drain contact 38 is provided contacting substrate 2.

The embodiment may be readily manufactured. A substrate 2 has an epilayer 4 deposited on it doped to provide the required doping in the low doped drain region. The body 6 and source regions 8 are prepared by implantation. The trenches are then etched, the plugs filled at the base of the trenches, and insulator used on the sidewalls of the trenches to form gate insulator 14 and source insulator 32. The gates 16 and trench source region 30 are then formed in the trenches. The gate electrode 24 is deposited and patterned, followed by insulating layer 26. The stepped via holes 34 are then formed and filled with the aluminium source electrode 36 to contact source 8 and body 6 as well as the trench source region 30.

Those skilled in the art will realise that the size and composition of the various components can be varied. A specific embodiment has been simulated, and the results are below.

The parameters for the specific embodiment are a trench width of 1.0 μm and a mesa width of 0.5 μm. Thus, the cell pitch is 3.0 μm. The trench depth is 1.7 μm. The doping concentration of the low doped drain region is $5.2x10^{16}cm^{-3}$, and the resistivity of the low doped drain region is 0.13 Ωcm and the total thickness of the source region 8, body region 6, and low doped drain region 4 is 1.7 μm. The gate 16 has a depth of 0.7 μm, and the boundary between the body region 6 and source region 8 is at the same depth. The channel length, i.e. the thickness of the body region 6, is approximately 0.5 μm. The thickness of the low doped drain region is approximately 1.0 μm and the source is a shallow 0.15 μm. The substrate 2 contribution to the total resistance is $1.5m\Omega.mm^2$.

Note in particular the feature that the trench width is significantly greater than the mesa width.

Figure 3 shows an alternative embodiment that is the same as the arrangement of Figure 2 except for the provision of a source connected conductor 50 in the gate trench 20 as well as in the source trench. This structure was simulated to achieve breakdown voltages in excess of 45 V with a similar size to the arrangements of Figures 2 and 3. In order for a sensible comparison between devices of different properties to be made, the trench depth and the total thickness of the source region 8, body region 6, and low doped drain region 4 was reduced from 1.7 μm to 1.4 μm.

Figure 4 illustrates a top view of a trench FET according to a further embodiment in which an edge termination structure 60 surrounds an active region 62. The edge termination structure is at least one source trench 22 – in the example two source trenches are used but this may be varied as required. The structure may use source and gate trenches according to the embodiment of either Figure 2 or 3, or indeed any suitable structure.

The remaining Figures show simulated results for Figure 1 (the related art) as well as the embodiments of Figures 2 and 3.

Figures 5 and 6 are the results for the related art of Figure 1. Figure 4 shows the on-state resistance against gate voltage, and Figure 5 shows the current on a log scale against drain voltage, thereby showing the breakdown voltage.

The simulations for the basic structure of Figure 1 achieves partial RESURF with a breakdown voltage (measured at 240 μA) of 33.8 V. At a gate voltage of 4.5V, the specific on-resistance is 8.55 $m\Omega.mm^2$. A figure of merit (FOM) is calculated by multiplying the specific on-resistance by the gate-drain charge density (Q_{gd}) which at 4.5 V gives the FOM of 13.6 $nC.m\Omega$. The specific on-resistance was also calculated at a gate voltage of 10 V to be 6.52 $m\Omega.mm^2$ and the FOM was calculated to be 10.6 $nC.m\Omega$.

Figures 7 and 8 are for the embodiment of Figure 2. Figure 7 shows the on-state resistance against gate voltage, and Figure 8 shows the current on a log scale against drain voltage, thereby showing the breakdown voltage.

The embodiment of Figure 2 shows improved results. At 4.5 V the specific on-resistance is 12.4 $m\Omega.mm^2$. Although this is marginally worse, though still very respectable, the figure of merit (FOM) is 9.2 $nC.m\Omega$, which is better (lower). A similar effect occurs at a gate voltage of 10 V, for which the specific on-resistance is 8.47 $m\Omega.mm^2$ and the FOM 6.27 $nC.m\Omega$.

Thus, significant improvements in switching are achieved with a specific on-resistance that remains good and a breakdown voltage of 33.2V.

Figures 9 and 10 are for the embodiment of Figure 3. Figure 8 shows the on-state resistance against gate voltage, and Figure 9 shows the current on a log scale against drain voltage, thereby showing the breakdown voltage.

The embodiment of Figure 3 achieves a breakdown voltage of 34.3V. At a gate voltage of 4.5 V the specific on-resistance is 10.5 $m\Omega.mm^2$, and the FOM 7.05 $nC.m\Omega$. At a gate voltage of 10V, the specific on-resistance is 7.00$m\Omega.mm^2$, and the FOM 4.70 $nC.m\Omega$.

Thus, this structure achieves the best results.

Without wishing to commit themselves to any theory, the inventors believe that the mesas are fully depleted at low drain-source voltage which permits the use of short channel lengths in these embodiments, and

corresponding shallow trenches. The greater width of the trenches over the mesas mitigates any problem with very small structures since it both decreases the resistance of the gate 16 and also permits the deposition of the gate electrode 24 of aluminium directly over the gate 16 along the full length of the gate greatly increasing the current carrying capacity of the gate 16.

The use of the thick oxide plug 12 (1 μm in embodiment 2) below the gate ensures that the gate-drain capacitance is minimised.

The narrow mesas 18 allow the mesas to be readily depleted which improves the RESURF effect. This means that doping levels can be higher, particularly in epilayer 4.

The trench source region 30 has three benefits in the embodiments. Firstly, it reduces the cell pitch reducing gate-source capacitance and gate-drain capacitance. Secondly, the trench source region 30 connects to both source and body on the sidewalls of the source trench 22 avoiding the need to expose both body and source at the top of the mesa which in turn makes smaller mesas possible.

The third benefit is that the source trenches can be used in exactly the same form in the periphery of the device as a terminating region thus avoiding the need for separate field plates.

An alternative approach to arranging the source and gate trenches 20,22 is illustrated in Figure 11, in top view. In this approach, the source trenches 22 are provided as trenches extending within a semiconductor mesa 18. In the embodiment shown the mesa 18 is in the form of a square ring around the source trench 22. A plurality of gate trenches 20 surround the semiconductor mesa; the gate trenches 20 are connected together to form a conductive gate trench network as illustrated in Figure 11.

In a preferred arrangement, the outer squares of mesas 18 are 2.0 μm across, the source trenches 22 are 1 μm across, the gate trenches 20 are likewise 1 μm across, making the width of the mesa 18 between source trench 22 and gate 0.5 μm.

The contents of source and gate trenches 20,22 may be the same as described above with respect to Figure 2, Figure 3, or other alternatives as

discussed above. Thus, the semiconductor mesa 18 may have a highly doped drain region 2, a low doped drain region 4, a body region 6 and a source region 8 as in the above embodiments.

Further, the source trenches 22 may contain polysilicon 36 in electrical contact with the body region 6 and source region 8 in the mesa 18 surrounding the source trench 22. The polysilicon 36 in the source trenches 22 may extend downwards to just below the boundary between body region 6 and low doped drain region 4 in the mesa 70, or this may be varied. For example, for higher voltages the polysilicon 36 may be present alongside the low doped drain region 4 to help deplete this region. Indeed, the polysilicon may extend for substantially the whole of the depth of the source trench 22.

The gate trench may include plug 12, gate 16, gate insulator 14, and optionally source connected conductor 50 of the type illustrated in Figure 3.

A preferred embodiment using the configuration of Figure 11 is illustrated in side view in Figure 12. For a particularly effective depletion of the low doped drain region, a source connected conductor 50 may be provided adjacent to the low doped drain region in the gate trench 20, and the polysilicon 36 in the source trench 22 may also extend down to be adjacent to the low doped drain region 4. In this way, the low doped drain region can be depleted from both sides. Those skilled in the art will realise that many alternatives are possible.

The mesas 18 may be square, rectangular, or of different form, for example a hexagonal arrangement of mesas may be used.

The various conductive layers can be formed of many different materials, including doped polysilicon or amorphous silicon, metals such as aluminium or copper, metal silicides, alloys of metals and any other suitable conductive material compatible with the semiconductor processes used.

Similarly, a variety of insulating materials are possible such as silicon dioxide, silicon nitride, spin-on glasses, TEOS layers, or any of a wide variety of insulating layers.

The p-type and n-type layers may be reversed to form a FET of opposite conductivity type.

Although the above embodiments are described using a silicon substrate, other semiconductors including for example gallium arsenide, silicon germanium, or more complex arrangements including silicon on insulator may also be used.

The widths, thicknesses and layouts of the various layers may also be changed as required.

CLAIMS

1. A semiconductor device, comprising:

a drain region (2,4) doped to be a first conductivity type;

a body region (6) doped to be a second conductivity type opposite to the first conductivity type on the drain region (2,4);

a source region (8) doped to be a first conductivity type on the body region (6) at a first major surface,

a plurality of trenches (10) extending from the first major surface through the source (8) and body (6) regions into the drain regions (2,4) dividing the source (8) and body region (6), the plurality of trenches dividing the source (8) and body (6) regions into a plurality of mesas (18) including the source (8) and body (6) regions, the trenches (10) including a plurality of gate trenches (20) each including an insulating plug (12) at the base of the trench, and a conductive gate (16) above the insulated plug (12), the conductive gate (16) being insulated from the body region by a gate insulating layer (14) at the sidewall of the trenches (20),

a gate electrode (24) connected in common to the gates (16) of the gate trenches (20); and

a drain electrode (38) connected to the drain region (2,4);

wherein the plurality of trenches (10) further include a plurality of source trenches (22), the source trenches (22) including an insulating plug (12) at the base of the trenches (22) and a trench source region (30) above the insulating plug (12) spaced from the mesas (18) by insulating side walls (32), the trench source regions (30) extending in the trench to below or at the interface between the body regions (6) and drain regions (2,4);

the semiconductor device further comprising a source electrode extending into the source trenches (22) to connect to the trench source regions (30), the source regions (8) and the body regions (6) at the side of the source trenches (22);

wherein the width of the source and gate trenches (20,22) is at least 1.5 times the width of the mesas (18) between the source and gate trenches (20,22).

2. A semiconductor device according to claim 1 wherein the source trenches (22) and gate trenches (20) alternate across the first major surface.

3. A semiconductor device according to claim 1 wherein the mesas (18) have the form of a ring extending around a respective source trench (20).

4. A semiconductor device according to any preceding claim wherein the width of the source and gate trenches (20,22) is in the range 0.75 μm to 2 μm and the width of the mesas (18) between the trenches is in the range 0.1 μm to 0.75 μm.

5. A semiconductor device according to any preceding claim wherein the thickness of the body region (6) is in the range 0.2 μm to 1 μm.

6. A semiconductor device according to any preceding claim wherein the gate electrodes (24) extend along the gate trenches (20) above and in contact with the gate (16).

7. A semiconductor device according to any preceding claim wherein the drain region (2,4) includes a low doped drain region (4) adjacent to the body region (6) and a high doped drain region (2), the source and gate trenches (20,22) extending through the low doped drain region (4) into the high doped drain regions (2).

8. A semiconductor device according to any preceding claim wherein the gate (16) is a stepped structure that has a first wider region (42) adjacent to the body region (6) and a second narrower region (44) adjacent to the drain region (2,4).

9. A semiconductor device according to any of claims 1 to 7 further comprising an insulated source metallisation (50) in the gate trenches (20) connected to the source electrode (36) and extending in the gate trenches (20) between the gate (16) and the base of the gate trenches (20).

10. A semiconductor device according to any preceding claim wherein the top of the trench source region (30) and the insulating sidewalls (32) are below the interface between the source region (8) and the body region (6) so that the source electrode (36) fills the trench above the trench source region (30) to be in contact with the body region (6) and the source region (8).

11. A semiconductor device according to any preceding claim further comprising an edge termination structure (60) formed of at least one source trench (22) extending around an active region (62).

12. A method of making a semiconductor device, comprising:

providing a drain region (2,4) doped to be a first conductivity type;

forming a body region (6) doped to be a second conductivity type opposite to the first conductivity type on the drain region;

forming a source region (8) doped to be a first conductivity type on the body region at the first major surface,

etching a plurality of trenches (10) extending from the first major surface through the source and body regions into the drain regions (2,4), the trenches including source trenches (22) and gate trenches (20);

filling the plurality of trenches (10) with an insulating plug (12) at the base of the trenches (10);

forming an insulating layer (14) on the sidewalls of the gate trenches (20) to form gate insulator and the sidewalls of the source trenches (22) to form source insulator;

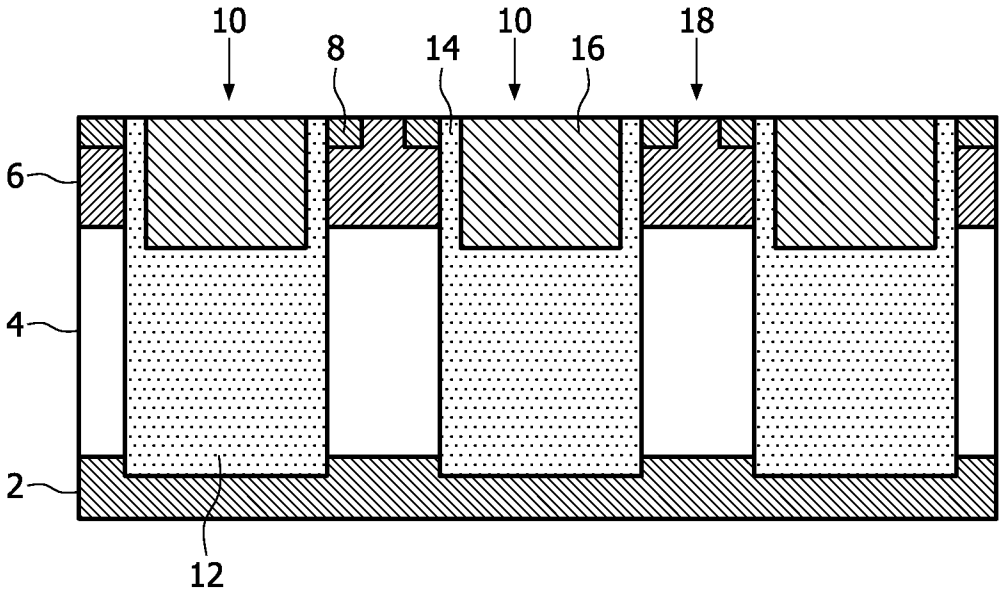
forming conductive gates (16) extending along the gate trenches (20) between the gate insulator on the sidewalls;

forming trench source regions (30) extending along the source trenches (22) between the source insulator on the sidewalls;

forming a drain electrode (38) connected to the drain region (2);

forming a gate electrode (24) connected in common to the conductive gates (16); and

forming a source electrode (36) connected in common to the source regions (8), the body regions (6) and the trench source regions (30).


10
8
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18
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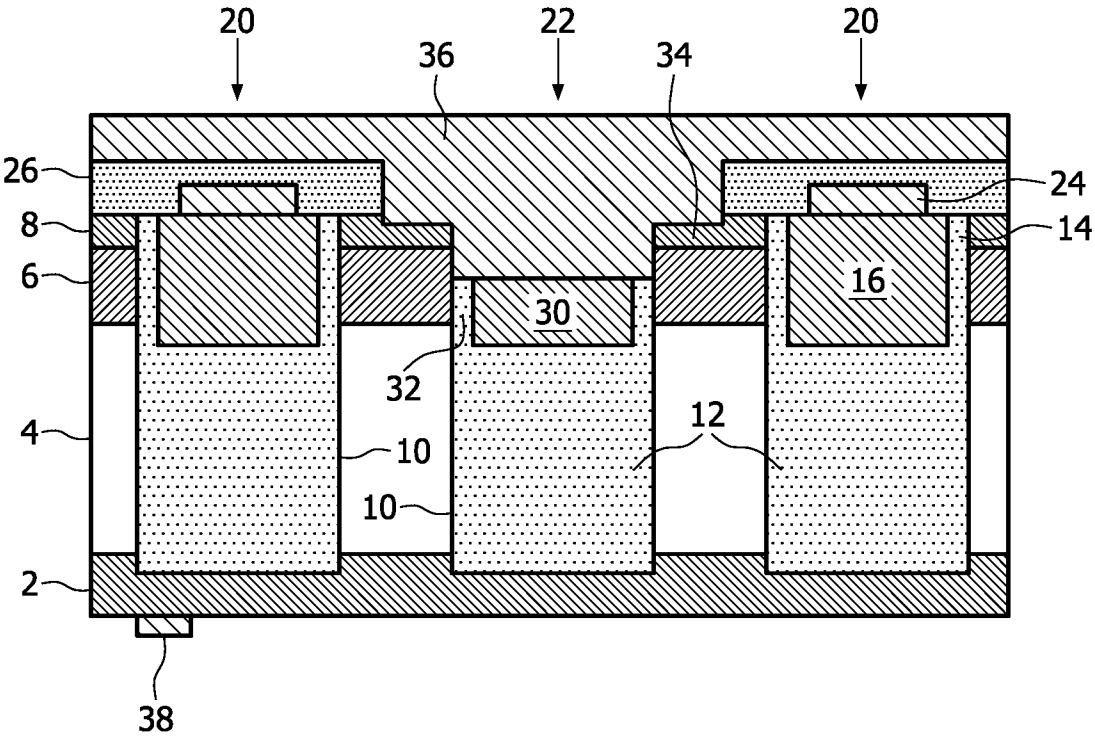
12

FIG. 1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38

FIG. 2

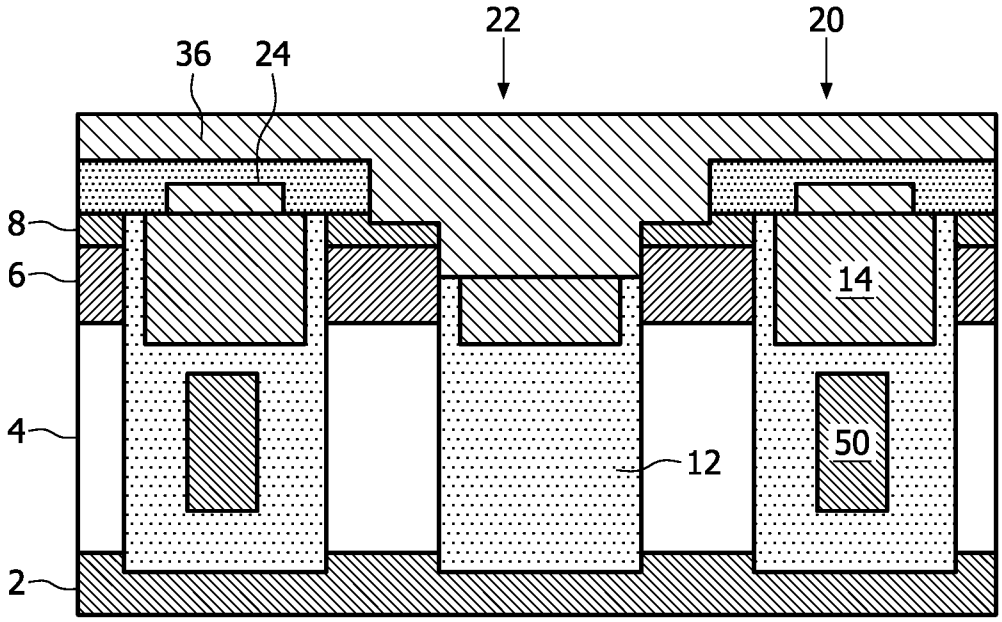


FIG. 3

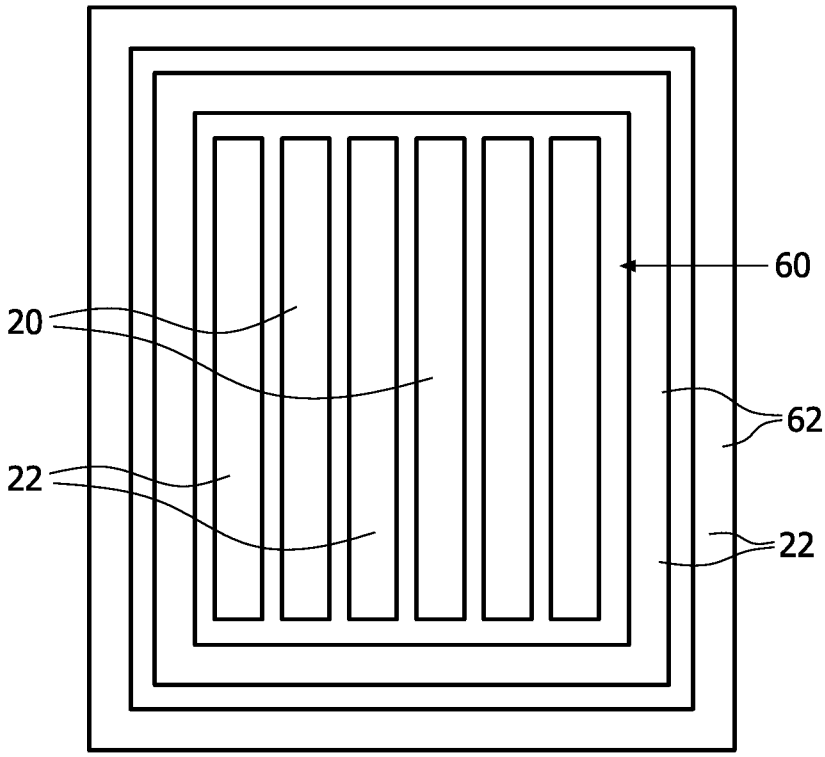
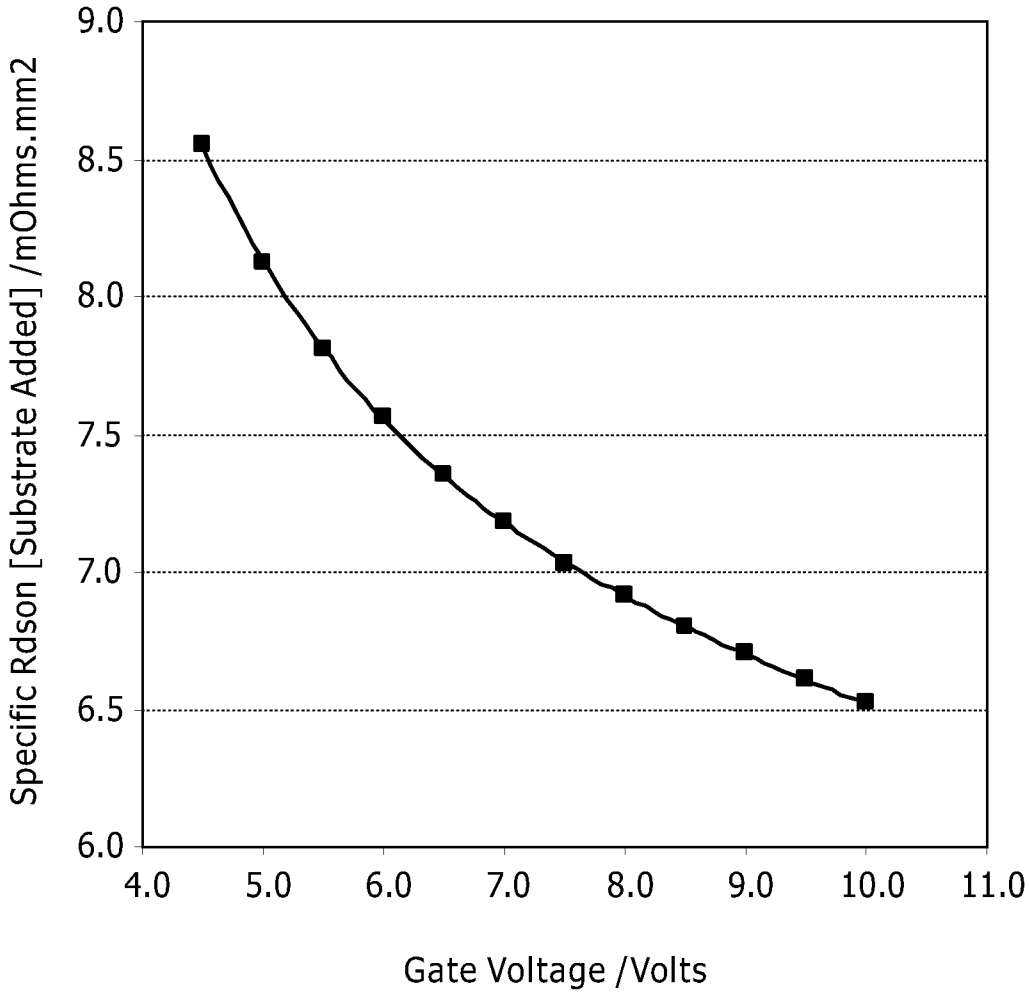


FIG. 4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8.0
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10.0
11.0
Gate Voltage /Volts

FIG. 5

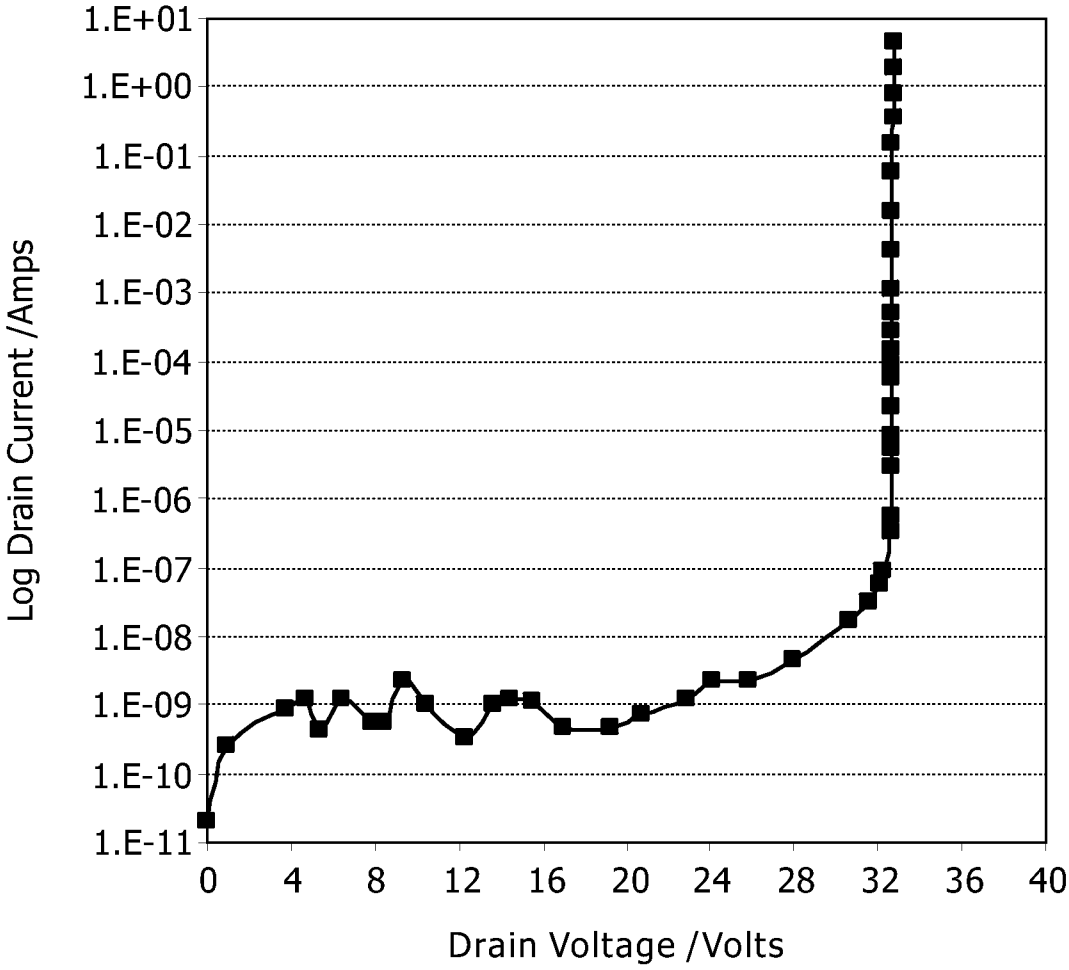
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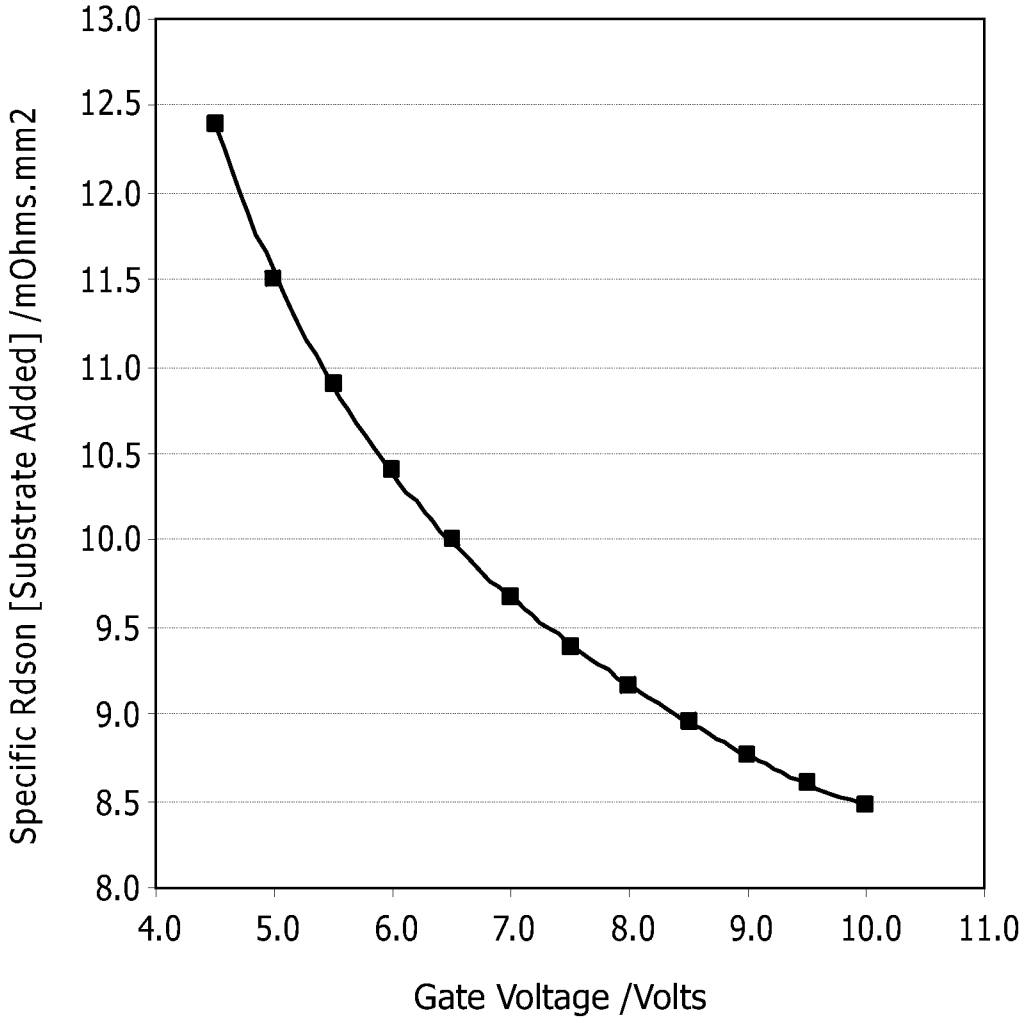
FIG. 6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8.0
Specific Rdson [Substrate Added] /mOhms.mm2
4.0
5.0
6.0
7.0
8.0
9.0
10.0
11.0
Gate Voltage /Volts

FIG. 7

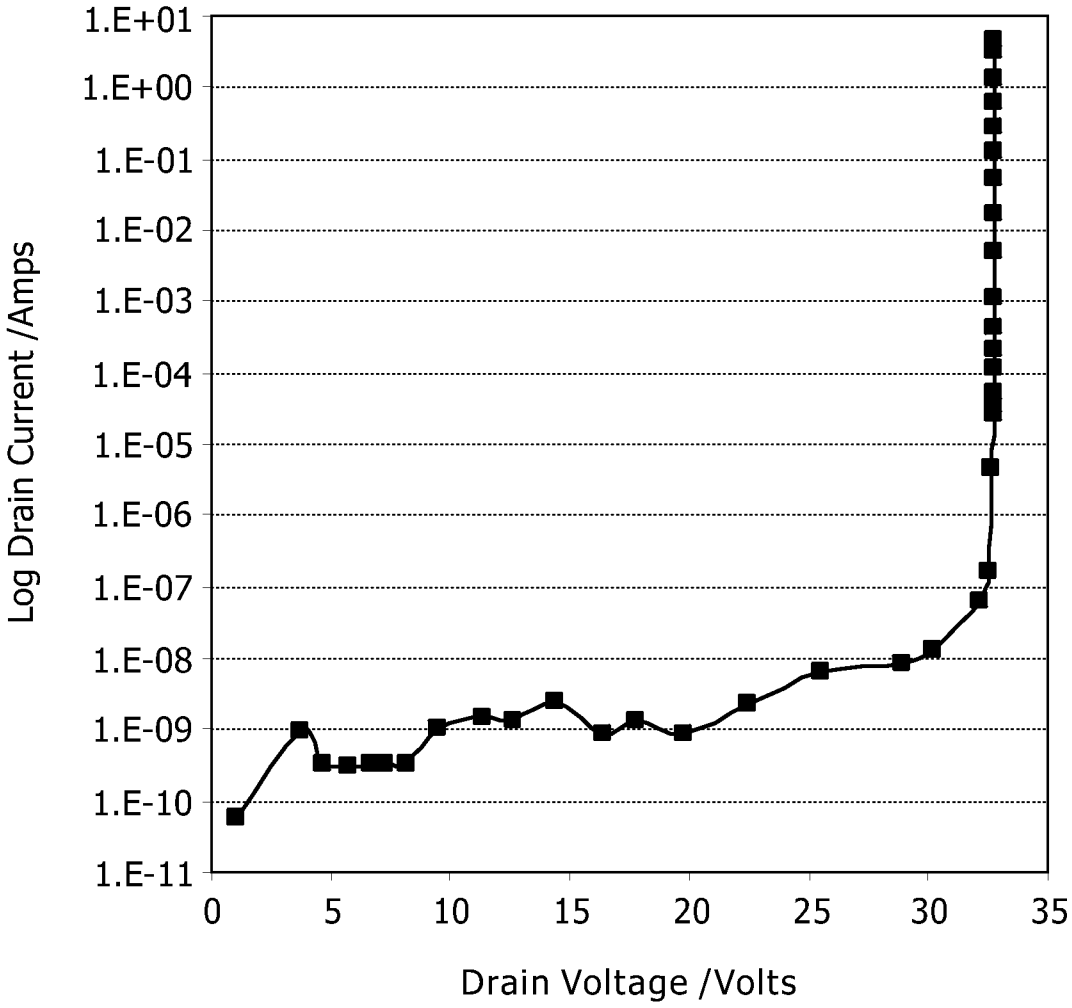
1.E+01
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
Log Drain Current /Amps
0
5
10
15
20
25
30
35
Drain Voltage /Volts

FIG. 8

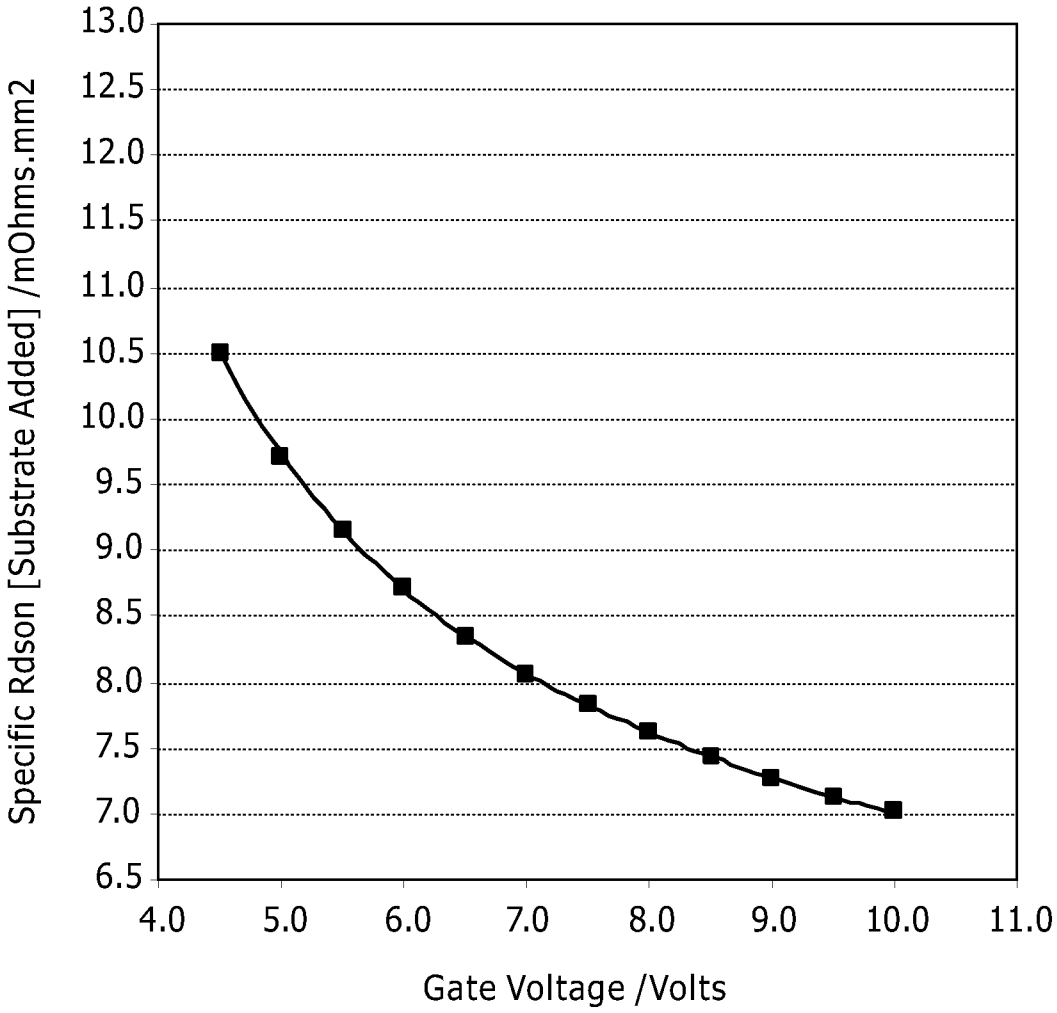
13.0
12.5
12.0
11.5
11.0
10.5
10.0
9.5
9.0
8.5
8.0
7.5
7.0
6.5
Specific Rdson [Substrate Added] /mOhms.mm2
4.0
5.0
6.0
7.0
8.0
9.0
10.0
11.0
Gate Voltage /Volts

FIG. 9

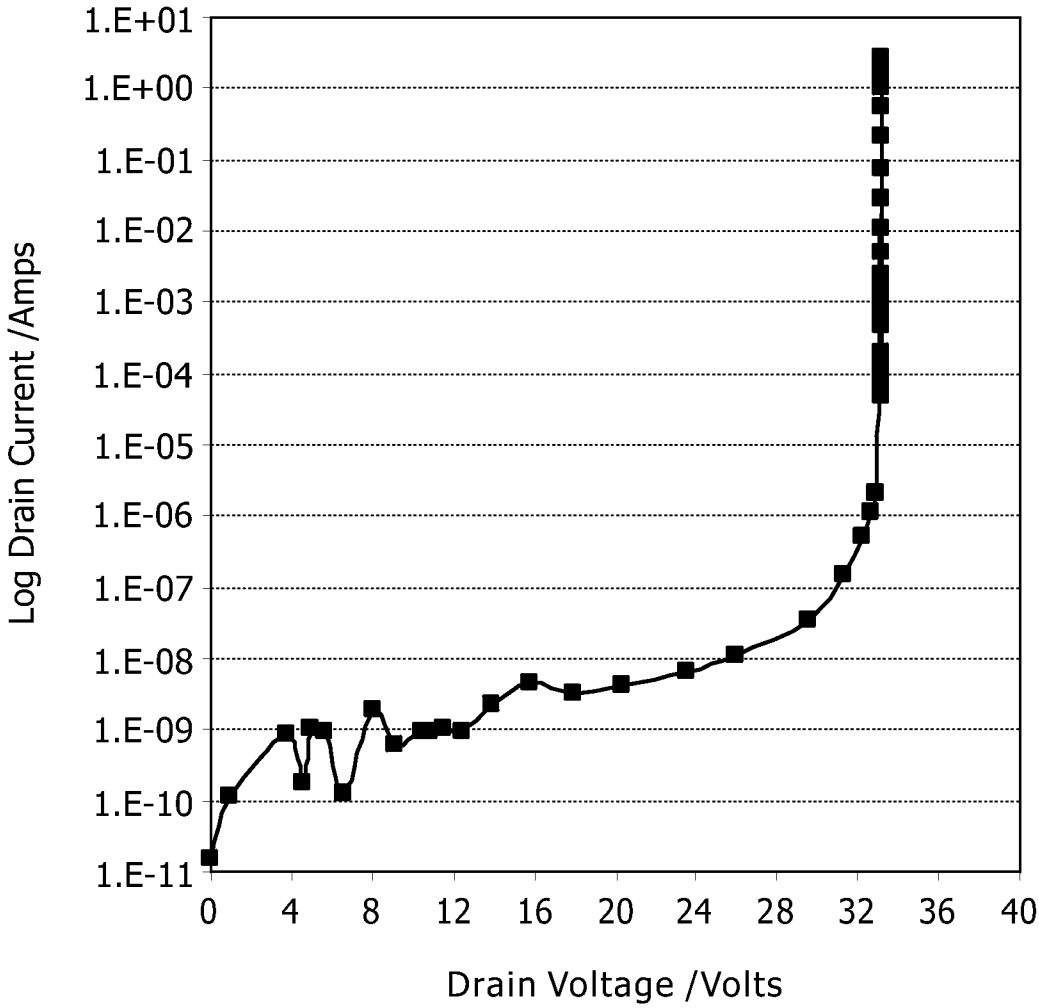
1.E+01
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
Log Drain Current /Amps
0
4
8
12
16
20
24
28
32
36
40
Drain Voltage /Volts

FIG. 10