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(54) METHOD AND APPARATUS FOR CONTROLLING METAL DOPING OF A CHALCOGENIDE MEMORY ELEMENT

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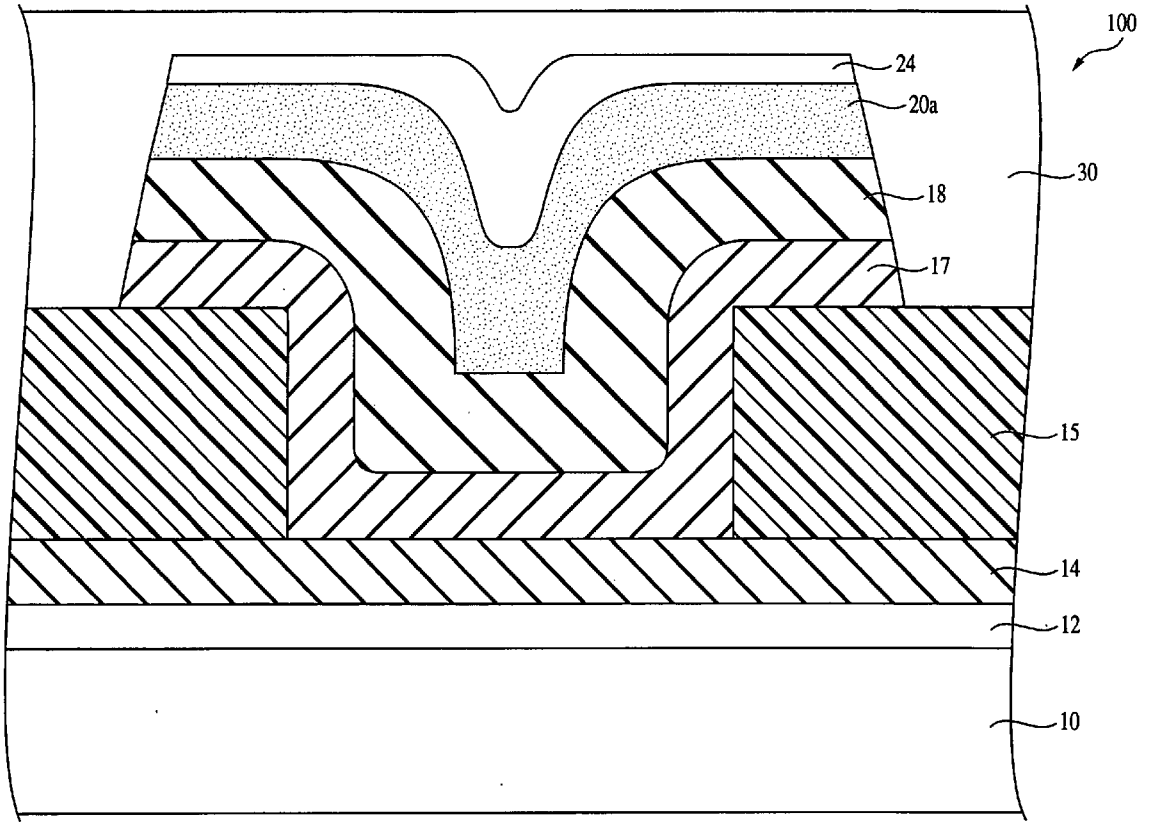
(52) **U.S. Cl.** **257/42**

(57) **ABSTRACT**

A method for controlling silver doping of a chalcogenide glass in a resistance variable memory element is disclosed herein. The method includes forming a silver layer over a chalcogenide glass layer. Processing the silver layer via heat treating, light irradiation, or a combination of both to form a layer comprising silver interstitially formed in a chalcogenide glass layer; silver-selenide formed in a layer comprising silver interstitially formed in a chalcogenide glass layer; or a silver doped chalcogenide glass layer having silver-selenide formed therein.



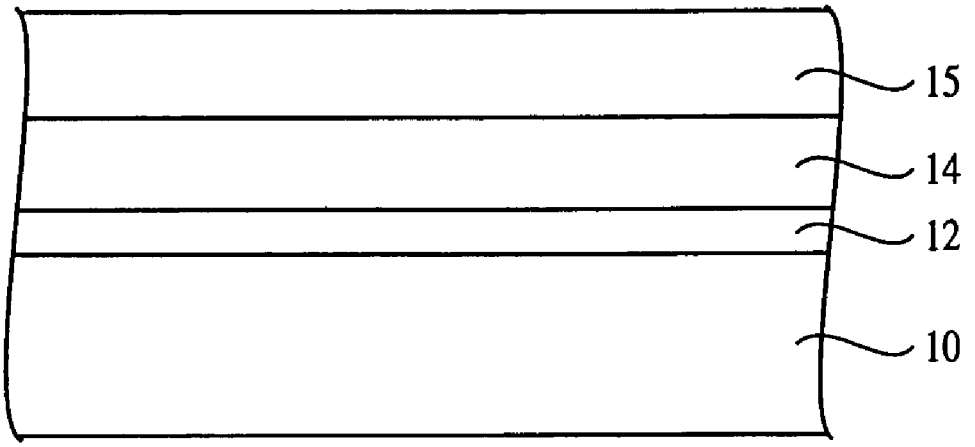


FIG. 1

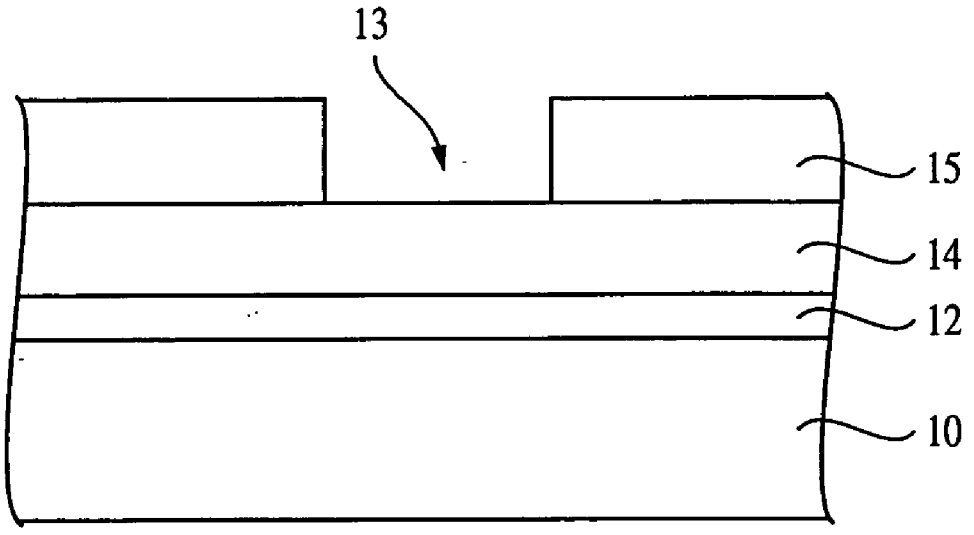


FIG. 2

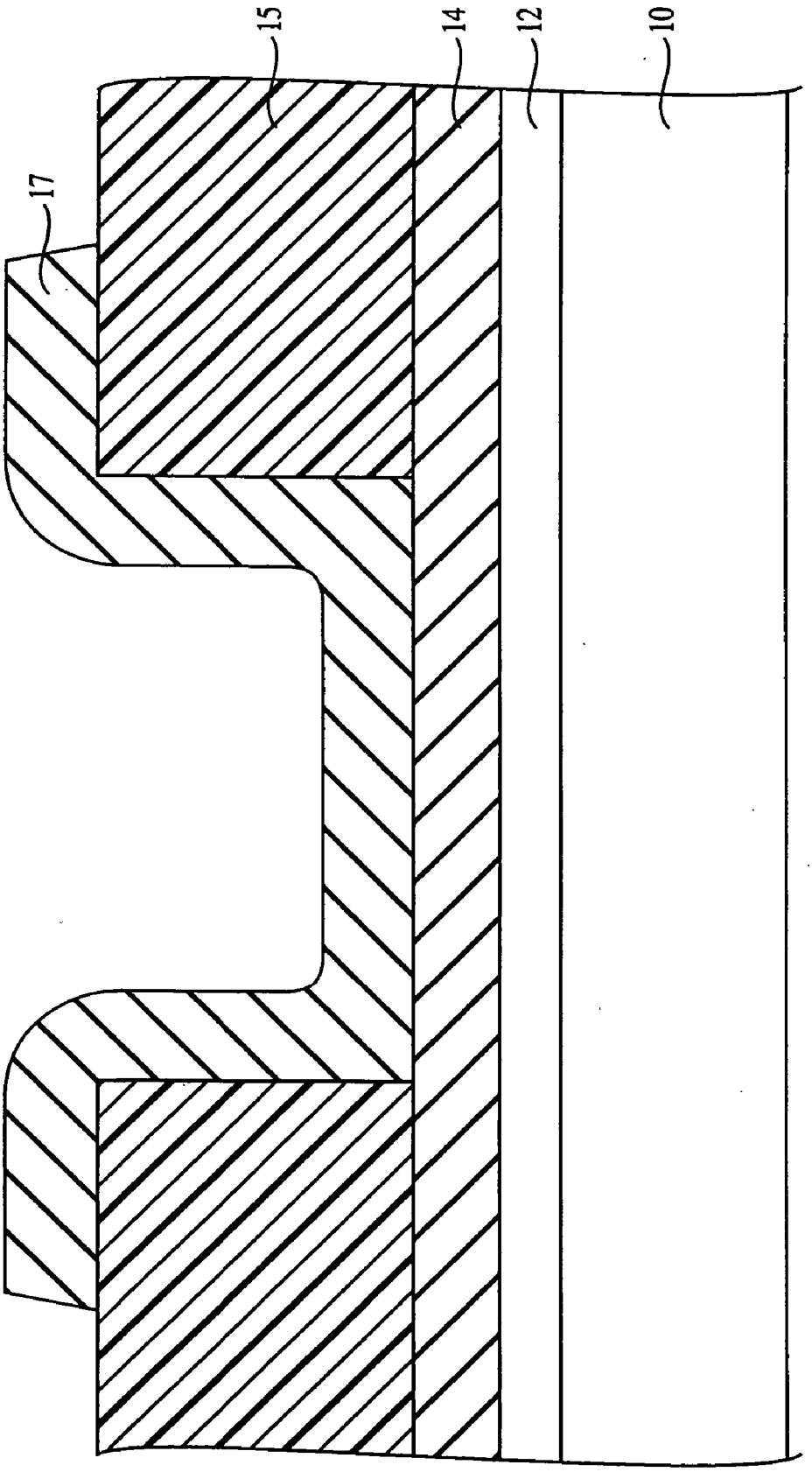


FIG. 3

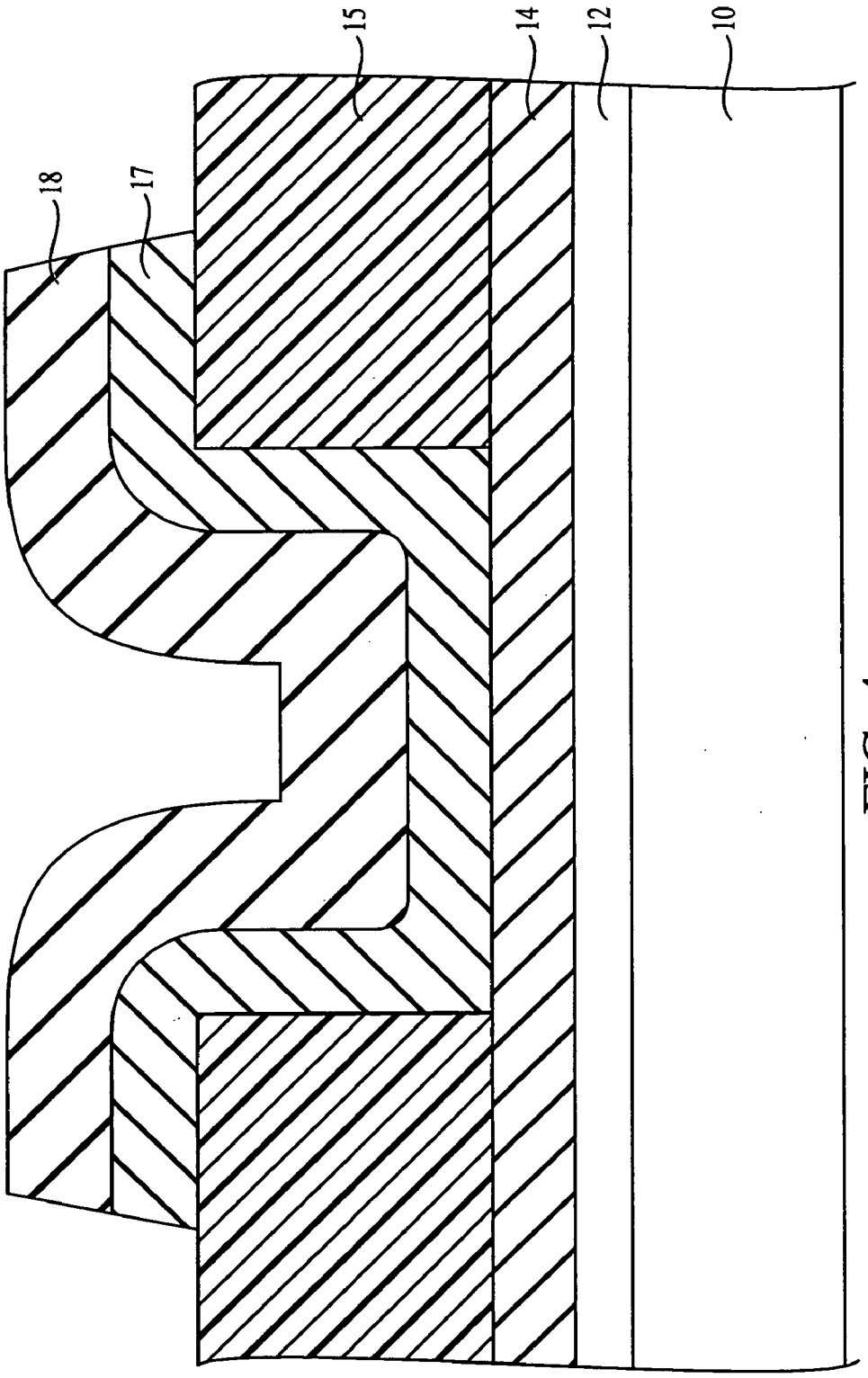


FIG. 4

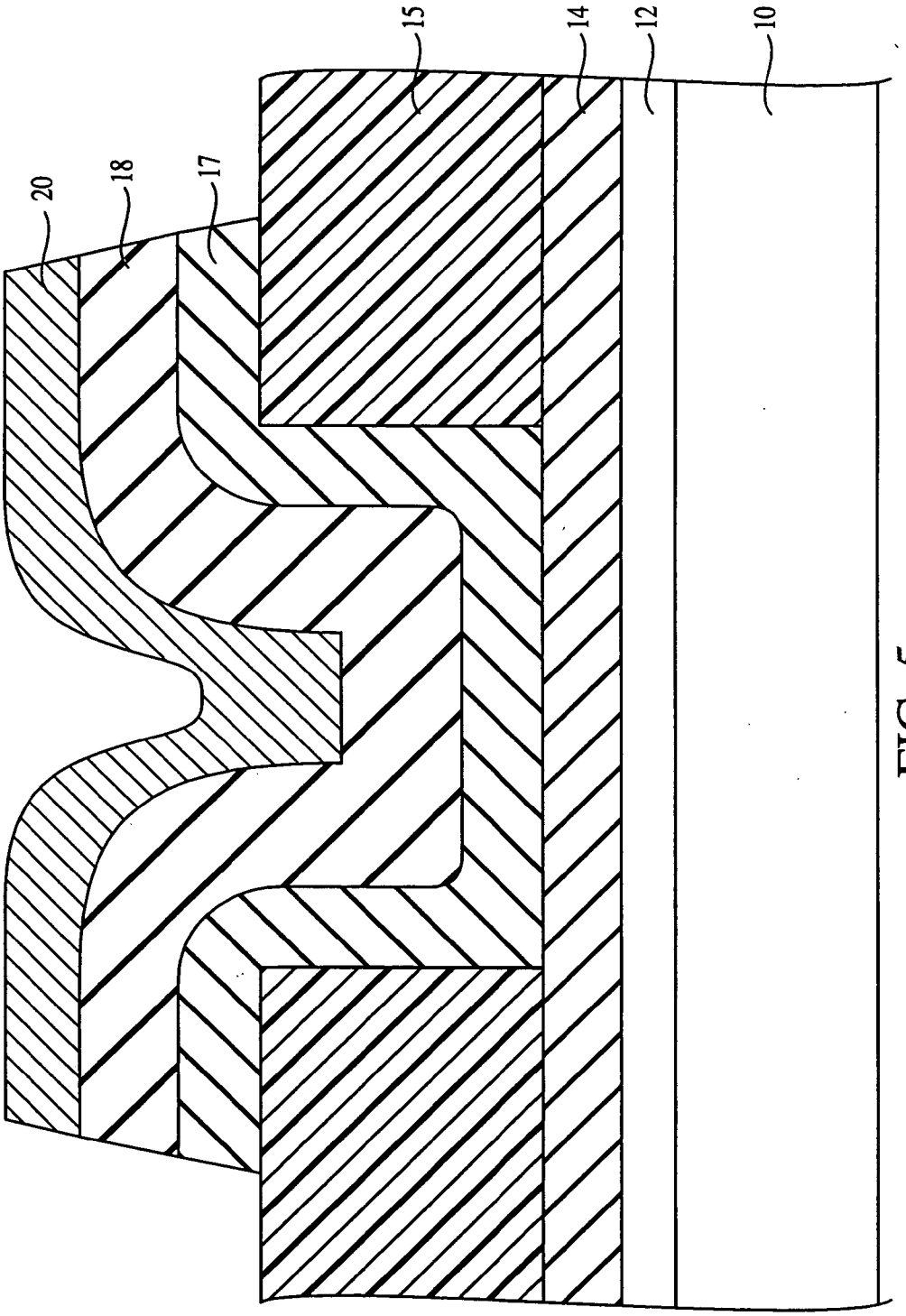


FIG. 5

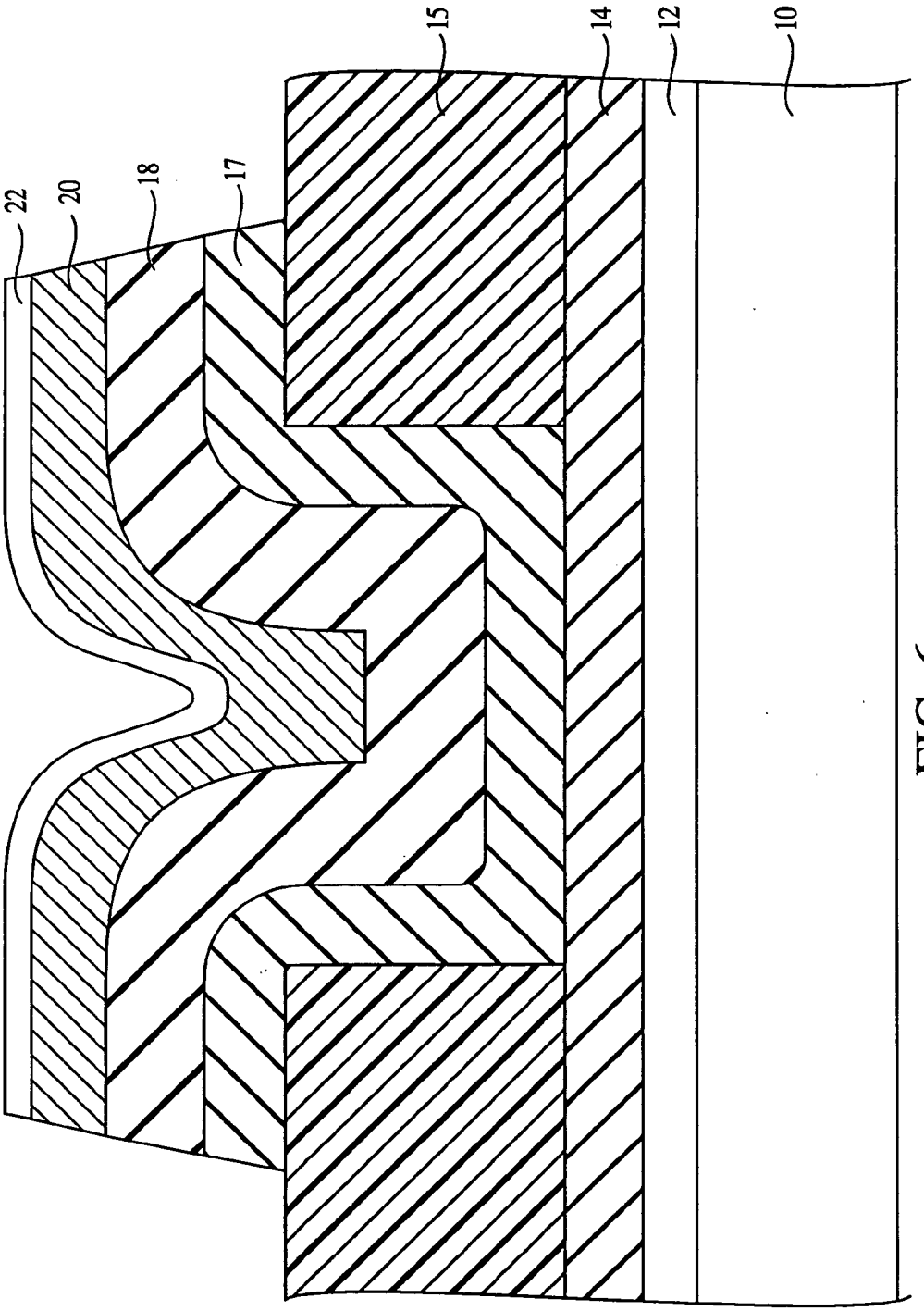


FIG. 6

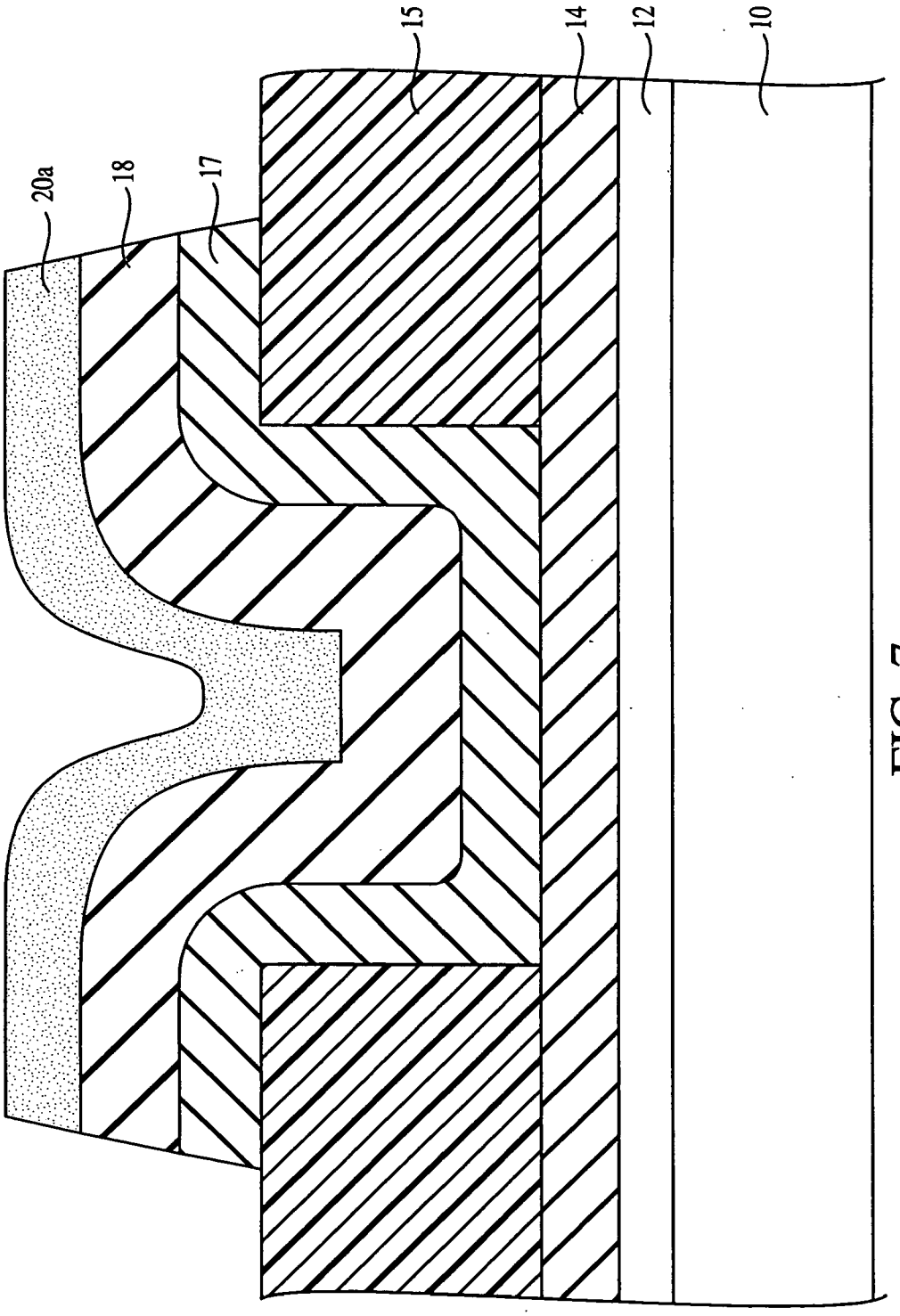


FIG. 7

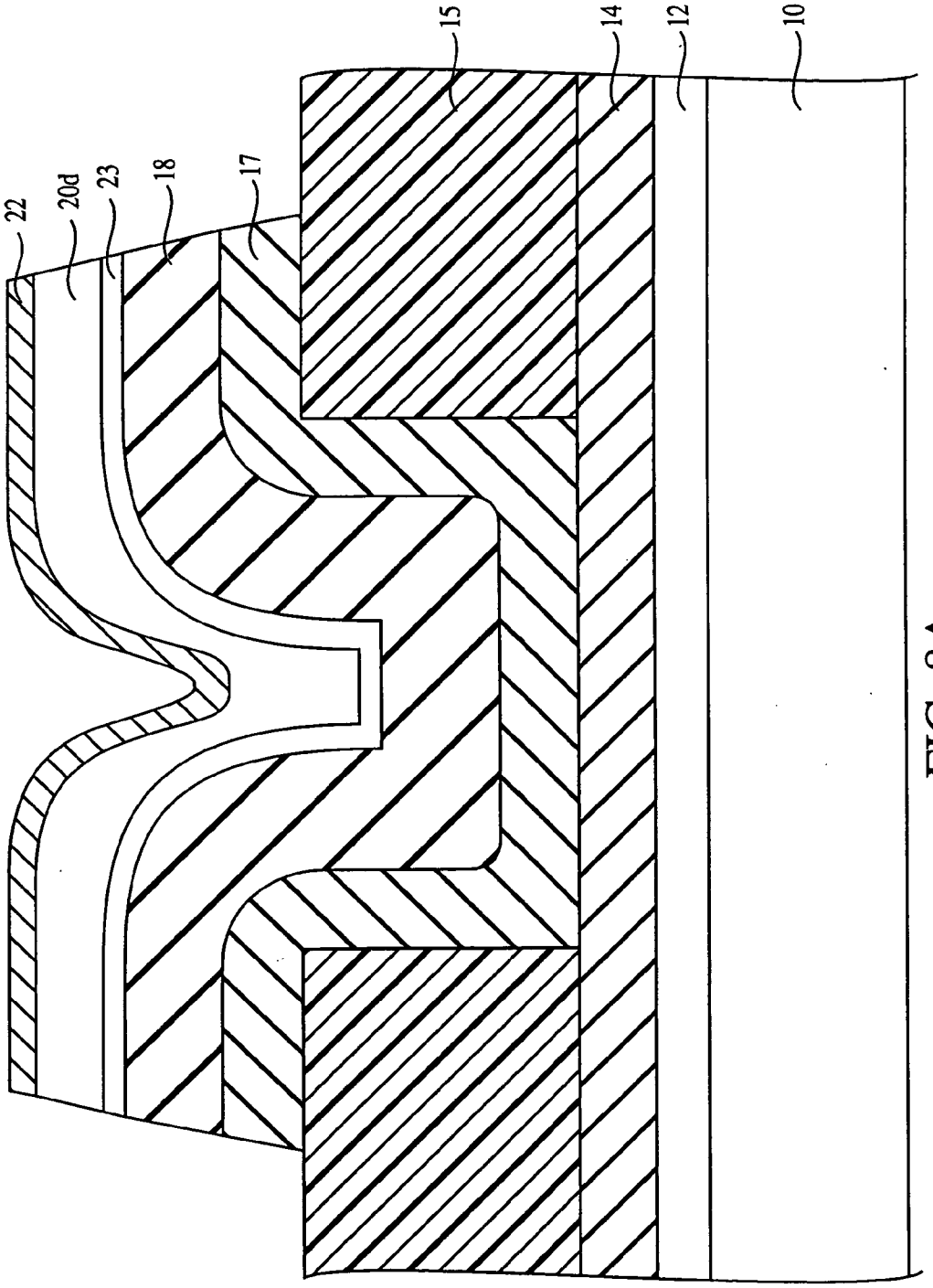


FIG. 8A

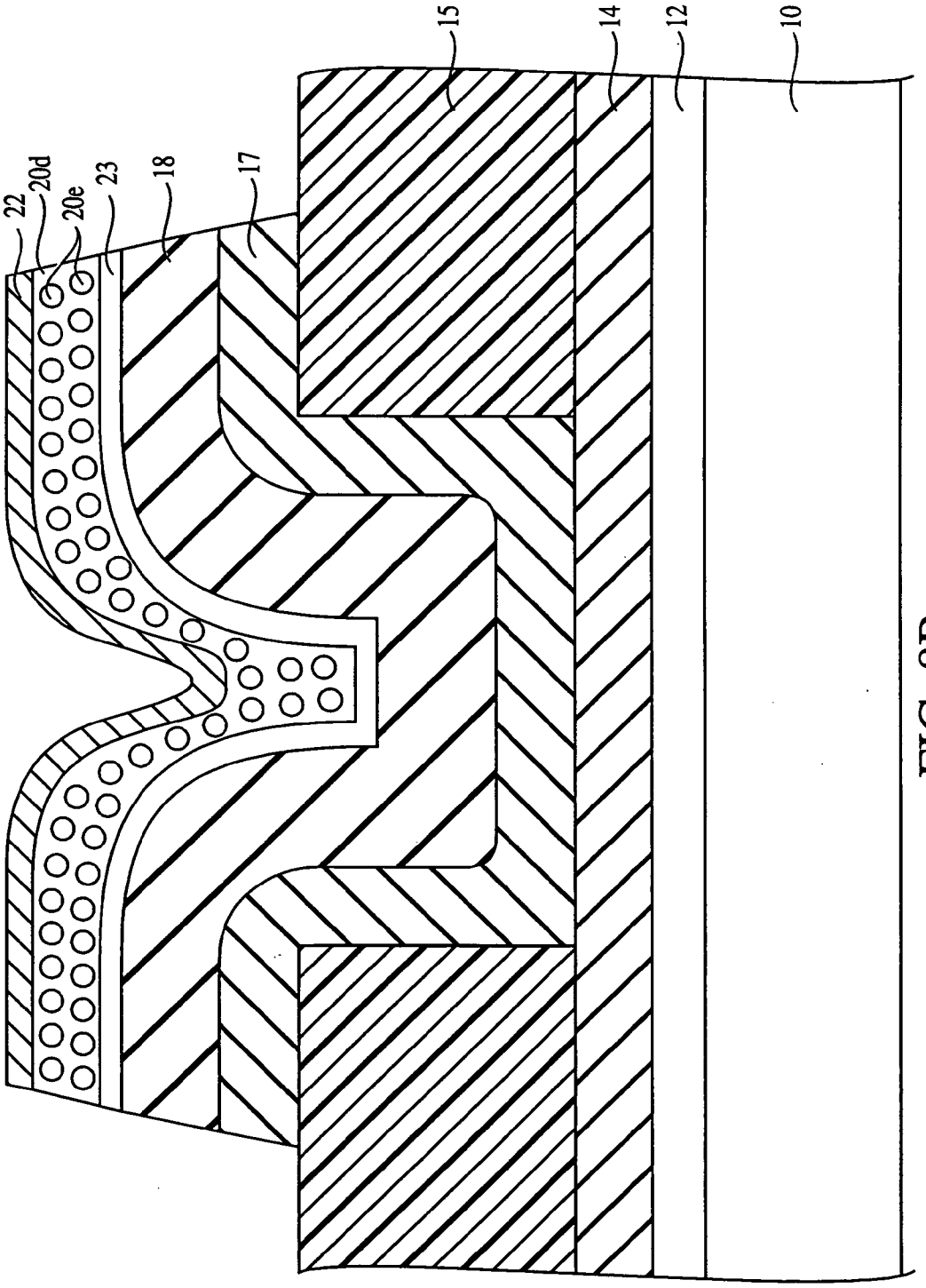


FIG. 8B

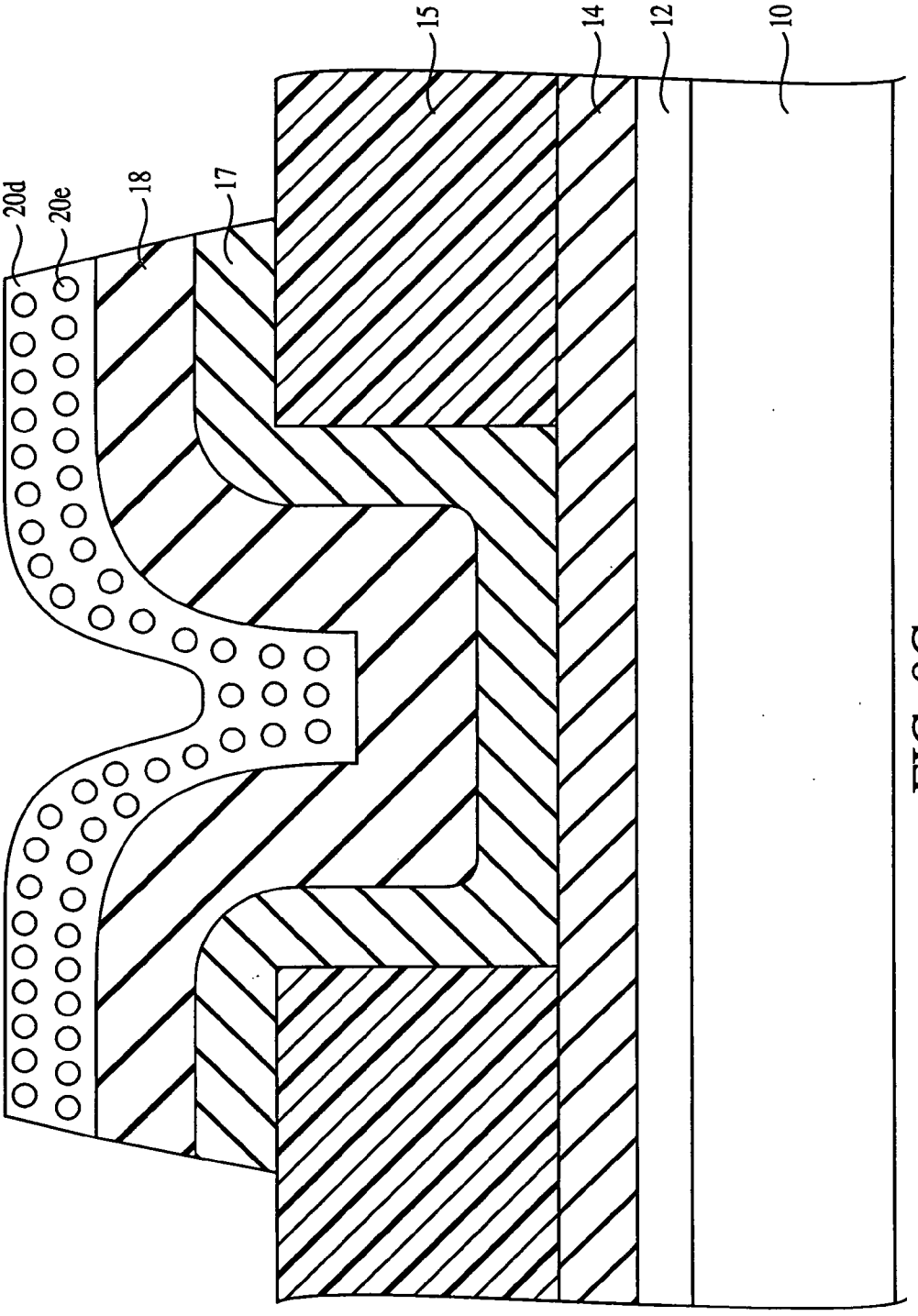


FIG. 8C

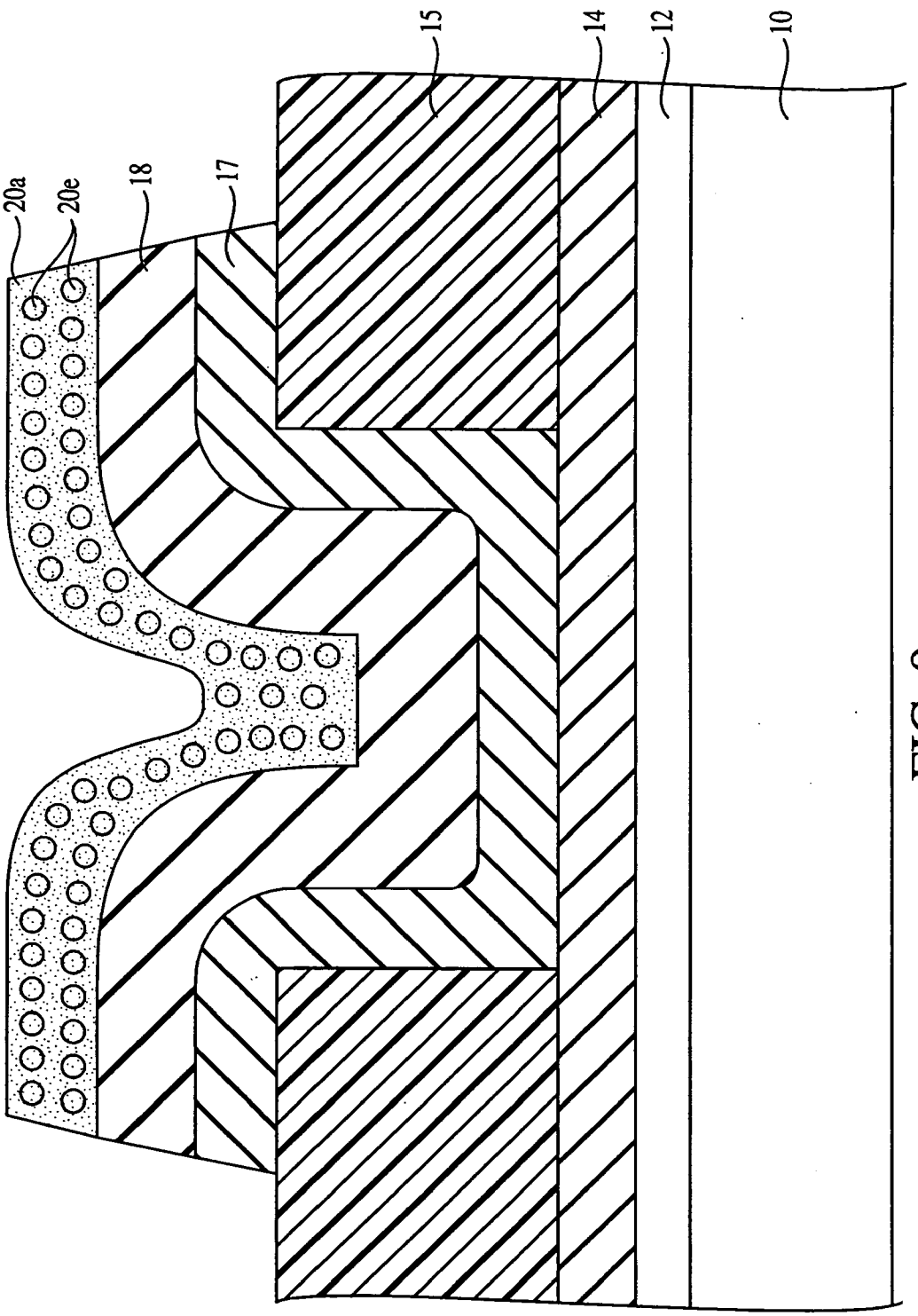


FIG. 9

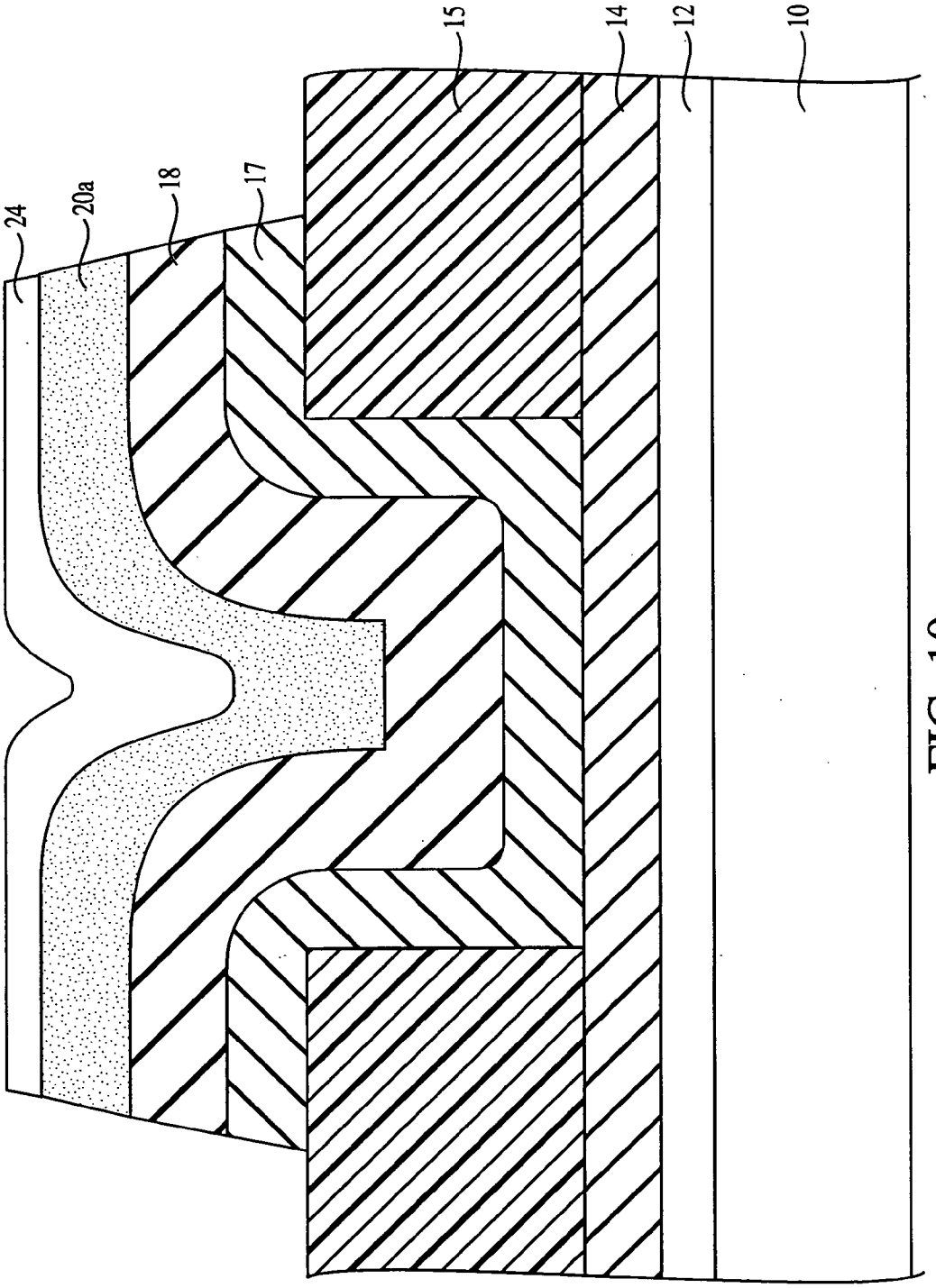


FIG. 10

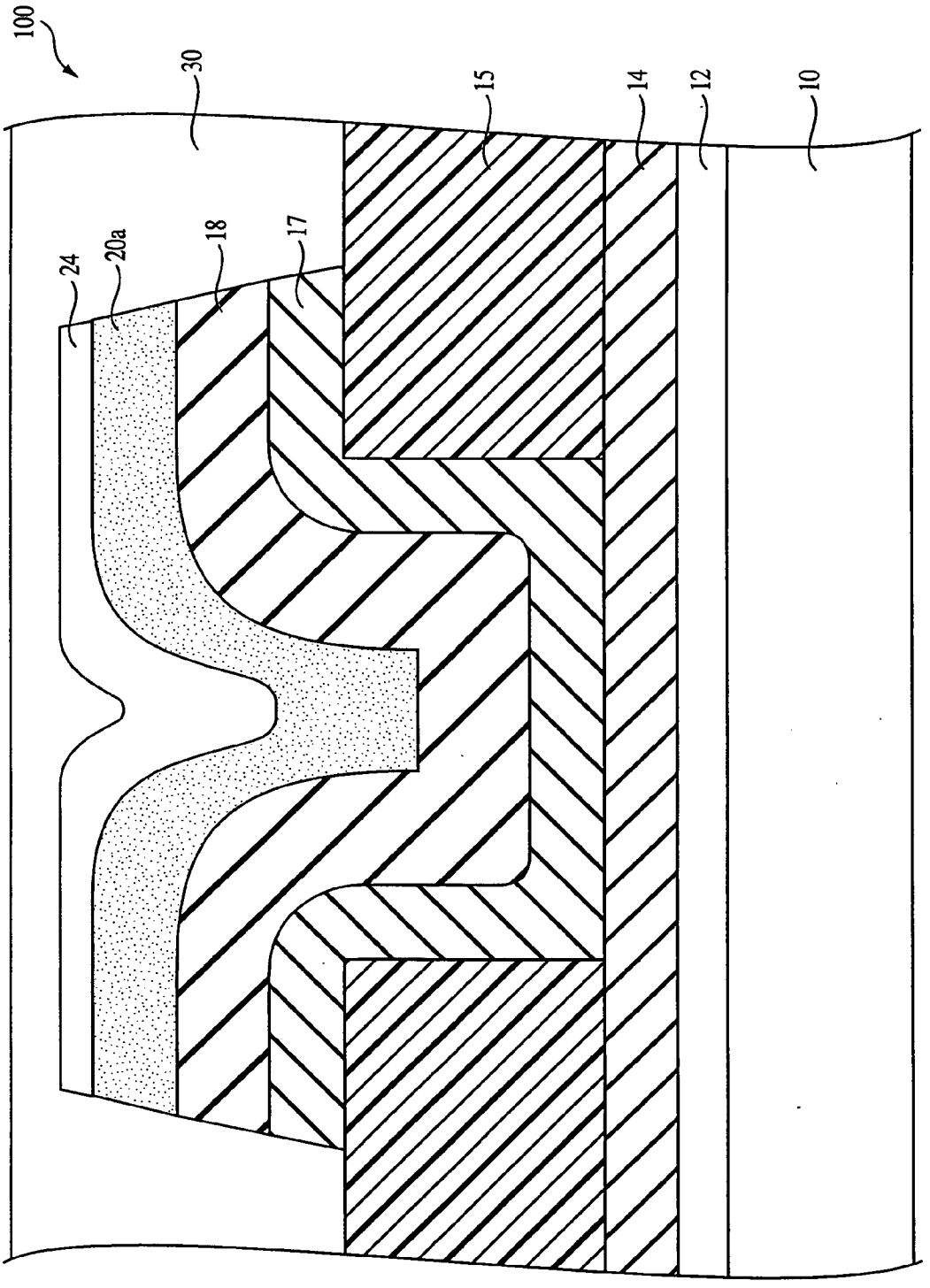
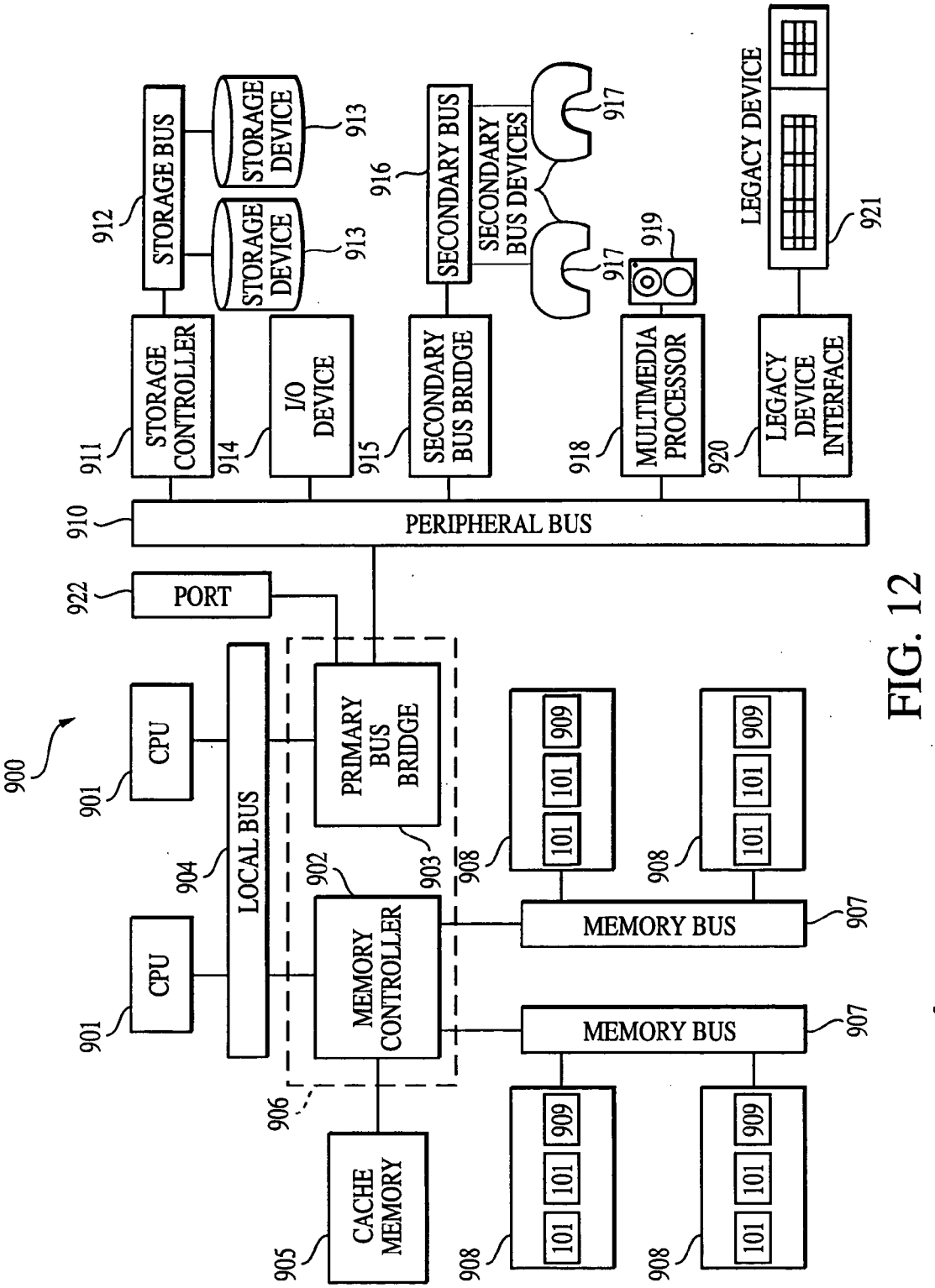


FIG. 11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CPU
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CPU
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LOCAL BUS
904
PRIMARY BUS BRIDGE
903
MEMORY CONTROLLER
902
CACHE MEMORY
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906
PORT
922
PERIPHERAL BUS
910
STORAGE CONTROLLER
911
I/O DEVICE
914
SECONDARY BUS BRIDGE
915
MULTIMEDIA PROCESSOR
918
LEGACY DEVICE INTERFACE
920
STORAGE BUS
912
STORAGE DEVICE
913
STORAGE DEVICE
913
SECONDARY BUS
916
SECONDARY BUS DEVICES
917
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919
LEGACY DEVICE
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MEMORY BUS
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MEMORY BUS
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101

FIG. 12

METHOD AND APPARATUS FOR CONTROLLING METAL DOPING OF A CHALCOGENIDE MEMORY ELEMENT

FIELD OF THE INVENTION

[0001] The invention relates to the field of random access memory (RAM) devices formed using a resistance variable material, and in particular to controlling silver incorporation into a resistance variable memory element formed using chalcogenide glass.

BACKGROUND OF THE INVENTION

[0002] A well known semiconductor memory component is random access memory (RAM). RAM permits repeated read and write operations on memory elements. Typically, RAM devices are volatile, in that stored data is lost once the power source is disconnected or removed. Non-limiting examples of RAM devices include dynamic random access memory (DRAM), synchronized dynamic random access memory (SDRAM) and static random access memory (SRAM). In addition, DRAMS and SDRAMS also typically store data in capacitors which require periodic refreshing to maintain the stored data.

[0003] Recently resistance variable memory elements have been investigated for suitability as semi-volatile and non-volatile random access memory elements. In a resistance variable memory element, a conductive material, such as silver, is incorporated into a dielectric material. The resistance of the conductive material containing dielectric material can be changed between high resistance and low resistance states. The resistance variable memory element is normally in a high resistance state when at rest. A write operation to a low resistance state is performed by applying a voltage potential across the two electrodes.

[0004] One preferred resistance variable material comprises a chalcogenide glass. A specific example is germanium-selenide (Ge_xSe_{100-x}) containing a silver (Ag) component. One method of providing silver to the germanium-selenide composition is to initially form a germanium-selenide glass and then deposit a thin layer of silver upon the glass, for example by sputtering, physical vapor deposition, or other known techniques in the art. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 600 nanometers, so that the energy passes through the silver and to the silver/glass interface, to break a chalcogenide bond of the chalcogenide material such that the glass is doped or photodoped with silver. Another method for providing silver to the glass is to provide a layer of silver-selenide on a germanium-selenide glass. A top electrode comprising silver is then formed over the silver-germanium-selenide glass or in the case where a silver-selenide layer is provided over a germanium-selenide glass, the top electrode is formed over the silver-selenide layer.

[0005] It has been found that over time devices fabricated via the above described methods fail if excess silver from a top silver containing electrode continues to diffuse into the silver germanium-selenide glass or into the silver-selenide layer and eventually into the germanium-selenide glass layer (the primary switching area) below the silver-selenide layer.

[0006] Furthermore, during semiconductor processing and/or packaging of a fabricated structure that incorporates the memory element, the element undergoes thermal cycling or heat processing. Heat processing can result in substantial amounts of silver migrating into the memory element uncontrollably. Too much silver incorporated into the memory element may result in faster degradation, i.e., a short life, and eventually device failure.

[0007] Control of the amount of available silver which enters the glass would be highly desirable to prevent premature memory cell failure.

BRIEF SUMMARY OF THE INVENTION

[0008] The present invention is a method of controlling silver doping of a chalcogenide glass in a resistance variable memory element. The method includes forming a first chalcogenide glass layer; forming a first silver-selenide layer in contact with the first chalcogenide glass layer; forming a second chalcogenide glass layer in contact with the first silver-selenide layer; forming a silver layer in contact with the second chalcogenide glass layer; processing the silver layer and second chalcogenide glass layer to incorporate silver into the second chalcogenide glass layer, thereby forming one or more silver containing layers; and removing any remaining portions of the silver layer. Electrodes are provided in contact with the first chalcogenide layer and the one or more silver containing layers. Forming a resistance variable memory element in accordance with the invention limits the amount of silver available for diffusion into the first glass layer.

[0009] The silver layer and second chalcogenide glass layer may be processed by heat treating, light irradiation or a combination of both heat treating and light irradiation. Heat treating the silver layer will cause silver to be incorporated into the second chalcogenide glass interstitially. Processing the second chalcogenide glass layer with light irradiation will cause the formation of a silver doped chalcogenide glass layer having silver-selenide formed therein. Combining a heat treating process with light irradiation will result in silver-selenide formed in a chalcogenide glass layer having silver interstitially formed in the chalcogenide glass layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] These and other features and advantages of the invention will be better understood from the following detailed description, which is provided in connection with the accompanying drawings.

[0011] **FIG. 1** illustrates a cross-sectional view of a memory element fabricated in accordance with a first embodiment of the invention and at an initial stage of processing.

[0012] **FIG. 2** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 1**.

[0013] **FIG. 3** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 2**.

[0014] **FIG. 4** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 3**.

[0015] **FIG. 5** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 4**.

[0016] **FIG. 6** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 5**.

[0017] **FIG. 7** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 6** in accordance with a first embodiment of the inventor.

[0018] **FIG. 8A** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 6** in accordance with a second embodiment of the inventor.

[0019] **FIG. 8B** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 8A** in accordance with a second embodiment of the inventor.

[0020] **FIG. 8C** illustrates a cross-sectional view of the memory element of **FIG. 1** at a state of processing subsequent to that shown in **FIG. 8B** in accordance with a second embodiment of the inventor.

[0021] **FIG. 9** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 6** in accordance with a third embodiment of the inventor.

[0022] **FIG. 10** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 7**.

[0023] **FIG. 11** illustrates a cross-sectional view of the memory element of **FIG. 1** at a stage of processing subsequent to that shown in **FIG. 10**.

[0024] **FIG. 12** illustrates a processor-based system having a memory element formed according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0025] In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0026] The term "substrate" used in the following description may include any supporting structure including, but not limited to, a plastic or a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0027] The term "silver" is intended to include not only elemental silver, but silver with other trace metals or in various alloyed combinations with other metals as known in the semiconductor industry, as long as such silver alloy is conductive, and as long as the physical and electrical properties of the silver remain unchanged.

[0028] The term "silver-selenide" is intended to include various species of silver-selenide, including some species which have a slight excess or deficit of silver, for instance, Ag_2Se, $Ag_{2+x}Se$, and $Ag_{2-x}Se$.

[0029] The term "chalcogenide glass" is intended to include glasses that comprise an element from group VIA (or group 16) of the periodic table. Group VIA elements, also referred to as chalcogens, include sulfur (S), selenium (Se), tellurium (Te), polonium (Po), and oxygen (O).

[0030] The invention will now be explained with reference to **FIGS. 1-10**, which illustrate exemplary embodiments of a resistance variable memory element **100** fabricated in accordance with the invention. **FIG. 1** depicts a portion of an insulating layer **12** formed over a semiconductor substrate **10**, for example, a silicon substrate. It should be understood that the resistance variable memory element can be formed on a variety of substrate materials and not just semiconductor substrates such as silicon. For example, the insulating layer **12** may be formed on a plastic substrate. The insulating layer **12** may be formed by any known deposition methods, such as sputtering by chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or physical vapor deposition (PVD). The insulating layer **12** may be formed of a conventional insulating oxide, such as silicon oxide (SiO_2), a silicon nitride (Si_3N_4), or a low dielectric constant material, among many others.

[0031] A first electrode **14** is next formed over the insulating layer **12**, as also illustrated in **FIG. 1**. The first electrode **14** may comprise any conductive material, for example, tungsten, nickel, tantalum, aluminum, or platinum, among many others. A first dielectric layer **15** is next formed over the first electrode **14**. The first dielectric layer **15** may comprise the same or different materials as those described above with reference to the insulating layer **12**.

[0032] Referring now to **FIG. 2**, an opening **13** extending to the first electrode **14** is formed in the first dielectric layer **15**. The opening **13** may be formed by known methods in the art, for example, by a conventional patterning and etching process. A first chalcogenide glass layer **17** is next formed over the first dielectric layer **15**, to fill in the opening **13**, as shown in **FIG. 3**.

[0033] The first chalcogenide glass layer **17** is preferably a germanium-selenide glass having a Ge_xSe_{100-x} stoichiometry. The preferred stoichiometric range is between about $Ge_{18}Se_{82}$ to about $Ge_{43}Se_{57}$ and is more preferably about $Ge_{40}Se_{60}$. The first chalcogenide glass layer **17** preferably has a thickness from about 100 Å to about 1000 Å and is more preferably between about 150 Å to about 200 Å.

[0034] The use of a metal containing layer, such as a silver-selenide layer, in contact with the chalcogenide glass layer makes it unnecessary to provide a metal (silver) doped chalcogenide glass, which would require photodoping of the substrate with light radiation.

[0035] The formation of the first chalcogenide glass layer **17**, having a stoichiometric composition in accordance with

the invention may be accomplished by any suitable method. For instance, evaporation, co-sputtering germanium and selenium in the appropriate ratios, sputtering using a germanium-selenide target having the desired stoichiometry, or chemical vapor deposition with stoichiometric amounts of GeH_4 and SeH_2 gases (or various compositions of these gases), which result in a germanium-selenide film of the desired stoichiometry are examples of methods which may be used to form the first chalcogenide glass layer **17**.

[**0036**] Referring now to **FIG. 4**, a first metal containing layer **18**, preferably silver-selenide, is deposited over the first chalcogenide glass layer **17**. Other suitable metal containing layers **18** may include silver-chalcogenide layers, for example, silver sulfide, silver oxide, and silver telluride. A variety of processes can be used to form the metal containing layer **18**. For instance, physical vapor deposition techniques such as evaporative deposition and sputtering may be used. Other processes such as chemical vapor deposition, co-evaporation or depositing a layer of selenium above a layer of silver to form silver-selenide can also be used.

[**0037**] The layers may be any suitable thickness and depends upon the desired electrical switching characteristics. The thickness of the layers is such that the metal containing layer **18** is thicker than the first chalcogenide glass layer **17**. The metal containing layer **18** is also thicker than a second glass layer, described below. The first metal containing layer **18** preferably has a thickness from about 300 Å to about 600 Å.

[**0038**] Referring now to **FIG. 5 a** second chalcogenide glass layer **20** is formed over the first metal containing layer **18**. The second chalcogenide glass layer **20** allows deposition of silver above the metal containing layer **18**, for example, a silver-selenide layer, since silver cannot be directly deposited on silver-selenide.

[**0039**] The second chalcogenide glass layer **20** is preferably a germanium-selenide glass having a Ge_xSe_{100-x} stoichiometry. The preferred stoichiometric range of the second glass layer depends on the type of processing the layer will undergo, i.e., thermal, light irradiation or a combination of thermal and light irradiation. The second chalcogenide glass layer **20** preferably has a thickness between about 150 Å to about 500 Å and is more preferably 200 Å.

[**0040**] The formation of the second chalcogenide glass layer **20** may be accomplished by any suitable method. For instance, chemical vapor deposition, evaporation, co-sputtering, or sputtering using a target having the desired stoichiometry, may be used.

[**0041**] Referring now to **FIG. 6**, a silver layer **22** is formed over the second chalcogenide glass layer **20**. The silver layer is preferably between about 150 Å to about 300 Å thick. The silver layer may be deposited by any suitable mechanism, for instance, physical vapor deposition (PVD) or evaporation. Next the silver layer **22** is thermally treated, irradiated with light, or thermally treated in combination with the irradiation treatment to cause sufficient diffusion of silver into the second chalcogenide glass layer **20**.

[**0042**] Referring now to **FIG. 7**, the silver layer **22** and the second chalcogenide glass layer **20** are thermally treated, preferably by heat annealing in order to form a silver-containing chalcogenide glass layer **20**a wherein silver is incorporated interstitially. The preferred stoichiometric range of the second chalcogenide glass layer **20** for thermal processing is between about $Ge_{18}Se_{82}$ to about $Ge_{43}Se_{57}$ and is more preferably about $Ge_{40}Se_{60}$. A suitable annealing temperature is an elevated temperature close to or slightly below the thin film glass transition temperature of the second chalcogenide glass layer **20**. The annealing temperature may be as low as 50° C. and as high as about 350° C. The preferred annealing temperature depends on the chosen glass stoichiometry. The substrate is preferably annealed for about 5 to about 15 minutes and more preferably about 10 minutes. The annealing preferably takes place in an atmosphere containing oxygen. A wet etch in nitric acid is then performed to remove any remaining portion of silver layer **22**.

[**0043**] Referring now to **FIGS. 8A-8C**, alternatively silver from the silver layer **22** may be incorporated into the second chalcogenide glass layer **20** via irradiation with light. The silver layer **22** is irradiated with light to cause diffusion of silver ions from silver layer **22** into the second chalcogenide glass layer **20** thereby forming a silver doped chalcogenide glass layer **20***d*. For example, when the second chalcogenide glass layer includes germanium-selenide, irradiation further causes the formation of regions of silver-selenide **20***e* in the silver doped chalcogenide glass layer **20***d*. Research in this area is reported in the article "Dual Chemical Role of Ag as an Additive in Chalcogenide Glasses" by Mitkova et al., Physical Review Letters, Vol. 83, No. 19 (1999), pgs. 3848-3851, the disclosure of which is incorporated herein by reference.

[**0044**] The preferred stoichiometric range for light irradiation processing is between about $Ge_{18}Se_{82}$ to about $Ge_{33}Se_{67}$ and is more preferably about $Ge_{25}Se_{75}$. Preferably, about 1% to about 10% less than the maximum amount of silver necessary to keep the glass layer **20** in an amorphous state is diffused into the glass layer. Any residual glass **23** will preferably have a lower stoichiometry than the pre-processing second chalcogenide glass layer **20**. Accordingly, a silver-doped germanium-selenide glass layer having regions of silver-selenide **20***b* incorporated therein, and a layer containing any remaining undoped glass **23** are formed. The silver layer **22** may be irradiated with any suitable light, for example, visible light or ultraviolet light. The silver layer **22** may be irradiated for about 5 to about 15 minutes at about 1 to about 10 mw/cm^2 with light between 200-600 nm. Any remaining silver layer is then removed, for example, via wet etching in nitric acid.

[**0045**] Not to be held to any particular theory, it is believed that as the silver layer **22** and second chalcogenide glass layer **20** are irradiated with light over time there is an initial doping of silver into the second chalcogenide glass layer **20** forming a structure having a silver doped chalcogenide glass layer **20**d formed between the silver layer **22** and any remaining undoped second chalcogenide glass layer **23** as shown in **FIG. 8A**. With further irradiation, regions of silver-chalcogenide, for example, silver-selenide, **20***e* are formed in the silver doped chalcogenide glass layer **20***d* as show in **FIG. 8B**. For purposes of simplified discussion, silver-chalcogenide **20***e* will be further described herein as silver-selenide. However, it should be understood that other silver-chalcogenides could also be used. Ideally with further irradiation, the silver layer **22** will be completely diffused into the silver doped chalcogenide glass layer **20***d* leaving no undoped remaining GeSe glass and forming a silver doped

chalcogenide glass layer **20***d* having regions of silver-selenide **20***e* formed therein as shown in **FIG. 8C**.

[**0046**] Referring now to **FIG. 9**, alternatively silver from layer **22** may be incorporated into the glass layer **20** by light irradiation as described above in combination with the thermal treatment described above. Preferably thermal treating would be done first to saturate a portion of the glass layer **20** with silver to form a silver containing germanium-selenide glass layer **20***a* wherein silver is incorporated interstitially. Then the substrate would be irradiated to form regions of silver-selenide **20***e* within the glass layer having silver incorporated interstitially therein **20***a*. However, although it is preferred that the silver be driven into the glass by thermal processing first then light irradiation, it is to be understood that the process may be reversed, in that silver may be driven into the glass by light irradiation first then thermal processing can be applied. Alternatively, light irradiation and thermal processing may be performed simultaneously. Combining a light irradiation process with a thermal process to process silver into the glass layer provides an interstitially formed silver containing glass layer **20***a* having silver-selenide regions **20***e* formed therein. Any remaining silver from layer **22** is then removed, for example, using wet etching in nitric acid. The preferred stoichiometric range for a combination of light irradiation and thermal processing is between about $Ge_{18}Se_{82}$ to about $Ge_{33}Se_{67}$ and is more preferably about $Ge_{25}Se_{75}$.

[**0047**] Referring now to **FIG. 10**, a second conductive electrode material **24** is formed over the resulting silver containing chalcogenide glass layer **20***a* (**FIG. 7**) or **20***d*/**20***e* (**FIG. 8C**) or **20***a*/**20***e* (**FIG. 9**). For example, if a thermal treatment is used, the second conductive electrode **24** is formed over the resulting interstially formed silver containing chalcogenide glass layer **20***a*, if light irradiation is used, the second conductive electrode **24** is formed over the silver doped chalcogenide glass layer **20***d* having silver-selenide regions **20***e* formed therein, or if a combination of thermal treatment and light irradiation is used, the second conductive electrode **24** is formed over the resulting interstitially formed silver containing glass layer **20***a* having silver-selenide regions **20***e* formed therein. The second conductive electrode material **22** may comprise any electrically conductive material, for example, tungsten, tantalum or titanium, among many others, but does not contain silver.

[**0048**] Referring now to **FIG. 11**, one or more additional dielectric layers **30** may be formed over the second electrode **24** and the first dielectric layer **15** to isolate the resistance variable memory element **100** from other structure fabrication over the substrate **10**. Conventional processing steps can then be carried out to electrically couple the first and second electrodes **14**, **24** to various circuits of memory arrays.

[**0049**] Devices fabricated in accordance with the invention, limit the amount of silver available to migrate into the first chalcogenide glass layer **17** by removing any remaining silver layer **22** and by using a second electrode that does not contain silver.

[**0050**] The resistance variable memory element **100** of the invention may be used in a random access memory device. **FIG. 12** illustrates an exemplary processing system **900** which utilizes a resistance variable memory random access device **101** containing an array of resistance variable memory elements constructed as described above with reference to **FIGS. 1-11**. The processing system **900** includes one or more processors **901** coupled to a local bus **904**. A memory controller **902** and a primary bus bridge **903** are also coupled the local bus **904**. The processing system **900** may include multiple memory controllers **902** and/or multiple primary bus bridges **903**. The memory controller **902** and the primary bus bridge **903** may be integrated as a single device **906**.

[**0051**] The memory controller **902** is also coupled to one or more memory buses **907**. Each memory bus accepts memory components **908**, which include at least one memory device **101** of the invention. Alternatively, in a simplified system, the memory controller **902** may be omitted and the memory components directly coupled to one or more processors **901**. The memory components **908** may be a memory card or a memory module. The memory components **908** may include one or more additional devices **909**. For example, the additional device **909** might be a configuration memory. The memory controller **902** may also be coupled to a cache memory **905**. The cache memory **905** may be the only cache memory in the processing system. Alternatively, other devices, for example, processors **901** may also include cache memories, which may form a cache hierarchy with cache memory **905**. If the processing system **900** include peripherals or controllers which are bus masters or which support direct memory access (DMA), the memory controller **902** may implement a cache coherency protocol. If the memory controller **902** is coupled to a plurality of memory buses **907**, each memory bus **907** may be operated in parallel, or different address ranges may be mapped to different memory buses **907**.

[**0052**] The primary bus bridge **903** is coupled to at least one peripheral bus **910**. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus **910**. These devices may include a storage controller **911**, an miscellaneous I/O device **914**, a secondary bus bridge **915**, a multimedia processor **918**, and an legacy device interface **920**. The primary bus bridge **903** may also coupled to one or more special purpose high speed ports **922**. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system **900**.

[**0053**] The storage controller **911** couples one or more storage devices **913**, via a storage bus **912**, to the peripheral bus **910**. For example, the storage controller **911** may be a SCSI controller and storage devices **913** may be SCSI discs. The I/O device **914** may be any sort of peripheral. For example, the I/O device **914** may be an local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be an universal serial port (USB) controller used to couple USB devices **917** via to the processing system **900**. The multimedia processor **918** may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one additional devices such as speakers **919**. The legacy device interface **920** is used to couple legacy devices, for example, older styled keyboards and mice, to the processing system **900**.

[0054] The processing system **900** illustrated in **FIG. 12** is only an exemplary processing system with which the invention may be used. While **FIG. 12** illustrates a processing architecture especially suitable for a general purpose computer, such as a personal computer or a workstation, it should be recognized that well known modifications can be made to configure the processing system **900** to become more suitable for use in a variety of applications. For example, many electronic devices which require processing may be implemented using a simpler architecture which relies on a CPU **901** coupled to memory components **908** and/or memory elements **100**. These electronic devices may include, but are not limited to audio/video processors and recorders, gaming consoles, digital television sets, wired or wireless telephones, navigation devices (including system based on the global positioning system (GPS) and/or inertial navigation), and digital cameras and/or recorders. The modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.

[0055] The invention is not limited to the details of the illustrated embodiment. Accordingly, the above description and drawings are only to be considered illustrative of exemplary embodiments which achieve the features and advantages of the invention. Modifications and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

1-53. (Cancelled).

54. A resistance variable memory element comprising:

a first chalcogenide glass layer;

a first metal-chalcogenide layer overlying and in electrical communication with said first chalcogenide glass layer, said first metal-chalcogenide layer represented by M_xC, wherein M is a metal, C is a chalcogenide chemical element, and x is about 2; and

a metal containing chalcogenide glass layer overlying and in electrical communication with said first metal-chalcogenide layer.

55. The element of claim 54 wherein said metal containing chalcogenide glass layer has metal incorporated interstitially therein.

56. The element of claim 54 wherein said metal containing chalcogenide glass layer comprises silver-selenide formed in a chalcogenide glass layer having silver incorporated interstitially therein.

57. The element of claim 56 wherein said metal containing chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein x is between about 18 to about 43.

58. The element of claim 57 wherein said metal containing chalcogenide glass layer has a stoichiometry of about $Ge_{40}Se_{60}$.

59. The element of claim 54 wherein said metal containing chalcogenide glass layer comprises a metal doped chalcogenide glass layer having silver-selenide incorporated therein.

60. The element of claim 59 wherein said metal containing chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein x is between about 18 to about 33.

61. The element of claim 60 wherein said metal containing chalcogenide glass layer has a stoichiometry of about $Ge_{25}Se_{75}$.

62. The element of claim 54 wherein said metal comprises silver.

63. The element of claim 54 wherein said first chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein x is between about 18 to about 43.

64. The element of claim 63 wherein said first chalcogenide glass layer has a stoichiometry of about $Ge_{40}Se_{60}$.

65. The element of claim 54 wherein said first metal-chalcogenide layer comprises silver-selenide.

66. The element of claim 54 wherein said first chalcogenide glass layer has a thickness of from about 100 Å to about 400 Å.

67. The element of claim 54 wherein said first metal-chalcogenide layer has a thickness from about 300 Å to about 600 Å.

68. The element of claim 54 wherein said second chalcogenide glass layer has a thickness of from about 150 Å to about 500 Å.

69. The element of claim 54 wherein said metal containing chalcogenide glass layer comprises metal-selenide.

70. The element of claim 69 wherein said metal containing chalcogenide glass layer comprises silver-selenide.

71. The element of claim 54 wherein said metal containing chalcogenide glass layer comprises metal-germanium-selenide.

72. The element of claim 71 wherein said metal containing chalcogenide glass layer comprises silver-germanium-selenide.

73. A resistance variable memory element comprising:

a first electrode;

a first germanium-selenide glass layer overlying and in electrical communication with said first electrode;

a first silver-selenide layer overlying and in electrical communication with said first germanium-selenide glass layer;

a silver containing chalcogenide glass layer overlying and in electrical communication with said first silver-selenide layer; and

a second electrode overlying and in electrical communication with said silver containing chalcogenide glass layer.

74. The element of claim 73 wherein said second electrode does not comprise silver.

75. The element of claim 73 wherein said silver containing chalcogenide glass layer comprises a chalcogenide glass layer having silver formed interstitially therein.

76. The element of claim 75 wherein said silver containing chalcogenide glass layer comprises a germanium-selenide glass layer having silver formed interstitially therein.

77. The element of claim 73 wherein said silver containing chalcogenide glass layer comprises silver-selenide formed in a chalcogenide glass layer having silver formed interstitially therein.

78. The element of claim 76 wherein said silver containing chalcogenide glass layer comprises silver-selenide formed in a germanium-selenide glass layer having silver formed interstitially therein.

79. The element of claim 73 wherein said silver containing chalcogenide glass layer comprises a silver doped chalcogenide glass layer having silver-selenide incorporated therein.

80. The element of claim 78 wherein said silver containing chalcogenide glass layer comprises a silver doped germanium-selenide glass layer having silver-selenide incorporated therein.

81. The element of claim 73 wherein said first germanium-selenide glass layer has a stoichiometry of between about $Ge_{18}Se_{82}$ to about $Ge_{43}Se_{57}$.

82. The element of claim 81 wherein said first germanium-selenide glass layer has a stoichiometry of about $Ge_{40}Se_{60}$.

83. The element of claim 73 wherein said first germanium-selenide glass layer has a thickness of from about 100 Å to about 400 Å.

84. The element of claim 83 wherein said first germanium-selenide glass layer has a thickness of from about 150 Å to about 200 Å.

85. The element of claim 73 wherein said first silver-selenide layer has a thickness of from about 300 Å to about 600 Å.

86. The element of claim 78 wherein said second germanium-selenide glass layer has a stoichiometry of between about $Ge_{18}Se_{82}$ to about $Ge_{43}Se_{57}$.

87. The element of claim 86 wherein second germanium-selenide glass layer has a stoichiometry of about $Ge_{40}Se_{60}$.

88. The element of claim 63 wherein said second germanium-selenide glass layer has a thickness of from about 150 Å to about 500 Å.

89. The element of claim 78 wherein said second germanium-selenide glass layer has a thickness about 200 Å.

90. The element of claim 80 wherein said silver containing chalcogenide glass layer has a germanium-selenide stoichiometry of about $Ge_{18}Se_{82}$ to about $Ge_{33}Se_{67}$.

91. The element of claim 90 wherein said silver containing chalcogenide glass layer has a stoichiometry of about $Ge_{25}Se_{75}$.

92. A processor-based system, comprising:

a processor; and

a memory circuit connected to said processor, said memory circuit including a resistance variable memory element comprising:

a first chalcogenide glass layer;

a first metal-chalcogenide layer overlying and in electrical communication with said first chalcogenide glass layer said first metal-chalcogenide layer represented by M_xC, wherein M is a metal, C is a chalcogenide chemical element, and x is about 2; and

a metal containing chalcogenide glass layer overlying and in electrical communication with said first metal-chalcogenide layer.

93. The system of claim 92 wherein said metal containing chalcogenide glass layer has metal incorporated interstitially therein.

94. The system of claim 92 wherein said metal containing chalcogenide glass layer comprises silver-selenide layer formed in a germanium-selenide layer having silver incorporated interstitially therein.

95. The system of claim 92 wherein said metal containing chalcogenide glass layer comprises a silver doped germanium-selenide layer having silver-selenide incorporated therein.

96. The system of claim 92 wherein said metal comprises silver.

97. The system of claim 92 wherein said first chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein x is between about 18 to about 43.

98. The system of claim 97 wherein said first chalcogenide glass layer has a stoichiometry of about $Ge_{40}Se_{60}$.

99. The system of claim 92 wherein said first metal-chalcogenide layer comprises silver-selenide.

100. The system of claim 92 wherein said first chalcogenide glass layer has a thickness of from about 100 Å to about 400 Å.

101. The system of claim 92 wherein said first metal-chalcogenide layer has a thickness from about 300 Å to about 600 Å.

102. The system of claim 92 wherein said second chalcogenide glass layer has a thickness of from about 150 Å to about 500 Å.

103. The system of claim 92 wherein said metal containing chalcogenide glass layer comprises metal-selenide.

104. The system of claim 103 wherein said metal containing chalcogenide glass layer comprises silver-selenide.

105. The system of claim 92 wherein said metal containing chalcogenide glass layer comprises a metal-germanium-selenide layer.

106. The system of claim 105 wherein said metal containing chalcogenide glass layer comprises a silver-germanium-selenide layer.

107. The system of claim 92 wherein said metal containing chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein x is between about 18 to about 33.

108. The system of claim 107 wherein said metal containing chalcogenide glass layer has a stoichiometry of about $Ge_{25}Se_{75}$.

109. The system of claim 92 wherein said metal containing chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein x is between about 18 to about 43.

110. The system of claim 109 wherein said metal containing chalcogenide glass layer has a stoichiometry of about $Ge_{40}Se_{60}$.

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