FORM 1

REGULATION 9 (1)

611919

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

APPLICATION FOR A STANDARD PATENT

We, HEWLETT-PACKARD COMPANY, a Company incorporated under the laws of the State of California, United States of America, of 3000 Hanover Street, Palo Alto, in the State of California, aforesaid, hereby apply for the grant of a Standard Patent for an invention entitled:-

"APPARATUS AND METHOD FOR TRACKING AND IDENTIFYING PRINTED CIRCUIT ASSEMBLIES"

which is described in the accompanying Complete Specification.

Details of basic application:-

Number: 098,595

Country: United States of America

Date: 17th September, 1987

Our address for service is:- SHELSTON WATERS,
55 Clarence Street,
SYDNEY. N.S.W. 2000

DATED this 30th day of June, 1988

HEWLETT-PACKARD COMPANY

by

Fellow Institute of Patent Attorneys of Australia
of SHELSTON WATERS

To: The Commissioner of Patents,
WODEN. A.C.T. 2606

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CONVENTION APPLICATION BY A COMPANY

FORM 8 – REGULATION 12 (2)

AUSTRALIA
PATENTS ACT 1952

DECLARATION IN SUPPORT OF A CONVENTION APPLICATION FOR A PATENT

In support of the Convention Application made by

(a) Here insert (in full) Name of Company.

(a) HEWLETT-PACKARD COMPANY

(hereinafter referred to as "Applicant") for a patent for an invention entitled:

(b) Here insert Title of Invention.

(b) "APPARATUS AND METHOD FOR TRACKING AND IDENTIFYING PRINTED CIRCUIT ASSEMBLIES"

(c) and (d) Here insert Full Name and Address of Company Official authorised to make declaration.

I, (c) D. Craig Nordlund

of (d) 3000 Hanover Street, Palo Alto, California 94304, U.S.A.

do solemnly and sincerely declare as follows:

1. I am authorised by Applicant to make this declaration on its behalf.

2. The basic Application(s) as defined by section 141 of the Act was ~~were~~ made

(e) Here insert Basic Country followed by date of Basic Application.

(f) Here insert Full Name(s) of Applicant(s) in Basic Country.

in (e) U.S.A. on the 17th day of September, 19 87

by (f) DONALD L. ROGERS

in ..... on the ..... day of 19

by .....

in ..... on the ..... day of 19

by .....

in ..... on the ..... day of 19

by .....

(g) Here insert (in full) Name and Address of actual Inventor or Inventors.

3. (g) DONALD L. ROGERS, of 564 Edelweiss Drive, San Jose, California 95136, U.S.A.

is/~~are~~ the actual Inventor(s) of the invention and the facts upon which Applicant is entitled to make the Application are as follows:

See reverse side of this form for guidance in completing this part.

Applicant is the Assignee of the said Inventor.

4. The basic Application(s) referred to in paragraph 2 of this Declaration was/~~were~~ the first Application(s) made in a Convention country in respect of the invention, the subject of the Application.

DECLARED at Palo Alto, California, U.S.A.

this 5th day of October 19 88

(h) Personal Signature Declarant (c) (no seal, ness or legalisation).

(h) D. Craig Nordlund
(Signature of Declarant)
Associate General Counsel

To THE COMMISSIONER OF PATENTS

(12) PATENT ABRIDGMENT (11) Document No. AU-B-18575/88
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 611919

(54) Title
APPARATUS AND METHOD FOR TRACKING AND IDENTIFYING PRINTED CIRCUIT ASSEMBLIES

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(71) Applicant(s)
HEWLETT-PACKARD COMPANY

(72) Inventor(s)
DONALD L. ROGERS

(74) Attorney or Agent
SHELSTON WATERS , 55 Clarence Street, SYDNEY NSW 2000

(57) Claim

1. In a computer system which includes a plurality of printed circuit assemblies, an apparatus for allowing the electronic storage and retrieving of information about each printed circuit assembly, the apparatus comprising:

memory means within each printed circuit assembly for storing information about that printed circuit assembly; and

retrieval and storage means, including a bus coupled to each printed circuit assembly, for electronically retrieving the information from each printed circuit assembly and making the information available to a user, and for enabling a user to electronically change the information.

7. A method for making information about printed circuit assemblies readily accessible to users, the method comprising the steps of:

(a) providing a memory within each printed circuit assembly for storing information about the printed circuit assembly, including information about the current revision

.../2

level of the printer assembly;

(b) storing information within a memory within a particular printed circuit assembly information pertaining to the particular printed circuit assembly;

(c) accessing the information within the memories electronically through a bus; and

(d) changing the information within the memories electronically through a bus.

611919

COMMONWEALTH OF AUSTRALIA

FORM 10

PATENTS ACT 1952

COMPLETE SPECIFICATION

FOR OFFICE USE:

Class Int.Class

Application Number:
Lodged:

Complete Specification Lodged:
Accepted:
Published:

Priority:

Related Art:

Name of Applicant: HEWLETT-PACKARD COMPANY

Address of Applicant: 3000 Hanover Street, Palo Alto, California 94304, United States of America

Actual Inventor: DONALD LEE ROGERS

Address for Service: SHELSTON WATERS, 55 Clarence Street, Sydney

Complete Specification for the Invention entitled:

"APPARATUS AND METHOD FOR TRACKING AND IDENTIFYING PRINTED CIRCUIT ASSEMBLIES"

The following statement is a full description of this invention, including the best method of performing it known to me/us:-

APPARATUS AND METHOD FOR TRACKING AND IDENTIFYING PRINTED CIRCUIT ASSEMBLIES

Background

In large computer systems, numerous printed circuit assemblies (PCA) are connected together at a computer backplane. Each PCA may be individually modified and updated. This modification is typically not discernable from the appearance of the PCA. Therefore, information is often placed on a label on the PCA.

Often the modification or update of one PCA in a computer system may require modification of one or more PCAs in the computer system in order for the computer system to function properly. Therefore, in order to update one PCA it may be necessary to examine several PCAs in order to determine versions of which PCAs are extant in the system. This can be extremely time consuming and inconvenient.

Additional problems arise when PCAs are remotely updated. That is, updating certain PCAs may not require the exchanging of hardware but only the replacing of software. The replacement software may be transferred through telephone lines and installed in a PCA without a service representative being required to visit the cite of the computing system. In this case, however, the service representative would be unable to read the labels on other PCAs within the computing system. Further, he would be unable to relabel the updated PCA.

Summary of the Invention

In accordance with the preferred embodiment of the present invention, a method and apparatus for tracking and identifying printed circuit assemblies is presented. Within each printed circuit assembly is a non-volatile random access memory (RAM). Within each RAM is stored information about the printed circuit assembly, including the current revision level of the assembly. This

information may be accessed by a user through a dedicated bus and hardware designed for this task. Additionally, through the dedicated bus and hardware, the user may update the information within the printed circuit assembly.

Brief Description of the Drawings

Figure 1 shows a block diagram of various printed circuit assemblies coupled to each other through a bus in accordance with a preferred embodiment of the present invention.

Figure 2 shows how certain of the printed circuit assemblies in Figure 2 may be arranged in slots in a cabinet.

Figure 3 shows an embodiment of an interface which exists in each printed circuit assembly shown in Figure 1, which is used to access the bus also shown in Figure 1.

Figure 4 and Figure 5 show various timing diagrams describing data flow to and from the interface shown in Figure 3.

Figure 6 is a block diagram of processor development hardware in accordance with the preferred embodiment of the present invention.

Description of the Preferred Embodiment

Figure 1 shows a bus 100. Bus 100 is wholly dedicated to transfer information describing printed circuit assemblies (PCA). Shown coupled to bus 100 are the following PCAs: a bus converter 101, a bus converter 102, a memory controller 103, a memory controller 104, a memory array 105 and a memory array 106 which are representative of sixteen memory arrays, a processor 122, a processor 123, a processor 124, a processor 125, a power system monitor 126, processor development hardware (PDH) 127 and a clock 128.

Typically the PCAs shown in Figure 1 will be mounted in a computer cabinet. Figure 2 shows how processor 122, processor 123, processor 124,

processor 125, power system monitor 126, PDH 127, bus converter 101, bus converter 102 and memory controller 103 might be placed within slots in a computer cabinet 130.

Each PCA shown in Figure 1 contains a special interface to bus 100. A block diagram of this special interface is shown in Figure 3. The interface consists of four chips interconnected as shown. Chips 201, 202 and 203 are manufactured by Texas Instruments Incorporated, P.O. Box 225012, Dallas, Texas 75265. Chip 201 has a part number 75ALS520. Chip 202 and chip 203 have a part number 74ALS240N. A chip 204 is a 16 x 16 Bit Serial Nonvolatile Static RAM produced by Xicor Inc., and has a part number X2444.

Data bus 100 includes the following lines from the interface of each of the PCAs connected to bus 100: lines 205, 206, 207, 208, 209, 219, 221, and 239. Each of these lines are interconnected to the bus, and thus are interconnected with corresponding lines from interfaces in each of the PCAs connected to bus 100. Lines 241, 242, 211, 228 and 229 are all set at a logic 1. Lines 243, 220, 223, 224 and 225 are all set at logic 0. Lines 244, 245, 246, 234, 236, 237 and 238 are not connected. Lines 212, 213, 214, 215 and 216 give a unique five-bit address for each PCA. This unique five-bit address is determined by the slot the PCA is placed in. The unique address allows each PCA to be addressed individually.

Bus 100 is controlled by PDH 127. The following is a description of how PDH 127 interacts with the interface circuit shown in Figure 3, and thus with the interface circuit in each of the interfaces within PCAs coupled to bus 100.

PDH 127 places a five-bit address on lines 506, 507, 508, 509 and 510. PDH 127 raises line 205 to a logic 1. . Chip 201 checks to see if the address on lines 506-510 matches the unique five-bit address on lines 512-516. If so, line 205 is activated to logic 0, enabling chip 203. Chip 202 is always enabled;

therefore, chip 202 receives the logic 0 at line 218, inverts the signal, and through line 227 enables chip 204. Once chip 204 is enabled, chip 204 is able to read a clock signal which PDH 127 places on line 219 and a data signal which PDH places on line 221. These signals are inverted by chip 202 and placed on lines 230 and 231 respectively. Additionally, once chip 203 is activated, chip 204 may transmit data to PDH 127 by placing the information on line 240. This information is inverted by chip 203 and placed on line 239, where it is read by PDH 127.

Chip 204 is able to contain 32 bytes of information. In the preferred embodiment the following information is stored by each PCA: an assembly number which indicates the type of board, e.g., memory array, processor, etc.; a date code which indicates what revision of the board currently resides in the PCA; A hardware identification number which is used to define the processor type, a serial number for the board, a division number, which indicates the company division which manufactures the board; boot identification number, which indicates which board will boot the system; and a software identification number which further defines the processor type. In addition a byte is reserved to store the unique five-bit address of each PCA. In the current embodiment, the Assembly number requires five bytes, so the last byte of address 0010, is reserved for PDH 127. However, this information is not actually stored in chip 204 because the information is already available to PDH 127. The following table lists how the information is arranged in sixteen 16-bit words stored in chip 204.

Table I

ADDR	INFORMATION STORED
0000	Assembly Number
0001	"
0010	"
0011	Date Code
0100	Hardware Identification Number
0101	"
0110	Serial number
0111	"
1000	"
1001	Division Number
1010	Boot Identification Number
1011	"
1100	Software Identification Number
1101	"
1110	Unused
1111	"

The following explains how chip 204 receives and sends information. More complete information is available from the data sheet for this part.

Figure 4 is a timing diagram indicating how data may be accessed from chip 204. Figure 4 shows a clock signal (RCLK+) 401 which is placed on line 219, an input signal (RDIN+) 402 to chip 204, which is placed on line 221, and a output signal (RDOUT+) 403 which is placed on line 239. As can be seen from Figure 4, chip 204 sends or receives one bit of information per clock cycle. After being enabled chip 204 looks for a command start bit 404. These are followed by four bits 405 indicating an address within the memory array within chip 204. The address is followed by 3 bits 406 which contain a command. This command may be a "read" or a "write" or a general command which specifies chip 204 to perform some function internally. If the command is a read, as in Figure 4, data is accessed from chip 204. Immediately upon

receiving a command to read chip 204 places a first byte 407 and a second byte 408 on line 240 through chip 203 to line 239. First byte 407 and second byte 408 contain data stored within chip 204 at the address specified by bits 405.

Figure 5 is a timing diagram indicating how information may be stored by chip 204. Figure 5 shows clock signal 401 and input signal 402 as they are used to write data into chip 204. After being enabled chip 204 looks for a command start bit 504. These are followed by four bits 505 indicating an address within the memory array within chip 204. The address is followed by 3 bits 506 which contain a command. If the command is a write, as in Figure 5, data is written to chip 204. Upon receiving a command to write, chip 204 continues to reads a first byte 507 and a second byte 508 on line 240 which are placed on line 221. First byte 507 and second byte 508 contain data to be stored within chip 204 at the address specified by bits 505.

Figure 6 shows a block diagram of PDH 127. A bus interface 601 essentially comprises the interface shown in Figure 3. Bus interface 601 is coupled to bus 100 through lines 605. Additional circuitry 602 is shown coupled to lines 605 through lines 606. It is through lines 606 and their associated drivers within additional circuitry 602, that PDH 127 communicates with PCAs connected to bus 100. PDH 127 communicates with computer system circuitry 603 through lines 607. Computer system circuitry 603 may include some or all of the PCAs shown in Figure 1. Although PDH 127 controls data flow through bus 100, PDH 127 receives instructions from computer system circuitry 603 as to what information PDH 127 should require to be accessed or stored. Ultimately a User (not shown) queries computer system circuitry 603 as to biographical information about PCAs within the computing system. For instance a user may do so by using a terminal 604 coupled to computer system 603 through lines 608. Computer system circuitry 603

through lines 607 requests PDH 127 to find this information. PDH through lines 606 requests this information from the PCAs through bus 100.

Since bus 100 is not a high speed bus it may be optimal for PDH 127 to request information from each PCA at start-up time. PDH uses bus 100 to secure the biographical information from each PCA, this information may be stored in a memory 607. When biographical information is requested, PDH 127 may access this information from memory 607, saving the time required to access this information through bus 100.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. In a computer system which includes a plurality of printed circuit assemblies, an apparatus for allowing the electronic storage and retrieving of information about each printed circuit assembly, the apparatus comprising:

memory means within each printed circuit assembly for storing information about that printed circuit assembly; and

retrieval and storage means, including a bus coupled to each printed circuit assembly, for electronically retrieving the information from each printed circuit assembly and making the information available to a user, and for enabling a user to electronically change the information.

2. An apparatus as in claim 1 wherein said bus is coupled to each printed circuit assembly and wholly dedicated to the electronic storage and retrieval of information about each printed circuit assembly.

3. An apparatus as in claim 2 wherein the memory means comprises an interface to the bus comprising an interaction means for interacting with the bus, and a non-volatile random access memory.

4. An apparatus as in claim 3 wherein a first printed circuit assembly from the plurality of printed circuit assemblies controls all data transactions which occur on the bus.

5. An apparatus as in claim 4 wherein upon booting up the computer system, the first printed circuit assembly secures the information from each of the printed circuit assemblies and stores the information within the first printed circuit assembly whereby a user may access the information quickly.

6. An apparatus as in claim 1 wherein the information within a printed circuit assembly includes information indicating the latest revision level of that printed circuit assembly.

7. A method for making information about printed circuit assemblies readily accessible to users, the method comprising the steps of:

(a) providing a memory within each printed circuit assembly for storing information about the printed circuit assembly, including information about the current revision level of the printer assembly;

(b) storing information within a memory within a particular printed circuit assembly information pertaining to the particular printed circuit assembly;

(c) accessing the information within the memories electronically through a bus; and

(d) changing the information within the memories electronically through a bus.

8. An apparatus for allowing the electronic storage and retrieving of information substantially as herein described with reference to the accompanying drawings.

MBS

9. A method for making information about printed circuit assemblies readily accessible to users substantially as herein described with reference to the accompanying drawings.

DATED this 3rd day of April 1991

HEWLETT-PACKARD COMPANY

Attorney: IAN T. ERNST

Fellow Institute of Patent Attorneys of Australia

of SHELSTON WATERS

N175

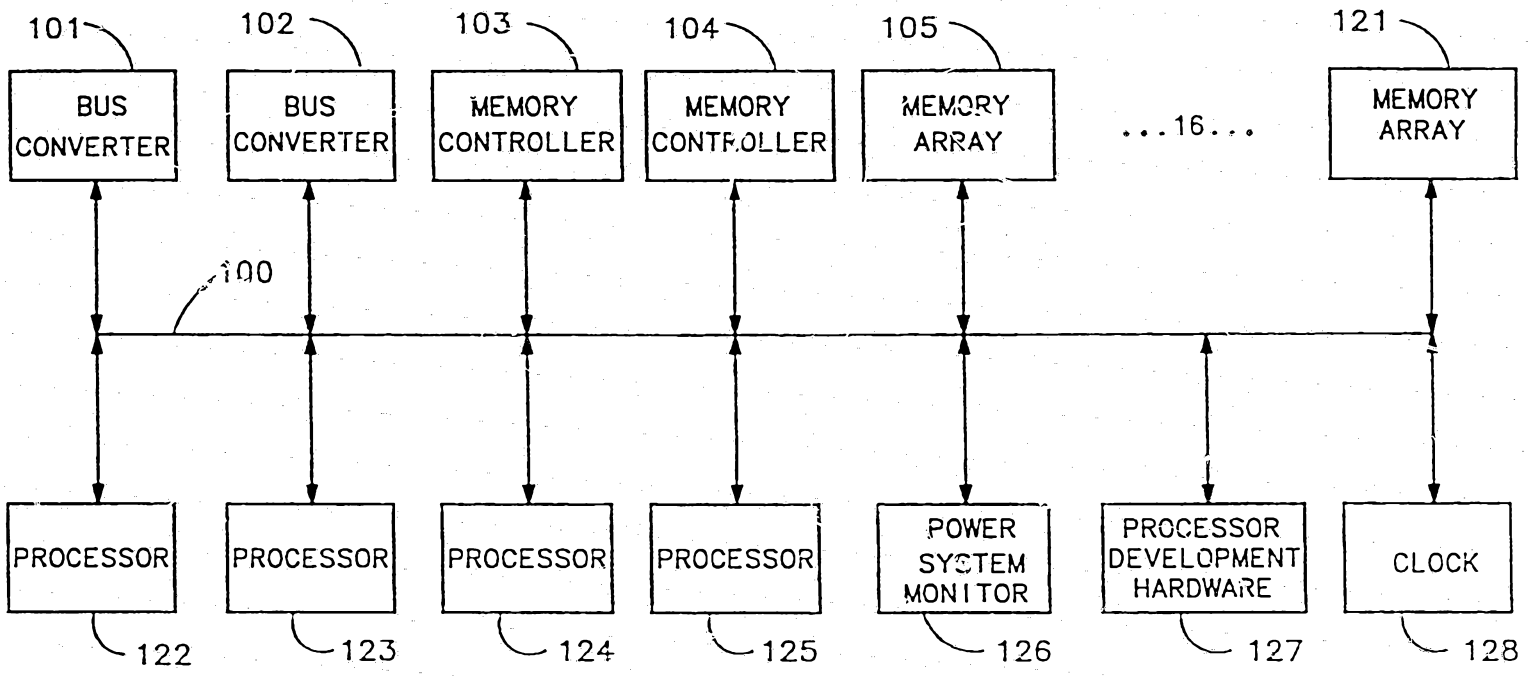


FIG 1

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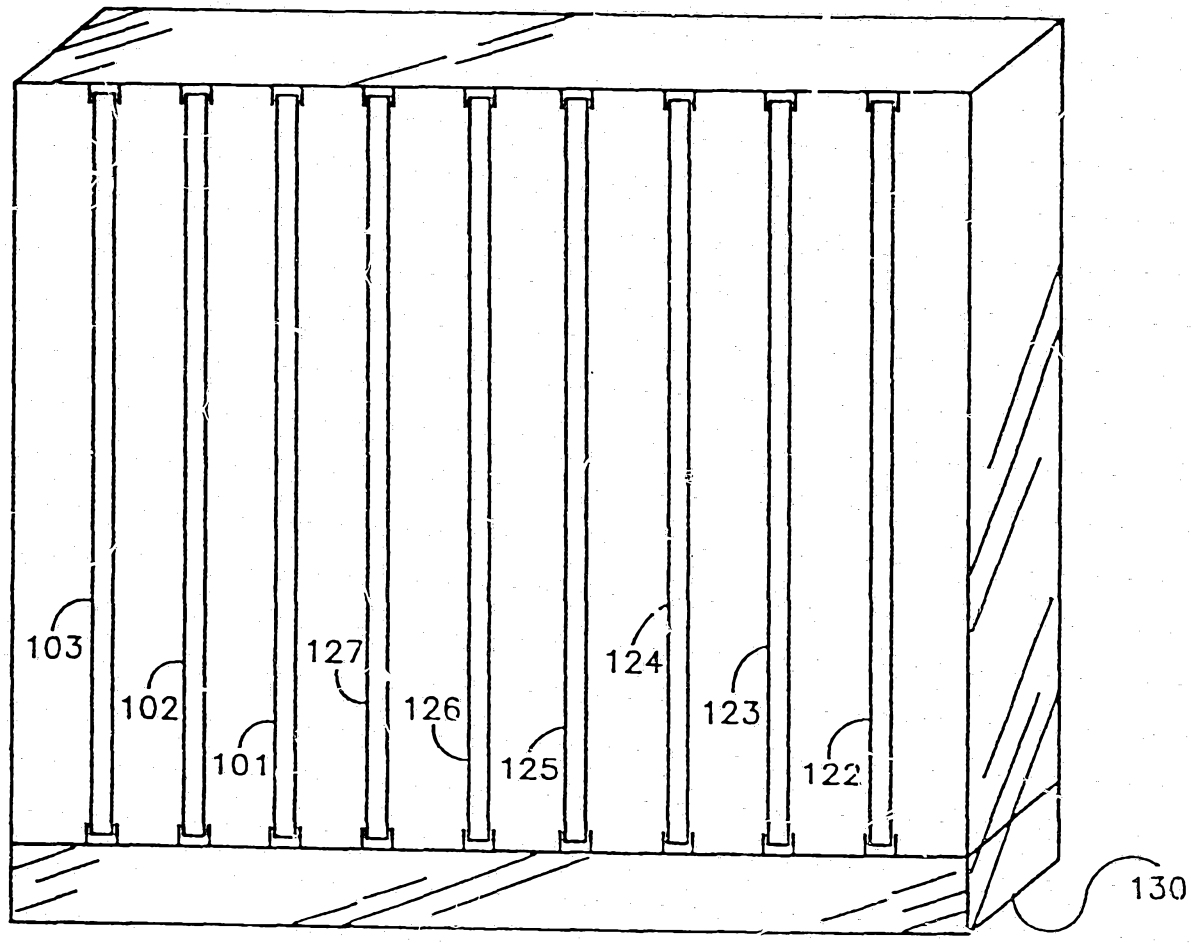


FIG 2

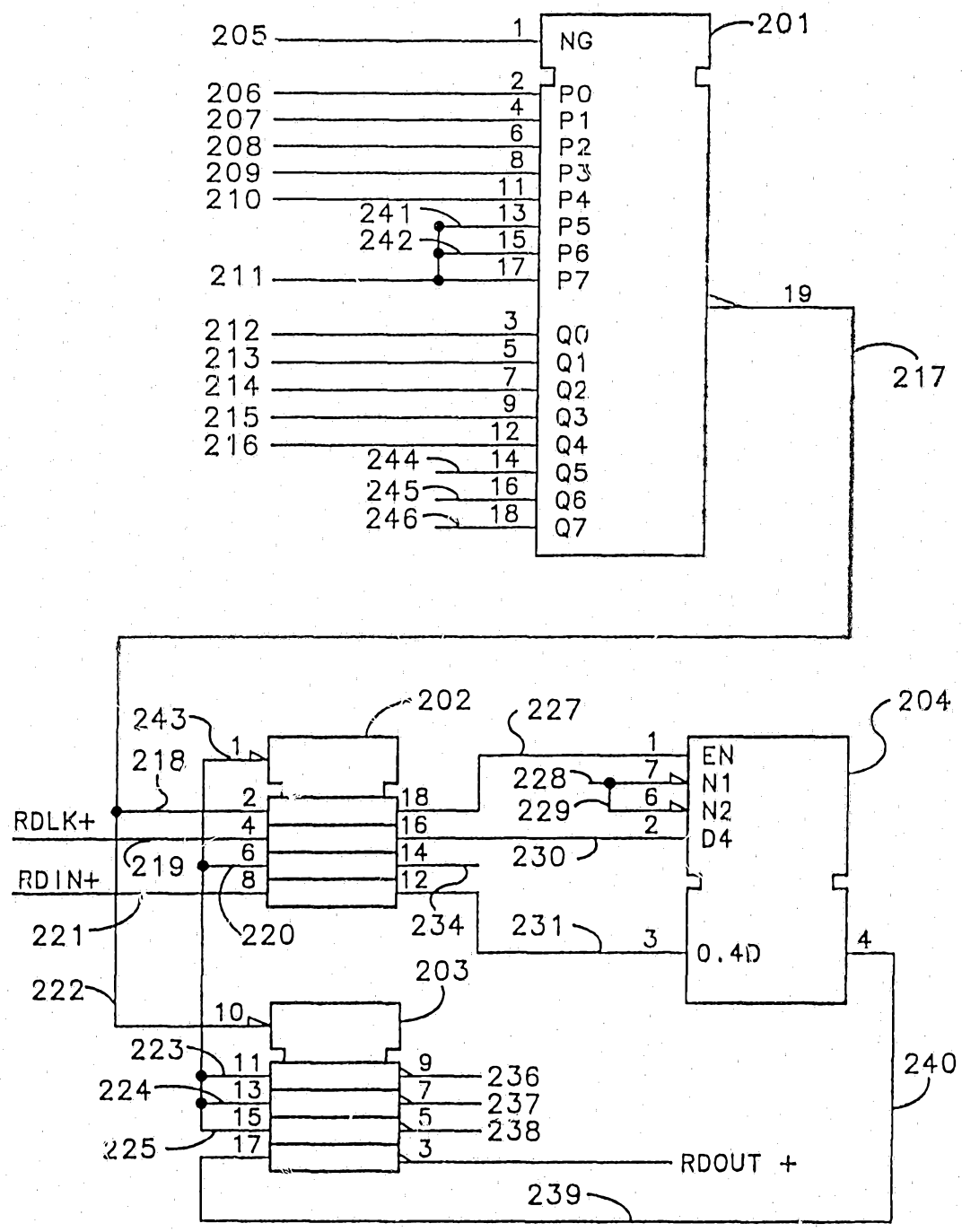

205
206
207
208
209
210
241
242
211
212
213
214
215
216
244
245
246
1
2
4
6
8
11
13
15
17
3
5
7
9
12
14
16
18
NG
P0
P1
P2
P3
P4
P5
P6
P7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
201
19
217
243
218
219
221
222
223
224
225
RDLK+
RDIN+
202
203
220
227
228
229
230
231
234
204
EN
N1
N2
D4
0.4D
236
237
238
RDOUT +
239
240

FIG 3



FIG 4A

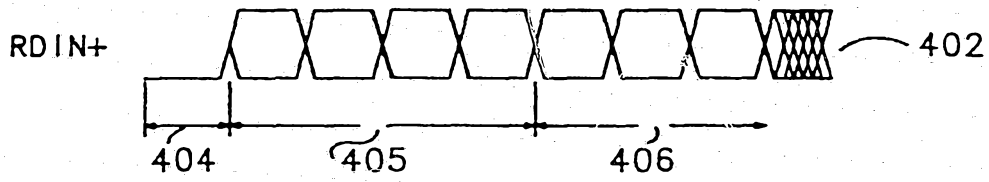


FIG 4B

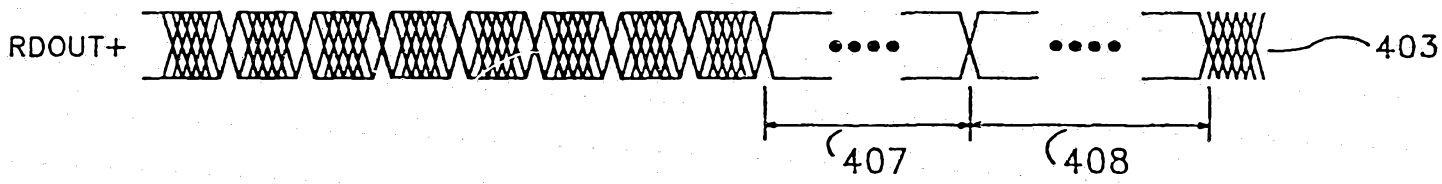


FIG 4C



FIG 5A

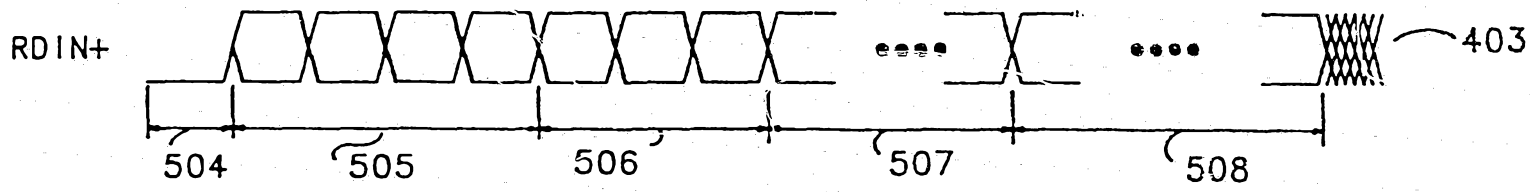


FIG 5B

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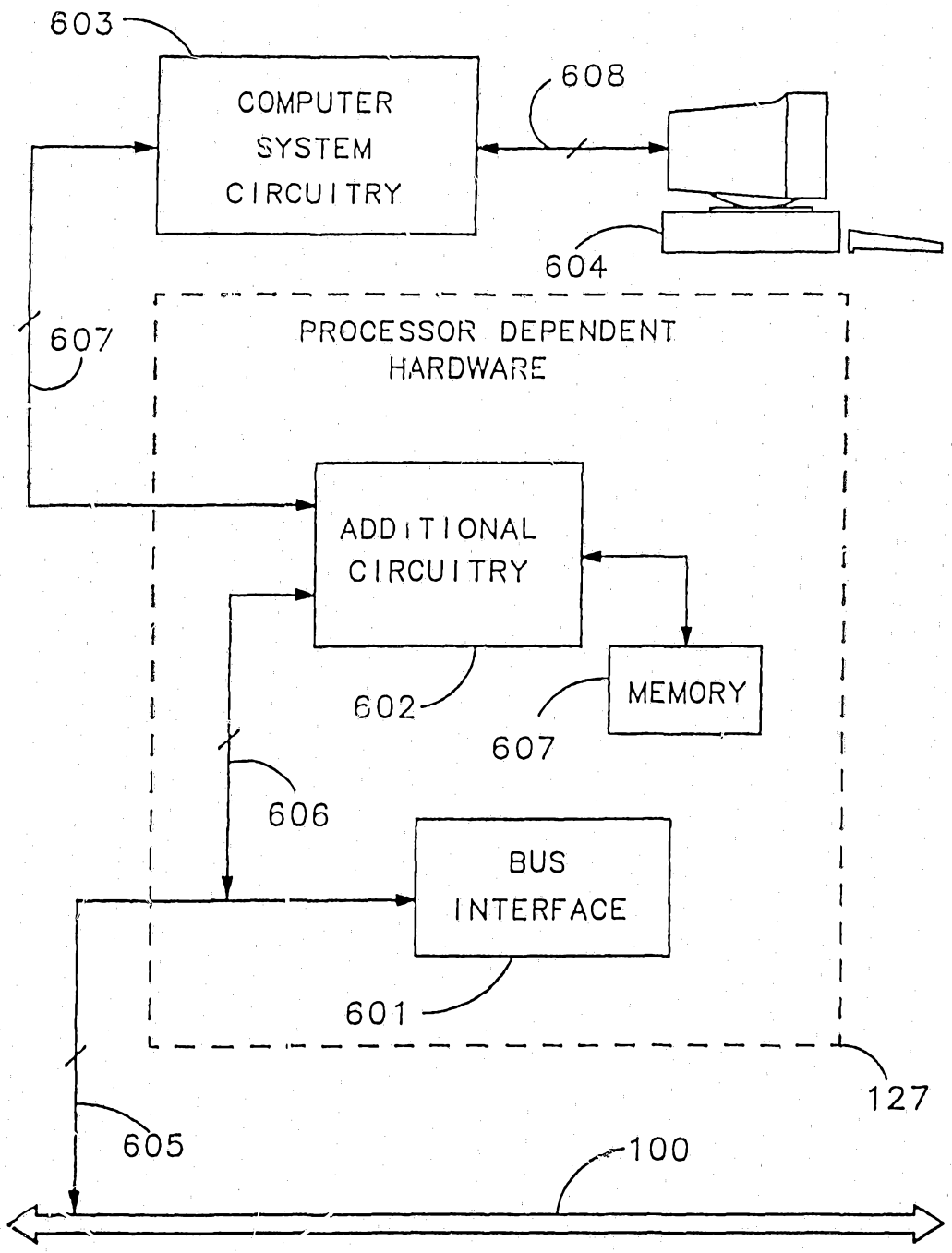


FIG 6