(54) Title: METHOD AND APPARATUS FOR IMAGE DATA PROCESSING
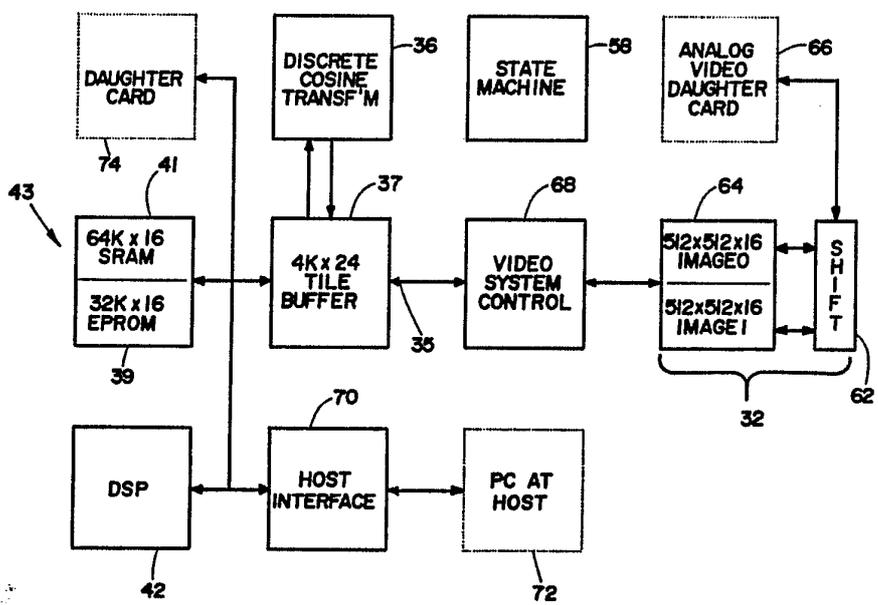
(57) Abstract

A method of processing digital image data such as obtained from a television screen for transmission along telephone lines such thtat the transmitted data can be transformed to produce images in colour. The method includes storing a frame of incoming digital image data in a frame buffer, transferring a group of tiles from said frame buffer to a tile buffer, generating a clock signal, generating address and sets of control signals in a state machine, applying the clock signal to a digital transformer and applying each address and set of control signals to said tile buffer to directly transfer a block of data in the tile buffer to the digital transformer. Next the data in the block is transformed, returned to the tile buffer and is written over the corresponding untransformed data in the tile buffer. These steps are repeated until all tiles in the tile block have been transformed and returned. The transformed tiles in the tile block are then coded so as to complete their compression. The compression steps are repeated until all tiles in the frame buffer are compressed.

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METHOD AND APPARATUS FOR IMAGE DATA PROCESSING

BACKGROUND

The present invention relates to a method and apparatus for processing image data for transmission along telephone lines and for decoding the processed data after transmission such that the data can be transformed to produce colour images of colour television quality.

Known systems for transmitting image data along telephone lines are severely limited in the speed at which the data can be transmitted and reassembled at a receiving end. For example, a single frame of a colour television quality image contains 512 by 512 by 24 bits and takes approximately 90 seconds to transmit without compression using a 64 kilobit per second standard ISDN B channel. One method to enhance transmission speed is to compress the data according to known transforms and then, after transmission, to decompress the compressed, transmitted data.

A television screen, for example, is divided up into a plurality of individual image units referred to as pixels. For colour images each pixel may contain three separate parameters such as red, green and blue. Each parameter may be defined as to intensity by an eight bit number called a byte. Thus, each pixel is defined by three bytes. In order to process the data efficiently it is useful to treat a block of 8 by 8 pixels known as a "tile". A known technique consists of directing a first tile of an image into a processor and then inputting the first tile into a digital transformer. The tile output modified by the transformer is sent back to the processor where it is further compressed and sent to an output port. The second tile in the image is then sent to the transformer. This process is repeated until all of the image tile have been processed. In such a system the requirement for numerous fetch and other instructions from the processor makes the process impractically slow. Thus, the advantages of transmission speed increase due to compression

is offset by the time take to compress and decompress.

Accordingly, it is an object of the invention to provide an improved method of processing imaging data for compression and decompression. It is a further object of the invention to provide a buffer to receive and store data corresponding to an image and then to process the captured data.

SUMMARY OF THE INVENTION

According to the invention there is provided a method of processing digital image data such as obtained from a television screen for transmission along telephone lines in a way that the transmitted data can be transformed to produce images in colour. The method includes storing a frame of digital data in a frame buffer, transferring a group of tiles from said frame buffer to a tile buffer, generating a clock signal, and generating address and sets of control signals in a state machine. The clock signal is applied to a digital transformer while the address and set of control signals are applied to the tile buffer to directly transfer a block of data in the tile buffer to the digital transformer. After the data is transformed in the digital transformer it is returned to the tile buffer where it is used to overwrite the corresponding original block of data stored in the tile buffer. The latter process is followed by coding the transformed tiles stored in the tile block so as to compress them The process is repeated until all tiles in the frame buffer have been compressed.

Preferably the group of tiles is transferred directly to the tile buffer. The clock signal may have a frequency of greater than approximately one megahertz. Advantageously, the digital transforming step applies a discrete cosine transform while the coding is Huffman coding.

An improvement in speed is achieved by utilizing Y, I

and Q parameters to define a pixel colour. By alternating I and Q data in each alternate pixel, a saving of 1/3 of the data required to describe the image is achieved without a significant loss of resolution or colour.

The compressing step may include sequentially transferring tiles of the data into a tile buffer and performing a discrete cosine transform on each of the tiles. The transformed tiles are then coded in accordance with Huffman Coding. The DCT and Huffman Coding are described in ISO/CCITT JPEG-8-R5.2 standard recently published.

The tile pixels in the frame buffer are extracted row by row tile by tile until an entire row of tiles has been transferred. commencing from the first row and proceeding in sequence row by row until the last row has been extracted.

The video signals, if in analog form are first digitized before storing a frame of them in the frame buffer. After compressing the data it is transferred to a communication output interface.

The method may also include reversing the order of processing to perform first inverse Huffman Coding on compressed data, followed by inverse Huffman Coding and then transferring the decompressed data to the frame buffer for further transfer to be transformed into analog video signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as other features and advantages thereof, will be best understood by reference to the detailed description which follow, read in conjunction with the accompanying drawings, wherein:

Figure 1 is a block diagram of a conventional system for processing image data;

Figure 2 is a block diagram of a preferred apparatus for processing image data from analog video source such as a television monitor;

Figure 3(a) and 3(b) are schematic diagrams showing a portion of a row of pixels in a part of the frame buffer to demonstrate their composition for two different choices of parameters to describe colour and intensity;

Figure 4 is a timing diagram showing the movement of tiles into and out of the discrete cosine transform chip;

Figure 5 is a schematic block diagram showing the state machine and its output of address and control signals which govern the flow of data between the frame buffer, the tile buffer and the discrete cosine transform;

Figure 6 is a table showing the structure of the address bits generated by the state machine which are used to transfer data between the frame buffer, the tile buffer and the discrete cosine transform (DCT); and

Figure 7 is a block diagram showing a more detailed system corresponding to that shown in Figures 2 and 5 hereof.

DETAILED DESCRIPTION WITH REFERENCE TO THE DRAWINGS

Referring to Figure 1 there is shown a conventional system for processing image data received from a video source in analog form on line 12. The signals on line 12 are converted to digital signals by analog to digital converter 14, outputted on line 16 to a frame buffer 17 and then to a processor 18. The processor transmits the data on line 20 to a digital transformer

22 which modifies the data and returns it back to the processor 18 where it is then sent along line 30 to a telephone line for transmission. The digital transformer 22, which performs a discrete cosine transform on tiles made up of a block of 8 pixels by 8 pixels, inputs and outputs its data in a predefined order. This required ordering of the data is determined by the internal structure of the digital transformer 22. The image data received by the processor 18 from the frame buffer 17 are sent to and received from the digital transformer 22 in tiles of 8 pixels by 8 pixels in the order expected by the digital transformer 22. Each tile of image data from the frame buffer 17 is directed through the digital transformer 22 and further processed by the processor 18 in order to compress the image. Although data is compressed by the transformer 22, the time for compression and subsequent decompression on a receiving end (not shown) would offset any advantage due to increased speed of transmission.

Referring to Figure 2 there is shown a system in accordance with a preferred embodiment of the invention in which analog signals on line 12 are converted to digital signals on line 16 by an analog-to-digital converter 14. The digitized image data from the analog to digital converter 14 is sent on line 16 to a frame buffer 32 in which the image data is temporarily stored or captured. The frame buffer 32 consists of 8 one megabit video dynamic random access memory chips (called "VRAMS") made by Texas Instruments Incorporated which form two image memory units each of 512 X 512 X 16 bits capacity. Data in the frame buffer 32 is stored in rows with each block of 8 pixel x 8 pixel forming a tile. A first row of tiles ("row 0") is moved into the tile buffer 37 from the frame buffer 32 along line 35 in response to control signals from a state machine 58. The memory 39 of the tile buffer 37 (see Figure 7) consists of enough high speed static random access memory (SRAM) chips 41 to contain one row of 8 pixel by 8 pixel tiles from the frame buffer 32. The state machine 58 moves the first two tiles in the tile buffer 37 into the digital transformer 36, which in this case is a discrete cosine transform chip manufactured by INMOS in the

United Kingdom and sold under part number 1MSA121 (hereinafter referred to as a "DCT"), where they are processed and then transferred back to the tile buffer 37. The state machine 58 presents the individual pixels
of each tile to the DCT chip 36 in the order required by the DCT chip 36. In addition, the state machine 58 overwrites each tile in the tile buffer 37 with the resulting DCT coefficients generated by the DCT chip 36. The DCT chip 36 takes 8 pixel x 8 pixel tiles, performs a discrete cosine transform, and then outputs the results.

Following the transformation of the first two tiles from the tile buffer 37 through the DCT chip 36, each remaining pair of tiles in the tile buffer 37 is directed through the DCT chip 36 by the state machine 58 until all of the tiles have been transformed and their resulting DCT coefficients are stored back in the tile buffer 37. The DCT coefficients in the tile buffer 37 are then accessed by a digital signal processor (DSP) 42 chip which commences a coefficient to symbol conversion, namely such as Huffman coding, on the data. Other types of conversion are possible. The DSP chip 42 is manufactured by Texas Instruments Incorporated under part number TMS320C25. The resulting compressed data from the DSP 42 is then sent to a communication card 74 and is ultimately sent over a telephone line or stored on a hard disk drive (not shown).

While the DSP chip 42 is performing coefficient to symbol conversion, the state machine 58 begins operation on the second row of tiles (row 1) in the frame buffer 32. It transfers this row of image data to the tile buffer 37 and, once again, runs this data through the DCT chip 36 and deposits the results back in the tile buffer 37 for the DSP 42 to eventually access. Row by row of tiles from the frame buffer 32 are transferred to the tile buffer 37, transformed by the DCT 36, and then directed to the DSP 42 for coefficient to symbol conversion until the entire image, comprised of all 64 rows of tiles, has been compressed. The data movement operations caused by the state machine 58 and the processing by the DSP 42 may occur concurrently so that discrete cosine transformations may occur

in parallel with Huffman coding, further increasing the compression speed.

The circuit of Figure 2 can also receive compressed data on line 44 into the DSP 42 which applies a symbol to coefficient conversion known as reverse Huffman coding. Other types of conversion are also possible. Following operation by the DSP 42, the data is transferred to the tile buffer 37 from which it goes into the DCT 36. The DCT chip 36 is configured to apply an inverse transform and hence decompress the data. The decompressed data is written into the frame buffer 32 from which it can be directed to a desired output.

Referring to Figure 7 there is shown a more detailed diagram of the imaging system. Here analog video signals received by a daughter card 66 are digitized and sent to shift register 62 which is incorporated into the frame buffer 32 together with the VRAM chip 64. The frame buffer 32 is controlled by a video system controller chip 68 which refreshes the frame buffer 32 and arbitrates access to the frame buffer 32. The DSP 42 has its own discrete memory 43 consisting of 64 kilobytes of high speed static ram memory 41 and 32 Kilobytes of electrically erasable programmable only memory (EPROM) 39. Output from the DSP is through either a communication daughter card 74 or to a host interface 70 couplable to a host computer 72.

Each pixel 46 of frame buffer 32 is shown schematically in Figure 3(a) as consisting of three parameters such as red 47, green 48 and blue 49. The intensity of each colour component is described by an 8 bit number. Other means of describing the colour and intensity of a pixel may be used. The method employed in the present invention consists of choosing a parameter Y corresponding to intensity and two parameters I and Q which correspond to colour. It is possible with such a choice to reduce the number of bytes required in each pixel from three to two by alternating I and Q in adjacent pixels as shown in Figure

3(b) without detracting noticeably from the quality of the picture. Thus, each tile consists of an 8 pixel x 8 pixel block with each pixel having a number of bits to describe its colour and intensity.

Image data in the frame buffer 32 is stored in a YIQ format. With respect to figure 2, when a row of tiles is transferred from the frame buffer 32 to the memory of the tile buffer 37, the Y, I and Q components are all transferred into the tile buffer memory 41. However, the state machine 58 first sends all of the Y image components of all tiles in the tile buffer 37 through the DCT chip 36, followed by the I then Q components. Once the operation of the DCT chip 36 is complete, the DSP 42 is able to access the DCT coefficients in the tile buffer 37 for all three components Y, I, and Q.

To appreciate the timing of transferring tiles Figure 4 shows that the first two tiles are transferred sequentially to the DCT 36 and are returned to the tile buffer before the next two tiles are extracted from the frame buffer 32 and placed in the tile buffer 37. Thus, there is a delay of two tiles introduced by the return of processed tiles from the DCT 36.

The operation of the state machine 58, implemented with programmable array logic the chips for which are commonly referred to as PAL's, is controlled by the digital signal processor 42. Upon informing the state machine 58 of the required operation, such as a frame buffer 32 to tile buffer 37 transfer or DCT 36 transformation, by depositing a specific control value in a state machine control register 60 (see Figure 5), the DSP 42 sends a signal to the state machine 58 informing it to "go". The state machine 58 performs the operation requested by the DSP 42 and, upon completion, sends an "I'm done" signal to the DSP 42. While the state machine 58 is performing an operation the DSP 42 is free to do other tasks.

When performing any transfer operation, as seen in

Figure 5, the state machine 58 must generate address signals for the tile buffer 37 and frame buffer 32 and control signals for the tile buffer 37, frame buffer 32, and DCT chip 36. The address generated by the state machine 58 originates from a group of counters 46 divided into address fields. Each field of addresses may be independently incremented by the state machine 58. The concatenated address fields form the full address used by both the tile buffer 37 and the frame buffer 32 memories. Individual address fields may define the tile number "t", row number "r", and column number "c" transferred at any given time in a state machine operation. By examining a control register 60 of the state machine 58 and the current address of the address fields, the state machine 58 is able to decide the appropriate "next address" for the next data transfer and pulses the appropriate increment signal on selected ones of lines 56 to the counters 46 so that that address is generated. The control signals inform the tile buffer 37, frame buffer 32, and DCT chip 36 when to read and write data. They are generated by the state machine 58 by examining the state machine control register 60 and the current state of the state machine 58.

The state machine addresses, shown in detail in Figure 6, each consist of 13 bits divided up into four different fields. The fields are write "w", row number "r", tile number "t" and column number "c". Together r, t, and c produce an address which points to a single pixel or coefficient within the frame buffer 32 or tile buffer 37. The tile field "t" indicates the current tile which is involved in a state machine transfer. There are 64 Y tiles and 32 of each of the I and Q tiles contained within a row of tiles. Therefore, 6 bits are required to indicate a unique Y field of a tile and 5 bits to indicate a unique I or Q field. The row field "r" indicates the row, numbered from 0 to 7 and the column field indicates the column numbered from 0 to 7 within the given tile. The value in the single bit write field is used to determine whether a tile buffer "read" or tile buffer "write" will occur during transfers to and from the DCT 36. Because I image components are stored only in even pixels in the

frame buffer and Q image components are stored only in odd pixels
in the frame buffer, as shown in Figure 3(b), the arrangement
for the I and Q tile and column fields differ from the Y
component's tile and column field arrangement.

The state machine carries out the following five
different transfer operations:

(1)   Transfer of a row of tiles from the frame buffer
32 to the tile buffer 37.

(2)   Transfer of a row of tiles from the tile buffer
37 to the frame buffer 32.

(3)   Transfer the Y component of the tiles in the tile
buffer through the DCT chip 36 and back into the tile buffer 37.

(4)   Transfer of the I component of the tiles in the
tile buffer 37 tiles through the DCT chip 37 and back into the
tile buffer 37.

(5)   Transfer of the Q component of the tiles in the
tile buffer 37 through the DCT chip 36 and back into the tile
buffer 37.

The address generated by the state machine 58 flows to
both the tile and frame buffers 37 and 32, respectively. As an
example, when setup by the DSP 42 to perform a frame buffer 32
to tile buffer 37 transfer and told to "go", the state machine's
address fields are initially all equal to zero. The address is
pointing, therefore, to row 0 and column 0 of tile 0, which is
the first pixel in both the frame and tile buffers 32 and 37,
respectively. A read signal is sent to the frame buffer 32, a
write signal is sent to the tile buffer 37 and the first word of
image components is transferred directly from frame buffer 32 to
the tile buffer 37.

Immediately following the aforementioned pixel transfer, the state machine 58 examines the current state of the address fields and the type of transfer requested. It uses this information to determine the proper "next address" required and strobes the appropriate increment pulses to generate that address. In this case, increment pulse 0 would be strobed resulting in the column field being increased to 1. The second pixel is then transferred directly from the frame buffer 32 to the tile buffer 37 by the state machine 58 by again strobing the appropriate read and write control signals.

The state machine 58 continually strobes the appropriate increment pulses to generate the required address and the read/write control signals to initiate the frame buffer 32 to tile buffer 37 transfer until all pixels in the selected row of tiles in the frame buffer 32 have been transferred to the tile buffer 37. The full address sent to both the frame buffer 32 and tile buffer 37 is simply incremented by one for each pixel transfer, in a frame buffer 32 to tile buffer 37 transfer, until the state machine 58 detects that the last transfer (the 4095th pixel) has been accomplished. At this time, the state machine 58 sends an "I'm done" signal to the DSP 42 to indicate the completion of the requested operation.

When the state machine 58 is conditioned by the DSP 42 to transfer data to and from the DCT 36 and told to "go", for each DCT chip 36 clock cycle, the state machine 58 must send an expected pixel or coefficient of data to or cause the tile buffer 37 to receive it from the DCT chip 36. The DCT chip 36 requires input and output data to be handled in a strict order. For example, the DCT chip 36 requires data to be presented to it row by row within a give tile. The state machine is able to generate the proper address by examining the type of DCT operation in progress (Y, I, or Q) and the current state of the address field. The address initially points to row and column 0 of tile 0. As data is transferred from the tile buffer 37 to the DCT chip 36, the column address field is first incremented until it reaches

a maximum, i.e. 7. For the next transfer the column address field is reset and the row field is incremented. Eventually, when both the column and row address field reach their maximum value, they are reset and the tile field is incremented. Using this technique to generate the address flowing to the tile buffer 37, the DCT chip 36, is able to receive tile input data in the appropriate order. Output data from the DCT chip 35, directed to the tile buffer 37, is stored back in the appropriate tile, column, and row address locations using the same address generation technique. The write field indicates whether a tile buffer to DCT chip or DCT chip 36 to tile buffer 37 data transfer is currently occurring. Once all tiles within the tile buffer 37 have been directed through the DCT chip 36, the state machine 58 sends an "I'm done" signal to the DSP.

It is possible to use adaptive Huffman Coding rather than Huffman Coding. However, in the latter case it would require transferring back transformed data after operation of the DCT into the frame buffer as adaptive Huffman Coding requires that the whole of the intermediate results be looked at.

Accordingly, while this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

I CLAIM:

1.   A method of processing digital image data such as obtained from a television screen for transmission along telephone lines such that the transmitted data can be transformed to produce images in colour, comprising:

(a)   storing a frame of incoming digital image data in a frame buffer;

(b)   transferring a group of tiles from said frame buffer to a tile buffer;

(c)   generating a clock signal;

(d)   generating address and sets of control signals in a state machine;

(e)   applying the clock signal to a digital transformer and applying each address and set of control signals to said tile buffer to directly transfer a block of data in the tile buffer to the digital transformer;

(f)   transforming the data in said block;

(g)   returning the block of data transformed to said tile buffer and overwriting the corresponding untransformed data in said tile buffer with transformed data;

(h)   repeating steps (c) to (g) until all tiles in said group of tiles have been transformed and returned;

(i)   coding the transformed tiles in said group of tiles so as to compress the tiles; and

(j)   repeating steps (b), (h) to (i) until all tiles in said frame buffer are compressed.

2.   A method according to claim 1, wherein said group of
tiles is transferred directly to said tile buffer.

3.   A method according to claim 1 or 2, wherein said clock
signal has a frequency greater than approximately one megahertz.

4.   A method according to claim 1 or 2, wherein said
digital transformer applies a discrete cosine transform.

5.   A method according to claim 2, wherein said coding is
Huffman coding.

6.   A method according to claim 1 or 2, wherein data stored
in said frame buffer is in the form of 8 bits of Y intensity
data, 8 bits of I colour data and 8 bits of Q colour data with
each pixel defined by either Y and I or Y and Q with I and Q
alternating along each row of pixels.

7.   A method according to claim 1, wherein said block of
data is a pair of tiles of Y, I, or Q data.

8.   A method according to claim 7, wherein data in said
tile buffer is transferred by transferring to said digital
transformer first all tiles of Y data, then all tiles of I data
and finally all tiles of Q data, two tiles at a time and
returning the transformed two tiles before transferring the next
two tiles, the tile transferring commencing with the first two
tiles of Y data in said tile buffer and proceeding sequentially
to the last two tiles of Q data in said tile buffer.

9.   A method processing digital image data such as obtained from a television screen for transmission along telephone lines such that the transmitted data can be transformed to produce images in colour, comprising:

(a)   storing a frame of tiles in a frame buffer;

(b)   transferring a group of tiles of digital data directly from said frame buffer to a tile buffer;

(c)   compressing said group of tiles of data;

(d)   repeating steps (b) and (c) until all tiles of data in said frame buffer have been compressed.

10.   A method according to claim 9, wherein said compressing step includes:

(c)   generating a clock signal;

(d)   generating address and sets of control signals in a state machine;

(e)   applying the clock signal to a digital transformer and applying each address and set of control signals to said tile buffer to directly transfer a block of data in the tile buffer to the digital transformer;

(f)   transforming the data in said block;

(g)   returning the block of data transformed to said tile buffer and overwriting the corresponding untransformed data in said tile buffer with transformed data;

(h)   repeating steps (c) to (g) until all tiles in said tile block have been transformed and returned;

(i)   coding the transformed tiles in said tile block so as to compress the tiles; and

(j)   repeating steps (h) to (i) until all tiles in said frame buffer are compressed.

11.   A method according to claim 10, wherein said state machine generates addresses by establishing counters for each address field and concatenating the fields to provide an address.

12.   A method according to claim 10, wherein said group of tiles is a row of tiles and performing discrete cosine transform on each tile in succession in said row of tiles, transferring said transformed row of tiles to a processor and operating on each transformed tile in said row of tiles in succession to perform coefficient to symbol conversion.

13.   A method according to claim 2, wherein said coding performed by said processor is Huffman coding.

14.   A method according to claims 5 or 13, including performing inverse Huffman Coding on incoming compressed data, performing an inverse discrete cosine transform on said compressed data after having applied inverse Huffman coding, and then transferring said decompressed data to said frame buffer for temporary storage.

15.   A method of processing image data from a video screen, comprising:

(a)   digitizing the analog video signals;

(b) storing a frame of the video signals in a frame buffer;

(c) extracting a first row of tiles from said frame buffer and transferring them directly to a tile buffer;

(d) compressing said first row of tiles of data;

(e) extracting and compressing sequentially subsequent rows of tiles in said frame buffer until all tiles have been extracted and compressed; and

(f) transferring said compressed data to a communication output interface.

16. A method according to claim 15, wherein said compressing step includes transferring sequentially rows of said tiles into a tile buffer, performing a discrete cosine transform on each such row of tiles and transferring said transformed row of tiles to a processor and operating on said transformed tiles in succession to perform Huffman Coding.

17. A method according to claim 16, including applying inverse Huffman coding to incoming compressed data, transferring said inversely coded data to a tile buffer, performing an inverse discrete cosine transform on said data and then transferring said data directly from said tile buffer to a frame buffer.

18. An apparatus for processing digital image data such as obtained from a television or video screen, comprising:

(a) means for storing a frame of data in a frame buffer;

(b) a tile buffer;

        (b)   means for transferring said data row by row directly
to said tile buffer; and

        (c)   means for compressing said extracted data.

19.   Apparatus according to claim 18, wherein said storing
means is a video dynamic random access memory unit.

20.   Apparatus according to claim 19, wherein said
transferring means is a state machine coupled to said frame
buffer, said tile buffer and said digital transformer and
operative to provide address and control signals to each of the
latter so as to cause data in said frame buffer to be transferred
directly row by row to or from said tile buffer, and to cause
tile transfers directly between said tile buffer and said digital
transformer.

21.   Apparatus for processing digital image data such as
obtained from a television or video screen, comprising:

        (a)   a frame buffer for capturing and storing a frame of
digital image data;

        (b)   a tile buffer electrically coupled to said frame
buffer;

        (c)   a discrete cosine transform unit electrically coupled
to said tile buffer;

        (d)   a state machine electrically coupled to said frame
buffer and said tile buffer;

        (e) a digital signal processor electrically coupled to said
tile buffer and said state machine,

wherein in response to control signals from said state machine, tiles are transferred from said frame buffer directly to said tile buffer, from said tile buffer to said discrete cosine transform unit for processing and then returned back to said tile buffer, and said digital signal processor extracts transformed tiles from said tile buffer for processing by Huffman coding or applies inverse Huffman coding to incoming compressed data and transfers that data to said tile buffer.

22.   An apparatus for processing digital image data such as obtained from a television screen for transmission along telephone lines such that the transmitted data can be transformed to produce images in colour, comprising:

        (a)   a frame buffer for storing a frame of digital image data;

        (b)   a tile buffer electrically coupled to said frame buffer;

        (c)   a digital transformer electrically coupled to said tile buffer;

        (d)   a processor electrically coupled to said tile buffer;

        (e)   a clock coupled to said transformer for generating a clock signal;

        (f)   a state machine electrically coupled to said frame buffer, tile buffer, and digital transformer, processor and responsive to a "go" signal from said processor to generated address and sets of control signals and apply them to said frame buffer and said tile buffer and in conjunction with said clock signal to effect transfers of groups of tiles directly from said frame buffer to said tile buffer or from said tile buffer to said frame buffer until a whole frame of tiles has been transferred and to effect a direct transfer of a block of data in the tile

buffer to said digital transformer where it is transferred and to subsequently return the transformed block of data to the tile buffer and overwrite corresponding untransformed data stored in said tile buffer and to repeat this process until a group of tiles has been transformed;

wherein said processor extracts transformed data from said tile buffer and performs Huffman coding on said data or receives compressed data, performs inverse Huffman coding on it and transforms it to the tile buffer.

23.   Apparatus according to claim 22, said digital transformer performs discrete cosine transforms or inverse discrete cosine transforms.

24.   Apparatus according to claim 22, wherein said group of tiles is a row of tiles and said block of tiles is a pair of tiles.

25.   Apparatus according to claim 22, including means for digitizing analog video data prior to its capture by said frame buffer.

26.   Apparatus according to claim 22, including means for transmitting compressed data along a telephone line.
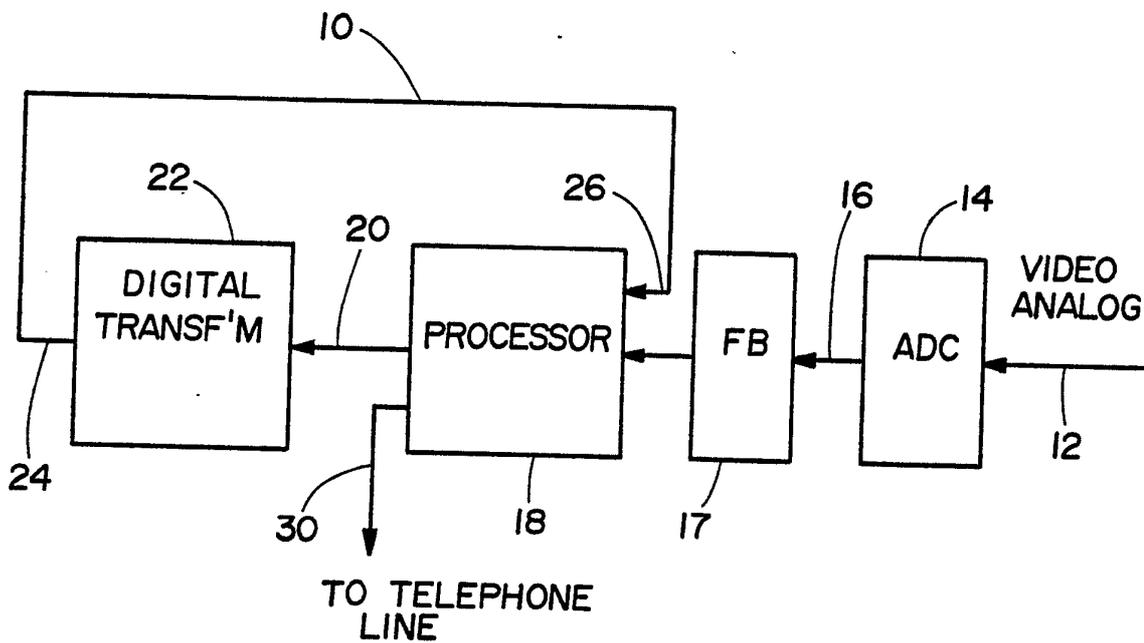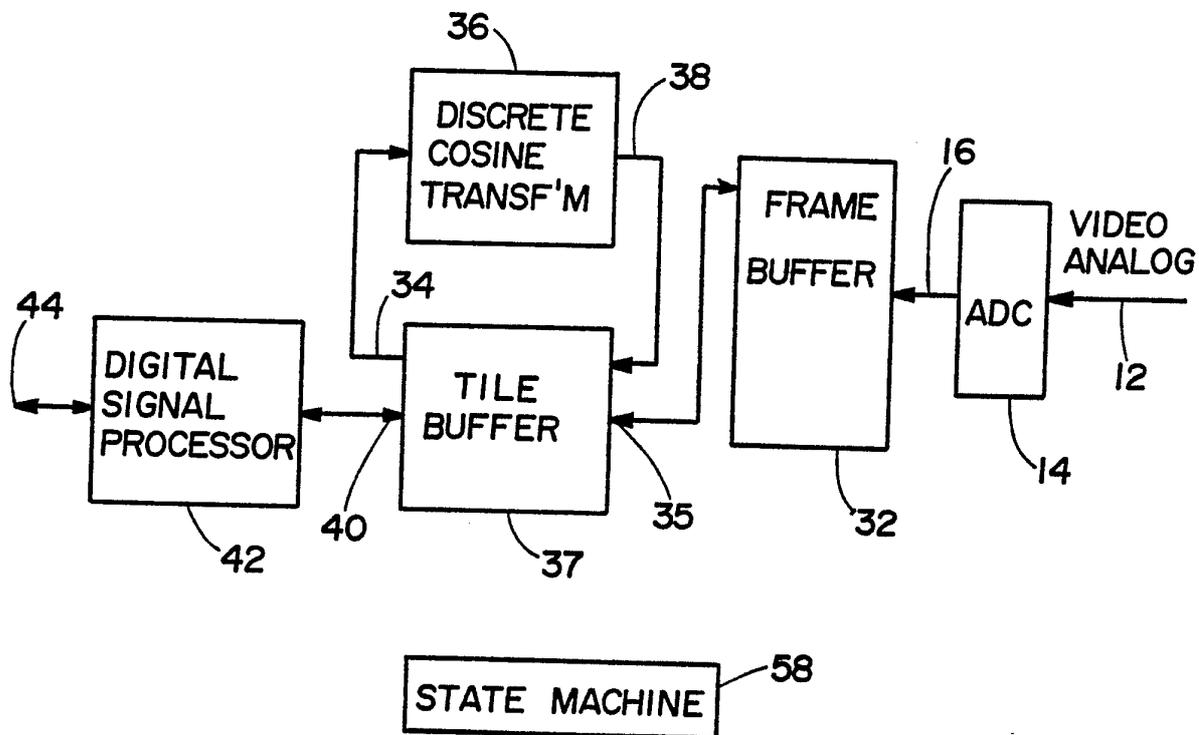
FIGURE 1

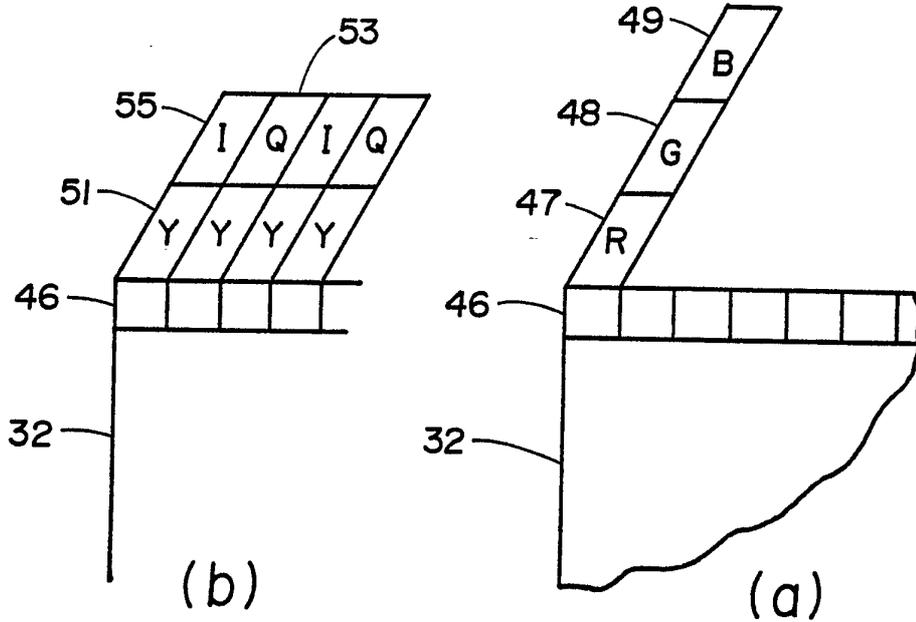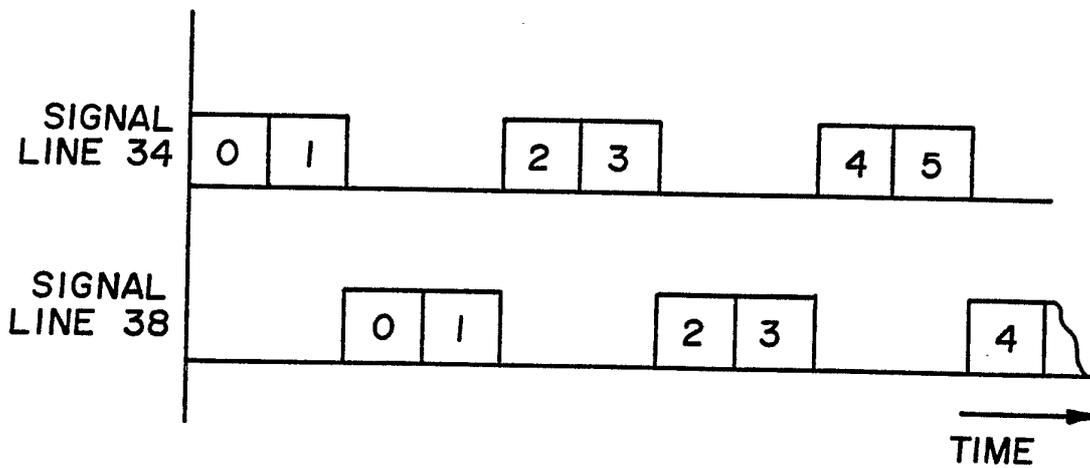FIGURE 2

FIGURE 3

FIGURE 4

3/5.
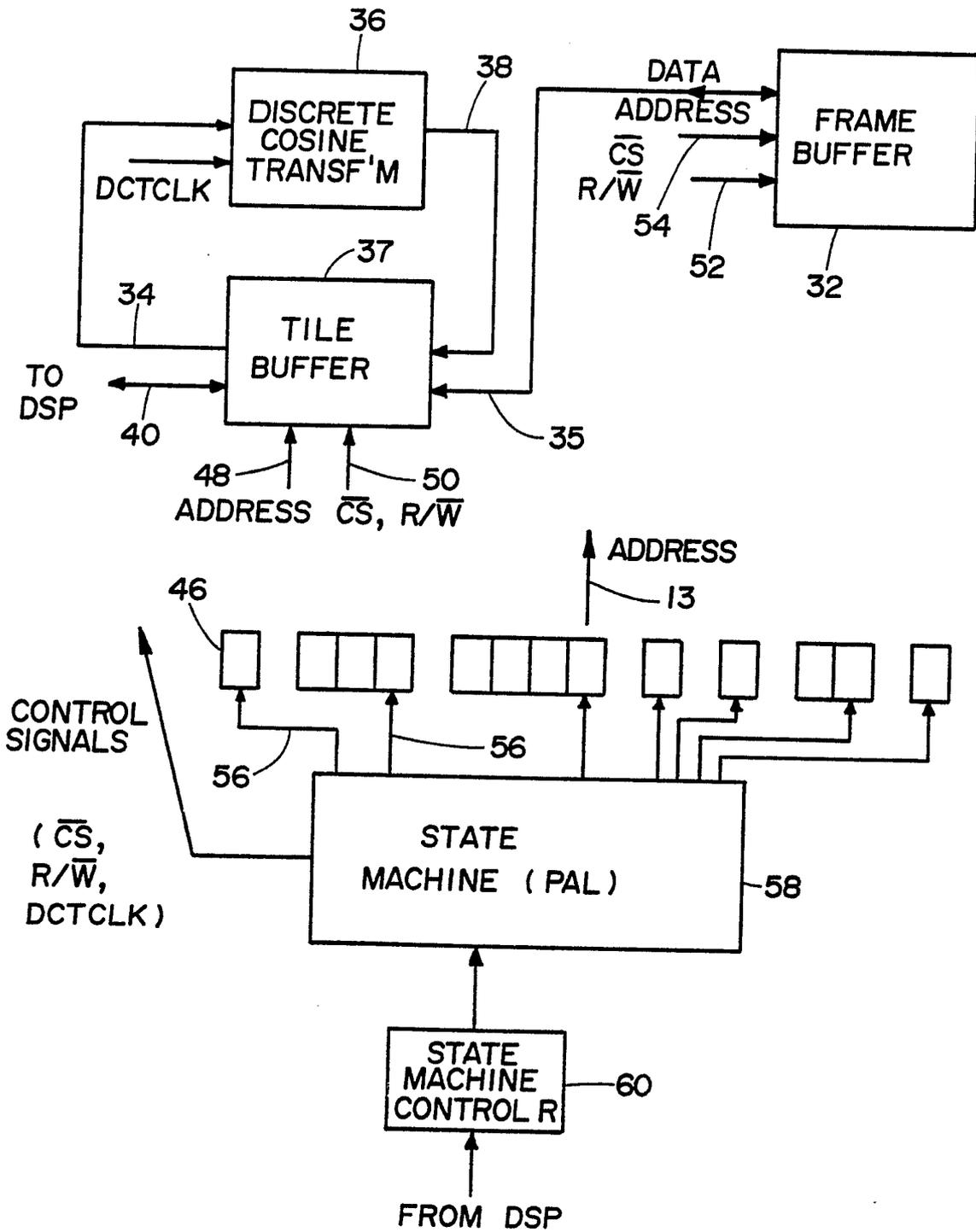
FIGURE 5

ADDRESS BIT	12	11	10	9	8	7	6	5	4	3	2	1	0
FB TRANSFER	W	R	R	R	T	T	T	T	T	T	C	C	C
Y DCT TRANSFER	W	R	R	R	T	T	T	T	T	T	C	C	C
I DCT TRANSFER	W	R	R	R	T	T	T	T	T	C	C	C	Ø
Q DCT TRANSFER	W	R	R	R	T	T	T	T	T	C	C	C	1
INCREMENT PULSES	6			5				4	3	2		1	0

W = WRITE FIELD

R = ROW FIELD
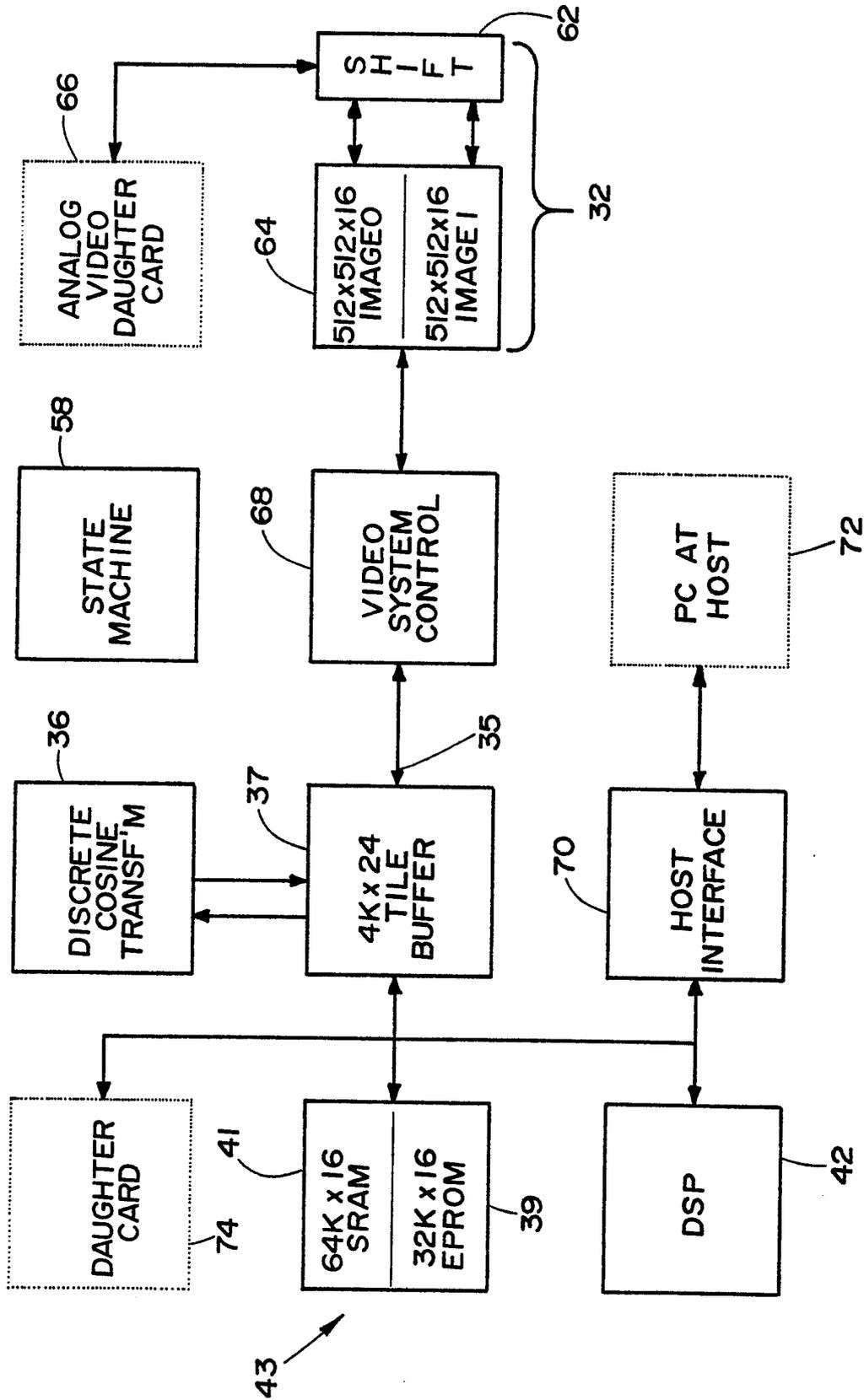
T = TILE FIELD

C = COLUMN FIELD

FIGURE 6

FIGURE 7

INTERNATIONAL SEARCH REPORT

International Application No PCT/CA 90/00244

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 6

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC⁵: H 04 N 11/04

II. FIELDS SEARCHED

Minimum Documentation Searched 7

Classification System	Classification Symbols
IPC⁵	H 04 N

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched 8

III. DOCUMENTS CONSIDERED TO BE RELEVANT 9

Category *	Citation of Document, 11 with indication, where appropriate, of the relevant passages 12	Relevant to Claim No. 13
A	US, A, 4774587 (SCHMITT) 27 September 1988 see column 3, line 56 - column 4, line 31; figure 1 --	1,4,9,15, 18,21,22
A	US, A, 4772956 (ROCHE) 20 September 1988 see column 4, line 4 - column 5, line 36; figure 1 --	1,4,9,15,18, 21,22
A	EP, A, 0084270 (COMPRESSION LABS, INC.) 27 July 1983	

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* Special categories of cited documents: 10

"A" document defining the general state of the art which is not considered to be of particular relevance

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
4tn April 1991	15. 05. 91

International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	Weinberg

Form PCT/ISA/210 (second sheet) (January 1985)

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on 24/04/91
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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 4774587	27-09-88	None		
US-A- 4772956	20-09-88	None		
EP-A- 0084270	27-07-83	US-A- CA-A-	4541012 1209266	10-09-85 05-08-86

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